128K × 8 CMOS FLASH MEMORY

GENERAL DESCRIPTION

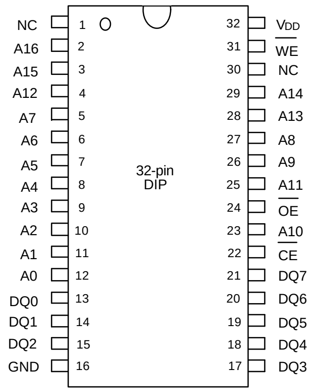
The W29EE012 is a 1-megabit, 5-volt only CMOS flash memory organized as 128K × 8 bits. The device can be programmed and erased in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W29EE012 results in fast program/erase operations with extremely low current consumption (compared to other comparable 5-volt flash memory products). The device can also be programmed and erased using standard EPROM programmers.

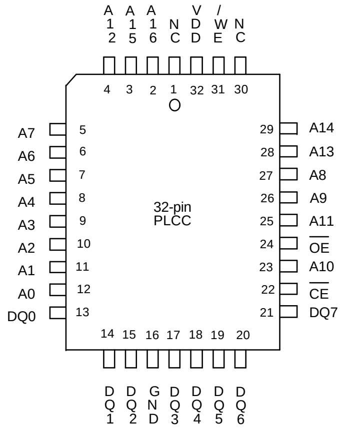
FEATURES

- Single 5-volt program and erase operations
- Fast page-write operations
  - 128 bytes per page
  - Page program cycle: 10 mS (max.)
  - Effective byte-program cycle time: 39 µS
  - Optional software-protected data write
- Fast chip-erase operation: 50 mS
- Read access time: 90/120/150 nS
- Page program/erase cycles: 1,000
- Ten-year data retention
- Software and hardware data protection
- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 µA (typ.)
- Automatic program timing with internal V_{PP} generation
- End of program detection
  - Toggle bit
  - Data polling
- Latched address and data
- TTL compatible I/O
- JEDEC standard byte-wide pinouts

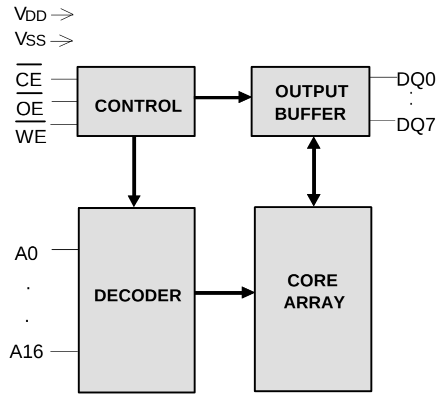
  Available packages: 32-pin 600 mil DIP, 450 mil SOP and PLCC

PIN CONFIGURATIONS





BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0–A16	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
VDD	Power Supply
GND	Ground
NC	No Connection

FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W29EE012 is controlled by $\overline{CE}$ and $\overline{OE}$, both of which have to be low for the host to obtain data from the outputs. $\overline{CE}$ is used for device selection. When $\overline{CE}$ is high, the chip is de-selected and only standby power will be consumed. $\overline{OE}$ is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. Refer to the timing waveforms for further details.

Page Write Mode

The W29EE012 is programmed on a page basis. Every page contains 128 bytes of data. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded will be erased to "FFh" during programming of the page.

The write operation is initiated by forcing $\overline{CE}$ and $\overline{WE}$ low and $\overline{OE}$ high. The write procedure consists of two steps. Step 1 is the byte-load cycle, in which the host writes to the page buffer of the device. Step 2 is an internal programming cycle, during which the data in the page buffers are simultaneously written into the memory array for non-volatile storage.

During the byte-load cycle, the addresses are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. If the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 200 µS, after the initial byte-load cycle, the W29EE012 will stay in the page load cycle. Additional bytes can then be loaded consecutively. The page load cycle will be terminated and the internal programming cycle will start if no additional byte is loaded into the page buffer within 300 µS (T_{BLCO}) from the last byte-load cycle, i.e., there is no subsequent $\overline{WE}$ high-to-low transition after the last rising edge of $\overline{WE}$. A_7 to A_{16} specify the page address. All bytes that are loaded into the page buffer must have the same page address. A_0 to A_6 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

In the internal programming cycle, all data in the page buffers, i.e., 128 bytes of data, are written simultaneously into the memory array. Before the completion of the internal programming cycle, the host is free to perform other tasks such as fetching data from other locations in the system to prepare to write the next page.

Software-protected Data Write

The device provides a JEDEC-approved optional software-protected data write. Once this scheme is enabled, any write operation requires a series of three-byte program commands (with specific data to a specific address) to be performed before the data load operation. The three-byte load command sequence begins the page load cycle, without which the write operation will not be activated. This write scheme provides optimal protection against inadvertent write cycles, such as cycles triggered by noise during system power-up and power-down.

The W29EE012 is shipped with the software data unprotection enabled. To enable the software data protection scheme, perform the three-byte command cycle at the beginning of a page load cycle. The device will then enter the software data protection mode, and any subsequent write operation must be preceded by the three-byte program command cycle. Once enabled, the software data protection will remain enabled unless the disable commands are issued. A power transition will not reset the software data protection feature. To reset the device to unprotected mode, a six-byte command sequence is required. See Table 3 for specific codes and Figure 10 for the timing diagram.

Hardware Data Protection

The integrity of the data stored in the W29EE012 is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A $\overline{\text{WE}}$ pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The programming operation is inhibited when V_{DD} is less than 3.8V.

(3) Write Inhibit Mode: Forcing $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high, or $\overline{\text{WE}}$ high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

Data Polling (DQ_7)-Write Status Detection

The W29EE012 includes a data polling feature to indicate the end of a programming cycle. When the W29EE012 is in the internal programming cycle, any attempt to read DQ_7 of the last byte loaded during the page/byte-load cycle will receive the complement of the true data. Once the programming cycle is completed. DQ_7 will show the true data.

Toggle Bit (DQ_6)-Write Status Detection

In addition to data polling, the W29EE012 provides another method for determining the end of a program cycle. During the internal programming cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's. When the programming cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation.

5-Volt-Only Software Chip Erase

The chip-erase mode can be initiated by a six-byte command sequence. After the command loading cycles, the device enters the internal chip erase mode, which is automatically timed and will be completed in 50 mS. The host system is not required to provide any control or timing during this operation.

Product Identification

The product ID operation outputs the manufacturer code and device code. Programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed by software or hardware operation. In the software access mode, a six-byte command sequence can be used to access the product ID. A read from address 0000H outputs the manufacturer code (DAh). A read from address 0001H outputs the device code (C1h). The product ID operation can be terminated by a three-byte command sequence.

In the hardware access mode, access to the product ID is activated by forcing $\overline{\text{CE}}$ and $\overline{\text{OE}}$ low, $\overline{\text{WE}}$ high, and raising A9 to 12 volts.

TABLE OF OPERATING MODES

Operating Mode Selection

Operating Range = 0 to 70°C (Ambient Temperature), VDD = 5V ±10%, VSS = 0V, VHH = 12V

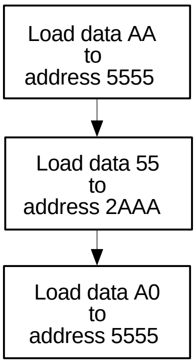
MODE	**PINS**				
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	**ADDRESS**	**DQ.**
Read	VIL	VIL	VIH	AIN	Dout
Write	VIL	VIH	VIL	AIN	Din
Standby	VIH	X	X	X	High Z
Write Inhibit	X	VIL	X	X	High Z/DOUT
	X	X	VIH	X	High Z/DOUT
Output Disable	X	VIH	X	X	High Z
5-Volt Software Chip Erase	VIL	VIH	VIL	AIN	DIN
Product ID	VIL	VIL	VIH	A0 = VIL; A1-A16 = VIL; A9 = VHH	Manufacturer Code DA (Hex)
	VIL	VIL	VIH	A0 = VIH; A1-A16 = VIL; A9 = VHH	Device Code C1 (Hex)

Command Codes for Software Data Protection

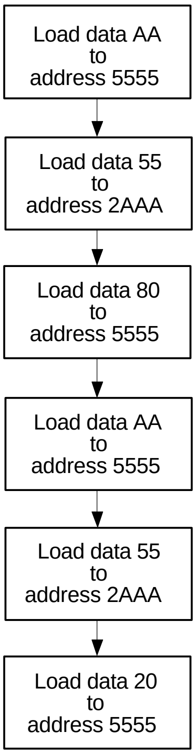
BYTE SEQUENCE	TO ENABLE PROTECTION		TO DISABLE PROTECTION	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	A0H	5555H	80H
3 Write	-	-	5555H	AAH
4 Write	-	-	2AAAH	55H
5 Write	-	-	5555H	20H

Sofware Data Protection Acquisition Flow

Software Data Protection Enable Flow



Software Data Protection Disable Flow



Notes for software program code:

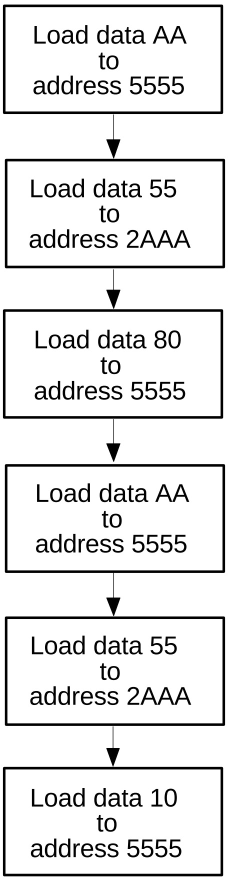
Data Format: DQ7–DQ0 (Hex)

Address Format: A14–A0 (Hex)

Command Codes for Software Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	80H
3 Write	5555H	AAH
4 Write	2AAAH	55H
5 Write	5555H	10H

Sofware Chip Erase Acquisition Flow



Notes for software chip erase:

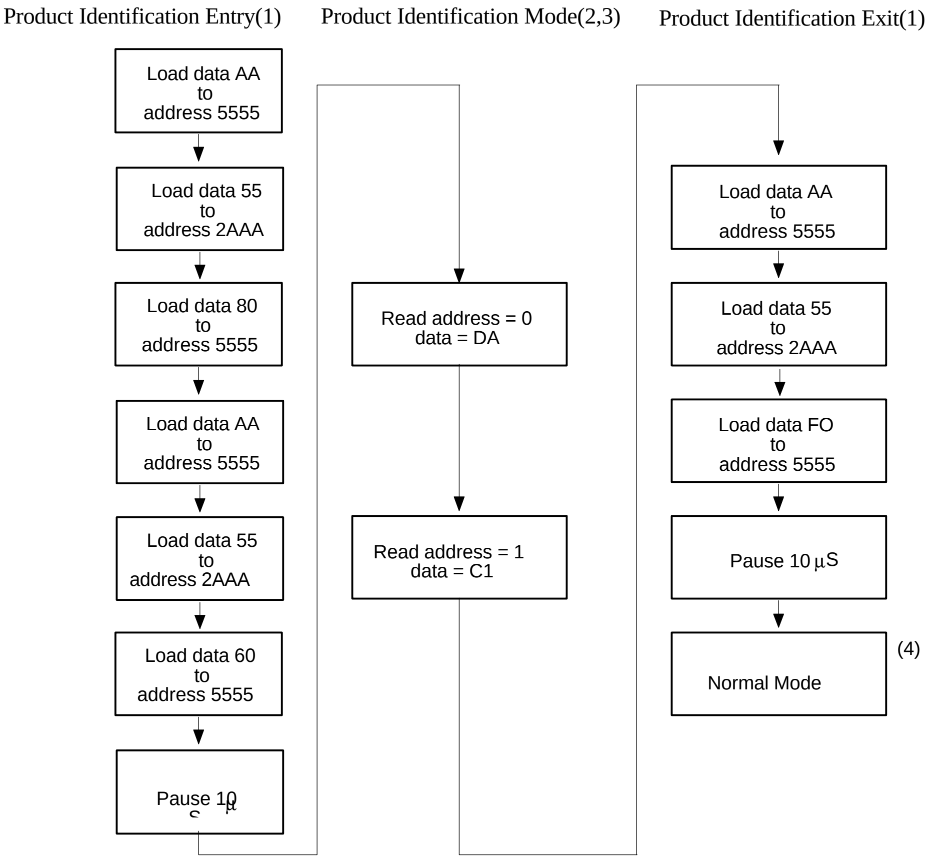
Data Format: DQ7–DQ0 (Hex)

Address Format: A14–A0 (Hex)

Command Codes for Product Identification

BYTE SEQUENCE	SOFTWARE PRODUCT IDENTIFICATION ENTRY		SOFTWARE PRODUCT IDENTIFICATION EXIT	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	80H	5555H	F0H
3 Write	5555H	AAH	-	-
4 Write	2AAAH	55H	-	-
5 Write	5555H	60H	-	-
	Pause 10 µS		Pause 10 µS	

Software Product Identification Acquisition Flow



Notes for software product identification:

(1) Data format: DQ7–DQ0 (Hex); address format: A14–A0 (Hex).

(2) A1–A16 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification mode if power down.

(4) The device returns to standard operation mode.

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential except $\overline{OE}$	-0.5 to V_{DD} +1.0	V
Transient Voltage (?20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on $\overline{OE}$ Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, all I/Os open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	-	50	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	$\overline{CE}$ = V_{IH}, all I/Os open Other inputs = V_{IL}/V_{IH}	-	2	3	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	$\overline{CE}$ = V_{DD} -0.3V, all I/Os open Other inputs = V_{DD} -0.3V/GND	-	20	100	µA
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{DD}	-	-	1	µA
Output Leakage Current	I_{LO}	V_{IN} = GND to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	V_{DD} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	$T_{PU.READ}$	100	µS
Power-up to Write Operation	$T_{PU.WRITE}$	5	mS

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	12	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF

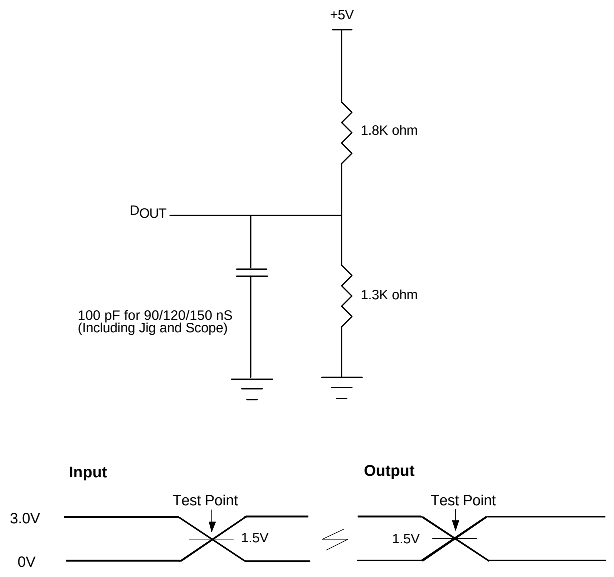
AC CHARACTERISTICS

AC Test Conditions

(V_{DD} = 5V ±10%)

PARAMETER	CONDITIONS	
	90 nS/120 nS	150 nS
Input Pulse Levels	0V/3V	0V/3V
Input Rise/Fall Time	5 nS	10 nS
Input/Output Timing Level	1.5V/1.5V	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 100 pF	1 TTL Gate and C_L = 100 pF

AC Test Load and Waveforms



Read Cycle Timing Parameters

(VDD = 5.0V ±10%, VSS = 0V, TA = 0 to 70° C)

PARAMETER	SYM.	W29EE012-90		W29EE012-12		W29EE012-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	90	-	120	-	150	-	nS
Chip Enable Access Time	TCE	-	90	-	120	-	150	nS
Address Access Time	TAA	-	90	-	120	-	150	nS
Output Enable Access Time	TOE	-	45	-	60	-	70	nS
$\overline{\text{CE}}$ Low to Active Output	TCLZ	0	-	0	-	0	-	nS
$\overline{\text{OE}}$ Low to Active Output	TOLZ	0	-	0	-	0	-	nS
$\overline{\text{CE}}$ High to High-Z Output	TCHZ	-	45	-	45	-	45	nS
$\overline{\text{OE}}$ High to High-Z Output	TOHZ	-	45	-	45	-	45	nS
Output Hold from Address change	TOH	0	-	0	-	0	-	nS

Byte/Page-Write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Write Cycle (erase and program)	TWC	-	-	10	mS
Address Setup Time	TAS	0	-	-	nS
Address Hold Time	TAH	50	-	-	nS
$\overline{\text{WE}}$ and $\overline{\text{CE}}$ Setup Time	TCS	0	-	-	nS
$\overline{\text{WE}}$ and $\overline{\text{CE}}$ Hold Time	TCH	0	-	-	nS
$\overline{\text{OE}}$ High Setup Time	TOES	10	-	-	nS
$\overline{\text{OE}}$ High Hold Time	TOEH	10	-	-	nS
$\overline{\text{CE}}$ Pulse Width	TCP	70	-	-	nS
$\overline{\text{WE}}$ Pulse Width	TWP	70	-	-	nS
$\overline{\text{WE}}$ High Width	TWPH	150	-	-	nS
Data Setup Time	TDS	50	-	-	nS
Data Hold Time	TDH	10	-	-	nS
Byte Load Cycle Time	TBLC	0.22	-	200	µS
Byte Load Cycle Time-out	TBLCO	300	-	-	µS

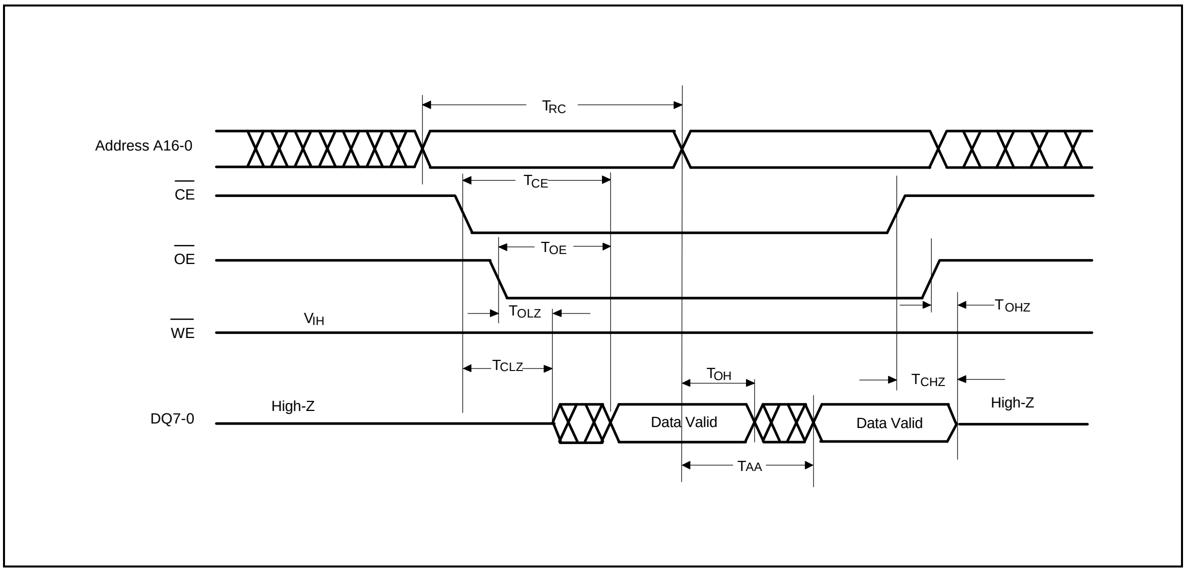
Note: All AC timing signals observe the following guidelines for determining setup and hold times:
(a) High level signal's reference level is VIH and (b) low level signal's reference level is VIL.

Data Polling and Toggle Bit Timing Parameters

PARAMETER	SYM.	W29EE012-90		W29EE012-12		W29EE012-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{\text{OE}}$ to Data Polling Output Delay	TOEP	-	45	-	60	-	70	nS
$\overline{\text{CE}}$ to Data Polling Output Delay	TCEP	-	90	-	120	-	150	nS
$\overline{\text{OE}}$ to Toggle Bit Output Delay	TOET	-	45	-	60	-	70	nS
$\overline{\text{CE}}$ to Toggle Bit Output Delay	TCET	-	90	-	120	-	150	nS

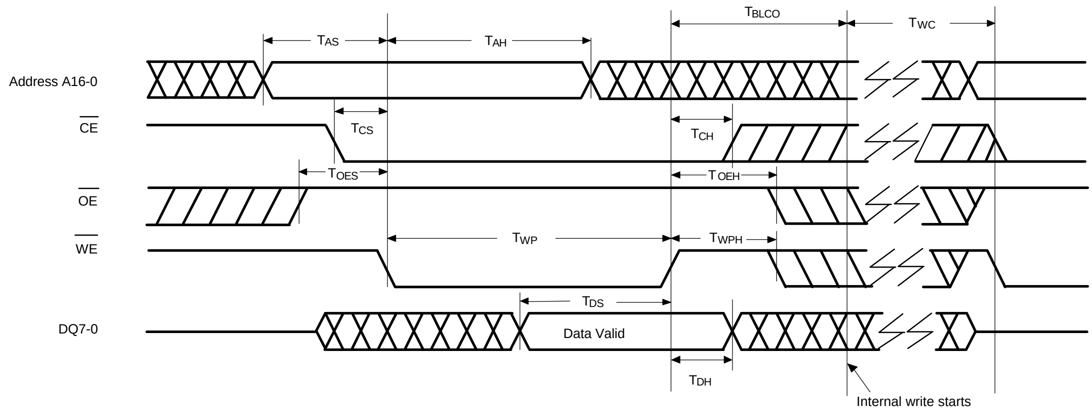
TIMING WAVEFORMS

Read Cycle Timing Diagram

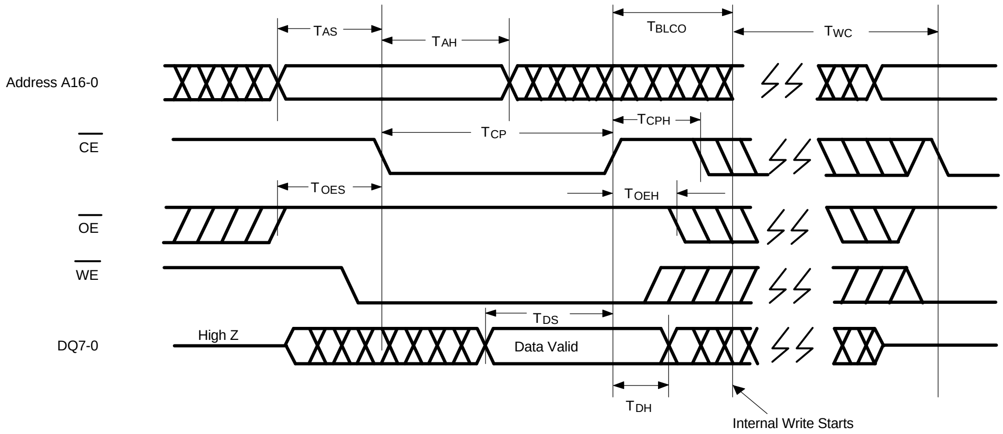


Timing Waveforms, continued

$\overline{\text{WE}}$ Controlled Write Cycle Timing Diagram

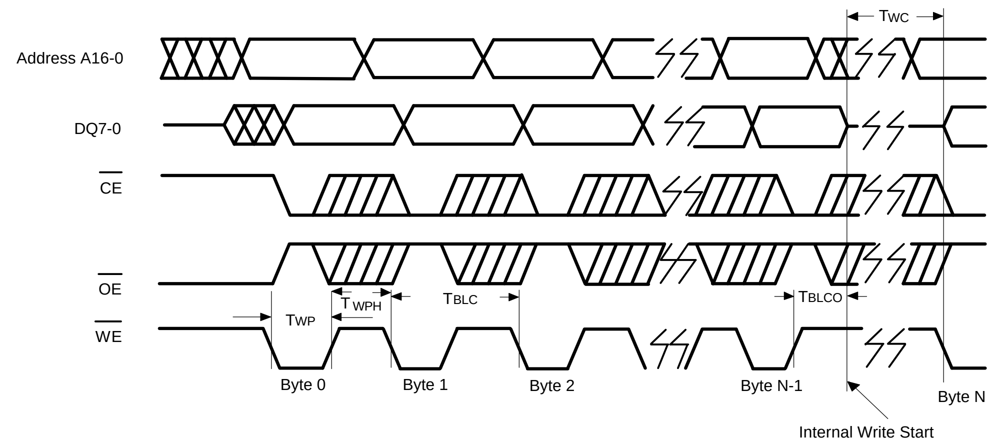


$\overline{\text{CE}}$ Controlled Write Cycle Timing Diagram

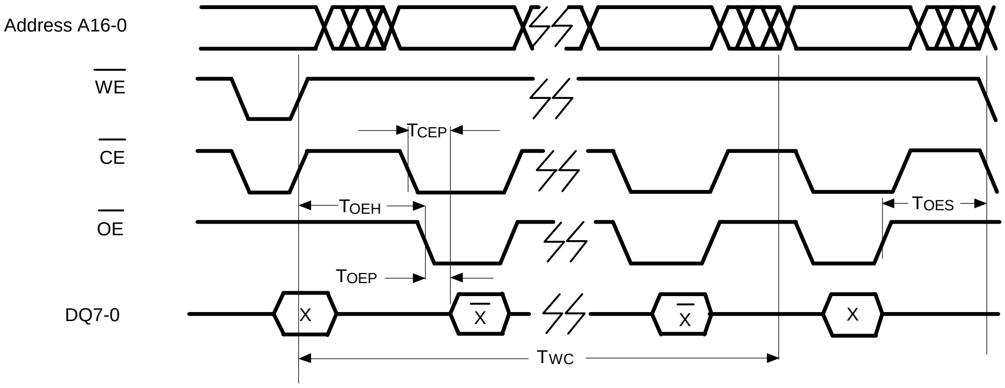


Timing Waveforms, continued

Page Write Cycle Timing Diagram

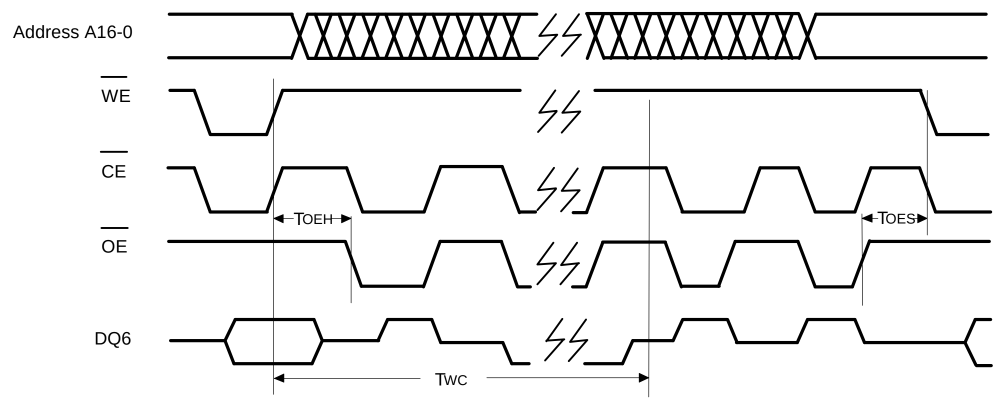


$\overline{\text{DATA}}$ Polling Timing Diagram

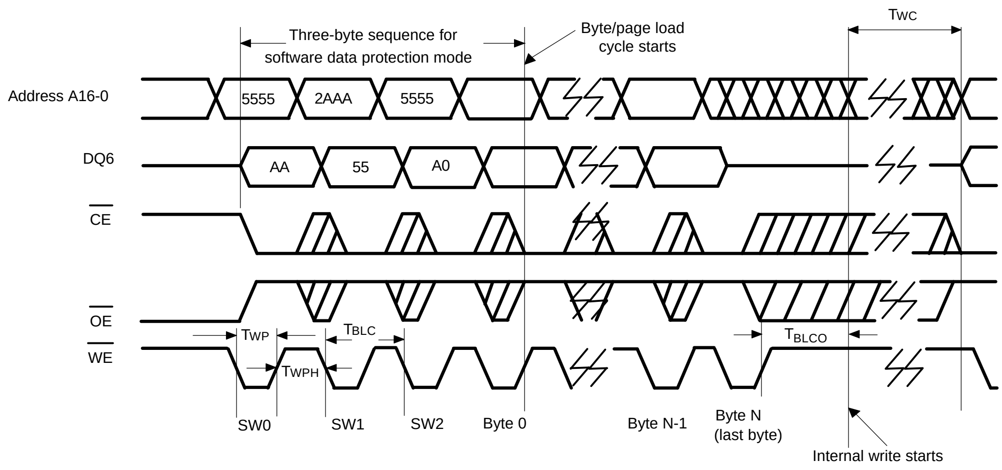


Timing Waveforms, continued

Toggle Bit Timing Diagram

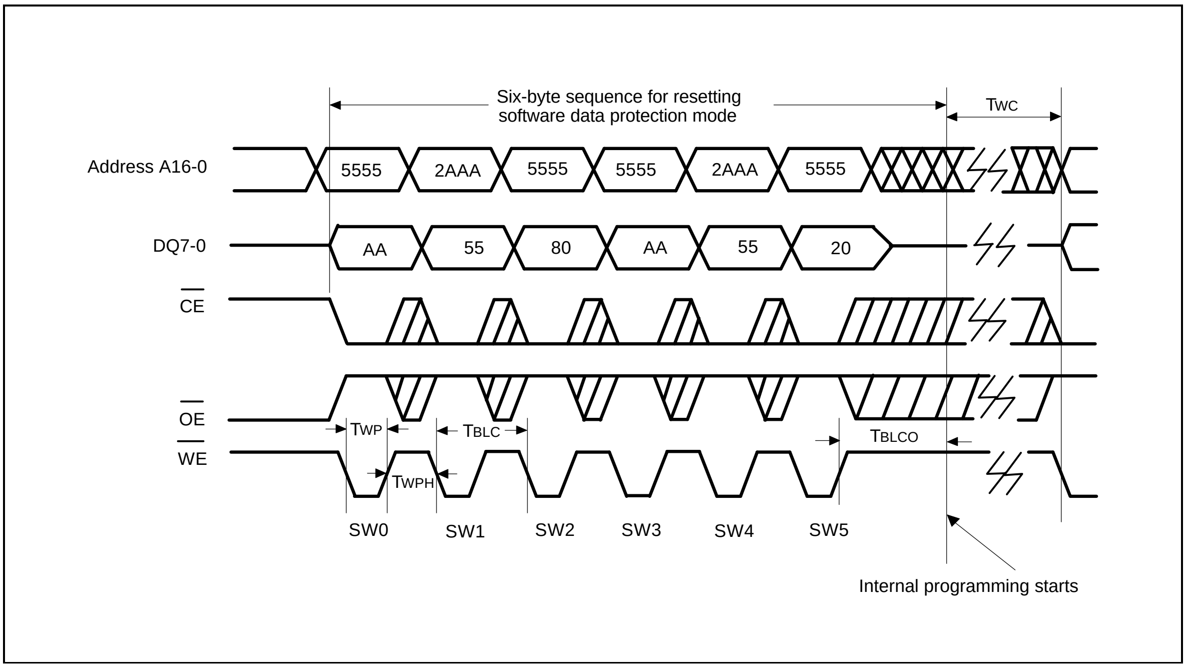


Page Write Timing Diagram Software Data Protection Mode

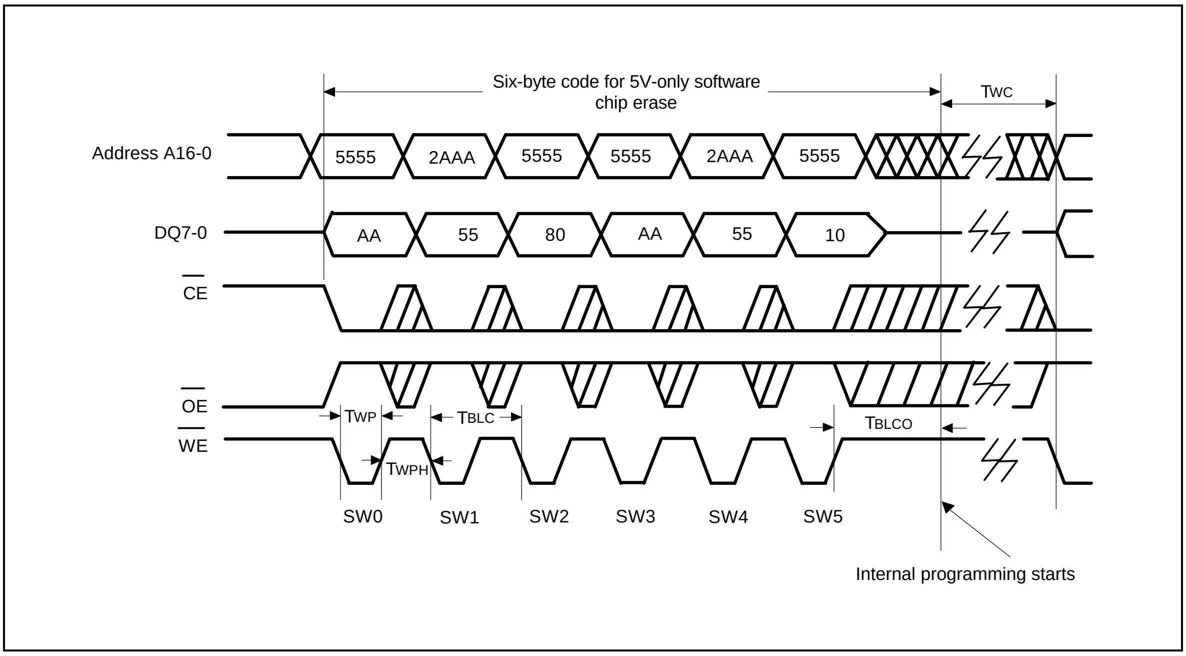


Timing Waveforms, continued

Reset Software Data Protection Timing Diagram



5 Volt-Only Software Chip Erase Timing Diagram



ORDERING INFORMATION

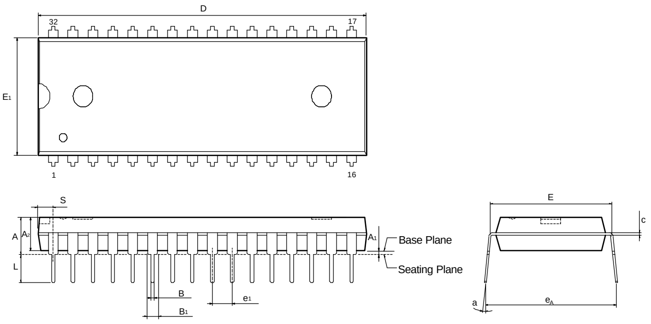
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (mA)	PACKAGE
W29EE012-90	90	50	100	600 mil DIP
W29EE012-12	120	50	100	600 mil DIP
W29EE012-15	150	50	100	600 mil DIP
W29EE012S-90	90	50	100	450 mil SOP
W29EE012S-12	120	50	100	450 mil SOP
W29EE012S-15	150	50	100	450 mil SOP
W29EE012P-90	90	50	100	32-pin PLCC
W29EE012P-12	120	50	100	32-pin PLCC
W29EE012P-15	150	50	100	32-pin PLCC

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-pin P-DIP

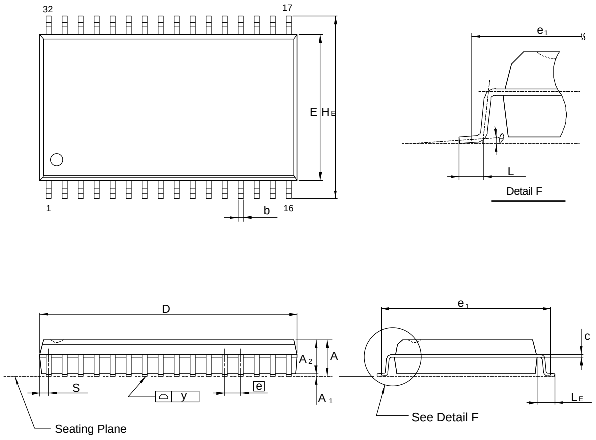


Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

32-pin SO Wide Body



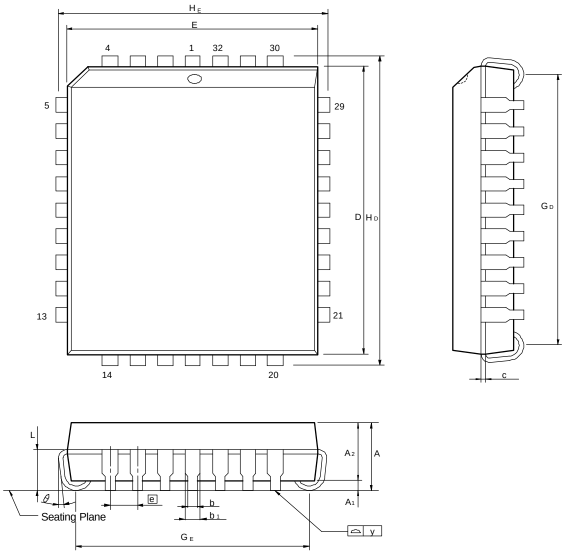
Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.118	—	—	3.00
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	—	0.805	0.817	—	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
$\boxed{e}$	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.546	0.556	0.556	13.87	14.12	14.38
L	0.023	0.031	0.039	0.58	0.79	0.99
L_E	0.047	0.055	0.063	1.19	1.40	1.60
S	—	—	0.036	—	—	0.91
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimensions D & E include mold mismatch and determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec should be based on final visual inspection spec.

Package Dimensions, continued

32-pin PLCC



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
$\boxed{e}$	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches.
4. General appearance spec. should be based on final visual inspection sepc.

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Jan. 1997		Initial Issued
A2	Apr. 2000	10	Modify V_{IH}/V_{IL} = 0V/3V and V_{OH}/V_{OL} = 1.5V/1.5V

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