Interfacing AT24CXX Serial EEPROMs with AT89CX051 Microcontrollers

Serial memory devices offer significant advantages over parallel devices in applications where lower data transfer rates are acceptable. In addition to requiring less board space, serial devices allow microcontroller I/O pins to be conserved. This is especially valuable when adding external memory to low pin count microcontrollers such as the Atmel AT89C1051 and AT89C2051.

This application note presents a suite of software routines which may be incorporated into a user's application to allow an AT89CX051 microcontroller to read and write AT24CXX serial EEPROMs. The software supports all members of the AT24CXX family, and may easily be modified for compatibility with any of the Atmel 8051-code compatible microcontrollers.

Hardware

A typical interconnection between an AT89CX051 microcontroller and an AT24CXX serial EEPROM is shown in Figure 1. As indicated in the figure, up to eight members of the AT24CXX family may share the bus, utilizing the same two microcontroller I/O pins. Each device on the bus must have its address inputs (A0, A1, A2) hard-wired to a unique address. In the figure, the first device recognizes address zero (A0, A1, A2 tied low), while the eighth recognizes address seven (A0, A1, A2 tied high). Not all members of the AT24CXX family recognize all three address inputs, limiting the number of some devices which may be present to less than eight. The exact number of devices of each type which may share the bus is shown in Table 1.

Bidirectional Data Transfer Protocol

The Bidirectional Data Transfer Protocol utilized by the AT24CXX family allows a number of compatible devices to share a

(continued)

Table 1. Atmel's 2-Wire Serial EEPROM Family

Device	Size (Bytes)	Page Size (Bytes)	Max Per Bus	Addresses Used
AT24C01	1K	8	1	None
AT24C01A	1K	8	8	A0, A1, A2
AT24C02	2K	8	8	A0, A1, A2
AT24C04	4K	16	4	A1, A2
AT24C08	8K	16	2	A2
AT24C16	16K	16	1	None
AT24C164	16K	16	8	A0, A1, A2
AT24C32	32K	32	8	A0, A1, A2
AT24C64	64K	32	8	A0, A1, A2

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Application Note

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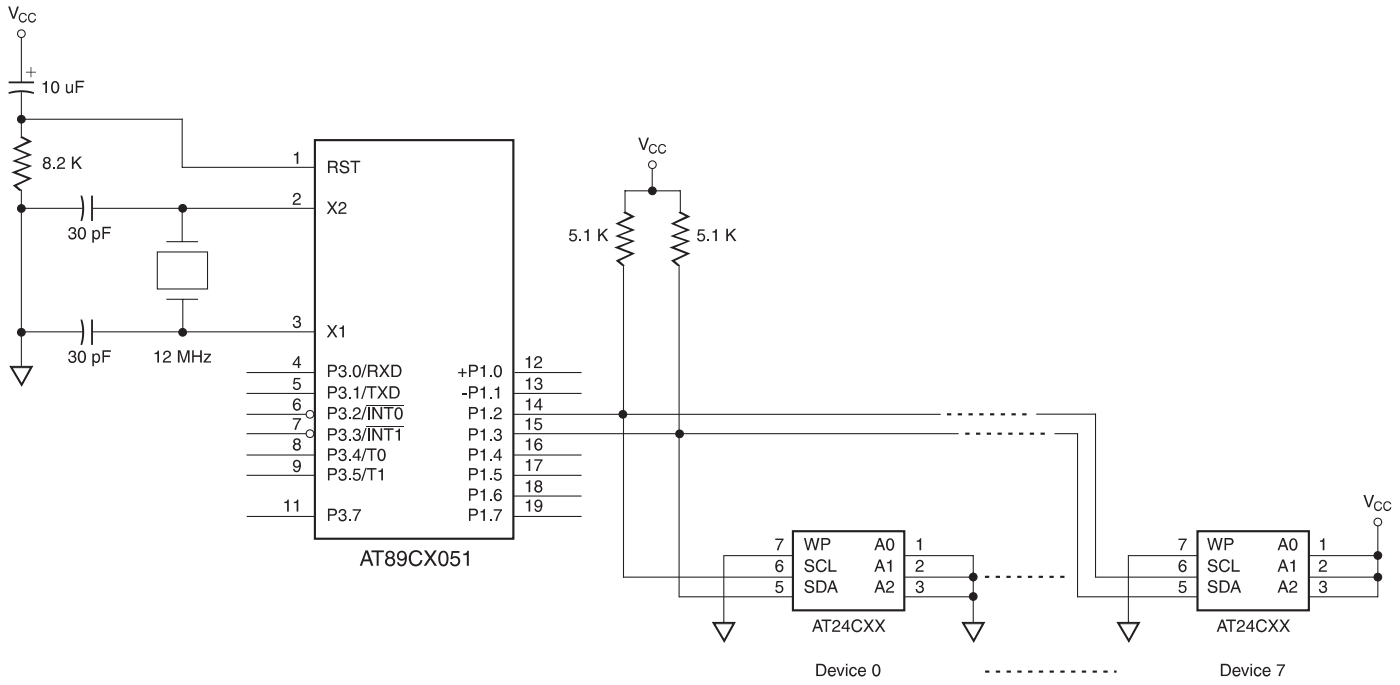
Figure 1. Typical Circuit Configuration



common 2-wire bus. The bus consists of a serial clock (SCL) line and a serial data (SDA) line. The clock is generated by the bus master and data is transmitted serially on the data line, most significant bit first, synchronized to the clock. The protocol supports bidirectional data transfers in 8-bit bytes.

In this application, the microcontroller serves as the bus master, initiating all data transfers and generating the clock which regulates the flow of data. The serial devices present on the bus are considered slaves, accepting or sending data in response to orders from the master.

The bus master initiates a data transfer by generating a start condition on the bus. This is followed by transmission of a byte containing the device address of the intended recipient. The device address consists of a 4-bit fixed portion and a 3-bit programmable portion. The fixed portion must match the value hard-wired into the slave, while the programmable portion allows the master to select between a maximum of eight slaves of similar type on the bus.

AT24CXX serial EEPROMs respond to device addresses with a fixed portion equal to ‘1010’ and a programmable portion matching the address inputs (A0, A1, A2). Not all members of the AT24CXX family examine all three address inputs; Table 1 shows which of the three address inputs are valid for each member of the family.

The eighth bit in the device address byte specifies a write or read operation. After the eighth bit is transmitted, the master releases the data line and generates a ninth clock. If a slave has recognized the transmitted device address, it will respond to the ninth clock by generating an acknowledge condition on the data line. A slave which is busy when addressed may not generate an acknowledge. This is true for the AT24CXX when a write operation is in progress.

Following receipt of the slave’s address acknowledgment, the master continues with the data transfer. If a write operation has been ordered, the master transmits the remaining data, with the slave acknowledging receipt of each byte. If the master has ordered a read operation, it releases the data line and clocks in data sent by the slave. After each byte is received, the master generates an acknowledge condition on the bus. The acknowledge is omitted following receipt of the last byte. The master terminates all operations by generating a stop condition on the bus. The master may also abort a data transfer at any time by generating a stop condition.

Refer to the AT24CXX family data sheets for detailed information on AT24CXX device operation and Bidirectional Data Transfer Protocol bus timing.

The software for this application may be obtained by downloading from Atmel’s Web Site or BBS: (408) 436-4309. Consult the comment block at the beginning of the source code file for detailed information on features and operation.

Web Site: http://www.atmel.com

BBS: 1-(408) 436-4309