Enhancing the Performance of Serial CMOS EEPROMs

Fairchild
Application Note 822

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INTRODUCTION

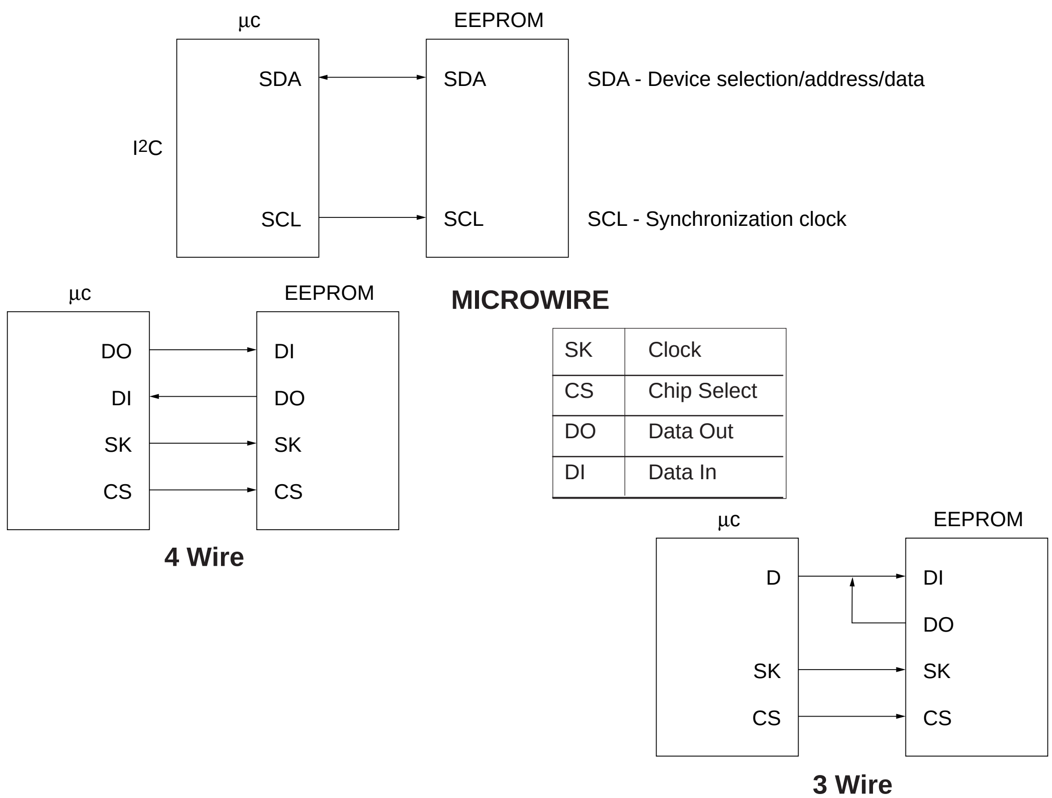
This application note presents a number of solutions to help a system designer overcome some possible limitations of serial Electrically Erasable PROMs (EEPROMs) to obtain greater system performance and flexibility.

This note assumes that the reader is familiar with Fairchild Semiconductor's range of MICROWIRE EEPROMs (NM93Cxx and NM93CSxx) and I^2C (NM24Cxx) devices.

1.0 COMPARING SERIAL EEPROM INTERFACE STANDARDS

The two industry standard serial interfaces for EEPROMs are the MICROWIRE and I^2C-bus specifications. The key features of these two interfaces are shown in Figure 1.

Serial Interface Standards



	MICROWIRE	I^2C
Max Bus Speed	1 MHz	100 kHz
Number of Active Pins	4	2
Maximum Memory	N/A	16 kbit
Acknowledge	No	Yes
Data Size	8- or 16-Bit	8-Bit
Block Write	No	Yes
Sequential Read	Yes	Yes
Number of Devices on Bus	Limited by Port Pins	32 Functions, 256 Total Devices

FIGURE 1. MICROWIRE vs I^2C

The key advantages of the MICROWIRE interface compared to the I^2C-bus are:

- Higher system speed (1 MHz vs 100 kHz)
- Greater memory size (unlimited vs 16 kbit maximum)
- Address programming pins are not required on peripherals

The key advantages of the I^2C-bus are:

- Only requires 2 pins (SDA and SCL)

- Allows easy implementation of a multi-master system

Both interface standards are supported by a variety of microcomputers; some have dedicated interfaces built-in (for example Fairchild Semiconductor's COPS™), while other microcomputers can interface to either standard by toggling I/O port pins as required.

2.0 I 2 C-BUS MEMORY SIZE

2.1 I 2 C-Bus Concept

The I 2 C-bus uses two wires, serial data (SDA) and serial clock (SCL) to carry information between various integrated circuits connected to the bus. Each device is recognized by a unique address and can operate as either a transmitter or receiver depending on the function of the individual device. A typical I^2C-bus system is shown in Figure 2.

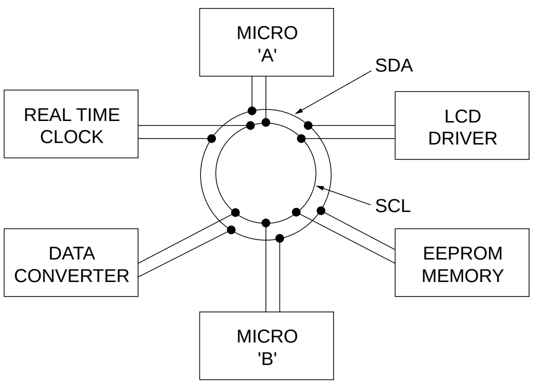


FIGURE 2. A Typical I 2 C-Bus System

In addition to transmitters and receivers, devices can also be defined as masters or slaves when performing data transfers.

A master is: — the device which initiates data transfer
— generates clock signals
— terminates a data transfer
— e.g., a microcomputer

A slave is: — the device addressed by a master
— e.g., a memory

Note: The I^2C-bus is a multi-master bus; each master generates its own clock signals when transferring data on the bus.

2.2 EEPROM Memory on the I^2C-Bus

The I^2C-bus specification allows a maximum of 16 kbits of EEPROM. The 4-bit device type identifier string which follows the START condition is 1010 for EEPROMs. Fairchild Semiconductor manufactures a range of different size I^2C EEPROMs (2k, 4k, 8k, and 16 kbits) to allow a system designer to select the amount of memory required.

EEPROMs on the I^2C-bus may be configured in any manner required, providing the total memory addressed does not exceed 16 kbits. EEPROM memory Addressing is controlled by two methods:

- Hardware configuring the A0, A1, and A2 pins (device address pins) with pull-up or pull-down resistors
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the slave address string)

Pin Descriptions

Serial Clock (**SCL**) an input used to clock data into and out of the memory

Serial Data (**SDA**) a bidirectional pin used to transfer data into and out of the device

Device Address Inputs connected to V_{CC} or V_{SS} to configure EEPROM address

Device	A0	A1	A2	Effect of Address	
NM24C02/03	ADR	ADR	ADR	$2^3 = 8$;	8 x (1x2K) = 16K
NM24C04/05	X	ADR	ADR	$2^2 = 4$;	4 x (2x2K) = 16K
NM24C08/09	X	X	ADR	$2^1 = 2$;	2 x (4x2K) = 16K
NM24C16/17	X	X	X	$2^0 = 1$;	1 x (8x2K) = 16K

ADR—active pin used for device addressing

X —not used for addressing (must be tied to ground/V_{SS})

Many applications now require greater than 16 kbits of EEPROM on an I^2C system. For the purpose of this application note we will consider how to use multiple 16 kbit (NM24C16/17) devices in an I^2C bus system to increase the total memory size.

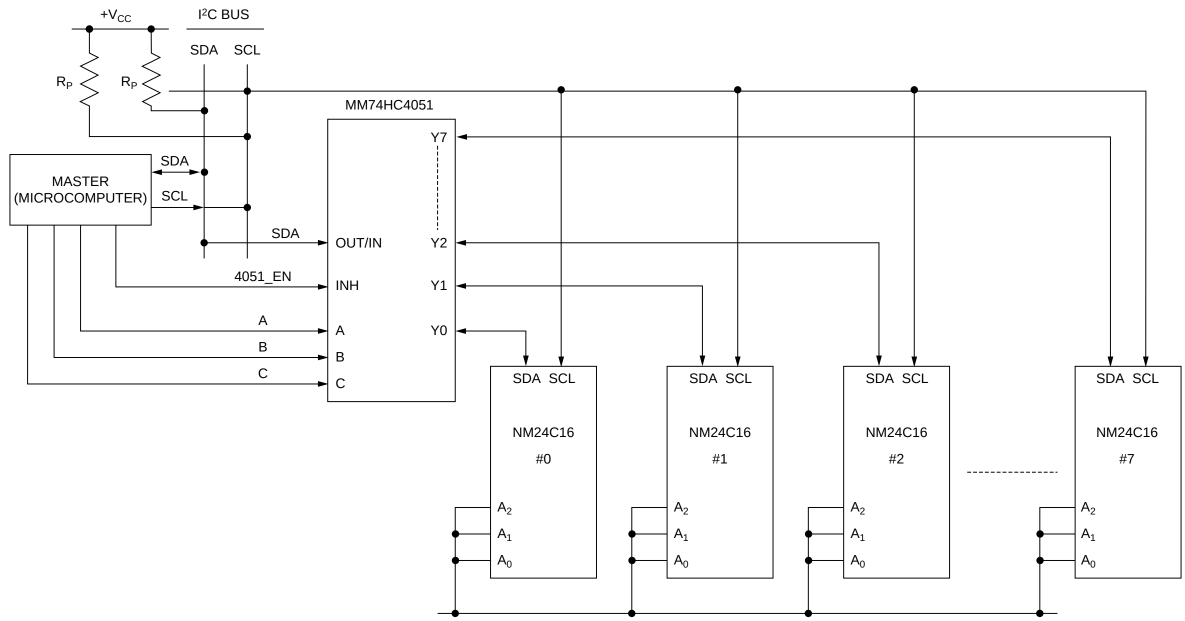


FIGURE 3. Increasing I²C-Bus EEPROM → 16 kbits

2.3 Bank Switching I²C EEPROMs

A circuit to increase the EEPROM memory size of the I²C bus, while still maintaining full software and hardware compatibility, is shown in Figure 3.

The circuit connects the serial clock (SCL) to each memory device, but the serial data (SDA) is connected by a multiplexed, bidirectional analog switch (MM74HC4051). The MM74HC4051 is an 8-channel analog multiplexer which connects together the outputs of 8 digitally controlled analog switches, thus achieving an 8-channel multiplexer. These switches are bidirectional, allowing any analog input to be used as an output and vice-versa. They have a low "on" resistance, typically 50W or less.

The MM74HC4051 is controlled by four inputs; INH which enables the switches to be "on" and inputs A, B and C which select one of the eight switches. The master (microcontroller) generates these four control signals to the MM74HC4051 directly.

In this case a typical software flow would be:

— set microcontroller port pins to select the NM24C16/17 required

— [DEVICE TYPE] → [DEVICE ADDRESS] → [PAGE BLOCK ADDRESS] → [BYTE ADDRESS]

This means that this low cost solution still maintains full I²C-bus compatibility.

Worst Case Analysis

I²C-Bus Specification	MM74HC4051 Solution Specification
C_{max} = 400 pF (Note 1) f_{max} = 100 kHz (Note 2) = 10 µs Period	C_{IN} = 90 pF max t_{PD} = 15 ns max = 5 ns typical

*

Note 1: The maximum number of devices connected to the I²C-bus is controlled by the maximum allowable capacitance which is 400 pF per line.

Note 2: The maximum I²C system clock is 100 kHz. The propagation delay through the MM74HC4051 is small enough to ensure that data set-up time of 250 ns min is not violated.

3.0 ACCESSING SERIAL EEPROMs

3.1 I^2C System

READ Operations

3.1.1 Random Read

Random read allows the master to access any memory location in a random manner. The master first performs a "dummy" write operation, then issues a start condition followed by the slave address and then the word address to be read. (See Figure 4.)

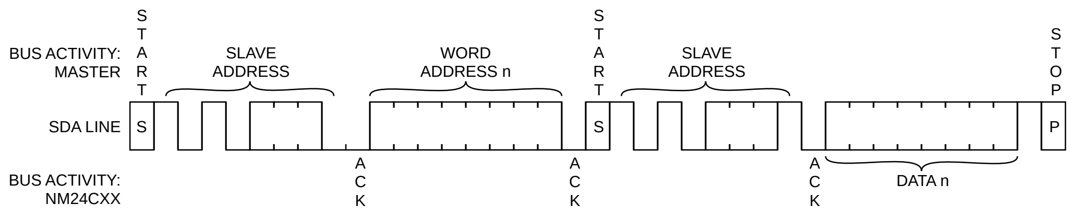


FIGURE 4. Random Read

3.1.2 Sequential Read

A sequential read operation allows the master to read a continuous stream of data from the memory without having to keep clocking in the word address and waiting for the memory to assert the ACK signal.

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as normal, however, the master now responds with an acknowledge (ACK) to indicate that it requires additional data. The memory continues to output data for each ACK received until the master does not send an ACK and generates a STOP condition.

The address counter increments all word address bits, allowing the entire memory contents to be read during one operation. When the top memory address is reached then the counter "rolls-over" to zero and continues counting. (See Figure 5.)

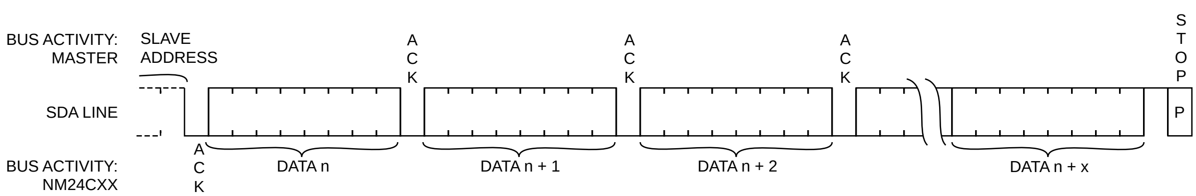


FIGURE 5. Sequential Read

3.1.3 Current Address Read

Internally the NM24Cxx devices contain an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+ 1, without the need for the master to transmit the 8-bit word address and then wait for the NM24Cxx acknowledge signal before transmitting the data. (See Figure 6.)

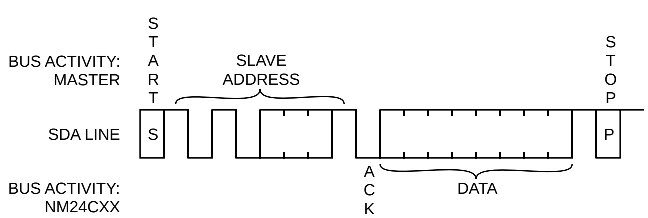


FIGURE 6. Current Address Read

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Write Operations

3.1.4 Byte Write

The normal write sequence is shown in Figure 7.

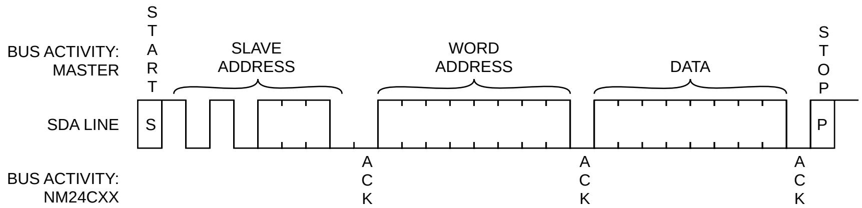


FIGURE 7. Byte Write

The master clocks the data into the NM24Cxx, and upon receipt of the ACK generates a STOP condition, at which time the NM24Cxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Cxx inputs are disabled, and the device will not respond to any requests from the master.

All NM24Cxx EEPROMs have a Write cycle time of T_{wr} = 10 ms MAXIMUM for 5V systems.

3.1.5 Page Write

The NM24Cxx devices are capable of a sixteen byte page write. The master starts the operation in the same manner as the byte write but instead of terminating it continues to transmit up to fifteen more words. The internal address counter in the memory automatically increments to the next address. When the master has finished writing data to the memory, it terminates the write cycle in the usual way when an internal write cycle occurs in the memory.

This method results in a single T_{wr} delay instead of sixteen. This is useful for applications such as saving data after detecting a power failure when speed of writing is critical.

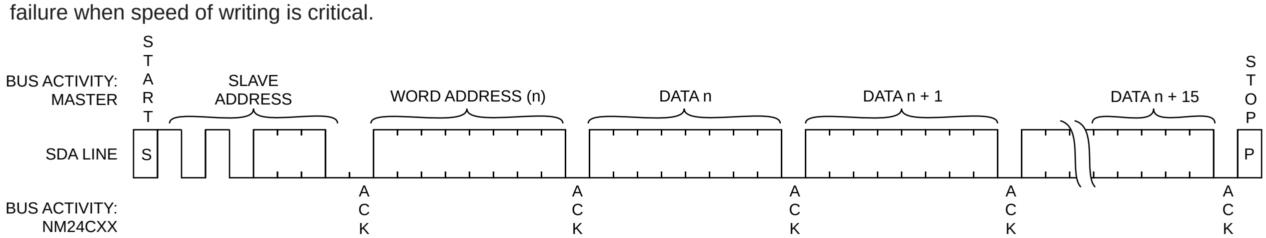


FIGURE 8. Page Write

3.1.6 Typical T_{wr} vs Maximum T_{wr}

Good design practice recommends using “worst-case” timing calculations rather than typical figures. After a master had initiated an internal write cycle in the memory there are two options before the next cycle can begin:

1. Master waits Twr MAX = 10 ms

   — this ensures that all “worst-case” write cycles will be finished

or

2. Master “polls” memory to detemine if the write cycle is complete T_{wr} TYP = 5 ms

With option 2 the master can start polling immediately after starting the internal memory write cycle as follows:

[STOP] → [START] → [SLAVE ADDRESS FOR WRITE OPERATION] → [POLL ACK]

IF no ACK then NM24Cxx still BUSY doing internal write

else NM24Cxx completed write cycle
master can proceed with next read or write operation.

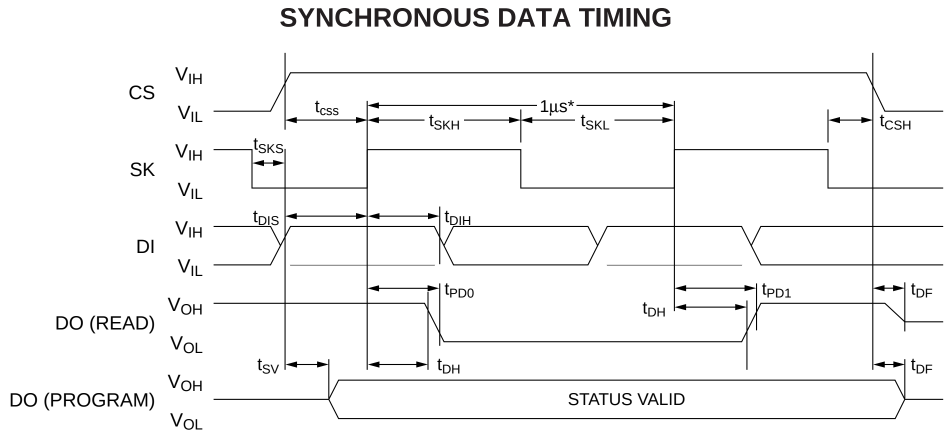
This method can make significant improvements to overall system performance.

Note: After receiving a no acknowledge the master should output a stop condition to free the I^2C-bus for other operations.

3.2 MICROWIRE Systems

3.2.1 Read Mode

A typical Read access is shown in Figure 9. The rising edge of CS is used to select and reset the EEPROM. Then the microcomputer clocks in the start bit and opcode for a read cycle using serial clock (SK) and Data In (DI pins). This is followed by the address where data is to be read from, after which the data is output via Data Out (DO) pin.

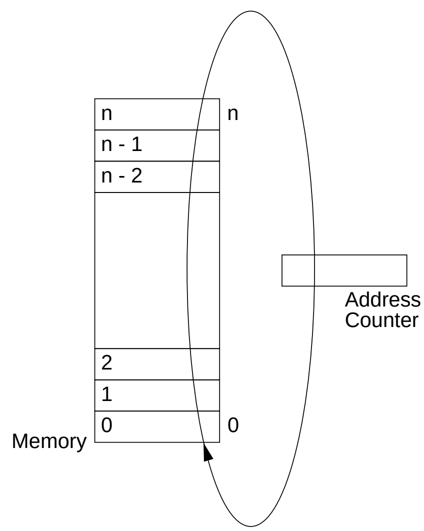


— Chip Select (CS) used to differentiate between various devices on bus.
— Rising edge of CS resets internal circuitry of EEPROM.
— Low-to-High transition of shift clock (SK) shifts all data in and out.
— CS brought low before next rising edge of SK to initiate self-timed programming cycle.

FIGURE 9. Read Mode

3.2.2 Sequential Read

All Fairchild's NM93CSxx devices support sequential read allowing the complete memory array to be read in a single operation.



CMOS: Sequential Read
Allows the user to obtain an endless loop of data simply by entering the read mode.
➔ Reduces overhead
➔ 50% faster read
Note: The NM93Cxx devices do NOT support sequential read.

FIGURE 10. Sequential Read

3.2.3 Write Mode

A write cycle is entered in a similar way to a read cycle; first the start bit and opcode for a write cycle are clocked in via DI, followed by the address and data to be written. The self timed programming cycle is initiated by bringing CS low before the next rising edge of SK as shown in Figure 11.

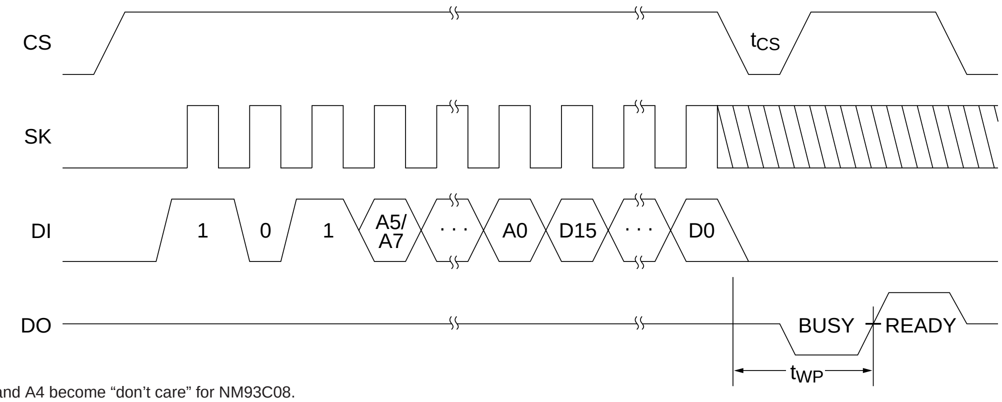
3.2.4 Typical Twp vs Maximum Twp

When the MICROWIRE EEPROMs the designer has three options to determine when the device has finished a programming cycle (either a write or erase instruction) as shown in Figure 11.

Option 1: µprocessor/µcontroller waits for **Twp(max) = 10 ms**

Option 2: µprocessor/µcontroller polls Data-Out (DO) for Busy/Ready status **Twp(typ) = 3 ms**

Option 3: if using the NM59C11 there is a separate RDY/BUSY pin: **Twp(typ) = 3 ms**



Address bit A6 and A4 become “don’t care” for NM93C08.

Address bit A7 becomes a “don’t care” for NM93C56.

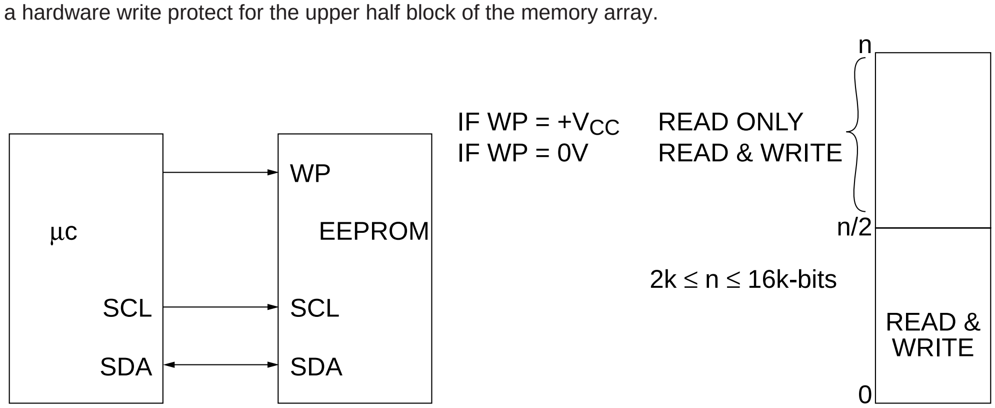
FIGURE 11. BUSY/READY Polling Options

All MICROWIRE EEPROMs can use options 1 or 2, and in the case of the NM59C11 there is a separate RDY/BUSY pin which the microcontroller/microprocessor can poll to determine the programming status.

4.0 WRITE PROTECTED MEMORY

4.1 I^{2}C EEPROMs

Fairchild Semiconductor manufactures two versions of I^{2}C EEPROMs: a “standard” version (NM24C02/04/08/16) and a “secure” version (NM24C03/05/09/17). The “secure” devices are fully software compatible with the standard devices plus they use one of the unused pins to implement a hardware write protect for the upper half block of the memory array.



$2k \le n \le 16k$

FIGURE 12. I^{2}C Secure Memory System

If the master does attempt to write to the protected memory, then the NM24C03/05/09/17 will accept the slave and word addresses, but will not generate an ACK, thus the programming cycle will not be started when the STOP condition is asserted.

4.2 MICROWIRE EEPROMs

All NM93CSxx devices have the security feature which allows the user to define a portion of the memory to be write protected, either permanently or temporarily. This is useful for storing secure information in a system, such as calibration data. To control the secure memory involves a combination of setting a hardware pin and various software instructions as shown in Figure 13.

— Protect Register:
  Input PRE must be high and PREN instruction executed before a write to protect register
— Disable Cell:
  Set via PRDS instruction, input PRE must be high and PREN instruction executed PRDS is a one time only instruction
— Address in register defines first location to be protected
— Protect register may be altered unless PRDS is executed

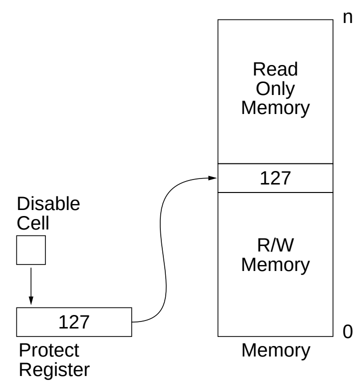
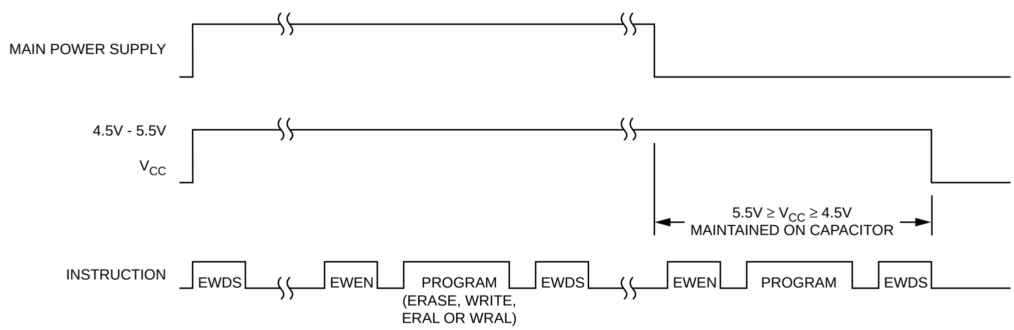


FIGURE 13. Memory Protect Register

Data in serial MICROWIRE EEPROMs is further protected from spurious write cycles (especially during power transitions) by including a program disable mode which will automatically abort any requested Erase or Write cycles. Figure 14 shows the suggested instruction flow for maximum data integrity with Fairchild's MICROWIRE EEPROMs.



* EWDS must be executed before V_{CC} drops below 4.5V to prevent accidental data loss during subsequent power down and/or power up transients.

FIGURE 14. Protecting Data in Serial EEPROMs

Typical Instruction flow for Maximum Data Protection

— Although EEPROM in non-volatile, the problem exists that stored data can be destroyed during power transitions.
— All Fairchild Semiconductor serial EEPROMs when initially powered up are in Program Disable Mode. In this mode it will abort any requested Erase or Write cycles.

5.0 EEPROM ENDURANCE AND SYSTEM LIFETIME

5.1 EEPROM Definitions

The two main specifications which determine the system reliability and lifetime of an EEPROM are Endurance and Data Retention.

Endurance: The number of data changes of an EEPROM before any bit fails to write correctly.

Data Retention: The ability of an EEPROM cell to retain charge once it has been programmed for extended periods under static or dynamic conditions of voltage or temperature.

Parameters which affect Endurance are:

- **Programming Duty Cycle and Waveform:** Although the NM93Cxx devices can have a F_{SK} (max) 1 MHz, it is important to make sure that the duty cycle is such that t_{SKH} (SK high time) and t_{SKL} (SK low time) have a minimum value of 250 ns.
- **Ambient Write Cycle Temperature:** The colder the operating temperature the better the endurance will be. For example 25°C vs 90°C will show approximately a 2:1 improvement.
- **Programming Time:** All Fairchild EEPROMs are self-timed and the programming time cannot be varied by the user, guaranteeing reliable system and lifetime performance.
- `**Programming Voltage:** The lower the programming voltage V_{PP} the longer the required timing period T_{wp}. All Fairchild's EEPROMs operate from a single V_{CC} supply and have an on-board V_{PP} generator which is V_{CC} independent. This ensures that all Fairchild EEPROMs are both easy to use and highly reliable. The programming voltage cannot be varied by the user.

5.2 Read Cycles

Read cycles are non-destructive so all EEPROMs have the capability for an infinite number of reads.

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5.3 Data Changes

With an EEPROM it is important to look at the endurance or number of write cycles the device can support. There are three types of write sequence to consider with EEPROM technology:

1) Erase before Write

As the names suggests, a memory location must be erased before it can be written to. A typical software flow for a write instruction is:

— send ERASE instruction to memory address n
— send WRITE instruction to memory address n

Disadvantages

— must perform 2 dedicated instructions
— slower system performance (2 instruction cycles, 2 T_{WP} delays)
— each write operation requires 2 data changes; i.e., endurance specification is effectively halved

2) Autoerase

— send WRITE instruction
— EEPROM automatically performs ERASE instruction, then performs the WRITE operation

Disadvantages

— still need 2 data changes for each WRITE cycle, thus reducing system performance and halving endurance rating

3) Direct Write

— single WRITE instruction, no ERASE needed
— writes over existing memory contents
— eliminates ERASE cycles

Advantages

— single instruction, faster system performance
— single data change for each WRITE instruction

All Fairchild Semiconductor CMOS EEPROMs (both MICROWIRE and I^2C) use Direct Write method giving the highest system performance, reliability and endurance characteristics of CMOS EEPROMs available on the market today.

When looking at EEPROM endurance specifications it is necessary to look more specifically at the number of data changes (ERASE & WRITE) per write cycle. Fairchild specifies 1 write cycle to be 2 data changes (to be consistent with other manufacturer's datasheets whose products are either Erase before Write or Auto Erase), so the figure of 500k Write cycles is actually equivalent to an endurance figure of 1 Million (10^6) data changes.

Fairchild Semiconductor produce full product qualification booklets giving process performance and reliability characteristics; for a copy contact your local Fairchild Sales representative.

6.0 CONCLUSION

Fairchild Semiconductor offer the widest range of serial EEPROMs covering two main industry standard serial interfaces;

MICROWIRE:
e.g. NM93Cxx, NM93CSxx
size: 256-bit → 4 kbit (16 kbit coming)

I^2C:
e.g. NM24Cxx
size: 2k → 16 kbits

All these EEPROMs offer the same high specifications of:

Endurance:	10^6 data changes
Direct Write:	no erase cycle required
Data Retention:	greater than 40 years
Self-Timed Write Cycle:	typical write cycle time 5 ms
Sequential Read:	NM93CSxx, NM24Cxx devices
Memory Protect:	NM93CSxx, NM24C03/05/09/17

These features make them easy to use, allowing the system designer to achieve high performance, highly reliable systems.

REFERENCES

Fairchild Semiconductor Memory Databook
Fairchild Semiconductor CMOS Logic Databook

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