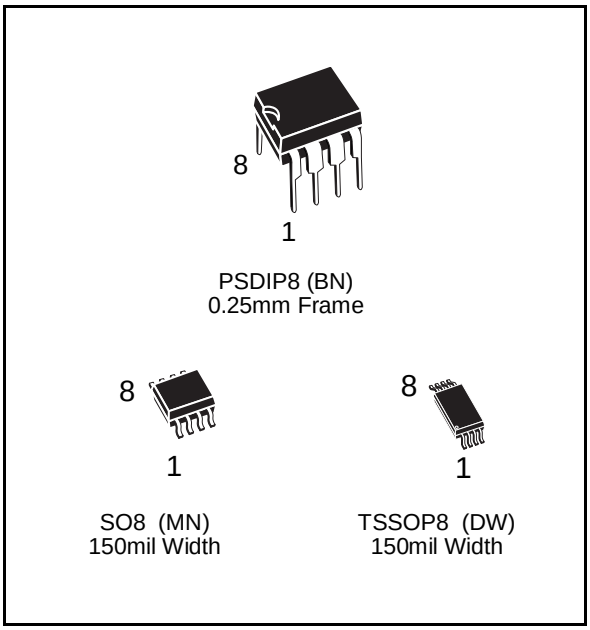
M95040
M95020, M95010

4K/2K/1K Serial SPI EEPROM with High Speed Clock and Positive Clock Strobe

PRELIMINARY DATA

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for M950x0
  - 2.5V to 5.5V for M950x0-W
  - 1.8V to 3.6V for M950x0-R
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 5 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



DESCRIPTION

The M950x0 is a family of Electrically Erasable Programmable Memories (EEPROM) fabricated with STMicroelectronics's High Endurance Single Polysilicon CMOS technology. Each memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

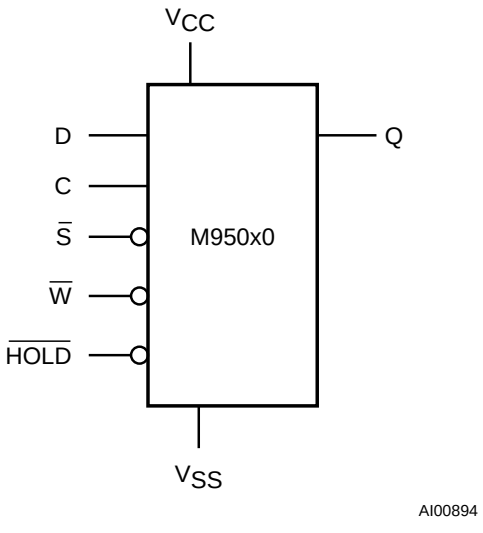


Figure 2A. DIP Pin Connections

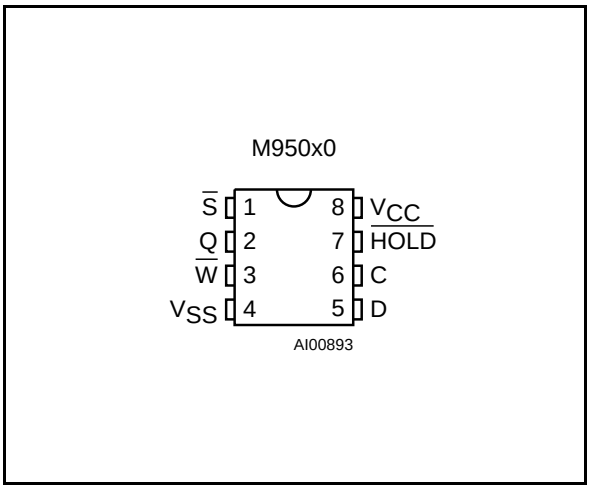


Figure 2B. SO and TSSOP Pin Connections

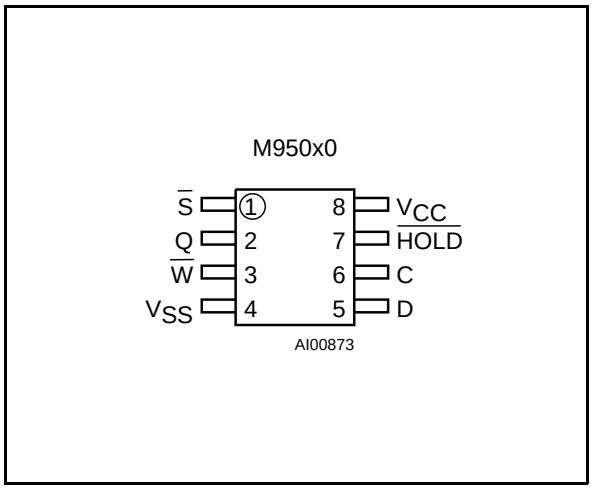


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the Memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Input is latched on the rising edge of the serial clock.

Figure 3. Data and Clock Timing

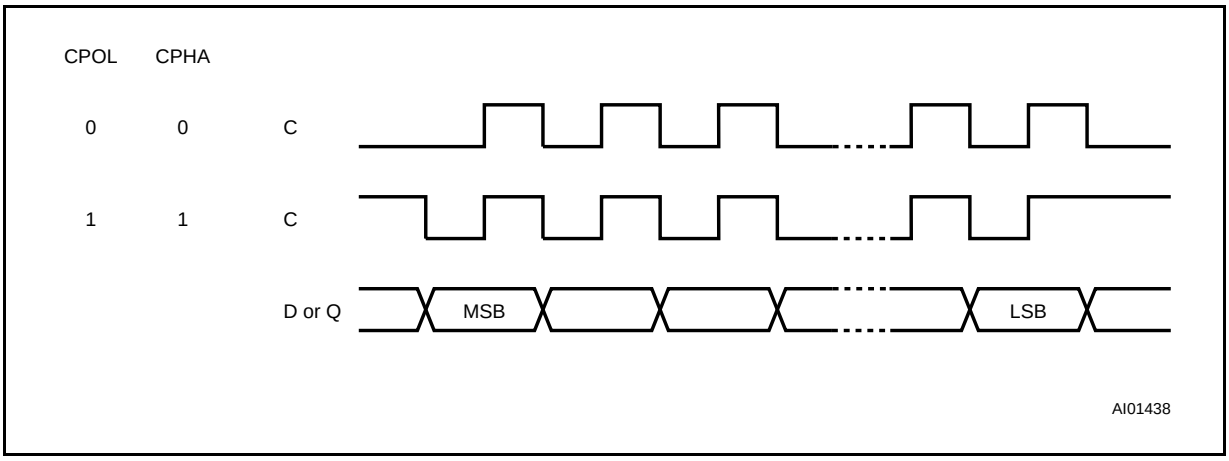
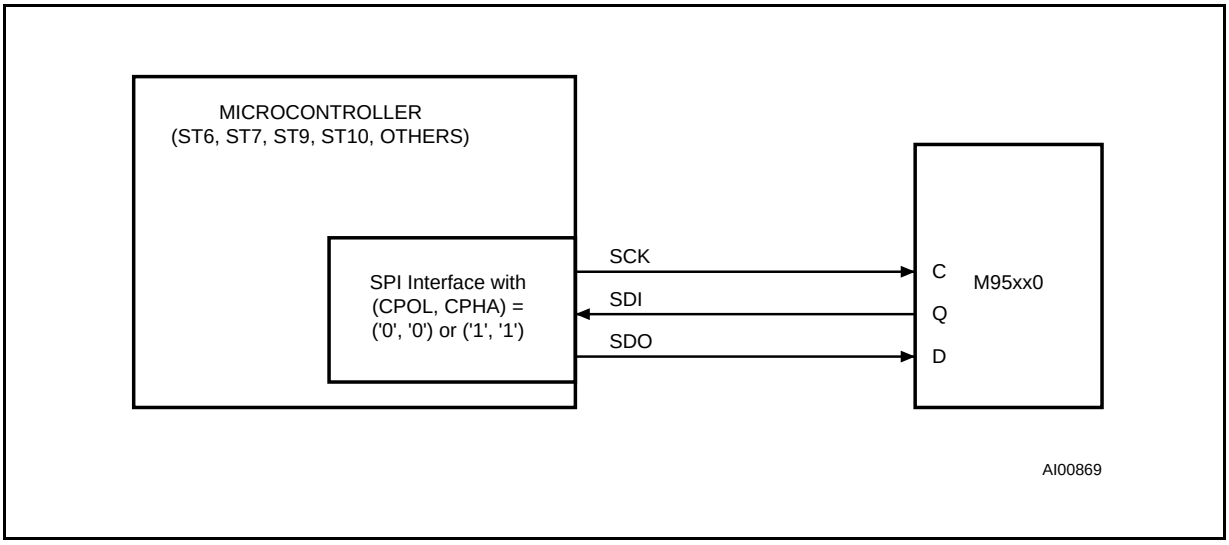


Figure 4. Microcontroller and SPI Interface Set-up



Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the Memory is deselected and the Q output pin is at high impedance and, unless an internal write operation is underway the Memory will be in the standby power mode. $\overline{S}$ low enables the Memory, placing it in the active power mode. For a safe design, it should be noted that during power up, the $\overline{S}$ input must be driven constantly high (or low) but must NOT be left floating until the supplied voltage reaches the specified V_{CC} value. After power up, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protection. When $\overline{W}$ is low, writes to the Memory are disabled but any other operations stay enabled. When $\overline{W}$ is high, all writes operations are available. $\overline{W}$ going low at any time before the last bit D0 of the data stream will reset the write enable latch and prevent programming. No action on $\overline{W}$ or on the write enable latch can interrupt a write cycle which has commenced.

Hold ($\overline{\text{HOLD}}$). The $\overline{\text{HOLD}}$ pin is used to pause serial communications with the Memory without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{\text{HOLD}}$ when C is low. To resume the communications, $\overline{\text{HOLD}}$ is brought high while C is low. During the Hold condition D, Q, and C are at a high impedance state.

When the Memory is under the Hold condition, it is possible to deselect the device. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The Memory can be driven by a microcontroller with its SPI peripheral running in either of the two following modes: (CPOL, CPHA) = ('0', '0') or (CPOL, CPHA) = ('1', '1').

For these two modes, input data is latched in by the low to high transition of clock C, and output data is available from the high to low transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the stand-by polarity: C remains at '0' for (CPOL, CPHA) = (0, 0) and C remains at '1' for (CPOL, CPHA) = (1, 1) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 3 shows the instruction set and format for device operation. If an invalid instruction is sent (one not contained in Table 3), the chip is automatically deselected. For operations that read or write data in the memory array, bit 3 of the instruction is the MSB of the address, otherwise, it is a don't care.

Write Enable (WREN) and Write Disable (WRDI)

The Memory contains a write enable latch. This latch must be set prior to every WRITE or WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under the following conditions:

– $\overline{W}$ pin is low
– Power on
– WRDI instruction executed
– WRSR instruction executed
– WRITE instruction executed

As soon as the WREN or WRDI instruction is received by the memory, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write to the memory operation. If a Read Status register reaches the 8th bit of the Status register, an additional 9th clock pulse will wrap around to read the 1st bit of the Status Register

The status register format is as follows:

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

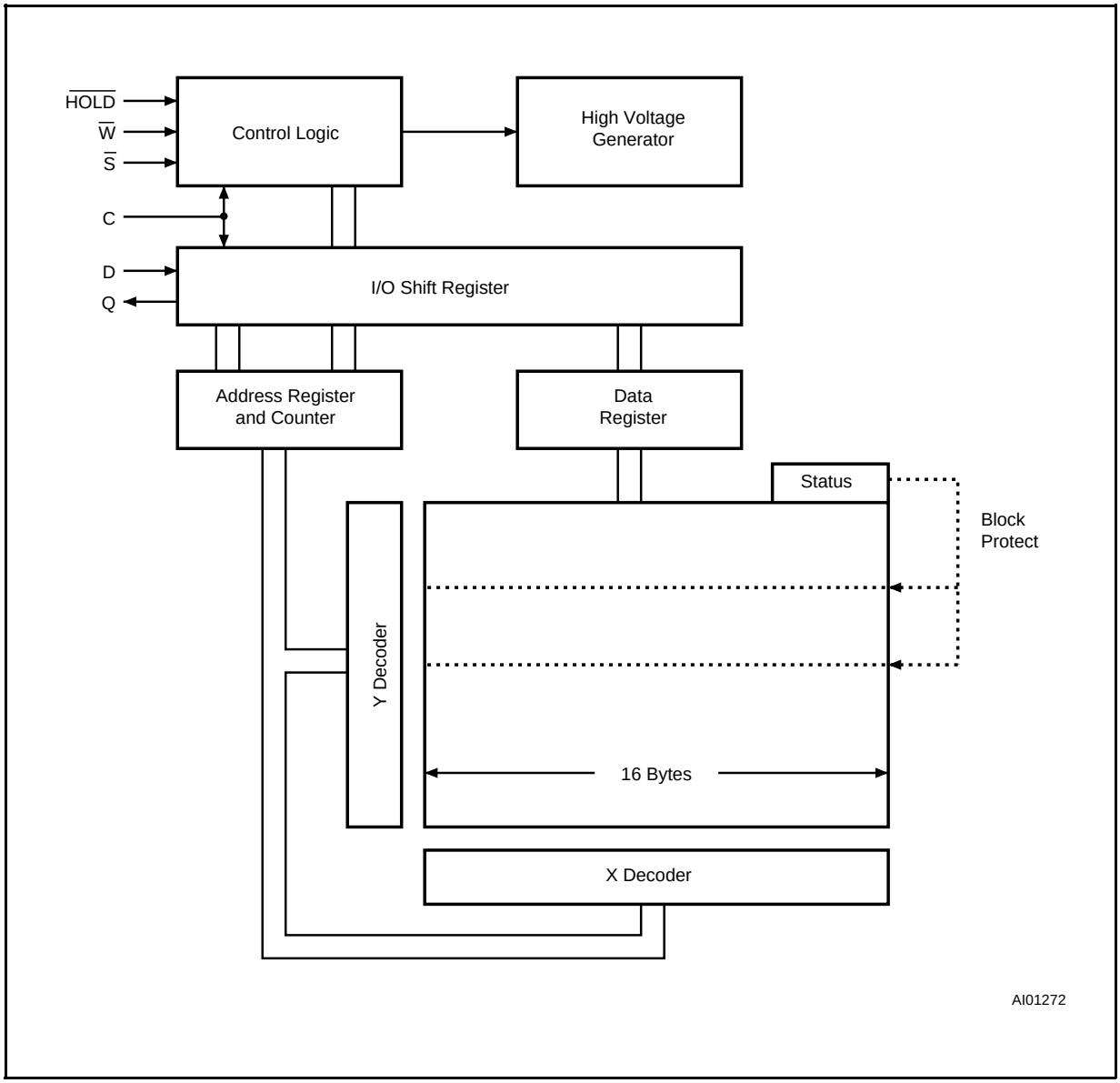
BP1, BP0: Read and write bits
WEL, WIP: Read only bits.
b7 to b4: Read only bits.

Table 3. Instruction Set

Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 X110
WRDI	Reset Write Enable Latch	0000 X100
RDSR	Read Status Register	0000 X101
WRSR	Write Status Register	0000 X001
READ	Read Data from Memory Array	0000 $A_8$011
WRITE	Write Data to Memory Array	0000 $A_8$010

Notes: A_8 = 1, Upper page selected on M95040.
A_8 = 0, Lower page selected on M95040.
X = Don't care.

Figure 5. Block Diagram

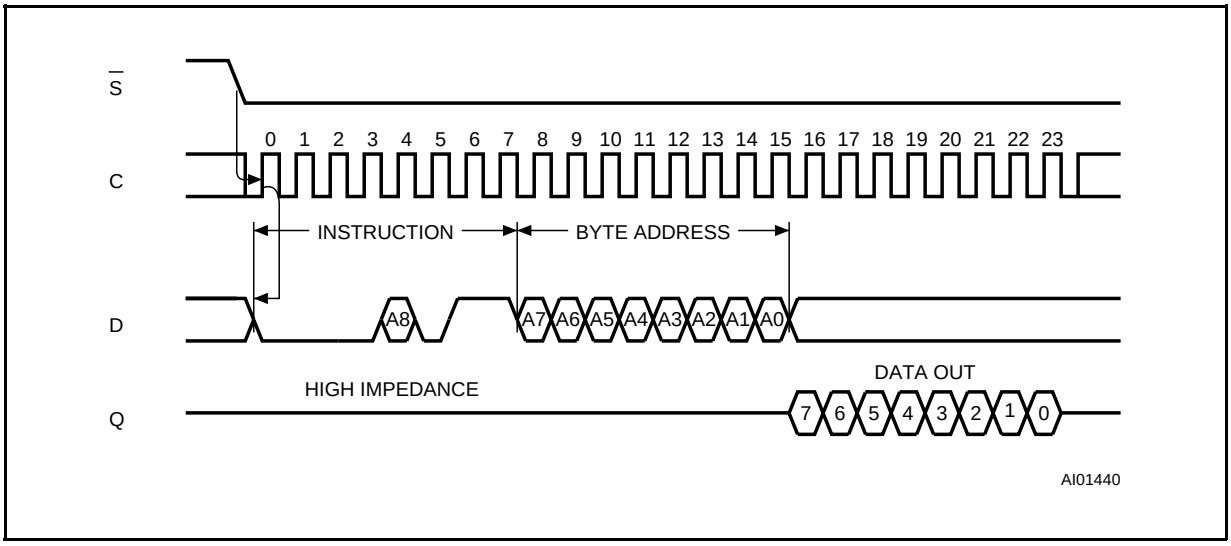


During a write to the memory operation to the memory array, all bits BP1, BP0, WEL, WIP are valid and can be read. During a write to the status register, only the bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read-only bit indicates whether the Memory is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read-only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Figure 6. Read Operation Sequence



Notes: A8 = A7 = X on M95010 and M95020; A8 is only active on M95040.
X = Don't care.

Table 4. Write Protected Block Size

Status Register Bits		Protected Block	Array Address Protected		
BP1	BP0		M95040	M95020	M95010
0	0	none	none	none	none
0	1	Upper quarter	180h - 1FFh	C0h - FFh	60h - 7Fh
1	0	Upper half	100h - 1FFh	80h - FFh	40h - 7Fh
1	1	Whole memory	000h - 1FFh	00h - FFh	00h - 7Fh

Write Status Register (WRSR)

The WRSR instruction writes (only) the BP1 and BP0 bits allowing to define the size of protected memory. The user may read the blocks but will be unable to write within the protected blocks. The blocks and respective WRSR control bits are shown in Table 4.

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$.

This rising edge of $\overline{S}$ must appear no later than the 16th clock cycle of the WRSR instruction of the Status Register content (it must not appear a 17th clock pulse before the rising edge of $\overline{S}$), otherwise the internal write sequence is not performed.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a one byte address (A7-A0), each bit being latched-in during the rising edge of the clock (C). Bit 3 (see Table 3) of the read instruction contains address bit A8 (most significant address bit). Then the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C).

The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to 0h allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a write cycle will be rejected and will deselect the chip.

Figure 7. Write Enable Latch Sequence

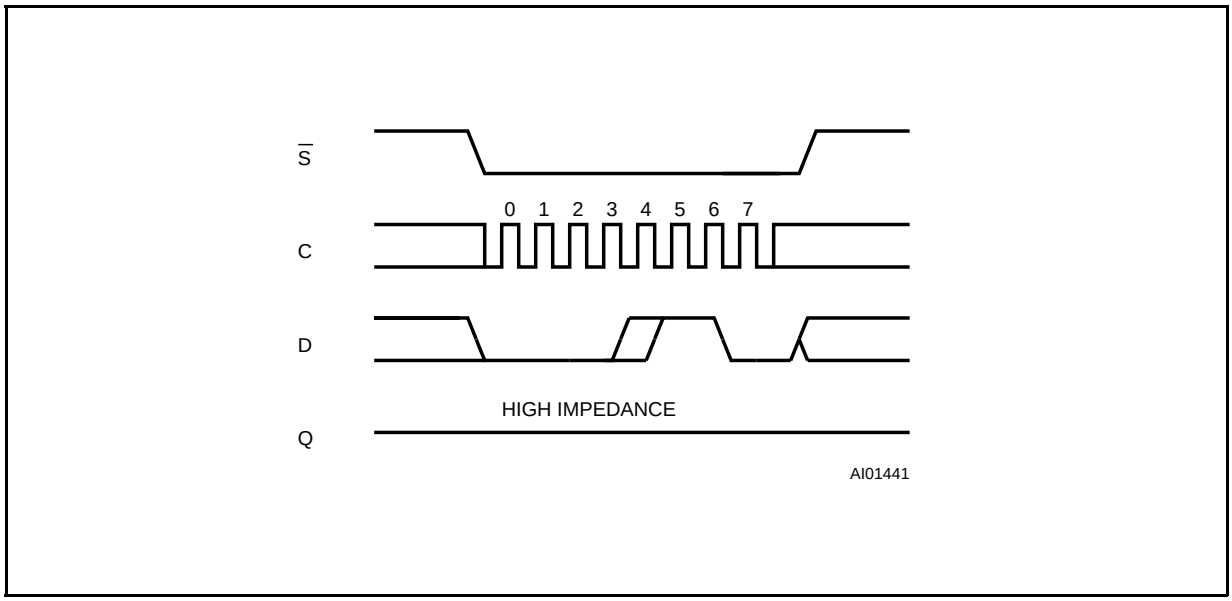
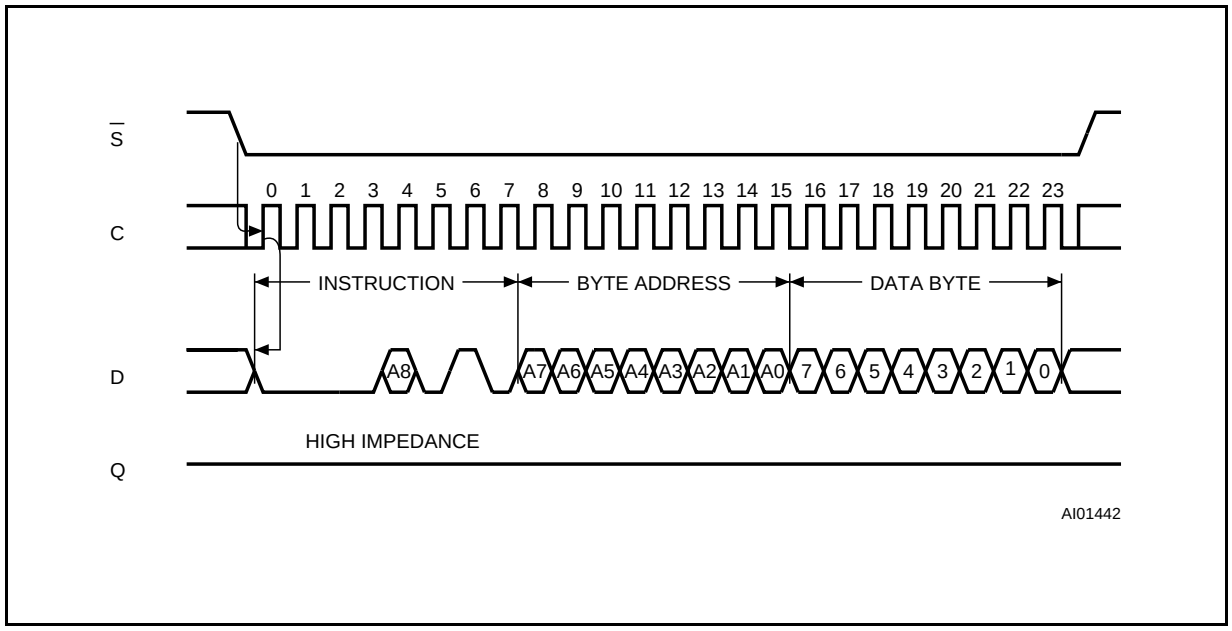
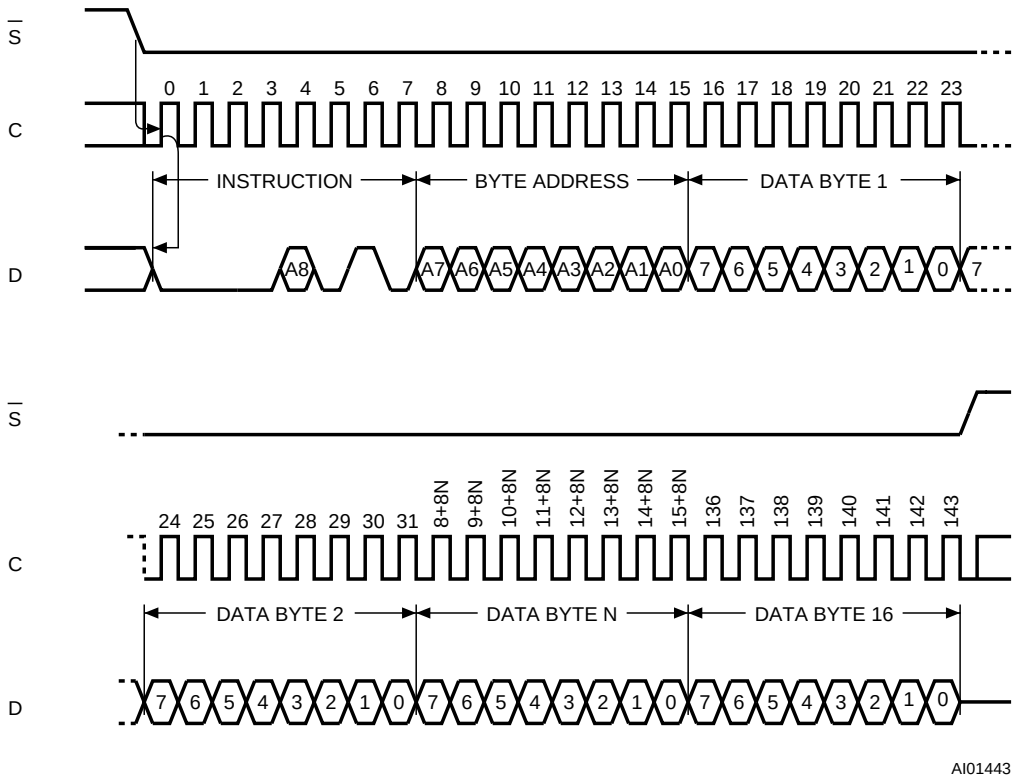


Figure 8. Byte Write Operation Sequence



Notes: A8 = A7 = X on M95010 and M95020; A8 is only active on M95040.
X = Don't care.

Figure 9. Page Write Operation Sequence



Notes: A8 = A7 = X on M95010 and M95020; A8 is only active on M95040.
X = Don't care.

Figure 10. RDSR: Read Status Register Sequence

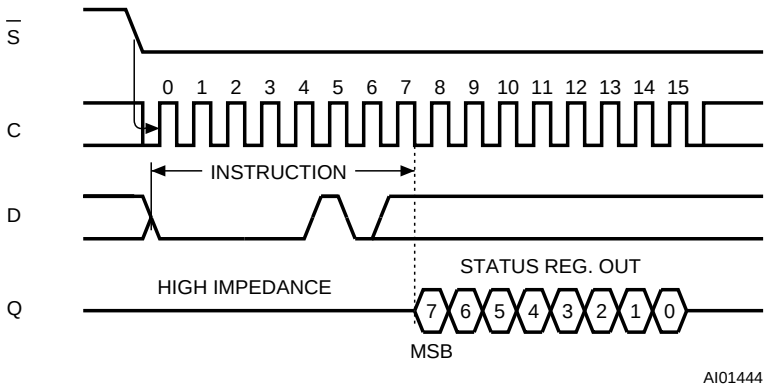
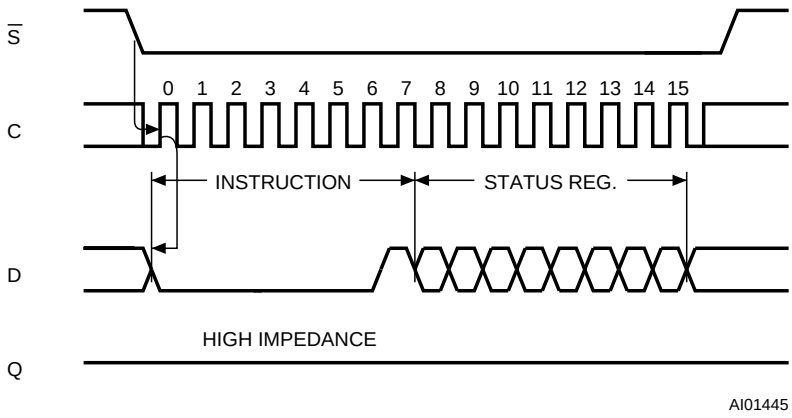


Figure 11. WRSR: Write Status Register Sequence



Byte Write Operation

Prior to any write attempt, the write enable latch must be set by issuing the WREN instruction. First the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the Memory will set the write enable latch and then remain in standby until it is deselected. Then the write state is entered by selecting the chip, issuing two bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remain low for the entire duration of the operation. The product must be deselected just after the eighth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is completed, the write enable latch is reset.

Page Write Operation

A maximum of 16 bytes of data may be written during one non-volatile write cycle. All 16 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting the device after the first byte of data, up to 15 additional bytes can be shifted in prior to deselecting the chip. A page address begins with address xxxx 0000 and ends with xxxx 1111. If the address counter reaches xxxx 1111 and the clock continues, the counter will roll over to the first address of the page (xxxx 0000) and overwrite any previously written data. The programming cycle will only start if the $\overline{S}$ transition occurs just after the eighth bit of data of a word is received.

POWER ON STATE

After a Power up the Memory is in the following state:

– The device is in the low power standby state.
– The chip is deselected.
– The chip is not in hold condition.

The Status Register content at power-up is:

				BP1	BP0	WEL	WIP
1	1	1	1	0	0	0	0

Figure 12. EEPROM and SPI Bus

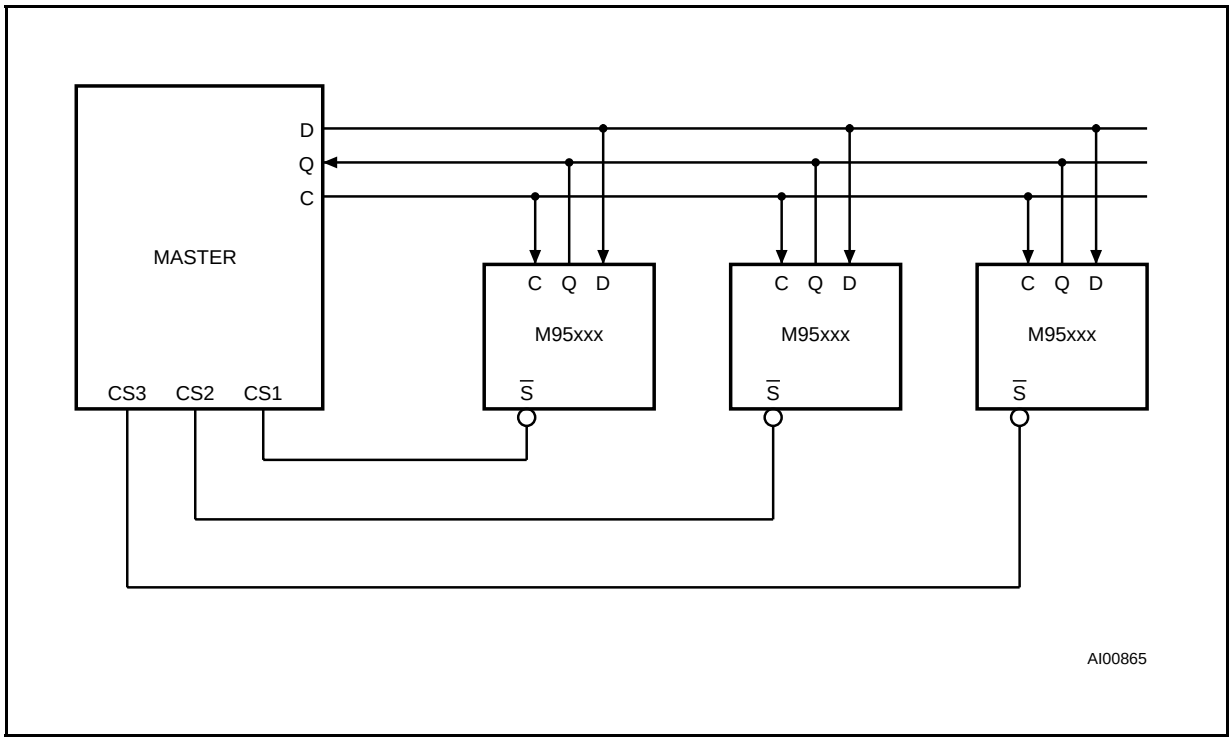


Table 5. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output Wavef.

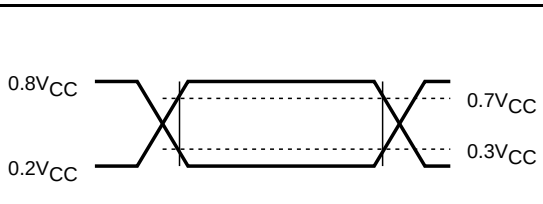


Table 6. Input Parameters (1) (T_A = 25 °C, f = 5 MHz)

Symbol	Parameter	Min	Max	Unit
C_{IN}	Input Capacitance (D)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF

Note: 1. Sampled only, not 100% tested.

Table 7. DC Characterististics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 4.5V to 5.5V)
(T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 2.5V to 5.5V)
(T_A = 0 to 70°C or –20 to 85°C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			±2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9 V_{CC}, at 5 MHz, V_{CC} = 5V, Q = Open		4	mA
		C = 0.1 V_{CC}/0.9 V_{CC}, at 2 MHz, V_{CC} = 5V, Q = Open, Note 2		4	mA
	Supply Current (W series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 2 MHz, V_{CC} = 2.5V, Q = Open		2	mA
	Supply Current (R series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 1 MHz, V_{CC} = 1.8V, Q = Open		2	mA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		10	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, Note 2		10	µA
	Standby Current (W series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		2	µA
	Standby Current (R series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8V		1	µA
V_{IL}	Input Low Voltage		– 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA, V_{CC} = 5V		0.4	V
		I_{OL} = 2mA, V_{CC} = 5V, Note 2		0.4	V
	Output Low Voltage (W series)	I_{OL} = 1.5mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.3	V
V_{OH} (1)	Output High Voltage	I_{OH} = –2mA, V_{CC} = 5V	0.8 V_{CC}		V
		I_{OH} = –2mA, V_{CC} = 5V, Note 2	0.8 V_{CC}		V
	Output High Voltage (W series)	I_{OH} = –0.4mA, V_{CC} = 2.5V	0.8 V_{CC}		V
	Output High Voltage (R series)	I_{OH} = –0.1mA, V_{CC} = 1.8V	0.8 V_{CC}		V

Notes: 1. The device meets output requirements for both TTL and CMOS standards.
2. Test performed at –40 to 125°C temperature range, grade 3.

Table 8A. AC Characteristics

Symbol	Alt	Parameter	M95040 / M95020 / M95010				Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = –40 to 125°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	5	D.C.	2	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	90		200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		ns
t_{CH} (1)	t_{CLH}	Clock High Time	90		200		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	90		200		ns
t_{CLCH} (2)	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} (2)	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		ns
t_{DLDH} (2)	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} (2)	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}		$\overline{HOLD}$ Setup Time	70		140		ns
t_{HLCH}		Clock Low Hold Time	40		90		ns
t_{CLHL}		Clock Low Setup Time before $\overline{HOLD}$ Active	0		0		ns
t_{CLHH}		Clock Low Setup Time before $\overline{HOLD}$ Not Active	0		0		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	90		200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time		100		250	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		50		100	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		50		100	ns
t_{HHQX} (2)	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/fc$.
2. Value guaranteed by characterization, not 100% tested in production.

Table 8B. AC Characteristics

Symbol	Alt	Parameter	M95040 / M95020 / M95010				Unit
			V_{CC} = 2.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V, T_A = 0 to 70°C, T_A = –20 to 85°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	2	D.C.	1	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	200		400		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	200		400		ns
t_{CH} (1)	t_{CLH}	Clock High Time	200		400		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	200		400		ns
t_{CLCH} (2)	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} (2)	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	40		60		ns
t_{CHDX}	t_{DH}	Data In Hold Time	50		100		ns
t_{DLDH} (2)	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} (2)	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}		$\overline{HOLD}$ Setup Time	140		350		ns
t_{HLCH}		Clock Low Hold Time	90		200		ns
t_{CLHL}		Clock Low Setup Time before $\overline{HOLD}$ Active	0		0		ns
t_{CLHH}		Clock Low Setup Time before $\overline{HOLD}$ Not Active	0		0		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	200		400		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	200		400		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	200		300		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time		250		500	ns
t_{CLQV}	t_V	Clock Low to Output Valid		150		380	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		100		200	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		100		200	ns
t_{HHQX} (2)	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		100		250	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		250		500	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/fc$.
2. Value guaranteed by characterization, not 100% tested in production.

Figure 14. Serial Input Timing

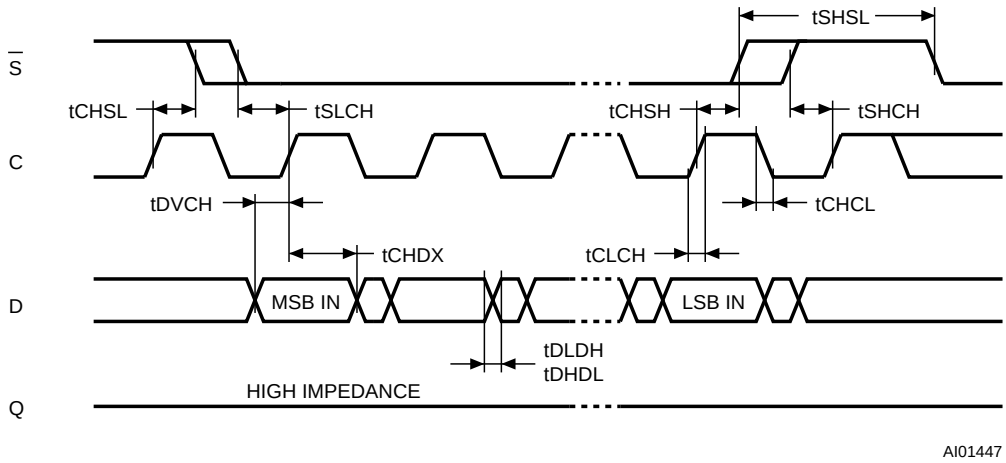


Figure 15. Hold Timing

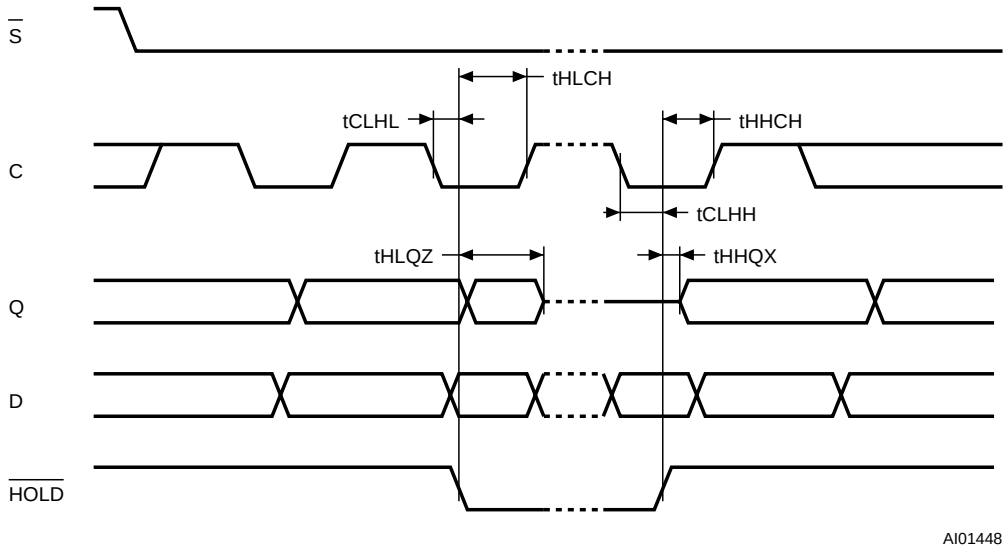
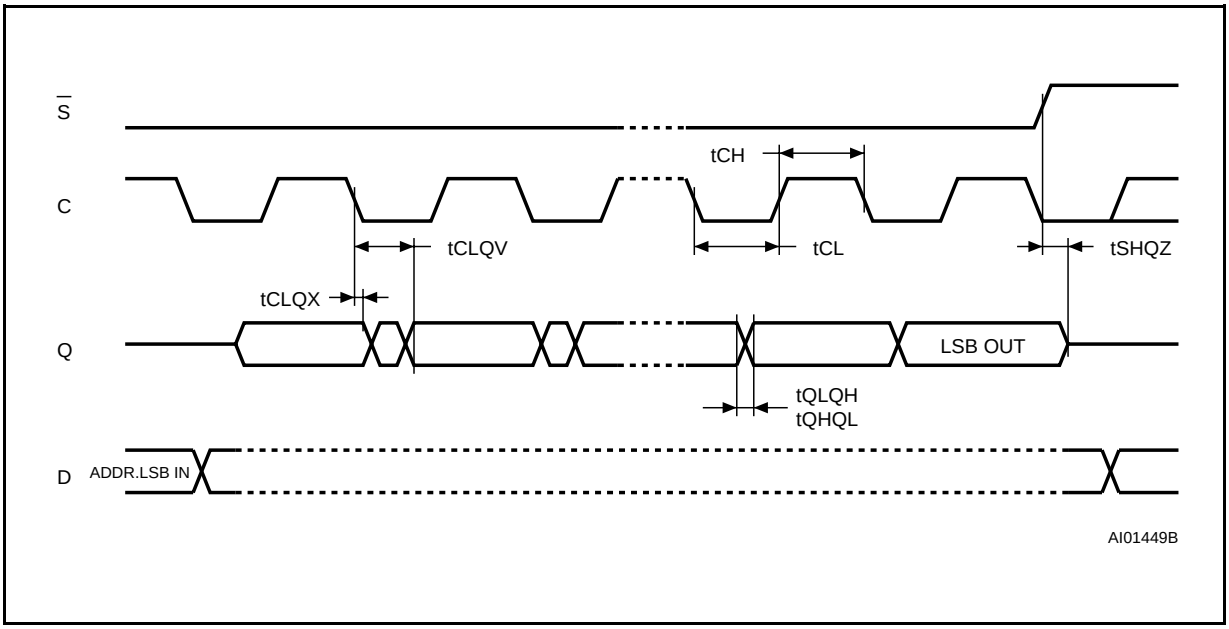
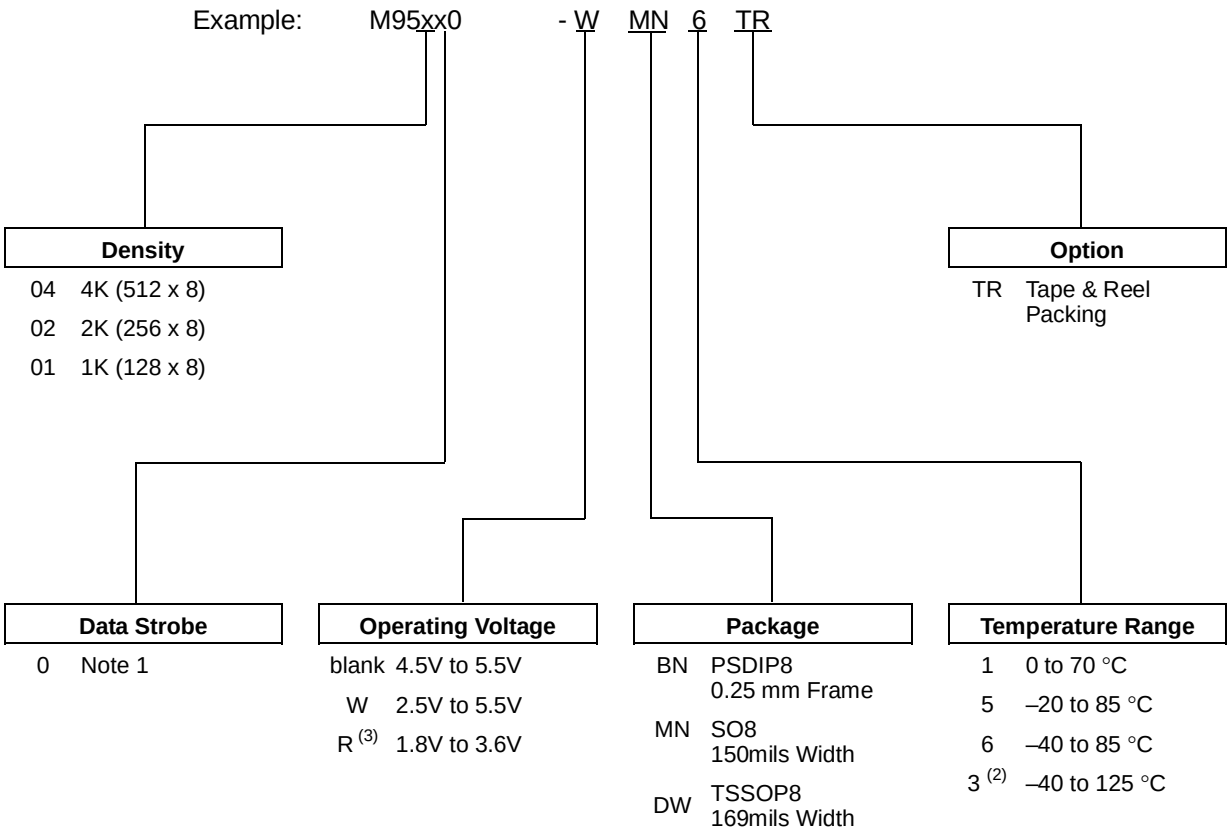


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



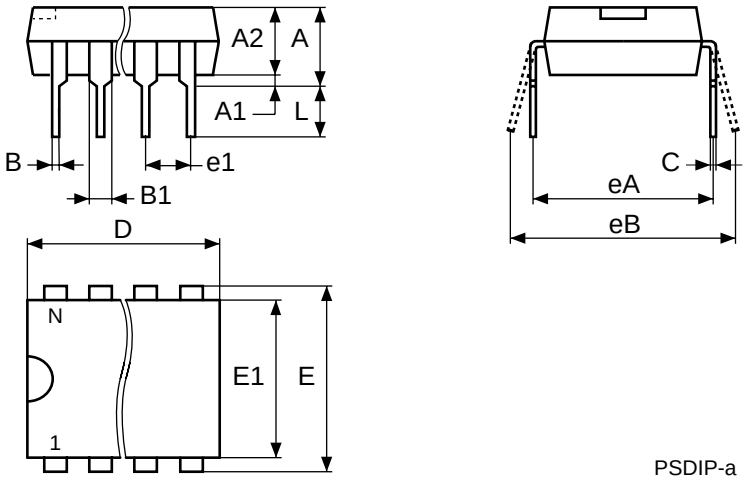
Notes: 1. Data In is strobed on rising edge of the clock (C) and Data Out is synchronized from the falling edge of the clock.
2. Temperature range on request only, 5V ± 10% only.
3. -R versions (1.8V to 3.6V) are only available in temperature range 5 or 1.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

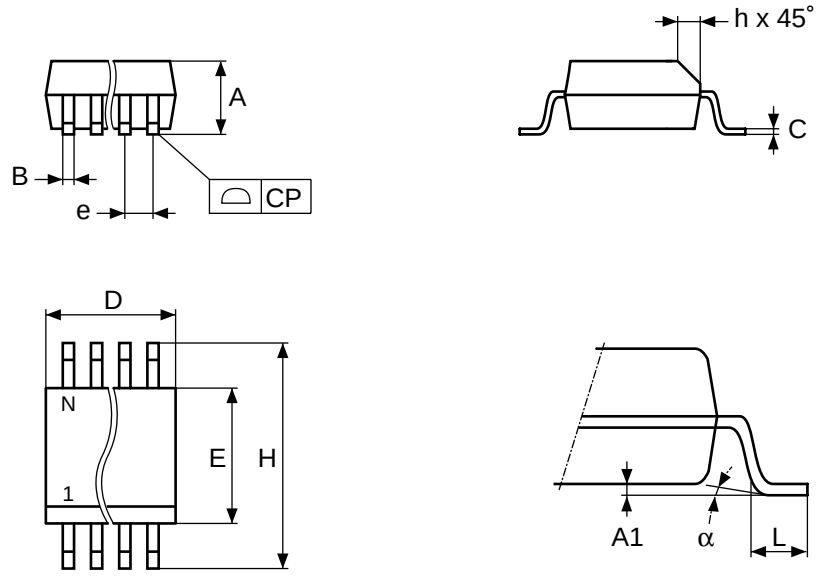


PSDIP-a

Drawing is not to scale

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

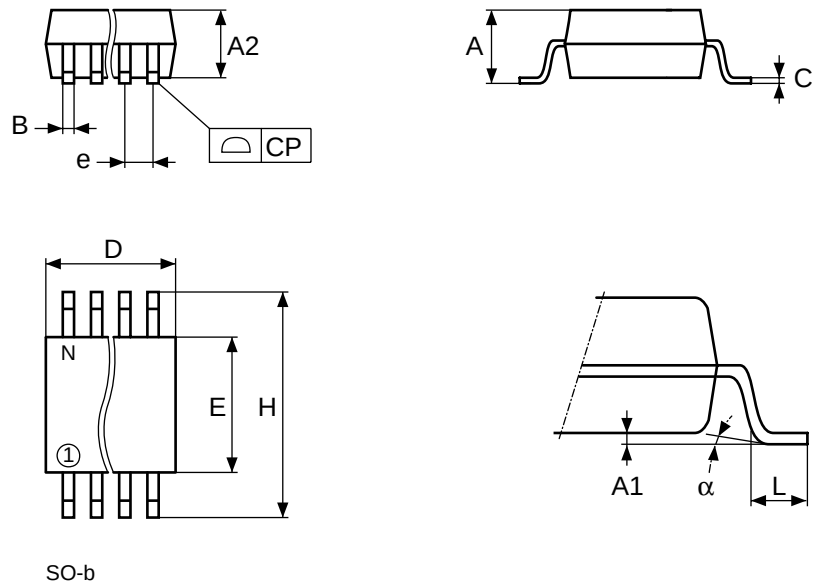


SO-a

Drawing is not to scale

TSSOP8 - 8 lead Thin Shrink Small Outline, 169 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	8			8		
CP			0.08			0.003



SO-b

Drawing is not to scale