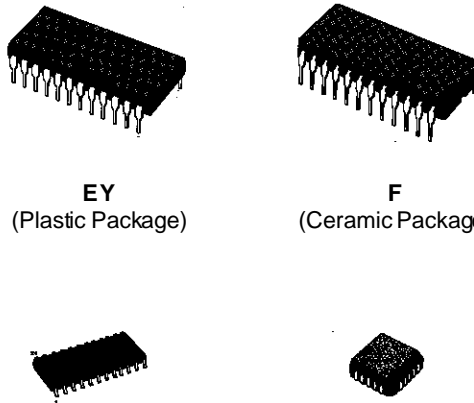


**ANALOG MULTIPLEXER/DEMULTIPLEXER**

**4067B-SINGLE 16-CHANNEL**  
**4097B-DIFFERENTIAL 8-CHANNEL**

- **LOW ON RESISTANCE:** 125Ω (typ.) OVER 15 V<sub>p-p</sub> SIGNAL INPUT RANGE FOR V<sub>DD</sub> - V<sub>SS</sub> = 15V
- **HIGH OFF RESISTANCE:** CHANNEL LEAKAGE OF ±10pA (typ.) @ V<sub>DD</sub> - V<sub>SS</sub> = 10V
- **MATCHED SWITCH CHARACTERISTICS:** ΔR<sub>ON</sub> = 5Ω (typ.) FOR V<sub>DD</sub> - V<sub>SS</sub> = 15V
- **VERY LOW QUIESCENT POWER DISSIPATION** UNDER A DIGITAL CONTROL INPUT AND SUPPLY CONDITIONS: 0.2μW (typ.) @ V<sub>DD</sub> - V<sub>SS</sub> = 10V
- **BINARY ADDRESS DECODING ON CHIP**
- **QUIESCENT CURRENT SPECIFIED TO 20V** FOR HCC DEVICE
- **STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS**
- **5V, 10V AND 15V PARAMETRIC RATINGS**
- **INPUT CURRENT OF 100nA AT 18V AND 25°C** FOR HCC DEVICE
- **100% TESTED FOR QUIESCENT CURRENT**
- **MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B-SERIE CMOS DEVICES"**



**EY**  
(Plastic Package)

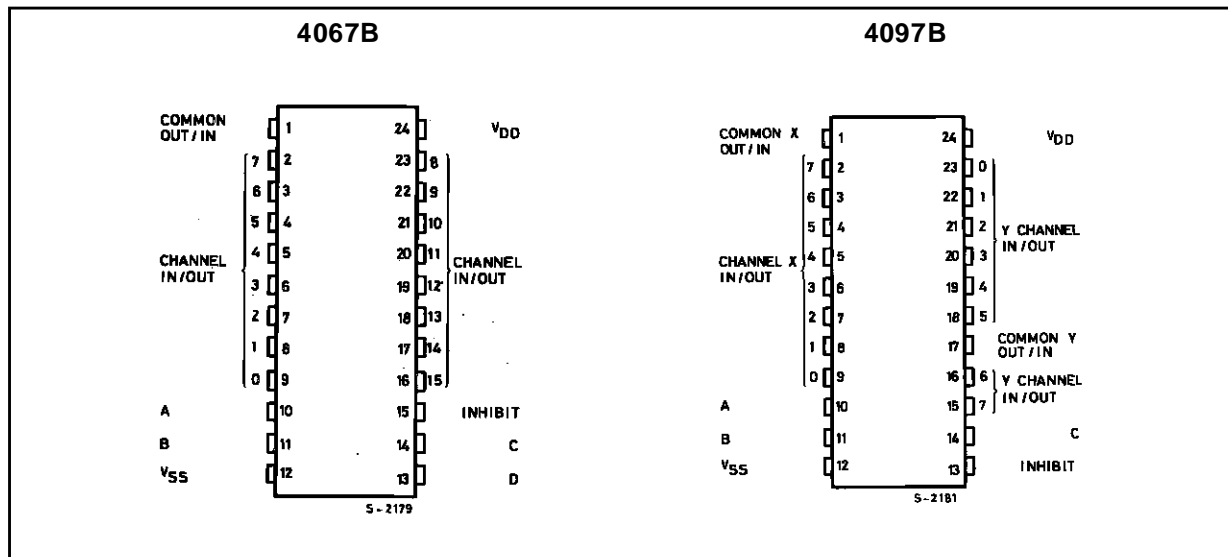
**F**  
(Ceramic Package)

**M1**  
(Micro Package)

**C1**  
(Chip Carrier)

**ORDER CODES :**  
HCC40XXBF      HCF40XXBM1  
HCF40XXBEY    HCF40XXBC1

**PIN CONNECTIONS**



## HCC/HCF4067B HCC/HCF4097B

### DESCRIPTION

The **HCC4067B**, **HCC4097B** (extended temperature range) and **HCF4067B**, **HCF4097B** (intermediate temperature range) are monolithic integrated circuits available in 24-lead dual in line plastic or ceramic package.

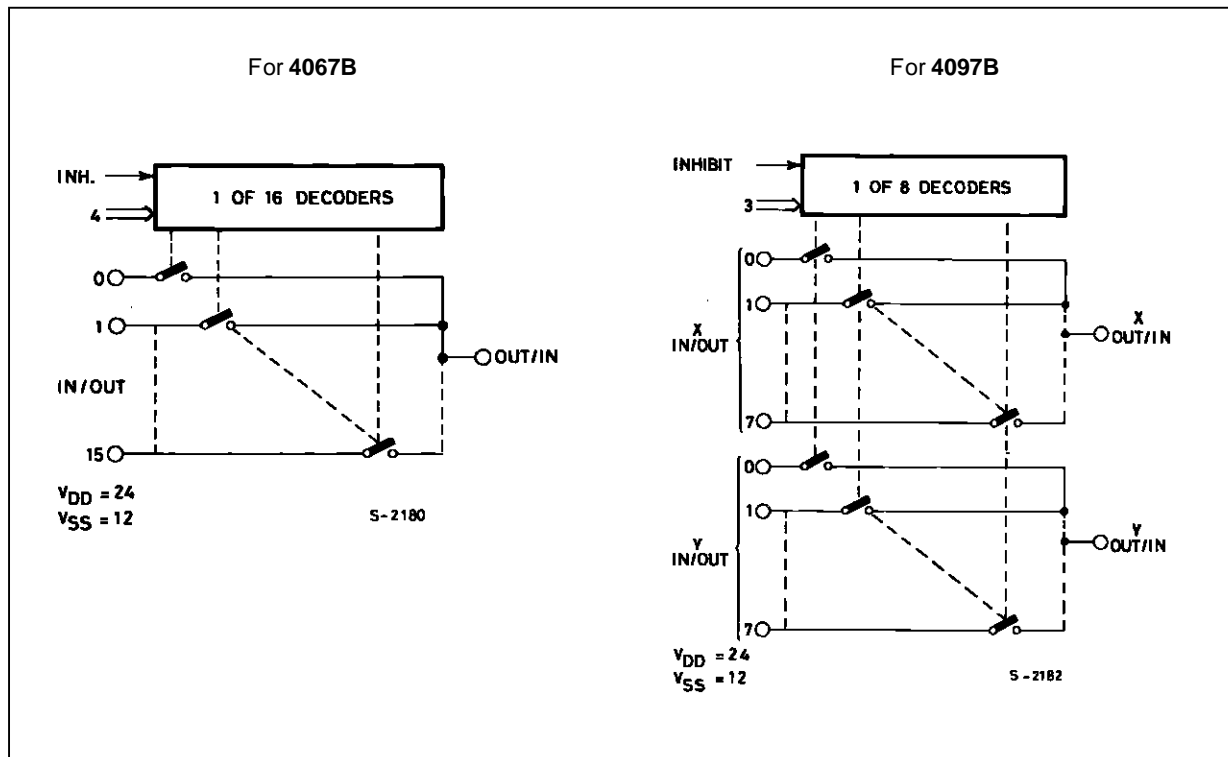
The **HCC/HCF4067B** and **HCC/HCF4097B** COS/MOS analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance, low OFF leakage current and internal

address decoding. in addition, the ON resistance is relatively constant over the full input-signal range.

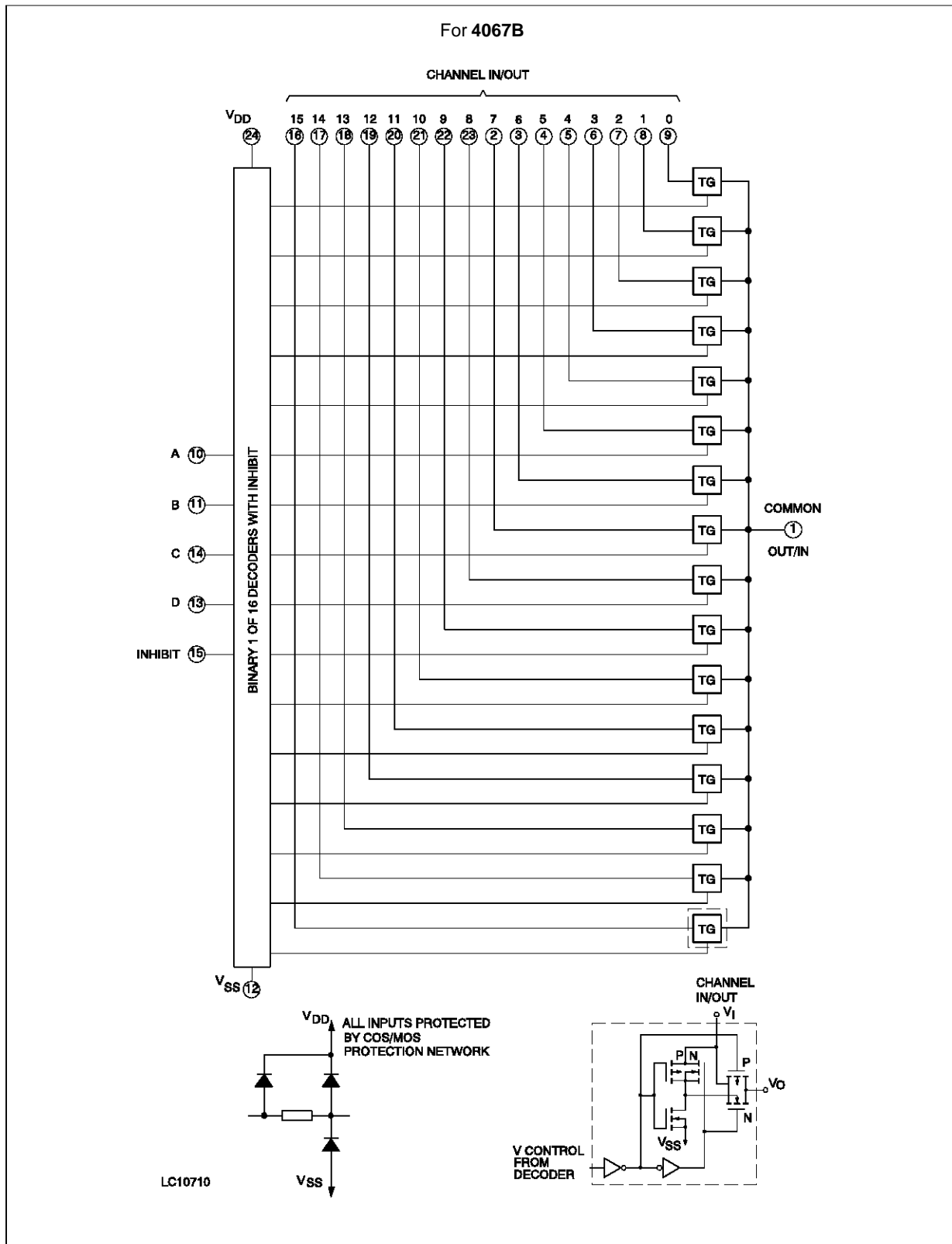
The **HCC/HCF4067B** is a 16-channel multiplexer with four binary control inputs A, B, C, D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The **HCC/HCF4097** is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one

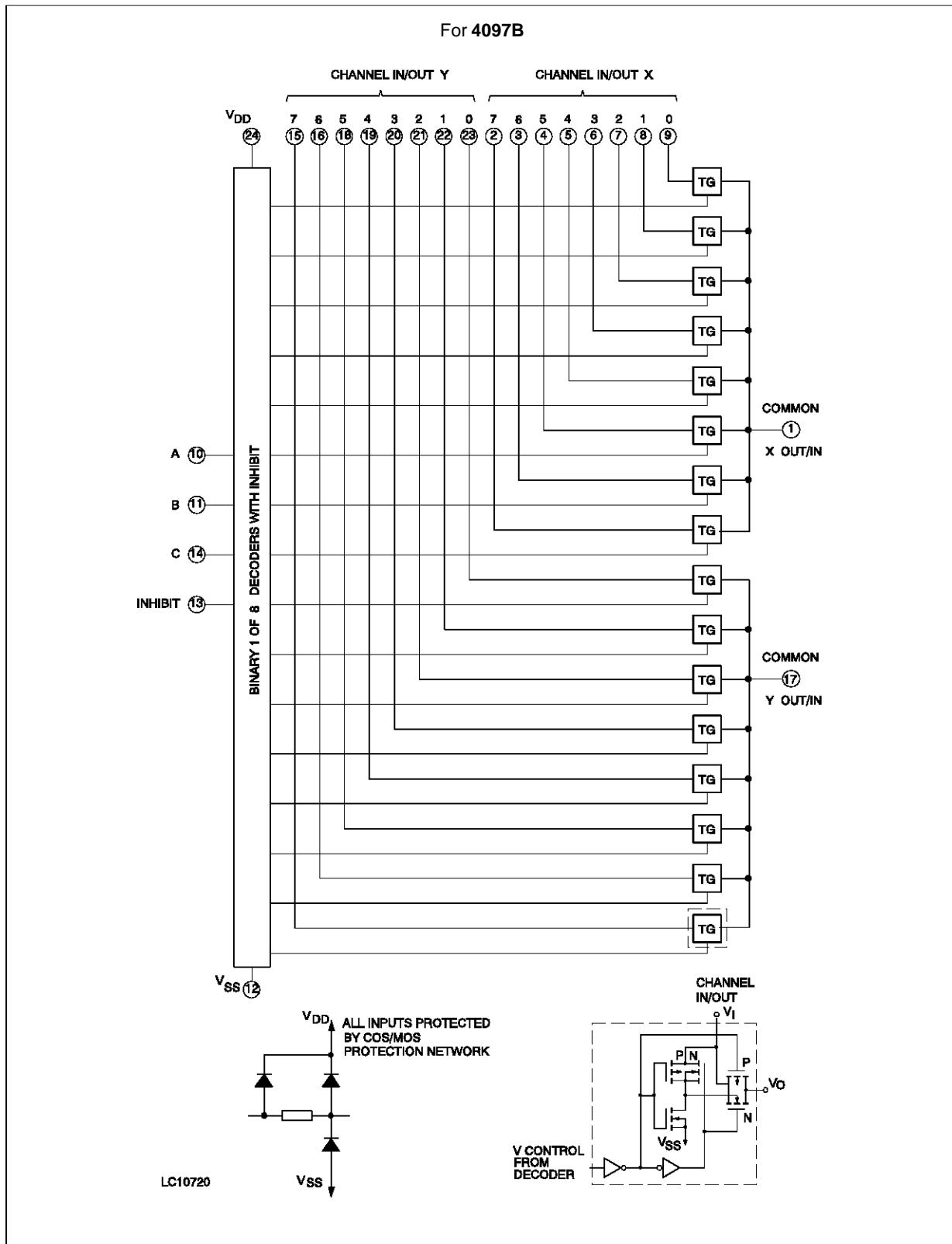
### FUNCTIONAL DIAGRAM



LOGIC DIAGRAM



LOGIC DIAGRAM



TRUTH TABLES FOR HCC/HCF4067B

A	B	C	D	INH	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

TRUTH TABLE FOR HCC/HCF4097B

A	B	C	INH	SELECTED CHANNEL
X	X	X	1	None
0	0	0	0	0X 0Y
1	0	0	0	1X 1Y
0	1	0	0	2X 2Y
1	1	0	0	3X 3Y
0	0	1	0	4X 4Y
1	0	1	0	5X 5Y
0	1	1	0	6X 6Y
1	1	1	0	7X 7Y

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V <sub>DD</sub> *	Supply Voltage: HCC Types HCF Types	-0.5 to +20	V
		-0.5 to +18	V
V <sub>I</sub>	Input Voltage	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>I</sub>	DC Input Current (any one input)	± 10	mA
P <sub>tot</sub>	Total Power Dissipation (per package) Dissipation per Output Transistor for Top = Full Package Temperature Range	200	mW
		100	mW
T <sub>op</sub>	Operating Temperature: HCC Types HCF Types	-55 to +125	°C
		-40 to +85	°C
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.





\* All voltage values are referred to V<sub>SS</sub> pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	Supply Voltage: HCC Types HCF Types	3 to 18	V
		3 to 15	V
V <sub>I</sub>	Input Voltage	0 to V <sub>DD</sub>	V
T <sub>op</sub>	Operating Temperature: HCC Types HCF Types	-55 to +125	°C
		-40 to +85	°C



**DYNAMIC ELECTRICAL CHARACTERISTICS** (T<sub>amb</sub> = 25 °C, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200 KΩ, typical temperature coefficient for all V<sub>DD</sub> values is 03 %/°C, all input rise and fall times= 20 ns)

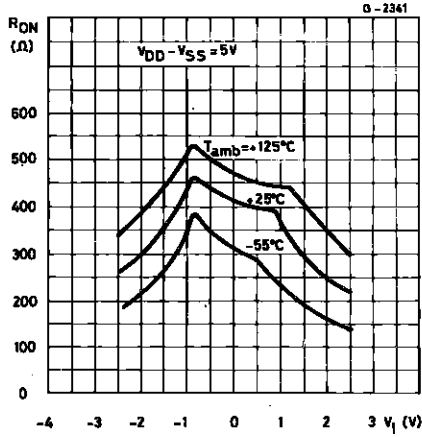
Symbol	Parameter	Test Conditions						Value		Unit	
		V <sub>C</sub> (V)	R <sub>L</sub> (KΩ)	f <sub>i</sub> (KHz)	V <sub>i</sub> (V)	V <sub>SS</sub> (V)	V <sub>DD</sub> (V)	Typ.	Max.		
<b>SWITCH</b>											
t <sub>pd</sub>	Propagation Delay Time (Signal Input to Output)	= V <sub>DD</sub>	200			0	5 10 15		30 15 11	60 30 20	ns
	Frequency Response Channel "ON" (Sine Wave Input) at $20 \text{ Log } \frac{V_O}{V_I} = -3 \text{ dB}$	= V <sub>DD</sub>	1		5 (●)	0	10	V <sub>O</sub> at Common OUT/IN 4067B 4097B	14 20		ns
	Feedthrough (All Channels OFF) at $20 \text{ Log } \frac{V_O}{V_I} = -40 \text{ dB}$	= V <sub>SS</sub>	1		5 (●)	0	10	V <sub>O</sub> at Any Channel	60		MHz
	Frequency Signal Crosstalk at $20 \text{ Log } \frac{V_{\alpha(B)}}{V_{I(A)}} = -40 \text{ dB}$	V <sub>C(A)</sub> =V <sub>DD</sub> V <sub>C(B)</sub> =V <sub>SS</sub>	1		5 (●)	0	10	Between Any two (A and B) Channels Between Sections (A and B) 4097B only	1 10 18		MHz
t <sub>w</sub>	Sine Wave Distortion (f <sub>is</sub> = 1KHz sine wave)	5 10 15	10	1	2 (●) 3 (●) 5 (●)	0	5 10 15		0.3 0.2 0.12		%
<b>CONTROL (address or Inhibit)</b>											
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time: Address or Inhibit to Signal OUT (Channel Turning ON)		1				0 0 0	5 10 15	325 135 95	650 270 190	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time: Address or Inhibit to Signal OUT (Channel Turning OFF)		0.3				0 0 0	5 10 15	220 90 65	440 180 130	ns
	Address or Inhibit to Signal Crosstalk		10*				0	10	75		mV peak

(●) Peak to peak voltage symmetrical about  $\frac{V_{DD} - V_{SS}}{2}$

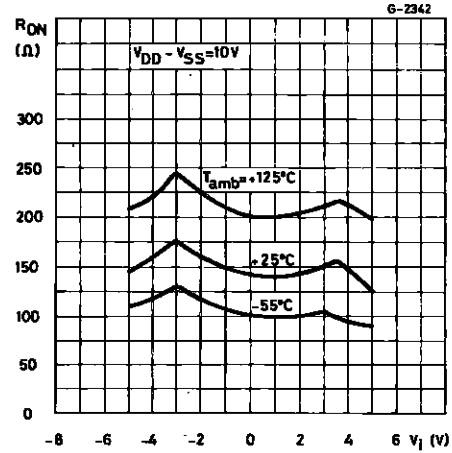
(\*) Both ends of channel

# HCC/HCF4067B HCC/HCF4097B

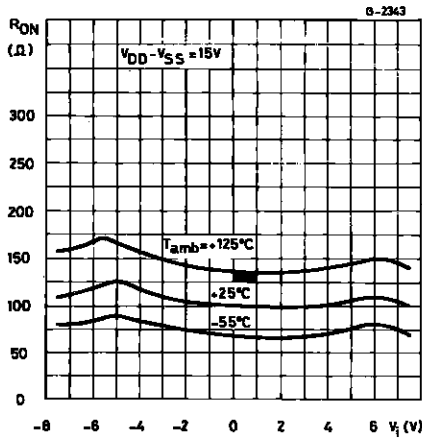
Typical ON Resistance vs Input Signal Voltage (All Types)



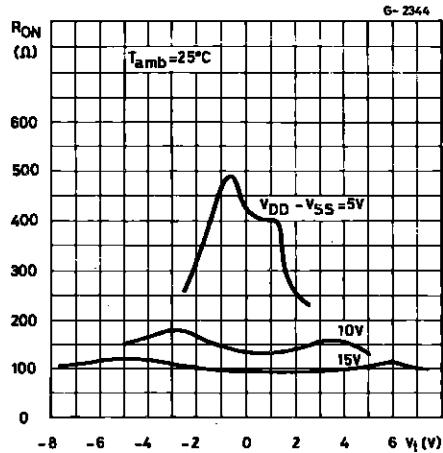
Typical ON Resistance vs Input Signal Voltage (All Types)



Typical ON Resistance vs Input Signal Voltage (All Types)

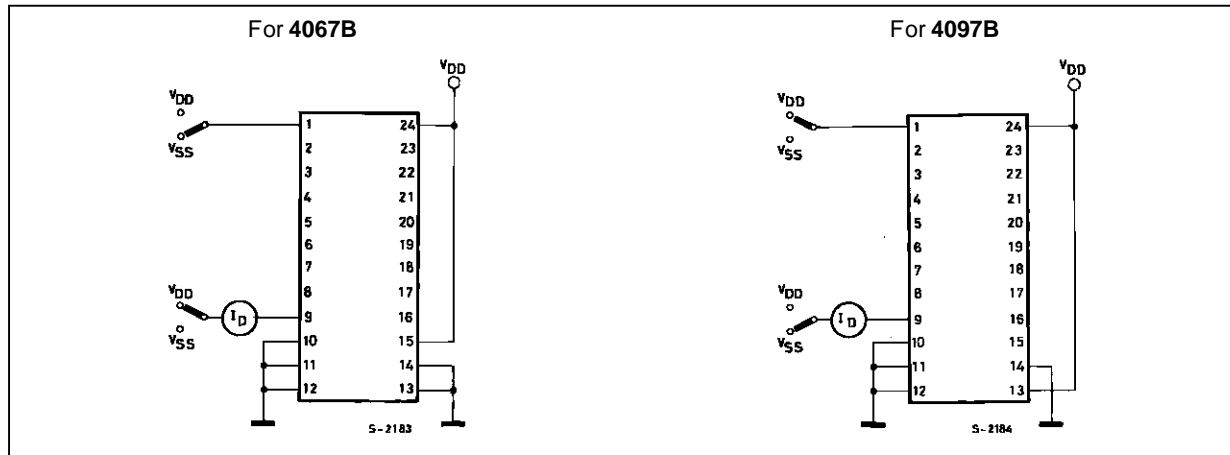


Typical ON Resistance vs Input Signal Voltage (All Types)



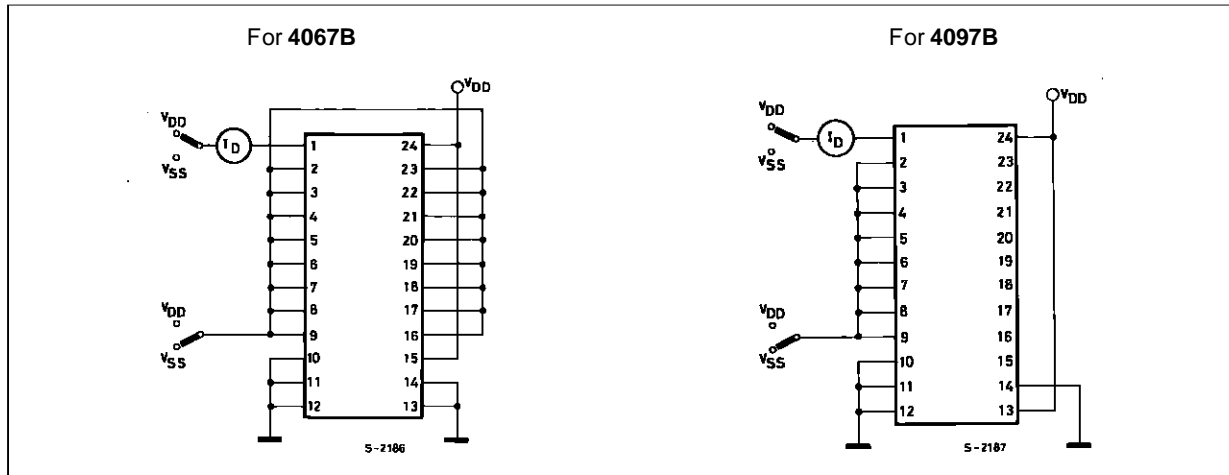
## TEST CIRCUITS

OFF Channel Leakage Current Any Channel OFF

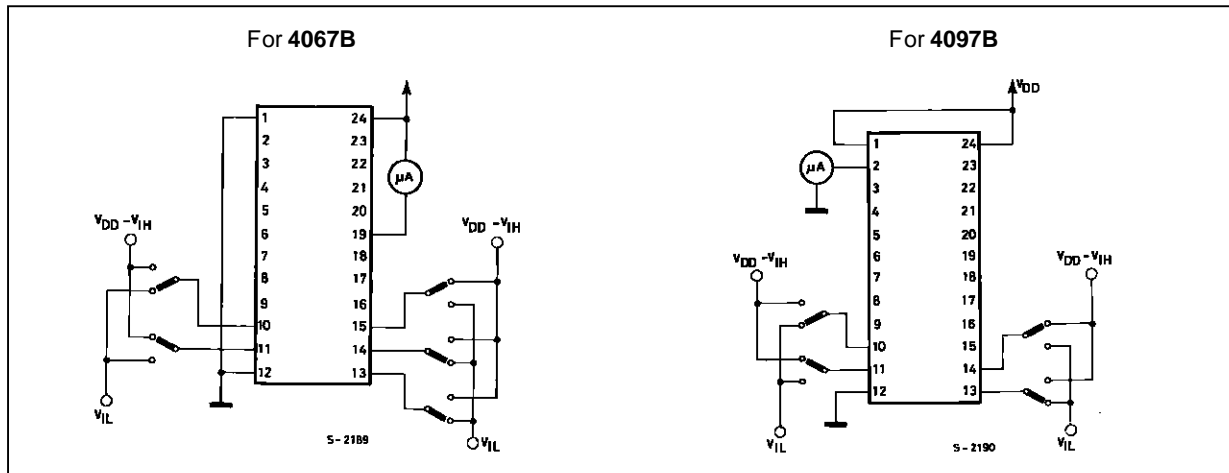




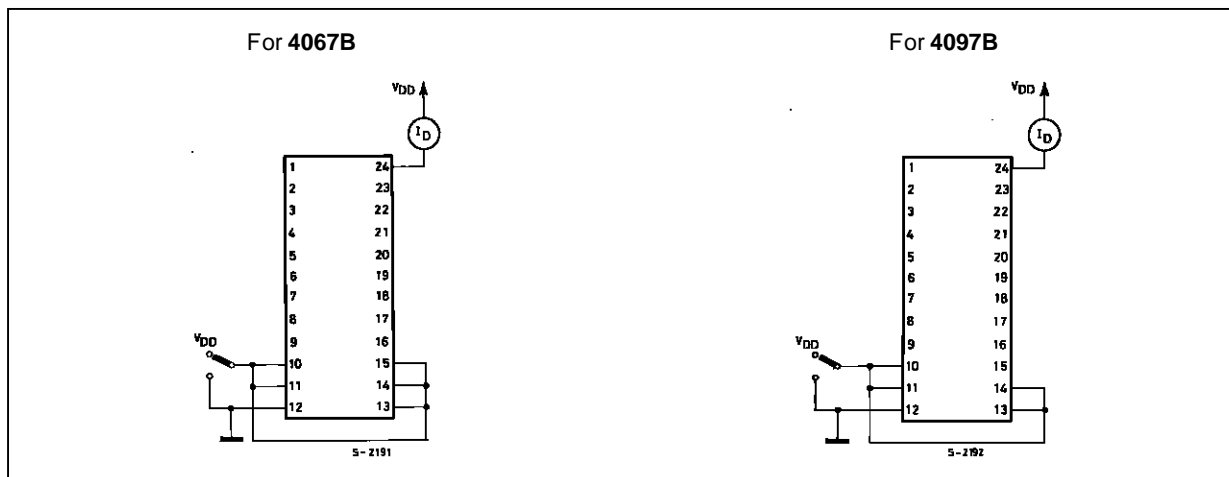
OFF Channel Leakage Current All Channels OFF



Input Voltage Measure < 2  $\mu$ A an All OFF Channels (e.g. Channel 12)

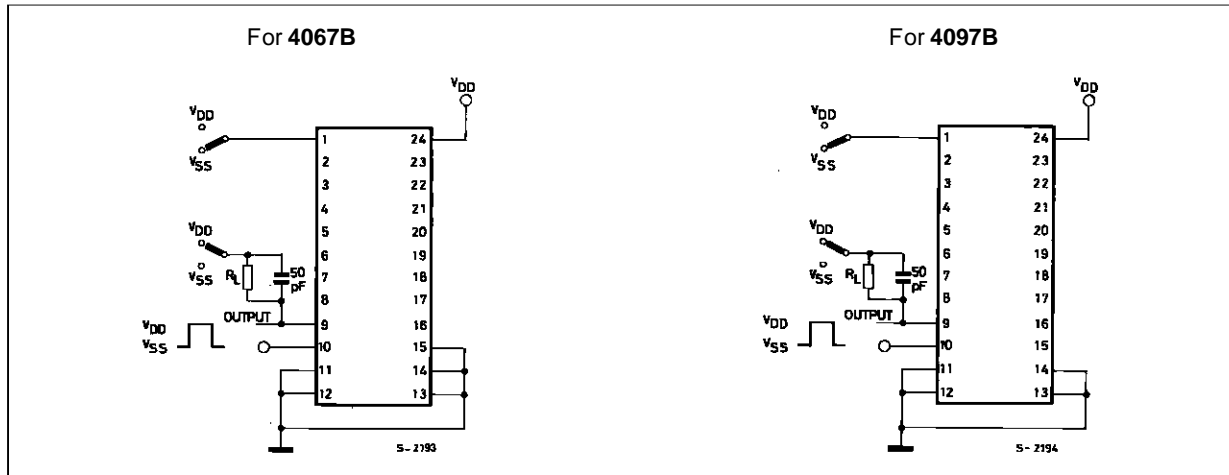


Quiescent Device Current

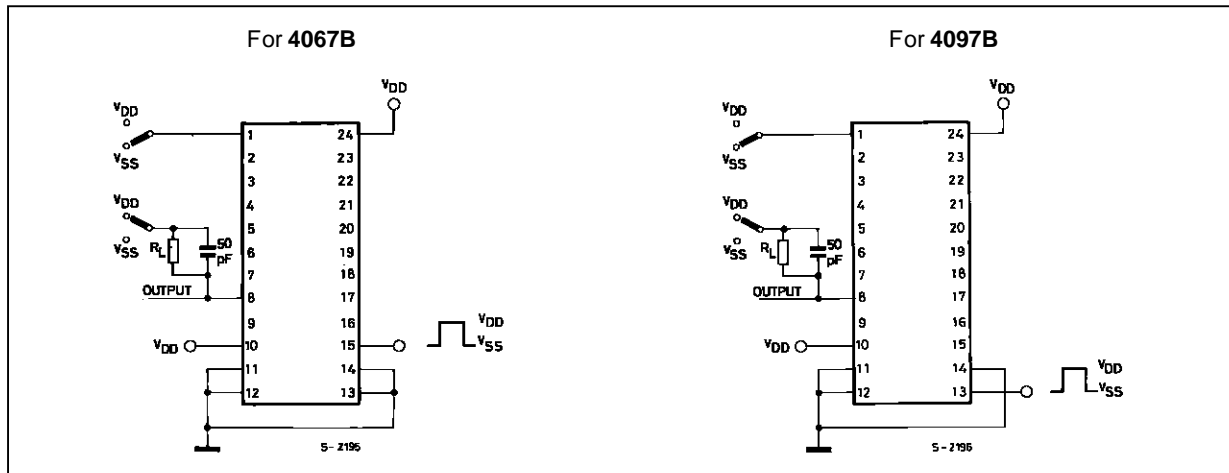


# HCC/HCF4067B HCC/HCF4097B

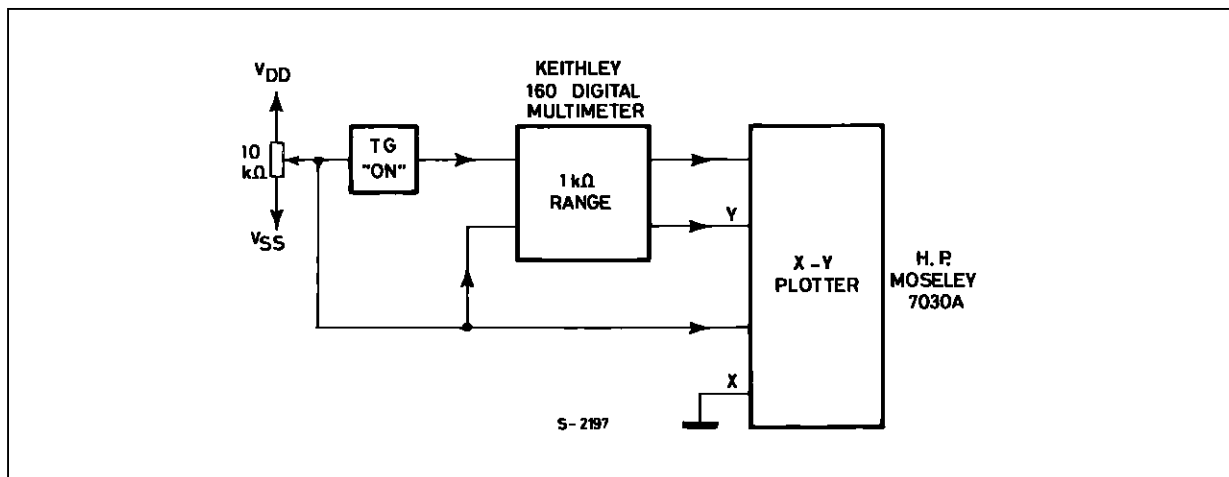
Turn-on and Turn-off Propagation Delay Address Select Input to Signal Output (e. g. Channel 0)



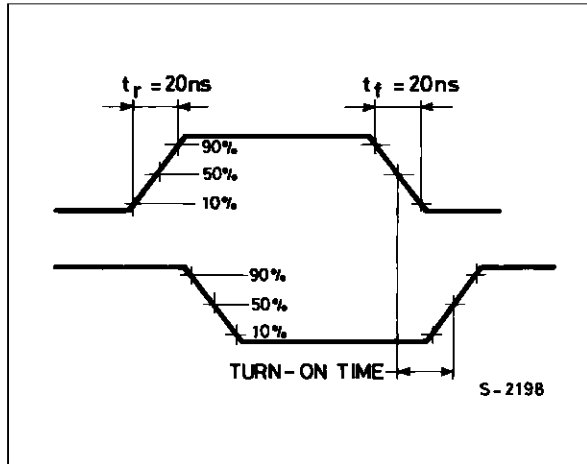
Turn-on and Turn-off Propagation Delay-Inhibit Input to Signal Output (e. g. Channel 1)



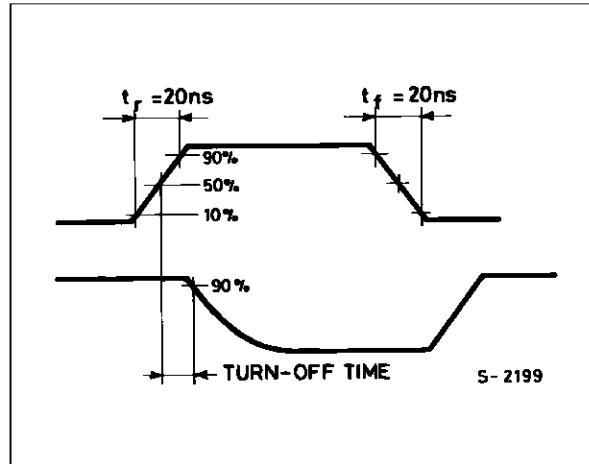
Channel ON Resistance Measurement Circuit



Propagation Delay Waveform Channel Being Turned ON ( $R_L = 10\text{ K}\Omega$ ,  $C_L = 50\text{ pF}$ )



Propagation Delay Waveform Channel Being Turned OFF ( $R_L = 300\ \Omega$ ,  $C_L = 50\text{ pF}$ )



### APPLICATIONS INFORMATION

In applications where separate power sources are used to drive  $V_{DD}$  and the signal inputs, the  $V_{DD}$  current capability should exceed  $V_{DD}/R_L$  ( $R_L =$  effective external load). This provision avoids permanent current flow or clamp action on the  $V_{DD}$  supply when power is applied or removed from the **HCC/HCF4067B** or **HCC/HCF4097B**.

When switching from one address to another, some of the ON periods of the channels of the multiplexers will overlap momentarily, which may be objectionable in certain applications. Also when a channel is turned ON or OFF by an address input, there is a momentary conductive path from the channel to  $V_{SS}$ , which will dump some charge from any capacitor connected to the input or output of the channel. The inhibit input turning on a channel will similarly dump some charge to  $V_{SS}$ .

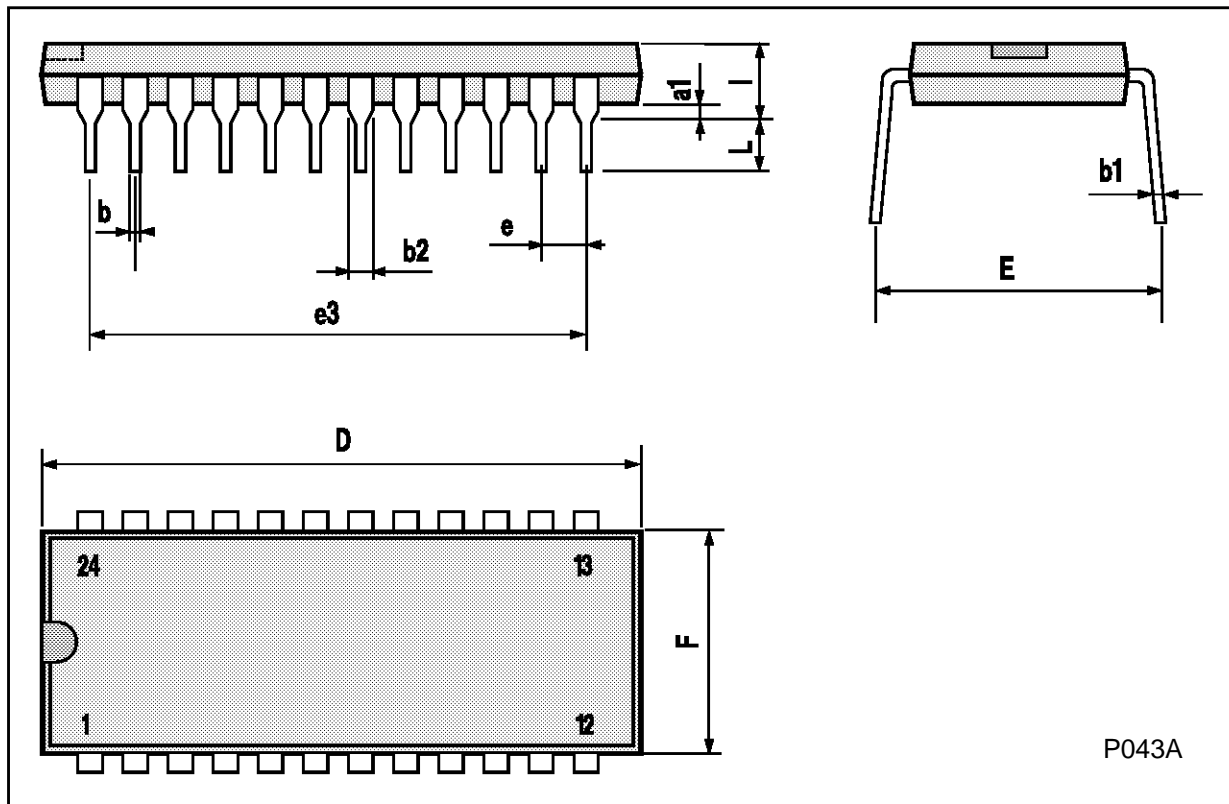
The amount of charge dumped is mostly a function of the signal level above  $V_{SS}$ . Typically, at  $V_{DD} - V_{SS} = 10\text{V}$ , a  $100\text{ pF}$  capacitor connected to the input or output of the channel will

lose 3-4% of its voltage at the moment the channel turns ON or OFF. This loss of voltage is essentially independent of the address or inhibit signal transition time, if the transition time is less than 1-2  $\mu\text{s}$ . When the inhibit signal turns a channel off, there is no charge dumping of  $V_{SS}$ . Rather, there is a slight rise in the channel voltage level (65 mV typ.) due to the capacitance coupling from inhibit input to channel input or output. Address input also couples some voltage steps onto the channel signal levels.

In certain applications, the external load-resistor current may include both  $V_{DD}$  and signal line components. To avoid drawing  $V_{DD}$  current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 V (calculated from  $R_{ON}$  values shown in ELECTRICAL CHARACTERISTICS CHART). No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into terminal 1 on the **HCC/HCF4067B**, terminals 1 and 17 on the **HCC/HCF4097B**.

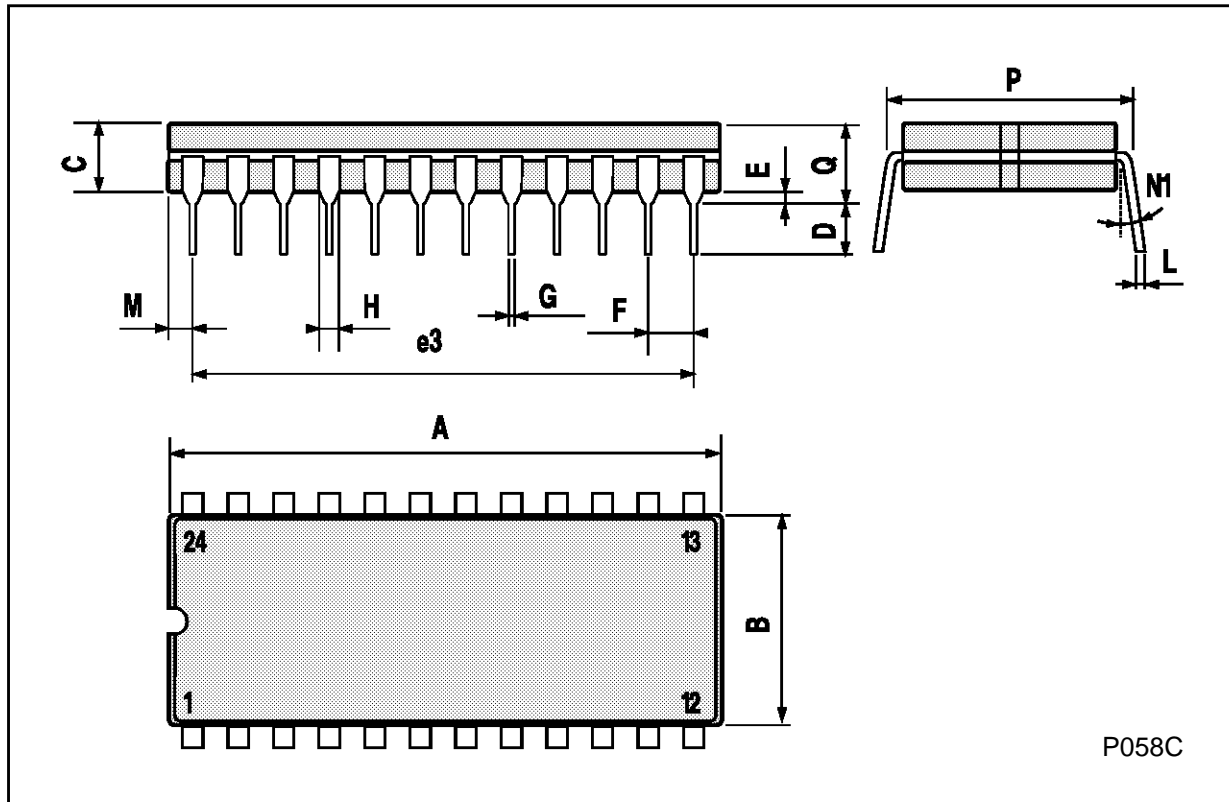
**Plastic DIP24 (0.25) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
l		4.445			0.175	
L		3.3			0.130	



**Ceramic DIP24 MECHANICAL DATA**

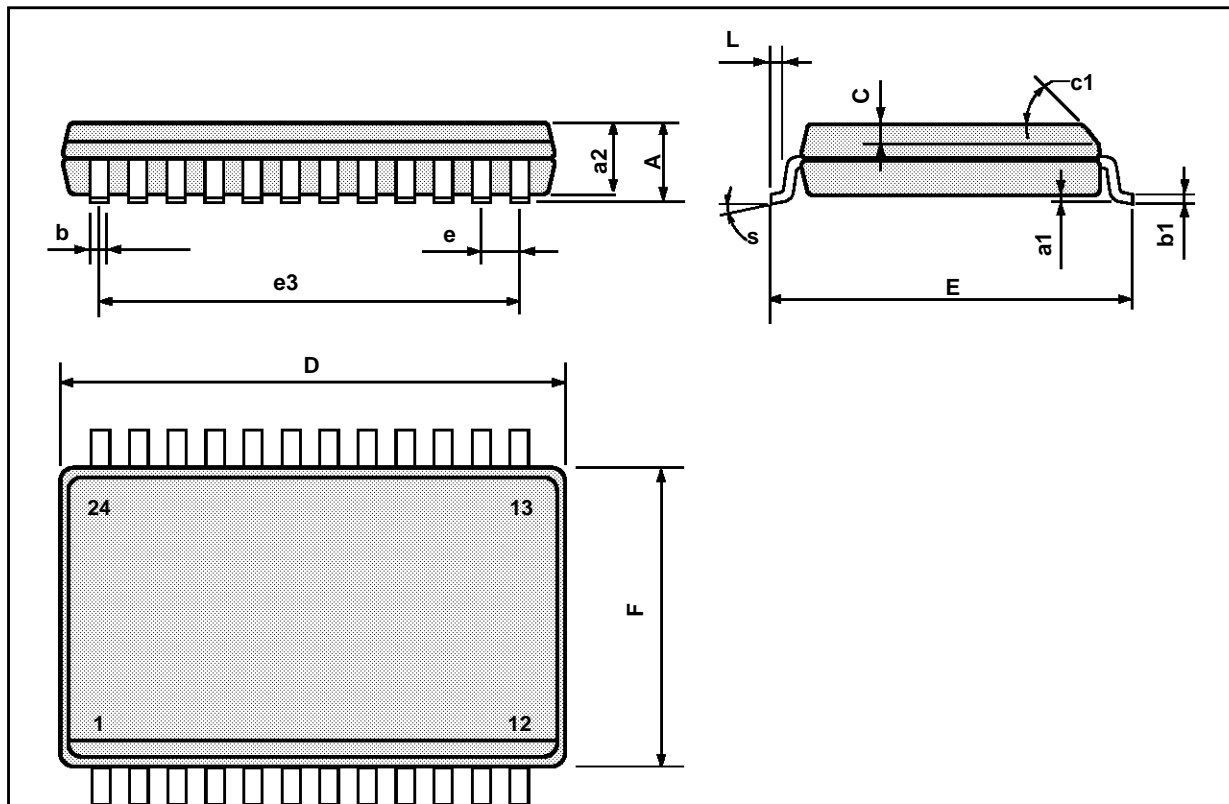
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			32.3			1.272
B	13.05		13.36	0.514		0.526
C	3.9		5.08	0.154		0.200
D	3			0.118		
E	0.5		1.78	0.020		0.070
e3		27.94			1.100	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N1	4° (min.), 15° (max.)					
P	15.4		15.8	0.606		0.622
Q			5.71			0.225



P058C

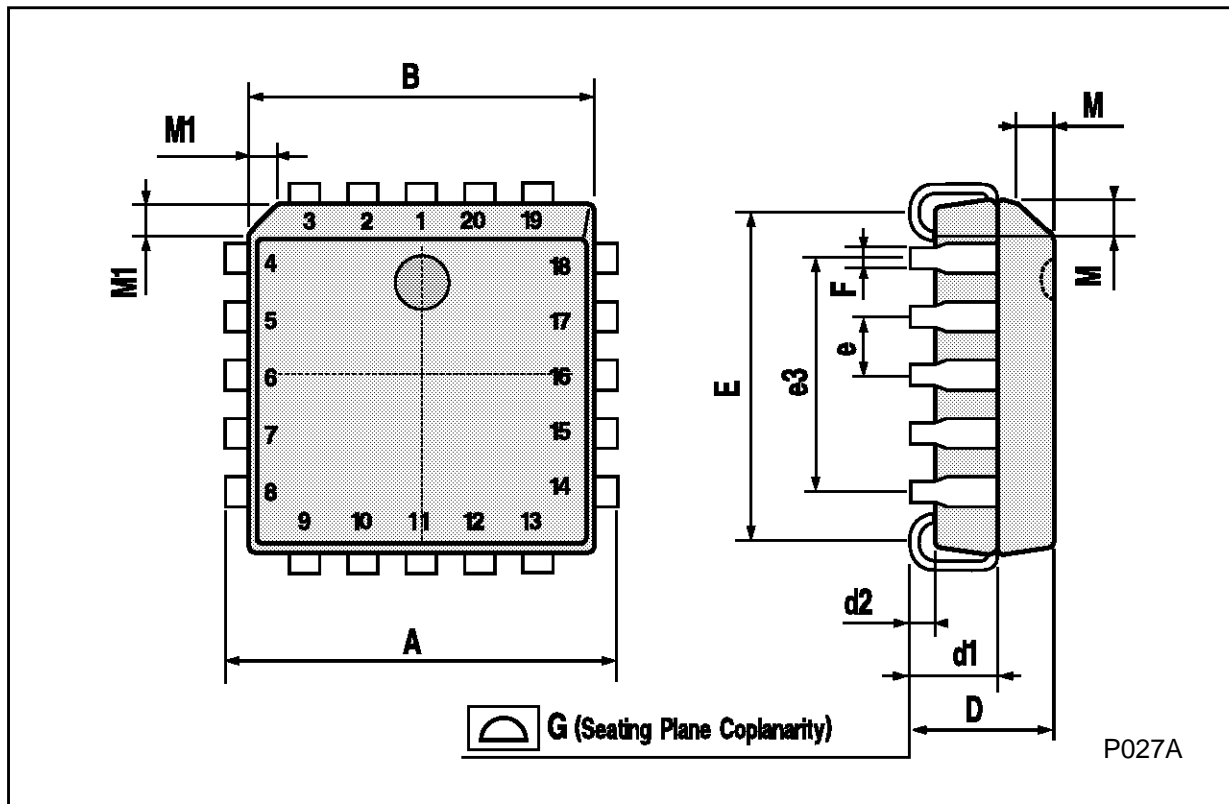
SO24 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.420
e		1.27			0.05	
e3		13.97			0.55	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
S	8° (max.)					



**PLCC20 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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