LM125 Precision Dual Tracking Regulator

National Semiconductor
Application Note 82
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INTRODUCTION

The LM125 is a precision, dual, tracking, monolithic voltage regulator. It provides separate positive and negative regulated outputs, thus simplifying dual power supply designs. Operation requires few or no external components depending on the application. Internal settings provide fixed output voltages at ±15V.

Each regulator is protected from excessive internal power dissipation by a thermal shutdown circuit which turns off the regulator whenever the chip reaches a preset maximum temperature. Other features include both internal and external current limit sensing for device protection while operating with or without external current boost. For applications requiring more current than the internal current limit will allow, boosted operation is possible with the addition of a one NPN pass transistor per regulator. External resistors sense load current for controlling the limiting circuitry. Internal frequency compensation is provided on both positive and negative regulators. The internal voltage reference pins is brought out to facilitate noise filtering when desired.

CIRCUIT DESCRIPTION

Figure 1 shows a block diagram of the basic dual tracking regulator. A voltage reference establishes a fixed dc level, independent of supply or temperature variations, at the noninverting input to the negative regulator Error Amplifier. The Error Amplifier drives the Output Control Circuit which includes the high current output transistors, current limiting, and thermal shutdown circuitry.

The negative regulator output voltage is established by comparing the Voltage Reference against a fraction of the output as set by R_A and R_B. To achieve the desired tracking action of the positive regulator, a voltage established between the positive and negative regulator outputs by resistors R_C and R_D is compared to ground by the positive regulator Error Amplifier. This insures that the positive regulator output voltage will always equal the negative regulator output voltage multiplied by the unity ratio of R_C to R_D. The positive regulator Output Control Circuit is essentially the same as that in the negative regulator.

The current limit and thermal shutdown circuitry sense the output load current and die temperature respectively and

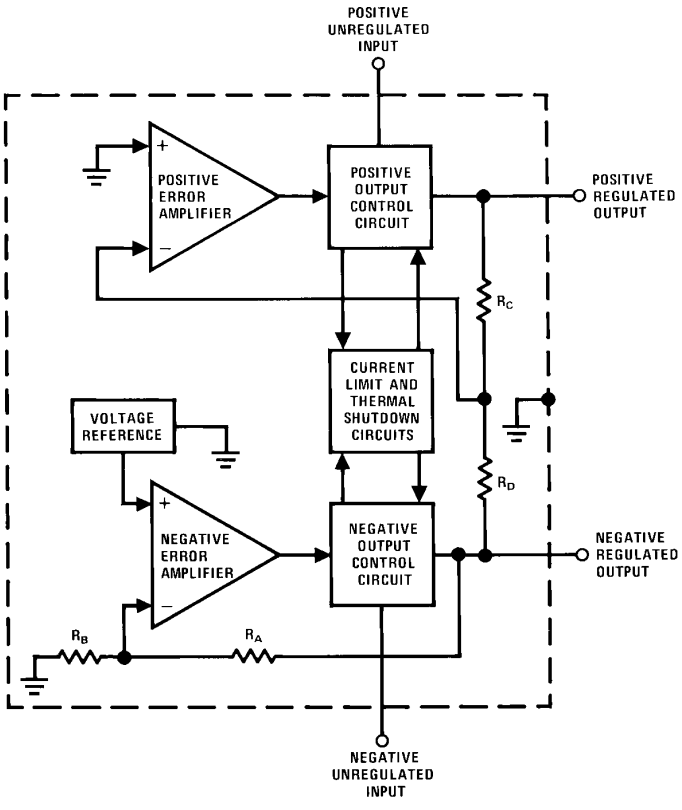

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FIGURE 1. Block Diagram for the Basic Dual Tracking Regulator

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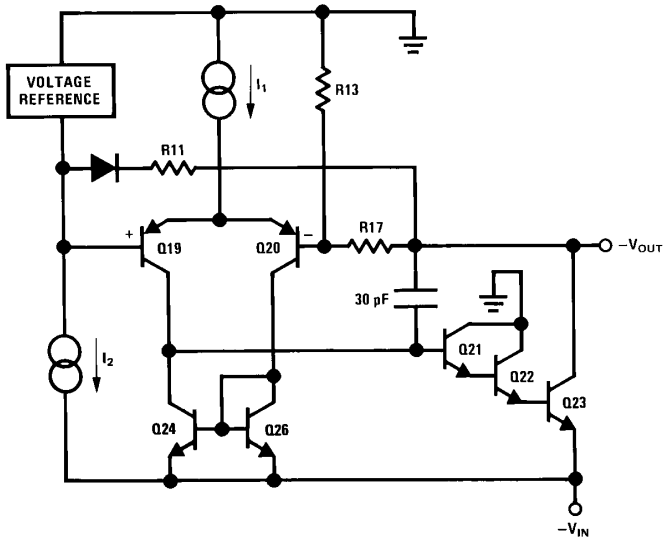

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FIGURE 2. Simplified Negative Regulator

switch off all output drive capability upon reaching their predetermined limits.

Figure 2 gives a more detailed picture of the negative regulator circuitry. The temperature compensated reference voltage appears at the non-inverting input of the differential amplifier, Q19 and Q20, while an error signal proportional

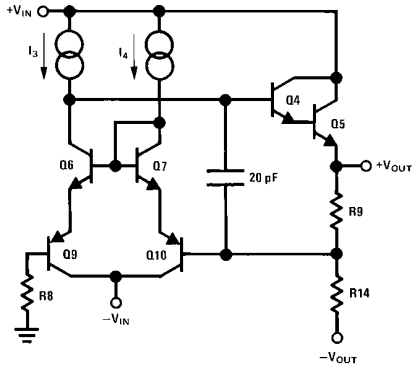

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FIGURE 3. Simplified Positive Regulator

to any change in output voltage is applied to the other input. This error signal is amplified by the differential amplifier, Q19 and Q20, and by the triple Darlington Q21, Q22, Q23 to produce a current change through R13 and R17 which brings the output voltage back to its original value. Loop gain is high, typically 88 dB at low output currents, so a 30 pF compensating capacitor is used to guarantee stability. Since $-V_{OUT}$ is the output of a high gain feedback amplifier, high supply rejection is ensured.

Figure 3 shows the basic positive regulator. This is actually an inverting operational amplifier. The negative regulated voltage ($-V_{OUT}$) is applied to the current summing input through R14 while the output ($+V_{OUT}$) is fed-back via R9. Then $+V_{OUT}$ is simply — (R9/R14) ($-V_{OUT}$). Any change in the positive regulator output will create an error signal at the base of Q10 which will be amplified and sent to the voltage follower, Q4 and Q5, forcing the output voltage to track the input voltage. Here the loop gain is on the order of 66 dB so a compensating capacitor of approximately 20 pF is used to ensure amplifier stability.

The circuitry used for regulator start up, biasing, temperature sensing, and thermal shutdown is shown in *Figure 4*. The field effect transistor Q28, is initially ON allowing the negative input voltage to force current through zener diode Q34. When enough current flows to fully establish the zener voltage, transistor Q29, Q30 and Q31 turn on and bias up all current sources. The zener voltage also decreases the gate to source voltage of the FET, pinching it off to a lower current value to reduce quiescent power dissipation.

The thermal sensing and shutdown circuitry is comprised of Q34, Q29, Q35, Q32, Q37, Q38, R27, R29, R30, R31, and R33. The voltage divider made up of R29 and R30 provides a relatively fixed bias voltage V_1 at the bases of Q35 and Q36, holding them in the OFF state. When the chip temperature increases to a maximum permissible level, the base to emitter voltage of Q35 and/or Q36 will have decreased sufficiently so that V_1 is now high enough to turn them ON. This causes a voltage drop across R27 sufficient to turn on Q32 which switches Q37 and Q38 to a conducting state shunting all output drive current to $-V_{IN}$. The regulator output voltages are then clamped to zero. Transistors Q35 and Q36 are located on the chip near the regulator output devices so they will see the maximum temperatures reached on the chip, ensuring that neither regulator will ever see more than this preset maximum temperature. The collectors of Q35 and Q36 are tied together so that if either regulator reaches the thermal shutdown temperature, both regulators will shutdown. This ensures that the device can never be destroyed because of excessive internal power dissipation in either regulator.

Figure 5 shows the current limiting circuitry used in the positive regulator; the negative regulator current limiter is identical. The internal current limiter is comprised of Q8 and R5; the external current limiter is comprised of Q11 and an external resistor R_{CL}. Both operate in a similar manner. As the

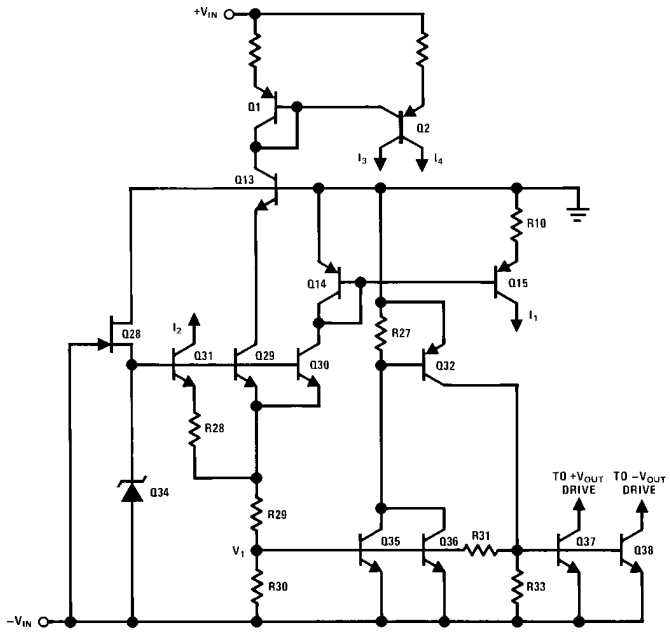

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FIGURE 4. Start-up, Biasing and Thermal Shutdown Circuitry

output current through Q5 increases, the voltage drop across resistor R5 eventually turns ON Q8 and shunts all base drive away from the output devices, Q4 and Q5. The maximum load current available with this circuit is approximately 250 mA at $T_j = 25°C$ (see *Figure 9*).

The external current limiting circuit works in a similar manner. Here the output current is sensed across the external resistor R_{CL}. When the voltage drop across R_{CL} is sufficient to turn ON transistor Q11, the output drive current is switched away from the output devices Q4 and Q5. This externally set current limit is particularly valuable when used with an external current boosting pass transistor where the current limit could be set to protect that transistor from excessive power dissipation.

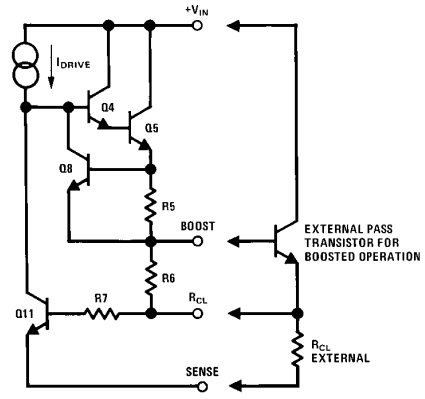

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FIGURE 5. Positive Regulator Current Limiting Circuitry

The constant voltage reference circuit is shown in *Figure 6*. Zener diode Z_1 has a positive temperature coefficient of known value. V_{BE} of Q18 (negative temperature coefficient) is multiplied by the ratio of R18 and R19 and added to the positive TC of Z_1 to produce a near zero TC voltage reference. Current source I_2 is used only during start-up.

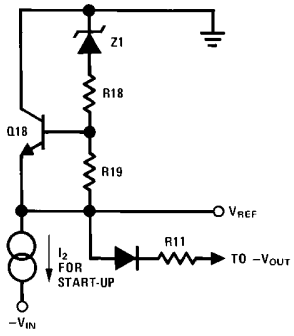

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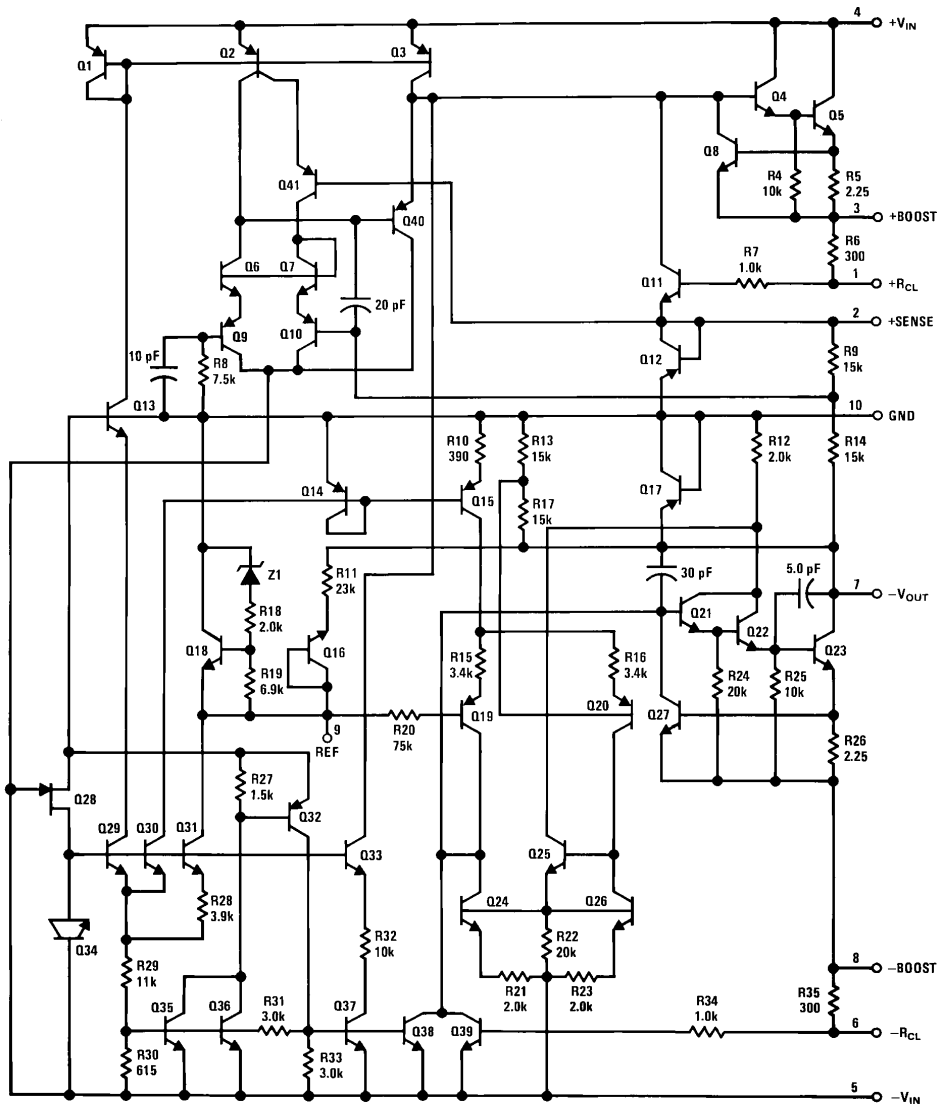
FIGURE 6. Voltage Reference Circuitry

Figure 7 shows the complete schematic of the LM125 dual regulator. Diodes Q12 and Q17 protect the output transistors, plus any external pass devices used, from breakdown in the event the positive and negative regulated outputs become shorted. Transistors Q6 and Q7 offer full differential voltage gain with the convenience of single ended output. Transistors Q13 and Q33 insure that operation with ±30V input is possible. Q24 and Q26 in the negative regulator amplifier provide single ended output from a differential input with no loss in gain.

APPLICATIONS

The basic dual regulator is shown connected in *Figure 8.* The only connections required other than plus and minus inputs, outputs, and ground are to complete the output current paths from $+R_{CL}$ to $+V_{OUT}$ and from $-R_{CL}$ to $-V_{IN}$. These may be a direct shorts if the internal preset current limit is desired, or resistors may be used to set the maximum current at some level less than the internal current limit. The internal 300Ω resistors from pins 3 to 1 and pins 8 to 6 should be shorted as shown when no external pass transistors are used. To improve line ripple rejection and transient response, filter capacitors may be added to the inputs, out-



Note: Pin numbers apply to metal can package only. TL/H/7390–7

FIGURE 7. LM125

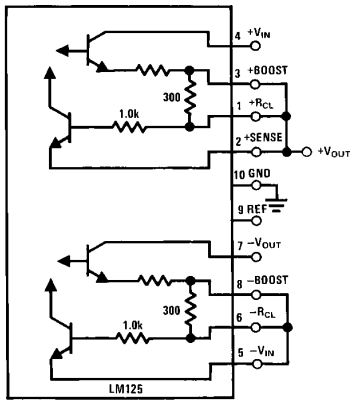


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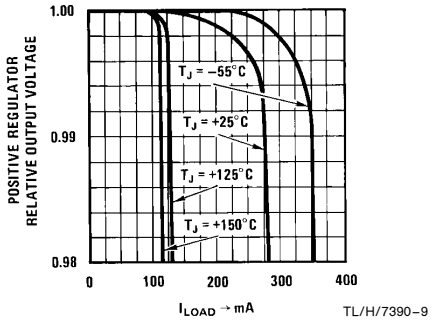
FIGURE 8. Basic Dual Regulator

puts, or both, depending on the unregulated input available. If a very low noise output voltage is desired, a capacitor may be connected from the reference voltage pin to ground. Thus shunting noise generated by the reference zener. *Figure 9* shows the internal current limiting characteristics for the basic regulator circuit of *Figure 8*.

HIGH CURRENT REGULATOR

For applications requiring more supply current than can be delivered by the basic regulator, an external NPN pass transistor may be added to each regulator. This will increase the maximum output current by a factor of the external transistor beta. The circuit for current boosted operation is shown in *Figure 10*.

In the boosted mode, current limiting is often a necessary requirement to insure that the external pass device is not overheated or destroyed. Experience shows this to be the usual cause of IC regulator failure. If the regulator output is grounded the pass device may fail and short, destroying the regulator. To limit the maximum output current, a series resistor (R_{CL} in *Figure 10*) is used to sense load current. The regulator will current limit when the voltage drop across R_{CL}



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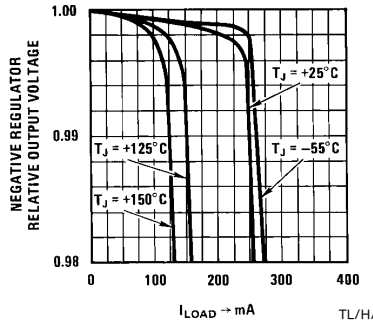
(a)



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(b)

FIGURE 9. Internal Current Limiting Characteristics

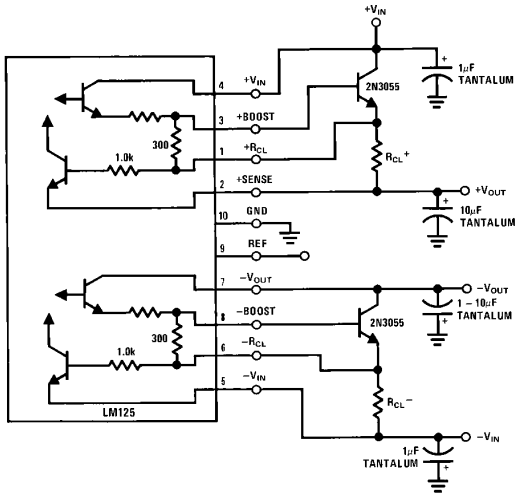

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FIGURE 10. Boosted High Current Regulator

equals the current limit sense voltage found in *Figure 11*. *Figure 12* shows the external current limiting characteristics unboosted and *Figure 13* shows the external current limiting characteristics in the boosted mode.

To ensure circuit stability at high currents in this configuration, it may be necessary to bypass each input with low inductance, tantalum capacitors to prevent forming resonant circuits with long input leads. A C $\geq$ 1 μF is recommended. The same problem can also occur at the regulator output where a C $\geq$ 10 μF tantalum will ensure stability and increase ripple rejection.

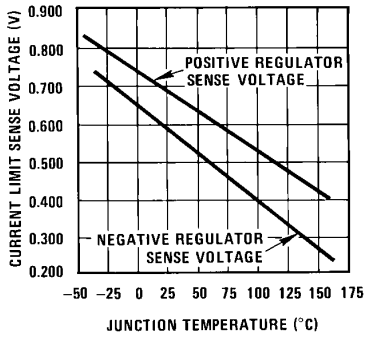

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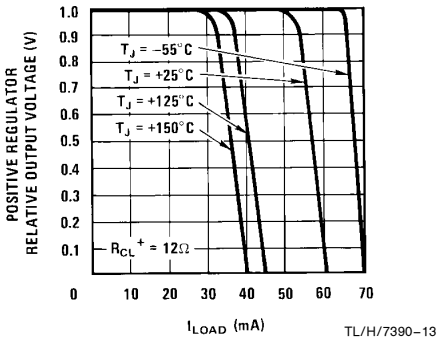
FIGURE 11. Current Limit Sense Voltage for a 0.1% Change in Regulated Output Voltage

The 2N3055 pass device is low in cost and maintains a reasonably high beta at collector currents up to several amps. The devices 2N3055 may be of either planar or alloy junction construction. The planar devices, have a high f_T providing more stable operation due to low phase shift. The alloy devices, with f_T typically less than 1.0 MHz, may require additional compensation to guarantee stability. The simplest of compensation for the slower devices is to use output filter capacitor values greater than 50 μF (tantalum). An alternative is to use an RC filter to create a leading phase response to cancel some of the phase lag of the devices. The stability problem with slower pass transistors, if it occurs at all, is usually seen only on the negative regulator. This is because the positive regulator output stage is a conventional Darlington while the negative output stage contains three devices in a modified triple Darlington connection giving slightly more internal phase shift. Additional compensation may be added to the negative regulator by connecting a small capacitor in the 100 pF range from the negative boost terminal to the internal reference. Since the positive regulator uses the negative regulator output for a reference, this also offers some additonal indirect compensation to the positive regulator.

7 AMP REGULATOR

In *Figure 14* the single external pass transistor has been replaced by a conventional Darlington using a 2N3715 and



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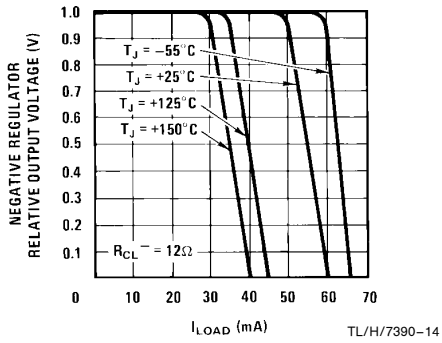
(a)



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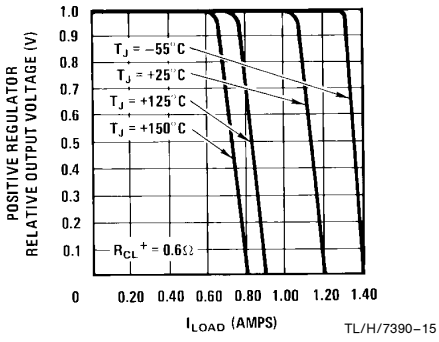
(b)

FIGURE 12. External Current Limiting Characteristics-Unboosted



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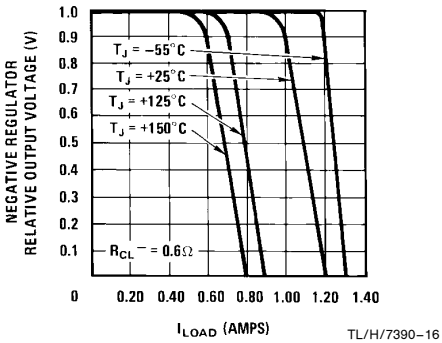
(a)



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(b)

FIGURE 13. External Current Limiting Characteristics-Boosted

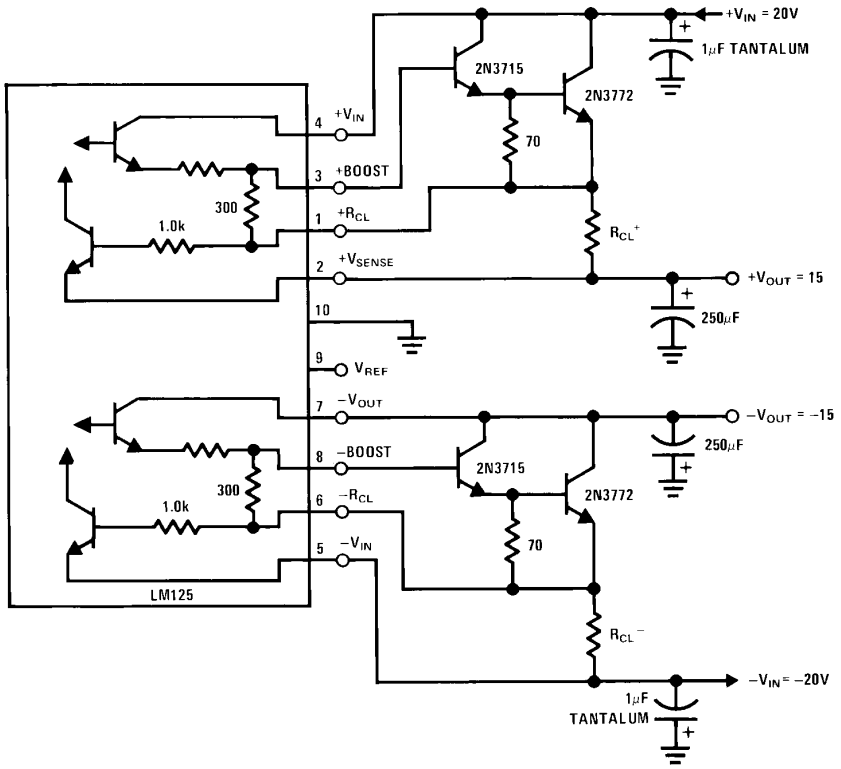

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FIGURE 14. High Current Regulator Using a Darlington Pair for Pass Elements

a 2N3772. With this configuration the output current can reach values to 10A with very good stability. The external Darlington stage increases the minimum input-output voltage differential to 4.5V. When current limit protection resistor is used, as in *Figure 14*, the maximum output current is limited by power dissipation of the 2N3772 (150W at 25°C). During normal operation this is $(V_{IN} - V_{OUT})\ I_{OUT}$ (W), but it increases to $V_{IN}\ I_{SC}$ (W) under short circuit conditions. The short circuit output current is then:

$$I_{SC} = \frac{P_{MAX}\ (T_C = 25°C)}{V_{IN}}$$

$$= \frac{150W}{20V\ (min)} = 7.5A\ max.$$

I_L could be increased to 10A or more only if $I_{SC} < I_L$. A foldback current limit circuit will accomplish this. The typical load regulation is 40 mV from no load to a full load. (T_j = 25°C, pulsed load with 20 ms t_{ON} and 250 ms t_{OFF}).

FOLDBACK CURRENT LIMITING

In many regulator applications, the normal operation power dissipation in the pass device can easily be multiplied by a factor of ten or more when the output is shorted. This may destroy the pass device, and possibly the regulator, unless the heat sink is oversized to handle this fault condition. A foldback current limiting circuit reduces short circuit output current to a fraction of the full load output current thus avoiding the need for larger heat sink. *Figure 15* shows a foldback current limiting circuit on both positive and negative regulators.

The foldback current limiting, a fraction of the output voltage must be used to oppose the voltage across the current limit sense resistor. Current limiting does not occur until the voltage across the sense resistor is higher than this opposing voltage by the amount shown in *Figure 11*. When the output is grounded, the opposing voltage is no longer present so current limiting occurs at a lower level. This is accomplished in *Figure 15* by using a programmable current source to give a constant voltage drop across R5 for the negative regulator, and by a simple resistor divider for the positive regulator. The reason for the difference between the two is that the negative regulator current limiting circuit is located between the output pass transistor and the unregulated input while the positive regulator current limiter is between the output pass transistor and the regulated output.

The operation of the positive foldback circuit is similar to that described in NSC application note AN-23. A voltage divider R1 and R2 from V_E to ground creates a fixed voltage drop across R1 opposite in polarity to the drop across $R_{CL}{}^+$. When the load current increases to the point where the drop across $R_{CL}{}^+$ is equal to the drop across R1 plus the current limit sense voltage given in *Figure 11*, the positive regulator will begin to current limit. As the positive output begins to drop, the voltage across R1 will also decrease so that it now requires less load current to produce the cur-

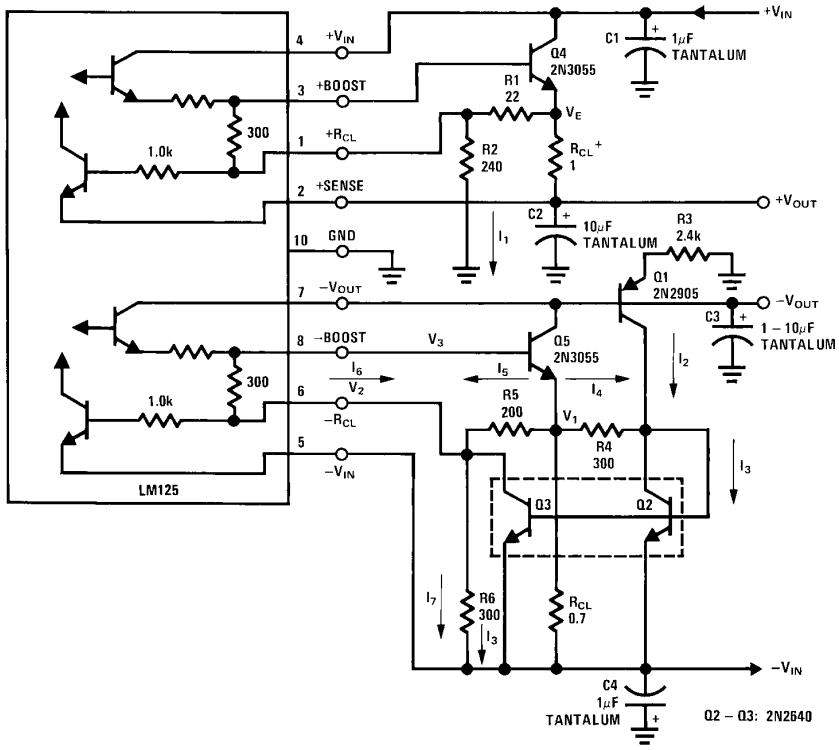

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FIGURE 15. Foldback Current Limiting Circuit

rent limit sense voltage. With the regulator output fully shorted to ground ($+V_{OUT} = 0$) the current limit will be set by the value of $+R_{CL}$ alone.

If $$\frac{I_{FB}}{I_{SC}} \leq 5$$

then the following equations can be used for calculating the positive regulator foldback current limiting resistors.

$$R_{CL}{}^{+} = \frac{V_{SENSE}}{I_{SC}} \quad (1)$$

where V_{SENSE} is from *Figure 11*.

At the maximum load current foldback point:

$$V_{RCL}{}^{+} = I_{FB}\, R_{CL}{}^{+} \quad (2)$$

$$V_{R1} = V_{RCL}{}^{+} - V_{SENSE} \quad (3)$$

$$V_{R1} = I_{FB}\, R_{CL}{}^{+} - V_{SENSE} \quad (4)$$

Then

$$R1 = \frac{V_{R1}}{I_1} \quad (5)$$

and

$$R2 = \frac{+V_{OUT} + V_{SENSE}}{I_1} \quad (6)$$

The only point of caution is to ensure that the total current (I_1) through R2 is much greater than the current contribution from the internal 300Ω resistor. This can be checked by:

$$\frac{I_{FB}\, R_{CL}{}^{+}}{300} << I_1 \quad (7)$$

Note: The current from the internal 300Ω resistor is $V_{3\text{-}1}/300\Omega$, but $V_{3\text{-}1} = V_{BE} + V_{RCL} - V_{SENSE}{}^{+}$ assuming $V_{BE} \approx V_{SENSE}{}^{+}$ at the foldback point, $V_{3\text{-}1} \approx V_{RCL}{}^{+} = I_{FB}\, R_{CL}{}^{+}$.

Design example: 2 amp regulator LM125 positive foldback current limiting (see *Figure 15*).

Given:

$$I_{FOLDBACK} = 2.0A$$
$$I_{SHORT\text{-}CIRCUIT} = 500\ mA$$
$$V_{SENSE}\ (\text{See } \textit{Figure 11})$$
$$+V_{IN} = 25V$$
$$+V_{OUT} = 15V$$
$$\beta_{PASS\ DEVICE} = 70$$
$$\theta_{JA} = 150°C/W$$
$$T_A = 50°C$$

With a beta of 70 in the pass device and a maximum output current of 2.0A the regulator must deliver:

$$\frac{2A}{\beta} = \frac{2A}{70} = 29\ mA$$

The LM125 power dissipation will be calculated ignoring any negative output current for this example.

$$P_{LM125} = (V_{IN} - V_{OUT})\, I_{OUT}$$
$$= (25 - 15)\, 29\ mA$$
$$= 290\ mW$$

$$T_{RISE} @ \theta_{JA} = 150°C/W = 150°C \times 0.29 = 44°C$$
$$T_J = T_A + T_{RISE} = 50°C + 44°C = 94°C$$

From *Figure 11*:

$$V_{SENSE} @ (T_J = 94°C) = 520\ mW$$

From equation (1)

$$R_{CL}{}^{+} = \frac{V_{SENSE}}{I_{SC}} = \frac{520\ mV}{500\ mA} \cong 1\Omega$$

From equation (2)

$$V_{RCL}{}^{+} = I_{FB}\, R_{CL}{}^{+} = (2A)(1\Omega) = 2V$$

From equation (3)

$$V_{R1} = V_{RCL}{}^{+} - V_{SENSE}$$

$$V_{R1} = 2V - 520\ mV = 1.480V$$

A value for I_1 can now be found from equation (7)

$$\frac{I_{FB}\, R_{CL}{}^{+}}{300} = \frac{2A \times 1\Omega}{300\Omega} = 6.6\ mA$$

So set $I_1 = 10 \times 6.6\ mA = 66\ mA$

From equations (5) and (6)

$$R1 = \frac{V_{R1}}{I_1} = \frac{1.480V}{66\ mA} \cong 22\Omega$$

$$R2 = \frac{+V_{OUT} + V_{SENSE}}{I_1} = \frac{15 + 0.520}{66\ mA} \cong 240\Omega$$

The foldback limiting characteristics are shown in *Figure 16* for the values calculated above at various operating temperatures.

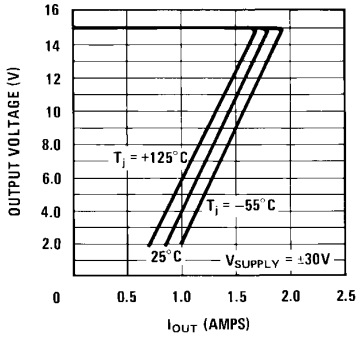

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FIGURE 16. Positive Regulator Foldback Current Limiting Characteristics

The negative regulator foldback current limiting works essentially the same way as the positive side. Q1 forces a constant current, I_2, determined by $-V_{OUT}$ and R3, through Q2. Transistors Q2 and Q3 are matched so a current identical to I_3 will flow through Q3. With the output short-circuited ($-V_{OUT} = 0$), Q1 will be OFF, setting $I_2 = 0$. The load current will be limited when V_1 increases sufficiently due to load current to make V_2 higher than $-V_{IN}$ by the current limit sense voltage.

The short circuit current is:

$$I_{SC} \cong \frac{V_{SENSE}}{R_{CL}{}^{-}} \tag{8}$$

For calculating the maximum full load current with the output still in regulation, current I_2

$$I_2 = \frac{V_{OUT} - V_{BEQ1}}{R3} \tag{9}$$

At the point of maximum load current, I_{FB}, where the regulator should start folding back:

$$V_1 = -V_{IN} + I_{FB}\, R_{CL}{}^{-} \tag{10}$$

and

$$V_2 = -V_{IN} + V_{SENSE} \tag{11}$$

The current through Q2 (and Q3) will have increased from I_2 by the amount of I_4 due to the voltage V_1 increasing above its no-load quiescent value. Since the voltage across Q2 is simply the diode drop of a base-emitter junction:

$$I_4 = \frac{[V_1 - (-V_{IN})] - V_{BE}}{R4}$$

Substituting in equation (10) gives:

$$I_4 = \frac{I_{FB}\, R_{CL}{}^{-} - V_{BE}}{R4} = \frac{I_{FB}\, R_{CL}{}^{-} - V_{BE}}{300\Omega} \tag{12}$$

The current through Q2 is now

$$I_3 = I_2 + I_4 \tag{13}$$

and the current through Q3 is:

$$I_3 = I_5 + I_6 - I_7 \tag{14}$$

The drop across R5 is found from:

$$V_1 - V_2 = (-V_{IN} + I_{FB}\, R_{CL}{}^{-}) - [V_{SENSE} + (-V_{IN})];$$

simplifying,

$$V_1 - V_2 = I_{FB}\, R_{CL}{}^{-} - V_{SENSE} \tag{15}$$

Since V_{SENSE} is the base to emitter voltage drop of the internal limiter transistor, the V_{SENSE} in equation (15) very nearly equals the V_{BE} in equation (12). Therefore the drop across R5 approximately equals the drop across R4. The current through R5, I_5, can now be determined as:

$$I_5 = \frac{I_{FB}\, R_{CL}{}^{-} - V_{SENSE}}{R5} \tag{16}$$

Summing the currents through Q3 is now possible assuming the base-emitter drop of the 2N3055 pass device can be given by $V_{BE} \approx V_{SENSE}$:

$$I_6 = \frac{V_3 - V_2}{300} \tag{17}$$

where $V_3 = V_1 + V_{BE} \approx V_1 + V_{SENSE}$

$$I_6 = \frac{V_1 + V_{SENSE} - V_2}{300}$$

Substituting in equation (15)

$$I_6 = \frac{I_{FB}\, R_{CL}{}^{-}}{300} \tag{18}$$

$$I_7 = \frac{V_2 - (-V_{IN})}{R6} = \frac{V_{SENSE}}{R6}$$

Equating equation (13) with equation (14) and inserting resistor values shown in *Figure 15*,

$$I_2 + I_4 = I_5 + I_6 - I_7$$

$$I_2 + \frac{I_{FB}\, R_{CL}^- - V_{SENSE}}{300} = I_5 + \frac{I_{FB}\, R_{CL}^-}{300} - \frac{V_{SENSE}}{300} \quad (19)$$

Canceling, we find:

$$I_2 = I_5 \quad (20)$$

This is the key to the negative foldback circuit. Current source Q1 forces current I_2 to flow through resistor R5. The voltage drop across R5 opposes the normal current limit sense voltage so that the regulator will not current limit until the drop across R_{CL}^- due to load current, equals the controlled drop across R5 plus V_{SENSE} (given in *Figure 11*). This can be written as:

$$I_{FB} = \frac{V_{SENSE} + I_2\, R5}{R_{CL}^-} \quad (21)$$

$$I_{FB} = \frac{V_{SENSE} + 200\, I_2}{R_{CL}^-}$$

A design example is now offered:

Given:

$$I_{FOLDBACK} = 2.5A$$

$$I_{SHORT\text{-}CIRCUIT} = 750\ mA$$

V_{SENSE} (See *Figure 11*)

$$-V_{IN} = 25V$$

$$-V_{OUT} = -15V$$

$$\beta_{PASS\ DEVICE} = 90$$

$$\theta_{JA} = 150°C/W$$

$$T_A = 25°C$$

The same calculations are used here to figure V_{SENSE} as with the positive regulator foldback example maximum regulator output current is calculated from:

$$I_{OUT} = \frac{2.5A}{90} = 28\ mA$$

$$P_{LM125} = (V_{IN} - V_O)\, I_{OUT} = 10V \times 28\ mA = 280\ mW$$

$$T_{RISE} = 150°C/W \times 0.28W = 42°C$$

$$T_J = T_A + T_{RISE} = 25°C + 42°C = 67°C$$

From *Figure 11*:

$$V_{SENSE} = 500\ mV$$

From equation (8):

$$R_{CL}^- = \frac{500\ mV}{750\ mA} = 0.68\Omega$$

From equation (21):

$$I_2 = \frac{I_{FB}\, R_{CL}^- - V_{SENSE}}{200\Omega} = 6.0\ mA$$

From equation (9):

$$R3 = \frac{V_{OUT} - V_{BEQ1}}{I_2}$$

$$R3 \cong \frac{14.3}{6.0\ mA} = 2.4k$$

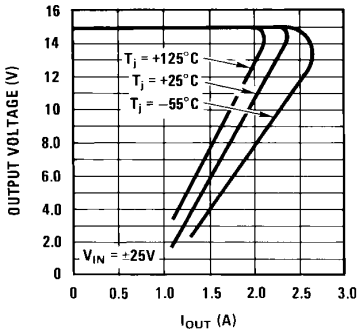

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FIGURE 17. Negative Regulator Foldback Current Limiting Characteristics

Figure 16 and *17* show the measured foldback characteristics for the values derived in the design examples. The value of R5 is set low so that the magnitude of I_5 for foldback is greater than I_4 through I_6. This reduces the foldback point sensitivity to the TC of the internal 300Ω resistor and any mismatch in the TC of Q2, Q3 or the pass device.

R6 can be computed from equation (18):

$$R6 = \frac{V_{SENSE}^-}{I_7} = \frac{V_{SENSE}^-}{I_5 + I_6 - I_3}$$

combining (13) and (20).

$$R6 = \frac{V_{SENSE}^-}{I_6 - I_4} = \frac{V_{SENSE}^-}{I_{FB}\, R_{CL}^- \left(\frac{1}{300} - \frac{1}{R4}\right) + \frac{V_{BE}}{R4}} \quad (22)$$

Setting $V_{BE} \cong V_{SENSE}$ and R4 = 300 to match the internal 300Ω (22) becomes:

$$R6 = R4$$

Also setting $\frac{I_4}{I_5} = \frac{2}{3} \rightarrow R5 = 200$

A 10 AMP REGULATOR

Figure 18 illustrates the complete schematic of a 10A regulator with foldback current limiting. The design approach is similar to that of the 2A regulator. However, in this design, the current contribution from the internal 300Ω resistor is greater due to the 2 V_{BE} drop across the Darlington pair. Expression (7) becomes:

$$\frac{I_{FB}\, R_{CL}^+ + V_{BE}}{300} << I_1\ ; \quad (23)$$

and, for the negative regulator, expression (22) becomes:

$$R6 = \frac{V_{SENSE}^-}{I_{FB}\, R_{CL}^- \left[\frac{1}{300} - \frac{1}{R4}\right] + V_{BE}\left[\frac{1}{300} + \frac{1}{R4}\right]} \quad (24)$$

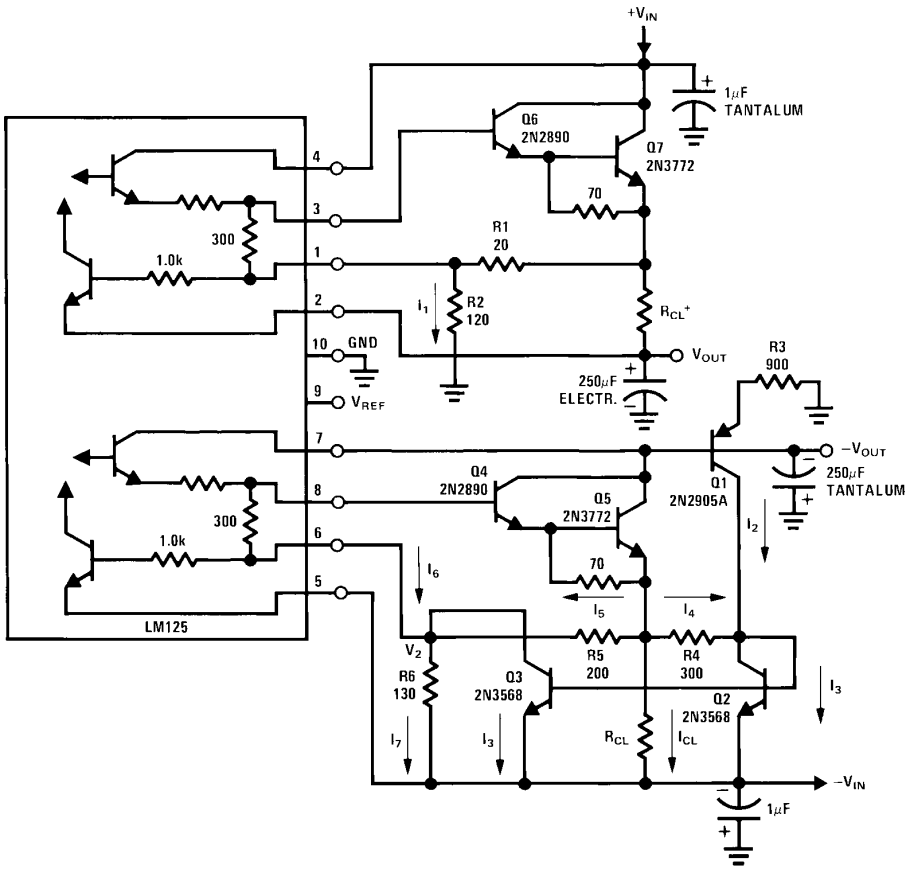

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FIGURE 18. 10A Regulator with Foldback Current Limiting

The disagreement between the theoretical and experimental values for the negative regulator is not alarming. In fact R_{CL} was based on equation (8), which is correct if for zero V_{OUT}, I_5 is zero as well. This implies:

$$V_{SENSE}\ (\text{at SC}) = \frac{V_{BEQ4} + V_{BEQ5}}{2}\ (\text{at SC})$$

which is a first order approximation.

Figure 19 illustrates the power dissipation in the external power transistor for both sides. Maximum power dissipation occurs between full load and short circuit so the heat sink for the 2N3772 must be designed accordingly, remembering that the 2N3772 must be derated according to 0.86W/°C above 25°C. This corresponds to a thermal resistance junction to case of 1.17°C/W.

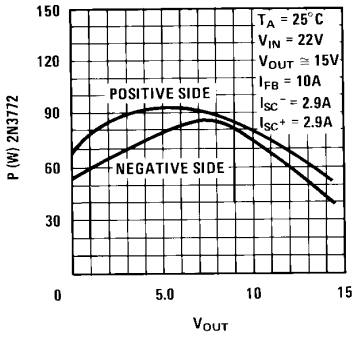

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FIGURE 19. Power Dissipation in the External Pass Transistor (Q5, Q7)

Example

Positive Side	Theoretical Value	Experimental Results
$I_{FB} = 10A$	$I_{125} = 13$ mA	$I_{FB} = 9.8A$
$I_{SC} = 2.5A$	$P_{LM125} = 150$ mW	$I_{SC} = 2.9A$
$V_{IN} = 22V$	$R_{CL}{}^{+} = 0.26\Omega$	$R_{CL}{}^{+} = 0.26\Omega$
$V_{OUT} = 15V$	$R1 = 21\Omega$	R1: adjusted to 20Ω
$\beta = \beta 1\, \beta 2 = 15 \times 50 = 750$ min	$R2 = 130\Omega$	R2: adjusted to 120Ω
$T_A = 25°C$	$V_{SENSE}{}^{+} = 650$ mV	

Negative Side	Theoretical Value	Experimental Results
$I_{FB} = 10A$	$R_{CL}{}^{-} = 0.22\Omega$	$I_{FB} = 10A$
$I_{SC} = 2.5A$	$R4 = 300\Omega$	$I_{SC} = 2.9A$
$V_{IN} = 22V$	$R5 = 200\Omega$	R_{CL}: adjusted to 0.3Ω
$V_{OUT} = 15V$	$R6 = 150\Omega$	R6: adjusted to 130Ω
$\beta = 800$	$R3 = 1.6\ k\Omega$	R3: adjusted 900Ω
$T_A = 25°$	$V_{SENSE}{}^{-} = 550$ mV	
$\frac{I_4}{I_5} = \frac{2}{3}$		

Note: For this example, in designing each side, the power dissipation of the opposite side has not been taken into the account.

POSITIVE CURRENT DEPENDENT SIMULTANEOUS CURRENT LIMITING

The LM125 uses the negative output as a reference for the positive regulator. As a consequence, whenever the negative output current limits, the positive output follows tracks to within 200−800 mV of ground. If, however, the positive regulator should current limit the negative output will remain in full regulation. This imbalance in output voltages could be a problem in some supply applications.

As a solution to this problem, a simultaneous limiting scheme, dependent on the positive regulator output current, is presented in *Figure 20*. The output current causes an I-R drop across R1 which brings transistor Q1 into conduction. As the positive load current increases I_1 increases until the voltage drop across R2 equals the negative current limit sense voltage. The negative regulator will then current limit, and positive side will closely follow the negative output down to a level of 700−800 mV. For $V_{OUT}{}^{+}$ to drop the final 700−800 mV with small output current change, $R_{CL}{}^{+}$ should be adjusted so that the positive current limit is slightly larger than the simultaneous limiting. *Figure 21* illustrates the simultaneous current limiting of both sides.

The following design equations may be used:

$$R1\, I_{CL}{}^{+} = R3\, I_1 + V_{BEQ1} \tag{25}$$

$$I_1 = \frac{V_{SENSE}{}^{-}}{R2} \tag{26}$$

Combining (25) and (26),

$$I_{CL}{}^{+} = \frac{\frac{R3}{R2} V_{SENSE}{}^{-} + V_{BEQ1}}{R1} \tag{27}$$

with

$$R_{CL}{}^{+} = \frac{V_{SENSE}{}^{+}}{1.1\, I_{CL}{}^{+}} \tag{28}$$

The negative current limit (independent of $I_{CL}{}^{+}$) can be set at any desired level.

$$I_{CL}{}^{-} = \frac{V_{SENSE}{}^{-} + V_{DIODE}}{R_{CL}{}^{-}} \tag{29}$$

Transistor Q2 turns off the negative pass transistor during simultaneous current limiting.

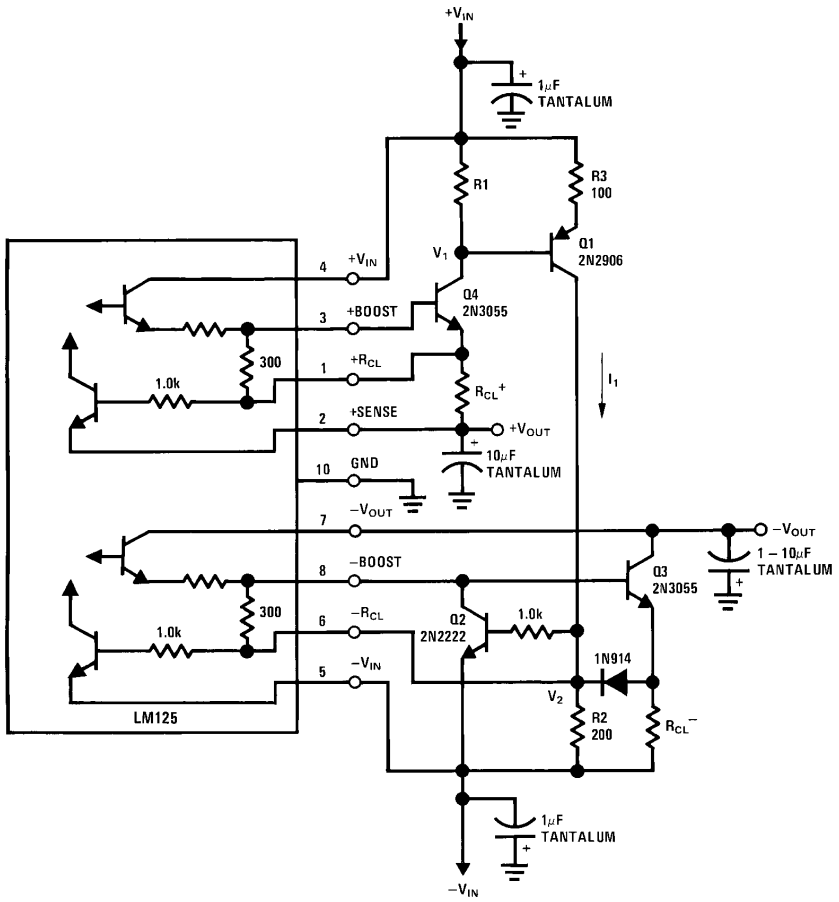

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FIGURE 20. Positive Current Dependent Simultaneous Current Limiting

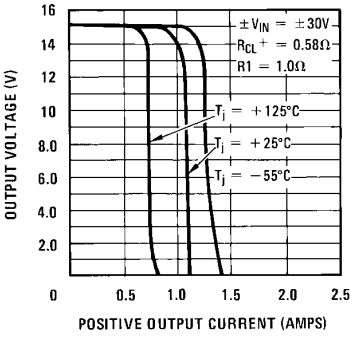

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FIGURE 21. Positive Current Dependent Simultaneous Shutdown

ELECTRONIC SHUTDOWN

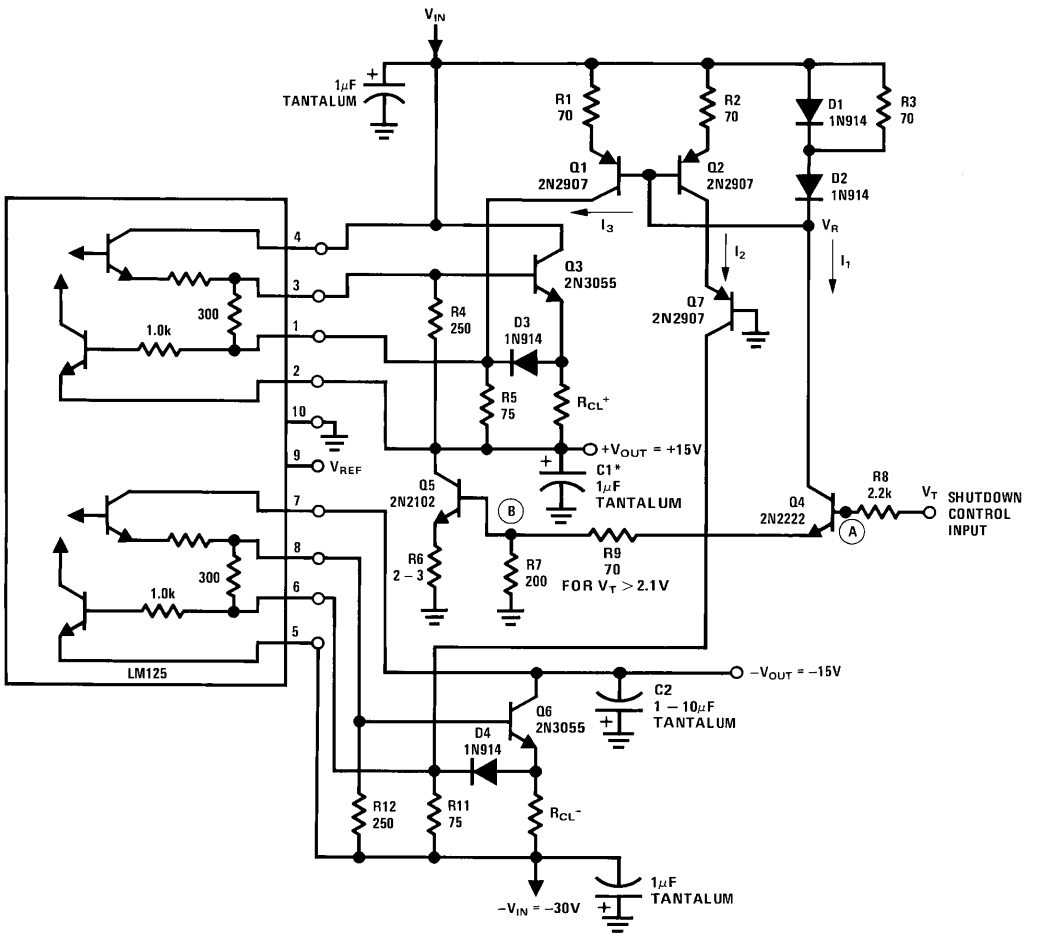
In some regulated supply applications it is desirable to shutdown the regulated outputs ($\pm V_O = 0$) without having to shutdown the unregulated inputs (which may be powering additional equipment). Various shutdown methods may be used. The simplest is to insert a relay, a saturated bipolar device, or some other type switch in series with either the regulator inputs or outputs. The switch must be able to open and close under maximum load current which, may be several amps.

As an alternate solution, the internal reference voltage of the regulator may be shorted to ground. This will force the positive and negative outputs to approximately +700 mV and +300 mV respectively. Both outputs are fully active so the full output current can still be supplied into a low impedance load. If this is unacceptable, another solution must be found.

The circuit in *Figure 22* provides complete electronic shutdown of both regulators. The shutdown control signal is TTL compatible but by adjusting R8 and R9 the regulator may be shutdown at any desired level above 2 V_{BE}, calculated as follows:

$$V_T \cong \left[\frac{R8}{R3\ \beta\ Q4} + \frac{R9}{R3}\right] V_{BE} + 2\ V_{BE} \qquad (30)$$

Positive and negative shutdown operations are similar. When a shutdown signal V_T is applied, Q4 draws current through R3 and D2 establishing a voltage V_R which starts



*For higher values of C1 increase R6 to limit the peak current through Q5 to a safe value.

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FIGURE 22. Electronic Shutdown for the Boosted Regulator

the current sources Q1 and Q2. Assuming that Q1 and Q2 are matched, and making R1 = R2 = R3, the currents I_1, I_2, I_3 are equal and both sides of the regulator shutdown simultaneously.

The current I_3 creates a drop across R5, which equals or exceeds the limit sense voltage of the positive regulator, causing it to shutdown. Since I_3 has no path to ground except through the load, a fixed load is provided by Q5, which is turned on by the variable current source Q4, C1 also discharges through Q5 and current limiting resistor R6. Resistor R4 prevents Q3 turn on during shutdown, which could otherwise occur due to the drop across R5 plus the internal 300Ω resistor. Diode D3 prevents I_3 from being shunted through R_{CL}.

C2 discharges through the load. Q7 shares the total supply voltage with Q2, thus limiting power dissipation of Q2. Another power dissipation problem may occur when the design is done for V_T = 2.0V for example, and V_T is increased above the preset threshold value. I_1 is increased and Q4 has to dissipate $(V_{IN} - 3\ V_{BE} - V_T)\ I_1$ (W). The simplest solution is to increase R8. If this is insufficient, a set of diodes may be added between nodes A and B to clamp, I_1 to a reasonable value. This is illustrated in *Figure 23*:

$$I_1 = \frac{V_{R9}}{R9} \cong \frac{V_T - V_{BE} - [V_T - 2\ V_{BE}]}{R9} = \frac{V_{BE}}{R9}$$

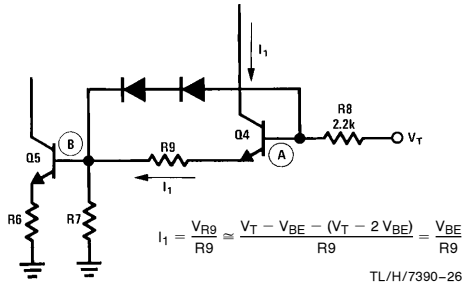

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FIGURE 23

So I_1 is made independent of V_T and by setting a minimum value of 10 mA (R9 = 70Ω). The regulator will shutdown at any desired level above 3 V_{BE}, without overheating transistor Q4. Also using *Figure 23* the diode D1 in *Figure 22* may be omitted. The shutdown characteristics of *Figure 22* are shown in *Figure 24*.

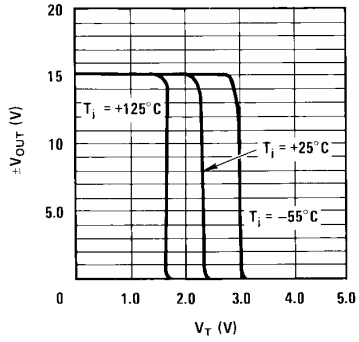

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FIGURE 24. Electronic Shutdown Characteristics

The normal current limiting current is set by equation (31)

$$I_{CL} = \frac{V_{SENSE} + V_{DIODE}}{R_{CL}} \quad (31)$$

The same approach is used with the unboosted regulator shown in *Figure 25*. In this case the voltage sense resistor is the internal 300Ω one. Since output capacitors are no longer required Q3 is just used as a current sink and its emitter load has been removed.

POWER DISSIPATION

The power dissipation of the LM125 is:

$$P_d = (V_{IN}^+ - V_{OUT}^+)\ I_{OUT}^+ + (V_{IN}^- - V_{OUT}^-)\ I_{OUT}^- + V_{IN}^+\ I_S^+ + V_{IN}^-\ I_S^-$$

where I_S is the standby current.

Ex: ±1A regulator using 2N3055 pass transistors. Assuming a β = 100, and ±25V supply,

$$P_d = 400\ \text{mW}.$$

The temperature rise for the TO-5 package will be:

$$T_{RISE} = 0.4 \times 150°C/W = 60°C$$

Therefore the maximum ambient temperature is $T_{AMAX} = T_{jMAX} - T_{RISE} = 90°C$. If the device is to operate at T_A above 90°C then the TO-5 package must have a heat sink. T_{RISE} in this case will be:

$$T_{RISE} = P_d\ (\theta_{J\text{-}C} + \theta_{C\text{-}S} + \theta_{S\text{-}A}).$$

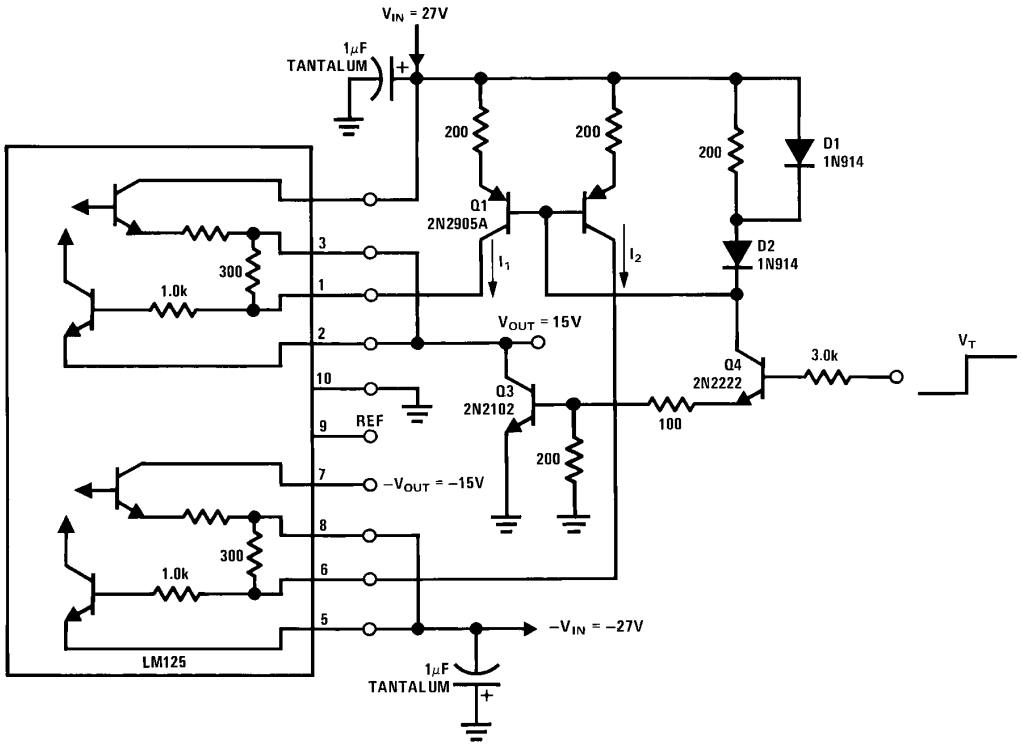

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FIGURE 25. Electronic Shutdown for the Basic Regulator

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