9XC1XX
Philips 16/32-bit microcontroller series

AN431

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INTRODUCTION

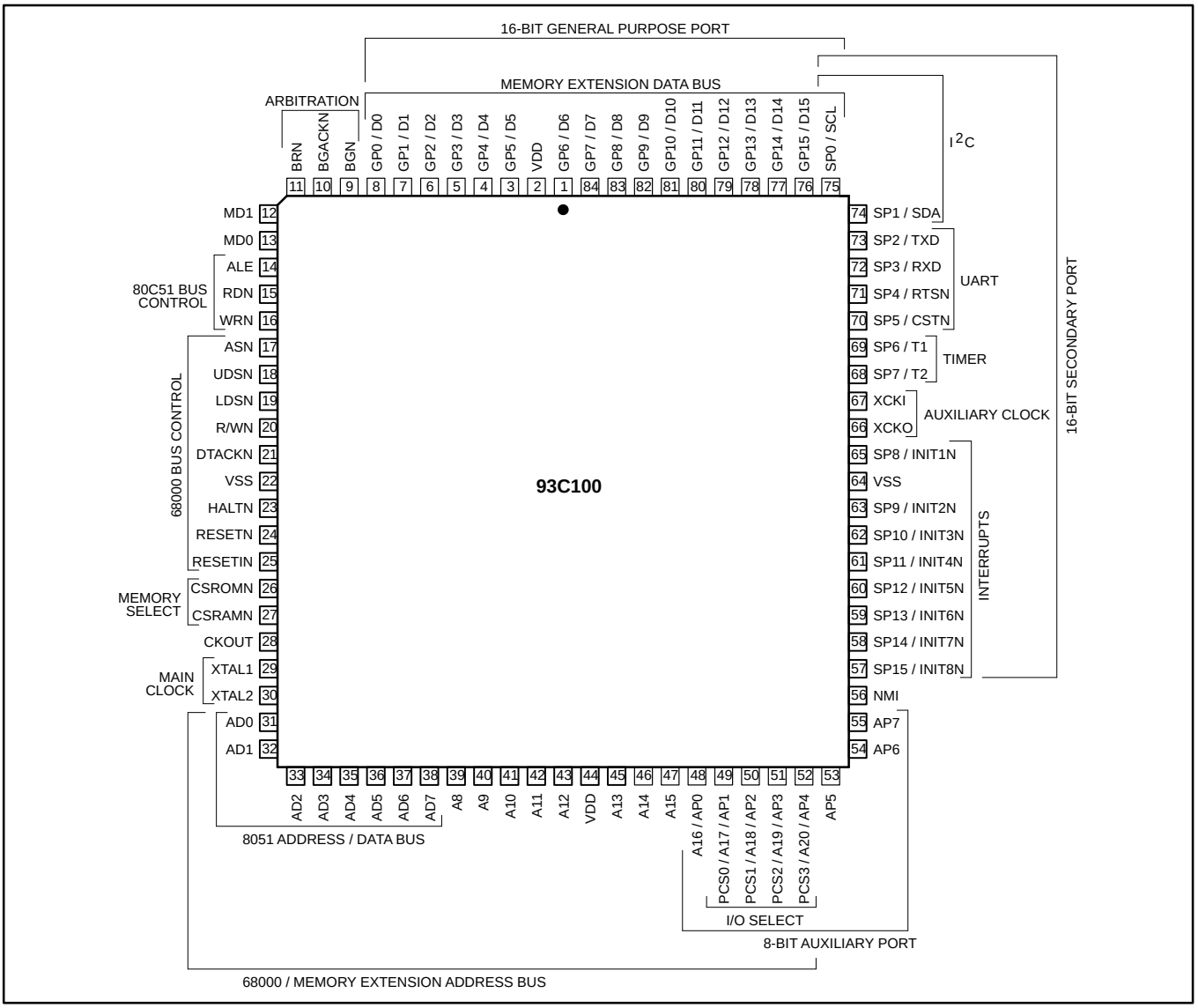
Philips 9XC1XX 16/32 bit microcontroller family introduces an innovative solution to 16-bit design by extending the 68000 design environment to 80C51 peripheral users. Based upon Philips 68070 microprocessor, the 9XC1XX line supports the full 68000 instruction set while providing up to 34K ROM, 512 bytes RAM, 256 Bytes EEPROM, UART, I^2C bus port, two counter/timers plus 40 quasi-bi, and bidirectional I/O lines. The EPROM version will house 32K Bytes of memory programmable by standard 80C51 programmer with a 90C adaptor.

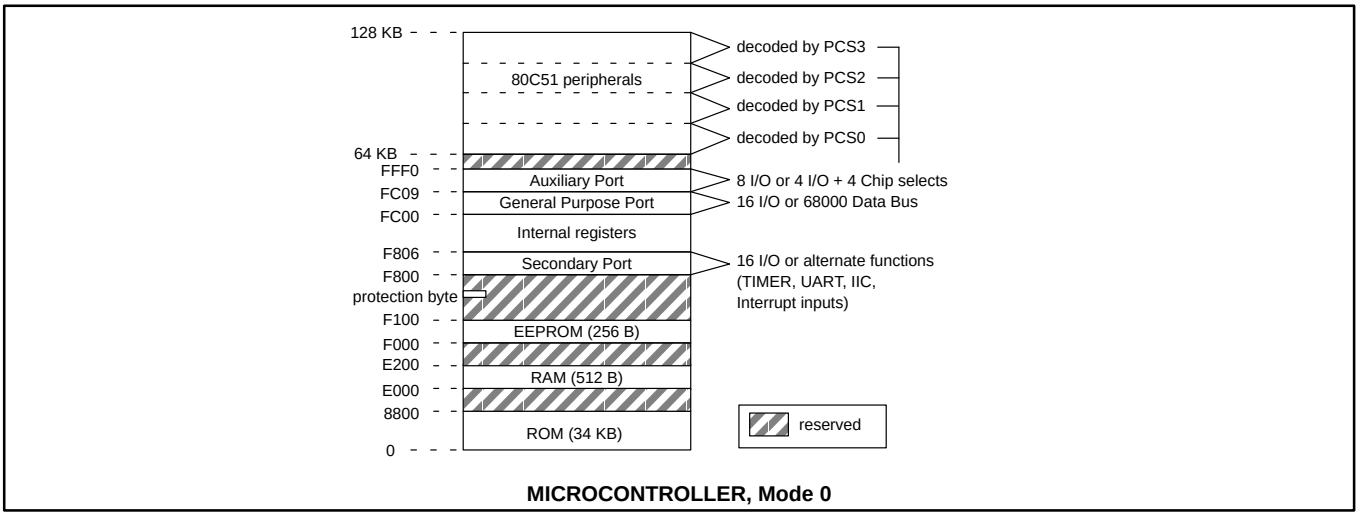
In addition to the on-chip peripherals the architecture has been updated to include decoded, latched external interrupts, an auto-DTACKN generator and control registers for user definition of system operation. Power consumption varies from 80mA during normal operation down to 10mA for Idle Mode and 8mA for Stand-by mode. All family members are available in 84-pin PLCC or 80-pin QFP in commercial and industrial temperature ranges.

NOTE: For the remainder of this article, 90C refers to all family members unless otherwise stated.

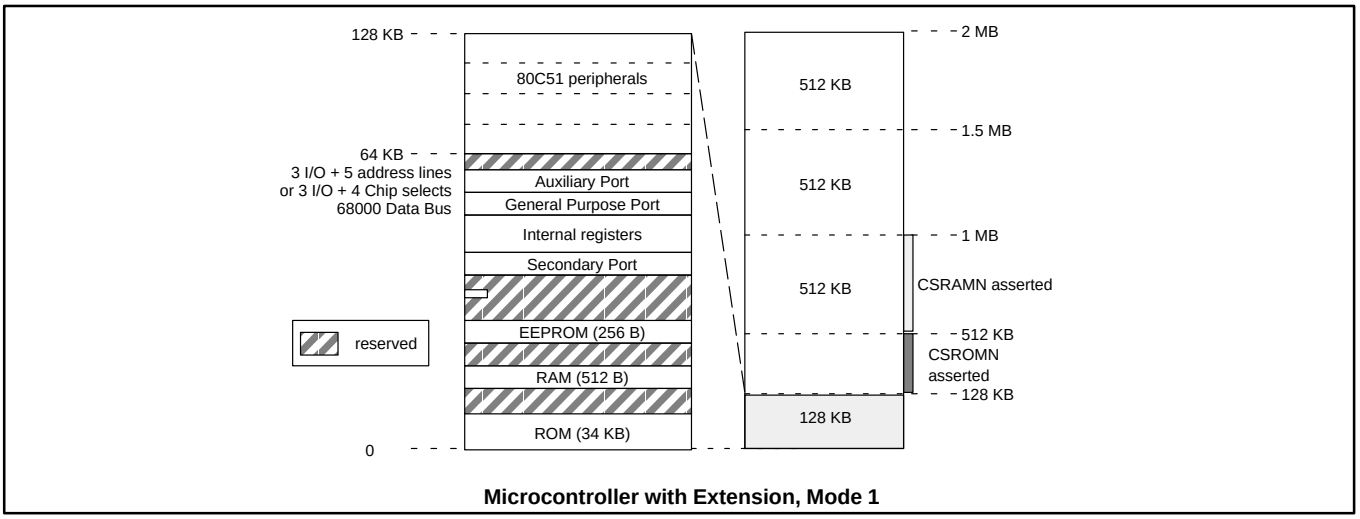
PINOUT

During RESET or power-up the 90C is configured to operate in one of four modes defined in hardware by the logic state of two input pins. The four modes differ primarily in external address range and I/O ports availability. Mode selection will depend upon the application's memory requirements vs. the need for I/O control. Once the operating mode has been established, port functions and peripherals are controlled by software access to on-chip memory locations.





MICROCONTROLLER, Mode 0



Microcontroller with Extension, Mode 1

MODE 0

Microcontroller mode is used for embedded applications requiring only minimal memory (34K) space but extensive I/O and peripheral interface. The three ports, the General Purpose Port, Secondary Port and Auxiliary Port are available for I/O, peripheral functions and 80C51 bus chip selects. Each pin is individually definable as I/O or alternate function.

This provides a total of 40 I/O lines or 24 I/O lines, all on-chip peripherals plus 8 external interrupts or 20 I/O lines, an 80C51 interface, all of the peripherals and 4 interrupts. The designer not only has multiple combinations of features available but features which are defined by software allowing the system to be re-configured by service routines as the operating environment changes.

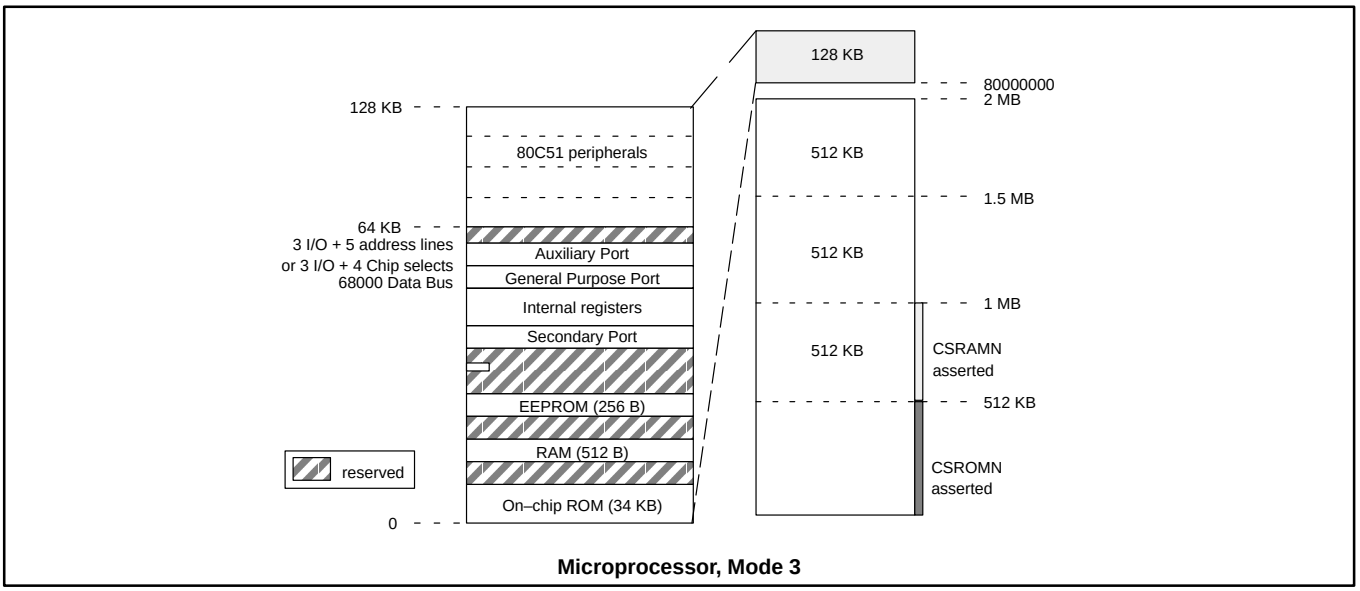
Mode 0 memory map divides the 128K memory into two 64K blocks reserving the lower 64K for on-chip functions. Access to the first 34K block are directed to the on-chip ROM. The next 30K maps peripheral operation, system control registers, RAM and EEPROM. The second 64K block defines the address range for the 80C51 bus. Access to locations $10000 to $1FFFF follow the synchronous 80C51 protocol supported by ALE, WRN and RDN signals. This block can be divided into four 16K blocks controlled by Auxiliary Port lines AP[1:4] enabled as chip selects PSEN [0:3]. The 64K 80C51 address block is the only available external address space. All other cycles are directed to on-chip locations.

MODE 1

MODE 1 offers a flexible option for designs which require only 34K of space now but may need up to 2 Meg for future upgrades.

External access, beyond the first 128K address block, uses the eight, 80C51 A/D lines combined with either AP[1:4] to give 2 Mega bytes external range or AP[1] for a 128K extension. The remaining AP lines act as quasi-bidirectional pins or can be enabled to provide the 80C51 bank chip selects. Data for external transfers outside the first 128K is handled over the 16-bit general purpose port which provides a dedicated data bus. The secondary port is still fully operational to support any combination of I/O, interrupt input and peripheral functions.

Mode 1 provides the easiest upgrade path when moving from 8-bit 80C51 family designs to 16-bit applications. By taking advantage of the 80C51 bus, memory can be expanded up to 2 Mega bytes without significant changes to the peripheral structure. Firmware engineers can design using 68000 C-compilers in place of INTEL assemblers.



Microprocessor, Mode 3

MODE 2

Referred to as Emulation Mode, Mode 2 operation is identical to Mode1 with one major exception. Access to the first 34K of on-chip ROM is now decoded off-chip. This provides for memory emulation for code development, prior to final mask definition, without using an EPROM version. This Mode is particularly important to designers using the 93C110 part, which does not have an EPROM twin. However, duplication of the on-chip timing does require either DTACKN to be generated externally or 266ns EPROMs used to mimic the 4 clock cycle internal transfer time. The remainder of the memory map is unaffected and models MODE 1.

MODE 3

This last mode creates a memory map that is almost an inversion of the Mode1 map. All on-chip memory locations reside in the upper 4G bytes of the 32-bit internal address bus. On-chip ROM, RAM, registers, etc., begin at $80000000 with the lower 2 Meg of memory filled by off-chip locations $0000 to $3FFFFF. In this mode the 90C behaves as a microprocessor drawing instructions from board memory. With the exception of new address locations, on-chip operation is as with Mode 1.

Now that you understand how the 90C operates, the remainder of the article will concentrate on unique features and how the part compares to the 68000 and the 68070.

THE CPU

The Central Processing Unit for the 90C family maintains the 68000 architecture programming model, instruction set and addressing modes. Any 68000 compiler or assembler can be used for code translation as long as the programmer considers the differences in information stored during exception processing. When the 68000 enters exception processing, the CPU stacks three words; program counter high, program counter low and the status word. The 90C stores one additional word, containing format bits and the vector number, when responding to normal exceptions. 13 additional words are stored for address exceptions to allow the CPU to recover and re-run the lost cycle.

Interrupts

The 90C has 29 potential interrupt sources individually programmable to seven priority levels:

GP[0:15]	A change in status of an input at the GP port.
INT[1:8]N	External Latched Interrupts
UART	Receiver and Transmitter
I^2C	Status
T1, T2	Status
NMIN	External Non-maskable interrupt, level 7.

The problem of simultaneous requests becomes a more critical concern as the number of interrupt sources increases. This situation is resolved in two ways. First, to prevent stack overflow, a bit set to the System Control Register will delay service to subsequent higher level requests once an interrupt routine has started. Pending interrupts are recognized and serviced according to priority when the bit is cleared at prior to RTE of the current interrupt. This feature allows greater software control over interrupt prioritization while significantly reducing the amount of dedicated stack space required to implement a multiple interrupt source design.

The second improvement adds an internal prioritization scheme to handle simultaneous interrupts from multiple sources programmed to the same priority level. The scheme is similar to the 68070 prioritization list but includes the NMIN and external latched requests giving them highest priority. For example, simultaneous interrupts from INT2N and the UART receiver, both programmed to level three are acknowledged by completing the INT2N requests first followed by the UART receiver request.

DTACKN Generator

Designers using external memory or peripherals mapped outside of the 80C51 address range (i.e., Modes 1–3) are ultimately faced with the need for a DTACKN generator, preferably one which optimizes rather than degrades system performance. This hardware overhead is eliminated by taking advantage of the ADD and FBC bits in the System Control Register to optimize READ cycles and enable auto-DTACKN control. When the Fast Bus Cycle bit (FBC) is set and DTACKN is pulled low, the minimum number of external READ bus cycles is reduced from four to three. With FBC asserted, software transferring block data from external memory executes about 10% faster than normal.

If DTACKN cannot be pulled low, normally the 90C will insert wait states to delay the cycle

4/4until the acknowledge is received. However, an internal acknowledge is automatically generated after 7 clock periods when the ADD bit (Auto DTACKN Disable) is cleared. The maximum access time required is 250ns at 17.5MHz CPU.

Power Down Modes

Two bits in the System Control Register control the main and auxiliary oscillators to enable normal, idle or stand-by operating mode. As expected, during normal operation all chip functions are supported and the main oscillator is running at full speed. In IDLE mode, power consumption is reduced by driving the chip from the auxiliary clock at 300KHz while the main oscillator remains running. This maintains minimal functionality while reducing power requirements to 50mW. Normal mode can be re-entered by external or internal interrupt. STAND-BY mode also drives the system from the auxiliary clock but the main oscillator is turn off to reduce power consumption to 40mW. The same functionality as IDLE mode is maintained, however, to return to normal operation the main oscillator must be restarted and stabilized for at least 10ms. During IDLE and STAND-BY modes some on-chip functionality is maintained (i.e., RAM integrity, timer and UART operation) and a minimal instruction set supported.

INTER-INTEGRATED CIRCUIT (I^2C) BUS

The I^2C port on the 90C family is a two-wire serial bus designed to support information transfers between multiple elements within a system rack or desk top range. The port operates as a master or slave transmitter or receiver and supports multimaster operation.

When operating as a master the SCL bus clock drives or receives byte data at transfer rates up to 189KHz (I^2C specification compatibility = 100KHz max). The port is controlled by access to memory mapped registers and operates in either polled or interrupt driven designs.

UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER

The UART interface follows the standard 2681/2692 programming models and operating modes. 8- or 7-bit characters are transferred at up to 19.2K baud using either a two- or four-wire handshake. Independent receiver and transmitter clocks are selected either from an onboard baud rate generator or an external source via the auxiliary clock. UART is initiated and controlled through a dedicated memory mapped register set.

16-BIT COUNTER TIMERS

An on-chip 16-bit continuous timer increments once every 192 CPU clocks to provide a reference for two 16-bit programmable timers operating in match, count, or event mode. Match mode generates a pulse output on the corresponding timer special function pin (T1 or T2). The pulse duty cycle equals Tx/($FFFF-RR) with duration $FFFF-RR where RR is a value programmed into the reload register and Tx is the T1 (T2) reference register. At rollover and match conditions an interrupt is issued and a status bit is set. In event counter mode, when a programmed number of events occurs at the T1 (T2) input, an interrupt is issued. An event is definable as +edge, –edge, ±edge or a level change. In capture mode, each time an event occurs, the content of the continuous timer is stored in the T1 (T2) register, an interrupt is issued and a status bit is set. Event mode is used to count the number of events occurring during a fixed time span while capture mode determines the time span between two events.

DEVELOPMENT TOOLS

When introducing a new microcontroller the second question customers always ask (after “What’s new about it?”) is “What development tools exist?”. The 90C family is supported by three levels of evaluation hardware and high level software all of which are currently available either from a third party or via distribution.

The simplest and least expensive hardware support is the Microcore III evaluation/demo board from Philips. This is a spin-off from the 68070 Microcore I and offers the same features minus the VSC and video interface. The board consists of 4×6” card with sockets for 512K EPROM and RAM, an RS232 port, I^2C port and 93C100. There is also a prototype area and 96 pin connector. No memory is included but the on-chip ROM holds a 32K monitor which supports line assembly, uploads and downloads from a host, breakpoints, single step operation and a few other general purpose functions. The board operates by RS-232 serial connection to a PC running in terminal mode. The MCIII costs less than $600 and is great for initial software development and debugging assembly level driver routines.

The second level of support is the 90CDS, a full emulation system designed by Philips and sourced and supported by third party for the U.S. market. The system consists of a stand-alone box with I.C.E. extension driven by serial connection to a PC. Although a low-level monitor is supplied with the system, most detailed hardware analysis will require the 90C-XRAY development software package from BSO/TASKING, Boston. The package includes a C-compiler, Assembler/Linker/Librarian and Microtec XRAY debugger. XRAY supports C code and Assembly level symbolic debug, real time operation, hardware and software breakpoints and 2K of Trace memory. The user interface is a windowed environment with on-screen help. The 90CDS retails for under $6000 and the Tasking package sells for less than $4000.

The most sophisticated development system, the Lauterbauch TRACE 32, is available from SIGNUM systems in Thousand Oaks, CA. While this is the most expensive solution, it is also the most powerful. Like the HP 64700, the TRACE 32 is actually a host system which supports numerous 8-, 16- and 32-bit controllers through plug-in modules. The unit recognizes multiple high level languages and includes a built in logic analyzer. In addition to the 90C family, the TRACE 32 also supports most of Philips 80C51family and the 68070. For designs using more than one controller or a mixture of controller/processor architectures, this system provides a common data base and may be the most economical solution.

During the last 6 months the 16-bit processor/ controller market has experienced a host of new product introductions from some healthy competition. However, in a side-by-side comparison, the 90C100 family wins out easily by providing more on-chip memory, standard instructions and more useable features than any other product in its class. The best news is that even with all these advantages it’s still one of the lowest cost 16-bit products in the world.