Dual Complementary Pair Plus Inverter

The MC14007UB multi–purpose device consists of three N–channel and three P–channel enhancement mode devices packaged to provide access to each device. These versatile parts are useful in inverter circuits, pulse–shapers, linear amplifiers, high input impedance amplifiers, threshold detectors, transmission gating, and functional gating.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin–for–Pin Replacement for CD4007A or CD4007UB
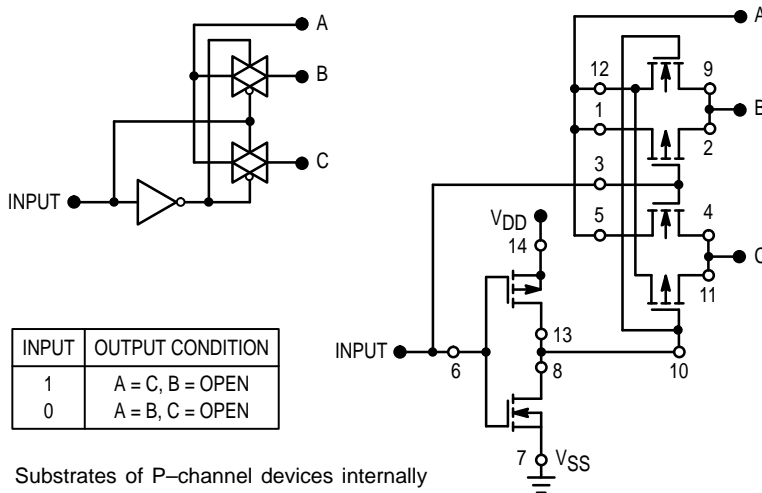- This device has 2 outputs without ESD Protection. Anti–static precautions must be taken.

MC14007UB

L SUFFIX
CERAMIC
CASE 632

P SUFFIX
PLASTIC
CASE 646

D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXUBCP	Plastic
MC14XXXUBCL	Ceramic
MC14XXXUBD	SOIC

T_A = – 55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
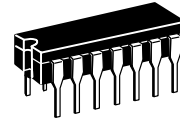†Temperature Derating:
　　Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
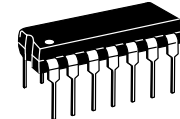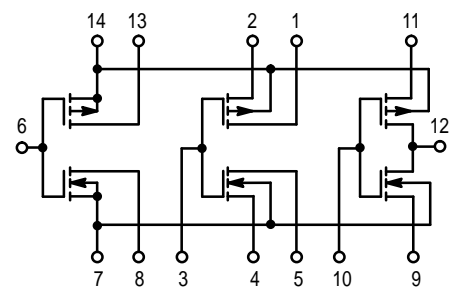　　Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

PIN ASSIGNMENT

D = DRAIN
S = SOURCE

SCHEMATIC

V_{DD} = PIN 14
V_{SS} = PIN 7

INPUT	OUTPUT CONDITION
1	A = C, B = OPEN
0	A = B, C = OPEN

Substrates of P–channel devices internally connected to V_{DD}; substrates of N–channel devices internally connected to V_{SS}.

Figure 1. Typical Application: 2–Input Analog Multiplexer

MOTOROLA

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	− 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage "0" Level V_{in} = V_{DD} or 0		V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD} "1" Level		V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 Vdc) (V_O = 9.0 Vdc) (V_O = 13.5 Vdc)		V_{IL}	5.0 10 15	— — —	1.0 2.0 2.5	— — —	2.25 4.50 6.75	1.0 2.0 2.5	— — —	1.0 2.0 2.5	Vdc
(V_O = 0.5 Vdc) "1" Level (V_O = 1.0 Vdc) (V_O = 1.5 Vdc)		V_{IH}	5.0 10 15	4.0 8.0 12.5	— — —	4.0 8.0 12.5	2.75 5.50 8.25	— — —	4.0 8.0 12.5	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)		I_{OH}	5.0 5.0 10 15	− 3.0 − 0.64 − 1.6 − 4.2	— — — —	− 2.4 − 0.51 − 1.3 − 3.4	− 5.0 − 1.0 − 2.5 − 10	— — — —	− 1.7 − 0.36 − 0.9 − 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)		I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	1.0 2.5 10	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)		I_{DD}	5.0 10 15	— — —	0.25 0.5 1.0	— — —	0.0005 0.0010 0.0015	0.25 0.5 1.0	— — —	7.5 15 30	µAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)		I_T	5.0 10 15	I_T = (0.7 µA/kHz) f + I_{DD}/6 I_T = (1.4 µA/kHz) f + I_{DD}/6 I_T = (2.2 µA/kHz) f + I_{DD}/6							µAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L − 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.003.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (1.2 ns/pF) C_L + 30 ns		5.0	—	90	180	
t_{TLH} = (0.5 ns/pF) C_L + 20 ns		10	—	45	90	
t_{TLH} = (0.4 ns/pF) C_L + 15 ns		15	—	35	70	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.2 ns/pF) C_L + 15 ns		5.0	—	75	150	
t_{THL} = (0.5 ns/pF) C_L + 15 ns		10	—	40	80	
t_{THL} = (0.4 ns/pF) C_L + 10 ns		15	—	30	60	
Turn–Off Delay Time	t_{PLH}					ns
t_{PLH} = (1.5 ns/pF) C_L + 35 ns		5.0	—	60	125	
t_{PLH} = (0.2 ns/pF) C_L + 20 ns		10	—	30	75	
t_{PLH} = (0.15 ns/pF) C_L + 17.5 ns		15	—	25	55	
Turn–On Delay Time	t_{PHL}					ns
t_{PHL} = (1.0 ns/pF) C_L + 10 ns		5.0	—	60	125	
t_{PHL} = (0.3 ns/pF) C_L + 15 ns		10	—	30	75	
t_{PHL} = (0.2 ns/pF) C_L + 15 ns		15	—	25	55	

* The formulas given are for the typical characteristics only. Switching specifications are for device connected as an inverter.
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
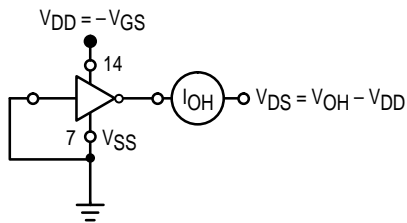
All unused inputs connected to ground.
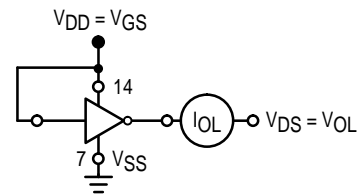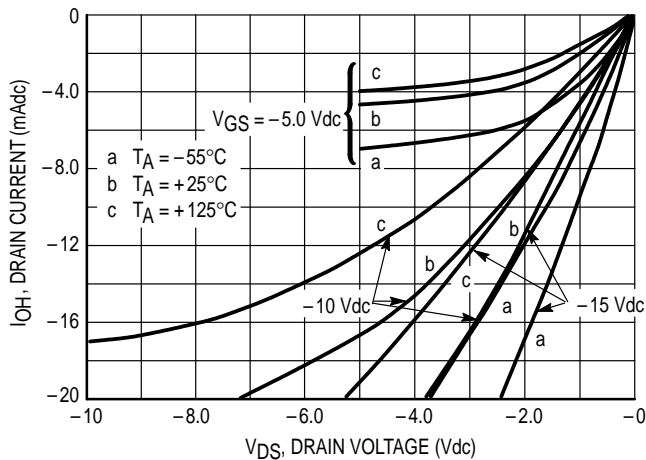

All unused inputs connected to ground.

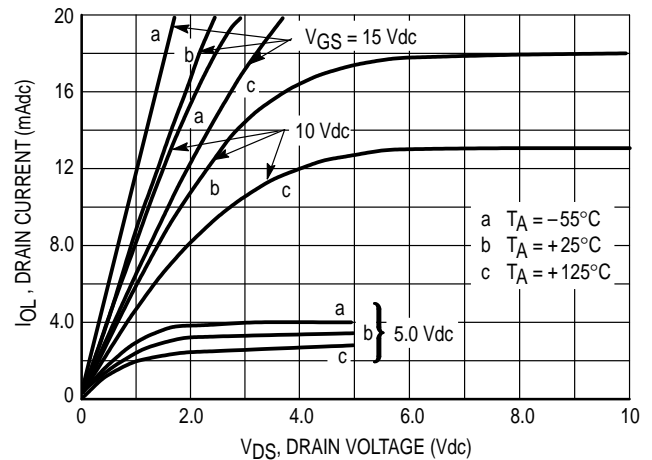**Figure 2. Typical Output Source Characteristics**

Figure 3. Typical Output Sink Characteristics

These typical curves are not guarantees, but are design aids.
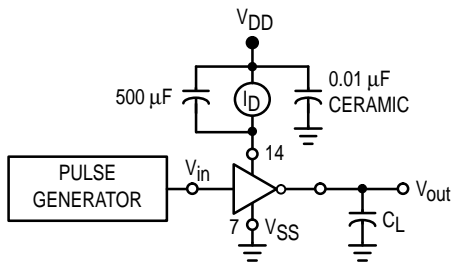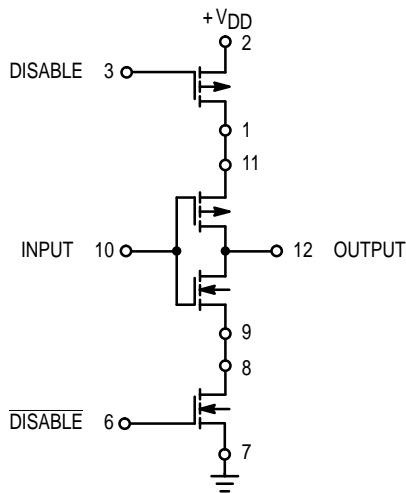Caution: The maximum current rating is 10 mA per pin.

Figure 4. Switching Time and Power Dissipation Test Circuit and Waveforms
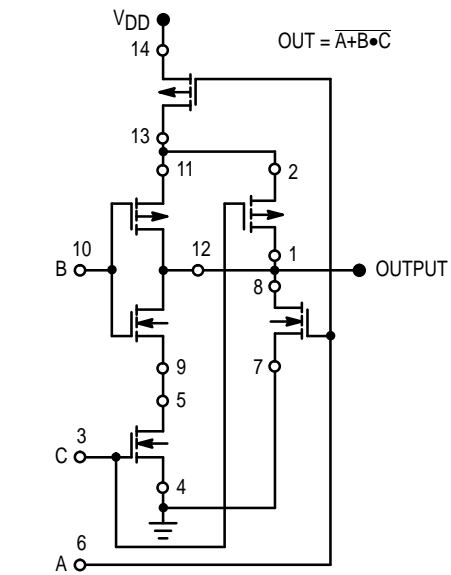
APPLICATIONS

The MC14007UB dual pair plus inverter, which has access to all its elements offers a number of unique circuit applications. Figures 1, 5, and 6 are a few examples of the device flexibility.

INPUT	DISABLE	OUTPUT
1	0	0
0	0	1
X	1	OPEN

X = Don't Care

Figure 5. 3–State Buffer

$OUT = \overline{A + B \bullet C}$

Substrates of P–channel devices internally connected to V_{DD};
Substrates of N–channel devices internally connected to V_{SS}.

Figure 6. AOI Functions Using Tree Logic

OUTLINE DIMENSIONS

L SUFFIX
CERAMIC DIP PACKAGE
CASE 632–08
ISSUE Y
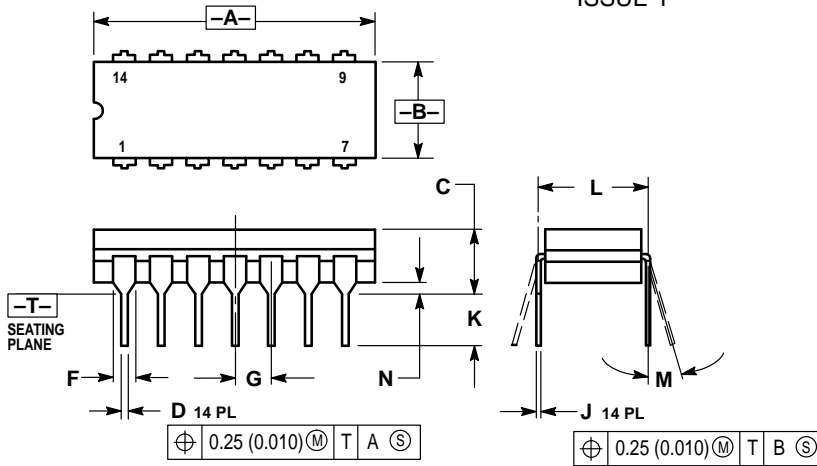
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L
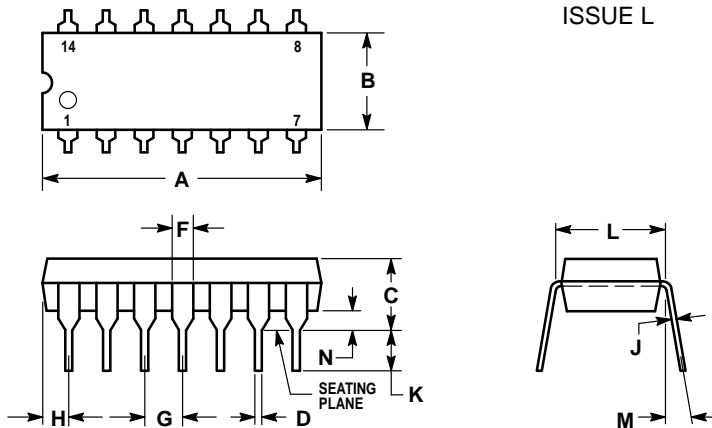
NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F
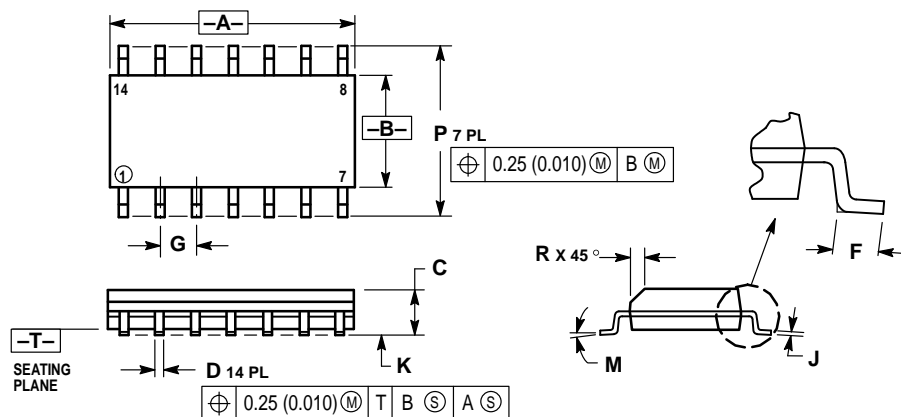
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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MC14007UB/D