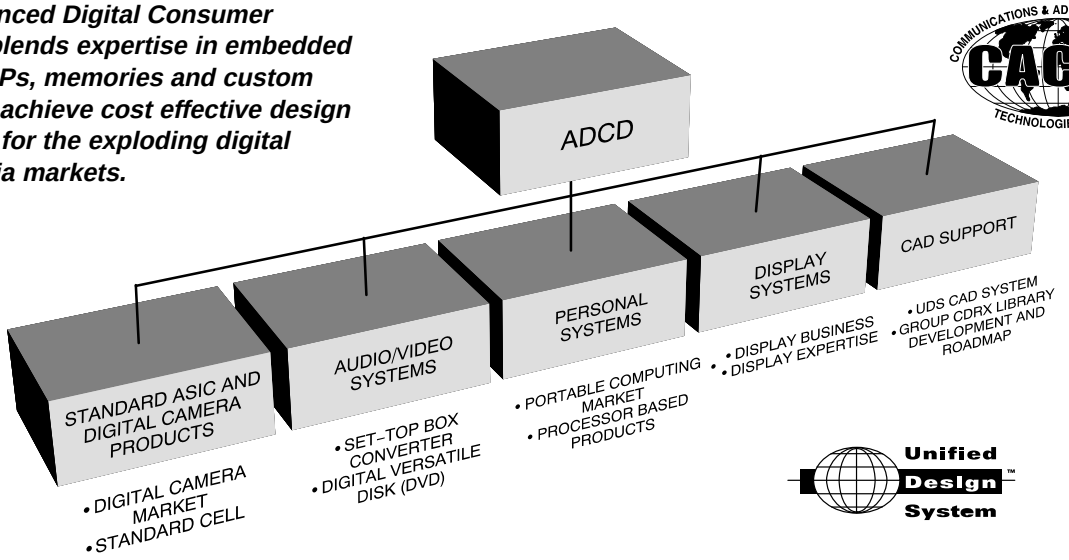
Advanced Digital Consumer Products

In Brief . . .

Motorola supports strategic programs and co–development partnerships to accelerate the availability of advanced digital consumer products.

Advanced Digital Consumer Division (ADCD) New Market Focus

The Advanced Digital Consumer Division blends expertise in embedded cores, DSPs, memories and custom silicon to achieve cost effective design solutions for the exploding digital multimedia markets.



Standard ASIC and Digital Camera Products

The ADC Division champions standard cell methodologies and libraries to provide a technology base for use across the Communications and Advanced Consumer Technologies Group (CACTG). The ADC Division is taking the lead role in the area of systems integration. Mixed (analog + digital) signal system integration is ideally suited to 'camera-on-a-chip' concepts for the digital camera market.

Audio/Video Systems

Focused to provide leadership products in multimedia markets, such as Set-Top Box (STB) converters, Advanced TV, and Digital Versatile Disk (DVD).

Set-Top Box Converters

One application of digital set-top boxes is in digital cable TV distribution networks. These systems expand the number of available channels while delivering high quality digital video and audio via cable to the home.

Cable operators are also offering high-speed data services for computer to computer communications. These modems make it possible for ordinary PCs to access the Internet at Ethernet speeds (10 Mbit/second) or higher.

Personal Systems

Personal Systems develops integrated microprocessors based on Motorola's 68K (M68328) and Embedded PowerPC™ (MPC821/MPC823) architectures for digital consumer products such as PDAs, Portable Clients, Smart Phones, Digital Cameras, and Web Appliances.

These highly integrated microprocessors include the peripherals most commonly required for these markets, such as LCD controller, serial interfaces, USB, IrDA, PCMCIA, etc. They provide solutions for systems requiring low cost, low power, and high performance using PowerPC™ and Embedded DSP to provide over 100 MIPS. By incorporating industry standard architectures these processors are backed by superior development tools and OS support. Some examples include Microware (OS–9), Microsoft (WindowsCE — 821/823 only), ISI (pSOS), WindRiver (VxWorks), Diab, SDS, Metrowerks, HP, Applied, and others. Personal Systems also provides reference designs for HandHeld PC, Digital Cameras and Web Appliances to shorten new product development time.

Display Systems

Products that provide best–in–class display system (flat panel and monitor) solutions for high growth, high volume communication and consumer electronic products. LCD Drivers for applications ranging from pager and cellular telephone displays to mid–range drivers for electronic translators, games, etc., to large LCD drivers for computer VGA displays.

CAD Support

Focused on developing next generation Cell-based libraries for delivery within the UDS design system.

Unified Design System (UDS 1.0 ASIC) – Now Available

The consumer marketplace is driven by low cost, high performance, and short development schedules. The UDS system rapidly takes a design from the system level to physical implementation, allowing designers more time to focus on system level design trade-offs and IC performance.

Now available to Sun, Solaris, and HP platform ASIC gate array customers. This CAD system is based upon the Open Architecture CAD System (OACS) and includes new graphical interfaces, silicon technology features, and enhancements to OACS tools.

Scorpion Chip (MC92100) Prototypes available – June '97

The MC92100 is a graphics display generator and digital video encoder for analog and digital video systems. The chip provides a highly integrated solution for Intelligent TV (iTV), Set-Top Box (STB), and Digital Versatile Disk (DVD) applications. The Scorpion chip support team offers customers the design talents of Motorola's Phoenix Technology Center combined with the silicon integration skills of the ADC Division.

Low Cost Plastic Ball Grid Array (LCPBGA) Packages – Now Available

The ADC Division is offering a new BGA family designed to match the cost of plastic QFP packages in the 100 - 200 lead range. The low cost BGA family presently includes packages with 100, 144, and 196 leads. The family employs a 1.0 mm solderball pitch which provides a very small, thin, and light package ideal for consumer products.

MPC821/MPC823 RISC Microprocessors and the MC68328 DragonBall™ Integrated Processor

The enhanced architecture of PowerPC™ microprocessors, created to drive the most powerful personal computers in the world, is now changing the world of embedded processing. It's the optimum solution any time:

- system performance is a principal goal,
- you need a range of software–compatible solutions that match your product's performance levels,
- you need a full computer architecture, or
- your product's software is closely related to PC software technology.

All embedded PowerPC™ microprocessors benefit — both technologically and economically — from their desktop heritage. Cutting–edge technologies are shared with desktop versions, from integral FPUs to the use of sub–half–micron process. And economies of scale make them more cost–effective than other RISC architectures.

MPC821 RISC Microprocessor

- Embedded PowerPC™ Core provides 66 MIPS (using Dhrystone 2.1) or 115K Dhrystones 2.1 at 50 MHz and 33 MIPS (using Dhrystone 2.1) or 58K Dhrystones 2.1 at 25 MHz
- Data Bus Dynamic Bus Sizing for 8–, 16–, and 32–Bit Busses
- Completely Static Design (0–50 MHz Operation)
- Four Baud Rate Generators
- Two Serial Communication Controllers (SCC)
- Two Serial Management Channels (SMCs)
- One Serial Peripheral Interface (SPI)
- One Interprocessor–Integrated Circuit (I(2)C) Port
- Time–Slot Assigner
- Parallel Interface Port
- General–Purpose Timers
- Memory Controller (Eight Banks)
- System Interface Unit (SIU)
- LCD Interface Controller
- PCMCIA Controller
- Low–Power Support
- Debug Interface
- 3.3 V Operation with TTL Compatibility on I/O Pins

MPC823 RISC Microprocessor

- Embedded PowerPC™ Core provides 66 MIPS (using Dhrystone 2.1) or 115K Dhrystones 2.1 at 50 MHz and 33 MIPS (using Dhrystone 2.1) or 58K Dhrystones 2.1 at 25 MHz
- Data Bus Dynamic Bus Sizing for 8–, 16–, and 32–Bit Busses
- Completely Static Design (0–50 MHz Operation)
- Two Baud Rate Generators
- One Serial Communication Controller (SCC)
- Two Serial Management Channels (SMCs)
- One Serial Peripheral Interface (SPI)
- One Interprocessor–Integrated Circuit (I(2)C) Port
- Time–Slot Assigner
- General–Purpose Timers
- Memory Controller (Eight Banks)
- System Interface Unit (SIU)
- LCD Interface Controller
- PCMCIA Controller
- Low–Power Support
- Debug Interface
- 3.3 V Operation with TTL Compatibility on I/O Pins

MC68328 DragonBall™ Integrated Processor

- Static 68EC000 Core
- PCMCIA Support
- LCD Controller
- Real Time Clock
- Pulse Width Modulator
- Serial Peripheral Interface
- UART
- Two 16–bit Timer/Counters
- 16 Chip Selects
- System Integration
- Low Power Consumption
- 24 Address Lines, 16 Data Lines
- 2.7 MIPS @ 16 MHz
- Available in 16 MHz
- Available in 3.3V

LCD Driver Product Summary

Part Number	Description	System	Application Examples	Display Size Examples	Package
Segmented LCD Driver for Low MUX Application					
MC14LC5003 MC14LC5004	4 MUX, total 128 Segments, Serial In 4 MUX, total 128 Segments, IIC	Low MUX, General MCU	Fax Machines, Pager, Digital Meter, Home Appliances	32 x 4	QFP, Bare die
DragonKat™ Series LCD Driver Kits with MC68HC05L10/L11					
MC141511A	DragonKat 1+ Slave Driver, 32/41 MUX, 128 Segments	DragonKat 1+ MC68HC05L10	Databank, Pager, Organizer, Games	128 x 32/41, 256 x 32/41	TAB, Bare die
MC141512 MC141514 MC141515 MC141519	DragonKat 2 Backplane Driver, 146 MUX, 80 Backplanes DragonKat 2 Segment Driver, 146 MUX, 160 Segments DragonKat 2 Backplane Driver, 146 MUX, 160 Backplanes DragonKat 2 Segment Driver, 80 MUX, 160 Segments	DragonKat 2 MC68HC05L11	Transistor, Dictionary, Pen–based Organizer, Low Cost PDA	160 x 80, 320 x 146, 320 x 160	TAB
MC141516 MC141518	64 MUX LCD Backplane Driver, 64 Backplane Outputs 64 MUX LCD Segment Driver, 80 Segment Outputs	DragonKat 2 MC68HC05L11, other MCU with SPI	Pager, Games, Dictionary	80 x 64, 160 x 64, 240 x 64	TQFP, Bare die
TFT LCD Driver Accepts RGB Signal Inputs					
MC141522 MC141524	TFT–LCD Gate (Row) Driver, 120 Row Outputs TFT–LCD Source (Column) Driver, 120 Column Outputs	Active LCD	Portable TV, Projector	480 x 240, 720 x 480	TAB
MC14158X Series LCD Driver with Commons, Segments, Annunciators "All In One" Chip					
MC141531 MC141532 MC141533 MC141535 MC141537 MC141539	17 Com, 120 Seg, 3 Annunciators 33 Com, 120 Seg, 4 Annunciators 33 Com, 120 Seg, 4 Annun, Split Com 17 Com, 161 Seg, 4 Annunciators 16 Com, 120 Seg, 3 Annunciators 32 Com, 120 Seg, 4 Annunciators	General MCU, 6800, 68K (Parallel Interface)	Mobile Communication Devices, Pager, Cellular, PHS	120 x 17 120 x 33 120 x 33 161 x 17 120 x 16 120 x 32	TAB, Bare die, Au bump die
300 MUX LCD Driver without Display DRAM					
MC141562 MC141563	LCD Common Driver, 100 Com o/p LCD Segment Driver, 80 Seg o/p	DragonBall™ MC68328, General MCU with LCD Controller	PDA, Palm–top, Sub–notebook	320 x 200, 320 x 240, 640 x 200	TAB, Au bump die
MC14180X Series LCD Driver for Cellular Phone/PHS Applications					
MC141800A	65 Common, 12B Segment o/p	General MCU, 6800, 68K (IIC, Parallel Interface)	Cellular Phone, PHS Large Display Pager	128 x 65, 128 x 64 plus 128 Icons	TAB, Au bump die

Monitor On Screen Display (MOSD)

Motorola's MOSD family includes **ES**(EMOSD & SMOSD) and **AG**(AMOSD2 & GMOSD) **pin–compatible** series which provide easy–to–use, sophisticated hardware to generate on screen display function for Monitor, LCD, TV and Display Systems. In **ES series**, either 128/256 number of font's device can be chosen and 8 real time programmable **RAM** are equipped for flexible icon design for different OEM models. For **AG series**, besides 128/256 font option, both devices provide a **SVGA** resolution display with maximum dot clock at **92.2MHz**. The two series offer DAC integration, programmable display resolutions and user–friendly display attribute controls. Users can freely choose Motorola MOSD devices to fulfill their full application spectrum: from low–end to high–end, from cost–sensitive to feature–oriented. In addition, **custom mask ROM** is welcome for tailor–made model design. Details of the MOSD devices can be found in the following section.

	EMOSD Enhance MC141541	**SMOSD Super MC141548/9**	**AMOSD2 Advance MC141546/7**	**GMOSD Graphic MC141542/5**
Display Area	10R x 24C	15R x 30C	15R x 30C	15R x 30C
Color	8	8	8	8
Intensity	High	High/Low	High/Low	High/Low
Windows	3	4	4	4
No. of Font	128	256	128	256
ROM	120	248	128	288
Mask ROM	Yes	Yes	Yes	Yes
RAM	8	8	0	0
Font Matrix	10 x 16	10 x 16	12 x 18	12 x 18
Resolution	EGA	VGA	SVGA	SVGA
Max. Dot Clk.	52.8 MHz	76.8 MHz	92.2 MHz	92.2 MHz
Max Freq.	110 KHz	120 KHz	120 KHz	120 KHz
DAC Integration	0	12	12	12
16 DIP, 0 DAC	MC141541P	MC141549P	MC141547P	MC141545P
24 DIP, 8 DAC	N.A.	MC141548P	MC141546P	MC141542P
28 SOIC, 12 DAC	N.A.	Custom	Custom	Custom
Special Display Feature	— Double Height — Double Width — Shadowing — Bordering	EMOSD Plus — Windows Shadow — Blinking — Fade–In/Fade–Out — Automatic Height — Icon Intensity — Windows Intensity	— Double Height — Double Width — Shadowing — Bordering — Automatic Height — Spacing Control — Windows Intensity	AMOSD2 Plus — 16 Multi–color Font — 7 Color Background — Windows Shadow — Blinking — Fade–In/Fade–Out — Automatic Height — Icon Intensity
Data Sheet	MC141541/D	MC141548/D	MC141546/D	MC141542/D
Evaluation	MC141541EVK	MC141548EVK	MC141546EVK	MC141542EVK

Scorpion Graphics Processor (MC92100)

Graphics Display Generator, SRAM Controller, and Digital Video Encoder – on a single chip

Scorpion is a graphic display generator and NTSC/PAL digital video encoder for analog and digital video systems including DVD, STB, and Internet TV applications. The display architecture has been designed to provide a high-quality television-oriented graphics overlay. The graphics overlay matches the resolution and color depth of the NTSC/PAL baseband video and optimizes memory usage. Scorpion can provide generation of true color graphics, mixing of video and graphics in 1.6% steps (64 different levels), and control and display on four image layers. Scorpion is controlled by high-level language instructions from a host processor (PowerPC™ or Coldfire™).

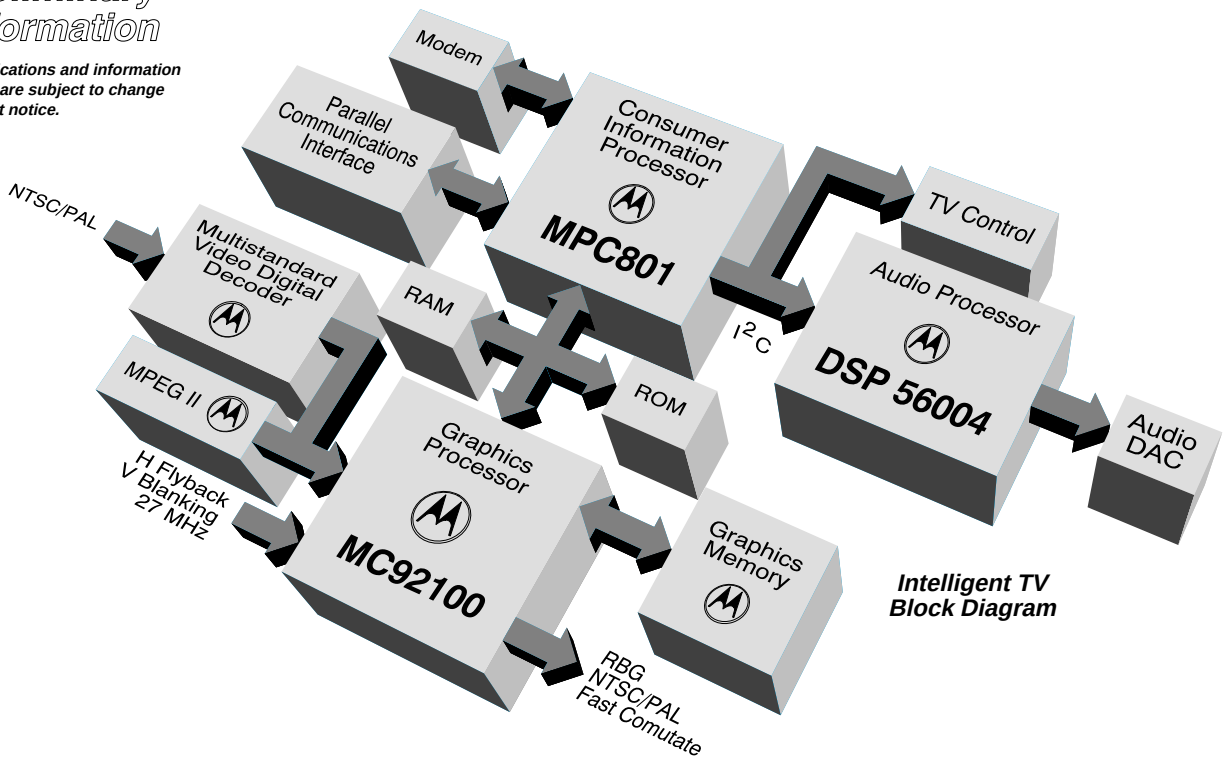
The digital video encoder accepts a CCIR-656 data stream with embedded synchronization codes or it may be genlocked with a television horizontal flyback and vertical synchronization signal. Scorpion supports both a composite and separate luma and chroma output (S-VHS) analog video generation, or composite and RGB. It also includes Macrovision™ generation of copy protection and a closed caption inserter for line 21.

MC92100 Features

- Graphics controller compatible with high-level languages
- Microware OS9000 (for PowerPC) MAUI dedicated software driver available
- Host processor interface for PowerPC and Coldfire
- True color graphics generator at VGA density with video/graphics mixing in 1.6% steps (64 levels)
- True color graphics generator for NTSC (720 x 480 pixels) and PAL (720 x 576 pixels)
- Selectable conversion from CCIR-656 aspect ratio to square pixels
- Selectable vertical filtering for flicker reduction
- Graphics matched to resolution and color depth of high-quality NTSC/PAL television graphics overlay
- Uses 12/16 bits per pixel to store images equivalent to 24-bit-per-pixel computer images and CCIR-601 data streams and/or a 2/4/8-bit color look-up table (CLUT)
- Maximum of two viewports on any horizontal line
- Multiple viewports vertically
- Supports four image levels including video, two viewports, and hardware cursor
- Graphics display requires less than 30% of memory bandwidth per viewport, allowing rapid processor updates
- Digital video encoder for converting CCIR-656 to composite and S-VHS analog video
- Macrovision generator for copy protection and closed caption inserter for line 21 data
- SDRAM controller for shared system and graphics memory with glueless interface
- 208 QFP and 196 PBGA packages

Preliminary Information

Specifications and information herein are subject to change without notice.



Intelligent TV Block Diagram

M5C™ Series Gate Arrays/M5CB™ Series Standard Cells

Deep Sub-Micron CMOS Process

The M5C/CB Series feature performance optimized 3.3 V and 5 V tolerant I/O capability, high-speed interfaces, and analog PLLs for chip-to-chip clock skew management. The gate length has been reduced to 0.45 μm nominal Leff to provide improved 3.3 V performance.

The M5C/CB Series utilizes Motorola's standard 0.5 micron CMOS process for logic, the same one used for products like the 68060 and low power 68040. The process has advanced features such as tungsten plugged, stacked vias and contacts, and planarized metalization.

High-speed SCI-LVDS, GTL, PCI and PECL macros offer enhanced chip-to-chip communication. Motorola's SCI-LVDS (Low-Voltage Differential Swing) interface enables differential operation up to 311 MHz. Analog PLLs may be embedded into three corners of the die for on-chip 50% duty cycle clock signals up to 175 MHz with only 250 ps jitter plus phase error, which provides on-chip clock synthesis.

The M5C/CB Series offers a large selection of diffused SRAM blocks through the FeliX™ Compiler. FeliX can generate a variety of word and bit length combinations in synchronous single-and dual-port RAMs.

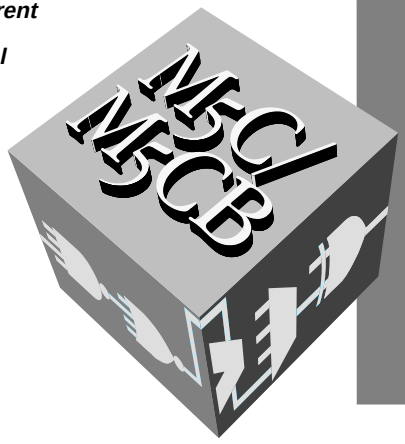
M5C/CB Series Features

- 0.45 μm effective gate length process, triple-layer metal
- Typical gate delay of 240 ps at 3.3 V (CMND20, FO=2)
- Performance optimized 3.3 V core
- Low power of 1 μW/gate/MHz at 3.3 V
- Multiple VDD rails for the core and 3.3 V outputs
- Cell library optimized for efficient logic synthesis
- Single-, and dual-port metal and diffused SRAM compilers
- Contact programmable ROM compiler
- Internal macros characterized from 1.4 to 3.6 volts
- High-speed SCI-LVDS, GTL, PCI and PECL interface macros
- Full support of DFT and SCAN methodology; JTAG/Boundary Scan embedded in periphery
- Clock tree synthesis with clock skew management through optional embedded analog PLL macro functions for clocks up to 175 MHz at 3.3 V with a 50% duty cycle
- Powerful design environment using Mentor Graphics, Synopsys, Cadence Design Systems, Viewlogic, and Motorola's design tools
- Advanced plastic - BGA, Tape Ball Grid Array (TBGA), MQUAD, thermally enhanced QFP and PQFP packaging

M5C Series Features	Available Gates	No. of Die Pads	I/O Cells	Package Pins
M5C078	77,763	188	196	128-160
M5C112	112,908	224	240	160-208
M5C142	142,572	248	272	160-225
M5C208	207,507	292	324	208-225
M5C252	252,300	320	368	208-313
M5C307	307,200	348	408	208-313
M5C380	380,200	388	456	208-352
M5C460	460,992	424	504	208-420
M5C557	557,283	460	556	313-420

0.5 Micron CMOS Process

Diffused SRAMs. User definable SRAMs configurations are available using Motorola's FeliX SRAM compiler. FeliX generates several versions of a given SRAM size, each with different performance, gate counts, and physical configurations.



M5CB Series Features	Available Gates	No. of Die Pads	I/O Cells	Package Pins
M5CB183	47,000	160	144	80-160
M5CB215	69,000	192	176	80-225
M5CB247	94,000	224	208	80-225
M5CB278	122,000	256	240	80-225
M5CB303	147,000	280	264	80-256
M5CB325	171,000	300	284	80-256
M5CB347	197,000	324	308	100-313
M5CB375	231,000	352	336	100-313
M5CB403	268,000	380	364	144-313
M5CB441	323,000	420	404	144-420
M5CB476	377,000	452	436	144-420
M5CB514	440,000	492	476	225-420
M5CB554	511,000	532	516	225-420
M5CB596	591,000	576	560	225-420

H4EPlus™ Series Gate Arrays

Enhanced Density Mixed-Voltage Environments

The H4EPlus Series arrays offer a fully featured 3.3 V, 5 V and mixed-voltage capable family combined with an increased core density providing over 50% more gates in the same die area as Motorola's H4CPlus Series. It offers a wide range of mixed-voltage I/Os, high-speed interfaces, and analog PLLs for clock skew management. The gate length of 0.65 µm nominal Leff provides a competitive 3.3 V performance, with increased performance at 5 V.

The low- and mixed-voltage capability allows designers to customize the H4EPlus arrays to fit power and performance needs. All H4EPlus arrays have dual VDD rails, with custom power/ground tying, to provide full 3.3 V, 5 V and mixed-voltage I/O capability. Additionally, the core logic may be powered at either 3.3 V or 5 V.

High-speed CMTL™, GTL™, PCI and PECL macros offer enhanced chip-to-chip communication. Motorola's CMTL (Current Mode Tranceiver Logic™) have optional internal active termination and support differential clock rates of up to 300+ MHz. GTL, PCI and PECL are available for interfacing to standard logic and RAMs.

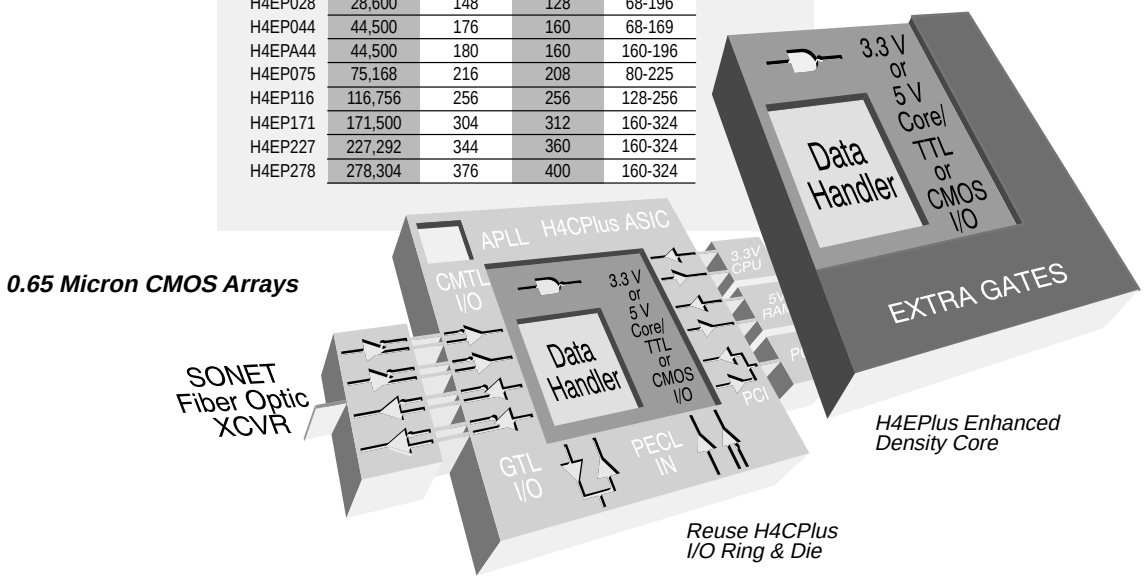
Each array can have up to two APLL (Analog Phased Lock Loop) macros with separate APLL power pins for lower noise and phase jitter. No external components are required since the VCO filter is built in. These can be used in applications such as clock synthesis with a worst–case VCO frequency of 70 to 250 MHz.

H4EPlus Series Features

- 0.65 µm Leff, channelless, triple-layer metal gate arrays
- 8,056 to 278,304 available gates
- Typical gate delay of 280 ps at 5 V and 420 ps at 3.3 V (NAN2, FO=2)
- Low power, 1 µW/gate/MHz (3.3 V), 3 µW/gate/MHz (5 V)
- 3.3 V, 5 V or mixed system and core voltage levels
- Custom power bus tying and ground bus isolation for special power needs
- Configurable I/O cell supports 2 to 24 mA, up to 48 mA using dual I/O cells
- PCI compliant 5 V and 3.3 V I/O buffers (5 V tolerant), 3 V I/O macros, and 5 V I/O fail-safe macros
- Differential and single-ended GTL I/O and PECL input macros
- Analog PLL with 70 to 250 MHz worst-case VCO frequency
- DFT methodology support (JTAG, BIST, LSSD, and ESSD)
- JTAG 1149.1 boundary scan built into I/O macros
- Single-, dual-, and quad-port metal SRAMs at 3.3 V and 5 V
- Single-, and dual-port diffused SRAMS
- Powerful design environment using Mentor Graphics, Cadence Design Systems, Synopsys, Quad Design Technology, and Motorola design tools
- GTPAC™ ball-grid array, Thin QFP, Thermally Enhanced QFP, PLCC, and Ceramic BGA packaging

H4EPlus Series Features	Available Gates	No. of Die Pads	I/O Cells	Package Pins
H4EP008	8,056	88	68	44-84
H4EP012	12,220	104	84	44-100
H4EP017	17,316	120	100	44-144
H4EP028	28,600	148	128	68-196
H4EP044	44,500	176	160	68-169
H4EPA44	44,500	180	160	160-196
H4EP075	75,168	216	208	80-225
H4EP116	116,756	256	256	128-256
H4EP171	171,500	304	312	160-324
H4EP227	227,292	344	360	160-324
H4EP278	278,304	376	400	160-324

H4EPlus provides 50% more gates than equivalent H4CPlus die size



Literature

To order any literature item(s), contact the Motorola Semiconductor Products Literature Center at 1–800–441–2447

Design Manuals

Order Number	Description
H4EPDM/D	H4EPlus Series CMOS Arrays
M5CDM/D	M5C Series CMOS Arrays

Data Sheets

H4EP/D	H4EPlus Series CMOS Arrays
M5C/D	M5C Series CMOS Arrays
M5CB/D	M5CB Series Standard Cells

Brochures/Selector Guides/Misc.

BR916/D	Packaging Manual for ASIC Arrays
BR1441/D	ASIC Reliability and Quality Report
BR1473/D	The Individual Solution

Application Notes/Article Reprints

Order Number	Description
AN1093/D	Delay and Timing Methods for CMOS and ASICs
AN1500/D	JTAG Boundary Scan for H4C Arrays
AN1502/D	Embedded RAM/BIST
AN1509/D	ASIC Clock Distribution Using PLL
AN1512/D	TestPAS Primer
AN1521/D	High-Performance CMOS Interfaces
AN1522/D	Analog Phase-Locked Loop for H4EPlus and M5C Series Arrays
AN1534/D	Design Considerations of Plastic Ball-Grid Arrays for CMOS Gate Arrays
AN1553/D	Minimizing Skew in Gate Arrays
AN1554/D	SRAM Built-in-Self Test
AR518/D	Gate Arrays Simplify Translation Between High Speed Logic Families
AR524/D	Pick the Right ASIC Package
AR611/D	Exploit the Potential of High-Performance CMOS by Selecting the Best Interface

Worldwide Design Centers

ADCD Regional Design Centers - U.S.A.
California, San Jose (408) 991-7331
Georgia, Atlanta (404) 729-7137
Illinois, Chicago (847) 413-2526
Massachusetts, Marlborough (617) 932-6084

Optimum Design, Service and Support

Motorola has established a worldwide network of ADC design centers to serve the design and applications needs of its customers. The centers provide support at all phases of your semi-custom design. Skilled designers provide training for Motorola's ADC design flows, as well as applications support for CAD and silicon issues during the design process.

ADCD Regional Design Centers - International

European Headquarters, Germany, Munich
(089) 92103-306
England, Aylesbury, Bucks (01296) 395252
France, Velizy (01) 34635900
Holland, Best (04998) 61211
Israel, Tel Aviv (09) 590-303
Italy, Milan (02) 82201
Sweden, Stockholm (08) 734-8800

Hong Kong, Silicon Harbour Center, Tai Po
(852) 2666-8333
Japan, Tokyo (03) 440-3311