# Interfacing AT93CXX Serial EEPROMs with AT89CX051 Microcontrollers

Serial memory devices offer significant advantages over parallel devices in applications where lower data transfer rates are acceptable. In addition to requiring less board space, serial devices allow microcontroller I/O pins to be conserved. This is especially valuable when adding external memory to low pin count microcontrollers such as the Atmel AT89C1051 and AT89C2051.

This application note presents a suite of software routines which may be incorporated into a user's application to allow AT89CX051 microcontrollers to read and write AT93CXX serial EEPROMs. All seven AT93CXX device functions are supported: read, write, write all, erase, erase all, erase/write enable and erase/write disable. The routines are general purpose, supporting both eight-bit and sixteen-bit accesses to all members of the 93CXX family. In addition, both 3-wire and 4-wire configurations are supported.

The AT93CXX may be connected to the AT89CX051 microcontroller in either a 3-wire (Figure 1) or 4-wire (Figure 2) configuration. In the 3-wire configuration, the EEPROM serial data in (DI) and serial data out (DO) pins are both connected to the same microcontroller I/O pin, thereby saving a pin. This is possible because the microcontroller I/O pins can be dynamically reprogrammed as input or output.

Note the strapping of the AT93CXX ORG pins shown in Figure 1 and Figure 2. The ORG (internal organization) pin selects 8-bit data when grounded and 16-bit data when floating or tied to $V_{CC}$. The ORG pin connections shown in the figures are for illustration only; 8-bit or 16-bit data may be selected in either the 3-wire or 4-wire configuration.

The software for this application may be obtained by downloading from Atmel's Web Site or BBS. Consult the comment block at the beginning of the source code file for detailed information on features and operation.

**Web Site: http://www.atmel.com**

**BBS: 1-(408) 436-4309**

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**Application Note**

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**Figure 1.** 3-Wire Configuration

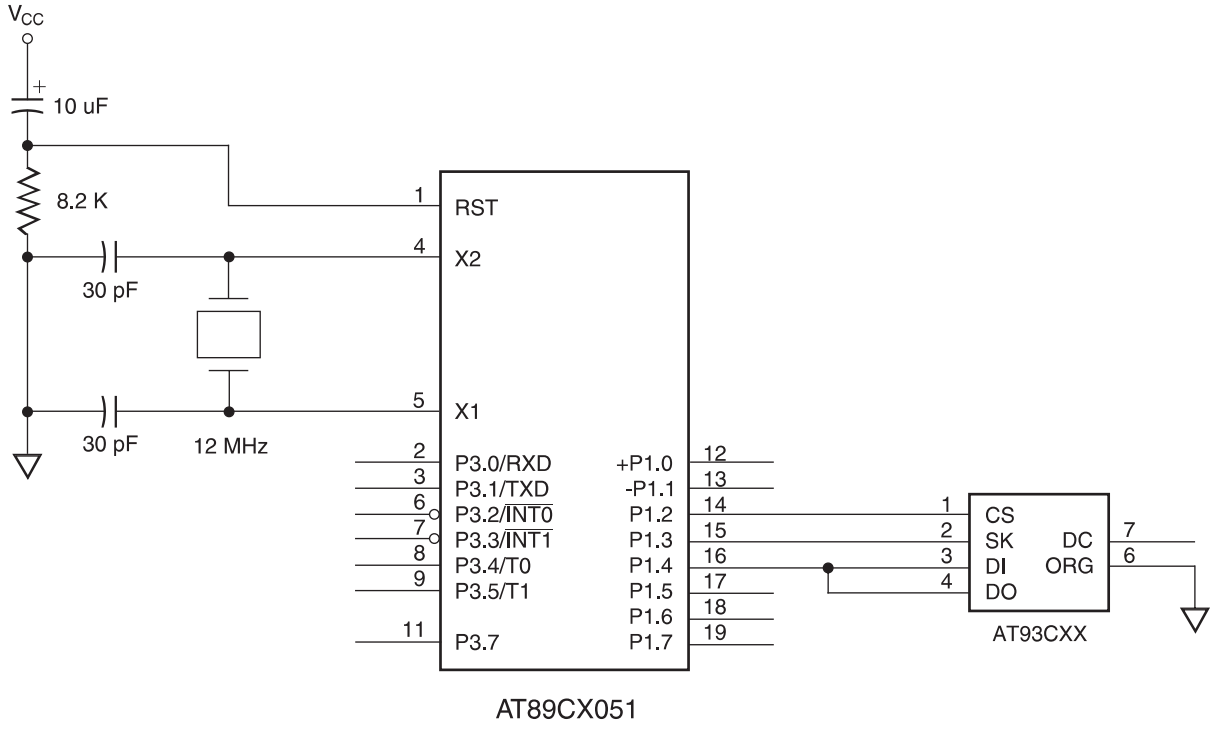


**Figure 2.** Typical Circuit Configuration