Intel® 840 Chipset Platform Memory Expansion Card (MEC)

Design Guide

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Revision History

Rev.	Description	Date
-001	• Initial Release	July 2000

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1. Overview

This document provides Memory Expansion Card (MEC) design guidelines for the Intel® 840 chipset platform. The memory cards will be designed to support both PC800 and PC600 RDRAM. These RDRAM-based MECs are intended for use as the main memory subsystem for workstation and server designs using the Intel® 840 chipset.

This design guide organizes Intel's design recommendations for memory expansion cards. In addition to providing motherboard design recommendations (e.g., layout and routing guidelines), this document also addresses system design issues.

This document presents design recommendations, board schematics, debug recommendations, and a MEC checklist. The design recommendations should be followed strictly for all MEC designs. These design guidelines have been developed to ensure maximum flexibility for MEC designers while reducing the risk of board-related issues.

Schematics for a Memory Expansion Card are included in this design guide. MEC board designers can use the MEC schematics as a reference. They provide a reference for RDRAM-based MEC designs. Additional flexibility is possible through other permutations of these options and components.

1.1. Terminology

Term	Description
Direct RDRAM	
RSL	Rambus* Signaling Level is the name of the signaling technology used by Direct RDRAM.
Rclk	Refers to the RSL bus' high speed clock in a generic fashion, often in the context of clock counts in timing specs.
RAC	Direct RDRAM ASIC Cell. It is the embedded cell designed by Direct RDRAM that interfaces with the Direct RDRAM devices using RSL signaling.
RMC	Direct RDRAM Memory Controller. This is the logic that directly interfaces to the RAC.
RIMM	Direct RDRAM Interface Memory Module.
Components	
MCH	The Memory Controller Hub component that contains the processor interface, Direct RDRAM controller, and AGP interface. It communicates with the I/O Controller Hub over a proprietary interconnect called Hub Interface.
Intel® 82803AA (MRH-R)	The Memory Repeater Hub for RDRAM.
'expansion' channel	The RSL bus which connects the MCH to the 82803AA (MRH-R). This term only applies to the interface between the MCH and MRH-R component.
'stick' channel	An RSL Direct RDRAM bus which connects an 82803AA (MRH-R) to its RDRAM devices. An MRH-R can support a max. of 2 stick channels, Stick Channel A and Stick Channel B.

1.2. References

- Intel® 840 (MCH) Datasheet
- Intel® 840 Chipset Platform Design Guide
- Rambus®* RDRAM Documentation
- Intel® 82803AA (MRH-R) Datasheet

1.3. Chipset MEC Memory Components

A memory expansion card can be used to increase memory size configurations that are required for most server and workstation designs. The Intel® 840 chipset has a memory repeater hub component that allows for this memory expandability (up to 2 GB). The Intel® 82803AA Memory Repeater Hub for RDRAM (MRH-R) provides this memory expansion capability.

The MRH-R provides a pass-through architecture for two additional Direct RDRAM channels from each MCH RDRAM ‘expansion’ channel. One MRH-R components per MCH Direct RDRAM channel is supported. It integrates:

- Support for two Direct RDRAM channels and one expansion channel
- Support for PC800 and PC600RDRAM
- Support for 64Mbit, 128Mbit and 256Mbit RDRAM technologies.
- 400 MHz or 300 MHz Direct RDRAM interface
- Integrated System Management Bus(SMBus) Controller for SPD of RIMMs

2. Memory Expansion Card Pinout

2.1. Edge Connector Example Pinout

Contact your local Intel representative for an example pinout.

2.2. Edge Connector Pin Description

The following pin description is only for the pins that are required/recommended to implement a fully functional Memory Expansion Card using Intel® 840 chipsets.

2.2.1. RSL and CMOS pins

Signal	Type	Description
CHx_EXP1	RSL	**Row Control:** This signal carries the row control packets from the memory controller to attached MRH-Rs.
CHx_EXP0	RSL	**Column Control:** This signal carries the column control packets from the memory controller to attached MRH-Rs.
CHx_DQA[8:0]	RSL	**RDRAM Data Bus, Data Byte A.** Bi-directional 9 bit data bus A. These correspond to the CHx_DQA[8:0] signals on the MCH.
CHx_DQB[8:0]	RSL	**RDRAM Data Bus, Data Byte B:** Bi-directional 9 bit data bus B. These correspond to the CHx_DQB[8:0] signals on the MCH.
CHx_RQ[7:5]/ ROW[2:0]	RSL	**RDRAM Row Request:** These signals carry row request packets from the memory controller to the MRH-Rs.
CHx_RQ[4:0]/ COL[4:0]	RSL	**RDRAM Column Request:** These signals carry column request packets from the memory controller to the MRH-Rs.
CHx_CTM	RSL	**RDRAM Clock To MCH:** One of the two differential transmit clock signals used for MRH-R to MCH operations.
CHx_CTM#	RSL	**RDRAM Clock To MCH Complement:** One of the two differential transmit clock signals used for MRH-R to MCH operations.
CHx_CFM	RSL	**RDRAM Clock from MCH:** One of the differential receive clock signals used for MCH to MRH-R operation.
CHx_CFM#	RSL	**RDRAM Clock From MCH Complement:** One of the differential receive clock signals used for MCH to MRH-R operation.
CHx_SIO	CMOS	**RDRAM Serial IO Chain:** Serial input/output pins used for reading and writing control registers. These correspond to the SIO signals on the MCH.
CHx_SCK	CMOS	**RDRAM Serial Clock:** Clock source used to used for timing of the CHx_SIO and CHx_CMD signals. This corresponds to the SCK signal on the MCH.
CHx_CMD	CMOS	**RDRAM Serial Command:** Serial command input used for control register read and write operations. This corresponds to the CMD signal on the MCH.
SDA	CMOS	**SMBus Data:** SMBus interface for DIMM SPD detection, disabling of SDRAM clocks and reading of any on-board FRU EEPROM.

Signal	Type	Description
SCLK	CMOS	**SMBus Clock:** SMBus clock used for timing on SDA.
SMBWE	CMOS	**Write Protect for SMBus EEROMS:** This signal is used to write protect all SMBus EEPROM devices to avoid SPD data corruption. This can be controlled by a system GPO.
RCI_AUX	CMOS	**System GPO:** This pin is required to implement the workaround for excessive RDRAM power consumption during initialization. See section 5.3 for details.
PWROK	CMOS	**PWROK for CMOS Shunting Logic on MEC:** The system PWROK signal is used to shunt the SCK CMOS signal to GND when entering/exiting the STR state. See section 3.5.7.2 for details.
RESET#	CMOS	**Reset:** When asserted, this signal asynchronously resets the MRH-R logic. This is the system reset signal used for resetting the MCH, ICH, etc. NOTE: Review MRH-R documentation for proper RESET# recommendations for STR implementations.

NOTES:
1. "x" denotes MCH 'Expansion' channel A and B. For example, the "x" in the signal name CHx_DQB[8:0] denotes A and B.

2.2.2. Voltage/Ground References

Signal	Description
CHx_RAMREF_FM	**Source Generated RSL Reference Voltage (1.4V):** This signal is from voltage divider network near memory controller on motherboard to MRH-R on MEC.
CHx_RAMREF_TM	**Source Generated RSL Reference Voltage (1.4V):** This signal is from voltage divider network on MEC to memory controller on motherboard.
1_8V	**1.8V Power Pins:** Power pins for MRH-R and all V_{term} on MEC.
3.3V	**3.3V Power Pins:** Power Pins for DRCG
12V	**12V Power Pins:** Power pins for on-board DC-to-DC converter for 2.5V (RDRAM) generation on MEC.
SPD_VCC	**2.5V Power Pin:** Power pin used for MRH-R SMBus pull-ups for operation at a 2.5V signaling level.
GND	**Ground Pins:** Ground pins placed between all RSL signals.

NOTES:
1. "x" denotes MCH 'Expansion' channel A and B. For example, the "x" in the signal name CHx_RAMREF_TM denotes A and B.

3. MEC Layout and Routing Guidelines

This chapter describes layout and routing recommendations to ensure a robust MEC design. Follow these guidelines as closely as possible. Any deviations from the guidelines listed here should be simulated to ensure adequate margin is still maintained in a MEC design.

Caution: If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals should still be simulated to ensure proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely. Any deviation from these guidelines must be simulated!

3.1. General Recommendations

When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed. In addition, the PCB should be fabricated as documented in section 0 of this document.

All recommendations in this section (except where noted) assume wider traces in trying to achieve a 28-ohm Direct RDRAM channel impedance. If trace width is greater than this recommendation then the trace spacing requirements must be adjusted accordingly (linearly).

Additionally, these routing guidelines are created using the *stack-up* described in section 0. If this stack-up is not used, extremely thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

3.1.1. Test Coupon Design Guidelines

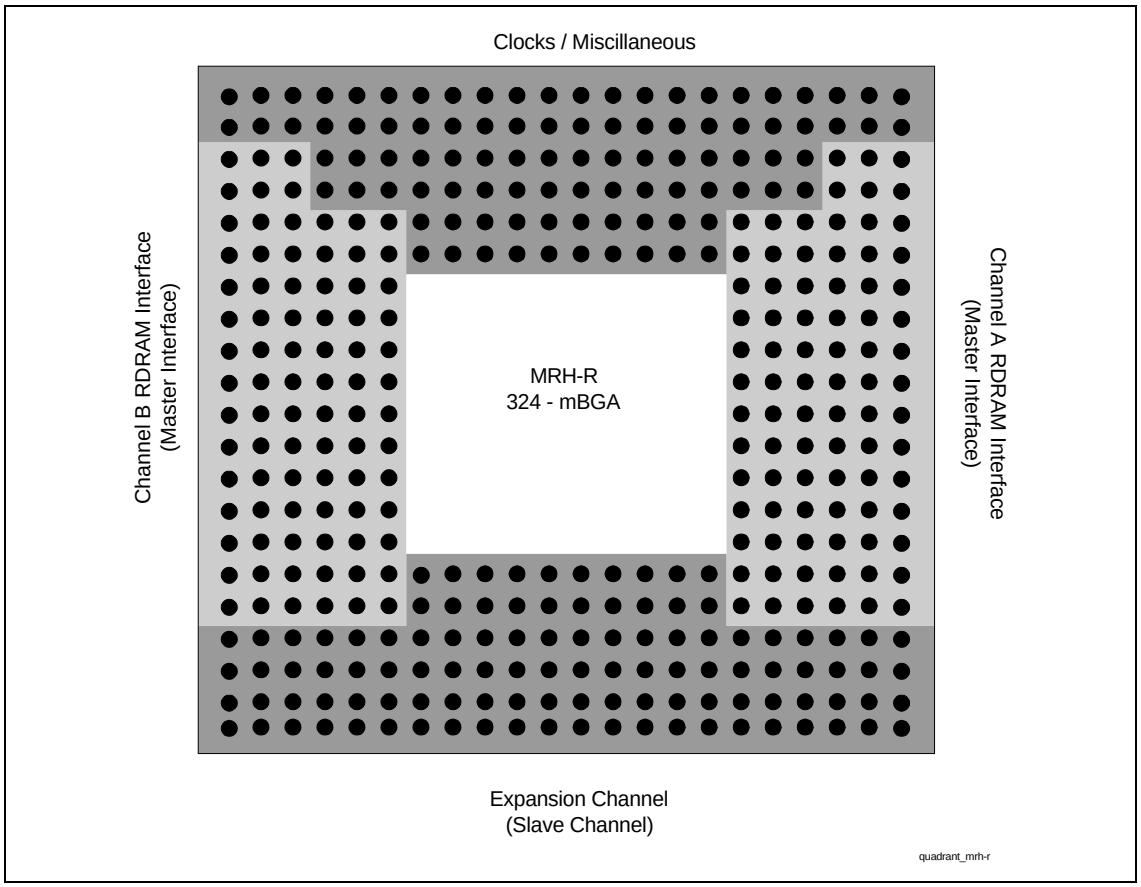
Characterization and understanding of the trace impedance is critical for delivering reliable systems at the increased bus frequencies. Incorporating a test coupon design into the MEC will make testing simpler and more accurate. The test coupon pattern must match the probe type being used.

The *Printed Circuit Board (PCB) Test Methodology* Document should be used to ensure MEC are within the 28Ω ±10% requirement. The *Intel Controlled Impedance Design and Test* Document should be used for the test coupon design and implementation. These documents can be found at: http://developer.intel.com/design/chipsets/applnotes/index.htm#rdram – Select “Application Notes”

3.2. 82803AA (MRH-R) Quadrant Layouts

The quadrant layouts shown should be used to conduct routing analysis. These quadrant layouts are also designed for use during component placement.

Figure 1. 82803AA (MRH-R) 324-MBGA Quadrant Layout (topview)



3.3. Printed Circuit Board Description

The perfect matching of transmission line impedance and uniform trace length are essential for the Direct RDRAM interface to work properly. Maintaining 28 Ω ±10%) loaded impedance for every RSL (Rambus* Signaling Level) signal has changed the standard requirements for trace width and prepreg thickness across Intel® 840 chipset platforms and Memory Expansion Card designs.

A Memory Expansion Card printed circuit board stack-up recommendation calls for six layers. However, the MEC design depends on the memory capacity required. The PCB stackup must be designed to achieve the following calculated board characteristics (see examples below):

Table 1. PCB Calculated Parameters

Parameter	Min	Max	Notes
Propagation delay: S_0 [ps/in] (outer layers)	150	160	3
Propagation delay: S_0 [ps/in] (inner layers)	175	185	3
Trace impedance: Z_0 [Ω] (RSL signal layers: 28-ohm, ±10%)	25.2	30.8	1, 2

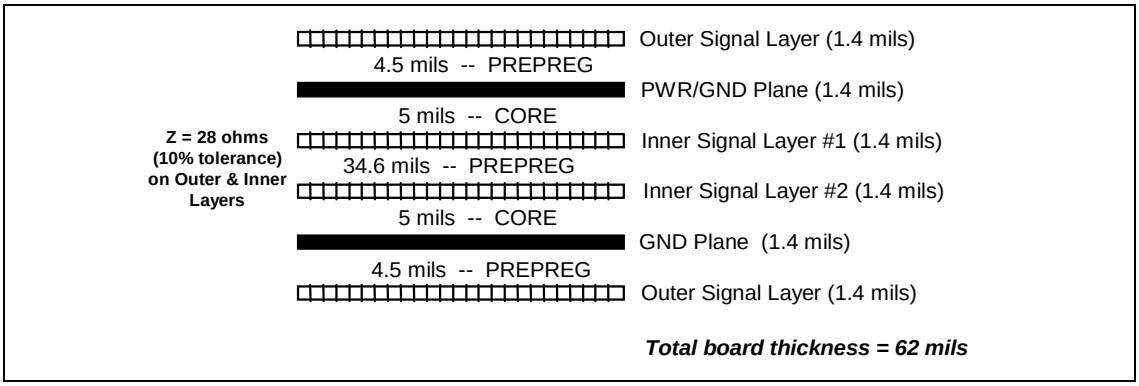
NOTES:
1. Required Dielectric: 4.1 to 4.3.
2. This is a strict requirement for routing all RSL signals.
3. Assumptions based on stack-up examples below.

The following stack-up examples allow for a uniform channel impedance of 28 Ω ±10%. Typically, to achieve 28 Ω nominal impedance with a standard prepreg will require wider traces (i.e., 28 mils wide with 7 mil standard prepreg thickness). Wider traces can make it difficult to break out of and break into the rows of RSL signals on the MRH-R. To reduce the trace width, a thinner prepreg is required. This thinner prepreg allows smaller trace widths to meet the 28 Ω ±10%) nominal impedance requirement (i.e., 18 mil wide traces).

The figure below is an example stack-up that can be used to design an MEC using the MRH-R component.

- Assumptions
  - — Example stack-up should meet the RSL impedance requirement of 28 Ω ±10% on inner/outer signal layers.
  - — Recommend routing all RSL signals referenced to a GND plane to insure proper current return paths.
  - — 18 mil wide RSL traces on inner and outer layers.

Figure 2. Example 6-layer RDRAM-based MEC PCB Stackup

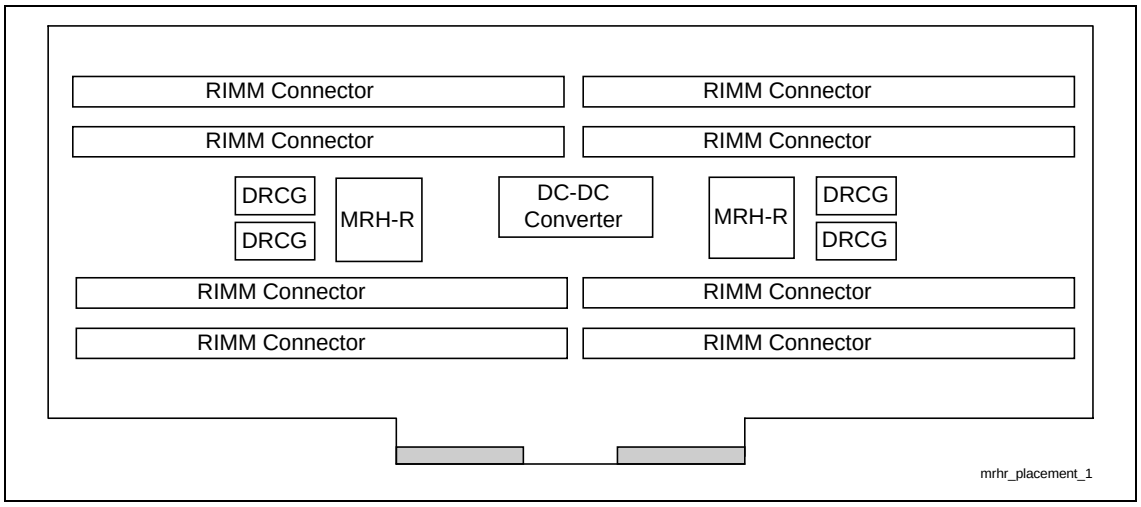


3.4. MEC Component Placement

Notes:

1. The component placements and layouts shown in the following figure are conceptual diagrams.
2. The trace length limitation between critical connections is addressed later in this document.
3. The figures are for ***reference only.***

Figure 3. Example 8 RIMM/2 MRH-R MEC Component Placement



3.5. RDRAM Interface

The Direct RDRAM Channel is a multi-symbol interconnect. Due to the length of the interconnect, and the frequency of operation, this bus is designed to allow multiple command and data packets to be present on a signal wire at any given instant. The driving device sends the next data out before the previous data has left the bus.

The nature of the multi-symbol interconnect forces many requirements on the bus design and topology. First and foremost, a drastic reduction in signal reflections is required. The interconnect transmission lines must be terminated at their characteristic impedance, or the signal reflections resulting from a mismatch in impedance will degrade signal quality. These reflections will reduce noise, timing margins, and the maximum operating frequency of the bus. Potentially, the reflections could create data errors.

Due to the tolerances of components such as PCBs, connectors, and termination resistors, there will be noise on the interconnect. In this multi-symbol interconnect, timings are pattern dependent due to the reflections interfering with the next transfer.

Additionally, coupled noise can greatly affect the performance of high-speed interfaces. Just as in source synchronous designs, the odd and even mode propagation velocity change creates skew between the clock and data or command lines; this reduces the maximum operating frequency of the bus. Efforts must be made to significantly decrease crosstalk, as well as the other sources of skew.

To achieve these bus requirements, the Direct RDRAM channel is designed to operate as a transmission line. All components, including the individual RDRAMs, are incorporated into the design to create a uniform bus structure that can support repeater hubs running at 800 MegaTransfers/second (MT/s).

3.5.1. Direct RDRAM Layout Guidelines

The signals on the Direct RDRAM Channel are broken into three groups: RSL signals, CMOS signals, and clocking signals.

- RSL Signals
  - DQA[8:0]
  - DQB[8:0]
  - RQ[7:0]
- CMOS Signals
  - CMD (*high-speed* CMOS signals)
  - SCK (*high-speed* CMOS signals)
  - SIO
- Clocking Signals
  - CTM
  - CTM#
  - CFM
  - CFM#

3.5.1.1. RSL Signal Routing – MEC 'Expansion' Channels and 'Stick' Channels

The 'stick' channel RSL signals from the 82803AA (MRH-R) enter the first RIMM (on either side), propagate through the RIMM, and then exit on the opposite side. The signals continue through the second RIMM until terminated at V_{TERM}. All unpopulated slots must have continuity modules in place to ensure that the signals propagate to the termination. However, the MRH-R has the added feature of allowing for its 'stick' channels to be powered-down if not in use, thus, avoiding the population of continuity modules. For example, 'stick' channel A can be populated with RIMMs and 'stick' channel B can be powered off if not used.

Refer to http://www.rambus.com/html/direct_docs.html for more information regarding the Direct RDRAM technology.

To maintain a nominal 28 Ω trace impedance, the RSL signals must be wider and is affected by whether the RSL channel is routed on inner or outer layers (asymmetrical stripline vs. microstrip).

- **Outer Layer Routing:** For outer layer (microstrip) RSL routing, an 18 mil wide trace will allow for a 28-ohm channel impedance if using the RDRAM-based MEC stack-up example defined in Figure 3. RSL trace widths of 14-15 mils can be used with the SDRAM-based MEC stack-up example defined in Figure 2. To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace routed between adjacent RSL signals. These 10 mil ground isolation traces must be connected to ground with a via every 1". A 6 mil gap is required between the RSL signals and the ground isolation trace. These signals must be length matched to ±10 mils from the MRH-R to the first RIMM and ±2 mils between the RIMMs using the trace length matching methods in Section 3.5.4. To ensure uniform trace lines, trace width variation must be uniform on all RSL signals at every neck-down for each line section.
- **Inner Layer Routing:** For inner layer (asymmetrical stripline) RSL routing, the same routing methods apply as described for outer layer routing. Figure 3 shows an RDRAM-based MEC stack-up example using 14-15 mil wide RSL traces when routing on inner layers.

All RSL signals must have the same number of vias. It may be necessary to place vias on RSL signals where they are not necessary to meet this via loading requirement (i.e. dummy vias).

Figure 4. General RSL Signal Routing Guidelines

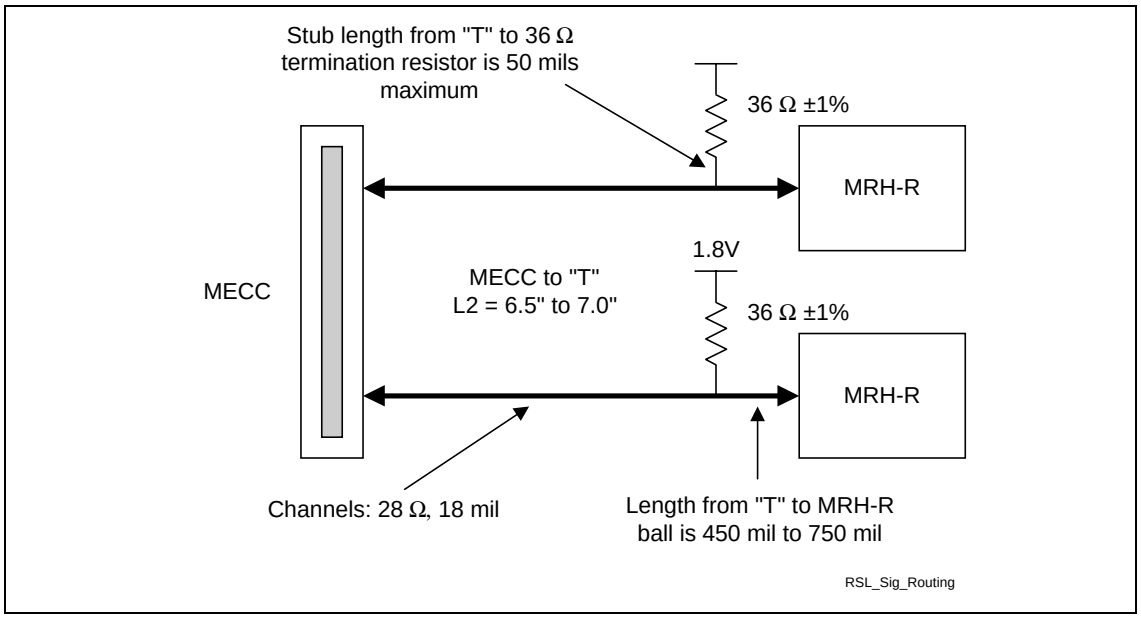


Figure 5. RSL (Outer Layer) Routing Diagram

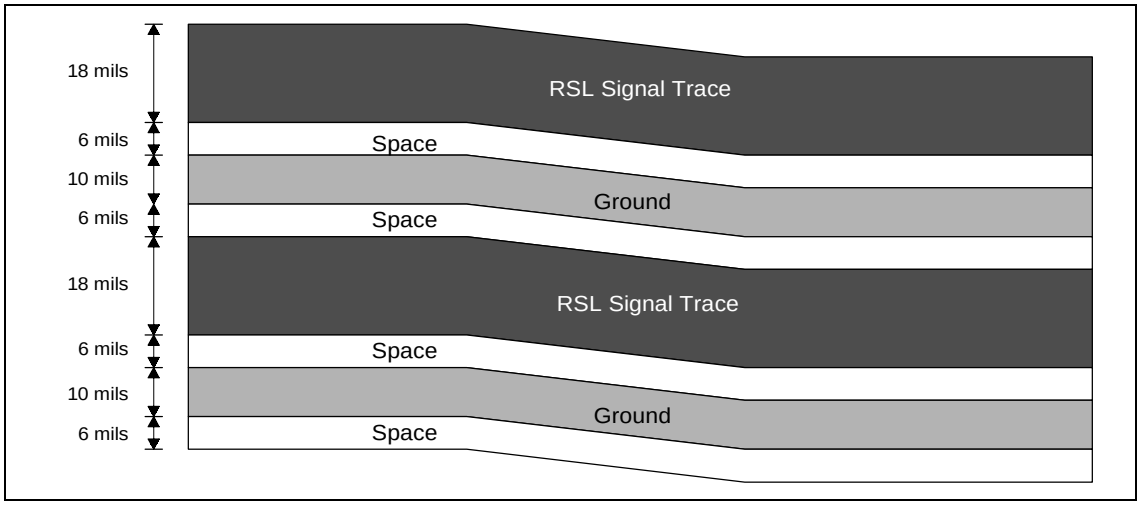


Figure 5 shows a top view of the trace width/spacing requirements for the RSL signals when routing on outer layers.

Figure 6. Example 8 RIMM/2 MRH-R MEC RSL Signal Routing

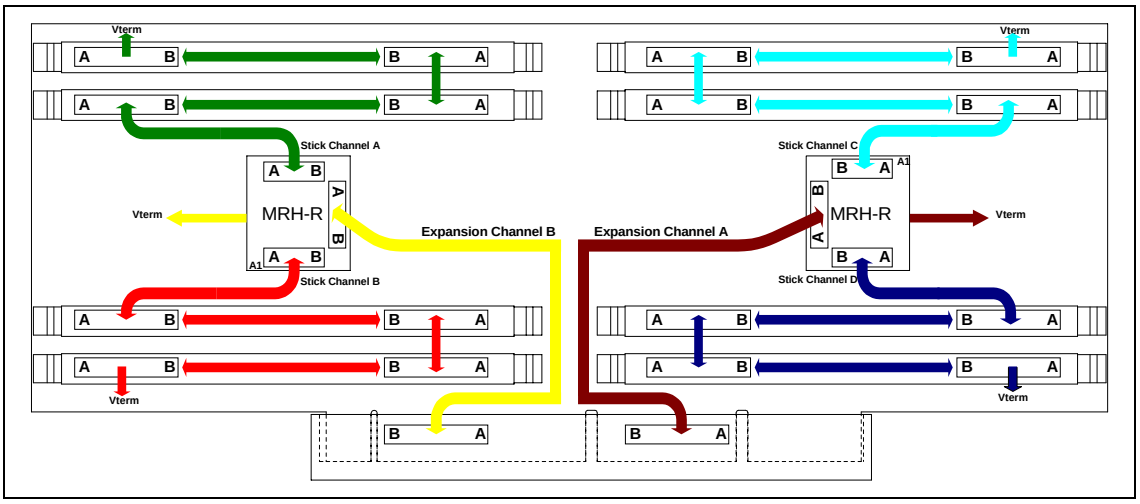


Table 2. Recommended Trace Lengths

Route	From	To	Min	Max	Notes
Expansion Channel	Card Edge Fingers	Resistor-T	6.5”	7.0”	1,2,4
Expansion Channel	Resistor - T	MRH-R	0.45”	0.75”	1,2
Expansion Channel	Resistor - T	Resistor	0.00”	0.05”	1,2
Stick Channel	MRH-R	1st RIMM	1”	6”	2,3
Stick Channel	1st RIMM	2nd RIMM	0.4”	0.45”	2,3
Stick Channel	2nd RIMM	Termination	0”	3”	2,3

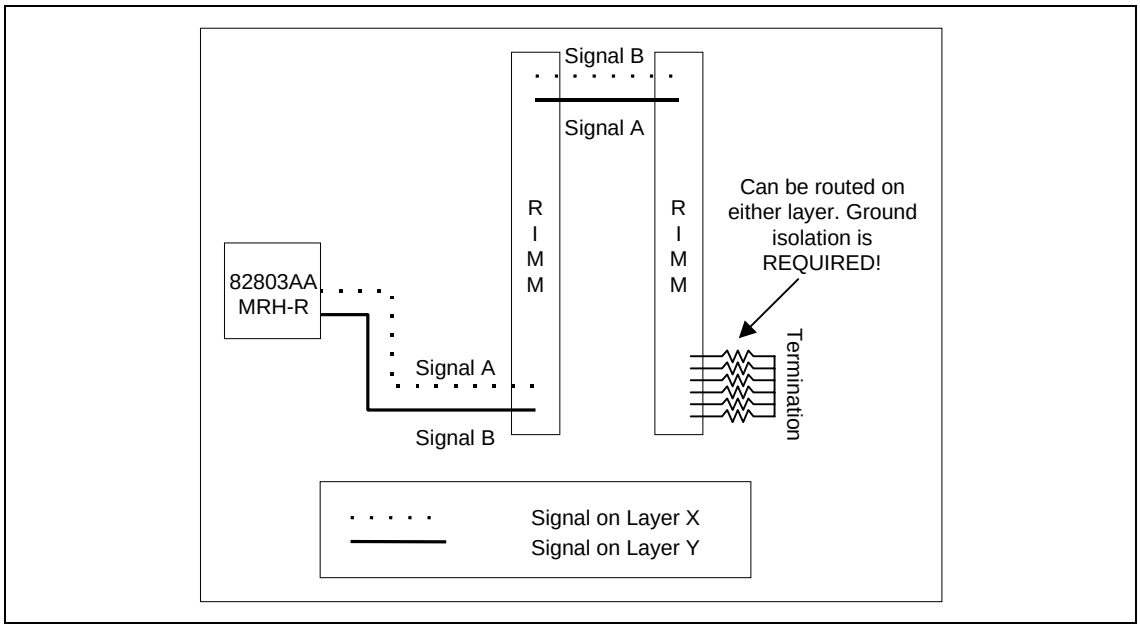
NOTES:

1. These numbers are all preliminary.
2. These numbers apply to both ‘expansion’ channels A & B.
3. These numbers apply to a 2RIMM per ‘stick’ channel implementation.
4. These lengths include the RSL length matching as described in Section 4.5.4.

3.5.2. RSL Signal Layer Alternation

All RSL signals must alternate layers as they are routed through the channel. A signal routed on a particular side from the MRH-R to the first RIMM socket must be routed on a different side from the first RIMM to the second RIMM. Signals can be routed on either layer from the last RIMM to the termination resistors.

Figure 7. RSL Signal Layer Alternation



NOTE: Signals can be routed on either layer from the last RIMM to the termination resistors.

3.5.3. RSL Termination Recommendation

All RSL signals must be terminated to 1.8V (Vterm) on the Memory Expansion Card using 27 Ω ±1% or 28 Ω ±2% resistors at the end of both the ‘expansion’ channel opposite the MCH and at the end of the ‘stick’ channels opposite the MRH-R. Resistor packs are acceptable.

Vterm must be decoupled using very high speed bypass capacitors (one 0.1 uF ceramic chip capacitor per two RSL lines) near the terminating resistors. Additionally, two 100 µF tantalum capacitors of bulk capacitance are required. The trace length between the last RIMM and the termination resistors should be less than 3”. Length matching in this section of the channel is not required. The Vterm power island should be at LEAST 50 mils wide. This voltage does not need to be supplied during a Suspend-to-RAM sleep state.

Figure 8. Direct RDRAM Termination

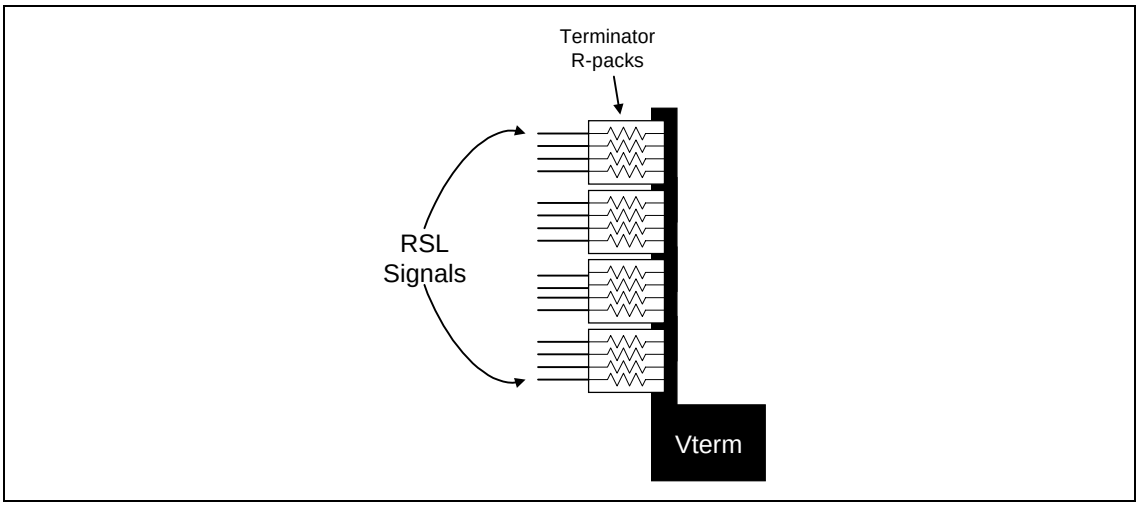
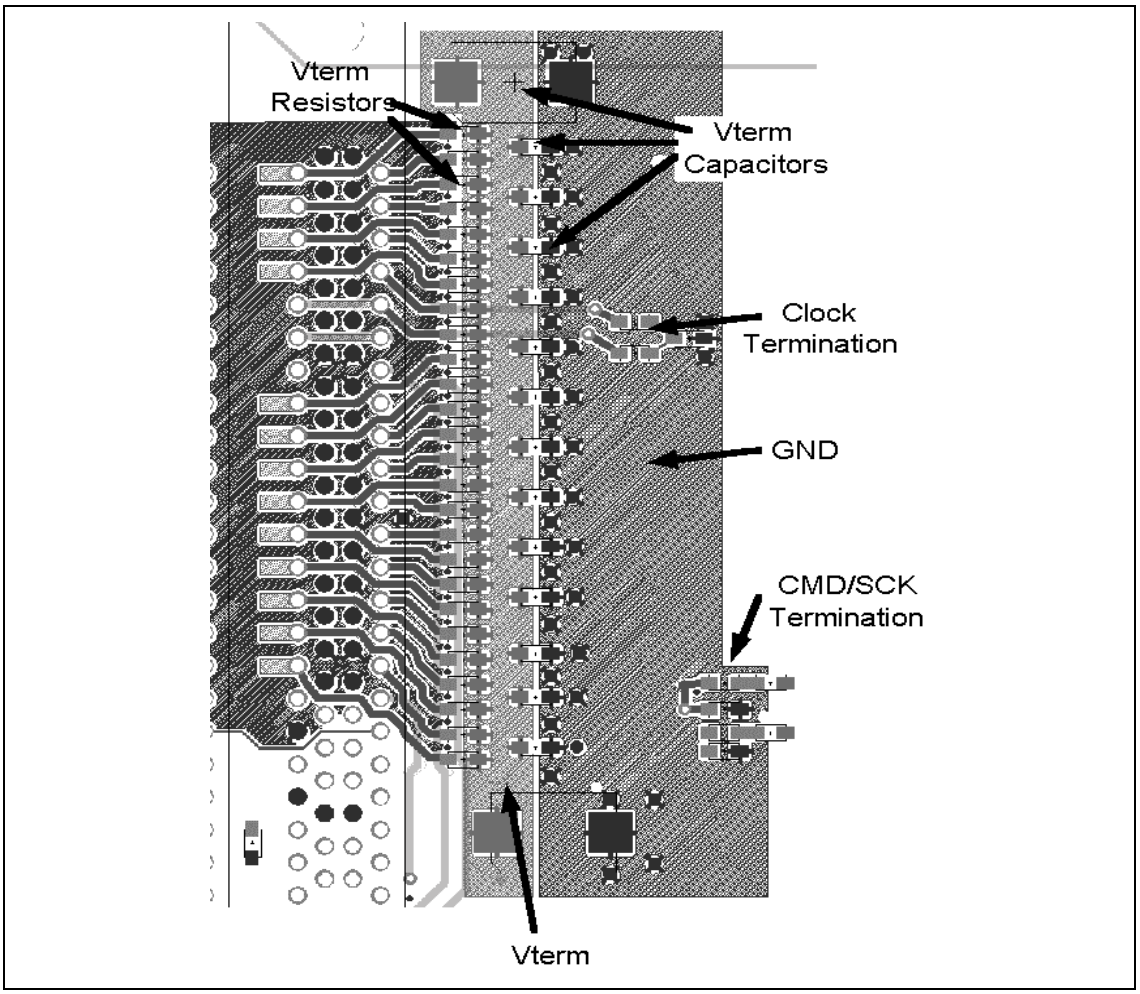


Figure 9. Direct RDRAM Termination Example



3.5.4. Length Matching Methods

For greater routing flexibility, the RSL signals require the following trace length matching methods:

- *pad-to-pad* length matching between the MCH and MRH-R
- *pad-to-pin* length matching between the MRH-R and the first RIMM connector.

If only the PCB trace lengths between the balls of the MCH and the balls of the MRH-R are matched, then the length mismatch between the pad (on the die) and the ball for each component has not been compensated. However, given the *package dimension* for each component, which is a representation of the length from the pad (on the die) to the ball, the PCB routing can compensate for this *package mismatch*.

The RSL channel requires matching trace lengths from *pad-to-pad* and *pad-to-pin* to within ±10 mils.

Given the following definitions:

- **Package Dimension (ΔL_{PKG}):** a representation of the length from the pad to the ball.
- **Board Trace Length (L_{MB}):** the trace length on the board.
- **Nominal RSL Length:** the length to which all signals are matched. (Note: there is not necessarily a trace that is EXACTLY to nominal length, but all RSL signals must be matched to within ±10 mils of a nominal length). The *Nominal RSL Length* is an arbitrary length (within the limits of the routing guidelines) to which all the RSL signals will be matched (within ±10 mils).

Figure 10. RDRAM Trace Length Matching Example From MRH-R to RIMM

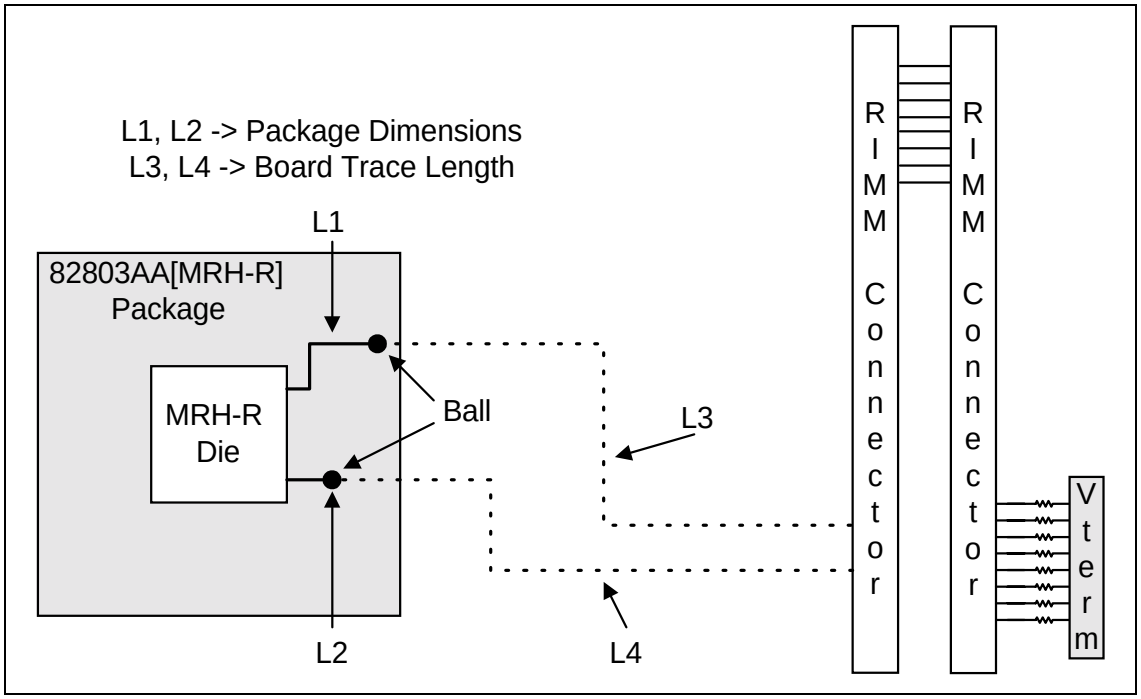
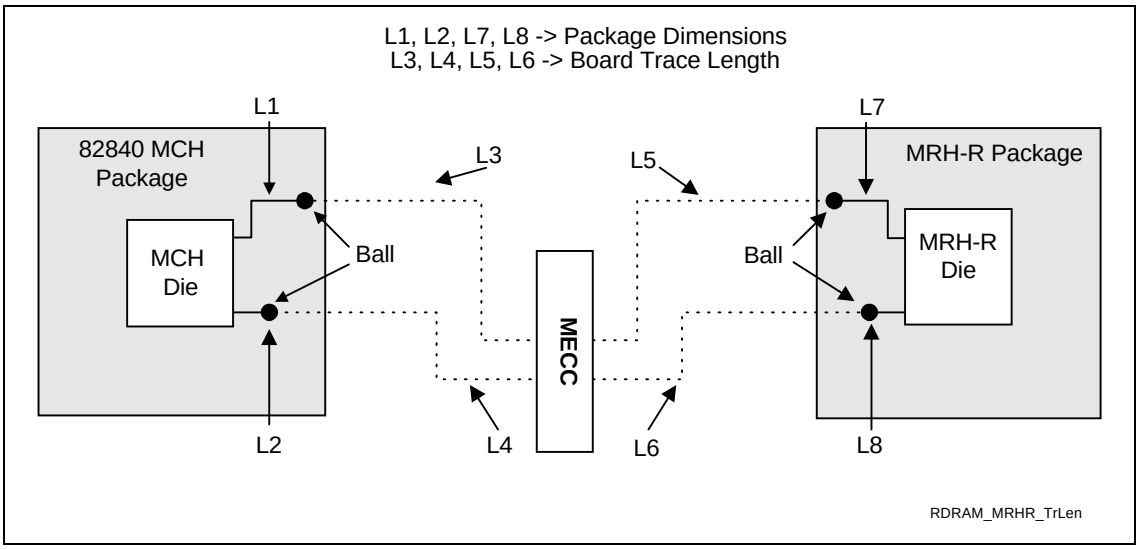


Figure 11. RDRAM Trace Length Matching Example From MCH to MRH-R



RSL Signals Length Match Requirement

For 'stick' channel RSL length compensation on a Memory Expansion Card, L1 and L3 must be length matched to L2 and L4 within ±10 mils. See Figure 10.

For 'expansion' channel RSL length matching on a Memory Expansion Card, L7 and L5 must be length matched to L8 and L6 on the MEC within ±10 mils. See Figure 11.

Compensated Trace Length Calculation

$$\Delta L_{PCB} = (\Delta L_{PKG} * \text{Package}_{\text{TRACE VELOCITY}}) / PCB_{\text{TRACE VELOCITY}}$$

The PCB trace length for each signal is a calculated value, and may vary with designs. The actual package trace velocity is between 177 ps/in and 183 ps/in. The nominal trace velocity of 180 ps/in can be used when calculating the compensated PCB trace length. The $PCB_{\text{TRACE VELOCITY}}$ is board dependent.

Refer to the appropriate Intel® 840 chipset datasheet for specific package information. **NOTE:** The ballout document provides signal lengths **NORMALIZED TO THE LONGEST** RSL trace length in each package. They do not represent the actual lengths from pad to ball. By normalizing to the longest length, you can reduce PCB trace lengths. Additional RSL length matching on the MEC is recommended, with the 82803AA (MRH-R). Package information for these components is also included in the datasheet.

The RSL signal lengths (ΔL_{PKG}) can be normalized to either the shortest or longest RSL trace using the equation below:

Equation 1. Normalized Trace Length Calculation

$$\text{New } \Delta L_{PKG} = \text{Old } \Delta L_{PKG} - \Delta L_{RSL}$$

Outer Layer Routing

The RDRAM clocks (CHx_CTM, CHx_CTM#, CHx_CFM and CHx_CFM#) must be longer than the RDRAM signals due to their increased trace velocity (because they are differential and routed as a pair) when routed on outer layers. To calculate the length for each clock, the following formula should be used:

Clock Length = Nominal RSL Signal Length (package + motherboard + card) * 1.021

Using this formula, the clock signals will be 21mils/inch longer than the Nominal Length. The lengthening of the clock signals, to compensate for their trace velocity change, ONLY applies to the routing of RSL signals on outer layers.

Inner Layer Routing

The clock signals should matched in length to the RSL signals when routing on inner layers. Refer to the clock section for more detailed Direct RDRAM clock routing guidelines.

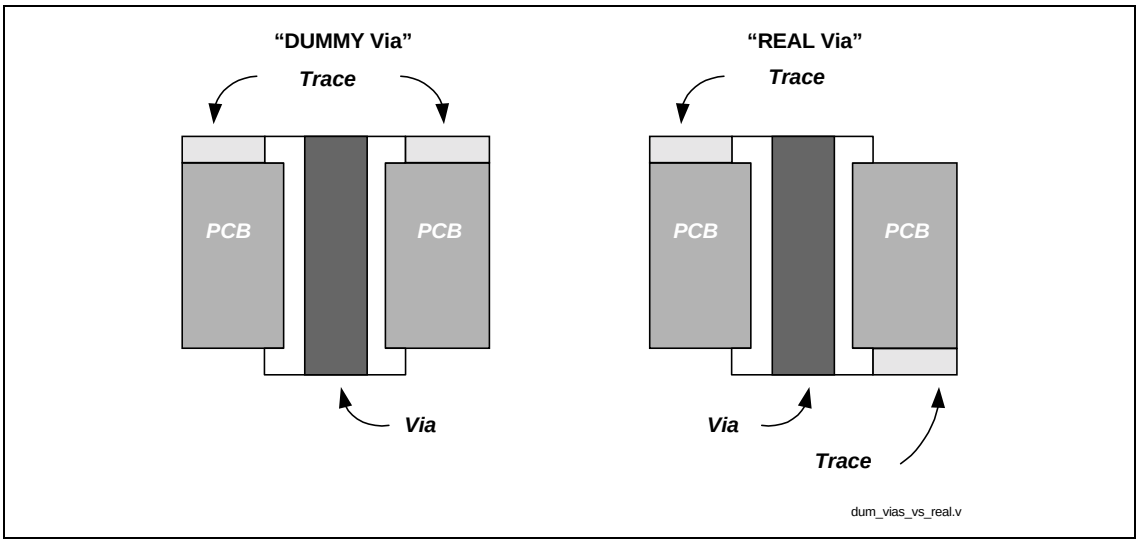
3.5.5. VIA Compensation

As described in Section 3.5.1.1, all RSL signals must have the same number of vias As a result, each trace will have 1 via (near the BGA pad) because some of the RSL signals must be routed on either top, bottom, or inner. It will be necessary to place “dummy” via on all signals that are routed on the top or bottom layers. The electrical characteristics between “dummy” and “real” vias are not exact, so additional compensation is needed on each signal that has “dummy” vias.

Each signal with dummy via must have 25 mils of additional trace length. The additional 25 mils trace length must be added to the signal, routed on the top layer, after length matching. *Real via = Dummy via + 25 mils of trace length.*

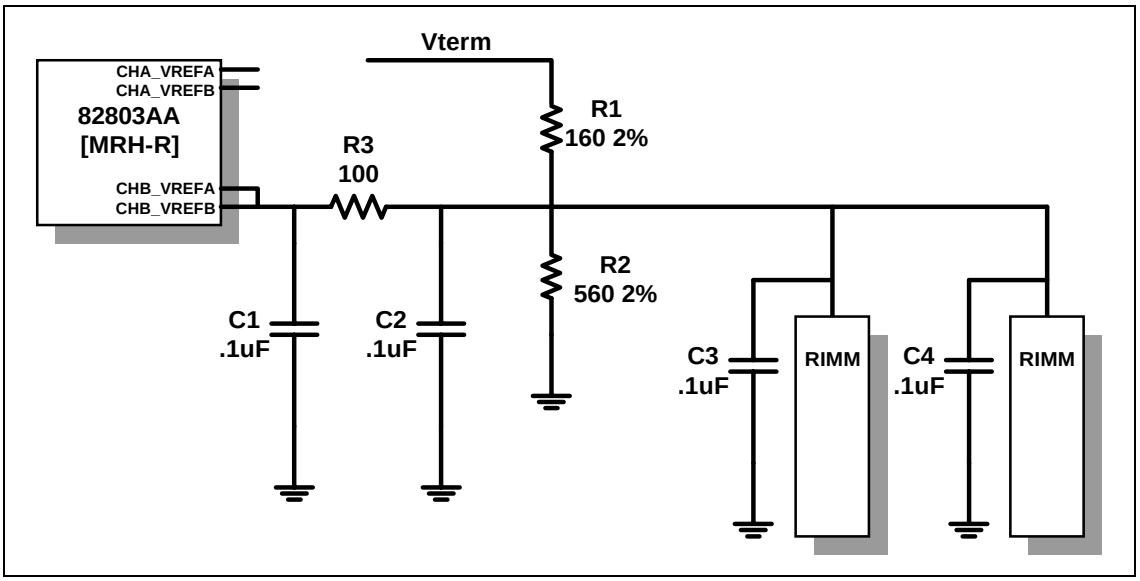
It is important to compensate for the electrical difference between “real” and “dummy” vias.

Figure 12. 'Dummy' via vs. 'Real' via



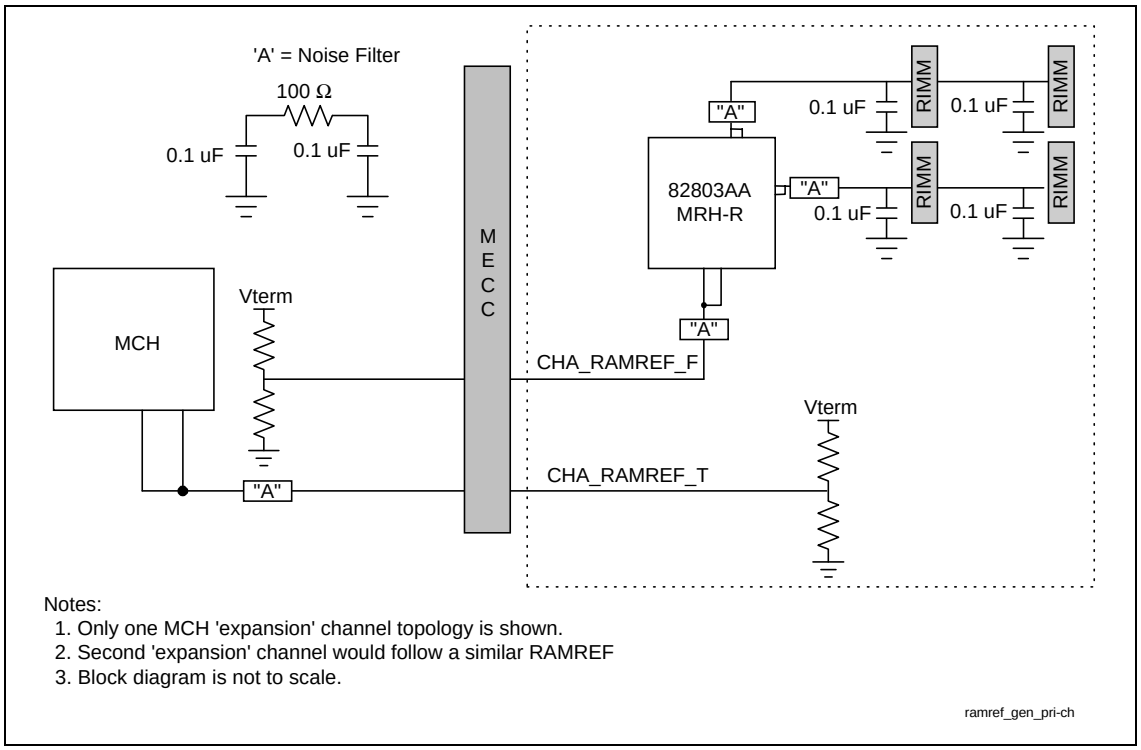
3.5.6. Direct RDRAM Reference Voltage

Figure 13. Secondary RDRAM Channel RAMREF Generation



The Direct RDRAM reference voltage (RAMREF), must be generated on all 'stick' channels as shown in Figure 13. RAMREF should be generated from a resistor divider network using 2% tolerant resistors and the values shown. It is also recommended that a separate RAMREF resistor divider network for each MRH-R stick channel be implemented. Additionally, RAMREF should be routed with a 6 mil trace and must be properly decoupled. Finally, as shown in Figure 13, a noise filter network composed of a 100 Ω series resistor with two 0.1 uF caps is recommended near the CHx_VREF/EXVREF/RAMREF pins on the memory repeater hubs and near the CHx_REF pins on MCH.

Figure 14. Primary RDRAM Channel RAMREF Generation



The generation of RAMREF on ‘expansion’ channels is different. To account for potential differences between RAMREF and GND on the motherboard and on the memory expansion cards, it is recommend using *source generated RAMREF* for the expansion channels.

That is, the RAMREF signal is generated at the memory repeater hubs on the MEC and *sent* down the memory expansion card connector to the MCH, and a separate RAMREF is generated on the motherboard at the MCH and *sent* up the memory expansion card connector to the repeater hubs (the signal names are EXVREFx for MRH-Rs where x-denotes the channel). (refer to Figure 14)

There are four pins defined on the MEC connector pinout example to allow for this RAMREF *passing*. These pins are:

CHx_RAMREF_TM	- RAMREF from the MEC to the chipset
CHx_RAMREF_FM	- RAMREF from the chipset to the MEC

**x-denotes expansion channel A&B

The voltage divider networks consists of DC elements as shown in Figure 13.

The RAMREF divider network should be placed as close to the *memory repeater hubs* as is practical to get the benefit of the common mode power supply effects. However, the trace spacing around the RAMREF signals must be a minimum of 25 mils to reduce crosstalk and maintain signal integrity. In addition the RAMREF signals should be routed with 6-8 mil wide traces.

3.5.7. High-speed CMOS Routing

Due to the synchronous requirements between the RSL signals and the high-speed CMOS signals, these signals should be routed as part of the RSL channel. They must be impedance matched and properly terminated (using a *different* termination scheme than the RSL signals – See Figure 15.

It is not necessary to perform the length matching calculation for the high-speed CMOS signals as described in section 3.5.4. For routing on the motherboard, the mismatch between the CMOS signals (CMD and SCK) and the RSL signals should be kept to within 1200 mils (1.2 in) due to a timing requirement between CMOS and RSL signals during NAP Exit and PDN Exit. Route the CMOS signals PCB trace length equal to the nominal RSL PCB trace length.

The high-speed CMOS signals should be routed in their respective positions in the channel. The only line section that does not have strict PCB length matching requirements is the section from the last RIMM to the termination resistors.

Figure 15. High-speed CMOS Termination on MRH-R Stick Channels

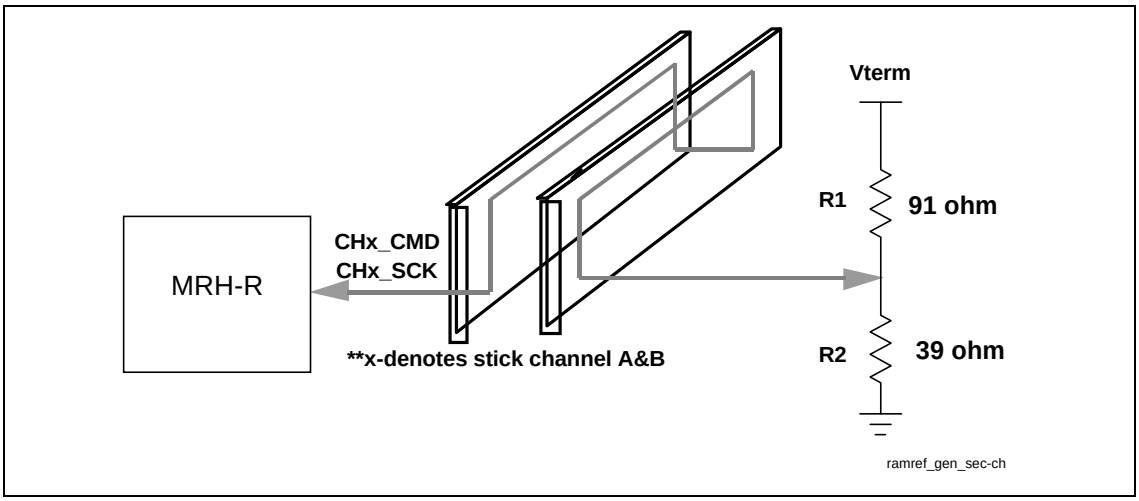
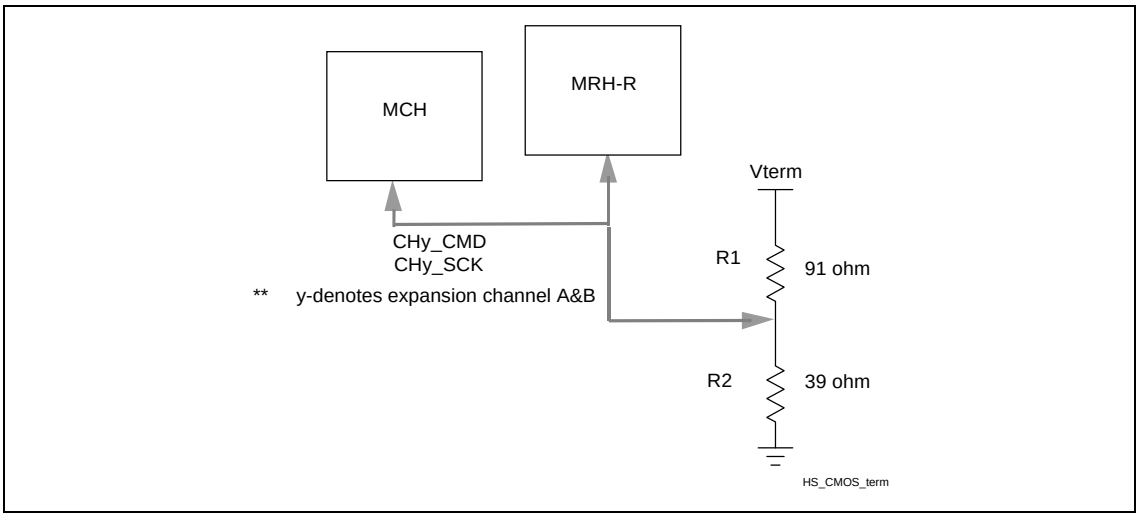


Figure 16. High-speed CMOS Termination from MCH to MRH-R



A CMOS voltage must be supplied to each RIMM. This CMOS voltage is used by the RDRAMs CMOS interface. This voltage (Vcmos) must be 1.8V and the maximum load is 3mA. Additionally, this voltage must be supplied during *Suspend-to-RAM*. Therefore, Vterm and Vcmos cannot be generated from the same source (i.e., they can not be the same power plane). Due to the low power requirements of Vcmos, it can be generated by a 36 Ω / 100 Ω resistor divider from 2.5V.

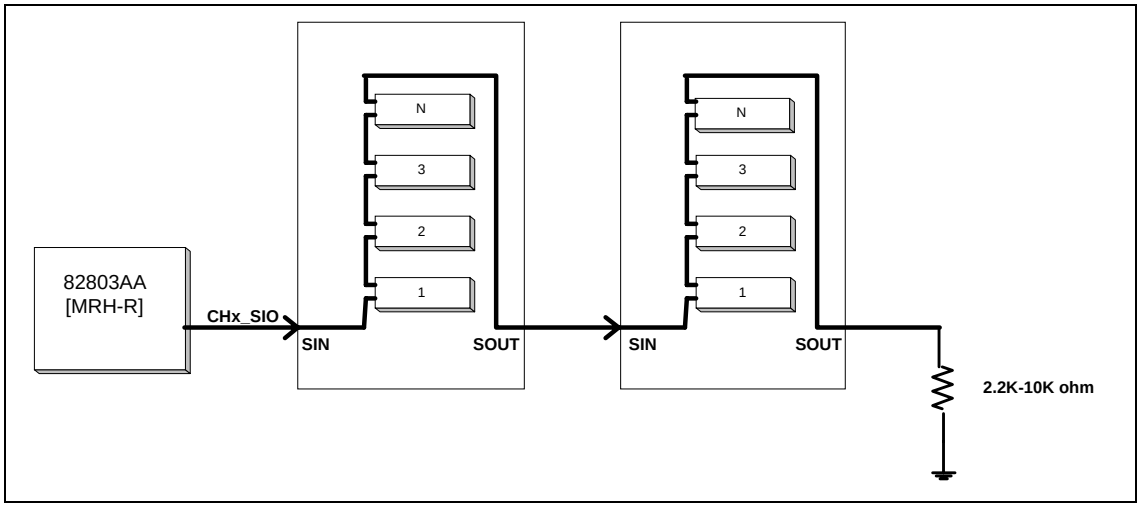
3.5.7.1. SIO Routing

The SIO signal is a bi-directional signal that operates at 1 MHz. The SIO signal enters the first RIMM, propagates through all the devices (this signal is buffered by each device) on the RIMM, and then exits the RIMM. The signal continues through the rest of the existing RIMMs and is terminated.

A pull-down through a 2.2KΩ-10KΩ resistor must be placed on the end of the SIO signal as shown in Figure 17.

The SIO signal is routed with a 5 mil wide 60 ohm trace with no need for ground isolation. Route from CHx_SIO (MRH-R) to SIN (RIMM #1 – Pin B36), from SOUT (RIMM #1 – Pin A36) to SIN (RIMM# 2 – Pin B36), and from SOUT (RIMM #2 – Pin A36) to termination.

Figure 17. SIO Routing Example



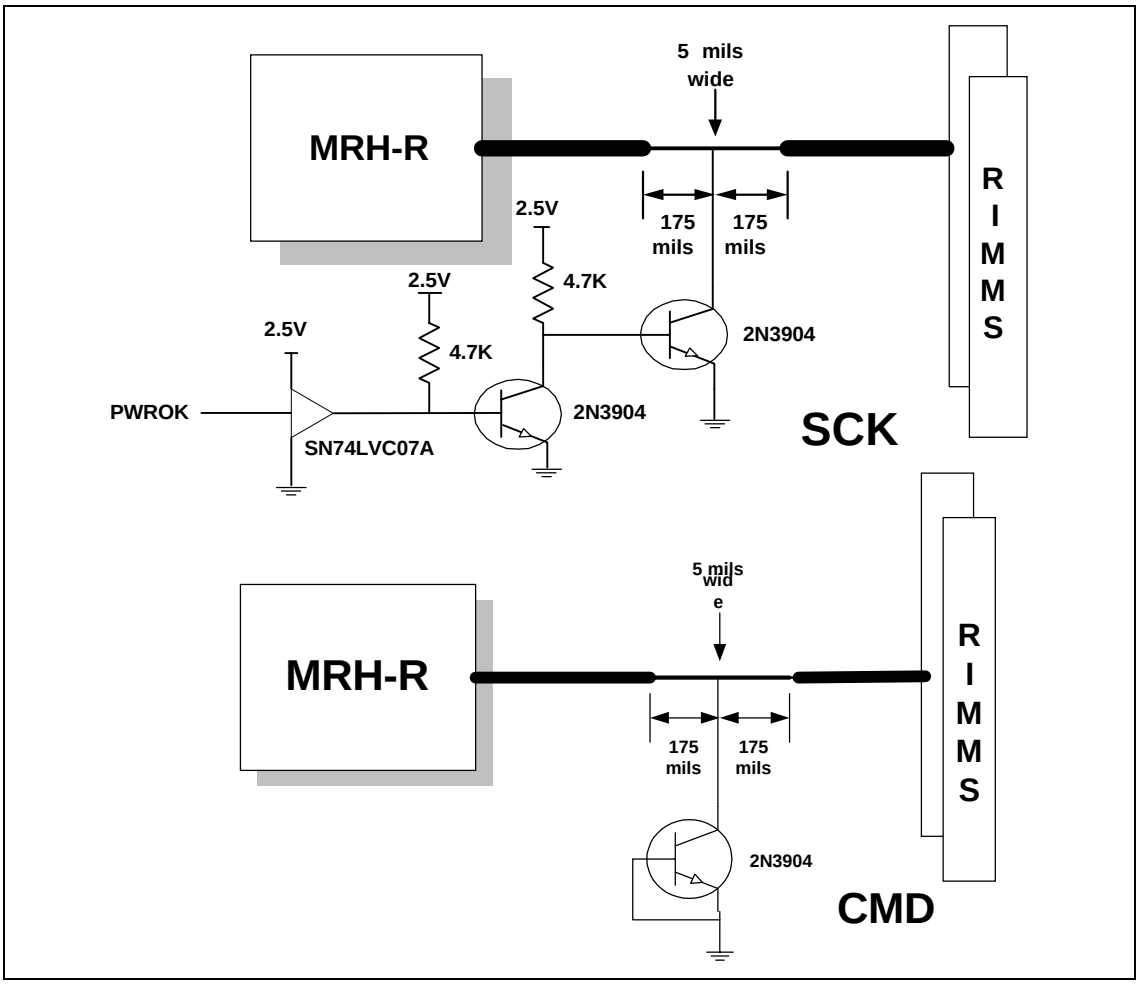
3.5.7.2. Suspend-to-RAM Shunt Transistor

When the Intel® 840 chipset-based systems enter or exit *Suspend-to-RAM*, power will be ramping to both the MCH and MRH-R (i.e., they will be powering-up or powering-down). When power is ramping, the state of the their CMOS outputs is not guaranteed. Therefore, the MCH could drive the CMOS signals through the MRH-R and issue some CMOS commands. One of the commands (the only one the RDRAMs would respond to) is the powerdown exit command. To avoid the MCH inadvertently taking the RDRAMs out of power-down due to the CMOS interface being driven during power ramp, the SCK (CMOS clock) signal must be shunted to ground when the MCH and MRH-R are entering and exiting *Suspend-to-RAM*. This shunting can be accomplished by placing the NPN transistor between the MRH-Rs and RIMMs as shown in Figure 25. The transistor should have a C_{obo} of 4 pF or less (i.e., MMBT3904LT1).

In addition, to match the electrical characteristics on the SCK signals, the CMD signals need a *dummy* transistor placed between the MRH-R and RIMMs. This transistor's base should be tied to ground (i.e., always turned off).

To minimize impedance discontinuities, the traces for the CMD and SCK signals should have a neckdown from the routed trace widths down to 5 mil traces for 175 mils on either side of the SCK/CMD attach points as shown in Figure 25.

Figure 18. RDRAM CMOS Shunt Transistor

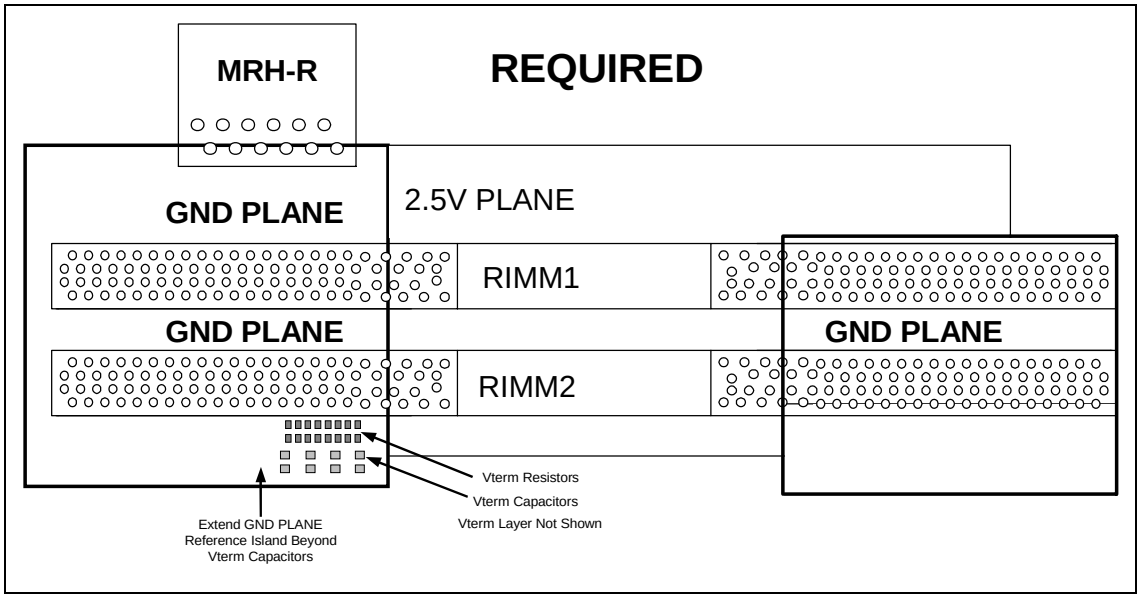


3.5.8. Direct RDRAM Ground Plane Reference

All RSL signals must be referenced to GND to provide an optimal current return path. The ground reference must be continuous from MRH-R to the RIMM connectors. This may require a GND reference island on the plane layers closest to the RSL signals. Choose the reference island shape such that power delivery to components is not compromised.

By referencing all RSL signals to ground, the optimized current return paths will improve system operation.

Figure 19. MEC with Ground Reference for RSL Signals



- The ground reference island under the RSL signals MUST be connected to the ground pins on the RIMM connector and the ground vias used to connect the ground isolation on the outer layers.
- The direct RDRAM ground plane reference must be continuous to the Vterm capacitors.
- The ground reference island under the RSL signals must be continuous from the last RIMM to the back of the termination capacitors. The return current will flow through the Vterm capacitors into the ground island and under the RSL traces. Any split in the ground island will provide a sub-optimal return path.

3.5.9. Direct RDRAM Connector Compensation

The RIMM connector inductance causes an impedance discontinuity on the Direct RDRAM channel. This may reduce voltage and timing margin.

Note: The examples in this section are specific to the Intel® 820 chipset. The Intel® 840 chipset only supports 2 RIMMs per Direct RDRAM channel.

In order to compensate for the inductance of the connector, approximately 0.65 pF–0.85 pF compensating capacitive tab (C-TAB) is required on each RSL connector pin. This compensating capacitance must be added to the following connector pins at each connector:

- LCTM
- LCTM#
- RCTM
- RCTM#
- LCFM
- LCFM#
- RCFM
- RCFM#
- LROW[2:0]
- RROW[2:0]
- LCOL[4:0]
- RCOL[4:0]
- RDQA[8:0]
- LDQA[8:0]
- RDQB[8:0]
- LDQB[8:0]
- SCK
- CMD

This can be achieved on the motherboard by adding a copper tab to the specified RSL pins at each connector. The target value is approximately 0.65 pF–0.85 pF. The copper tab area for the recommended stackup was determined through simulation. The placement of the copper tabs can be on any signal layer, independent of the layer on which the RSL signal is routed.

Equation 2 is an approximation that can be used for calculating copper tab area on an outer layer.

Equation 2: Approximate Copper Tab Area Calculation

$$Length*Width = Area = C_{plate} * Thickness\ of\ prepreg\ /\ [(\varepsilon_0)\ (\varepsilon_r)\ (1.1)]$$

- $\varepsilon_0 = 2.25 \times 10^{-16}$ Farads/mil
- ε_r = Relative dielectric constant of prepreg material
- Thickness of prepreg = Stackup dependent
- Length, Width = Dimensions in mils of copper plate to be added
- Factor of 1.1 accounts for fringe capacitance.

Different stackups require different copper tab areas. The table below shows example copper tab areas.

Table 3. Copper Tab Area Calculation

Dielectric Thickness (D)	Separation Between Signal Trace & Copper Tab	Minimum Ground flood	Air Gap between Signal & GND Flood	Compensating Capacitance in pF	Copper Tab (C-TAB) Area (A) In sq mils	C-TAB Shape (mils)
4.5	6	10	6	0.65	2800	140 L x 20 W 70 L x 40 W

Based on Equation 2, the tab area is 2800 sq mils, where ε_r is 4.2 and D is 4.5. These values are based on 2116 prepreg material.

The tab dimensions are based on copper area over the ground plane. The actual length and width of the tabs may be different due to routing constraints (e.g., if tab must extend to center of hole, or antipad); however, each copper tab should have equivalent area. For example, the copper tabs in Figure 21 have the following dimensions, when measured tangent to the antipad:

Inner C-TAB = 140 (length) x 20 (width)

Outer C-TAB = 70 (length) x 40 (width)

The following figures show a routing example of tab compensation capacitors. Note that the capacitor tabs must not interrupt ground floods around the RIMM pins, and they must be connected to avoid discontinuity in the ground plane as shown. The following figures are examples from the Intel® 820 Chipset Platform and consequently display two RIMMs.

Figure 20. Connector Compensation Example

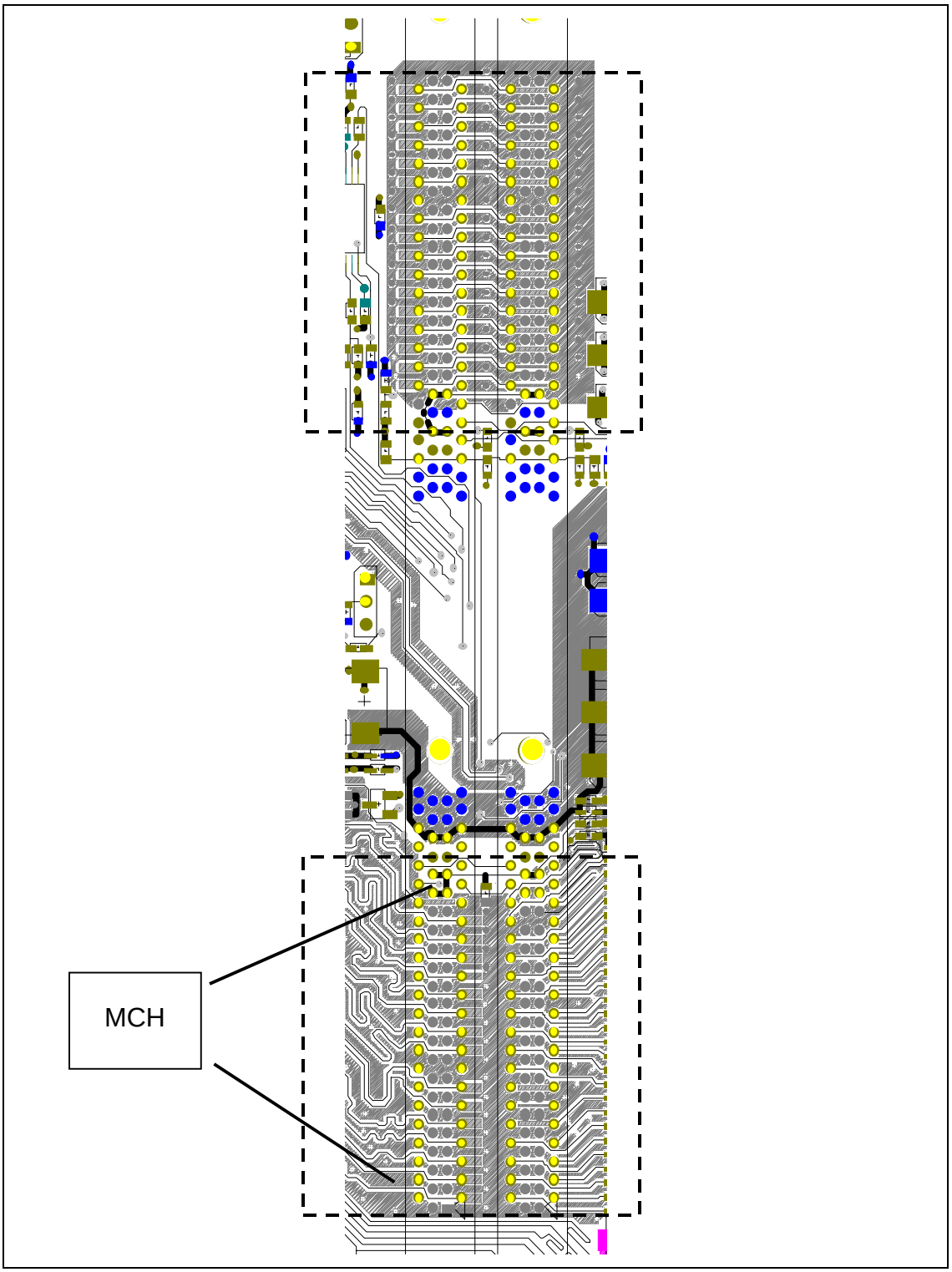
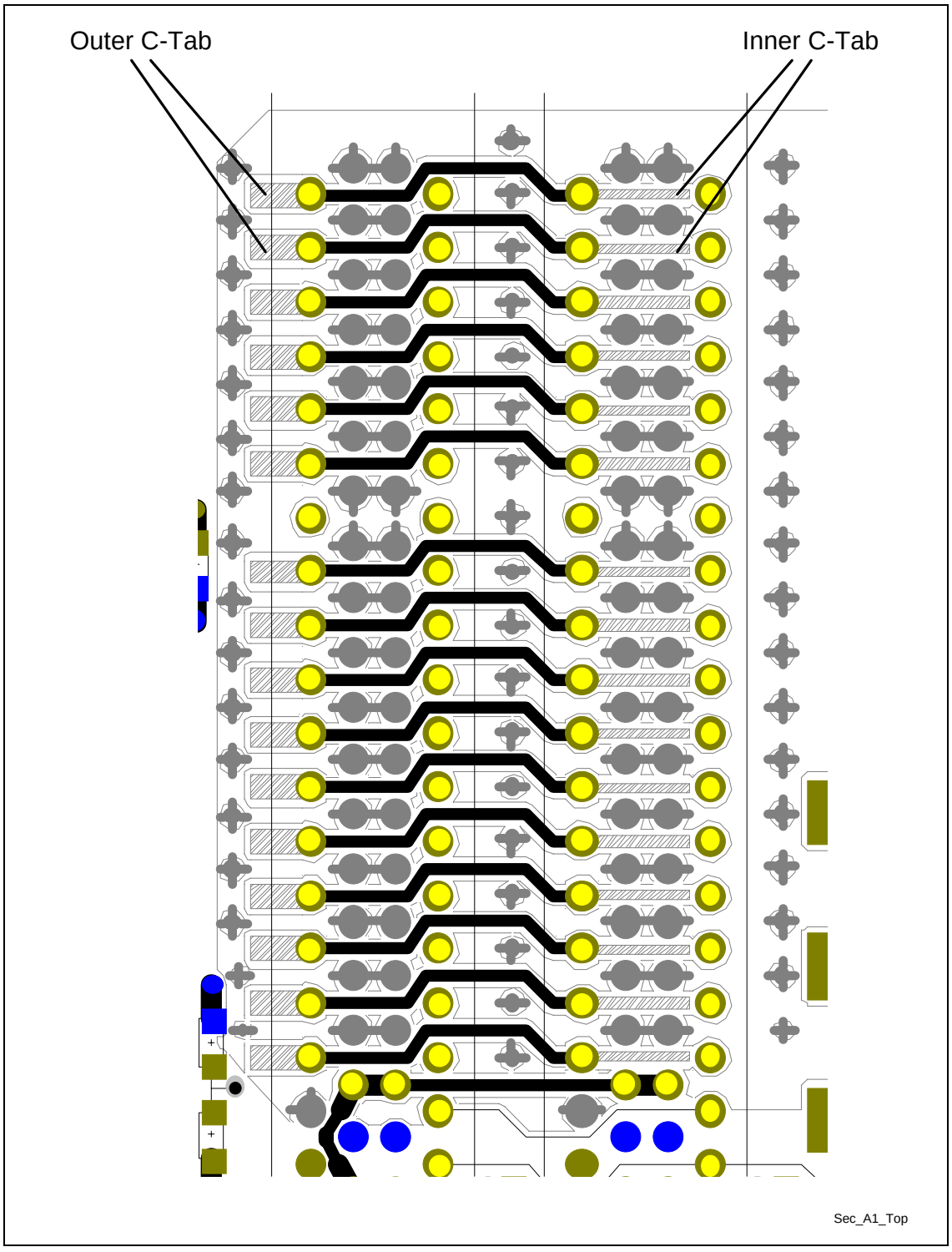
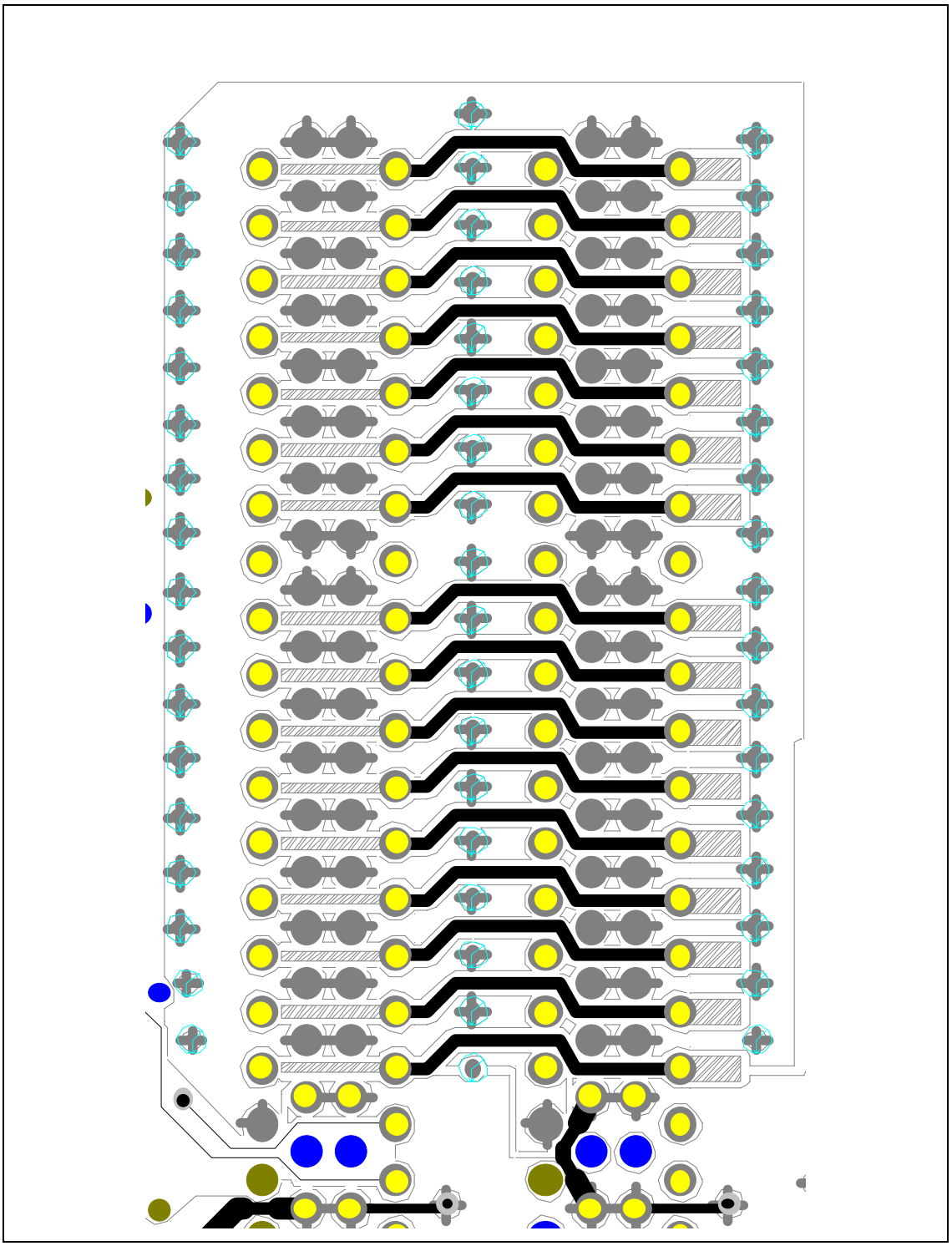


Figure 21. Section A[1], Top Layer



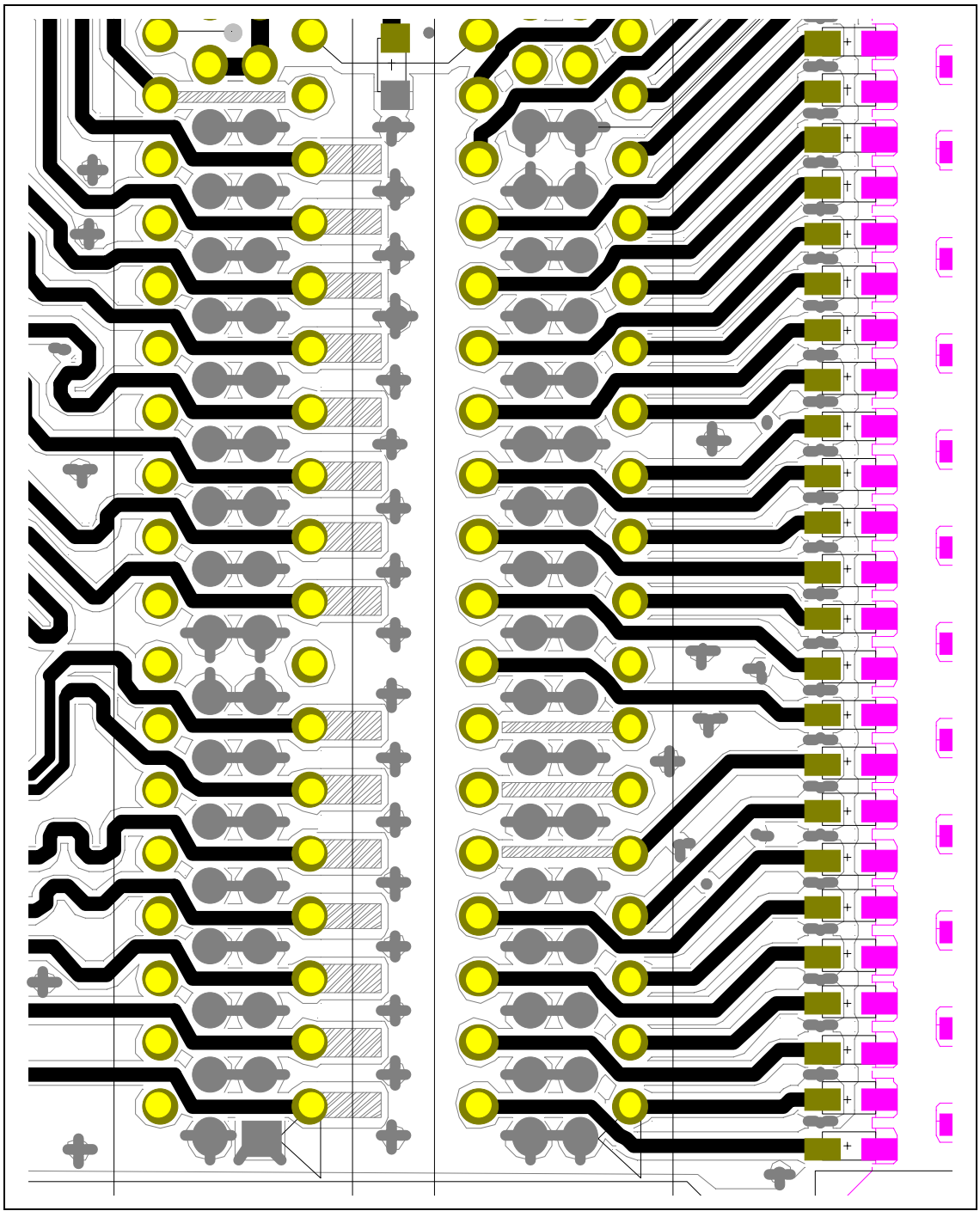
[1] Refer to Figure 29. Ground flood removed from picture for clarity.

Figure 22. Section A[1], Bottom Layer



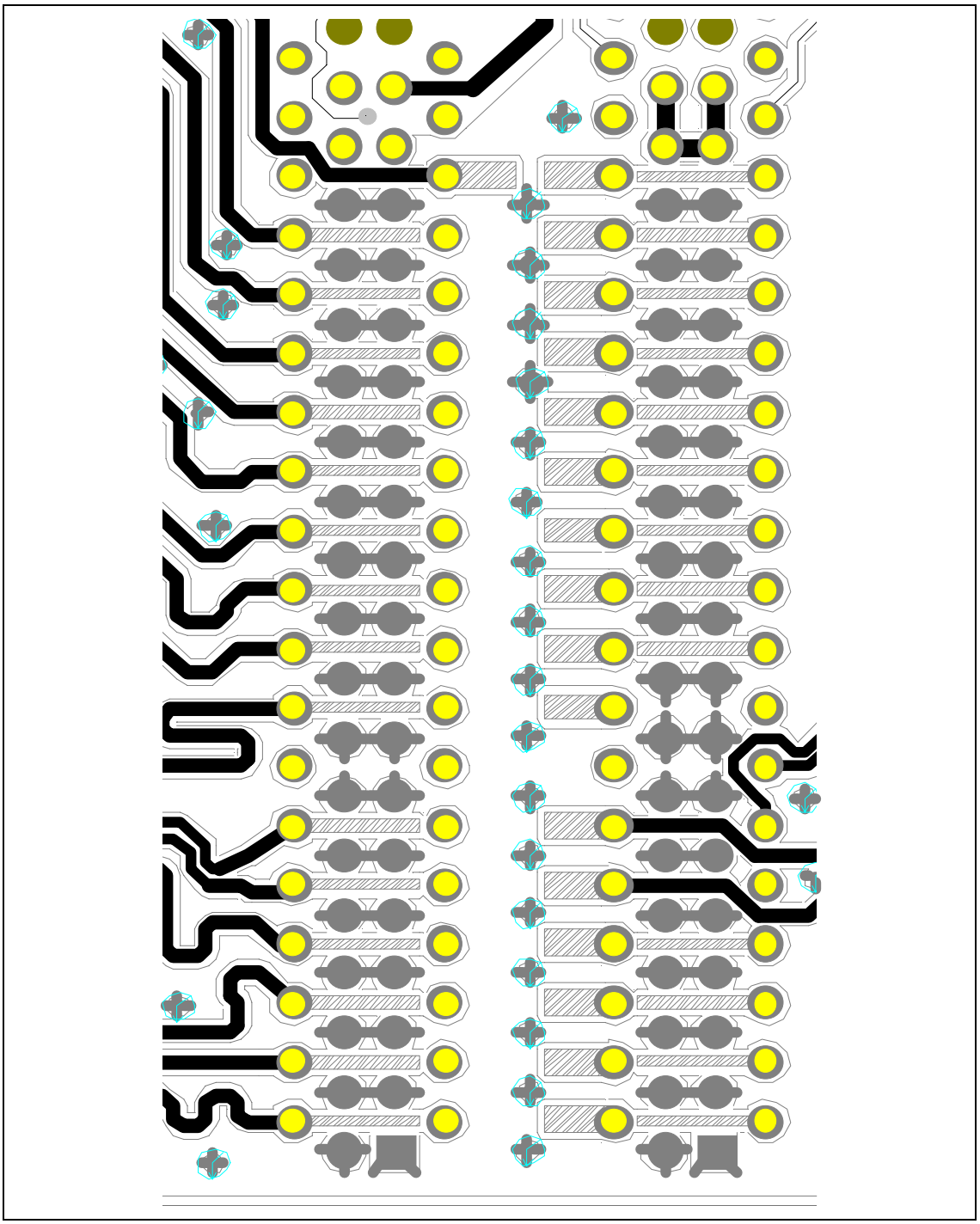
[1] Refer to Figure 29. Ground flood removed from picture for clarity.

Figure 23. Section B[1], Top Layer



[1] Refer to Figure 29. Ground flood removed from picture for clarity.

Figure 24. Section B[1], Bottom Layer



[1] Refer to Figure 29. Ground flood removed from picture for clarity.

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4. MEC Clock Topologies

4.1. RDRAM Clock Routing Guidelines

The following figure shows a conceptual overview of the RDRAM-based Memory Expansion Card clock topologies.

Figure 25. RDRAM-based MEC Clock Topology

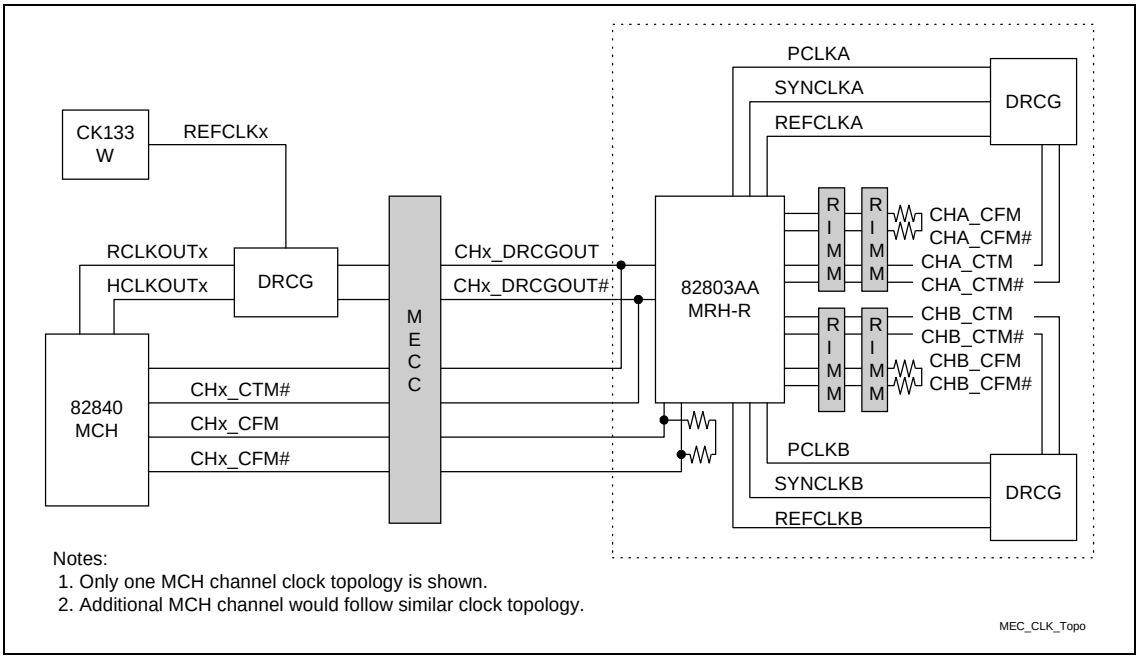
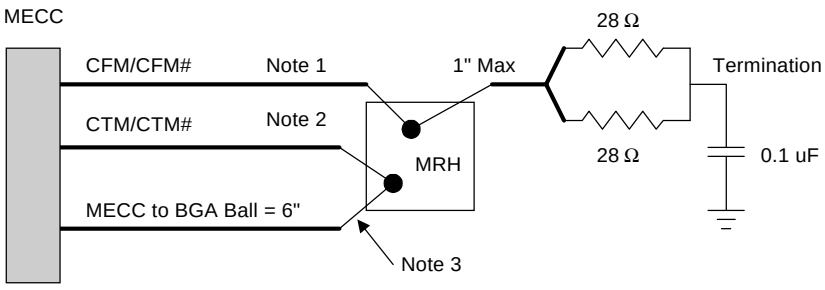


Figure 26. Additional RDRAM Clock Routing Guidelines



Equation 3: CFM/CFM# Trace Length Calculation

CFM_Length = (RSL_Channel_Nominal_Length + CFM_Package_Compensation_Length) * 1.021

CFM#_Length = CFM_Length

Equation 4: CTM/CTM# Trace Length Calculation

CTM_Length = (RSL_Channel_Nominal_Length + 0.5" +
CTM_Package_Compensation_Length) * 1.021

CTM#_Length = CTM_Length

Notes:

1. In both the equations above the variable “RSL_Channel_Nominal_Length” corresponds to “L2” in Figure 4.
2. Each set of differential clocks must be matched to within ± 2mils.
3. Add 21mils of trace to the differential clock routing per 1000 mils of RSL signal trace.
4. 48 Ω, 350 mils MAX neck-down for package Z_O compensation.
5. Refer to Section 4.5.4 for more information on CFM_Package_Compensation_Length and CTM_Package_Compensation_Length.

4.1.1. MRH-R to DRCG

VddIR and REFCLKx routing Example

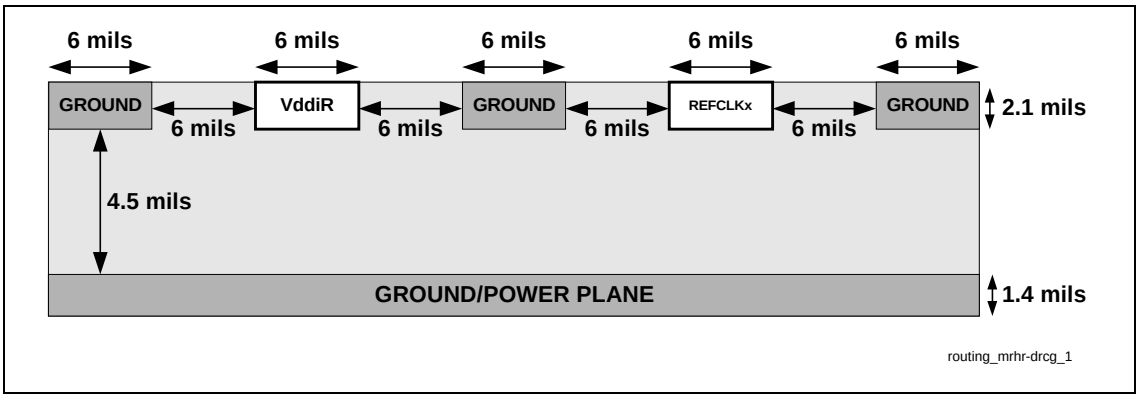
- REFCLKA, REFCLKB
- VddIR – Used as a reference for 1.8V signaling

An example of VddIR and REFCLKx routing is shown in the following figure.

Note: If a 1.8V plane can be placed near the DRCG, then the VddIR pin should be connected directly to the 1.8V plane. However, it may be difficult to place a 1.8V power plane near the DRCG. If necessary, a 1.8V trace (VddIR) should be routed from the 1.8V plane near the MRH-R to the DRCG and routed as shown in the figure below. VddIR should be decoupled with a 0.1 uF, 0603, ceramic chip capacitor.

The maximum routing length for REFCLKx is 8”.

Figure 27. MRH-R to DRCG Routing Example 1



VddIPD, PCLKM and SYNCLKN Routing Example

- PCLKMA, PCLKMB
- SYNCLKNA, SYNCLKNB
- VddIPD – Used as a reference for 1.8V signaling

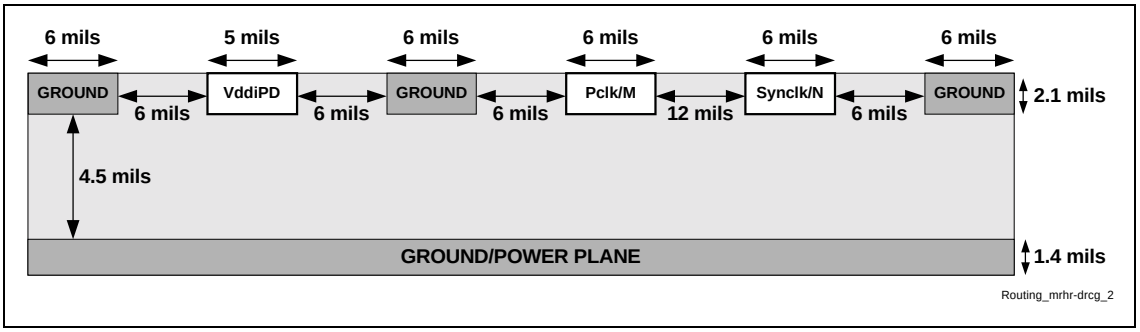
An example of VddIPD, PCLKM and SYNCLKN routing is shown in the following figure.

Note: If a 1.8V power plane can be placed near the DRCG, then the VddIPD pin should be connected directly to the 1.8V plane. However, it may be difficult to place a 1.8V power plane near the DRCG. If necessary, a 1.8V trace (VddIPD) should be routed from the 1.8V plane near the MRH-R to the DRCG and routed as shown in the figure below. VddIPD should be decoupled with a 0.1 uF, 0603, ceramic chip capacitor. If VddiPD is connected to the 1.8V plane using a via (e.g., a trace is not run from the clock syntesizer), PCLK/M and SYNCLK/N (HCLKOUT and RCLKOUT) must still be routed differentially and ground isolated.

This group of signals needs to be routed on the same routing layer. If these signals need to be on different signal planes to escape the MRH-R, they must via back to the same layers after escaping the BGA package. If these signals must have vias, the via counts for these signals must be matched. Further, these signals should be run on the signal layer adjacent to the ground layer (refer to section 0).

The maximum routing length for PCLKMx and SYNCLKNx is 6”. Additionally, PCLKMx and SYNCLKNx must be length matched (to each other) within 50 mils.

Figure 28 . MRH-R to DRCG Routing Example 2



4.1.2. DRCG to RDRAM Channel

The Direct RDRAM clock signals (CHx_CTM/CTM# and CHx_CFM/CFM# on both the expansion and stick channels) are high-speed, impedance matched transmission lines. The Direct RDRAM clocks begin at the end of the Direct RDRAM channel and propagate to the MRH-R end as CHx_CTM/CTM# (see figure below), where it loops back as CHx_CFM/CFM# (see figure below) to the RDRAMs and terminates at the end of the channel. If any signals are routed on the top or bottom layers of the board from the 2nd RIMM to the termination, then the ground reference island must extend to the ground side of the termination capacitors.

Figure 29 . Direct RDRAM Clock Routing Recommendations

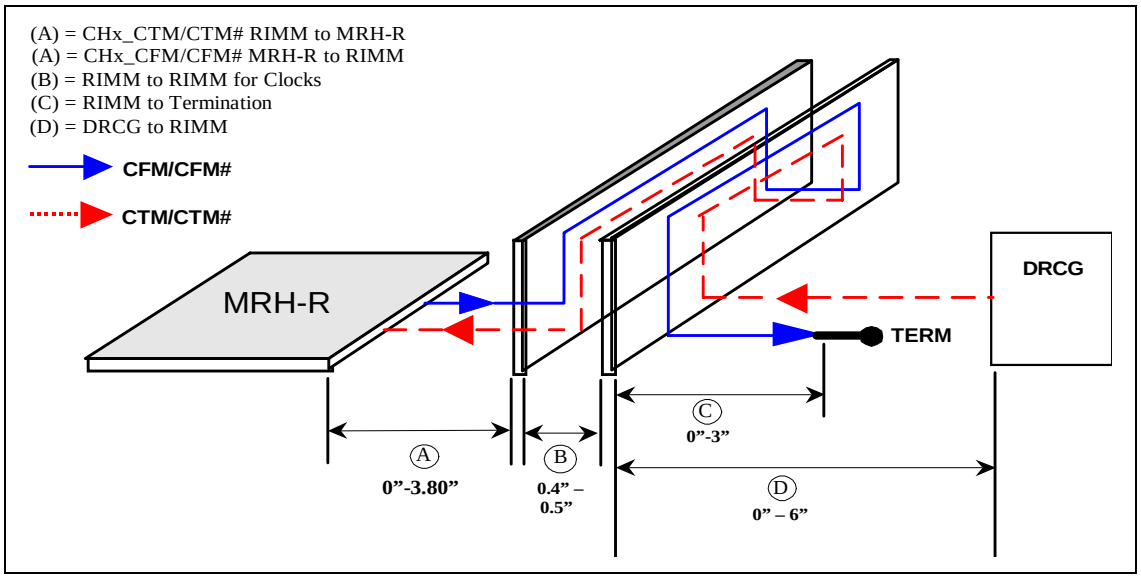


Table 4. Direct RDRAM Clock Routing Length Guidelines (Recommended Trace Lengths)

Clock	From	To	Length (inches)	Section[2]
CHx_CTM/ CHx_CTM#	DRCG	2nd RIMM Connector	0.000 – 6.000	D
	RIMM	RIMM	0.400 - 0.500	B
	1st RIMM Connector	MRH-R	0.000 – 3.800	A
CHx_CFM/ CHx_CFM#	MRH-R	1st RIMM Connector	0.000 - 3.800	A
	RIMM	RIMM	0.400 - 0.500	B
	2nd RIMM Connector	Termination	0.000 - 3.000	C

NOTES: Notes:
1. These are preliminary numbers.
2. Stick channel A&B.

Trace Geometry

In Sections labeled ‘A’ and ‘D’ in Figure 29 , the clock signals (CHx_CTM/CTM# and CHx_CFM/CFM#) are routed differentially as shown in Figure 30. Sections ‘A’ and ‘D’ in the differential routing example are 14 mils wide to meet the 28-ohm channel impedance with the stack-up shown. There must be a ground isolation trace routed around the differential clock pair (22 mils wide as shown in the example in Figure 30). The ground isolation traces must be connected to ground with a via every 1”. A 6 mil gap is required between the clock signals (NOTE: this gap should be exactly 6 mil – not greater, not less). When these clocks are routed on outer layers, 0.021 inches of CLK trace per 1 inch of RSL trace length must be added to compensate for the clocks faster trace velocity on outer (stripline) layers.

For section ‘B’ and ‘C’, the clock signals are routed non-differentially as shown in . The clock signals in this section, as shown in the routing example, must be routed with 18 mil wide traces to meet the 28-ohm channel impedance. In addition, a ground isolation trace and a 6 mil gap between the ground isolation traces and the clock signals (same routing as RSL signals) is recommended. The ground isolation traces must also be connected to ground with a via every 1”.

Trace Length

For the section labeled “A” in Figure 29 (1st RIMM to 82803AA (MRH-R) and 82803AA (MRH-R) to 1st RIMM), CHx_CTM/CTM# and CHx_CFM/CFM# must be length matched within ±2 mils (exact trace length matching is recommended).

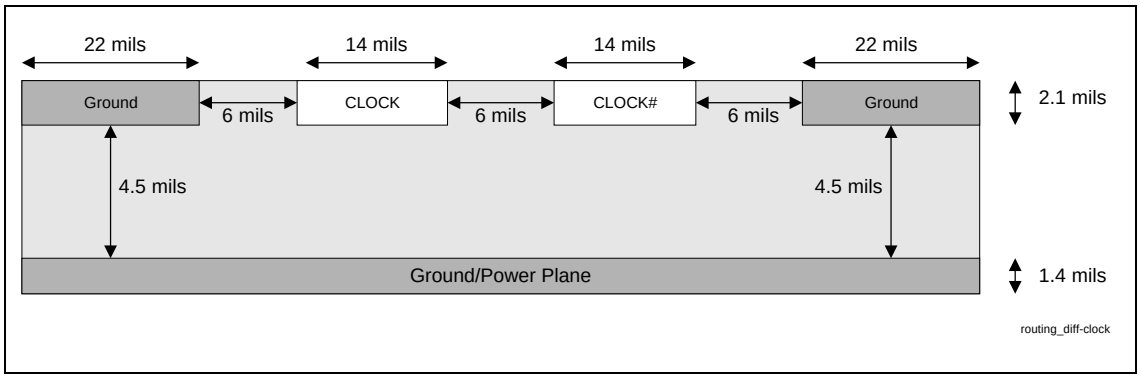
Package trace compensation (as described in section 3.5.1.1), *via compensation* (as described in section 3.5.5) and *RSL signal layer alternation* (also described in section **Error! Reference source not found.**) must also be completed on the clock signals. Additionally, 0.021 inches of CLK per 1 inch of RSL trace length must be added to compensate for the clocks faster trace velocity as described in section 3.5.4.

For the line sections labeled ‘B’ in Figure 29 (RIMM to RIMM), the clock signals must be matched within ±2 mils to the trace length of every RSL signal. Exact length matching is preferred.

For the line section labeled ‘D’ (DRCG to 2nd RIMM) the CHx_CTM/CTM# must be length matched within ±2 mils (exactly is recommended), **and for the section labeled ‘C’, ± 2 mil trace length matching is required for the CHx_CFM/CFM# signals.**

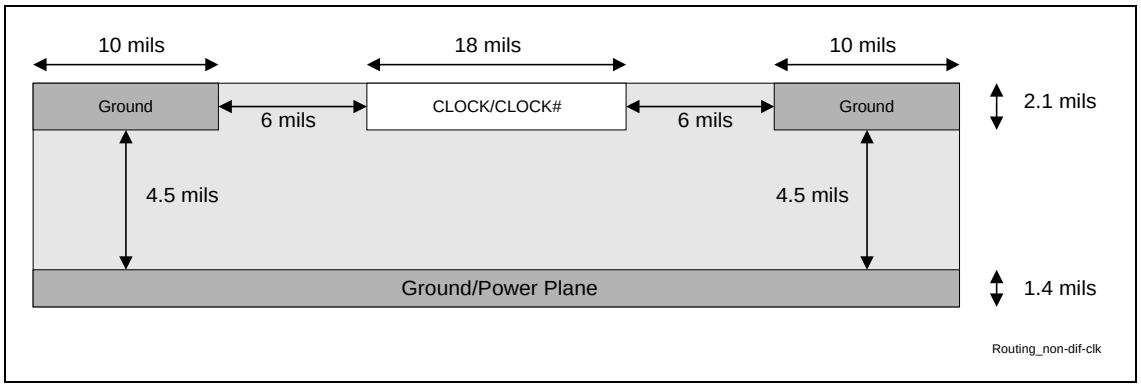
Note that the total trace length matching for the entire CHx_CTM/CTM# signal traces (Sections A+B+D) and for the CHx_CFM/CFM# signal traces (Sections A+B) is ±2 mils (exact length matching is recommended).

Figure 30. Differential Clock Routing Diagram



Note: "CLOCK" stands for the signals CTM and CFM and "CLOCK#" stands for the signals CTM# and CFM#.

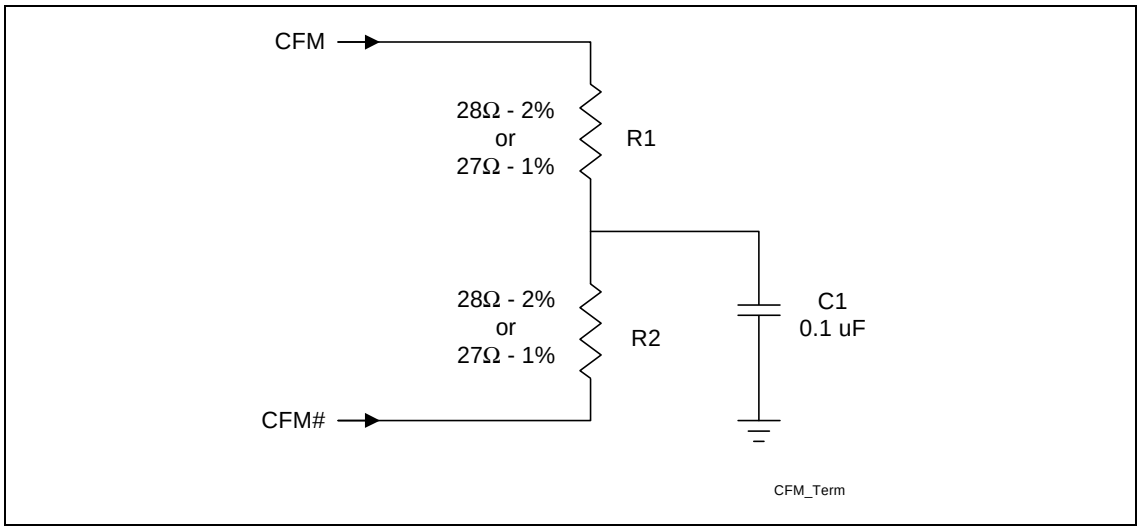
Figure 31. Non-Differential Clock Routing Diagram



Note: "CLOCK" stands for the signals CTM, CTM#, CFM and CFM#.

The CHx_CFM/CFM# differential pair signals require termination using either 27Ω ±1% ??the 1% matches figure below?? or 28Ω ±2% resistors and a 0.1 uF capacitor as shown in the figure below.

Figure 32 . Termination for Direct RDRAM Clocking Signals CHx_CFM/CFM#



4.1.3. DRCG Impedance Matching Circuit

The external DRCG impedance matching circuit is shown in Figure 33

Figure 33 . DRCG Impedance Matching Network

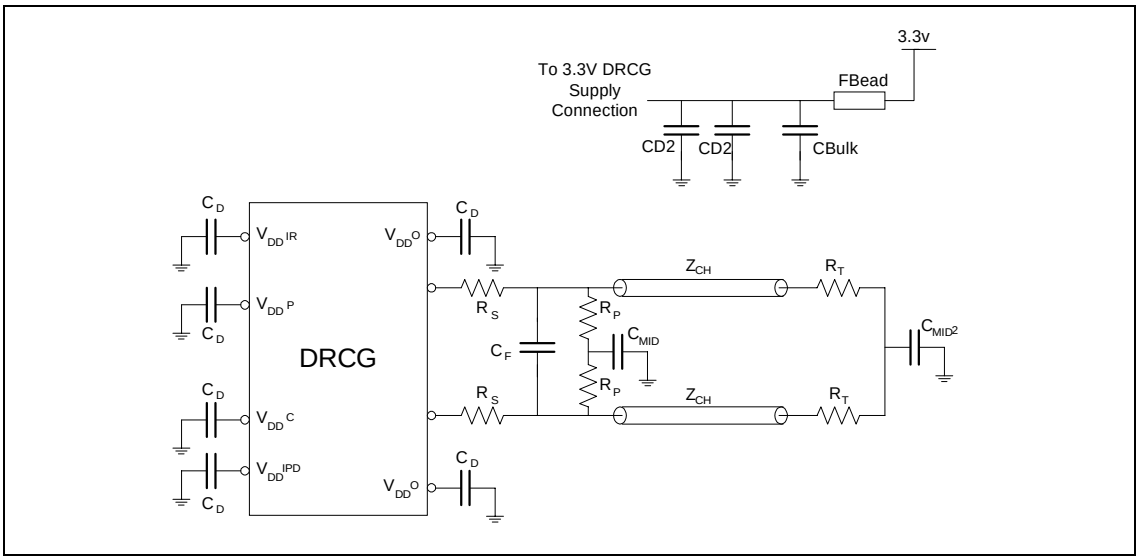


Table 5. DRCG Impedance Matching Network Values

Component	Nominal Value	Notes
C_D	0.1 uF	Decoupling caps to GND
R_S	39 Ohms	Series termination resistor
R_P	51 Ohms	Parallel termination resistor
C_{MID1}, C_{MID2}	0.1 uF	Virtual GND caps
R_T	27 Ohms	End of channel termination
C_F	4-15 pF	Do Not Stuff, leave pads for future use
FBead	50 Ohms @ 100 MHz	Ferrite bead
CD2	0.1 uF	Additional 3.3V decoupling caps
CBulk	10 uF	Bulk cap on device side of ferrite bead

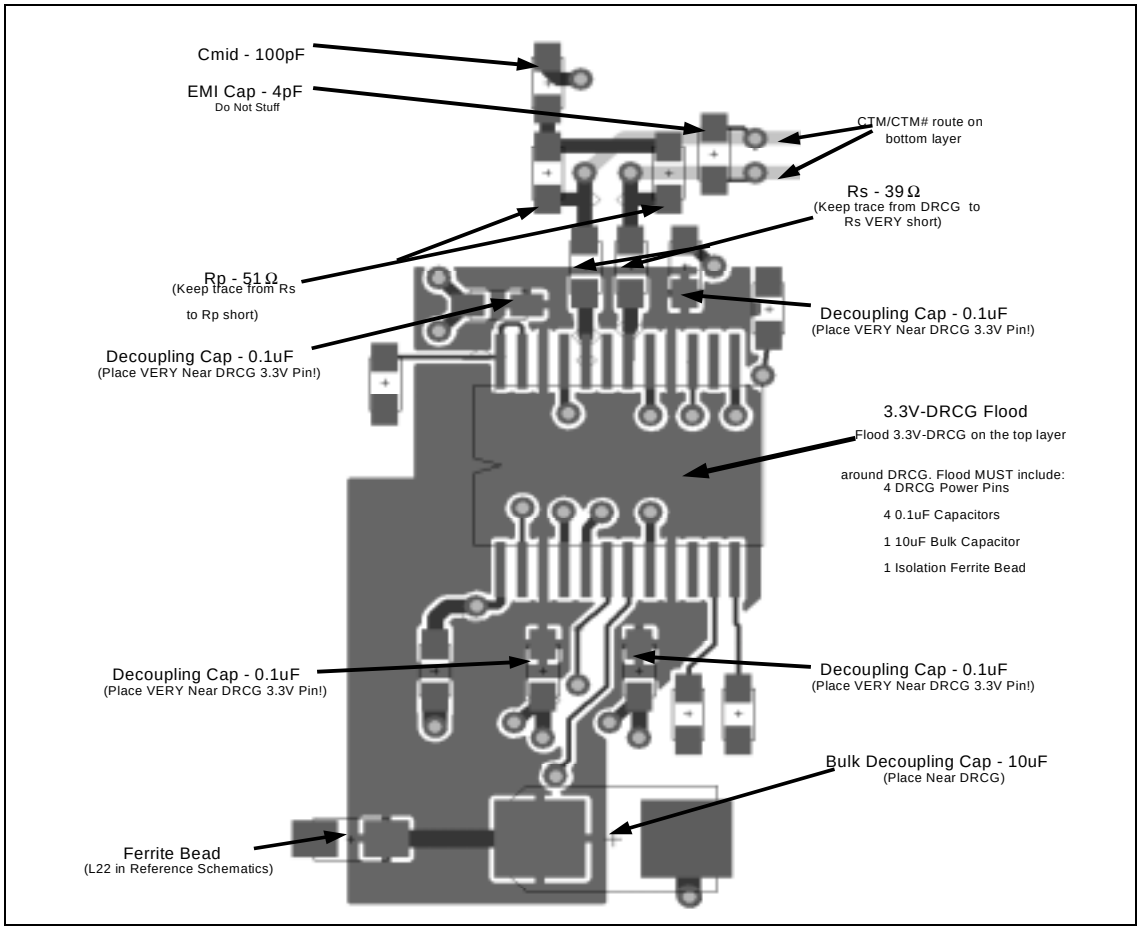
NOTES: (Notes are for above table and Figure 33)

1. Note the removal of the original EMI capacitors between the junctions of R_S, R_P and ground. These capacitors had minimal impact on EMI and increased DRCG output jitter by approximately 2X.
2. The intent of component C_F is to decouple CLK, but early data shows this actually increases device jitter. C_F should not be stuffed at this time.
3. The ferrite bead and 10 µF bulk cap combination improves jitter and helps to keep the clock noise away from the rest of the system. The additional 3.3V capacitors (CD2) have a minor positive impact, but the ideal values have not been extensively optimized. There is a possibility that one or both CD2 caps can be removed in future board revisions.

4. 0.1 µF capacitors are better than 0.01 µF or 0.001 µF caps for DRCG decoupling. Most decoupling experiments that replaced 0.1 µF caps with higher frequency caps ended up with the same or worse jitter. Replacing the existing 0.1 µF caps with higher frequency caps is not advised.
5. C_{mid} at 0.1 µF has improved jitter versus C_{mid} at 100 pF. However, this will increase the latency coming out of a stop clock or tri-state mode.
6. R_S, R_P, R_T were modified to improve channel signal integrity through increasing CTM/CTM# swing.
7. The circuit shown is required to match the impedance of the DRCG to the 28 Ω channel impedance. More detailed information can be found in the Direct RDRAM Clock Generator Specification.
8. The previously recommended 15 pF capacitors on CTM/CTM# should be removed. The 4 pF capacitor shown in the figure should not be assembled ("no-stuff").

4.1.4. DRCG Layout

Figure 34 . DRCG Layout Example



4.2. DRCG+ and DRCG Frequency Selection

To allow additional flexibility in board design, Intel has enabled a variation of the DRCG labeled the *DRCG+*. The device has the same specifications, pinout and form-factor as the existing DRCG device document at www.rambus.com.

The DRCG+ and DRCG Mult[0:1] select table is shown in Table 6. The Mult[0:1] pins can be hardwired for a multiple ratio of 6:1. This is made possible because the reference clock supplied by the MRH-Rs has already undergone a static 1:6 division ratio, making the net ratio 1:1. Support for 300 MHz and 400 MHz memory bus is unchanged.

Table 6. Mult[0:1] Ratio Selection

Mult[0:1]	DRCG	DRCG+
0:0	4:1	9:2
0:1	6:1	6:1
1:0	8:3	16:3
1:1	8:1	8:1

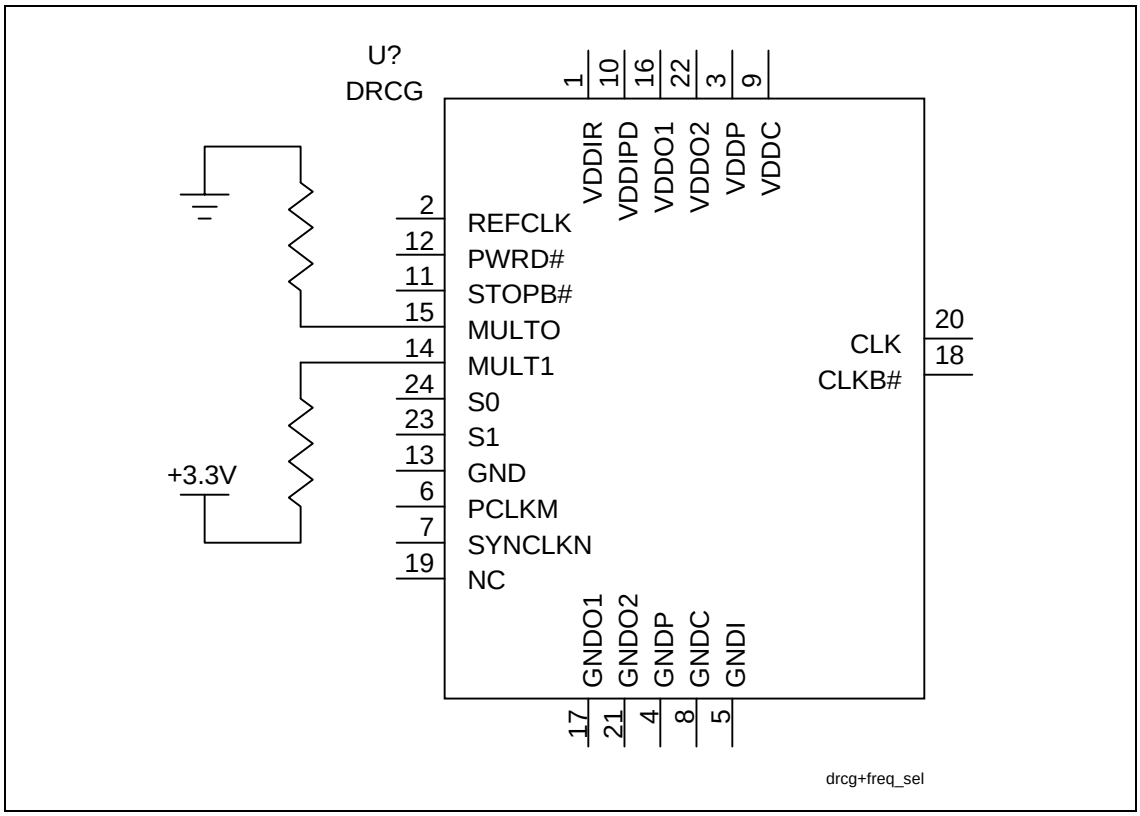
The jitter timing specifications shown in Table 7 are expanded to encompass both the component specification (for DRCG or derivative products) and the channel specification. Follow the component specification when measuring jitter at the DRCG output resistor. Follow the channel jitter guidelines when measuring jitter at the MCH or at the termination for CFM/CFM# on the RDRAM interface.

Table 7. Jitter Timing Specifications

Output Frequency (MHz)	Component Jitter Specification	Channel Jitter Guidelines
400	50 ps	100 ps
300	70 ps	120 ps

DRCG+ and DRCG frequency selection can be accomplished by strapping the MULT[0:1] pins as shown in the figure below. This will allow the selection of the 6:1 multiplier that is required by an MRH-R Memory Expansion Card.

Figure 35. DRCG+ Frequency Selection



5. MEC Power Delivery

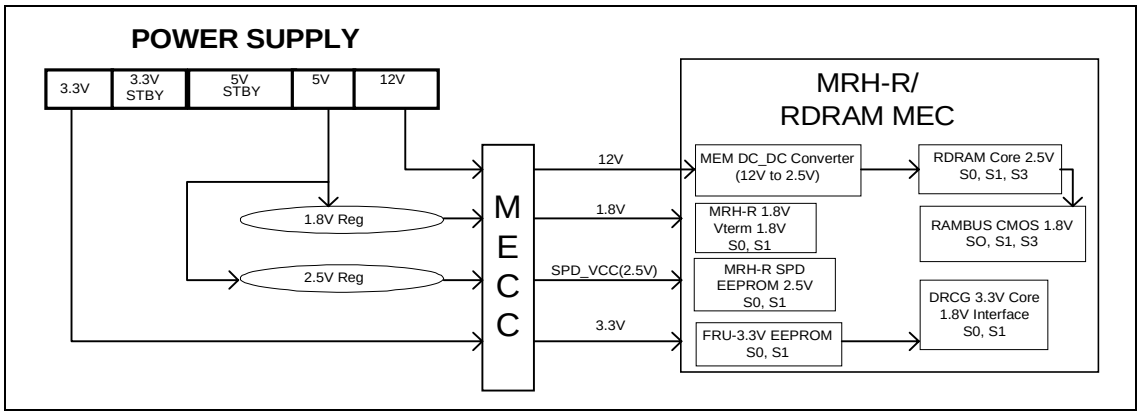
5.1. Definitions

Term	Description
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered.
Full-power operation	During *full-power* operation, all components on the Memory Expansion Card remain powered. Note that *full-power* operation includes both the *full-on* operating state and the S1 (processor stop grant state) state.
Suspend operation	During *suspend* operation, power is removed from some components on the Memory Expansion Card. MEC designs may support the following two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).
Core power rail	A power rail that is only on during full-power operation.
Standby power rail	A power rail that is on during suspend operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). These standby rails are created with a DC-to-DC converter on the MEC.
Derived power rail	A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator or a voltage divider network. For example, 1.8VCMOS can be derived (on the MEC) from either the 2.5V generated using a DC-to-DC converter.

5.2. Power Delivery Block Diagrams

The figure below shows the power delivery architecture for RDRAM based Memory Expansion Cards. This power delivery architecture supports the S*uspend-to-RAM* (STR). During STR, only the necessary devices are powered and this includes main memory. In order to ensure that enough power is available during STR, a thorough power budget must be completed. The power requirements must include each device's power requirements, both in *suspend* and in *full-power*. The power requirements must be compared against the power budget supplied by the power supply.

Figure 36. MRH-R/RDRAM MEC Power Delivery



The examples in this Design Guide are only examples. There are many power distribution methods that achieve the similar results. It is critical, when deviating from these examples in any way, to consider the effect of the change.

The examples in this Design Guide show power planes provided by a WTX power supply. The requirements for each power plane are documented in this section. In addition, an on-board DC-to-DC converter is recommended if using a WTX power supply in order to minimize the number of power pins required on the MECC. Systems implementing an ATX power supply should follow these guidelines, but make the appropriate power rail changes where needed.

12V

In a WTX system, the 12V plane powers the DC-to-DC converter on the MEC. The DC-to-DC converter provides either 2.5V or 3.3V as an output depending on the type of MEC: RDRAM. This implementation minimizes the number of power pins required on the MECC.

Note: This power rail should only be implemented in a WTX design. ATX designs should implement a different power delivery method to generate 2.5V or 3.3V on the MEC. In addition, this power rail needs to remain powered during STR.

2.5V

The 2.5V power plane is used to power the RDRAM core and the VCMOS rail on the RDRAMs.

The RDRAM core requires 2.0 A *maximum average DC current* at 2.5V. On the Memory Expansion Card power delivery examples shown, the 2.5V plane is derived from an onboard DC-to-DC converter.

The VCMOS rail requires a maximum of 3 ma at 1.8V. This rail MUST be powered during Suspend-to-RAM and therefore, the VCMOS rail should NOT be connected to the Vterm rail. Because the current requirements of VCMOS are so low, a resistor divider can be used to generate VCMOS from 2.5V, which remains powered during STR. The resistor divider should be 36 Ω (top) / 100 Ω (bottom). Additionally, it should be bypassed with a 0.1 µF chip capacitor.

1.8V

The 1.8V plane powers the MRH-R core and the RDRAM termination resistors (Vterm). This 1.8V power plane should be generated on the motherboard via a switching regulator.

The MRH-R component requires 1.8V for operation. The MRH-R is not required to be powered during the *Suspend-to-RAM* state. Thus, this power rail can be powered off when the system enters an STR state.

The termination resistors do NOT need to be powered during the STR state.

SPD_VCC (2.5V)

In an RDRAM-based MEC using MRH-R components, this power plane implements a 2.5V signaling environment on the MRH-R SMBus interface used for Serial Presence Detect. This power rail should be generated on the motherboard.

This pin is used to power the EEPROMs on the RIMMs. In addition, the SMBus pullups should be pulled up to SPD_VCC. This power rail should be powered off when entering the Suspend-to-RAM state to avoid leakage into the MRH-R component, which is also powered off.

3.3V

The 3.3V plane powers the DRCG cores and FRU EEPROMs on the MEC. This power rail can be powered off when entering an STR state.

In the power delivery examples shown, 3.3V plane is derived from an onboard DC-to-DC converter to minimize the number of power pins required on the MECC.

5.3. 64/72Mbit RDRAM Excessive Power Consumption

Some 64/72Mbit RDRAM devices interpret non-broadcast, device-directed commands as broadcast commands. These commands are the SET_FAST_CLOCK, SET_RESET, and CLEAR_RESET commands. RDRAM devices consume more current during these initialization steps than during normal operation. As a result of these devices accepting device directed commands as broadcast commands, the device can not be reset/initialized serially. All devices must be reset/initialized simultaneously.

This will result in excessive current draw during the initialization of memory. The amount of excessive current depends on the number of devices and frequency used. There are two potential solutions:

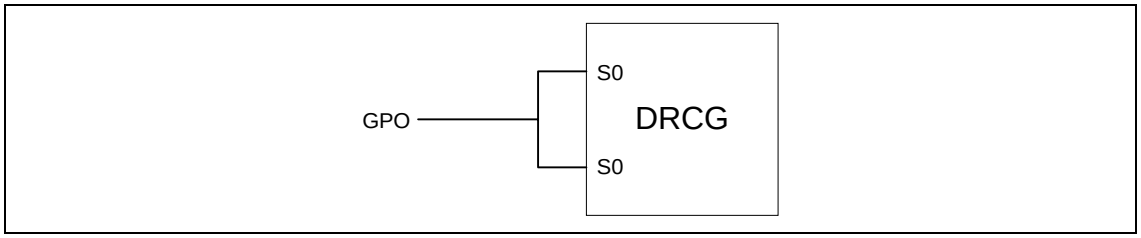
- Reduce the clock frequency during initialization (Section 5.3.1)
- Increase the current capability of the 2.5V voltage regulator (Section 5.3.2).

5.3.1. Option 1—Reduce Clock Frequency During Initialization

Tie a single core well GPO with a default high state to both the S0 and S1 pins of the DRCG (i.e., tie S0 and S1 together and then connect to a GPO as shown in the figure below. When the core power supply to the system is turned on, the DRCG will enter a test mode and the output frequency will match the input REFCLKx frequency. For details on this DRCG mode, refer to the latest DRCG specification. By slowing down the DRCG output clock, the power consumption from the 2.5V power supply will be reduced. After the SetR/ClrR commands have been issued, BIOS drives the GPO low to bring the DRCG back to normal operation.

Note that if a default low GPO is used on power up, all the devices may come up in the standby state at full speed; this requires more power.

Figure 37. GPO Workaround Diagram



This solution requires BIOS modifications.

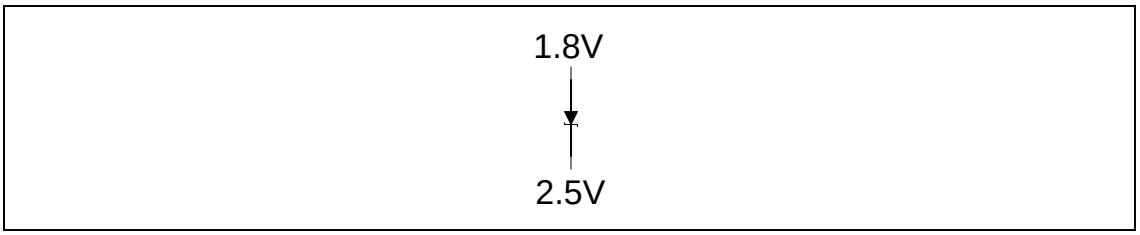
5.3.2. Option 2—Increase Current Capability of 2.5V Voltage Regulator

The second implementation option requires that the 2.5V power supply be modified to maintain the maximum amount of current required by two fully populated RDRAM channels in an Intel system.

5.4. Vterm/Vdd Power Sequencing Requirement

Power MUST NOT be applied to the RDRAM termination resistors (Vterm) prior to applying power to the RDRAM core . This can be guaranteed by placing a Schottky diode between 1.8V and 2.5V as shown in the following figure.

Figure 38. 1.8V and 2.5V Power Sequencing (Schottky Diode)



5.5. 8 RIMM / 2 MRH-R Memory Expansion Card Thermal Considerations

Table 8. RDRAM Power States

Power State	Power (W)
ActiveRead	1.524
ActiveWrite	1.683
Active	0.3922
Standby	0.2677
NAP	0.0111

Assumptions:

1. Latest RDRAM 2.5V Current Specification values.
2. 72-Mbit&144-Mbit components (x18 devices)
3. Vddmax = 2.65V

Table 9. RDRAM Pool Definition

Power State	# of Devices
ActiveRead	2
Active	14
Standby	112
NAP	0

Assumptions:

1. Assumes NO NAP for best performance.
2. *Refer to the *Intel 840 Chipset: 82840 Memory Controller Hub (MCH)* datasheet for pooling information.

Table 10. MEC RDRAM Power (Reads)

Power State	Power(W)
ActiveRead	3.048
Active	5.5
Stby	30.0
NAP	0.0
Total	**38.5**

Table 11. MEC RDRAM Power (Writes)

Power State	Power(W)
ActiveWrite	3.366
Active	5.5
Stby	30.0
NAP	0.0
Total	**38.8**

Table 12. MEC Discrete Device Power

Device	Power(W)	Quantity	Total (W)
DRCG (3.3V)	0.33	4	1.32
DRCG (1.8V)	0.0036	8	0.0288
MRH-R (1.8V)	2.2	2	4.4
Vterm (1.8V)	0.054	88	4.752

Table 13. MEC Power Rails

Rail	Current (A)	Power(W)
1.8 V	5.100444444	9.1808
3.3 V	0.4	1.32
2.5 V	15.53568	38.8
12 V	3.8	45.7

NOTES:
1. 2.5V is derived from a DC-DC converter with 12V input.
2. Efficiency of the DC-DC converter is rated at ~85%.

6. Design Checklist

Use the following checklist as a final check to ensure the motherboard incorporates solid design practices. This list is only a reference. For correct operation, all of the design guidelines within this document must be followed.

Table 14. Signal List

RSL Signals	High-Speed CMOS Signals	Serial CMOS Signal	Clocks
• DQA[8:0] • DQB[8:0] • RQ[7:0]	• CMD • SCK	• SIO	• CTM • CTM# • CFM • CFM#

- Ground Isolation Well Grounded
  - — Via to ground every ½ inch around edge of isolation island
  - — Via to ground very ½ inch between RIMMs
  - — Via to ground every ½ inch between RSL signals
  - — Via between every signal within 100mils of the MRH edge and the connector edge
  - — No unconnected ground floods
  - — All ground isolation at lest 10 mils wide
  - — Ground isolation fills between *serpentines*
  - — Ground isolation not *broken* by C-TABs
  - — Ground isolation connects to the ground pins in the middle of the RIMM connectors
  - — Ground isolation vias connect on all layers and should NOT have thermal relieves
  - — Ground pins in RIMM connector connect on all layers

- Vterm Layout Yields Low Noise (Decoupling Vterm is CRITICAL!)
  - Solid Vterm island is on top routing layer – do not split this plane
  - Ground island (for ground side of Vterm caps) is on top routing layer
  - Termination Resistors connect DIRECTLY to the Vterm island on the routing (without vias)
  - Decoupling capacitors connect to top layer Vterm island and top routing layer ground island directly (see layout example)
  - Use AT LEAST 2 vias per decoupling capacitor in the top layer ground island
  - Use 2 x 100 uF TANTALUM capacitors to decouple Vterm (Aluminum/Electrolytic capacitors are too slow!)
  - High-frequency decoupling capacitors MUST be spread-out across the termination island so that all termination resistors are near high-frequency capacitors
  - 100uF TANTALUM capacitors should be at each end of the Vterm island
  - 100uF TANTALUM capacitors must be connected to Vterm island directly
  - 100uF TANTALUM capacitors must have AT LEAST 2 vias/cap to ground
  - Vterm island should be 50 – 75 mils wide
  - Vterm island should not be broken
  - If any RSL signals are routed out of the 2nd RIMM (towards termination) on a plane referenced to power (even for a short distance), ensure Ground Reference Plane (on the power plane) is continuous under the termination resistors/capacitors
  - Ensure current path for power delivery to the MRH does not go through the Vterm island
  - Refer to section 3.5.3 in this design guide.
- CTM/CTM# Routed Properly
  - CTM/CTM# are routed differentially from DRCG to 2nd RIMM
  - CTM/CTM# are ground isolated from DRCG to 2nd RIMM
  - CTM/CTM# are ground referenced from DRCG to 2nd RIMM
  - Vias are placed in ground isolation and ground reference every ½”
  - When CTM/CTM# serpentine together, they MUST maintain EXACTLY 6 mils spacing
- Clean DRCG Power Supply
  - 3.3V DRCG power flood on the top layer. This should connect to each
  - High frequency (0.1µF) capacitors are near the DRCG power pins. One capacitor next to each power pin.
  - 10 µF bulk *tantalum* capacitor near DRCG connected directly to the 3.3V DRCG power flood on the top layer
  - Ferrite bead isolating DRCG power flood from 3.3V main power also connecting directly to the 3.3VDRCG power flood on the top layer
  - Use 2 vias on the ground side of each
- Good DRCG Output Network Layout
  - Series resistors (39 Ω) should be VERY near CTM/CTM# pins
  - Parallel resistors (51 Ω) should be very near series resistors
  - CTM/CTM# should be 18mils wide from the CTM/CTM# pins to the resistors
  - CTM/CTM# should be 14 on 6 routed differential as soon as possible after the resistor network
  - When not 14 on 6, the clocks should be 18 mils wide
  - Ensure CTM/CTM# are ground referenced and the ground reference is connected to the ground plane every ½” to 1”
  - Ensure CTM/CTM are ground isolated and the ground isolation is connected to the ground plane every ½” to 1”
  - Ensure 15 pf EMI capacitors to ground are removed (the pads are not necessary and removing the pads provides more space for better placement of other components)
  - Ensure the 4 pf EMI capacitor described in Section 4.1.3 of this design guide is implemented (but do not assemble the capacitor)

- Good RSL Transmission Lines
  - RSL traces are 18 mils wide
  - RSL traces do NOT neckdown when routing into the RIMM connector
  - If tight serpentining is necessary, 10 mil ground isolation MUST be between serpentine segments (i.e., an RSL signal CAN NOT serpentine so tightly that the signal is adjacent to itself with no ground isolation between the serpentines).
  - RSL traces do not cross power plane splits. RSL signals must also not be routed *on next to* a power plane splits
  - Uniform ground isolation flood is exactly 6 mils from the RSL signals at all times
  - ALL RSL, CMD/SCK, and CTM/CTM#/CFM/CFM# signals have C-TABs on each RIMM connector pin
  - All RSL signals are routed adjacent to a ground reference plane. This includes all signals from the 2nd RIMM to the termination. If signals are routed referenced to ground from the 2nd RIMM to the termination, the ground reference plane MUST extend under these signals AND include the ground side of the Vterm decoupling capacitors.
  - CTABs must not cross (or be on top of) power plane splits. They must be ENTIRELY referenced to ground.
  - At least 10 mils ground flood isolation required around ALL RSL signals (ground isolation must be exactly 6 mils from RSL signals). Ground flood recommended for isolation. This ground flood should be as close to the MRH-R (and the 1st RIMM) as possible. If possible connect the flood to the ground balls/pins on the MRH-R/connector.
- Clean Vref Routing
  - Ensure 1 x 0.1 uF capacitor on Vref at each connector
  - Use 10 mil wide trace (6 mils minimum)
  - Do not route Vref near high-speed signals
- RSL Routing
  - All signals must be length matched within ±10 mils of the Nominal RSL Length as described in the in this design guide. Ensure that signals with a dummy via are compensated correctly.
  - ALL RSL signals must have 1 via near the MRH BGA pad. Signals routed on the bottom layer of the MB will have a “real via” while signals routed on the top layer will have a “dummy via”. Additionally, all signals with a dummy via must have an additional trace length of 25 mils.
  - Signals must “alternate” layers as shown in the in this design guide.
- RSL Routing
  - Clock signals must be routed as a differential pair. The traces must be 14 mils wide and 6 mils apart (with no ground isolation) when they are routed as a differential pair. For very short sections under the MRH-R and under the 1st RIMM, it will not be possible to route as a differential pair. In these sections, the clocks signals MUST neck up to 18 mils and be ground isolated with at least 10 mils ground isolation.
  - Clock signals must be length compensated (using the 1.021 length factor described in Section 4.1). Ensure that each clock pair is length matched within ±2 mils.
  - When clock signals serpentine, they must serpentine together (to maintain differential 14:6 routing).
  - 22 mils ground isolation required on each side of the differential pair.

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7. Schematics

NOTE: The MRH-R MEC schematics shown assume the MRH-R component is completely powered off if support for *Suspend to Ram (S3)* is required.

MEMORY EXPANSION CARD SCHEMATICS [MRH-R]
REVISION 1.0

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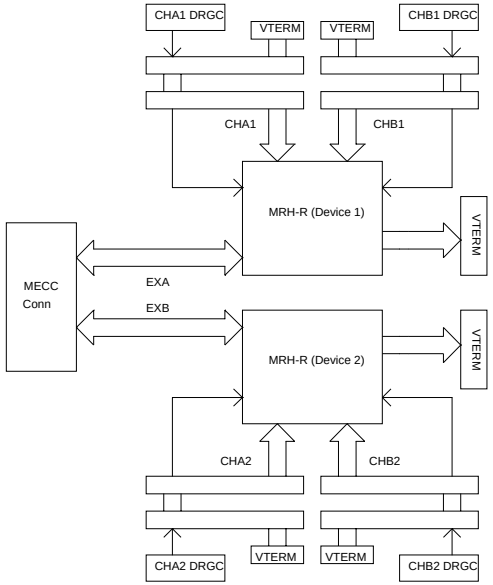
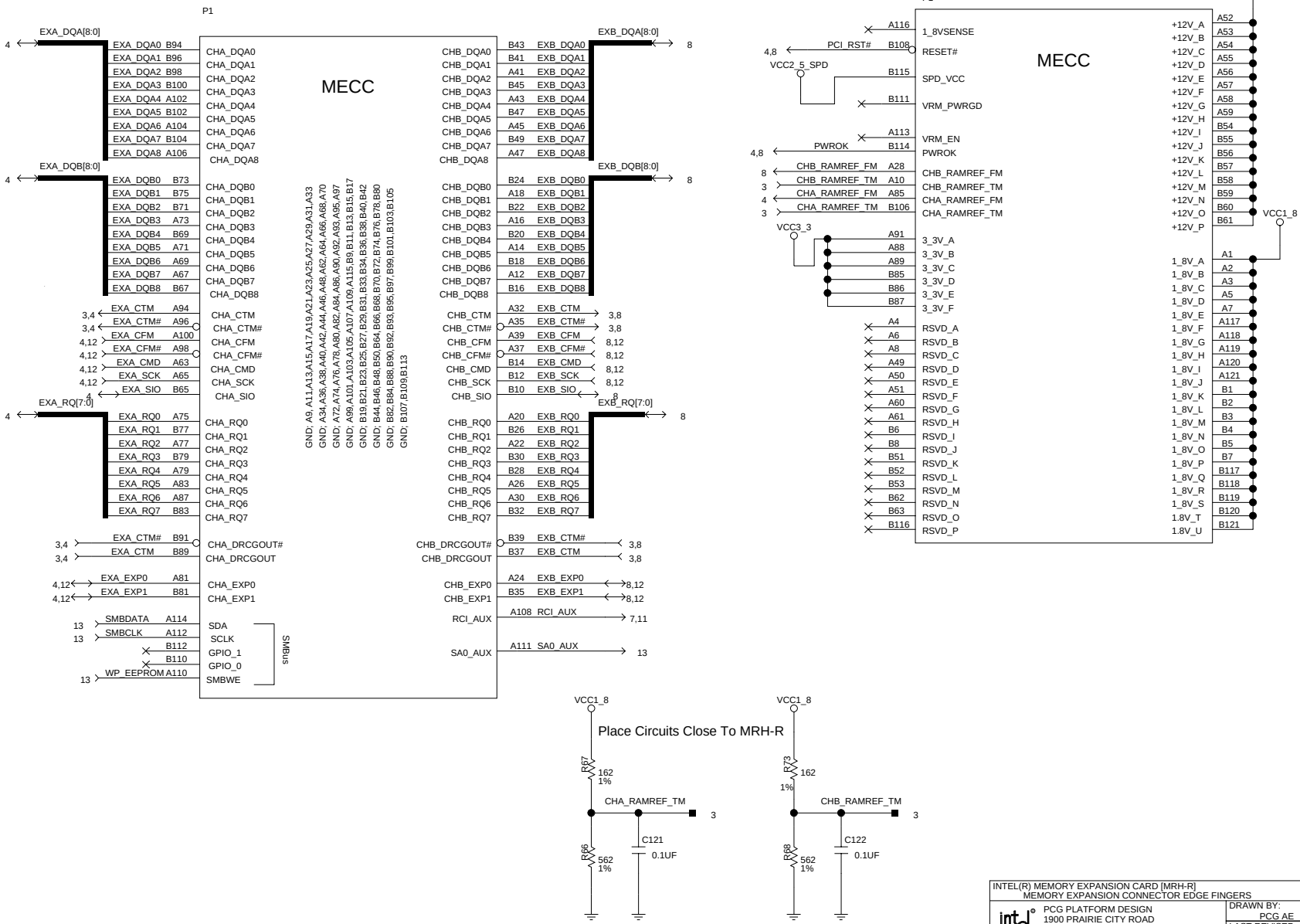
INTEL(R) MEMORY EXPANSION CARD [MRH-R]		REV: 1.0
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 1 OF 14

2 MRH-R Block Diagram (4 RIMM)



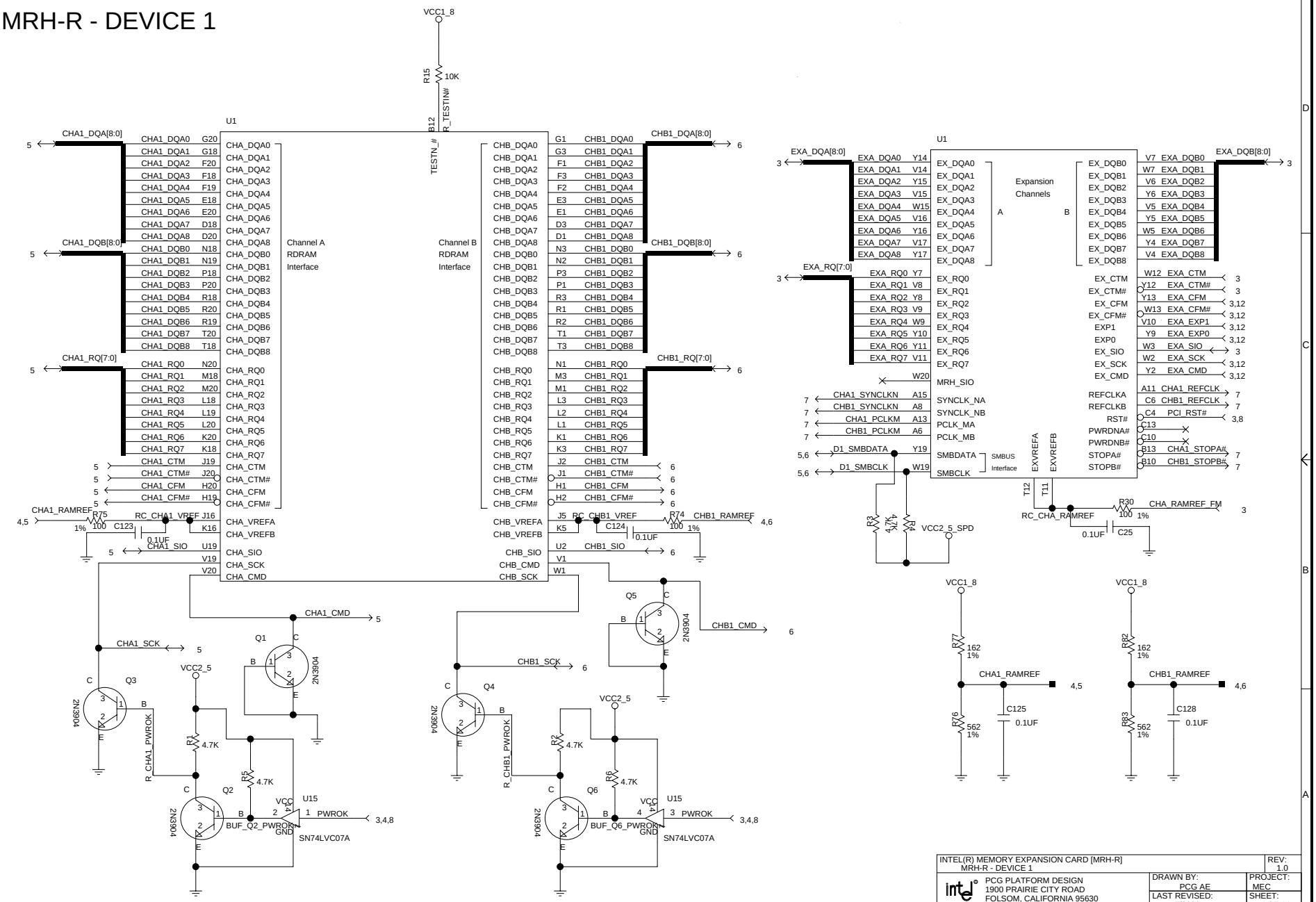
INTEL(R) MEMORY EXPANSION CARD [MRH-R]		REV: 1.0
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE LAST REVISED: 7/2000	PROJECT: MEC SHEET: 2 OF 14

MEMORY EXPANSION CONNECTOR EDGE FINGERS



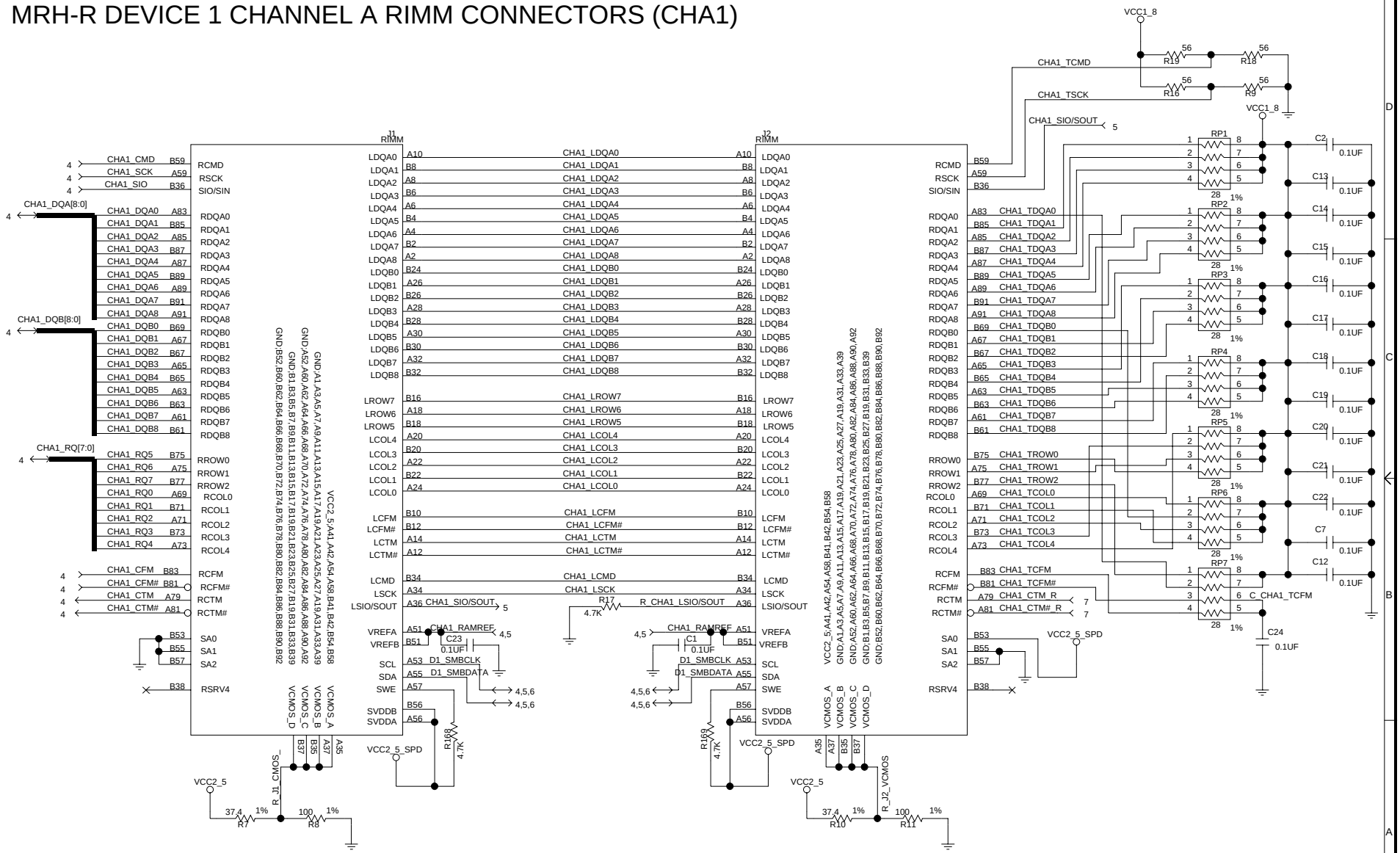
INTEL(R) MEMORY EXPANSION CARD [MRH-R] MEMORY EXPANSION CONNECTOR EDGE FINGERS		REV: 1.0
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 3 OF 14

MRH-R - DEVICE 1



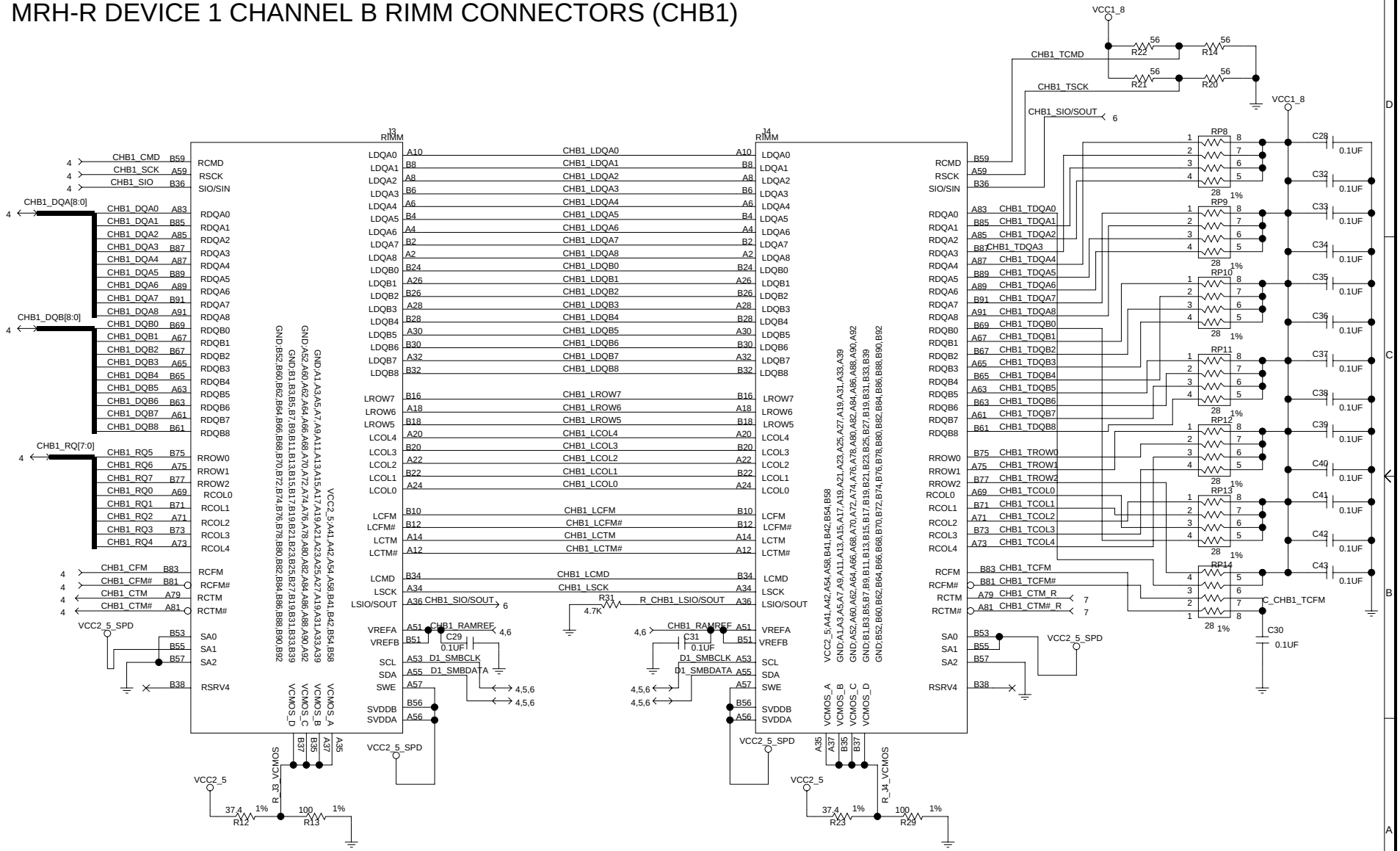
INTEL(R) MEMORY EXPANSION CARD [MRH-R] MRH-R - DEVICE 1		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 4 OF 14

MRH-R DEVICE 1 CHANNEL A RIMM CONNECTORS (CHA1)



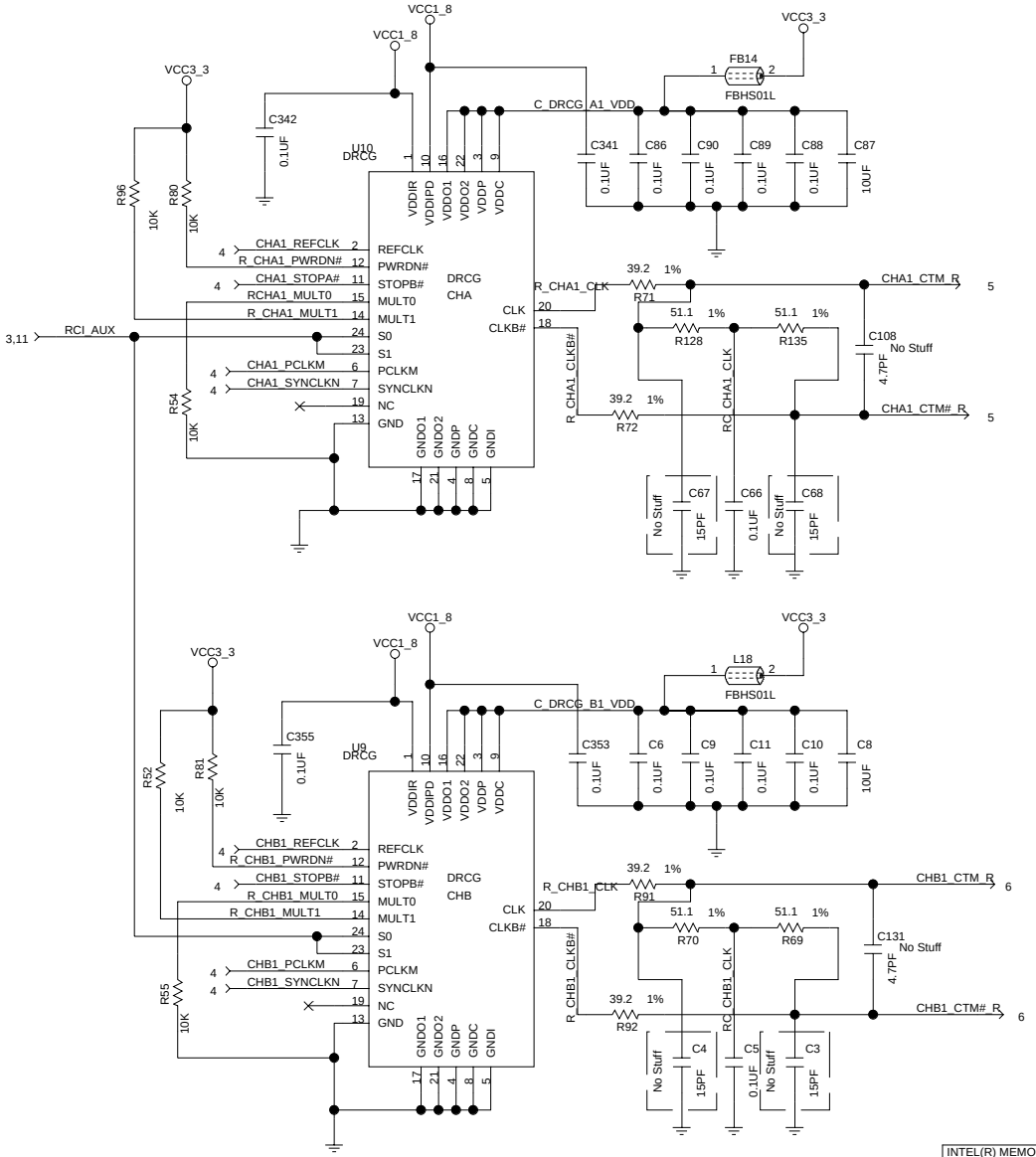
INTEL(R) MEMORY EXPANSION CARD [MRH-R] MRH-R DEVICE 1 CHANNEL A RIMM CONNECTORS (CHA1)		REV: 1.0
intel PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 5 OF 14

MRH-R DEVICE 1 CHANNEL B RIMM CONNECTORS (CHB1)



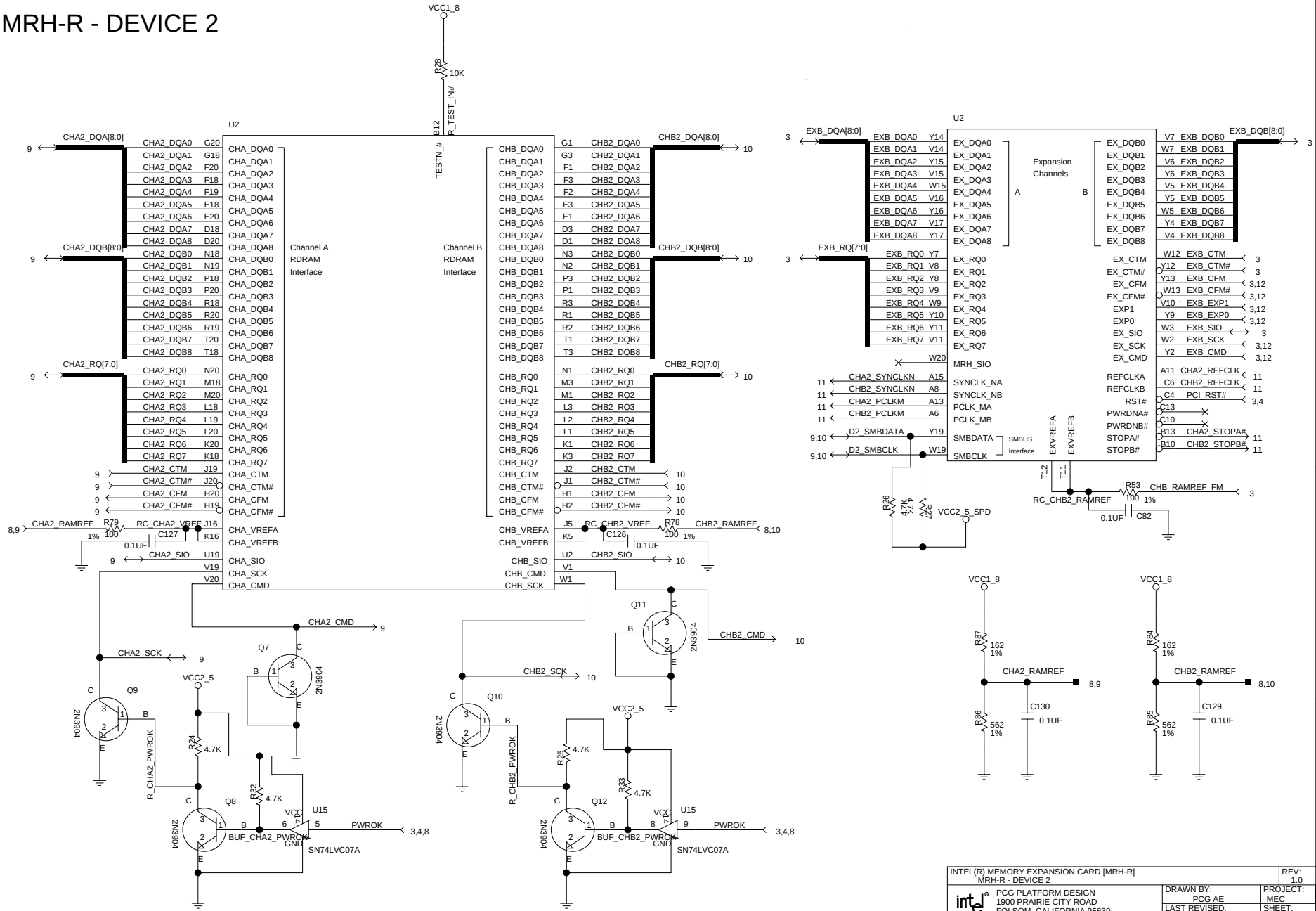
INTEL(R) MEMORY EXPANSION CARD [MRH-R] MRH-R DEVICE 1 CHANNEL B RIMM CONNECTORS (CHB1)		REV: 1.0
intel PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 6 OF 14

MRH-R DEVICE 1 DRCG SYNTHESIZERS



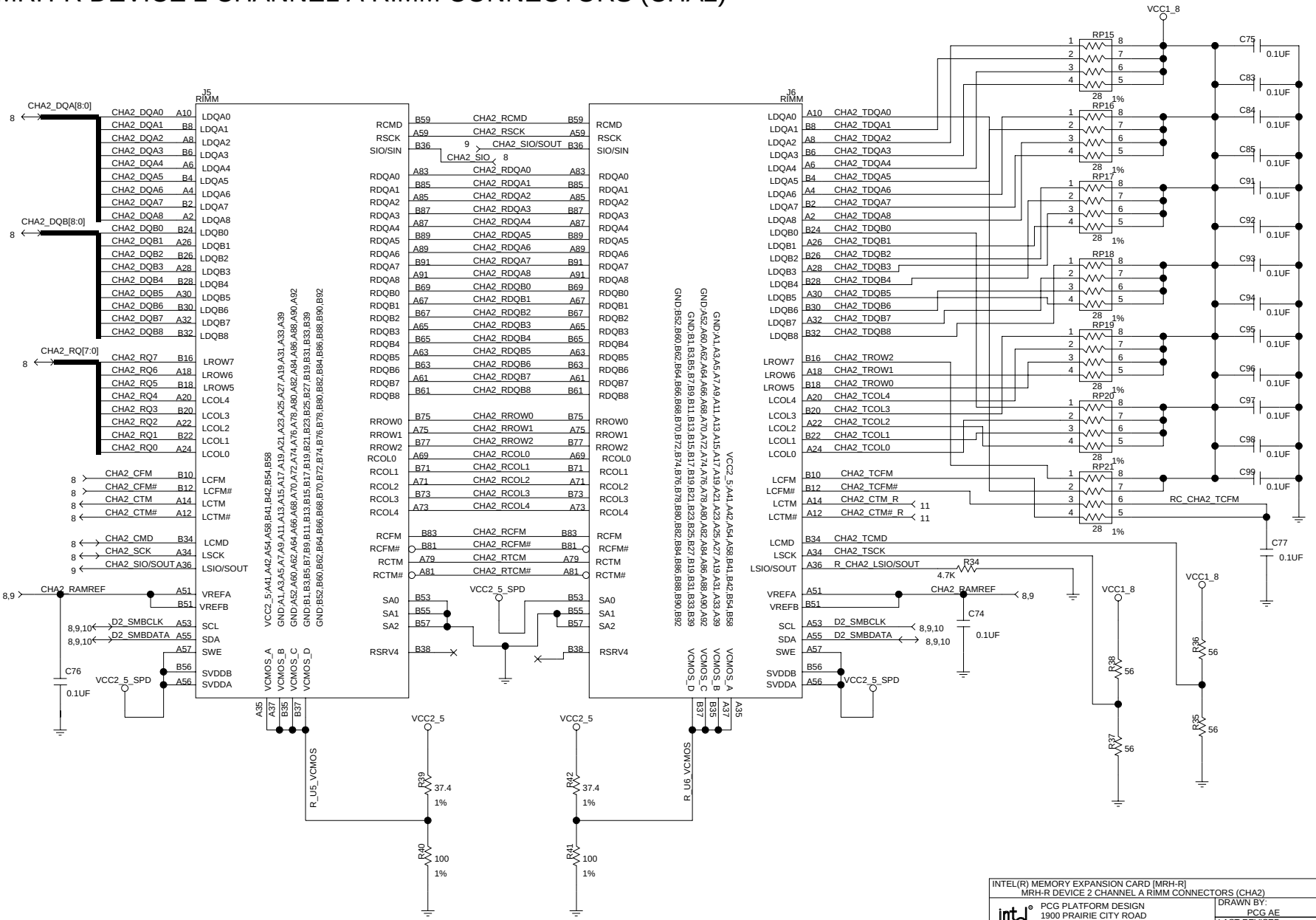
INTEL(R) MEMORY EXPANSION CARD [MRH-R] MRH-R DEVICE 1 DRCG SYNTHESIZERS		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 7 OF 14

MRH-R - DEVICE 2

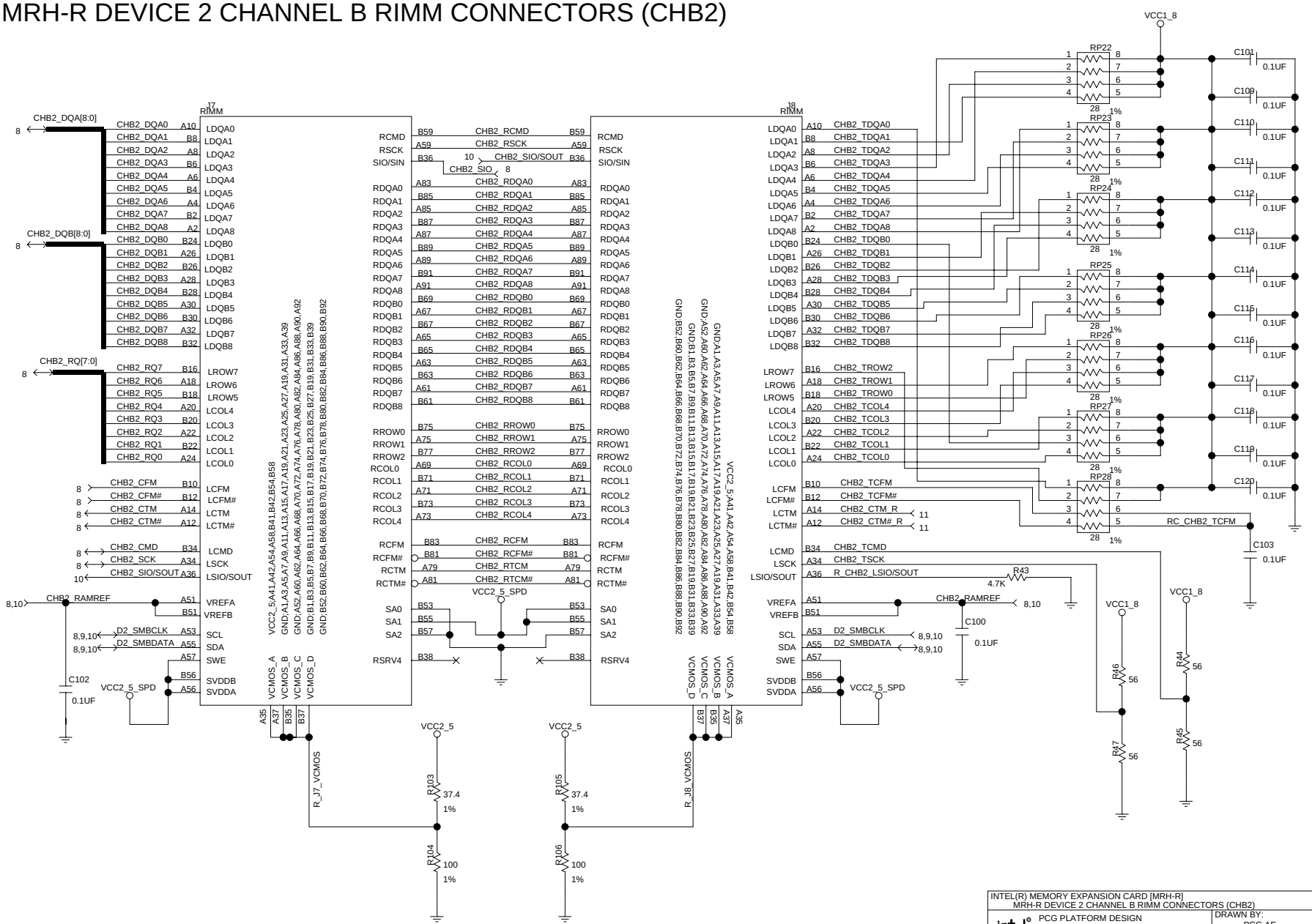


INTEL(R) MEMORY EXPANSION CARD [MRH-R] MRH-R - DEVICE 2		REV: 1.0
PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE LAST REVISED: 7/2000	PROJECT: MEC SHEET: 8 OF 14

MRH-R DEVICE 2 CHANNEL A RIMM CONNECTORS (CHA2)

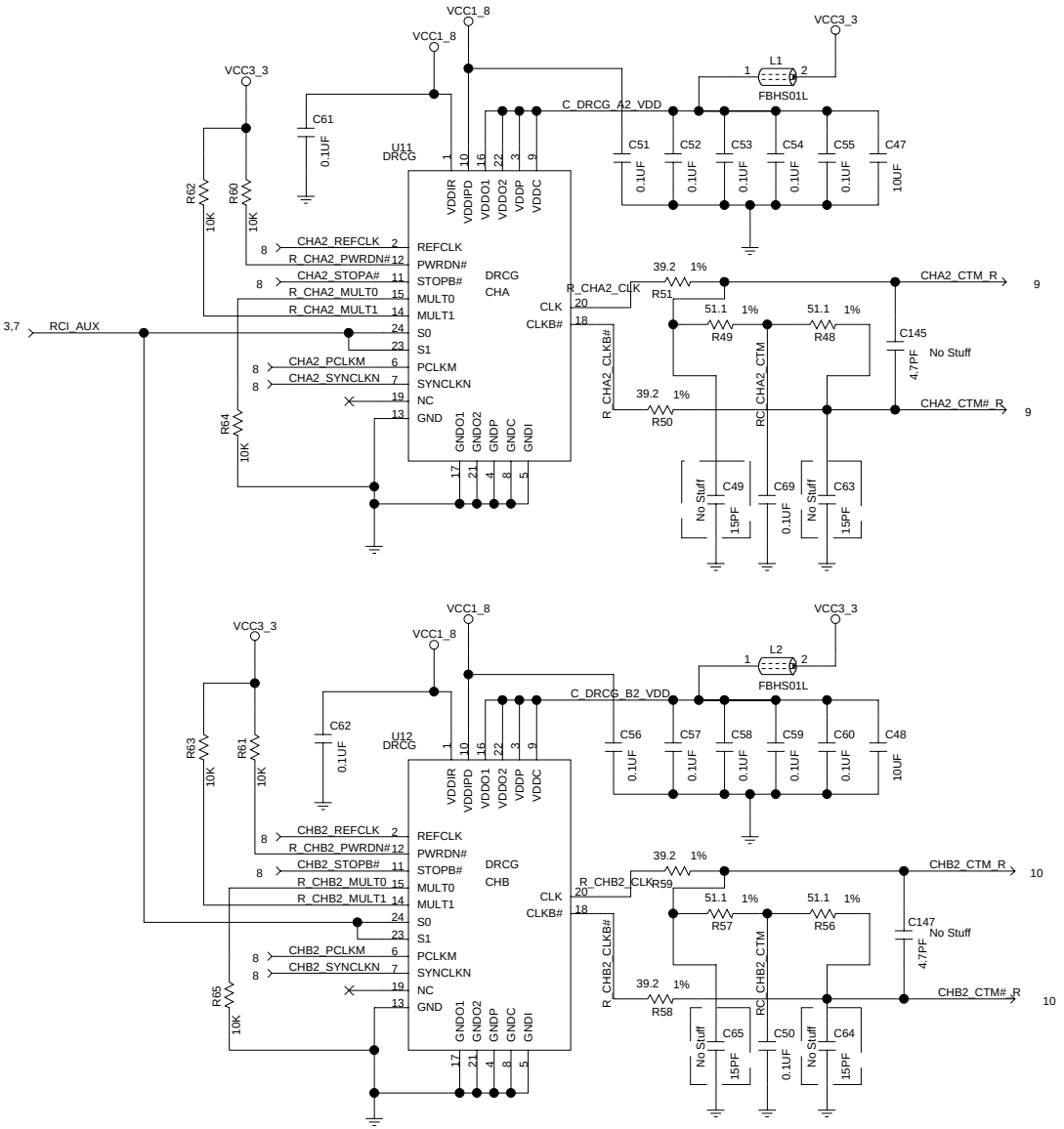


MRH-R DEVICE 2 CHANNEL B RIMM CONNECTORS (CHB2)



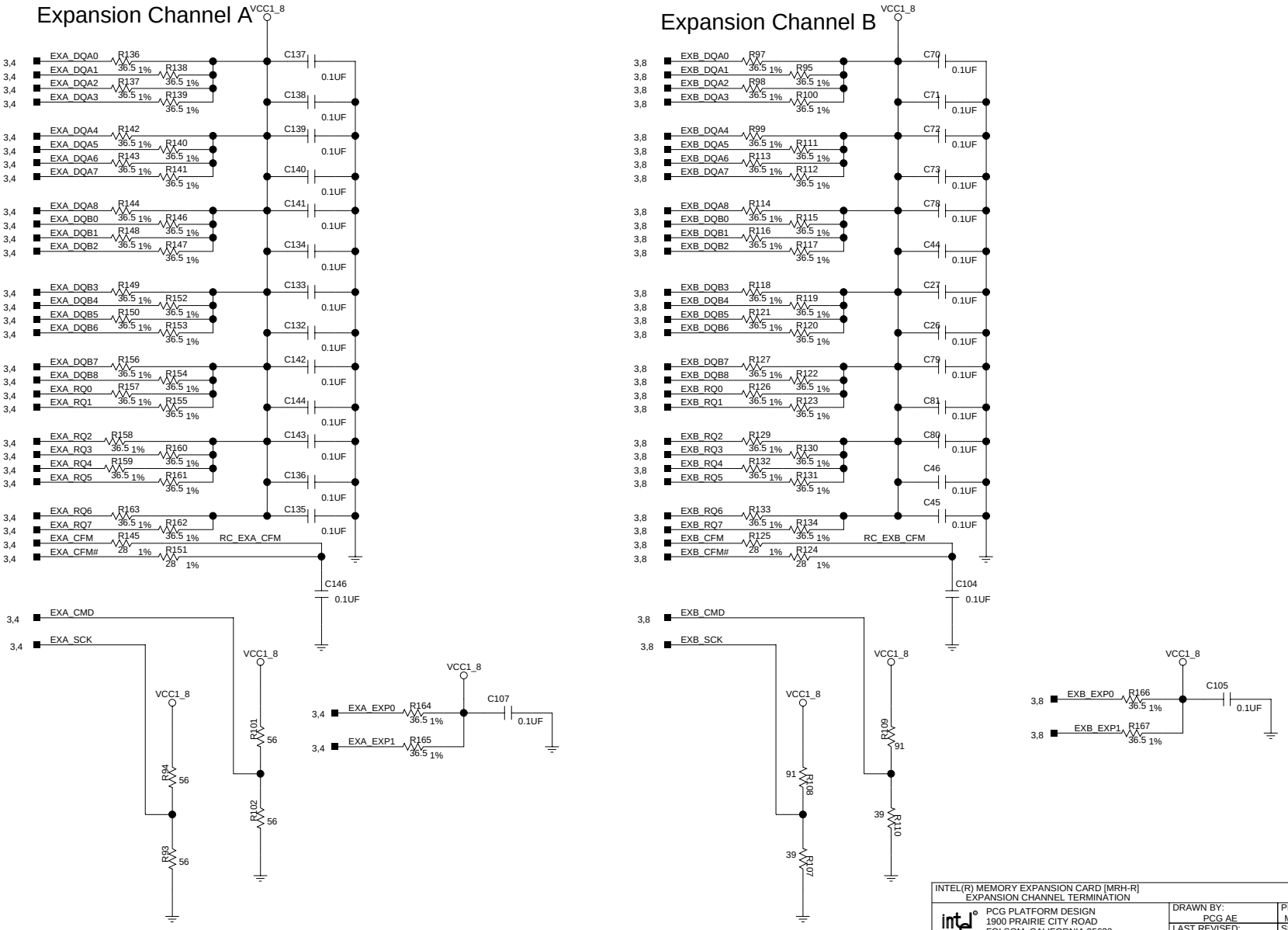
INTEL(R) MEMORY EXPANSION CARD [MRH-R] MRH-R DEVICE 2 CHANNEL B RIMM CONNECTORS (CHB2)		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 10 OF 14

MRH-R DEVICE 2 DRCG SYNTHESIZERS



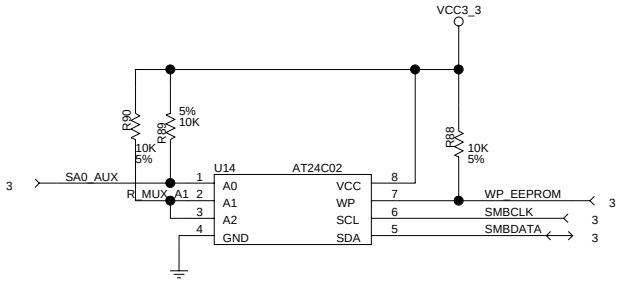
INTEL(R) MEMORY EXPANSION CARD [MRH-R] MRH-R DEVICE 2 DRCG SYNTHESIZERS		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 11 OF 14

EXPANSION CHANNEL TERMINATION



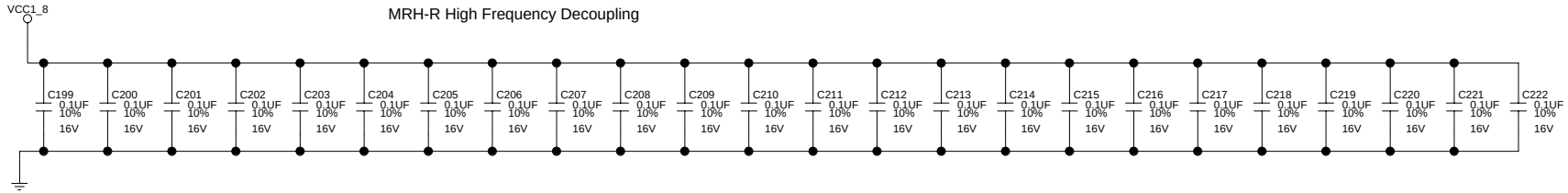
INTEL(R) MEMORY EXPANSION CARD [MRH-R] EXPANSION CHANNEL TERMINATION		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 12 OF 14

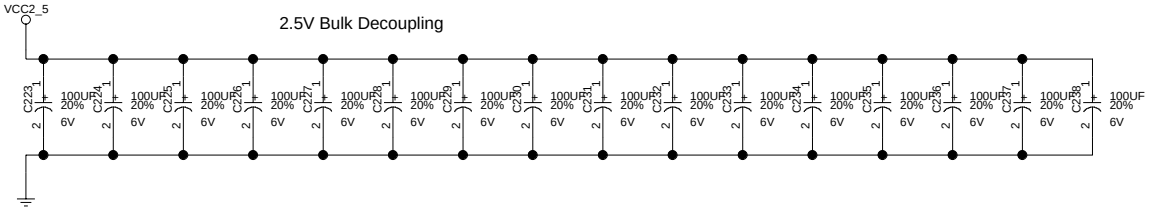
MECC EPROM

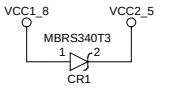


INTEL(R) MEMORY EXPANSION CARD [MRH-R] MECC EPROM		REV: 1.0
intel® PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 13 OF 14

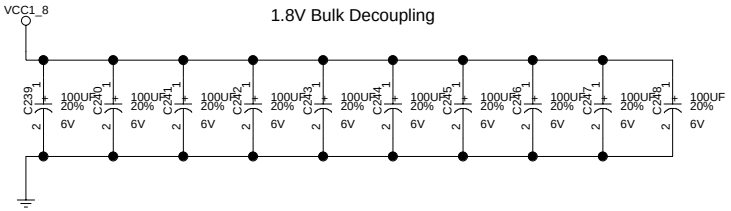
DECOUPLING

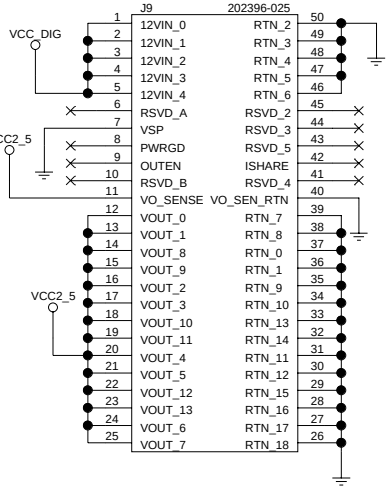


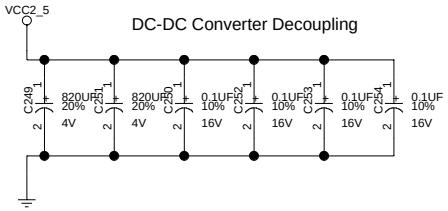


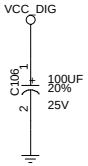


POWER SEQUENCEING DIODE









INTEL(R) MEMORY EXPANSION CARD [MRH-R] DECOUPLING		REV: 1.0
intel PCG PLATFORM DESIGN 1900 PRAIRIE CITY ROAD FOLSOM, CALIFORNIA 95630	DRAWN BY: PCG AE	PROJECT: MEC
	LAST REVISED: 7/2000	SHEET: 14 OF 14

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