SRKA4 / ISP4400 Server System

Technical Product Specification

Intel Order Number A43494-001

Revision 1.4

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Enterprise Platforms Group
Server Products Division

Revision History

Date	Revision Number	Modifications
July 20, 2000	1.2	Production release.
August 16, 2000	1.2	Minor typographical changes
September, 2000	1.3	Deleted section 2.6 Expansion Support Added section 2.6.2 MTBF Specifications. Added section 2.6.3 Operational Specifications. Added section 3.1 Interconnect Block Diagram
April 19, 2002	1.4	Added Appendix C: Slim CD Specifications

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1. Introduction

This document provides an overview of the SRKA4 and ISP4400 server systems and includes information on chassis hardware, cables, connectors, power subsystem, hard disk bay assembly, front panel board, fan carrier board, and regulatory requirements. Throughout the remainder of this document, references to the SRKA4 server system will also imply the ISP4400 server system unless otherwise noted.

1.1 Document Structure and Outline

This document is organized into the following chapters:

Chapter 1: Introduction
Provides an overview of this document.

Chapter 2: System Overview
Provides an overview of the SRKA4 server chassis hardware.

Chapter 3: Cables and Connectors
Describes the cables and connectors used to interconnect the SKA4 board set and the server system components.

Chapter 4: Power Subsystem
Describes the specifications of the power subsystem.

Chapter 5: Hard Disk Bay Assembly
Describes the specifications of the hard disk bay assembly.

Chapter 6: Front Panel Board
Describes the specifications of the front panel board.

Chapter 7: Fan Carrier Board
Describes the specifications of the fan carrier board.

Chapter 8: Regulatory Specifications
Describes system compliance to regulatory specifications.

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2. System Overview

This chapter describes the features of the Intel® SRKA4 Server System chassis. The system chassis houses the SKA4 board set and supporting system boards within a 4U x 32.5" (+/-) deep space, and mounts in a 19-inch rack. The chassis itself is 26.5" deep with the extra six inches accounting for cable management. The chassis provides easy access for performing maintenance and upgrades, for adding memory, and for adding or removing PCI cards.

The functional server weighs between 56 and 88 pounds, depending on the internal configuration. The chassis provides adequate thermal cooling of all devices within an ambient temperature of 5° to 35°C, while maintaining noise levels below 55 dBa.

2.1 System Features

Table 2-1 provides a list and brief description of the features of the SRKA4 Server System, which utilizes the SKA4 baseboard.

Table 2-1: SRKA4 Server System Feature List

Feature	Description
Upgradeability	The system can be upgraded to future processors within the Pentium® III Xeon™ processor family.
PCI hot plug	The chassis with the SKA4 board set supports six 64-bit PCI hot-plug slots (two at 66/33 MHz, four at 33 MHz).
Half-length PCI	The SKA4 board set supports two 32-bit 33-MHz half-length PCI slots.
Compact, high-density system	The system size is a 4U (7-inch) rack-mount server.
Redundant power	The system supports three 350-W power supplies in a redundant (2+1) configuration.
Redundant cooling	Six system fans in a redundant (5+1) configuration cool the system. The system can also be configured in a non-redundant (3+0) configuration.
User configurable peripheral bay	The peripheral bay supports one 5.25-inch half-height device, and either a 1/2-inch floppy disk drive and 1/2-inch CDROM **or** a single 3.5-inch floppy drive.
Intelligent Management Platform Initiative (IPMI) compliant	Intelligent Platform Management Bus (IPMB) for intrachassis communication is provided. Emergency management port (EMP) is used for remote management.

2.2 Overview

The scalable architecture of the SRKA4 server system supports symmetrical multiprocessing (SMP) and a variety of operating systems (OS). The SKA4 baseboard contains connectors for installing up to four Intel® Pentium® III Xeon™ processors packaged in single-edge contact cartridges (SECC). A single memory expansion card supports up to 16 GB of error correction code (ECC) PC-100 compatible registered DIMMs. The baseboard contains two 66-MHz/33-MHz and four 33-MHz 64-bit hot-swap PCI slots, two 33-MHz 32-bit PCI slots, I/O ports, and various controllers.

Figure 2-1 shows an isometric view of the system. Figure 2-2 shows the system with the top covers and the front bezel removed.

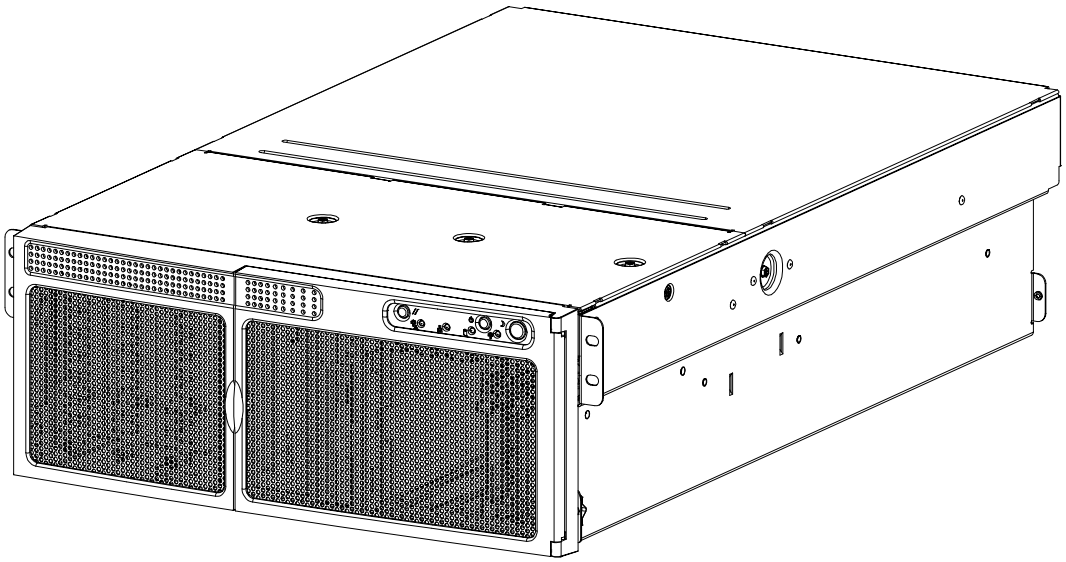

Figure 2-1: SRKA4 Server System

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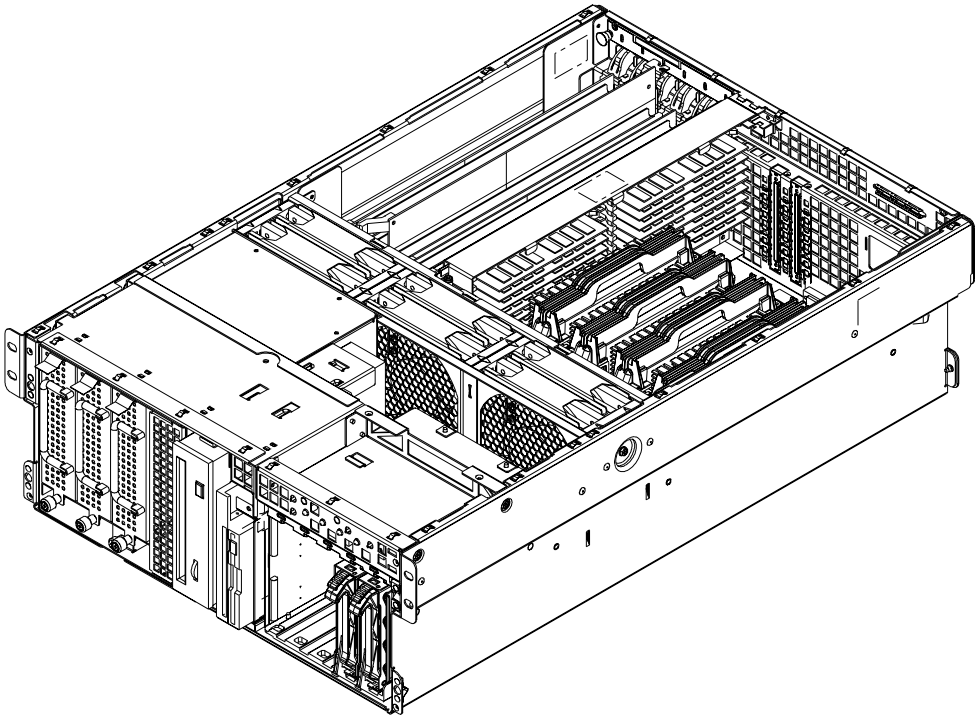

Figure 2-2: SRKA4 System (shown with top covers and bezel removed)

The peripheral bay at the front of the chassis supports a half-height 5.25-inch device (e.g., CD-ROM or DAT) and either a 1/2 inch floppy and a 1/2 inch CD-ROM, or a 3.5-inch floppy. If no device is installed in the 5.25 inch device bay, an EMI shield should be installed to maintain proper cooling and EMI shielding.

To the right of this area is the hot-swap hard drive bay. This supports five 1.0 inch or three 1.6 inch hot-swap (SCA) hard drives, depending on the system configuration. SCSI drives installed in the hot-swap hard drive bays can be hot-swapped if supported by the operating system.

The front panel is located above the hard drive bay and provides user interface for system management.

The chassis supports up to three hot-swap, redundant power supplies in a 2+1 configuration. A cover plate for the unoccupied power supply location is supplied for systems without redundancy, and should be used to provide adequate cooling and EMI shielding.

The system baseboard is mounted horizontally in a subassembly called the e-bay, shown in Figure 2-3. The e-bay is mounted near the rear of the chassis. The bay is divided into two logical areas, a user accessible area and a trained service personnel area. The user area allows hot-plug PCI functionality under normal system operation. The service personnel area is protected by a piece of EPAK* material clearly denoted with a caution label and should be entered only when the system has been powered off and the AC cable is disconnected.

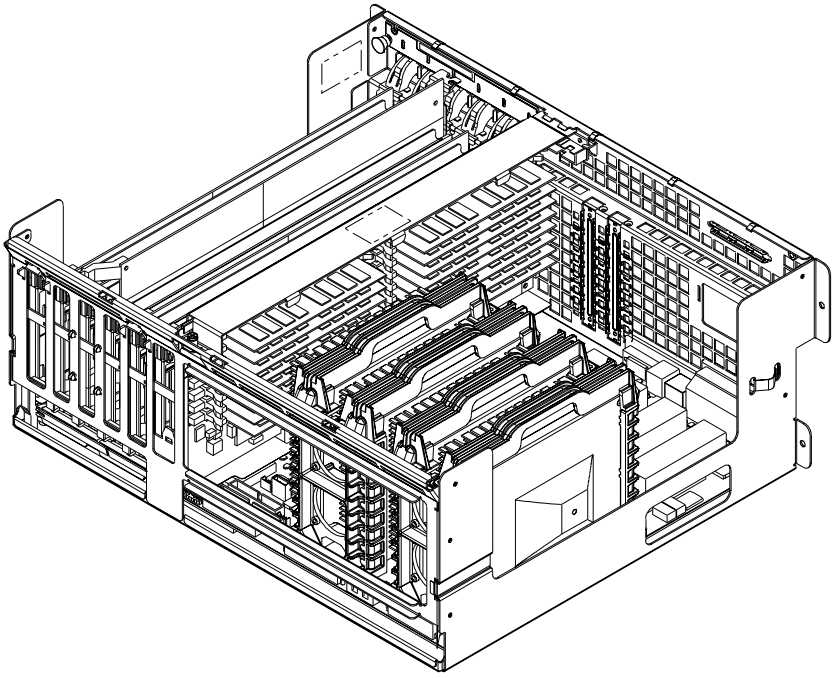

Figure 2-3: E-bay Containing SKA4 Baseboard

The system contains a hot-swap, redundant (5 + 1) fan array to cool the baseboard and other components. The fans are installed in a bay located in front of the e-bay. Individual fan status indicators are located on the fan board mounted in the fan bay. A fan failure is also indicated by the general fault light-emitting diode (LED) located on the front panel.

The front bezel can be customized so integrators can meet their industrial design requirements. The bezel design allows adequate airflow to cool the system components. It also contains a door to provide access to the peripheral devices and the hot-swap hard drives.

Figure 2-4 shows a block diagram of the SRKA4 server system with interconnections.

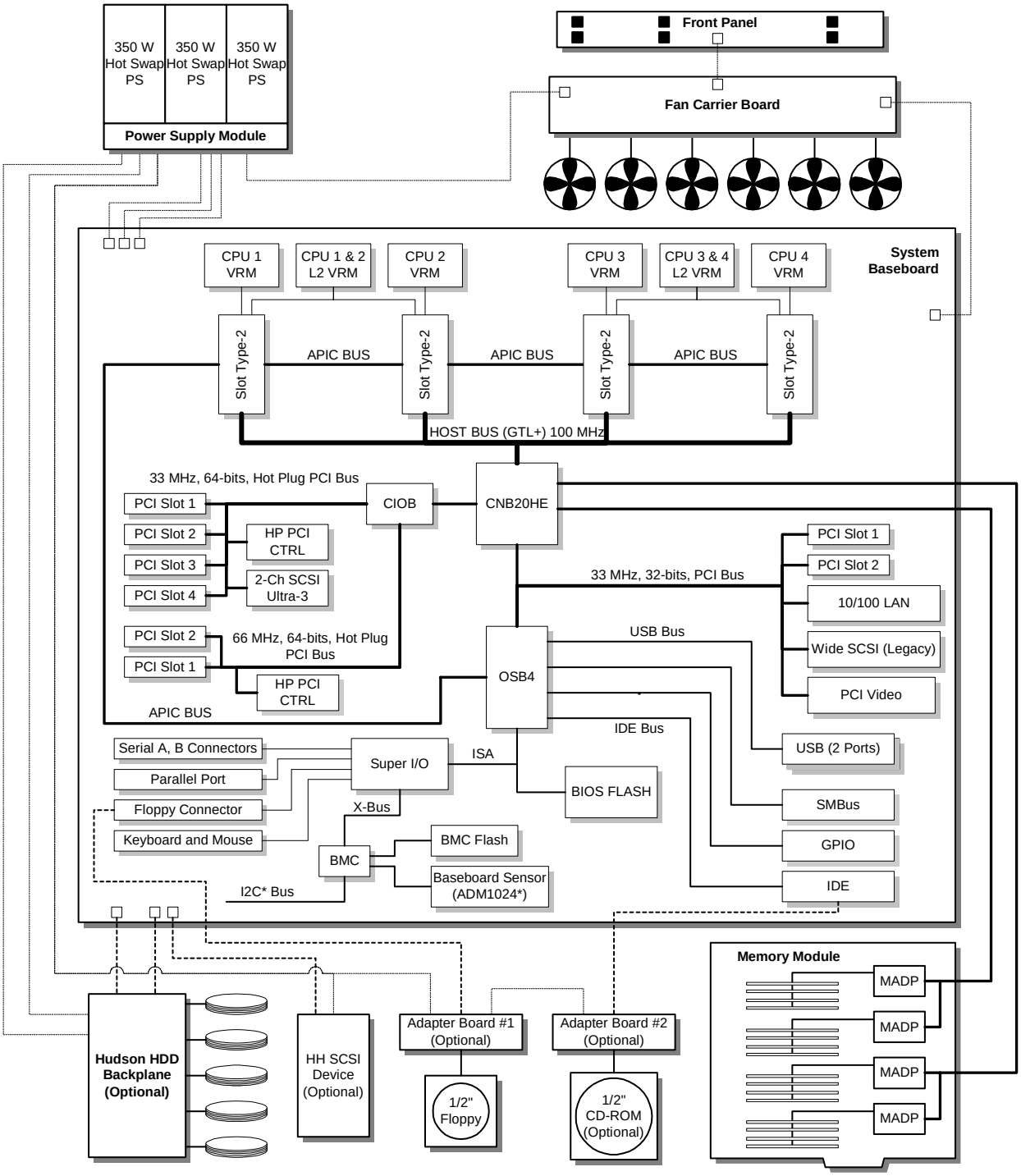

Figure 2-4: SRKA4 Server System Block Diagram

2.3 External Chassis Features

2.3.1 Front View of Chassis

The front panel assembly consists of a hinged metal and plastic bezel, which serves as a cosmetic piece only, and can be integrator-specific. An oval clear plastic lens or hole on the bezel door provides visibility to the front panel indicator lights (power indicator, hard disk drive activity, network activity, and general system fault).

When the bezel door is opened, the hot-swap hard drive bay assembly, peripheral device bay, and (if plastic lens is installed) the front panel switches (power, reset, and sleep) are exposed. When the bezel door is removed, the power supply subsystem, and the front panel switch for non-maskable interrupts (NMI) are exposed.

Figure 2-5 shows the front view of the system. Figure 2-6 shows the front view of the system with the front bezel removed. The front bezel provides access to the following user-accessible areas:

- Front panel
- Peripheral bay
- Hard disk drive bay

These areas are described in detail in the following sections.

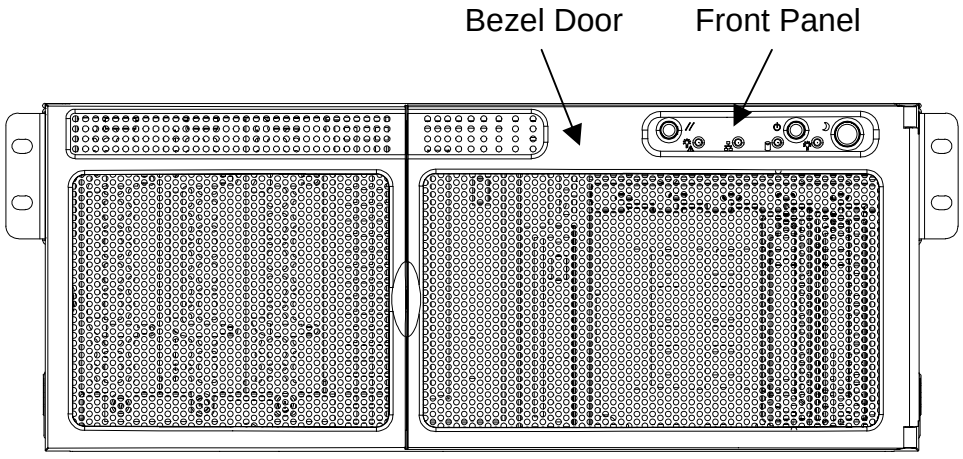

Figure 2-5: Front View of System

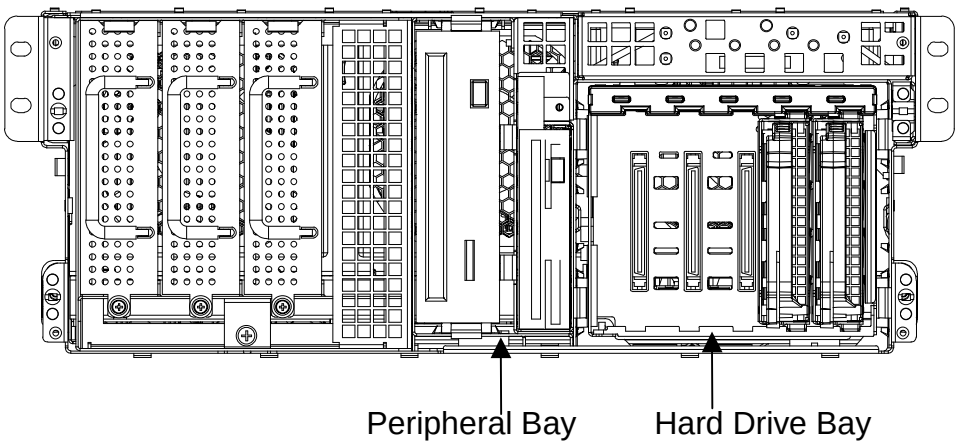

Figure 2-6: Front View of System (shown with bezel removed)

2.3.2 Front Panel

The front panel contains system control switches and status indicators. Front panel features are shown in Figure 2-7 and described in Table 2-2.

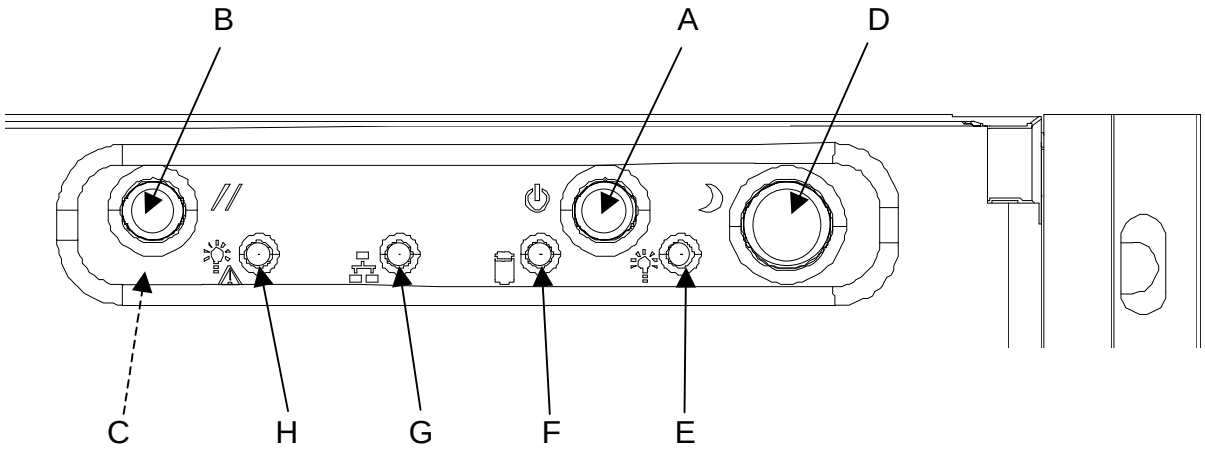

Figure 2-7: Front Panel Details

Table 2-2: Front Panel Features

Item	Feature	Description
Front Panel Switches		
A	Power switch	Toggles the system power.
B	Reset switch	Resets the system.
C	NMI switch (not visible)	Causes an NMI. Switch is located behind the front bezel to prevent inadvertent activation. Front bezel door must be opened to access switch. A narrow tool is required to activate the switch.
D	Sleep switch	Activates the sleep mode.
Front Panel LEDs		
E	Main power LED (green)	When continuously lit, indicates the presence of DC power in the server. The LED goes out when the power is turned off or the power source is disrupted. When flashing, it indicates the system is in ACPI sleep mode.
F	HDD activity LED (green)	Indicates any system hard drive activity.
G	NIC activity LED (green)	Indicates NIC activity.
H	General system fault LED (yellow)	Indicates any system failure condition.

2.3.3 Peripheral Bay

The peripheral bay consists of two bays for removable media:

- Half-height media bay – for a 5.25-inch CD-ROM or DAT drive
- Configurable media bay – bay can be configured as:
  - A 1/2-inch floppy drive and 1/2-inch CD-ROM drive
  - A 3.5-inch floppy drive

Note: Installing a hard disk drive in the 5.25-inch half-height bay is not recommended due to cooling and electromagnetic interference (EMI) constraints.

2.3.4 Hard Disk Drive Bay

The hard disk drive bay supports either five 3.5 inch by 1.0 inch, or three 3.5 inch by 1.6 inch hot-swap Ultra-160 SCSI technology SCA hard disk drives. These disk drives are accessed by opening the bezel door. The Ultra-160 SCSI technology hot-swap backplane provides industry standard 80-pin SCA-2 connectors. Ultra-160 SCSI technology SCA type or slower hard disk drives can be installed in this bay. The hot-swap backplane is designed to accept 10,000 RPM (and below) hard drives that consume up to 23 W of power.

Hard drive carriers that accommodate 3.5 inch wide by either 1.0 or 1.6 inch height drives are required as part of the hot-swap implementation. The carrier is attached to the drive with four fasteners and is retained in the chassis by a locking handle.

The LED above each hard drive displays the individual drive status:

- A continuously lit green LED indicates the presence of the hard drive and that the drive is powered on.
- A flashing green LED indicates hard drive activity.

- A continuously lit yellow LED indicates an asserted fault status on the hard drive.
- A flashing yellow LED indicates that a hard drive rebuild is in progress.

Note: Because all hard drives have different cooling, power and vibration characteristics, Intel will validate specific hard drive types in the SRKA4 server system.

The hot-swap SCSI backplane board-set performs the tasks associated with hot-swappable SCSI hard drives and enclosure (chassis) monitoring and management, as specified in the *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification,* Revision 1.00. The SAF-TE specified features supported by the hot-swap SCSI backplane board-set include, but are not limited to, the following:

- Monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages include: activate a drive fault indicator; power down a drive that has failed; and report backplane temperature.
- SAF-TE intelligent agent, which acts as proxy for "dumb" I^2C* devices (that have no bus mastering capability) during intrachassis communications.

This board set consists of two separate boards. The SCSI backplane board provides power distribution and SCSI interfacing of the hard drives. The SAF-TE board provides the SAF-TE features and hard drive failure indicators.

2.3.5 Rear View of Chassis

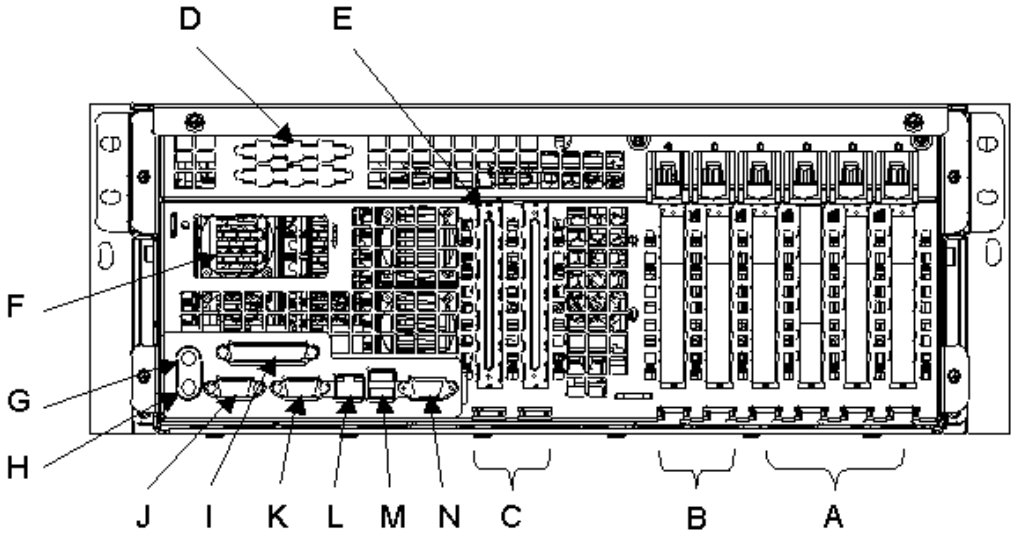

Figure 2-8: Rear View of System

Table 2-3: System Features - Rear

Item	Description
A	Four hot-plug 64-bit, 33-MHz PCI add-in board slots (P64-B1, P64-B2, P64-B3, P64-B4)
B	Two hot-plug 64-bit, 66-MHz PCI add-in board slots (P64-A1, P64-A2)
C	Two 32-bit, 33-MHz PCI add-in board slots (P32-1, P32-2)
D	Two optional external SCSI connector knockouts
E	Optional ICMB connectors in/out ICMB port 0, SEMCONN 6-pin connector ICMB port 1, SEMCONN 6-pin connector
F	AC input power connector
G	PS/2-compatible mouse port, 6-pin connector
H	PS/2-compatible keyboard port, 6-pin connector
I	PS/2-compatible parallel port (LPT), 25-pin bi-directional subminiature D connector
J	Serial port 1 (COM1), 9-pin RS-232 connector
K	Serial port 2 (COM2), 9-pin RS-232 connector
L	NIC RJ45 connector
M	USB ports 0 (upper) and 1 (lower), 4-pin connectors
N	Video connector

2.4 Internal Chassis Features

2.4.1 System Baseboard

Please refer to the *SKA4 Baseboard and Memory Board Technical Product Specification* for detailed description of the system baseboard.

2.4.2 Power Subsystem

The power supply modules are located in the power supply bay mounted towards the left front of the chassis. The power subsystem may contain up to three 350-W power supply modules and can be configured as follows:

- Three 350-W power supply modules installed, (2 + 1) power redundancy for maximally loaded system.
- Two 350-W power supply modules installed[1], non-redundant for maximally loaded system.
- Two 350-W power supply modules installed (see footnote below), (1 + 1) power redundancy for system loading not exceeding single power supply module requirements.
- One 350-W power supply module installed (see footnote below), non-redundant for system loading not exceeding single power supply module requirements.

When the system is configured with three power supply modules, the hot-swap feature allows the user to replace a failed power supply module without interrupting system functionality.

[1] Proper system cooling requires the population of all three (power supply bay) receptacles either by a power supply module or a filler panel.

Power from the power subsystem is carried to internal system boards and peripheral devices via discrete cables. Two 350-W power supply modules are capable of handling the worst case power requirements for a fully configured SRKA4 server system. This includes four Pentium III Xeon Slot-2 processors, 16 GB of memory and five hard drives at 23 W per drive (typical worst case 3.5 inch by 1.6 inch, 10k RPM drive).

The system baseboard contains three embedded voltage converters (two 5 V input and one 12 V input) and provides connectors for three VRM 8.3-compatible voltage converters. The converter input is +12 Vdc from the power subsystem. Each Pentium III Xeon slot-2 processor core requires its own converter and the L2 caches of these processors require half of a converter. The three embedded VRMs provide core voltage for processor 1 and power for the L2 cache on all processors. Additional processors require one VRM to be added for each processor added to the system.

The total power requirement for the SRKA4 server system exceeds the 240 VA energy hazard limit, which defines an operator-accessible area. As a result, only qualified technical individuals should access the processor, memory, and non-hot-plug I/O areas on the system baseboard while the system is energized.

Refer to *Section 4, Power Subsystem,* for detailed power specifications.

2.4.3 Cooling Subsystem

2.4.3.1 Description

All system components are cooled by a set of fans mounted in a fan bay near the middle of the chassis and in front of the e-bay. The fan bay is shown in Figure 2-9.

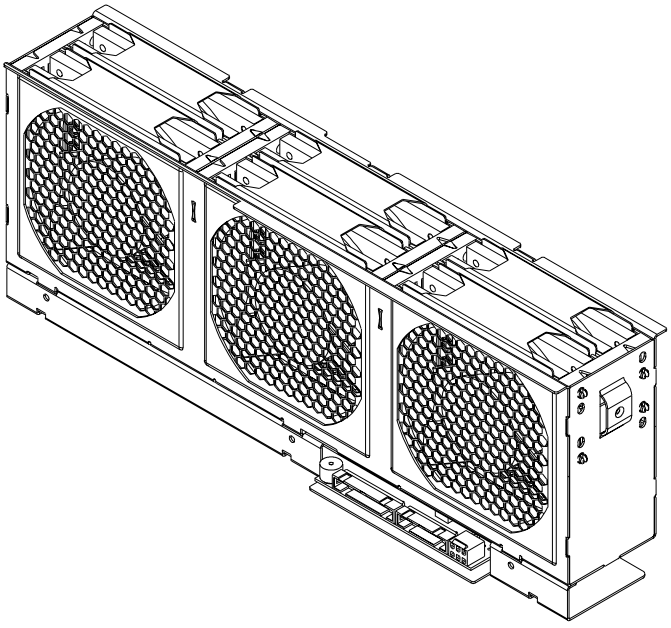

Figure 2-9: Fan Bay (shown with six fans installed)

The SRKA4 system is available in either a non-redundant, three-fan configuration or a redundant six-fan configuration.

Air flows in through the front bezel over the power supply bay, the peripheral bay and the hard disk drive bay, passes through the fan bay and the e-bay, and exhausts through the rear and left side of the chassis. Each fan provides tachometer signal output to the fan printed circuit board (PCB) to indicate a fan failure. Each fan also provides a fan-presence signal to the fan PCB.

2.4.3.2 Redundancy and Ambient Temperature Control

The fan PCB contains a pulse-width-modulation (PWM) circuit, which cycles the 12 Vdc fan voltage to provide quiet operation when system ambient temperature is low, and there are no fan failures. Under normal room ambient conditions (less than 30°C) the fan power circuit supplies an effective fan voltage of 9.0 Vdc. If a fan fails or if the room ambient temperature exceeds 30°C, the fan control circuit stops cycling and delivers 12 Vdc. Following a room temperature excursion above 30°C the fan voltage does not reenter PWM mode until the room temperature drops below 28°C and all fans are operational.

2.4.3.3 Cooling Summary

The fan bay configured with three fans is sized to provide cooling for the following:

- Up to four Pentium III Xeon processors.
- 16 GB of SDRAM memory.
- Five 10,000 RPM hard drives.
- Eight PCI cards.
- Redundant, fully-loaded power subsystem.

The addition of three more fans to the fan bay supports full redundancy of the cooling subsystem. To ensure that all components remain within specification under all system environmental conditions, it is recommended that fan or power supply module hot-swap operations not exceed two minutes in duration.

2.4.4 PCI Hot-plug (PHP)

2.4.4.1 Description

PCI hot-plug (PHP) functionality provides a facility to add, remove, and replace PCI adapter cards in the PHP slots while the system is running. Below is a list of hot-plug scenarios:

- Add: The user can add a new adapter card to the system.
- Remove: The user can remove an adapter card from the system.
- Replace: The user can replace a PCI card with an identical card. The replacement card will use the same PCI resources assigned to the previous card.
- Upgrade: The user can replace the existing card with a new version of the card, which does not need to match the old card exactly.

Note: Support for PHP operations is OS dependent.

2.4.4.2 Hardware Components

Intel has licensed the hardware technology and methods for the implementation of PHP, which conform to the *PCI Hot-Plug Specification*. The implementation in the SRKA4 server is based upon a discrete hot-plug controller application specific integrated circuit (ASIC) developed by NEC. Additional components also are required. The basic components consist of:

- Power cycling hardware, which complies with the *PCI Local Bus Specification*, Revision 2.1.
- Bus isolation switches to physically disconnect the PHP capable card from the PCI bus. These switches are located on the hot-plug indicator board (HPIB) between each PHP PCI slot.
- Indicators (LEDs) located on the HPIB to provide service personnel with positive slot identification. These LEDs are visible when viewed from the rear of the system through the holes in the chassis.
- Protection hardware to isolate the live components of the system from the PCI card being inserted/removed. Mechanical barriers prevent access to the baseboard and memory components and between PCI cards. Each PHP PCI connector is limited to 240 VA.
- A controller element which controls the above hardware and provides an interface for system software.

2.4.4.3 Software Components

The main software components for the PHP system are described below.

2.4.4.3.1 Hot-plug User Interface

- Provides user with access to the hot-plug control panel.
- Receives user input and sends a request to the service layer.
- Displays the status of the PCI slot.
- Graphical user interface (GUI) and method for user access to PHP functions may vary with OS.

2.4.4.3.2 Hot-plug Service

- Mediates between the user interface and the hot-plug driver (which may be an ACPI control method), and also is responsible for configuring, loading and unloading the driver component.
- Responsible for powering down the adapter via standard system calls.
- Communicates to the hot-plug controller through hot-plug primitives.
- Reports adapter status to the hot-plug user interface.

2.4.4.3.3 Hot-plug Driver

- Executes request from the service layer.
- Drives the hot-plug controller.

2.4.4.3.4 BIOS

- Responsible for initialization of the hot-plug hardware components.

2.4.4.3.5 Adapter Drivers

- For Microsoft* Windows NT*, the driver must be *Advanced Configuration And Power Interface Specification*, Revision 1.0b (ACPI) compliant and provide (at a minimum) the device states D0 and D3.
- For SCO* Unixware*, the driver must be DDI-8 compliant.
- For Novell* Netware*, the driver must comply with the *NetWare Peripheral Architecture (NWPA) 2.32* and *Open Data-link Interface (ODI) 3.2* specifications.

An adapter card should be "qualified" by Intel to insure proper hot-plug functionality. For current information on qualified adapter cards, see the *SRKA4 Server System Validation Summary*.

2.5 Server Management

The SKA4 server management architecture features a BMC, which autonomously monitors server status and provides the interface to server management control functions. This controller is responsible for controlling system power and resets; monitoring voltages, temperatures, and fans; and communicating with secondary controllers on its Intelligent Platform Management Bus (IPMB).

The functions of each controller are summarized in the following sections. The firmware for all of the controllers is field upgradeable using the Server Management Firmware Update Utility.

2.5.1 Baseboard Management Controller

The BMC on the SKA4 server baseboard provides server management monitoring capabilities. Associated with the BMC is a flash memory that holds the operational code, sensor data records (SDR), and system event log (SEL). A serial EEPROM holds the BMC configuration defaults and field replaceable unit (FRU) information. The various server management functions provided by the BMC are as follows:

- Baseboard voltage monitoring
- Fan failure detection
- Fan speed control
- Processor voltage monitoring
- Processor presence detection
- Processor internal error (IERR) monitoring
- Fault resilient booting (FRB)
- Processor disable control
- Watchdog timer
- Periodic system management interrupt (SMI) timer
- I^2C master controller for the Intelligent Platform Management Bus (IPMB)
- Two private I^2C management bus interfaces

- Server management software (SMS) and server management mode (SMM) IPMB message receiver.
- Event message receiver.
- System event log management and access.
- Sensor data record repository management and access.
- Processor nonmaskable interrupt monitoring.
- Processor SMI monitoring.
- Time-stamp clock.
- Secure mode, video blank, and floppy write protect.
- Software front panel NMI generation.

2.5.2 Hot-swap Controller

The hot-swap controller (HSC) on the Ultra-160 SCSI technology hot-swap backplane is connected to other system boards via the IPMB. The HSC provides server management information through both the IPMB and the SCSI Accessed Fault-Tolerant Enclosures (SAF-TE). SAF-TE is an industry standard for communicating drive and slot status.

The HSC:

- Implements the SAF-TE command set accessed through SCSI
- Provides an IPMB path for drive presence, drive fault status, backplane temperature and fan failure
- Controls the fault lights and drive power on the SRKA4 server system hot-swap backplane
- Controls drive power on and off, facilitating hot swapping of drives

2.6 Specifications

2.6.1 Physical Specifications

Table 2-4 describes the physical specifications of the SRKA4 system.

Table 2-4: Dimensions and Weight

Height	7 inches (178 mm)
Width	17.5 inches (445 mm)
Depth	26.5 inches (673 mm)
Front clearance	3 inches (76 mm)(inlet airflow<35°C/95°C)
Side clearance	1 inches (25 mm)
Rear clearance	6 inches (152 mm)no airflow restriction
Weight	57 lbs. minimum configuration 88 lbs. maximum configuration

2.6.2 MTBF Specifications

The basic system MTBF as calculated with an ambient temperature of 40°C is 20,216 hours. The calculation is based on the basic system configuration and component MTBF as show in Table 2-5. The MTBF for a fully configured system (without add-in cards) is 9,759 hours as shown in Table 2-6.

Table 2-5: MTBF Calculation for Basic System

Sub Assembly Description	Sub Assy QTY	Assy Temp. Accel. Valid? Drives=0	Sub Assy MTBF Quote (hrs)	Sub Assy Temp Quote (C)	Sub Assy Duty Cycle Quote (%)	Assy Temp. Mapped inside System?	Duty Cycle as used in Sys (%)	Sub Assy temp in sys (C)	Sub Assy MTBF from Quote (hrs)	Assy Quote to Intern Temp Acc Fact	Sub Assy Dty Cyc Acc Fact	Total Sub Assy MTBF (in hrs)	Total Sub Assy Failure Rate (FITs)
CPU Baseboard	1	Yes	70,803	55	100	No	100	55	70,803	1.000	1.00	70,803	14,124
CPU	1	Yes	1,000,000	55	100	No	100	55	1,000,000	1.000	1.00	1,000,000	1,000
VRM	0	Yes	512,847	55	100	No	100	55	NA	1.000	1.00	NA	NA
Mem board	1	Yes	337,344	55	100	No	100	55	337,344	1.000	1.00	337,344	2,964
Front panel board	1	Yes	2,416,685	55	100	No	100	55	2,416,685	1.000	1.00	2,416,685	414
Hotswap BP	1	Yes	1,059,401	55	100	No	100	55	1,059,401	1.000	1.00	1,059,401	944
IO RISER	1	Yes	803,013	55	100	No	100	55	803,013	1.000	1.00	803,013	1,245
Fan distribution	1	Yes	1,529,029	55	100	No	100	55	1,529,029	1.000	1.00	1,529,029	654
Termination board pcard	3	Yes	8,761,938	55	100	No	100	N/A	8,761,938	NA	NA	2,920,646	342
Hotplug indicator board	1	Yes	4,759,638	55	100	No	100	55	4,759,638	1.000	1.00	4,759,638	210
CD ROM IDE	1	No	100,000	50	25	No	5	55	100,000	1.000	5.00	500,000	2,000
Hard Drive	1	No	1,000,000	55	100	No	100	55	1,000,000	1.000	1.00	1,000,000	1,000
Power supply	1	Yes	100,000	50	100	No	100	55	100,000	0.800	1.00	79,991	12,501
1.44MB 3.5" FDU	1	No	81,000	35	5	No	1	55	81,000	1.000	5.00	405,000	2,469
64 Meg DIMM	4	Yes	1,358,496	55	100	No	100	55	1,358,496	1.000	1.00	339,624	2,944
FAN	3	No	450,833	40	100	No	100	55	450,833	1.000	1.00	150,278	6,654
Total Failure Rate (FIT)													49,467
MTBF hours													20,216

Table 2-6: MTBF Calculation for Fully Configured System

Sub Assembly Description	Sub Assy QTY	Assy Temp. Accel. Valid? Drives=0	Sub Assy MTBF Quote (hrs)	Sub Assy Temp Quote (C)	Sub Assy Duty Cycle Quote (%)	Assy Temp. Mapped inside System?	Duty Cycle as used in Sys (%)	Sub Assy temp in sys (C)	Sub Assy MTBF from Quote (hrs)	Assy Quote to Intern Temp Acc Fact	Sub Assy Dty Cyc Acc Fact	Total Sub Assy MTBF (in hrs)	Total Sub Assy Failure Rate (FITs)
CPU Baseboard	1	Yes	70,803	55	100	No	100	55	70,803	1.000	1.00	70,803	14,124
CPU	4	Yes	1,000,000	55	100	No	100	55	1,000,000	1.000	1.00	250,000	4,000
VRM	3	Yes	512,847	55	100	No	100	55	512,847	1.000	1.00	170,949	5,850
Mem board	1	Yes	337,344	55	100	No	100	55	337,344	1.000	1.00	337,344	2,964
Front panel board	1	Yes	2,416,685	55	100	No	100	55	2,416,685	1.000	1.00	2,416,685	414
Hotswap BP	1	Yes	1,059,401	55	100	No	100	55	1,059,401	1.000	1.00	1,059,401	944
IO RISER	1	Yes	803,013	55	100	No	100	55	803,013	1.000	1.00	803,013	1,245
Fan distribution	1	Yes	1,529,029	55	100	No	100	55	1,529,029	1.000	1.00	1,529,029	654
Termination board pcard	0	Yes	8,761,938	55	100	No	100	NA	NA	NA	NA	NA	NA
Hotplug indicator board	1	Yes	4,759,638	55	100	No	100	55	4,759,638	1.000	1.00	4,759,638	210
CD ROM IDE	1	No	100,000	50	25	No	5	55	100,000	1.000	5.00	500,000	2,000
Hard Drive	5	No	1,000,000	55	100	No	100	55	1,000,000	1.000	1.00	200,000	5,000
Power supply	3	Yes	100,000	50	100	No	100	55	100,000	0.800	1.00	26,664	37,504
1.44MB 3.5" FDU	1	No	81,000	35	5	No	1	55	81,000	1.000	5.00	405,000	2,469
64 Meg DIMM	16	Yes	1,358,496	55	100	No	100	55	1,358,496	1.000	1.00	84,906	11,778
FAN	6	No	450,833	40	100	No	100	55	450,833	1.000	1.00	75,139	13,309
Total Failure Rate (FIT)													102,465
MTBF hours													9,759

2.6.3 Operational Specifications

Table 2-7 and Table 2-8 detail the system configurations used to determine operational power budgets and power consumed. Table 2-8 lists operational power budget figures for a minimum configuration, a maximum configuration, and maximum available from the system.

Table 2-7: SRKA4 Configurations for Power Budget

	Min Configuration	Max Configuration
Processors	One Pentium® III Xeon™ 2.8V (650MHz/1M & 2M)	Four Pentium® III Xeon™ 2.8V (650MHz/1M & 2M)
VRM	None	Three 12V VRMs
Add-in Adaptors	None	Two PCI (5V) High (5A) Four PCI (5V) Typical (3A) Two PCI (5v) Low (1A)
Hard Drives	One Quantum* 18GB 1"	Five Seagate* 18GB LP 1"
Fans	Three SRKA4 Fans	Six SRKA4 Fans
5 ¼ Drive Bay	None	Quantum* DLT 7000
3.5 Drive Bay	1/2" Floppy + 1/2" CDROM	1/2" Floppy + 1/2" CDROM

Table 2-8: SRKA4 Operational Power Budget

	Max Available	Min Configuration	Max Configuration
Inrush Current (Max ½ Cycle)	70A peak at 90 degree phase 264VAC input		
Power supply efficiency	62%		
VA Rating (Max)	890VA		
+3.3V	50.00A	22.26A	34.06A
+5V	58.00A	15.62A	47.72A
+12V	22.00A	3.74A	19.45A
-12v	0.50A	0.02A	0.20A
System Wattage	631.00W	204.90W	592.80W
BTU/Hr	3471 BTU	1127 BTU	3260 BTU

NOTE:

The total combined wattage consumed on the +3.3V and +5V supply lines cannot exceed 351 watts. The total wattage per PCI slot cannot exceed 25 watts. The total combined wattage for all PCI slots cannot exceed 120 watts.

The formula for BTU calculation from system wattage to BTU is:

```
System wattage / power efficiency x 3.41 = BTU
```

BTU calculations to determine the proper system cooling requirements are determined based on the system configuration. The minimum and maximun system configuration calculations for BTU are as follows:

MAX Available: `631 / .62 x 3.41 = 3471 BTU`

MIN Configuration: `204.90 / .62 x 3.41 = 1127 BTU`

MAX Configuration: `592.80 / .62 x 3.41 = 3260 BTU`

2.7 System Software

2.7.1 BIOS, Firmware, FRUSDR

In order for the system to function, certain system software must be installed and properly configured. This system software includes the BIOS, firmware (BMC and HSC), and FRUSDR data.

The BIOS is installed using the iFLASH utility provided with the BIOS image. Firmware operational code is installed with the FWUPDATE utility. FRUSDR records are installed with the FRUSDR utility.

2.7.2 Load Order

In general, a system should be updated in the order shown below. The BIOS and FRUSDR can be updated independently, but the BMC code can not be. If the BMC code is updated, the

FRUSDR must be updated (or reloaded) after the BMC code update. This is because the FRUSDR data records are cleared whenever the BMC code is written. Refer to the specific release notes accompanying a BIOS, firmware, or FRUSDR version to determine if there are any specific installation requirements.

The recommended load order for system software is:

- Firmware (BMC or HSC)
- FRUSDR
- BIOS
- Clear CMOS

2.7.3 BIOS Recovery Boot

If the system BIOS becomes corrupted, booting the system will likely not be possible. To recover from this condition a BIOS Recovery Boot feature is availible. To enable Recovery Boot a jumper on the baseboard must be enabled. The jumper can be found in jumper block J9F2 and is shown in Figure 2-10.

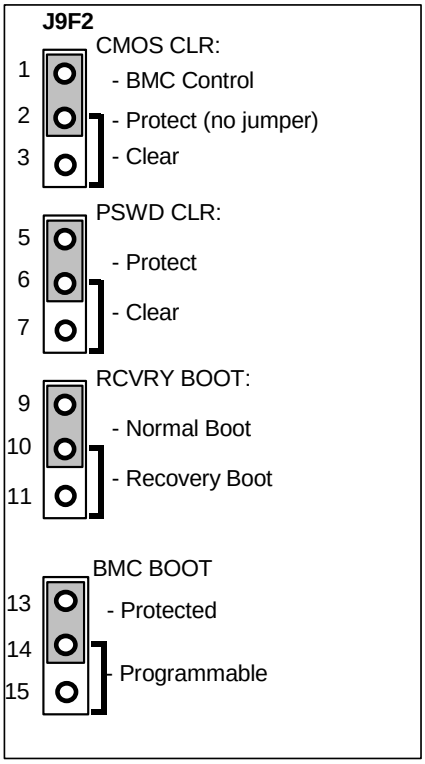

Figure 2-10. SKA4 Boot Jumpers

The BIOS is in normal boot mode when pins 9 and 10 of J9F2 are jumpered (default). If the normal BIOS is corrupted and the user is not able to load it from the floppy disk, the jumper can be installed between pins 10 and 11 of J9F2. This enables the system to boot from the Recovery BIOS. This feature expects a fresh copy of the normal BIOS to be located on a floppy disk present in the floppy drive. Follow the below procedure to reload BIOS using the Recovery Boot.

1. Create a system BIOS diskette.
2. Turn system off.
3. Move the Recovery Boot jumper to pins 10 and 11.
4. Turn the system on with the BIOS diskette in drive A: (note: the diskette must have system boot files on it).
5. No video will be available. A single beep indicates to OS has been loaded and the BIOS recovery is in process. Four beep codes indicates that the system could not boot from the diskette. Continuous beeps indicates that the incorrect BIOS files are being used.
6. Two beeps will be heard when Recovery Boot has finished successfully.
7. Turn the system off.
8. Move the Recovery Boot jumper to pins 9 and 10.
9. Clear CMOS.

3. Cables and Connectors

This chapter describes interconnections between the various components of the SRKA4 server system. This chapter also includes an overview diagram of the SRKA4 server system interconnections, as well as tables describing the signals and pinouts for the 1/2-inch peripheral adapter boards. Refer to the appropriate board External Product Specification (EPS) for other connector signal descriptions and pinouts.

3.1 Interconnect Block Diagram

Figure 3-1 on the following page shows interconnections for all of the boards used in the SRKA4 server system.

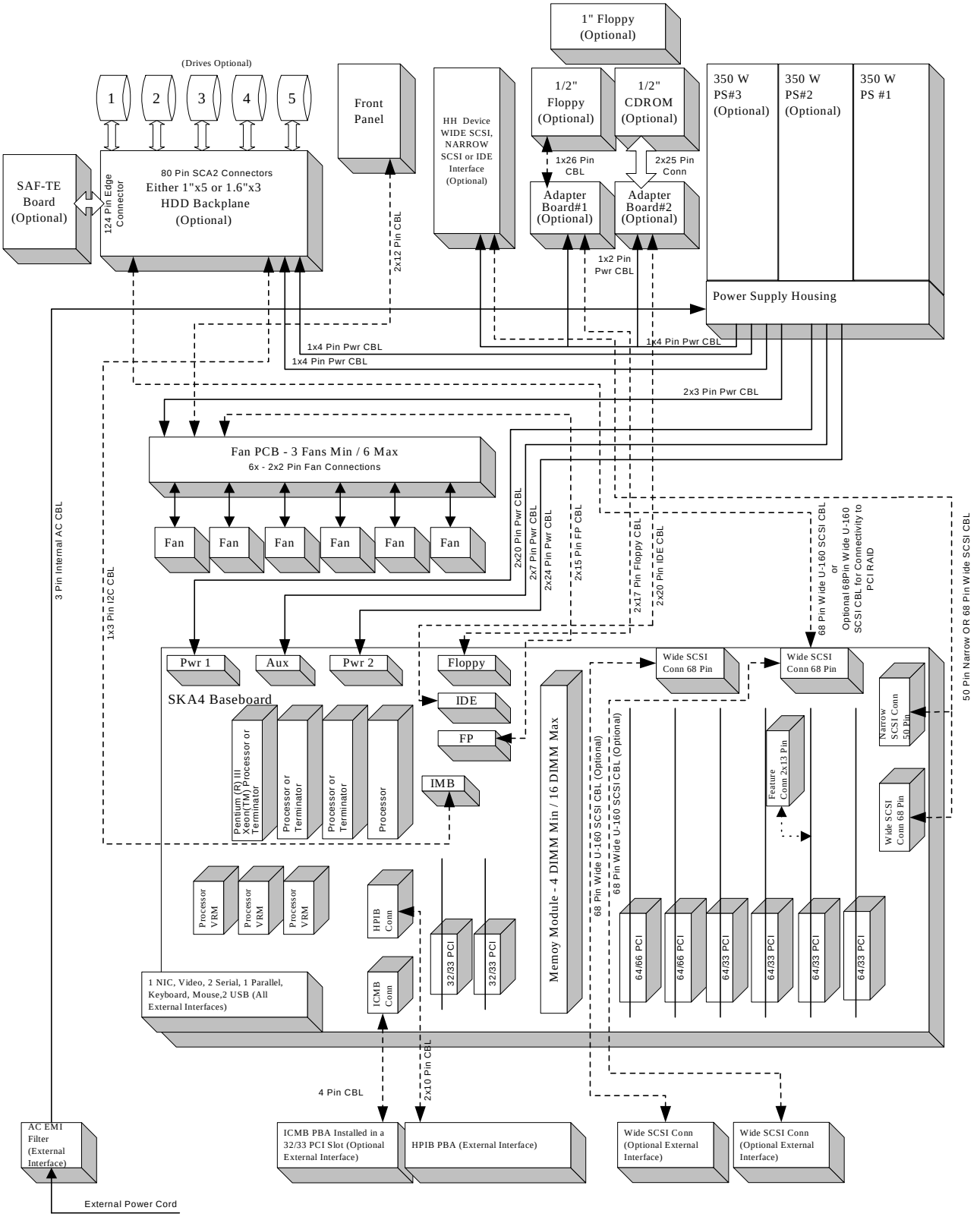

Figure 3-1: SRKA4 System Interconnect Block Diagram

3.2 Cables

Table 3-1 through Table 3-3 list flat ribbon cables and wire bundles that are used in the assembly of the SRKA4 Server System.

Table 3-1: Flat Ribbon Cables

Quantity	Number of Pins	Type	Path
1	68	Wide SCSI cable	From the baseboard to the hard disk drive backplane.
1	30	FCB cable	From the baseboard to the Fan Carrier Board (FCB).
1	24	Front panel cable	From the FCB to the front panel board.
1	34	Floppy drive cable	From the baseboard to the floppy drive.
1	20	HPIB cable	From the baseboard to the Hot-plug Indicator Board (HPIB).

Table 3-2: Wire Bundles

Quantity	Number of Pins	Type	Path
3	4	Power cable	From the power supply assembly to the peripheral bay.
1	3	I2C cable	From the baseboard to the hard drive bay.
1	20	Power cable	From the midplane to the peripheral bay backplane.

Table 3-3: Optional Cables

Quantity	Number of Pins	Type	Path
1	50	Narrow SCSI cable	From the baseboard to the 5-1/4" device bay.
1	68	Wide SCSI cable	From the baseboard to the rear of the chassis (external drive support).
1	4	Power cable	From a peripheral power connector to a half-height floppy and CD-ROM.
1	40	IDE cable	From the baseboard to an IDE CD-ROM.

3.3 Externally Accessible Connectors

The following section describes the signals and pinouts for various connectors on the SKA4 board set.

3.3.1 Keyboard and Mouse Ports

These identical PS/2 compatible ports share a common housing. The connector on top is the mouse and one on the bottom is the keyboard.

Table 3-4: Keyboard and Mouse Ports

Mouse		Keyboard	
Pin	**Signal**	**Pin**	**Signal**
1	MSEDAT (mouse data)	1	KEYDAT (keyboard data)
2	No connection	2	No connection
3	GND (ground)	3	GND (ground)
4	Fused VCC (+5 V)	4	Fused VCC (+5 V)
5	MSECLK (mouse clock)	5	KEYCLK (keyboard clock)
6	No connection	6	No connection

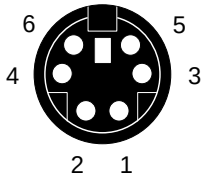

Figure 3-2: Keyboard or Mouse Connector

3.3.2 Serial Ports

The baseboard provides two RS-232C serial ports (COM1 is to the left, COM2 is to the right). These are D-subminiature, 9-pin connectors. Each serial port can be enabled separately with the configuration control provided on the baseboard.

The COM2 serial port can be used either as an emergency management port (EMP) or as a normal serial port. As an emergency management port, COM2 is used as a communication path by the server management RS-232 connection to the BMC on the baseboard. This provides a level of emergency management through an external modem, and also enables console redirection.

Table 3-5: Serial Port Connector

Pin	Signal
1	DCD (carrier detect)
2	RXD (receive data)
3	TXD (transmit data)
4	DTR (data terminal ready)
5	GND
6	DSR (data set ready)
7	RTS (request to send)
8	CTS (clear to send)
9	RIA (ring indicator)

Figure 3-3: Serial Port Connector

3.3.3 Parallel Port

The IEEE 1284-compatible parallel port, used primarily for a printer, sends data in parallel format. The parallel port is accessed through a D-subminiature, 25-pin connector.

Table 3-6: Parallel Port Connector

Pin	Signal	Pin	Signal
1	STROBE_L	14	AUFDXT_L (auto feed)
2	Data bit 0	15	ERROR_L
3	Data bit 1	16	INIT_L (initialize printer)
4	Data bit 2	17	SLCTIN_L (select input)
5	Data bit 3	18	GND (ground)
6	Data bit 4	19	GND
7	Data bit 5	20	GND
8	Data bit 6	21	GND
9	Data bit 7	22	GND
10	ACK_L (acknowledge)	23	GND
11	BUSY	24	GND
12	PE (paper end)	25	GND
13	SLCT (select)		

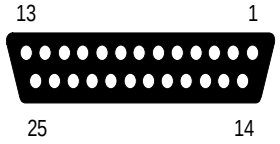

Figure 3-4: Parallel Port Connector

3.3.4 Video Port

The video port interface is a standard VGA compatible, 15-pin connector. On-board video is supplied by an ATI* Rage* 2C_VT4 video controller with 2 MB of onboard video SGRAM.

Table 3-7: Video Connector

Pin	Signal
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND
6	GND
7	GND
8	GND
9	Fused VCC (+5 V)
10	GND
11	No connection
12	DDCDAT
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	DDCCLK

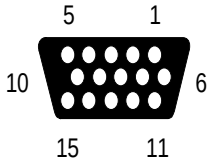

Figure 3-5: Video Connector

3.3.5 USB Interface

The baseboard provides two stacked USB ports (Port 0 on top, Port 1 on bottom). The built-in USB ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports.

Table 3-8: Dual USB Connector

Pin	Signal
A1	Fused VCC (+5 V w/over-current monitor of both ports 0 and 1)
A2	DATAL0 (differential data line paired with DATAH0)
A3	DATAH0 (differential data line paired with DATAL0)
A4	GND
B1	Fused VCC (+5 V w/over-current monitor of both ports 0 and 1)
B2	DATAL1 (differential data line paired with DATAH1)
B3	DATAH1 (differential data line paired with DATAL1)
B4	GND

Figure 3-6: Dual USB Connector

3.3.6 ICMB Connectors

The external Intelligent Chassis Management Bus (ICMB) provides external access to IMB devices within the chassis. This makes it possible to externally access chassis management functions, alert logs, post-mortem data, etc. It also provides a mechanism for chassis power control. As an option the server can be configured with an ICMB adapter board to provide two SEMCONN 6-pin connectors to allow daisy chained cabling.

Table 3-9: ICMB Connector

Pin	Signal
1	No connection
2	No connection
3	B (negative)
4	A (positive)
5	No connection
6	No connection

Figure 3-7. : ICMB Connector

3.3.7 Ethernet Connector

The system supports one Intel® 82559-based onboard Ethernet connection. This controller drives LEDs on the upper edge of the connector. The green LED (left) indicates network connection when on and transmit/receive (TX/RX) activity when blinking. The yellow LED (right) indicates 100 Mbps operation when lit.

Table 3-10: Ethernet Connector

Pin	Signal
1	TX+
2	TX-
3	RX+
4	NIC termination
5	NIC termination
6	RX-
7	NIC termination
8	NIC termination
9	Speed LED signal
10	+3.3 V standby (for LED)
11	Activity LED signal
12	+3.3 V standby (for LED)
13	GND
14	GND

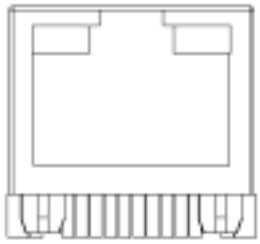

Figure 3-8: Ethernet Connector

3.3.8 Internal SCA-2 HDD Connector

An SCA-2 connector is used on the primary side of the HDD backplane. The pinout is the same as that for SCA-1. The connector pin assignment is shown in table 3-11.

Table 3-11: SCA-2 Connector

80-pin Connector Contact and Signal Name			80-pin Connector Contact and Signal Name		
1	12 V Charge	(L)	(L)	12 V Ground	41
2	12 V	(S)	(L)	12 V Ground	42
3	12 V	(S)	(L)	12 V Ground	43
4	12 V	(S)	(S)	Mated 1	44
5	Reserved/ESI-1	(S)	(L)	-EFW	45
6	Reserved/ESI-2	(S)	(L)	DIFFSNS	46
7	-DB(11)	(S)	(S)	+DB(11)	47
8	-DB(10)	(S)	(S)	+DB(10)	48
9	-DB(9)	(S)	(S)	+DB(9)	49
10	-DB(8)	(S)	(S)	+DB(8)	50
11	-I/O	(S)	(S)	+I/O	51
12	-REQ	(S)	(S)	+REQ	52
13	-C/D	(S)	(S)	+C/D	53
14	-SEL	(S)	(S)	+SEL	54
15	-MSG	(S)	(S)	+MSG	55
16	-RST	(S)	(S)	+RST	56
17	-ACK	(S)	(S)	+ACK	57
18	-BSY	(S)	(S)	+BSY	58
19	-ATN	(S)	(S)	+ATN	59

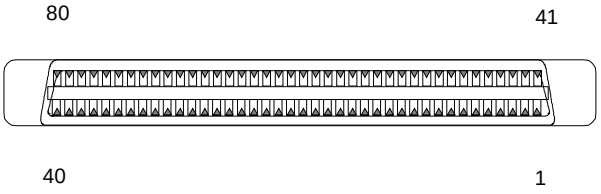

Figure 3-9: SCA-2 Connector

20	-DB(P)	(S)	(S)	+DB(P)	60
21	-DB(7)	(S)	(S)	+DB(7)	61
22	-DB(6)	(S)	(S)	+DB(6)	62
23	-DB(5)	(S)	(S)	+DB(5)	63
24	-DB(4)	(S)	(S)	+DB(4)	64
25	-DB(3)	(S)	(S)	+DB(3)	65
26	-DB(2)	(S)	(S)	+DB(2)	66
27	-DB(1)	(S)	(S)	+DB(1)	67
28	-DB(0)	(S)	(S)	+DB(0)	68
29	-DB(P1)	(S)	(S)	+DB(P1)	69
30	-DB(15)	(S)	(S)	+DB(15)	70
31	-DB(14)	(S)	(S)	+DB(14)	71
32	-DB(13)	(S)	(S)	+DB(13)	72
33	-DB(12)	(S)	(S)	+DB(12)	73
34	5V	(S)	(S)	Mated 2	74
35	5V	(S)	(L)	5 V Ground	75
36	5V Charge	(L)	(L)	5 V Ground	76
37	Spindle Sync	(L)	(L)	Active LED Out	77
38	MTRON	(L)	(L)	DLYD_START	78
39	SCSI ID (0)	(L)	(L)	SCSI ID (1)	79
40	SCSI ID (2)	(L)	(L)	SCSI ID (3)	80

3.3.9 External Ultra-160 SCSI Technology

As an option, the server system can support a shielded external SCSI connection. This connection is on Channel B of the Adaptec AIC7899 Ultra-160 SCSI controller. Channel A of this controller is connected to the internal hard drive backplane.

Table 3-12: SCSI Connector

Signal Name	Pin	Pin	Signal Name
DP(12)	1	35	DM(12)
DP(13)	2	36	DM(13)
DP(14)	3	37	DM(14)
DP(15)	4	38	DM(15)
DAPHP	5	39	DAPHM
DP(0)	6	40	DM(0)
DP(1)	7	41	DM(1)
DP(2)	8	42	DM(2)
DP(3)	9	43	DM(3)
DP(4)	10	44	DM(4)
DP(5)	11	45	DM(5)
DP(6)	12	46	DM(6)
DP(7)	13	47	DM(7)
DAPLP	14	48	DAPLM

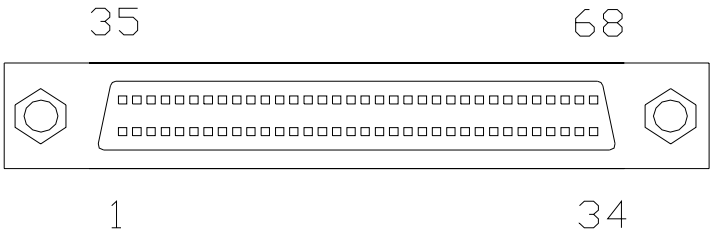

Figure 3-10: SCSI Connector

Signal Name	Pin	Pin	Signal Name
GND	15	49	GND
DIFFSENSE	16	50	GND
TERMPWR	17	51	TERMPWR
TERMPWR	18	52	TERMPWR
NC	19	53	NC
GND	20	54	GND
ATNP	21	55	ATNM
GND	22	56	GND
BSYP	23	57	BSYM
ACKP	24	58	ACKM
RSTP	25	59	RSTM
MSGP	26	60	MSGM
SELP	27	61	SELM
CDP	28	62	CDM
REQP	29	63	REQM
IOP	30	64	IOM
DP(8)	31	65	DM(8)
DP(9)	32	66	DM(9)
-DP(10)	33	67	-DM(10)
-DP(11)	34	68	-DM(11)

3.3.10 AC Power Input

A single IEC320-C13 receptacle is provided at the rear of the server. It is recommended that an appropriately sized power cord and AC main be used. Refer to *Section 4, Power Subsystem,* for system voltage, frequency, and current draw specifications.

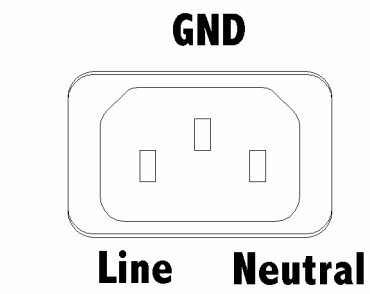

Figure 3-11: AC Power Input Connector

3.4 Peripheral Adapter Boards and Connectors

The peripheral adapter boards convert the 50-pin JAE and flexible flat circuit (FFC) signal interface connectors of the 1/2 inch-slim line peripherals to a standard 40-pin IDE and 34-pin

floppy cable pinouts. Two unique boards are required, one for the floppy and one for the CD-ROM.

The CD-ROM peripheral connector is an 8 mm, 50-pin JAE receptacle, the power connector is a 3 mm Molex* Micro-Fit and the cable interface is a standard .100" center-line IDE latching header (with pin #20 pulled).

The floppy peripheral connection is a short length of FFC, the power connector is a right angle, four position header and the cable interface is a standard right angle, floppy header (with pin #3 pulled).

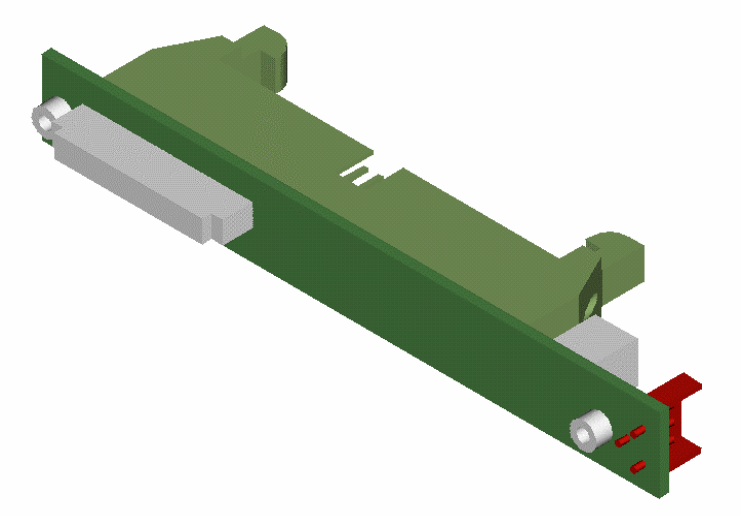

Figure 3-12: CD-ROM Adapter Board

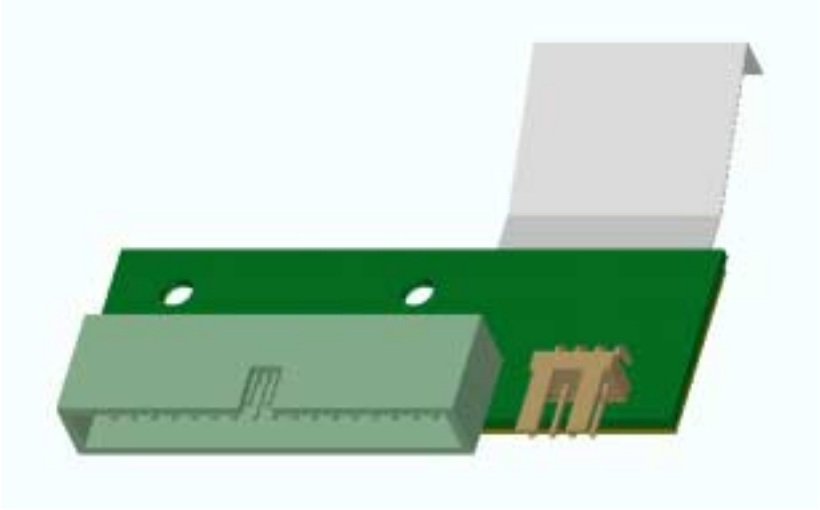

Figure 3-13: Floppy Adapter Board

3.4.1 CD-ROM Connectors

The 40-pin connector for the CD-ROM adapter board is the standard IDE pinout, as shown in Table 3-13.

Table 3-13: CD-ROM Adapter Board, 40-Position, IDE Connector

Pin	Signal	Pin	Signal
1	RSTDRV	2	GROUND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD1
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GROUND	20	KEY PIN
21	DRQ	22	GROUND
23	DIOW	24	GROUND
25	DIOR	26	GROUND
27	IORDY	28	CSEL
29	DACK	30	GROUND
31	IRQ	32	No Connection
33	DA1	34	No Connection
35	DA0	36	DA2
37	CS1P_L	38	DS3P_L
39	DHACT_L	40	GROUND

Table 3-14: CD-ROM Adapter Board Power Connector

Pin	Signal
1	GND
2	+5 Power

Table 3-15: Audio Connector

Pin	Signal
1	Audio Left
2	GND
3	Audio Right

Table 3-16: CD-ROM JAE Connector Pinout

Pin	Signal	Signal	Pin

Pin	Signal	Signal	Pin
1	Audio L-Ch	Audio R-Ch	2
3	Audio GND	GND	4
5	RESET-	DD8	6
7	DD7	DD9	8
9	DD6	DD10	10
11	DD5	DD11	12
13	DD4	DD12	14
15	DD3	DD13	16
17	DD2	DD14	18
19	DD1	DD15	20
21	DD0	DMARQ	22
23	GND	/DIOR	24
25	DIOW-	GND	26
27	IORDY	/DMACK	28
29	INTRQ	/IOCS16	30
31	DA1	/PDIAG	32
33	DA0	DA2	34
35	/CS1FX	/CS3FX	36
37	/DASP	+5V	38
39	+5V	+5V	40
41	+5V	+5V	42
43	GND	GND	44
45	GND	GND	46
47	CSEL	GND	48
49	RESERV	RESERV	50

3.4.2 Floppy Connectors

Table 3-17: 34-Position Floppy Connector Pinout

Pin	Signal	Signal	Pin
1	NC	HD IN/HD Out/Open	2
3	NC	N/C	4
5	NC	N/C	6
7	GND	FD_INDEX_L	8
9	GND	Drive Select 0	10
11	GND	Drive Select 1	12
13	GND	N/C	14
15	GND	Motor On	16
17	GND	Direction Select	18
19	GND	STEP	20
21	GND	Write Data	22
23	GND	Write Gate	24
25	GND	Track 00	26

Pin	Signal	Signal	Pin
27	GND	Write Protect	28
29	GND	Read Data	30
31	GND	Side One Select	32
33	GND	Disk Change/Ready	34

Table 3-18: Floppy Adapter Board Power Connector

Pin	Signal
1	+5 Power
2	GND
3	GND
4	No Connection

Table 3-19: FFC Cable Pinout

Pin	Signal	Signal	Pin
1	+5V	INDEX	2
3	+5V	DRIVE SELECT	4
5	+5V	DISK CHANGE	6
7	NC	READY	8
9	HD OUT (HD AT HIGHT LEVEL)	MOTOR ON	10
11	NC	DIRECT SELECT	12
13	NC	STEP	14
15	GND	WRITE DATA	16
17	GND	WRITE GATE	18
19	GND	TRACK 00	20
21	NC	WRITE PROTECT	22
23	GND	READ DATA	24
25	GND	SIDE ONE SELECT	26

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4. Power Subsystem

This chapter defines the features and functionality of the switching power subsystem.

4.1 Features

- 630 W output capability in full AC input voltage range.
- Power good indication LEDs.
- Predictive failure warning.
- External cooling fans with multispeed capability.
- Remote sense of 3.3 V, 5 V, and 12 Vdc outputs.
- AC_OK circuitry for brown out protection and recovery.
- Built-in load sharing capability.
- Built-in overloading protection capability.
- Onboard field replaceable unit information.
- I^2C interface for server management functions.
- Integral handle for insertion/extraction.

4.2 Overview

The SRKA4 server system uses a universal input switching power subsystem, which provides up to 630 W DC with power factor corrected AC input and with current and remote sense regulation.

The power subsystem consists of up to three 350-W power supply modules. Each power supply module can be used as a single module, or with its DC outputs paralleled with one or two other identical modules to form a non-redundant or (2+1) redundant power subsystem respectively, with operating replacement (hot-swap) capability. All power supply module connectors, including AC and DC connectors, accommodate “blind mating.”

The power subsystem has four externally enabled outputs, and one +5 V standby output at 2.0 A. The +5 Vdc standby output is present whenever AC power is applied. The four externally enabled outputs have the following ratings:

Single Power Supply Module	Power Subsystem (2 or 3 modules)
+3.3 Vdc at 28 A†	+3.3 Vdc at 50 A††
+5 Vdc at 32 A†	+5 Vdc at 58 A††
+12 Vdc at 12 A with 15 A peak	+12 Vdc at 22 A with 28 A peak†††
-12 Vdc at 0.5 A	-12 Vdc at 0.5 A

Notes:

† The total combined output power of the +3.3 V and +5 V channels shall not exceed 195 W.

†† The total combined output power of the +3.3 V and +5 V channels shall not exceed 351 W.

††† Maximum current drawn on the +12V output from the power subsystem shall not exceed 28 A for greater than 12 seconds.

4.3 Mechanical Interface

4.3.1 Mechanical Outline

The server system's mechanical outline and dimensions are shown in Figure 4-1 and Figure 4-2. The unit of measurement in the drawings is inches. The power subsystem enclosure has dimensions of 168.9 mm (6.65") H X 170.2 mm (6.7") W X 228.6 mm (9.0") D. The following mechanical sketches should be used for reference only.

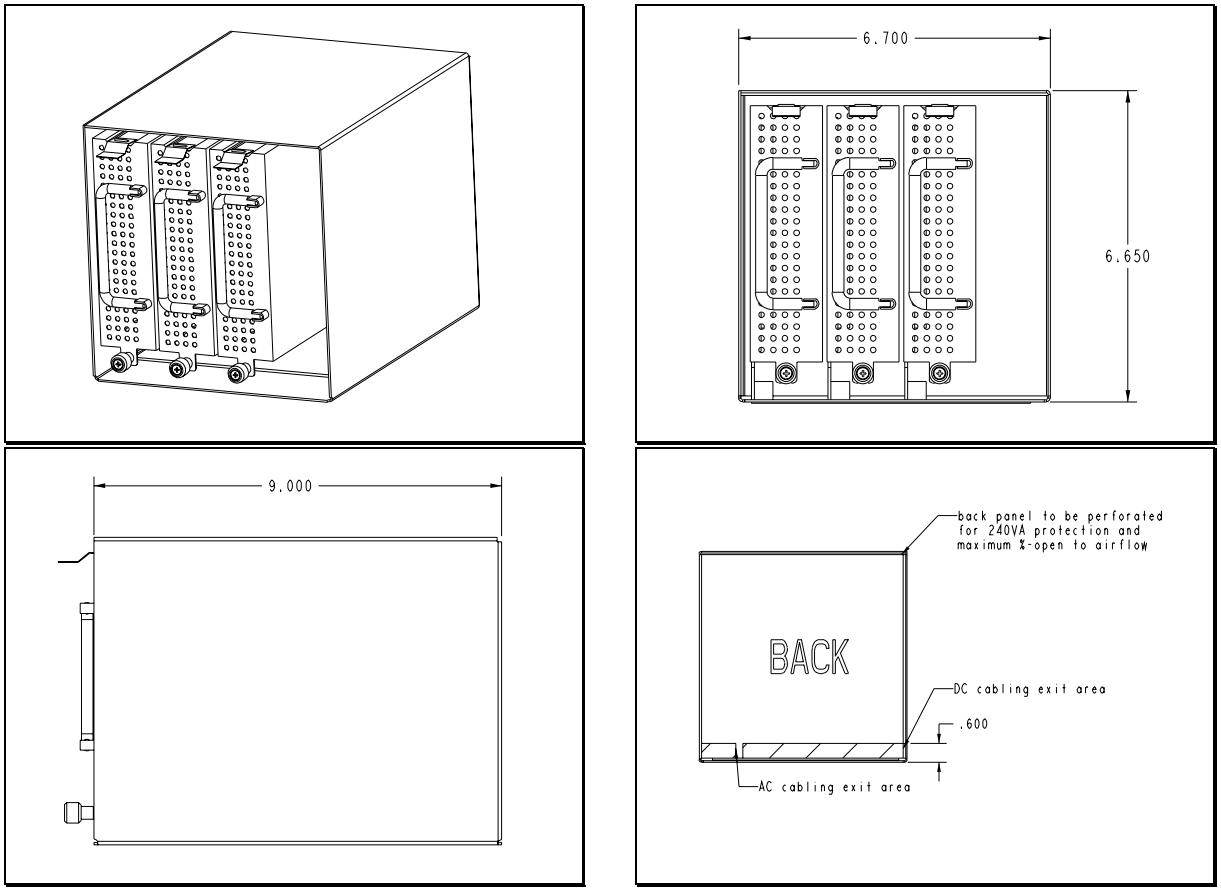


Figure 4-1: Power Subsystem Enclosure Outline Drawing

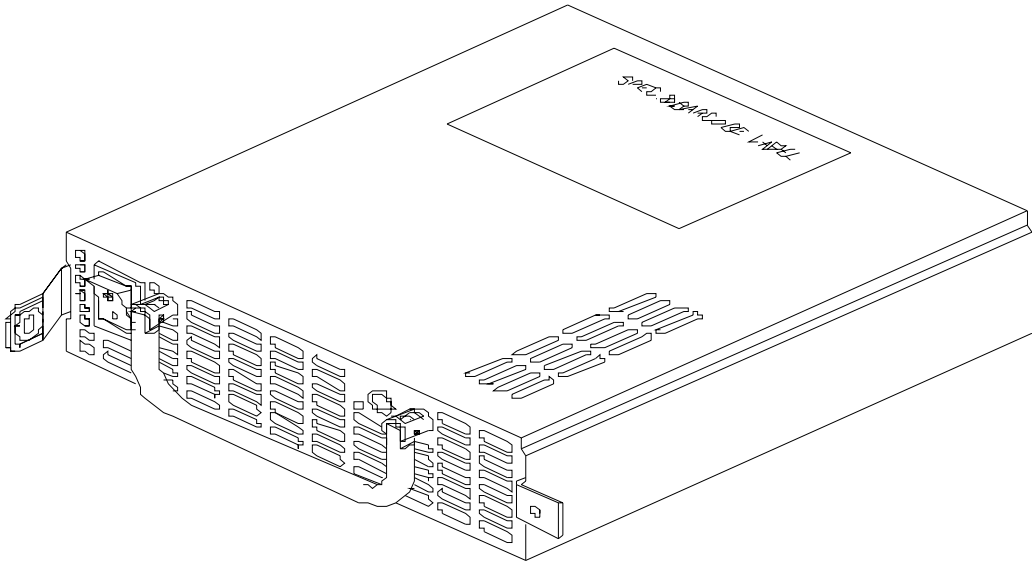


Figure 4-2: Power Supply Module Enclosure Outline Drawing

Note: The power supply module enclosure has dimensions of 39.5mm (1.555”) in height by 139.1mm (5.47”) in width by 190.6mm (7.5”) in depth (including the connector the depth is 200.6mm (7.9”).

4.3.2 Fan Requirements

4.3.2.1 Air Flow

The power subsystem in non-redundant (2+0) mode should be provided with no less than 50 CFM air flow from the system fans in redundant mode (all fans operating). The power subsystem in redundant mode (2+1) should be provided with no less than 40 CFM air flow from the cooling subsystem in non-redundant mode (one fan failure). The power subsystem in a non-redundant, minimum configuration (1+0) will be provided with no less than 37 CFM from the systems fans in minimum configuration (three fans), when the power supply filler panels are in place.

The cooling air enters the subsystem from the front of the system, passing through the power subsystem. The air exhausting from the power subsystem may be preheated by 25°C. Inlet air to the power subsystem shall be in the range of 5°C to 35°C.

4.3.2.2 Over-temperature Protection (OTP)

The power subsystem is protected from over-temperature conditions caused by loss of cooling air for the module or for the standby (Stdby) section, multiple fan failures, one fan failure plus one power supply module failure, or excessive ambient temperature. In the module OTP condition, the power supply unit (PSU) is in power off mode with the exception of +5 V Stdby output, but the power subsystem shall not latch in the power off mode. In the Stdby section OTP condition, the power subsystem will latch in the power off mode.

When the temperature drops to the operating level, the power subsystem automatically restores the power. The power subsystem alerts the system of the OTP condition via the Power Subsystem Fail (I^2C) signal and the corresponding LED on the power subsystem or the power supply module is turned off to indicate such condition.

4.3.3 Interface Requirements

4.3.3.1 AC Inlet

The AC power pins and wiring prior to the protective fuse(s) have a peak current rating higher than the peak inrush current or maximum fault current drawn by the power subsystem. The safety ground pin of the power supply module is the first pin to connect and the last to disconnect when the module is being inserted or removed from the power subsystem housing. The area near the AC inlet is service-only access and is protected with one level of protection – shrink insulation wrap on the bare parts.

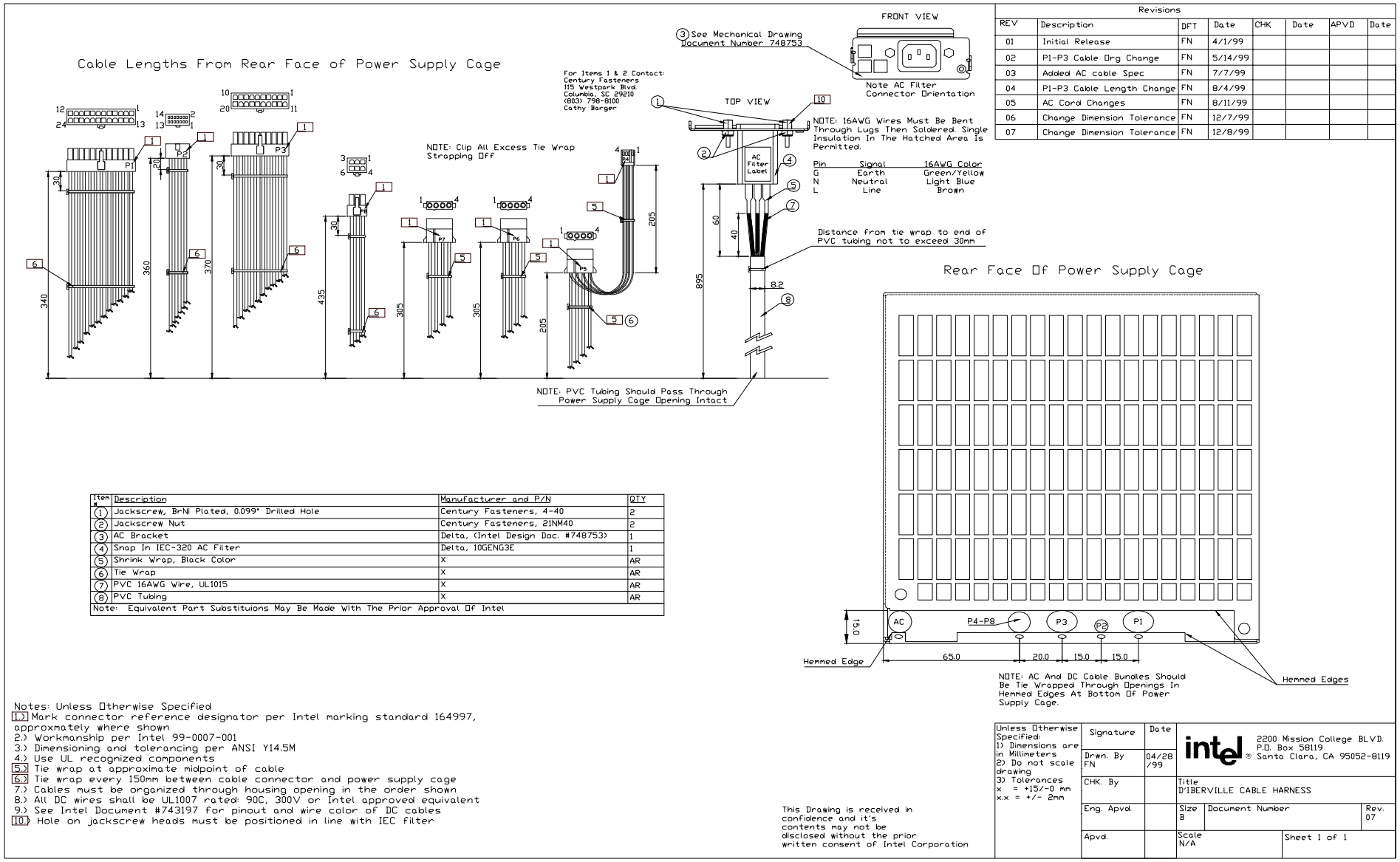
4.3.3.2 DC Output Connectors

The power subsystem DC power and control signals are interfaced to the server system via wire harnesses when the power supply modules are inserted into the power subsystem enclosure. In addition to the 5 V Stdby, -12 V, +3.3 V, +5 V and +12 V DC outputs, the following signals and output pins are included:

- +3.3 Vdc remote sense.
- +5 Vdc remote sense.
- +12 Vdc remote sense.
- Remote sense return.
- Power Subsystem On (DC PWR enable).
- Power Good.
- I^2C. (Note: PS Failure, PS Presence, PS Predictive Fail, +12 V Mon, +5 V Mon, and the 5 V Stdby rails failure are monitored via an I^2C interface chip.)

4.3.3.3 DC Output Harness

The DC output harness connectors and lengths are shown in Figure 4-3.



Revisions							
REV	Description	DFT	Date	CHK	Date	APVD	Date
01	Initial Release	FN	4/1/99				
02	P1-P3 Cable Org Change	FN	5/14/99				
03	Added AC cable Spec	FN	7/7/99				
04	P1-P3 Cable Length Change	FN	8/4/99				
05	AC Cord Changes	FN	8/11/99				
06	Change Dimension Tolerance	FN	12/7/99				
07	Change Dimension Tolerance	FN	12/8/99				

Item #	Description	Manufacturer and P/N	QTY
(1)	Jackscrew, BrNi Plated, 0.099" Drilled Hole	Century Fasteners, 4-40	2
(2)	Jackscrew Nut	Century Fasteners, 21NM40	2
(3)	AC Bracket	Delta, (Intel Design Doc. #748753)	1
(4)	Snap In IEC-320 AC Filter	Delta, 10GENG3E	1
(5)	Shrink Wrap, Black Color	X	AR
(6)	Tie Wrap	X	AR
(7)	PVC 16AWG Wire, UL1015	X	AR
(8)	PVC Tubing	X	AR
Note: Equivalent Part Substituions May Be Made With The Prior Approval Of Intel			

Notes: Unless Otherwise Specified
1.) Mark connector reference designator per Intel marking standard 164997, approxmately where shown
2.) Workmanship per Intel 99-0007-001
3.) Dimensioning and tolerancing per ANSI Y14.5M
4.) Use UL recognized components
5.) Tie wrap at approximate midpoint of cable
6.) Tie wrap every 150mm between cable connector and power supply cage
7.) Cables must be organized through housing opening in the order shown
8.) All DC wires shall be UL1007 rated: 90C, 300V or Intel approved equivalent
9.) See Intel Document #743197 for pinout and wire color of DC cables
10.) Hole on jackscrew heads must be positioned in line with IEC filter

Unless Otherwise Specified: 1) Dimensions are in Millimeters 2) Do not scale drawing 3) Tolerances x = +15/-0 mm x.x = +/- 2mm	Signature	Date
	Drwn. By FN	04/28/99
	CHK. By	
	Eng. Apvd.	
	Apvd.	

intel 2200 Mission College BLVD. P.O. Box 58119 Santa Clara, CA 95052-8119

Title: D'IBERVILLE CABLE HARNESS
Size: B | Document Number | Rev.: 07
Scale: N/A | Sheet 1 of 1

Figure 4-3: Output Harness Detail

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Table 4-1: P1 Connector Pin Assignments

P1 Main Power Connector:
Harness Length: 340 mm (13.4”) from rear of housing

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+3.3Vdc	Orange	13	+3.3Vdc	Orange
2	+3.3Vdc	Orange	14	+3.3Vdc	Orange
3	+3.3Vdc	Orange	15	+3.3Vdc	Orange
4	+3.3Vdc	Orange	16	+3.3Vdc	Orange
5	+3.3Vdc	Orange	17	+3.3Vdc	Orange
6	+3.3Vdc	Orange	18	+3.3Vdc	Orange
7	COM	Black	19	COM	Black
8	COM	Black	20	COM	Black
9	COM	Black	21	COM	Black
10	COM	Black	22	COM	Black
11	COM	Black	23	COM	Black
12	+12Vdc	Yellow	24	+12Vdc	Yellow

Table 4-2: P2 Connector Pin Assignments

P2 AUX Power Connector:
Harness length: 360 mm (14.2”) from rear of housing

Pin	Signal	24 AWG COLOR	Pin	Signal	24 AWG COLOR
1	COM	Black	2	+5VRS	Red
3	+3.3VRS	Orange	4	Fan Speed Input†	Brown
5	I^2C-SCL	Brown/White stripe	6	I^2C-SDA	Green/White stripe
7	COM	Black	8	PS-GOOD	Gray
9	PS-ON	Green	10	COM	Black
11	-12V	Blue	12	N/A	-
13	+12VRS	Yellow	14	Remote Sense Return	Black

Notes:

†Conducts System Fan Control Signal. Should be connected with pin 2 of connector P4 inside the power subsystem.

Table 4-3: P3 Connector Pin Assignments

P3 Main Power Connector:
Harness length: 370 mm (14.6”) from rear of housing

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+12Vdc	Yellow	11	+5VsdBy	Purple
2	COM	Black	12	COM	Black
3	COM	Black	13	COM	Black
4	COM	Black	14	COM	Black
5	COM	Black	15	COM	Black
6	+5 Vdc	Red	16	+5 Vdc	Red
7	+5 Vdc	Red	17	+5 Vdc	Red
8	+5 Vdc	Red	18	+5 Vdc	Red
9	+5 Vdc	Red	19	+5 Vdc	Red
10	+5 Vdc	Red	20	+5 Vdc	Red

Table 4-4: P4 Connector Pin Assignments

P4 Floppy Power Connector:
Harness length: P8 205 mm (8.1”) from rear of housing

Pin	Signal	22 AWG COLOR
1	+5 Vdc	Red
2	COM	Black
3	COM	Black
4	+12Vdc	Yellow

Table 4-5: P5-P7 Connectors Pin Assignments

P5-P7 Peripheral Power Connector
Harness length: P7 & P6 305 mm (12”) from rear of housing
Harness length: P5 205 mm (8.1”) from rear of housing

Pin	Signal	18 AWG COLOR
1	+12Vdc	Yellow
2	COM	Black
3	COM	Black
4	+5 Vdc	Red

Table 4-6: P8 Connector Pin Assignments

P8 FAN Power Connector:
Harness length: 435 mm (17.1”) from rear of housing

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+12Vdc	Yellow	4	+12Vdc	Yellow
2	Fan Speed Out†	Black	5	AC_OK	Blue
3	COM	Black	6	COM	Black

Notes:
†Conducts System Fan Control Signal. Should be connected with pin 4 of connector P2 inside the power subsystem.

Table 4-7: AC Distribution Cord Wiring

Double Insulated.

Pin	Signal	16 AWG COLOR
G	Earth	Green/yellow stripe
N	Neutral	Light Blue
L	Line	Brown

4.3.4 Marking and Identification

The power supply module and power subsystem markings and labels are described in the following sections.

4.3.4.1 LED Labeling

The power LED (green) is labeled **PWR.** The Stdby LED is labeled **SdBy (1,2,3)**.

4.3.4.2 Internal System Marking

The power supply module and power subsystem are marked to support the safety agency requirements, government requirements (if required, e.g., point of manufacturing), power supply vendor requirements, and Intel manufacturing and field support requirements. This marking is applied on an external surface of the power supply module and power subsystem and is not visible from the exterior of the server system. Label formats are shown in Figure 4-4, Figure 4-5, and Figure 4-6.

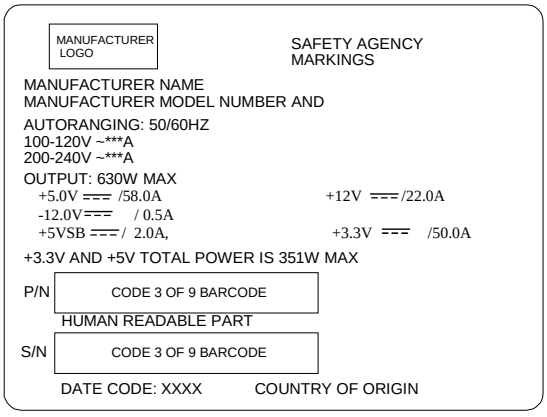


Figure 4-4: Internal Power Supply Module Label

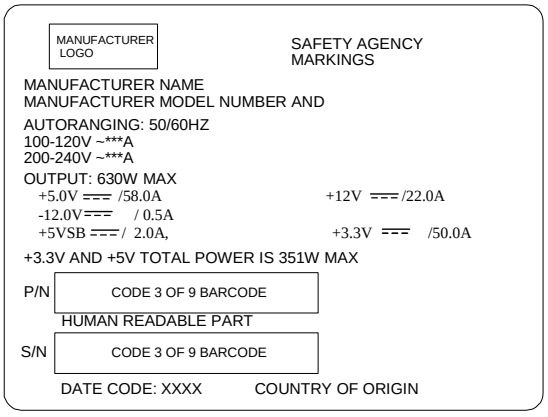


Figure 4-5: Internal Power Subsystem Label

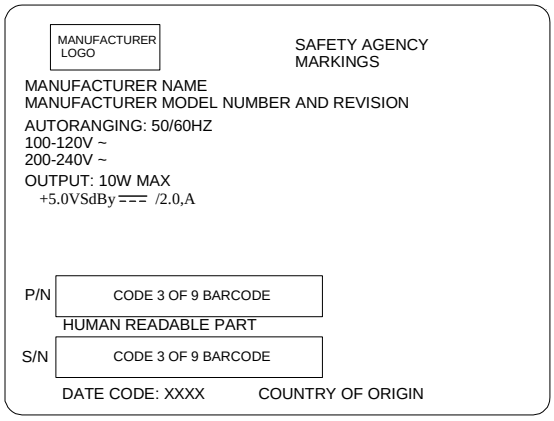


Figure 4-6: Power Cage Label

Note: Figure 4-4, Figure 4-5, and Figure 4-6 are provided for reference only. The exact content of these figures may not reflect the actual values characterized for this power subsystem.

4.3.4.3 Service Label

The power supply module and power subsystem are marked with an international label to indicate that no user serviceable parts are contained in the enclosure. This label is shown in Figure 4-7. This label is printed on bright yellow vinyl label stock with black symbols.

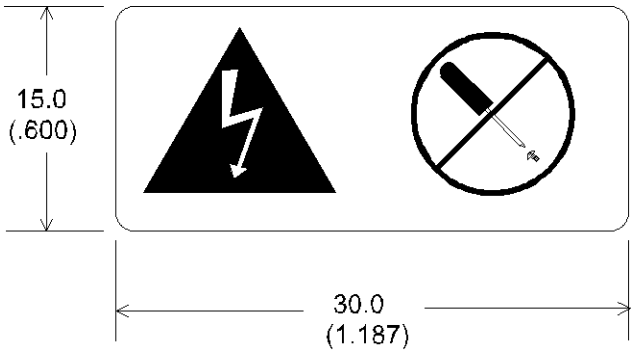


Figure 4-7: Service Label

4.3.4.4 Internal Power Subsystem Markings

The fuse rated current and voltage are marked adjacent to each fuse holder. The printed circuit boards containing the fuses are labeled “CAUTION. Double pole/neutral fusing” near the fuses where they are easily visible to service personnel.

4.4 Electrical Interface

4.4.1 Efficiency

The power subsystem has a minimum efficiency of 62% to its DC output pins at maximum load currents and at rated nominal input voltages and frequencies per Section 4.4.2.1 of this document.

4.4.2 AC Input Voltage Specification

4.4.2.1 AC Input Voltage Ranges

The nominal input voltage ranges specified in AC volts RMS are 100, 120, 208, 220, and 240 Vac. The power subsystem incorporates a universal power input with active power factor correction, which reduces line harmonics in accordance with EN61000-3-2 and JEIDA MITI standards. The ratings are marked on the power supply labels as referenced in Table 4-8.

Table 4-8: Input Voltage Requirements

Parameter	Min	Nom	Max	Units
Vin (115)	90	100-120	132	Vrms
Vin (230)	180	200-240	264	Vrms
Vin Frequency	47	50/60	63	Hz
Input Current 115 Vac range	7.6	10	11.0	Amps
Input Current 220 Vac range	3.8	5	5.5	Amps

4.4.2.2 AC Line Dropout and Hold-up Time

AC line dropout is a transient condition defined as the line voltage input to the power subsystem dropping to 0 volts. While operating at full load, an AC line dropout condition with a period equivalent to a complete cycle of AC input power frequency (i.e., 20 milliseconds at 50 Hz) or less will not cause any out of regulation conditions such as overshoot or undershoot. The Power Good signal does not go to a low state under these conditions. The one full cycle hold-up time requirement is met in a redundant configuration.

When a power supply module fails and the power subsystem is no longer in the redundant mode, it is no longer in the normal operating mode and will not meet this requirement. This requirement does not apply during mean time to repair (MTTR), when the failed power supply module is to be replaced. AC dropout transients in excess of 20 milliseconds may cause shutdown of the power subsystem or out of regulation conditions, but will not cause a latch off condition or damage to the power subsystem.

4.4.2.3 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. A sag (also referred to as “brownout”) condition is defined as the AC line voltage dropping below the nominal voltage. Surge is defined as a condition when the AC line voltage rises above the nominal voltage. The power subsystem meets the performance requirements under the AC line sag and surge conditions described in Table 4-9 and Table 4-10.

Table 4-9: AC Line Sag Transient Performance

Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 15 minutes	15% 97.75 V	Mid-point of rated AC voltages 115/220 Vac	50/60 Hz	No loss of function or performance
0 to ½ AC cycle	30% 80.5 V	Mid-point of rated AC voltages 115/220 Vac	50/60 Hz	No loss of function or performance
0 to 5 AC cycles	50% 57.5 V	Mid-point of rated AC voltages 115/220 Vac	50/60 Hz	Loss of function acceptable, self recoverable

Table 4-10: AC Line Surge Transient Performance

Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 15 minutes	15% 253 V	Mid-point of rated AC voltages 115/220 Vac	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30% 286 V	Mid-point of rated AC voltages 115/220 Vac	50/60Hz	No loss of function or performance

4.4.2.4 AC Line Inrush

The AC line inrush current of one power supply module does not exceed i^2t fuse rating when the power subsystem is turned on at the 90 degree phase point of a 264 Vac line input.

4.4.2.5 Dielectric Strength Requirements

The power supply module and the power subsystem meet all safety agency requirements for dielectric strength.

4.4.2.6 AC Line Fuse

The LINE and NEUTRAL AC inputs are fused. AC line fusing is acceptable for all safety agency requirements.

4.4.2.7 Power Recovery

The power subsystem recovers automatically after an AC power failure. AC power failure is defined as any loss of AC power that exceeds the AC line dropout criteria defined in Section 4.4.2.2 of this document.

4.4.2.8 Power Factor Correction

The power supply modules incorporate Power Factor Correction circuits.

4.4.3 DC Output Specification

The power subsystem DC output specifications may be met, depending on system configuration, by a single power supply module or by two or three power supply modules operating with their outputs directly paralleled inside the power subsystem. When operated in parallel the power supply modules equally share the total load currents within the limits specified herein while meeting all the performance requirements of individual power supply modules.

In redundant mode operation (three power supply module configuration), failure of a power supply module in a paralleled group or removal of an operational or failed power supply module from a paralleled group does not cause DC output transients in excess of the limits specified. Adding an operational power supply module to the power subsystem or extracting a power supply module from the power subsystem does not cause DC output transients in excess of the limits specified.

Steady state DC output voltages at the remote sense points remain within the limits specified in Table 4-11 for all combinations of operating line, load, load transient, and environment specified herein. The combination of set point limits, line/load regulation and ripple/noise does not exceed the DC output voltage limits specified in Table 4-11.

Table 4-11: DC Output Voltage Limits

Parameter	Min	Max	Units	Tolerance
+3.3 V	+3.201	+3.465	V	-3%, + 5%
+5 V	+4.80	+5.25	V	-4% + 5%
+12 V	+11.40	+12.60	V	± 5%
-12 V	-11.40	-12.60	V	± 5%
+5 V STANDBY	+4.75	+5.25	V	± 5%

4.4.3.1 DC Outputs Rating

The steady state and peak DC output load currents of the power subsystem shall be in the ranges specified in Table 4-12 and Table 4-13.

Table 4-12: Total Power Subsystem Load Range

	1 Module Configuration			2 and 3 Module Configuration		
Voltage	**Minimum Continuous**	**Maximum Continuous**	**Peak**	**Minimum Continuous**	**Maximum Continuous**	**Peak**
+3.3 V	1.0 A	28 A		1.0 A	50 A	
+5 V	1.0 A	32 A		1.0 A	58 A	
+12 V	0 A	12 A	15 A	0 A	22 A	28 A
-12 V	0 A	0.5 A		0 A	0.5 A	
+5 V STANDBY	0.1 A	2.0 A		0.1 A	2.0 A	

Table 4-13: Sleep Mode Load Range

Voltage	**Total Power Subsystem Load Condition, A**					
	S1		**S4 (Stdby)**		**S5 (Stdby)**	
	Min	**Max**	**Min**	**Max**	**Min**	**Max**
+3.3 V	6.6	6.6	0	0	0	0
+5 V	2.1	4.98	0	0	0	0
+12 V	2.35	3.55	0	0	0	0
-12 V	0.2	0.2	0	0	0	0
+5 V STANDBY	0.05	2.0	0	2.0	0	2.0

4.4.3.2 DC Output Maximum Rating

Maximum continuous power output with one power supply module should not exceed 350 W. Maximum continuous power output with two or three power supply modules should not exceed 630 W. Maximum current drawn on the +12 V output from power subsystem should not exceed 28 A for longer than 12 seconds.

4.4.3.3 DC and Transient Load Output Voltage Limit

The power subsystem maintains regulation under all specified conditions including parallel operation of two and three power supply modules, line variations, load variations, transient load conditions, peak ripple/noise, maximum remote sense drops, and temperature change. The +3.3 Vdc, +5 Vdc, and +12 Vdc output voltages are measured at their respective remote sense points.

4.4.3.4 Power Timing

Table 4-14 and Table 4-15 show the timing requirements for single power supply module operation. The output voltages rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 200 ms. The +3.3 V, +5 V, and +12 V output voltages start to rise at approximately the same time. All outputs rise monotonically. Each output voltage reaches regulation within 100 ms (T_{vout_on}) of

each other and begins to turn off within 100 ms (T_{vout_on}) of each other. Please refer to Table 4-14 for a summary. shows the timing requirements for a single power supply module being turned on and off via the AC input, with PSON held low and the AC input applied. The AC_OK signal is not used to enable the turn on timing of the power supply module.

Refer to Figure 4-8 and Figure 4-9 for details.

Table 4-14: Output Voltage Timing

Item	Description	Min	Max	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	200	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		100	msec

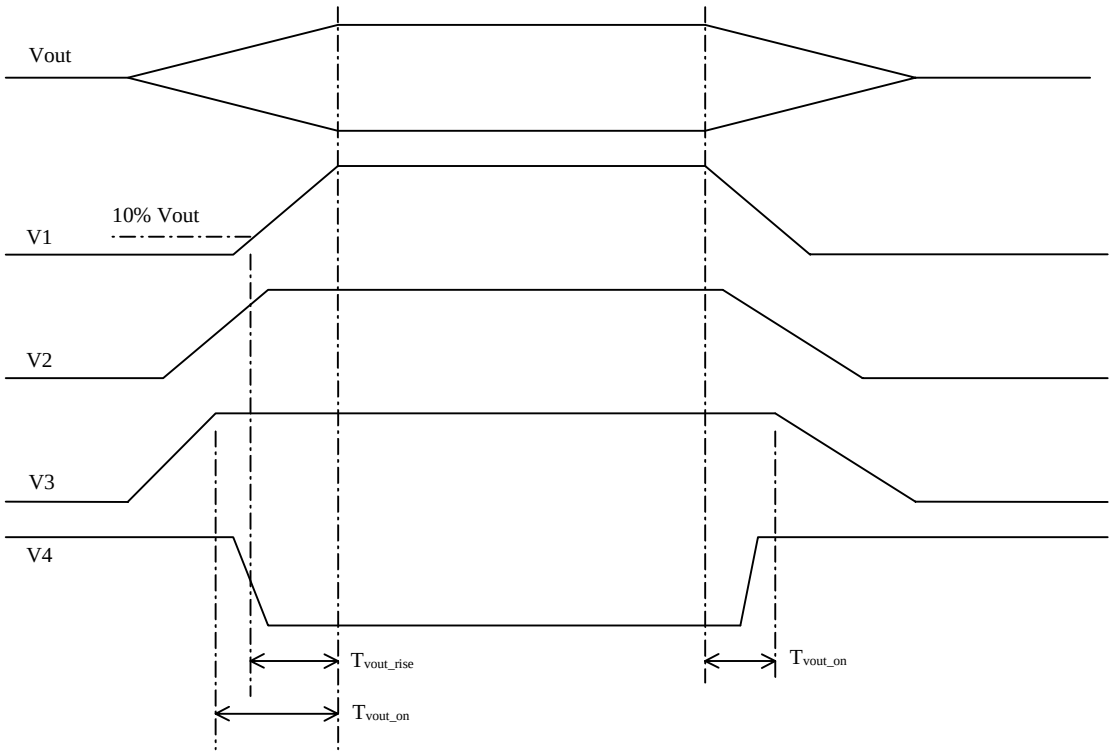


Figure 4-8: Output Voltage Timing

Table 4-15: Turn On/Off Timing

Item	Description	Min	Max	Units
$T_{sb\_on\_delay}$	Delay from AC being applied to 5 VSB being within regulation.		1500	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	msec
T_{vout_holdup}	Time all output voltages, including 5 VSB, stay within regulation after loss of AC.	21		msec
T_{pwok_holdup}	Delay from loss of AC to deassertion of PWOK.	20		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSON# deactive to PWOK being deasserted.		50	msec
T_{acok_delay}	Delay from loss of AC input to deassertion of ACOK#.	20		msec

Item	Description	Min	Max	Units
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T_{pwok_off}	Delay from PWOK deasserted to output voltages (3.3 V, 5 V, 12 V, -12 V, 5 VSB) dropping out of regulation limits.	1	200	msec
T_{pwok_low}	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON signal.	100		msec

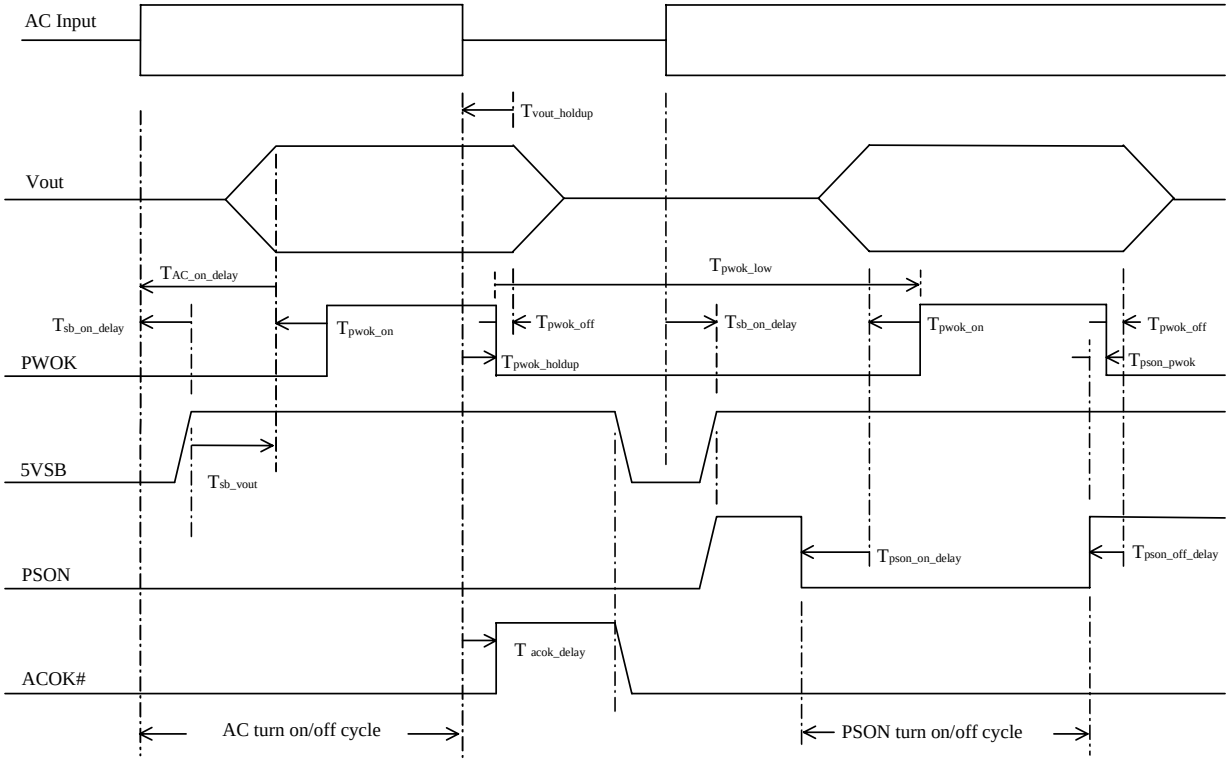


Figure 4-9: Turn On/Off Timing

4.4.3.5 Turn-on Delay and Rise Time

Output voltages reach their nominal ranges within 1.5 seconds after the Power Subsystem On signal is asserted. The output voltage rise from 10% to within regulation limits within a minimum of 5 msec and a maximum of 350 msec is measured at full load range on each output. No voltage of opposite polarity will be present during turn-on.

The +3.3 V, +5 V, +12 V, and –12 V output voltages will be in their respective regulation bands within 100 msec of each other. The 3.3 V output will not be delayed from the +5 V output.

4.4.3.6 Turn-off Delay

The DC outputs will drop below 80% of nominal voltage within 2 seconds and below 20% of nominal voltage within 10 seconds after receipt of the turn-off Power Subsystem On signal level.

A minimum of 100 msec power down time is required. The power down time is defined as the time the power subsystem must be powered down before it is powered back up again.

4.4.3.7 Over-voltage Protection

The power supply module over-voltage protection is locally sensed. The power subsystem will shutdown in a latch off mode after an over-voltage condition. This latch can be cleared by toggling Power Subsystem On signal or by an AC power interruption of greater than 1 second. This limit applies over all specified AC input voltages and output loading conditions. Table 4-16 specifies the over-voltage limits. The values are measured at the output of the power subsystem connector.

Table 4-16: Over-voltage Protection

Output Voltage	Protection Point [V]
+3.3 V	3.8 -- 4.3
+5 V	6.0 -- 6.5
+12 V	13.5 – 15

4.4.3.8 Over-current Protection

The power supply module has a current limit to prevent the +3.3 Vdc, +5 Vdc, and +12 Vdc outputs from exceeding the values shown in Table 4-17. Other outputs are short circuit protected. The power supply module may latch off without any time delay, if the 5 VStdby or the -12 V outputs are overloaded or shorted to ground.

The current limiting for the +3.3 Vdc, +5 Vdc, and +12 Vdc outputs are of the voltage foldback type. The time delay should be long enough to let the other power supply modules come up and reach a steady current share state. The over-current limit level is maintained for a period of 2.0 seconds maximum. After this time, the power supply module will latch off. The latch may be cleared by toggling the Power Subsystem On signal or by an AC power interruption of greater than 1 second. The power subsystem will not be damaged from repeated power cycling in this condition.

Table 4-17: Over-current Protection

Voltage	Over-current Limit (See Notes)
+3.3 V	53 A minimum; 60 A maximum
+5 V	62 A minimum; 69 A maximum
+12 V	30 A minimum; 36 A maximum

Notes:
The limits shown do not depend on the number of power supply modules in the power subsystem.

4.4.3.9 Short Circuit Protection

Applying of short circuit to any DC output will not damage the power subsystem. Short circuits will not turn into the over-current protection process described in Section 0. A hard short circuit

will turn off the power subsystem immediately. A hard short circuit is defined when the load level is less than 10 mΩ.

4.4.3.10 Grounding Requirements

The power subsystem DC output ground is earth ground and connected to the power subsystem case. Resistance from the DC return pins to the chassis does not exceed 1.0 mΩ.

4.4.3.11 Current Share Requirements

Equal power sharing of paralleled power supply modules is provided to prevent life shortening stress concentration in individual power supply modules. Power sharing is accomplished by actively matching the output currents on the high power outputs. The Current Sharing load deviation is defined as follows:

```
Load_Deviation = [(Actual_Load – Mean_ Load)/(Mean Load)] * 100%.
```

The +3.3 V, +5 V, and +12 V output currents of paralleled modules maintain a maximum Load Deviation of ± 10% at max rated current. At one half of rated current, the maximum Load Deviation is ± 20%. At less than half the rated current, the maximum Load Deviation can be greater than ± 20%.

The other DC outputs may share to any degree, as long as regulation, transient, and hot-swap limits are met.

4.4.4 Control Signals

4.4.4.1 Power Subsystem On (DC Power Enable) Signal (Input)

The Power Subsystem On circuit is safety extra low voltage (SELV). Upon receiving a logic LOW at this signal, the power subsystem is turned on and power outputs and other signals are provided at the corresponding DC connector output pins.

A logic HIGH on this pin at the DC connector will turn the power subsystem off. The normal turn off delay and shut down sequence described in Section 4.4.3.6 are followed when the Power Subsystem On signal is used to turn the power subsystem off.

The characteristics of the Power Subsystem On signal are shown in Table 4-18. The Power Subsystem On is an input signal to the power subsystem from the system.

Table 4-18: Power Subsystem On Signal Specification

DC Power Enable Signal	Voltage Level†	Current
HIGH, PWR SUPPLY DISABLED	2 V min	0.5 mA max source current
LOW, PWR SUPPLY ENABLED	1 V max or open circuit	

Notes:

†Measured relative to the power subsystem DC common output ground pins.

4.4.4.2 Power Good (Output)

The power subsystem provides a Power Good signal. This signal indicates that all outputs have reached acceptable operating voltage. The Power Good signal levels and souring/sinking requirements are described in Table 4-19. The Power Good is an output signal from the power subsystem to the system.

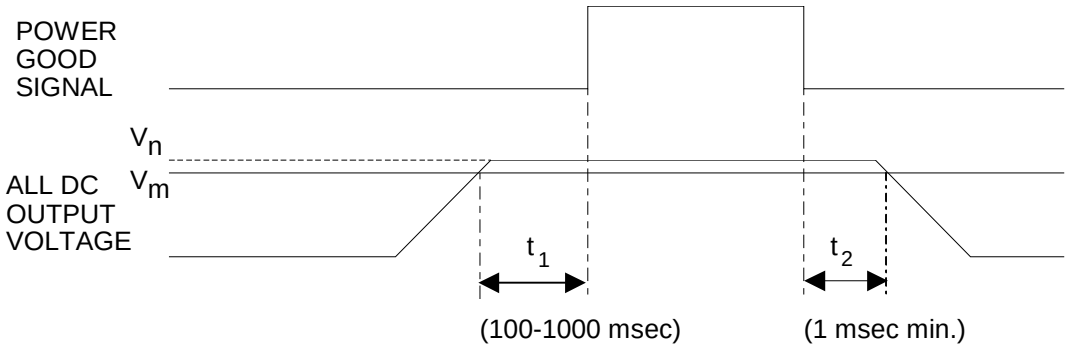
Table 4-19: Power Good Signal

Power Good Signal	Voltage Level†	Current
LOW STATE DEASSERTED (Power Not Good)	0.4 V max	4 mA min sink current
HIGH STATE ASSERTED (Power Good)	2.4 V min	0.5 mA max source current

Notes:
†Measured relative to the power subsystem DC common ground output connector pins.

The Power Good signal is held low until all outputs have reached at least 95% of their respective operating voltages. The turn on delay for the Power Good signal is between 100 and 1000 msec.

The Power Good signal will be low for a minimum of 1 msec before any of the output voltages falls below the regulation limits. Refer to Figure 4-10.



Vn Nominal Output Voltage +5 VDC
Vm Minimum Output Voltage + 4.8 VDC
t_1 Delay Turn-on (100-1000 msec)
t_2 Delay Turn-off (1 msec min)

Figure 4-10: Power Good Signal Characteristics

4.4.4.3 I²C Interface Signals

The following 12 signals are communicated back to the system via the server system infrastructure (SSI) optional connector.

- PS1_PRESENT
- PS2_PRESENT
- PS3_PRESENT
- PS1_PREDICT_FAIL
- PS2_PREDICT_FAIL
- PS3_PREDICT_FAIL
- PS1_ FAIL
- PS2_ FAIL
- PS3_ FAIL
- +5VSB_FAIL
- +12V_MON
- +5V_MON

4.4.4.3.1 Power Supply Module Present Indicator (3)

This signal is used to sense the number of power supply modules in the system (operational or not).

4.4.4.3.2 Power Supply Module Failure Signal (3)

This signal is available on the power supply module connector. Upon receiving this signal, the system informs the operator that one of the power supply modules has failed and a replacement of that module is necessary.

The Power Supply Module Failure is defined as OVP at any output, under-voltage (UV) at any output, and/or latch off condition inside the power supply module. It is an output signal from the power subsystem to the system.

4.4.4.3.3 SdBy Failure Signal (1)

The Stdby circuitry generates a SdBy Failure signal to indicate that one of the redundant standby converters has failed.

4.4.4.3.4 Predictive Failure Signal (3)

A Predictive Failure signal indicates that the power subsystem or a power supply module is likely to fail in the near future due to high temperature, lack of air flow, a poorly performing fan, etc. Predictive Fan Failure signal does not cause the power supply module to shut down. This signal is utilized by the system to generate a signal, which alerts an operator that the loading condition, ambient temperature, or air flow are not adequate, and one or several power supply modules will be shut down if no actions are taken to correct this condition. The Predictive Failure is an output signal from the power subsystem to the system.

4.4.4.3.5 5 V and 12 V Output Monitoring Signals (2)

These signals are utilized by the system to monitor the 5 V and the 12 V rail tolerances.

4.4.4.4 AC_OK Signal (1)

Each power supply module provides an AC_OK signal. This signal is utilized by the power subsystem to synchronize the power on timing of up to three power supply modules (if all the modules are present) within a nominal line input AC voltage range and under PFC CKT operational condition. The AC_OK signal allows the system to turn on at 90 Vac with 10% THD. AC_OK will not deassert during any of the operating-level tests in this specification, including the 20 msec dropout (hold-up time) test.

An AC_OK signal is generated with any number of power supply modules present in the power subsystem.

Table 4-20: AC_OK Signal

AC_OK Signal	Voltage Level	Current
LOW STATE – DEASSERTED (AC not OK)	0.4 V max	4 mA min sink current
HIGH STATE – ASSERTED (AC is OK)	2.4 V min	1.3K pull up resistor on system side

4.4.4.5 Power Supply Field Replacement Unit Signal (1)

The FRU data format is compliant with the Intelligent Platform Management Interface (IPMI) specification.

The I^2C address of the Power Subsystem EEPROM is 0xA6. The FRU circuits inside the power supply are powered by 5 VStby on the system side of the OR'ing device and grounded to ReturnS (remote sense return). The Write Control (or Write Protect) pin is tied to ReturnS inside the power supply module so that information can be written to the EEPROM.

4.4.4.6 LED Indicators

The three green Stdby LEDs (Stdby 1,2,3) indicate that AC is applied to the power subsystem and standby voltage is available. There is a green Power (PWR) LED on each power supply module to indicate that all the power outputs are available.

The Power LED is turned off when:

- the power supply modules are disabled by DC enable signal,
- the power supply module has been overstressed,
- the power supply module has failed and therefore, a replacement of the unit is necessary.

The LEDs are visible on the power supply modules and Stdby section.

5. Hard Disk Drive Bay Assembly

This chapter describes the design and external interface of the SRKA4 server system hard disk drive bay assembly.

5.1 Features

The SRKA4 server system hard disk drive bay assembly:

- Provides a cost effective ease of power-on (hot-swap) drive replacement.
- Provides easy RAID integration over a wide range of RAID controller products.
- Monitors the SCSI bus for enclosure services messages, and acts on them appropriately. Examples of such messages include:
  - Activate a drive fault indicator.
  - Power down a drive which has failed.
  - Report fan tachometer status.
- Includes a SAF-TE intelligent agent, which acts as proxy for “dumb” I2C devices (that have no bus mastering capability) during intra-chassis communications.

5.2 Overview

The hard disk drive bay assembly is an LVD/SE SCSI design that provides support for SCSI devices using Low Voltage Differential Signaling (Ultra 2) as well as older SE SCSI devices (Ultra and older). The single backplane has a single SCSI channel with a SAF-TE controller and microcontroller on an add-in card. The backplane supports hot swapping SCA-2 style drives when mounted in the docking drive carrier.

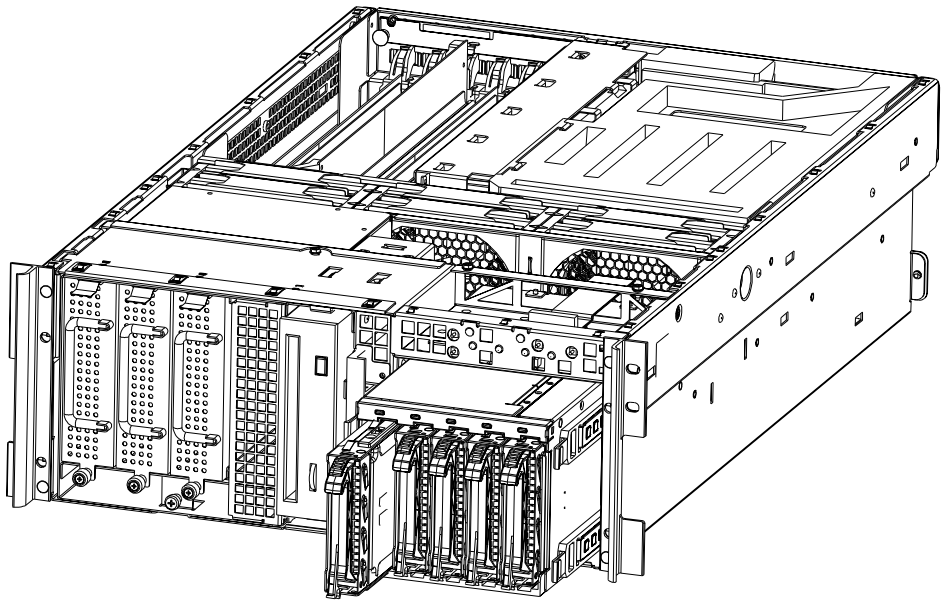


Figure 5-1: SRKA4 Server System Hard Disk Drive Bay

5.3 Functional Description

The SRKA4 server system supports up to five 1 inch high, 3.5 inch wide SCA LVDS hard drives that are accessed by opening the door on the bezel[2]. Five metal carriers are provided with the system to mount the hard drives. When no drive is installed in a carrier, an air baffle is installed to ensure proper cooling of the hard drives.

The hard disk drive bay assembly is designed to accept 1" peripherals that consume up to 14 watts of power. This wattage number is intended as a guideline. Thermal performance of specific hard drives must be verified to ensure compliance to the drive manufacturer's specifications. Peripherals must be specified to operate at a maximum ambient temperature of 50°C.

5.3.1 SCA-2 Connectors

The assembly includes five SCA-2 connectors. Each SCSI drive attaches to the backplane using one of these connectors. Each connector:

- Provides both power and SCSI signals.
- Has control signals that enable the backplane to provide SCSI ID assignments as well as drive motor spin-up configuration.

5.3.2 SCSI Multi-mode Termination

The multi-mode terminators provide SCSI-3 SPI-2 compliant termination for the backplane. These terminators provide termination in both SE mode and LVD mode.

5.3.3 SCSI Interface

The SCSI interface on the SRKA4 server system hard disk drive backplane provides the link between the SCSI bus and the microcontroller. This interface allows the microcontroller to respond as a SCSI target to implement the SAF-TE protocol. This is implemented using a Symbios* logic 53C80S SCSI Interface Chip (or equivalent).

5.3.4 Power Control

Power control on the backplane supports the following features:

- Spin-down of a drive when a failure is detected and reported (using enclosure services messages) via the SCSI bus. An application or RAID controller detects a drive related problem that indicates a data risk. In response, it takes the drive out of service and sends a spin down SCSI command to the drive. This decreases the likelihood of the drive being damaged during removal from the hot-swap drive bay. When a new drive is inserted, the power control waits a small amount of time for the drive to be fully seated, and then applies power with a controlled power ramp.

- If system power is on, the backplane immediately powers off a drive slot when it detects that the drive has been removed. This prevents possible damage to the drive when it is partially removed and re-inserted while full power is available, and prevents disruption of the entire SCSI array from possible sags in supply voltage and resultant current spikes.

[2] An optional accessory is available that supports three 1.6 inch high, 3.5 inch wide hard disk drives.

5.3.5 Microcontroller

The microcontroller provides all the intelligence for the SRKA4 server system hard disk drive bay and is commonly referred to as the Hot Swap Controller (HSC). It is an 80C652 microcontroller, with a built-in I^2C interface that uses Intel® Flash for program code storage, and Static RAM for program variables and buffers.

5.3.6 Hard Drive Fault LED

The HSC turns the drive fault LEDs on or off according to the states specified via commands received via SAF-TE and the IMB. The drive fault LEDs are yellow and serve to indicate failure status for each drive. The LEDs are physically located on the LVD/SE SCSI backplane, and are driven from the backplane.

During initialization, the microcontroller flashes the LEDs for two seconds to signal successful POST completion.

Additionally, a green LED is turned on when its drive is accessed.

5.3.7 IMB (I^2C bus)

The I^2C bus is a system-wide server management bus. It provides a way for various system components to communicate independently of the standard system interfaces (e.g., PCI bus or processor/memory bus). The I^2C bus controller is integrated into the microcontroller.

5.3.8 Temperature

The SRKA4 server system hard disk drive assembly bay provides a temperature sensor in the center of the SAF-TE add-in card. This may be accessed by a private I^2C bus and can be reached through the BMC.

5.3.9 Serial EEPROM

The SRKA4 server system hard disk drive bay assembly provides 256 bytes of non-volatile storage. This storage holds the serial number, part number, FRU inventory information and miscellaneous application code used by firmware about the LVD/SE SCSI backplane. This is accessed by a private I^2C bus.

5.4 Connector Interface

The signal mnemonics defined here may appear in descriptive text in the document. An "_L" as a suffix on the signal name indicates that the signal is active-low. Two colons between numbers indicate a range of signals (e.g., AD[31::0]).

5.4.1.1 SCSI SCA-2 Drive Connector

An SCA-2 connector is used on the primary side of the board. The pinout is the same as SCA-1. The connector pin assignment is from the current draft *Small Form Factor-8046 Rev. 1.1* document.

Table 5-1: SCA-2 Connector

80-pin Connector Contact and Signal Name			Cable Conductor Numbers are not Applicable	80-pin Connector Contact and Signal Name		
1	12V Charge	(L)		(L)	12V Ground	41
2	12V	(S)		(L)	12V Ground	42
3	12V	(S)		(L)	12V Ground	43
4	12V	(S)		(S)	Mated 1	44
5	Reserved/ESI-1	(S)		(L)	-EFW	45
6	Reserved/ESI-2	(S)		(L)	DIFFSNS	46
7	-DB(11)	(S)		(S)	+DB(11)	47
8	-DB(10)	(S)		(S)	+DB(10)	48
9	-DB(9)	(S)		(S)	+DB(9)	49
10	-DB(8)	(S)		(S)	+DB(8)	50
11	-I/O	(S)		(S)	+I/O	51
12	-REQ	(S)		(S)	+REQ	52
13	-C/D	(S)		(S)	+C/D	53
14	-SEL	(S)		(S)	+SEL	54
15	-MSG	(S)		(S)	+MSG	55
16	-RST	(S)		(S)	+RST	56
17	-ACK	(S)		(S)	+ACK	57
18	-BSY	(S)		(S)	+BSY	58
19	-ATN	(S)		(S)	+ATN	59
20	-DB(P)	(S)		(S)	+DB(P)	60
21	-DB(7)	(S)		(S)	+DB(7)	61
22	-DB(6)	(S)		(S)	+DB(6)	62
23	-DB(5)	(S)		(S)	+DB(5)	63
24	-DB(4)	(S)		(S)	+DB(4)	64
25	-DB(3)	(S)		(S)	+DB(3)	65
26	-DB(2)	(S)		(S)	+DB(2)	66
27	-DB(1)	(S)		(S)	+DB(1)	67
28	-DB(0)	(S)		(S)	+DB(0)	68
29	-DB(P1)	(S)		(S)	+DB(P1)	69
30	-DB(15)	(S)		(S)	+DB(15)	70
31	-DB(14)	(S)		(S)	+DB(14)	71
32	-DB(13)	(S)		(S)	+DB(13)	72
33	-DB(12)	(S)		(S)	+DB(12)	73
34	5V	(S)		(S)	Mated 2	74
35	5V	(S)		(L)	5V Ground	75
36	5V Charge	(L)		(L)	5V Ground	76
37	Spindle Sync	(L)		(L)	Active LED Out	77
38	MTRON	(L)		(L)	DLYD_START	78
39	SCSI ID (0)	(L)		(L)	SCSI ID (1)	79
40	SCSI ID (2)	(L)		(L)	SCSI ID (3)	80

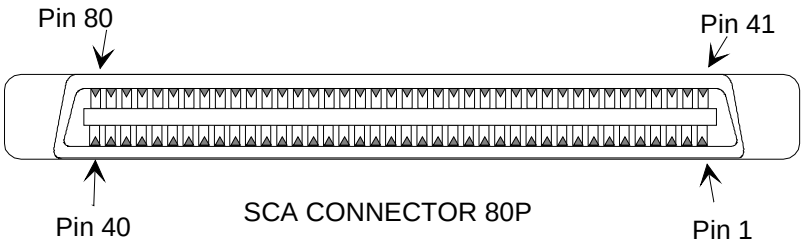


Figure 5-2: SCA-2 Connector

5.4.2 SCSI Input Connector

The SCSI input connector is a non-shielded device connector.

Table 5-2: SCSI Input Connector Pinout

Signal Name	Connector Contact Number	SCSI Bus Conductor Number	SCSI Bus Conductor Number	Connector Contact Number	Signal Name
+DB(12)	1	1	2	35	-DB(12)
+DB(13)	2	3	4	36	-DB(13)
+DB(14)	3	5	6	37	-DB(14)
+DB(15)	4	7	8	38	-DB(15)
+DB(P1)	5	9	10	39	-DB(P1)
+DB(0)	6	11	12	40	-DB(0)
+DB(1)	7	13	14	41	-DB(1)
+DB(2)	8	15	16	42	-DB(2)
+DB(3)	9	17	1 8	43	-DB(3)
+DB(4)	10	19	20	44	-DB(4)
+DB(5)	11	21	22	45	-DB(5)
+DB(6)	12	23	24	46	-DB(6)
+DB(7)	13	25	26	47	-DB(7)
+DB(P)	14	27	28	48	-DB(P)
GROUND	15	29	30	49	GROUND
GROUND	16	31	32	50	GROUND
RESERVED	17	33	34	51	RESERVED
RESERVED	18	35	36	52	RESERVED
RESERVED	19	37	38	53	RESERVED
GROUND	20	39	40	54	GROUND
+ATN	21	41	42	55	-ATN
GROUND	22	43	44	56	GROUND
+BSY	23	45	46	57	-BSY
+ACK	24	47	48	58	-ACK
+RST	25	49	50	59	-RST
+MSG	26	51	52	60	-MSG
+SEL	27	53	54	61	-SEL
+C/D	28	55	56	62	-C/D
+REQ	29	57	58	63	-REQ
+I/O	30	59	60	64	-I/O

Signal Name	Connector Contact Number	SCSI Bus Conductor Number	SCSI Bus Conductor Number	Connector Contact Number	Signal Name
+DB(8)	31	61	62	65	-DB(8)
+DB(9)	32	63	64	66	-DB(9)
+DB(10)	33	65	66	67	-DB(10)
+DB(11)	34	67	68	68	-DB(11)

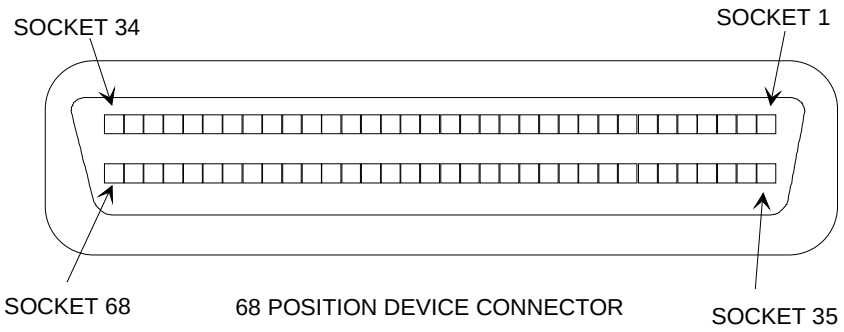


Figure 5-3: SCSI Input Connector 68P Non-Shielded

5.5 Specifications

5.5.1 Electrical Specifications

This section contains a summary of DC specifications for the SRKA4 server system hard disk drive bay assembly connectors.

5.5.1.1 Power Connector

Table 5-3: Power Connector (J4A1, J3A2) Pinout

Pin	Signal
1	12V
2	Ground
3	Ground
4	+5V

5.5.1.2 I2C Connector

Table 5-4: I2C Connector (J2A1) Pinout

Pin	Signal
1	I2C_SDA
2	Ground
3	I2C_SCLK
4	I2C_ADDR_CNTRL

5.5.1.3 SAF-TE PCI Connector Interface

The PCI connector interfaces the LVD bus to the AIC3860 on the SAF-TE card.

Table 5-5: PCI Connector (J5C1) Pinout

Pin	Signal	Pin	Signal
A1	Ground	B1	Ground
A2	LVD_SCSI:1	B2	LVD_SCSI:0
A3	LVD_SCSI:28	B3	LVD_SCSI:27
A4	LVD_SCSI:3	B4	LVD_SCSI:2
A5	LVD_SCSI:30	B5	LVD_SCSI:29
A6	LVD_SCSI:5	B6	LVD_SCSI:4
A7	LVD_SCSI:32	B7	LVD_SCSI:31
A8	LVD_SCSI:7	B8	LVD_SCSI:6
A9	LVD_SCSI:34	B9	LVD_SCSI:33
A10	LVD_SCSI:9	B10	LVD_SCSI:8
A11	LVD_SCSI:36	B11	LVD_SCSI:35
A12	LVD_SCSI:11	B12	LVD_SCSI:10
A13	LVD_SCSI:38	B13	LVD_SCSI:37
A14	LVD_SCSI:13	B14	LVD_SCSI:12
A15	LVD_SCSI:40	B15	LVD_SCSI:39
A16	LVD_SCSI:15	B16	LVD_SCSI:14
A17	LVD_SCSI:42	B17	LVD_SCSI:41
A18	LVD_SCSI:17	B18	LVD_SCSI:16
A19	LVD_SCSI:44	B19	LVD_SCSI:43
A20	LVD_SCSI:19	B20	LVD_SCSI:18
A21	LVD_SCSI:46	B21	LVD_SCSI:45
A22	LVD_SCSI:21	B22	LVD_SCSI:20
A23	LVD_SCSI:48	B23	LVD_SCSI:47
A24	LVD_SCSI:23	B24	LVD_SCSI:22
A25	LVD_SCSI:50	B25	LVD_SCSI:49
A26	LVD_SCSI:25	B26	LVD_SCSI:24
A27	LVD_SCSI:52	B27	LVD_SCSI:51
A28	LVD_SCSI:53	B28	LVD_SCSI:26
A29	Ground	B29	Ground
A30	DRVPRSN:0	B30	DRVACT:0
A31	DRVPRSN:1	B31	DRVACT:1
A32	DRVPRSN:2	B32	DRVACT:2
A33	DRVPRSN:3	B33	DRVACT:3
A34	DRVPRSN:4	B34	DRVACT:4
A35	Ground	B35	Ground
A36	DIFFSENSE	B36	PWRON:0
A37	FAN_CNTRL	B37	PWRON:1
A38	FAN1_TACH	B38	PWRON:2
A39	FAN2_TACH	B39	PWRON:3

Pin	Signal	Pin	Signal
A40	Ground	B40	PWRON:4
A41	IMB_SDA	B41	Ground
A42	IMB_CLK	B42	VCC
A43	I2C_ADDR_CNTRL	B43	VCC
A44	Ground	B44	Ground
A45	Ground	B45	Ground
A46	Ground	B46	Ground
A47	Ground	B47	+12V
A48	Ground	B48	+12V
A49	Ground	B49	Ground
A50	Ground	B50	Ground
A51	Ground	B51	Ground
A52	Ground	B52	Ground
A53	Ground	B53	Ground
A54	Ground	B54	Ground
A55	Ground	B55	Ground
A56	Ground	B56	Ground
A57	Ground	B57	Ground
A58	Ground	B58	Ground
A59	Ground	B59	Ground
A60	Ground	B60	Ground
A61	Ground	B61	Ground
A62	Ground	B62	Ground

5.5.2 Mechanical Specifications

The following figure shows the mechanical dimensions of the hard disk drive bay. All dimensions are given in inches.

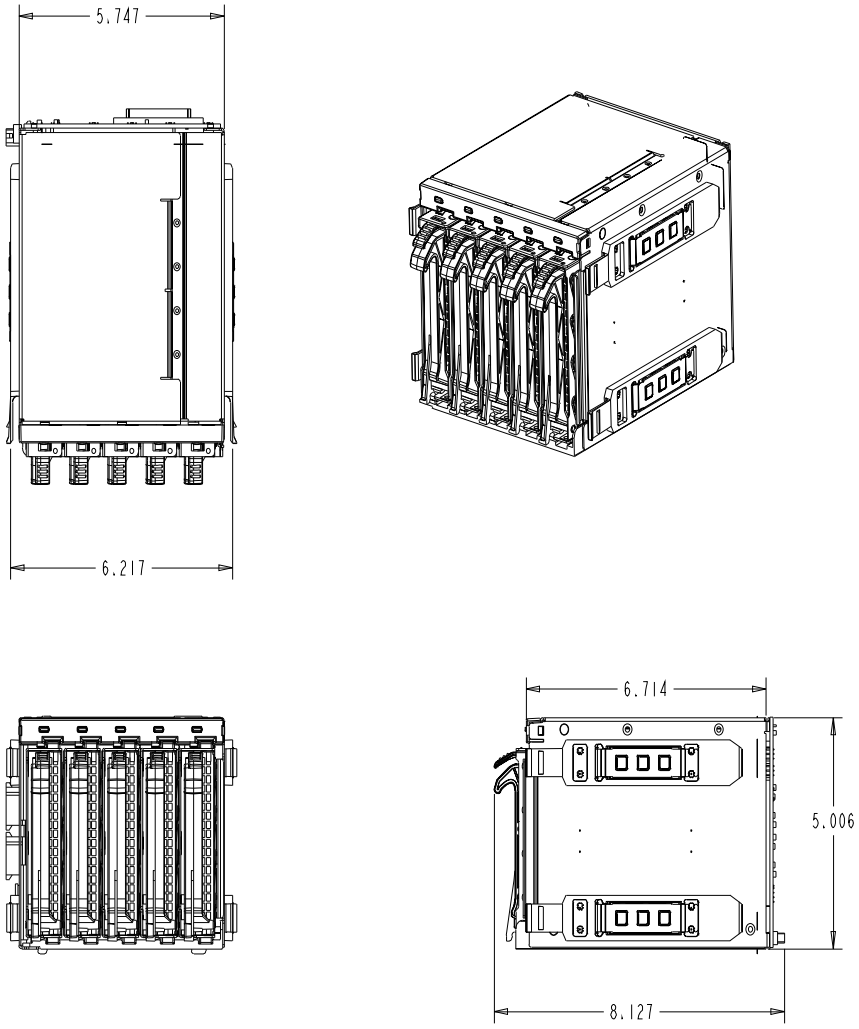


Figure 5-4: Hard Disk Drive Bay Mechanical Drawing

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6. Front Panel Board

6.1 Features

- Switches for power, sleep, reset and NMI.
- Indicator lights for power, disk activity, network activity and failure.

6.2 Overview

The front panel is located in the right-hand side of the front of the chassis. Opening the bezel door allows access to the momentary power on/off button, system reset button, ACPI sleep switch and tool activated NMI switch. The front panel includes a green power-on LED, a green hard drive activity LED, a green network activity LED and an amber general system fault LED, which are visible with the exterior access door closed. When the hot-swap drive bay is installed, five bi-color hard drive LEDs located on the drive bay indicate specific drive failure or activity, and are visible upon opening the front bezel door.

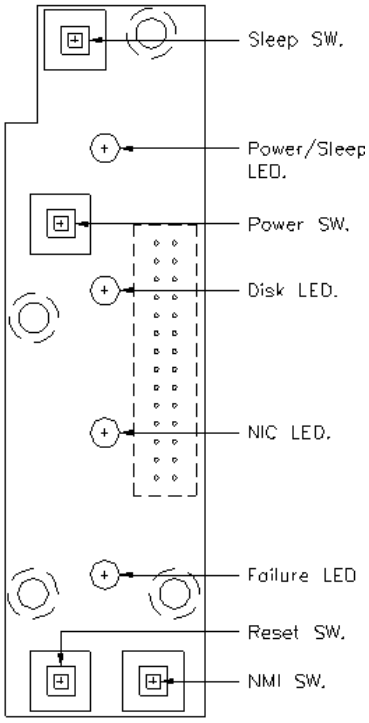

Figure 6-1: SRKA4 Server System Front Panel Board Components

6.3 Connector Interface

The signal mnemonics defined here may appear in descriptive text in the document. A suffix of "_L" on the signal name indicates that the signal is active-low.

Table 6-1: Front Panel Board Connector Pinout

		Front Panel Connector
Pin #	I/O	Description
1	I	Power LED Anode
2	-	Reserved
3	Key	Key
4	I	System Fault LED Anode
5	I	Power LED Cathode
6	I	D5 isolation diode Cathode
7	I	Hard Drive Activity LED Anode
8	-	Reserved
9	I	Hard Drive Activity LED Cathode
10	I	D6 isolation diode Cathode
11	O	Open Collector Low True = toggle system power
12	I	NIC Activity LED Anode
13	PWR	GND
14	I	NIC Activity LED Cathode
15	O	Open Collector Low True = reset system
16	-	Reserved
17	PWR	GND
18	-	Reserved
19	O	Open Collector Low True = toggle ACPI sleep
20	-	Reserved
21	PWR	GND
22	-	Reserved
23	O	Open Collector Low True = NMI to CPU
24	-	Reserved

6.4 Specifications

Figure 6-3 shows the mechanical specifications of the front panel board on the SRKA4 server system. All dimensions are given in millimeters.

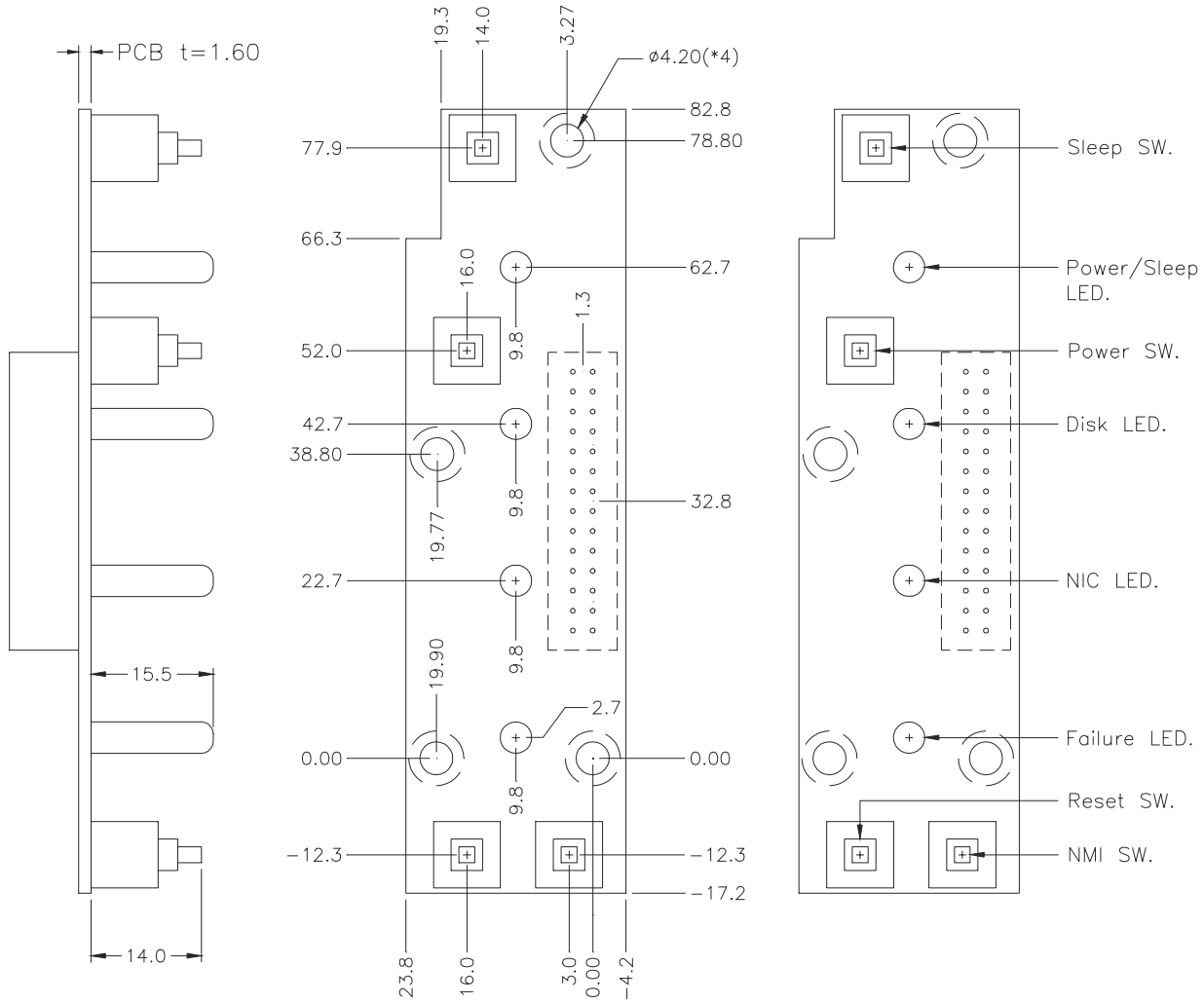

Figure 6-3: Front Panel Board Mechanical Specifications

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7. Fan Carrier Board

This chapter describes the design and external interface of the SRKA4 server system fan carrier board.

7.1 Features

- Fan control, monitoring, presence detect, and individual fan fail indication.
- Buzzer.
- Operation from standby power.

7.2 Overview

The fan carrier board on the SRKA4 server system serves as an interface between the SKA4 baseboard and the SRKA4 server system as a whole. All six of the system fans can be hot-swapped into the fan carrier board. Circuitry located on the fan carrier board controls the fan speed, monitors individual fan tachometer signals, monitors individual fan presence, and indicates (via LEDs) whether an individual fan failed in the system. All of these functions are controlled via the SKA4 BMC. Nine connectors reside on the fan carrier board, a 30-pin RA (SKA4 interface), a 24-pin RA (front panel interface), a 6-pin RA (12 V power and speed control signal), and six fan connectors. The system speaker also resides on the fan carrier board.

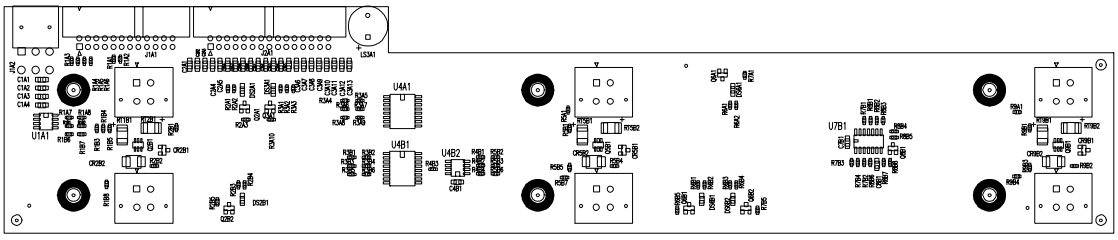

Figure 7-1: SRKA4 Server System Fan Carrier Board Components

7.3 Functional Description

7.3.1 Dual Speed Fan Control

The fan voltage has a low setting to minimize acoustic noise. Under normal conditions, the fans run at the slower, quieter speed. Under some conditions the fan speed is set to high. The high/low decision is made by the BMC. These conditions may include:

- A fan failure is sensed
- A fan is not detected
- The ambient temperature sensor reads 30^{o} C or higher (there is 2^{o} C of hysteresis built into this algorithm, so the ambient temperature must drop to 28^{o} C before the fan speed is reduced to low after having been set to high).

The speed of the six system fans is controlled by a PWM circuit, which resides on the fan carrier board. The duty cycle of the PWM circuit is controlled by the signal A_FAN_2P5V. This signal is delivered by the SKA4 baseboard via the 6-pin RA connector (J1A2). The maximum current during full-speed operation is approximately 3.36 A.

7.3.2 Fan Speed Monitoring

Each fan has its own tachometer output signal. All six tachometer signals, FAN_TACH_1-FAN_TACH_6, are routed to the SKA4 baseboard via the 30-pin RA connector (J3A1). The BMC determines if each fan is operating within the predetermined fan speed specification.

7.3.3 Fan Failure Indication/Fan Presence Detect

If a fan is determined to have failed or if it is not present in the system, the COOLING_FAULT_L signal turns on the yellow failure LED on the front panel. The LED that indicates which fan has failed also illuminates. This individual fan failure LED is driven by the PCF8574 I/O expander (U4A1) with BMC communication via the private I^2C bus.

Fan presence detect gives the system the ability to determine if each fan is present in the system. If a system fan is not present in the system, a fan failure is indicated as described above. This individual fan presence detect is sensed by the PCF8574 I/O expander (U4B1), with BMC communication via the private I^2C bus.

7.3.4 Serial EEPROM/Temperature Sensor

The serial EEPROM is accessible on the BMC's private I^2C bus. See the Atmel* literature on the AT24C02 for accessing this device. A DS1621* temperature sensor is also on the private I^2C bus, which is used to sense the ambient temperature outside the system. It should be placed as close to the front of the system as possible to allow accurate sensing.

7.3.5 Speaker

The speaker impedance is approximately 80 ohm and resides on the fan carrier board. The speaker is commanded by the SKA4 baseboard via pin #1 on the 30-pin RA connector.

7.3.6 I^2C Interfaces

The BMC interfaces to two I^2C buses, the BMC's private I^2C bus and the IMB or global I^2C bus. These are described in the following sections.

7.3.6.1 BMC Private I^2C Bus

The BMC's private I^2C bus is used for the BMC to communicate with dumb I^2C devices that do not support multimaster mode. These are shown in Table 7-1.

Table 7-1: BMCs Private I^2C Bus Devices

Device	Part Number	Address
Fan Board 1/4 KB by 8 Serial EEPROM (used for FRU)	Intel® 666529-002 Atmel* AT24C02	U4B2 = AAH
Fan Board Ambient Temperature	Intel 644106-151	U1A1 = 9AH

Device	Part Number	Address
Sensor	Dallas* DS1621	
Fan Board I^2C I/O Expander (used for Fan Presence Detect U4B1 and Individual Fan Fail indication U4A1)	Intel 626455-001 Phillips* PCF8574	U4A1 = 4EH U4B1 = 4CH

7.3.6.2 IMB I^2C Bus

The public I^2C bus (IMB bus) is automatically connected to the main I^2C bus whenever power is valid. This bus is used to allow communication between smart I^2C devices that operate in multimaster mode. Specifically, this bus connects the BMC and the HSC. The IMB bus is connected to the fan carrier board via the 30-pin RA connector, but currently is not routed to any other node on the board.

7.4 Connector Interface

The signal mnemonics defined here may appear in descriptive text in the document. An "_L" as a suffix on the signal name indicates that the signal is active-low. (**Note:** this is the same convention used in schematics and simulations.) Two colons between numbers indicate a range of signals (for example, AD[31::0]).

Table 7-2: 30-Pin J3A1 Connector

Pin	Fan Board Signal	Pin	Fan Board Signal
1	SPEAKER_IN	16	PF_PWR_SW_L
2	GND	17	NC
3	NC	18	GND
4	FP_HD_ACT_L	19	FAN_TACH_1
5	VCC	20	FAN_TACH_2
6	FP_SLEEP_SW_L	21	FAN_TACH_3
7	COOLING_FAULT_LED_L	22	FAN_TACH_4
8	POWER_LED_L	23	FAN_TACH_5
9	SYSTEM_FAULT_L	24	FAN_TACH_6
10	GND	25	NC
11	SM_IMB_5V_SDA	26	NC
12	FP_NMI_SW_L	27	NIC_ACTIVITY_L
13	SM_IMB_5V_SCL	28	NC
14	FP_RST_SW_L	29	SM_PRI_5V_SCL
15	SB5V	30	SM_PRI_5V_SDA

Table 7-3: 24-Pin J1A1 Connector

Pin	Fan Board Signal	Pin	Fan Board Signal
1	SB5V	13	GND
2	NC	14	NIC_ACTIVITY_L
3	NC	15	FP_RST_SW_L
4	SB5V	16	NC
5	POWER_LED_L	17	GND
6	COOLING_FAULT_LED_L	18	NC
7	VCC	19	FP_SLEEP_SW_L
8	NC	20	NC
9	FP_HD_ACT_L	21	GND
10	SYSTEM_FAULT_L	22	NC
11	FP_PWR_SW_L	23	FP_NMI_SW_L
12	SB5V	24	NC

Table 7-4: 6-Pin J1A2 Connector

Pin	Fan Board Signal	Pin	Fan Board Signal
1	+12V	4	+12V
2	A_FAN_2P5V	5	NC
3	GND	6	GND

7.5 Specifications

7.5.1 Absolute Maximum Ratings

Operating the fan carrier board at conditions beyond those shown in the Table 7-5 may cause permanent damage to the board. Exposure to absolute maximum rating conditions for extended periods may affect its reliability.

Table 7-5: Absolute Maximum Ratings

Voltage on any signal with respect to ground	5.5 Vdc
SB5 V supply voltage with respect to ground	5.5 Vdc
5 V supply voltage with respect to ground	5.5 Vdc
+12 V supply voltage with respect to ground	13.2 Vdc

7.5.1.1 Power Connection

Table 7-6 describes the pinout for the six fan connectors (X= Fan #).

Table 7-6: Fan Connector Pinout

Pin	Signal
1	FAN_PRES_X_L
2	FAN_BANK_X
3	GND
4	FAN_TACH_X

7.5.2 Mechanical Specifications

Figure 7-2 shows the mechanical specifications of the fan carrier board on the SRKA4 server system. All dimensions are given in inches.

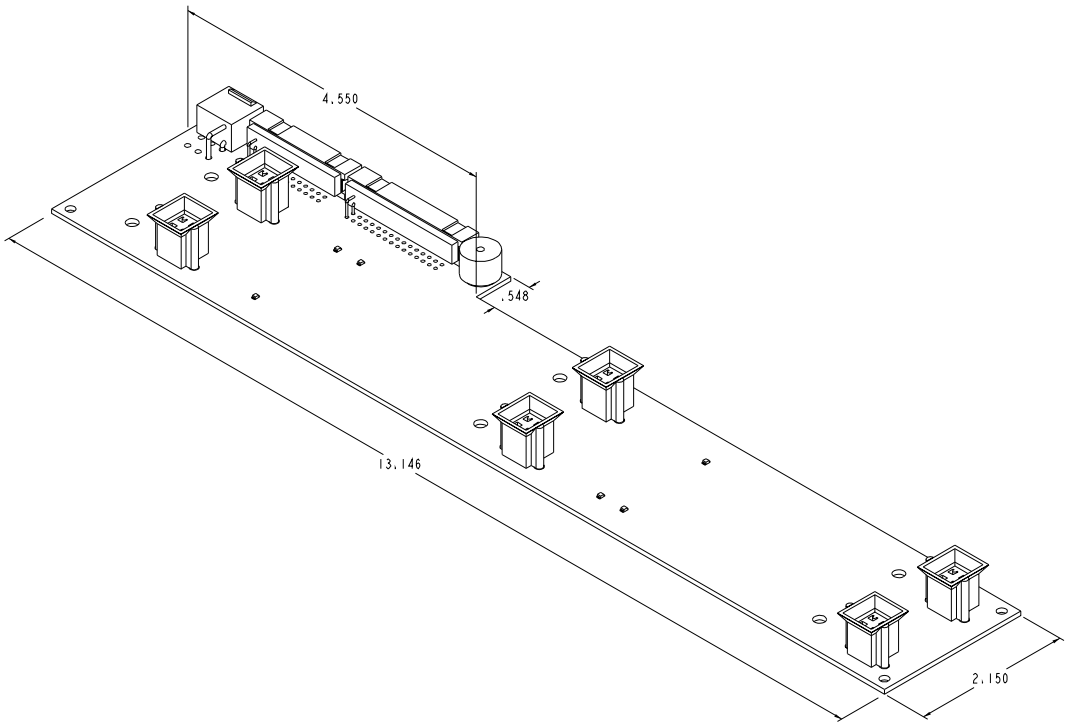

Figure 7-2: Fan Carrier Board Mechanical Specifications

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8. Regulatory Specifications

The SRKA4 server system meets the specifications and regulations for safety and EMC defined in this chapter.

8.1 Safety Compliance

USA/Canada:	UL 1950, 3rd Edition/CSA 22.2, No. 950-M93, 3rd Edition
Europe:	Low Voltage Directive, 73/23/EEC TUV/GS to EN60950 2nd Edition with Amendments, A1 = A2 + A3 + A4
International:	CB Certificate and Report to IEC 950, 2nd Edition w/ A1 + A2 + A3 + A4 including EMKO-TSE (74-SEC) 207/94

8.2 Electromagnetic Compatibility

USA	FCC 47 CFR Parts 2 and 15, Verified Class A Limit
Canada	IC ICES-003 Class A Limit
Europe	EMC Directive, 89/336/EEC EN55022, Class A Limit, Radiated & Conducted Emissions EN55024 ITE Immunity Requirements EN61000-4-2 ESD Immunity (level 2 contact discharge, level 3 air discharge) EN61000-4-3 Radiated Immunity (level 2) EN61000-4-4 Electrical Fast Transient (level 2) EN61000-4-5 Surge EN61000-4-11 Voltage Dips, Interruptions and Variations EN61000-3-2 Harmonic Currents
Australia/New Zealand	AS/NZS 3548, Class A Limit
Taiwan	BSMI (CNS14438, Class A)
Korea	RRL (CISPR 22, Class A)
Japan	VCCI Class A ITE (CISPR 22, Class A Limit). IEC 1000-3-2; Harmonic Currents
Russia	GOST (EN60950, EN55022, EN55024, Acoustics)
International	CISPR 22, Class A Limit

8.3 CE Mark

The CE marking on this product indicates that it is in compliance with the European Union's EMC Directive 89/336/EEC, and Low Voltage Directive, 73/23/EEC.

8.4 Electromagnetic Compatibility Notice (USA)

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if

not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case, the user will be required to correct the interference at his own expense.

8.5 Electromagnetic Compatibility Notices (International)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:
This is a Class A product based on the standard of the Voluntary Control Council for Interference by Information Technology Equipment (VCCI). If this equipment is used in a domestic environment, radio disturbance may arise. When such trouble occurs, the user may be required to take corrective actions.

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: “Appareils Numériques”, NMB-003 édictée par le Ministre Canadian des Communications.

English translation of the notice above:
This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled “Digital Apparatus,” ICES-003 of the Canadian Department of Communications.

Appendix A: Glossary

Term	Definition
AC	Alternating current
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
APIC	Advanced Programmable Interrupt Controller
ASIC	Application specific integrated circuit
BIOS	Basic input/output system
BMC	Baseboard management controller
CE	Community European
CFM	Cubic feet per minute
CISPR	International Special Committee on Radio Interference
CSA	Canadian Standards Organization
CTS	Clear to send
DAT	Digital audio tape
dB	Decibel
dBA	Acoustic decibel
DC	Direct current
DIMM	Dual inline memory module
DMI	Desktop management interface
DRAM	Dynamic random access memory
DSR	Data set ready
DTR	Data terminal ready
ECC	Error checking and correcting
EEPROM	Electrically erasable programmable read-only memory
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EMP	Emergency management port
EN	European Standard (Norme Européenne or Europäische Norm)
EPS	External product specification
ESCD	Extended system configuration data
ESD	Electrostatic discharge
ESR	Equivalent series resistance
FPC	Front panel controller
FRB	Fault resilient booting
FRU	Field replaceable unit
HPIB	Hot-plug indicator board
HSC	Hot-swap controller
Hz	Hertz – 1 cycle/second
I/O	Input/output
i^2t	i^2tproduct = peak current^2 * time duration of pulse. Parameter by which some current carrying devices are rated (spec'd) before the "fuse" blows.
ICMB	Intelligent Chassis Management Bus
IDE	Integrated drive electronics

Term	Definition
IEC	International Electrotechnical Commission
IMB	Intelligent management bus
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Initiative
IRQ	Interrupt request line
ITE	Information technology equipment
ITP	In-target probe
JAE	Japan Aviation Electronics
LED	Light-emitting diode
LVDS	Low voltage differential SCSI
mA	Milliamp
MEC	Memory expansion card
MTTR	Mean time to repair
mΩ	Milliohm
NEMKO	Norges Elektriske Materiellkontroll (Norwegian Board of Testing and Approval of Electrical Equipment)
NIC	Network interface card
NMI	Nonmaskable interrupt
OS	Operating system
OTP	Over-temperature protection
OVP	Over-voltage protection
PCB	Printed circuit board
PCI	Peripheral component interconnect
PHP	PCI hot-plug
PID	Programmable interrupt device
PIRQ	PCI interrupt request line
PSU	Power supply unit
PWM	Pulse-width-modulation
SAF-TE	SCSI Accessed Fault-Tolerant Enclosures
SCA	Single connector attachment
SCL	Serial clock
SCSI	Small Computer Systems Interface
SDR	Sensor data records
SDRAM	Synchronous dynamic RAM
SEC	Single edge connector
SEL	System event log
SEMKO	Sverge Elektriske Materiellkontroll (Swedish Board of Testing and Approval of Electrical Equipment)
SMI	System management interrupt
SMM	Server management mode
SMP	Symmetric multiprocessing
SMS	Server management software
SPD	Serial presence detect
SSI	Server system infrastructure
TUV	Technischer Uberwachungs-Verein (A safety testing laboratory with headquarters in Germany)

Term	Definition
UL	Underwriters Laboratories, Inc.
USB	Universal Serial Bus
UV	Under-voltage
V	Volt
VA	Volt-amps (volts multiplied by amps)
Vac	Volts alternating current
VCCI	Voluntary Control Council for Interference
Vdc	Volts direct current
VDE	Verband Deutscher Electrotechniker (German Institute of Electrical Engineers)
VRM	Voltage regulator module
VSB	Voltage standby
W	Watt
WfM	Wired for Management
Ω	Ohm
µF	Microfarad
µs	Microsecond

Appendix B: Reference Documents

Refer to the following documents for additional information:

ACPI

- *Advanced Configuration And Power Interface Specification*, Revision 1.0b, http://www.teleport.com/~acpi/.

Boot

- *BIOS Boot Specification*, Version 1.01, http://www.ptltd.com/techs/specs.html.
- *El Torito CD-ROM Boot Specification*, Version1.0, http://www.ptltd.com/techs/specs.html.

DMI

- *Desktop Management Interface (DMI) Specification*, Version 2.0s, Desktop Management Task Force, Inc., http://www.dmtf.org/spec/dmis.html.

ESCD

- *Extended System Configuration Data Specification*, Version 1.02a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

Ethernet

- *Intel 82559 Fast Ethernet Multifunction PCI/Cardbus Controller Datasheet*, Intel Corporation, http://developer.intel.com/design/network/datashts/738259.htm.

Flash

- *Intel 5 VOLT FlashFile™ Memory (28F008SA x8) Datasheet*, December 1998, Intel Corporation, Number 290429-008, http://developer.intel.com/design/flcomp/datashts/290429.htm.

I_2O

- *Intelligent Input/Output (I_2O) Architecture Specification*, Revision 1.0, I_2O Special Interest Group, http://www.i2osig.org/.

MPS

- *Multiprocessor Specification*, Version 1.4, Intel Corporation, http://www-techdoc.intel.com/design/intarch/manuals/242016.htm.

PC100 SDRAM

- *PC SDRAM Registered DIMM Specification*, Revision 1.2, Intel Corporation, http://developer.intel.com/design/chipsets/memory/index.htm.

- *PC SDRAM Specification*, Revision 1.63, Intel Corporation, http://developer.intel.com/design/chipsets/memory/index.htm.
- *PC SDRAM Serial Presence Detect (SPD) Specification*, Revision 1.2A, Intel Corporation, http://developer.intel.com/design/chipsets/memory/index.htm.

PCI

- *PCI Bus Power Management Interface Specification*, Revision 1.1, PCI Special Interest Group, http://www.pcisig.com/.
- *PCI Local Bus Specification*, Revision 2.1, PCI Special Interest Group, http://www.pcisig.com/.
- *PCI Hot-plug Specification*, Revision 1.0, PCI Special Interest Group, http://www.pcisig.com/.
- *PCI Hot-plug Application and Design*, Alan Goodrum, ISBN 0-929392-60-4.
- *Compaq PCI Hot-Plug Megacell Specification.*

Phoenix* BIOS

- *Phoenix BIOS* 6.0 Users Manual*, Phoenix Technologies Ltd.

PID

- *Programmable Interrupt Device External Product Specification*, Revision 1.1, Intel Corporation, Document number OR4-680777.

Plug and Play

- *Plug and Play BIOS Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.
- *Clarification to Plug and Play BIOS Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.
- *Plug and Play ISA Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.
- *Clarification to Plug and Play ISA Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

PMM

- *POST Memory Manager Specification*, Version 1.01, http://www.ptltd.com/techs/specs.html.

ServerWorks Chip Set

- *ServerWorks Champion 2.0 North Bridge (CNB20HE) Specification*, Version 1.8.
- *ServerWorks Champion 2.0 Open South Bridge (OSB4) Specification*, Version 1.16.
- *ServerWorks Champion 2.0 Memory Address and Data Path (MADP) Specification*, Version 1.5.
- *ServerWorks Champion 2.0 I/O Bridge (CIOB) Specification*, Version 1.6.

Regulatory

- *CISPR 22: Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment*, 2nd Edition.
- *CFR 47: Federal Communications Commission (FCC) Compliance with the Class A Limits for Computing Devices (FCC Mark)*, Part 2 & 15.
- *ANSI C63.4: American National Standard for Methods of Measurement of Radio-Noise Emissions from Low Voltage Electronic Equipment in the Range of 9kHz to 40GHz for EMI Testing*, 1992.
- *CISPR 24: Information Technology Equipment - Immunity Characteristics Limits and Methods of Measurement*, 1st Edition.
- *ICES-003: Canadian Radio Interference Regulations for Digital Apparatus*.
- *EN 61000-3-2: Electromagnetic Compatibility (EMC) Part 3: Limits - Section 2: Limits for Harmonic Current Emissions.*
- *JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment*.

SCSI

- *Adaptec AIC-7899 Dual-Channel PCI-to-Ultra 160/M SCSI Single-Chip Host Adapter Specification*, http://www.adaptec.com/.
- *Adaptec AIC-7880 PCI Bus-to-Ultra SCSI Single-Chip Bus Master Host Adapter Specification*, http://www.adaptec.com/.
- *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification*, http://www.safte.org/.

Server Management

- *Emergency Management Port v1.0 Interface External Product Specification*, Revision 0.83, Intel Corporation.
- *Intelligent Platform Management Interface (IPMI) Specification*, Version 1.0, Revision 1.1, Intel Corporation, http://developer.intel.com/design/servers/ipmi/spec.htm.

SMBIOS

- *System Management BIOS Reference Specification*, Version 2.3, http://www.ptltd.com/techs/specs.html.

Super I/O

- *National PC97317 Super I/O Plug and Play Compatible Chip with ACPI-Compliant Controller/Extender*, http://www.national.com/pf/PC/PC97317.html.

USB

- *Universal Serial Bus Specification*, Revision 1.0, http://www.usb.org/developers.

VGA

- *ATI Rage IIC Technical Reference Manual*.
- *ATI-264 VT4 Graphics Controller Technical Reference Manual*.

Wired for Management

- *Wired for Management (WfM) Baseline Specifications*, Version 2.0, Intel Corporation, http://developer.intel.com/ial/wfm/wfmspecs.htm.

Windows

- *Hardware Design Guide for Microsoft Windows NT Server*, Version 2.0, http://www.microsoft.com/HWDEV/serverdg.htm.

Miscellaneous

- *VRM 8.3 DC-DC Converter Specification.*
- *VRM 8.4 DC-DC Converter Specification.*

Appendix C: Slim CD Specifications

The following specifications have been provided by the device manufacturer.

TEAC 224E 24x CD-ROM drive

General

Manufacturer	TEAC
Model Number	CD-224E-Bxx
Interface	IDE (ATAPI), 50 pin JAE KX15-50KLD type.
Compatible CD-ROM standards:	CD-DA, CD-ROM Mode 1 and Mode 2, CD-ROM XA Mode 2 (Form 1, Form 2), Single and Multi-session Photo CD, Video CD, CD-I, CD-Text, Enhanced CD, CD-R, CD-RW

Performance

User data capacity	650 MB, mode 1 748 MB, mode 2
Total number of blocks	33000 blocks
Data transfer rate	10.3X to 24X, 17.2X average, 1.55 MB/sec to 3.6, 25.8 MB/sec average
Rotational speed	5136 RPM, typical
IDE interface burst transfer rate	33.3 MB/sec (Ultra DMA)
Access time	115ms typical (Random stroke), by TEAC standard
Memory buffer	128KB

Reliability

MTBF	60,000POH or more (10% duty)
User Error Rates	Hard Error Rate (Mode 1 and Mode 2 Form 1): Block/10^{12} bit Soft Error Rate (Mode2 Form 2 and CD-DA): Block/10^{9} bit Seek Error Rate: Block/10^{6} bit

Audio

Sampling Frequency	44.1 kHz
Quantifying bit number	16 bit linear
Number of channels	2 channels (L, R stereo)
Frequency response	20-20,000 Hz (±3dB)
Signal-to-noise ratio	77dB or more (IHF A)
Total harmonic distortion	0.08% or less (1kHz, 400Hz to 30kHz BPF)
Wow and flutter	Below measurable limits
Line output	0.75Vrms, ±3dB

Environmental

Ambient Temperature	Operating: 5 to 55° C (41 to 131° F) Storage: -20 to 60° C (-4 to 140° F)
Relative Humidity	Operating: 8 to 80% (non-condensing), Max wet bulb temperature 29° C (84.2° F) or less Storage: 5 to 95% (non-condensing)
Acoustical Noise	45dBA or less (at distance of 0.5m, except at eject and loading operations)

Power

DC +5V

Operating voltage range	±5% (4.75 to 5.25V)
Allowable ripple voltage	100mV p-p or less (including spike noise)

Typical Current consumption at 5V

Standby	15mA
Idle	450mA
Active	800mA max.
Start/Seek	1.2A max.
Eject	1.4A max.

Physical

Height	12.7mm (0.5 in.), not including front bezel.
Width	128mm (5.04 in.), not including front bezel.
Depth	129.4mm (5.09 in.), not including eject button.
Weight	195g (0.43 lbs.)

Connectors

IDE/Power Interface connector	JAE KX15-50KLD or equivalent