SKA4 Baseboard and Memory Board

Technical Product Specification

Intel Order Number A45041-001

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Enterprise Products Group

Revision History

Date	Revision Number	Modifications
8/00	0.99	Initial release.
10/00	2.0	Extensive updates, additions and clarifications.
11/01	3.0	Extensive updates, additions and clarifications. Added errata section
04/23/02	4.0	Corrected chipset name which has been wrong since SRA

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PCI Hot-plug functionality is based upon a licensed design from Compaq Corporation.

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1. Introduction

This chapter provides an architectural overview of the SKA4 board set, including functional blocks and their electrical relationships.

Figure 1-1 shows the functional blocks of the SKA4 baseboard and MEC (Memory Expansion Card).

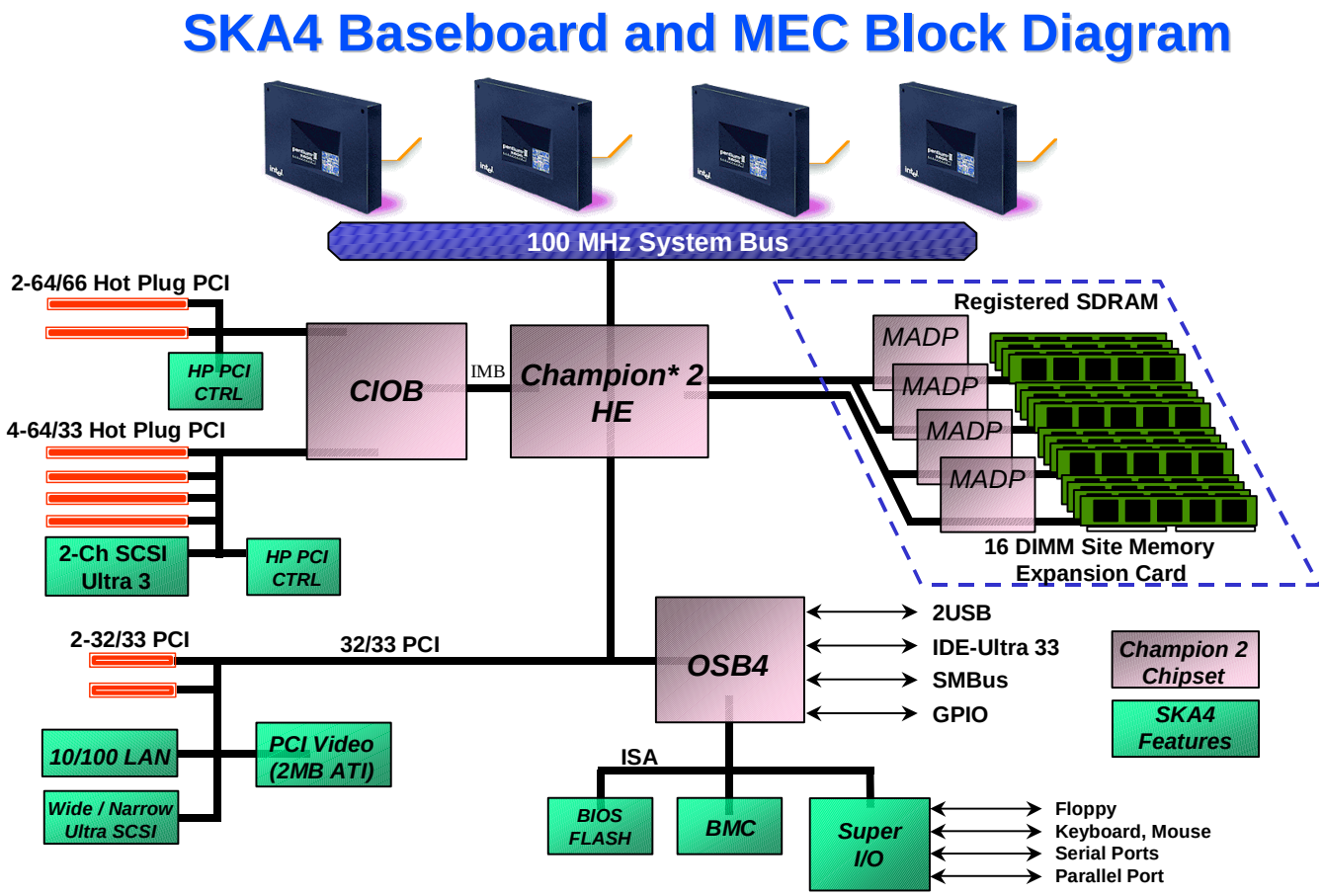

Figure 1-1: SKA4 Baseboard and MEC Block Diagram

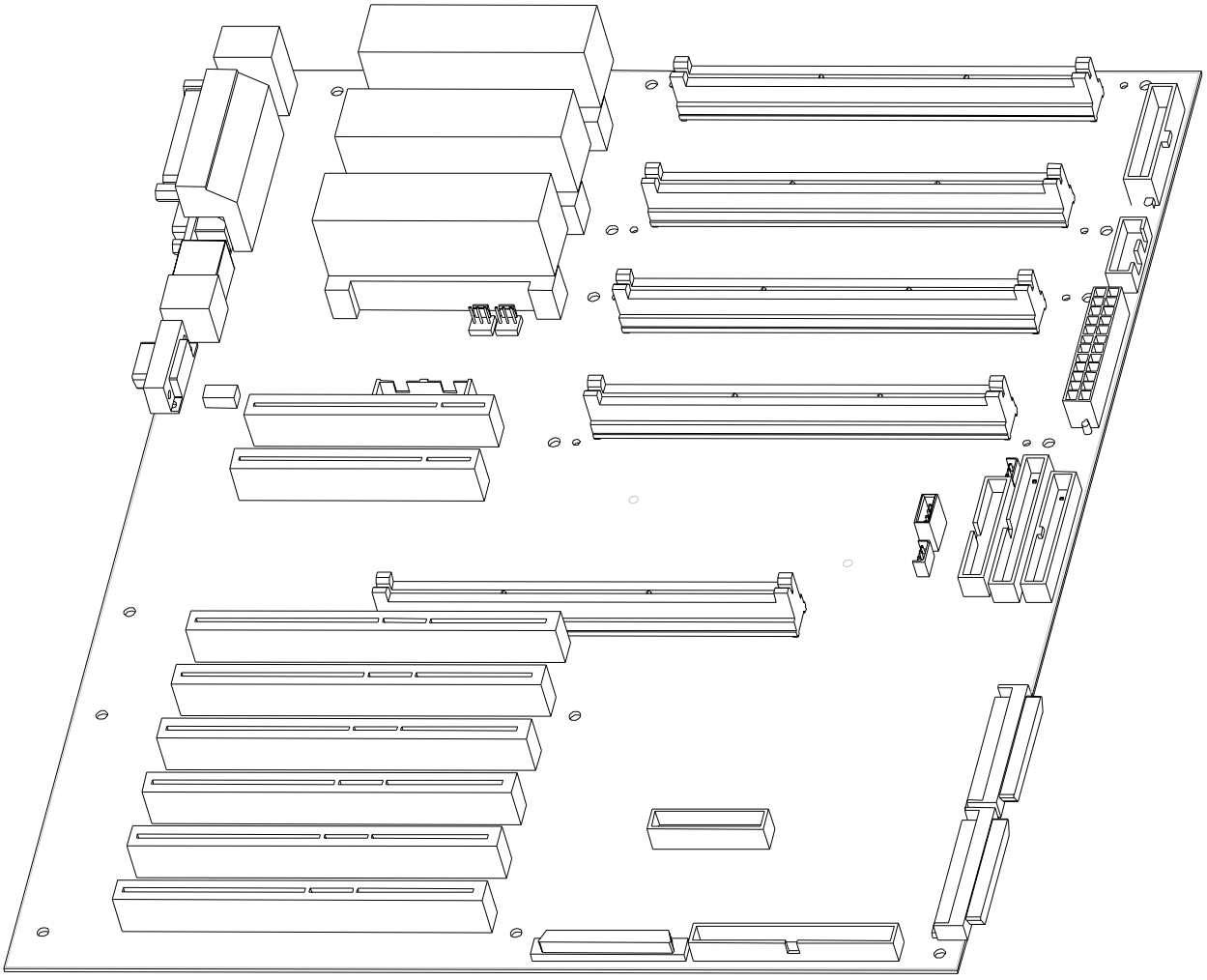

Figure 1-2: SKA4 Baseboard Preliminary Placement Diagram

1.1 SKA4 Architecture Overview

The SKA4 board set is designed around the Intel® Pentium® III Xeon™ processor and the ServerWorks* ServerSet III HE chipset. This combination provides the basis for a high performance system with leading edge processor, memory, and I/O performance.

The SKA4 baseboard architecture provides for four SC330.1-compliant processor connectors that support quad processing operation using Intel Pentium III Xeon processor cartridges. The baseboard also contains eight industry standard PCI expansion slots that support a mixture of 32-bit/33-MHz, 64-bit/33-MHz and 64-bit/66-MHz slots.

The processor baseboard provides an array of embedded I/O devices, including two SCSI controllers, providing four external connection points, and three independent channels at SCSI bus speeds up to 160 MB/sec, an embedded 10/100 Network Interface Controller, and a 2D/3D graphics accelerator. PCI Hot-plug support and server management and monitoring hardware are also included. These features and the others listed below make this one of the most highly integrated board sets in this class.

The SKA4 memory subsystem consists of a single memory expansion board. This board supports as many as 16 PC-100 compatible registered SDRAM memory modules (DIMMs). Each DIMM may provide up to 1 GB of memory capacity, providing up to 16 GB of system memory.

The SKA4 board set provides the following features:

- Quad Intel Pentium III Xeon processor cartridge support.
  - Four SC330.1 edge connectors for installation of one to four identical Intel Pentium III Xeon processor cartridges.
  - Four embedded VRMs and three VRM connectors to support four processor cartridges.
- ServerWorks ServerSet II HE chipset.
  - Champion 2 HE North Bridge (CNB20HE).
  - Open South Bridge (OSB4).
  - Champion 2 I/O Bridge (CIOB).
  - Memory Address and Data Path (MADP).
- Support for 16 PC-100-compliant registered ECC SDRAM DIMMs.
  - ECC single-bit correction, and multiple-bit error detection and memory scrubbing.
- 32-bit, 33-MHz 5V keyed PCI segment (P32-C) with two expansion connectors and three embedded devices.
  - PCI narrow/wide Ultra SCSI controller—Adaptec* AIC-7880 SCSI Controller.
  - PCI network interface controller—Intel® 82559 Fast Ethernet Controller.
  - 3D/2D Graphics Accelerator —ATI RAGE* IIC Video Controller.
- 64-bit, 66-MHz, 3.3V keyed Hot-plug PCI segment (P64-A) with two expansion connectors and one embedded device.
  - DesotoE2* PCI Hot-plug Controller.
- 64-bit, 33-MHz, 5V keyed PCI Hot-plug segment (P64-B) with four expansion connectors and two embedded devices.
  - DesotoE2 PCI Hot-plug Controller.
  - Dual Channel Wide Ultra/Ultra II/Ultra 160/M SCSI controller—Adaptec 7899 SCSI Controller.
- ISA bus segment with three embedded devices.
  - Super I/O controller chip providing all PC-compatible I/O (floppy, parallel, serial, keyboard, mouse).
  - Baseboard Management Controller (BMC) providing monitoring, alerting, and logging of critical system information obtained from embedded sensors on baseboard.
  - 8 megabit Flash device for system BIOS.
- Two externally accessible Universal Serial Bus (USB) ports.
- One IDE connector, supporting up to two ATA33 compatible devices.

1.2 Document Structure and Outline

The information contained in this document is organized into 13 chapters. The content of each chapter is summarized below:

Chapter 1: Introduction
Architectural overview of the SKA4 server board set showing functional blocks and identifying major features.

Chapter 2: Processor and Chipset
Detailed description of the chipset and the supported processors.

Chapter 3: Baseboard PCI I/O Subsystem
Detailed descriptions of the PCI I/O subsystem. Three PCI buses are detailed, with specifics on embedded devices and provided slots. Interrupt routing information is also provided.

Chapter 4: PCI Hot-plug
Detailed description of the PCI Hot-plug implementation, and the DesotoE2 ASICs used.

Chapter 5: SKA4 SDRAM Memory Board
Specifics of the 16 GB SDRAM memory board.

Chapter 6: Clock Generation and Distribution
Identification of the clock signals generated and used on the SKA4 board set, and detailed drawings of their implementation.

Chapter 7: SKA4 ACPI Implementation
Description of the SKA4 ACPI implementation.

Chapter 8: SKA4 System Bus Error Monitoring
Details regarding the types of error conditions monitored by the SKA4 board set and how they propagate to SMI#.

Chapter 9: Server Management
Detailed description of the Server Management hardware integrated on the SKA4 baseboard and memory board. I2C addresses and block diagrams are provided.

Chapter 10: Jumpers
Identification and description of all jumpers used on the SKA4 baseboard.

Chapter 11: Connections
Identification of all connectors on the SKA4 board set, by ‘J’ number and manufacturer's part number. Interfacing specifics are identified where applicable.

Chapter 12: Electrical and Thermal Specifications
Description of operational parameters and considerations, and other hardware specifications.

Chapter 13: Mechanical Specifications
Mechanical drawings of both the SKA4 Baseboard and Memory Board.

2. Processor and Chipset

2.1 Overview

The SKA4 processor / PCI bridge / memory subsystem consists of

- One to four identical Intel Pentium III Xeon processors
- The ServerWorks II HE chipset
- A plug-in memory board
- Support circuitry.

The baseboard houses four SC330.1 processor connectors, four embedded VRMs, and three VRM connectors that support VRM 8.3-compliant, plug-in voltage regulator modules.

The ServerWorks II HE chipset provides the 36-bit address / 64-bit data processor host bus interface, operating at 100 MHz in the AGTL+ signaling environment. The Champion II HE North Bridge (CNB20HE) provides an integrated memory controller, a high-speed I/O connection to the CIOB and a legacy PCI segment. The board set supports up to 16 GB of ECC memory, using registered SDRAM DIMMS that are PC-100 compliant.

Additional descriptions and features include the following:

- The ServerSet II HE chipset provides an integrated I/O Bridge and memory controller and a flexible I/O subsystem core (PCI), optimized for multiprocessor systems and standard high-volume (SHV) servers.
- Quad SC330.1-compliant edge connectors that accept the Intel Pentium III Xeon processors.
- A 330-pin connector interface to the memory expansion board.
- A processor host bus AGTL+ support circuitry, including termination power supply.
- Four embedded VRMs that provide Vtt power, cache power for all processor slots, and Vcc core for the first processor. Three sockets for plug-in VRMs provide Vcc core power for up to three additional processor cards.
- APIC bus support.
- Miscellaneous logic for reset configuration, processor card presence detection, ITP port, and server management.

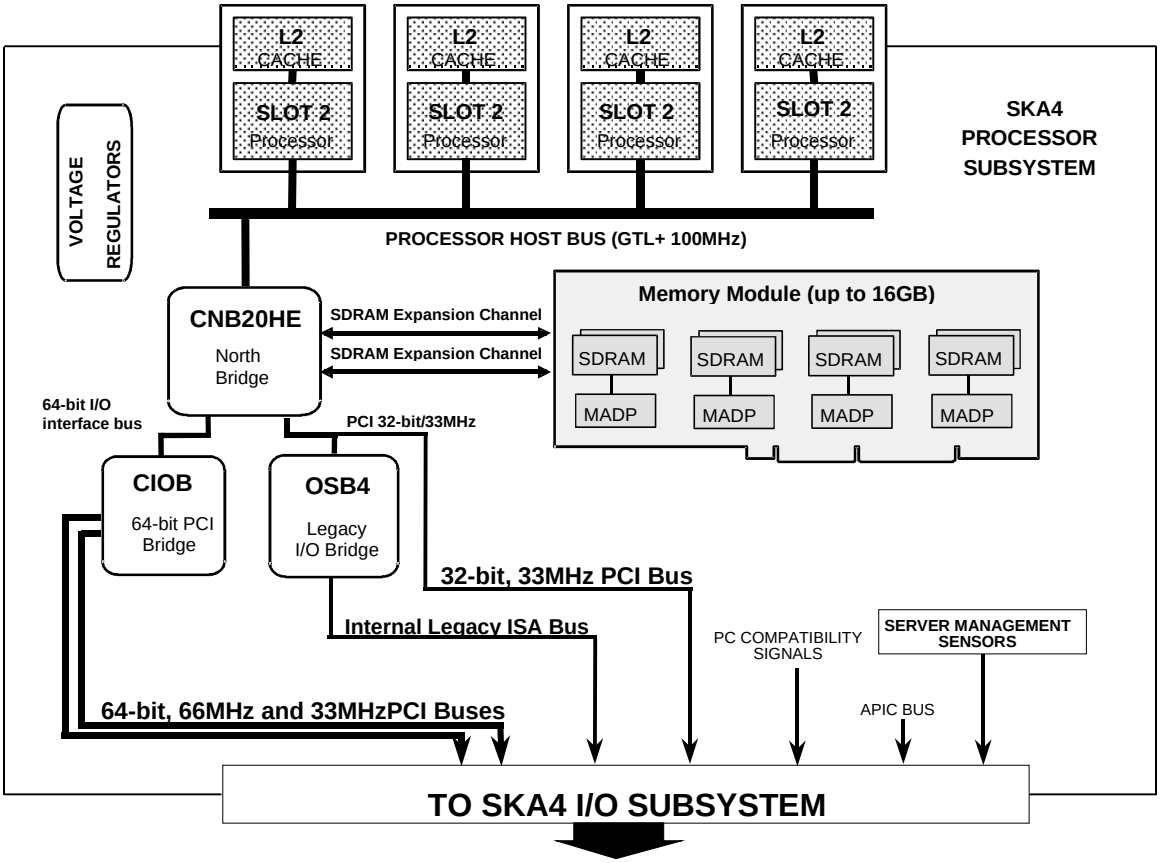

Figure 2-1: SKA4 Processor Functional Blocks

2.2 Processor Support

The SKA4 specifically supports all Pentium III Xeon processors at 500 MHz and 550 MHz with 512k, 1 MB, and 2 MB cache sizes. The SKA4 also supports the 2.8V 700 MHz and 900 MHz+ Pentium III Xeon processors with cache sizes of 1 MB and 2 MB. The SKA4 will not support the 256 KB cache size versions or the 5/12V 600MHz+ Pentium III Xeon processors. The table below summarizes this information.

Table 2-1: SKA4 Pentium® II Xeon™ and Pentium® III Xeon™ Processor Support Matrix

Name	Frequency	Cache Size	Support
Pentium® II Xeon™ processor	**500MHz 550MHz**	**512k, 1M, 2M**	**Yes**
Pentium III Xeon processor	600MHz +	256k	No
2.8V Pentium III Xeon processor	**600MHz +**	**1M, 2M**	**Yes**
5/12V Pentium III Xeon processor	600MHz +	1M, 2M	No
2.8V Pentium III Xeon processor	**700MHz +**	**1M, 2M**	**Yes**
2.8V Pentium III Xeon processor	**900MHz +**	**1M, 2M**	**Yes**

The supported processor package conforms to the Single Edge Contact (SEC) cartridge form factor and provides a thermal plate for heat sink attachment with a plastic cover located opposite the thermal plate.

The Pentium III Xeon processor cartridge edge connector conforms to the SC330.1 (“Slot 2”) specification, which can also accommodate future processor cartridges. The SC330.1 processor cartridge connectors are keyed to ensure proper orientation.

As with previous versions of Intel Pentium Pro processors, the Intel Pentium III Xeon processor card external interface is designed to be multi-processor (MP)-ready. Each processor contains a local APIC section for interrupt handling. When four processor cards are installed, all processor cards must be of identical revision, core voltage, cache voltage and bus/core speeds.

Note: All processor slots must be populated with either a processor or a termination card. The BMC will not allow DC power to be applied to the system unless all four SC330.1 slots contain a properly seated processor or termination card.

Note: Processors must be populated in the correct sequential order. That is, processor slot #1 must be populated prior to populating processor slot #2, processor slots #1 & #2 must be populated prior to populating slot #3, and so on.

2.2.1 Processor Bus Termination/Regulation/Power

The termination circuitry required by the Intel Pentium III Xeon processor bus (AGTL+) signaling environment, and the circuitry to set the AGTL+ reference voltage, are implemented directly on the processor cards. The baseboard provides 1.5 V AGTL+ termination power (VTT), and VRM 8.3-compliant DC-to-DC converters to provide processor power (VCCP) at each connector.

The baseboard provides three embedded and three VRM sockets to power the processors, which derive power from the +5 V and 12 V supplies. Each processor has a separate VRM to power its core; however, two processors share a VRM to power their cache. For more information, see the *VRM 8.3 DC-DC Converter Specification*.

2.2.2 Miscellaneous Processor Subsystem Logic

In addition to the circuitry described above, the processor subsystem contains the following:

- Reset configuration logic.
- Processor card presence detection circuitry.
- APIC bus.
- Server management registers and sensors.

2.2.2.1 Reset Configuration Logic

On the SKA4 platform, the BMC is responsible for configuring the processor speeds. The BMC uses the processor speed information (derived from the Pentium III Xeon processor SECC FRU devices) to determine the appropriate speed to program into the speed setting device (I^2C*-based EEPROM Mux).

The processor information is read at every system power-on. The EEMUX is set to correspond to the speed of the slowest processor.

Note: Manual processor speed setting options do not exist either in the form of a BIOS setup option or jumpers.

2.2.2.2 Processor Card Presence Detection

Logic is provided on the baseboard to detect the presence and identity of installed processors or termination cards. This keeps the system from powering on if an empty connector is detected, thus preventing operation of the system with an improperly terminated AGTL+ processor bus. The BMC checks this logic and will not turn on the system DC power until the bus is terminated properly. If any SEC processor cartridge is not installed in the system, a termination card must be installed in the vacant SEC processor cartridge slot to ensure reliable system operation. The termination card contains AGTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector.

2.2.2.3 APIC Bus

Interrupt notification and generation for the processors is accomplished with an independent path between local APICs in each processor and the I/O APIC in the OSB4 located on the baseboard. This independent bus consists of two data signals and one clock line.

2.2.3 Server Management Registers and Sensors

The baseboard management controller manages registers and sensors associated with the processor/memory subsystem. For more information, refer to the Section 9, Server Management.

2.3 ServerWorks ServerSet II HE Chipset

The ServerWorks ServerSet II HE chipset provides an integrated I/O bridge and memory controller and a flexible I/O subsystem core (PCI), targeted for multiprocessor systems and standard high-volume servers based on the Intel Pentium III Xeon processor. The ServerWorks ServerSet IIII HE chipset consists of four components, as listed below:

- **CNB20HE—Champion North Bridge.** The CNB20HE is responsible for accepting access requests from the host (processor) bus and for directing those accesses to memory or to one of the PCI buses. The CNB20HE monitors the host bus, examining addresses for each request. Accesses may be directed to a memory request queue, for subsequent forwarding to the memory subsystem, or to an outbound request queue, for subsequent forwarding to one of the PCI buses. The CNB20HE also accepts inbound requests from the CIOB and the legacy PCI bus. The CNB20HE is also responsible for generating the appropriate controls to the MEC to control data transfer to and from the memory.
- **CIOB—Champion I/O Bridge.** The CIOB provides the interface for both the 64-bit / 66-MHz Revision 2.1-compliant PCI bus and the 64-bit / 33-MHz Revision 2.1-compliant PCI bus. The CIOB is both master and target on both PCI buses.

- **OSB4—Open South Bridge**. The OSB4 controller has several components. It provides the interface for a 32-bit / 33-MHz Revision 2.1-compliant PCI bus. The OSB4 can be both a master and a target on that PCI bus. The OSB4 also includes a USB controller and an IDE controller. The OSB4 is also responsible for much of the power management functions, with ACPI control registers built in. The OSB4 also provides a number of GPIO pins.
- **MADP—Memory Address and Data Path**. The SKA4 memory board has four MADP components. These devices are used to expand the SDRAM signaling environment to support up to 16 PC-100 Registered SDRAM DIMMs. These DIMMs can be up to 1 GB each.

2.3.1 ServerWorks ServerSet II HE Chipset Memory Architecture Overview

The CNB20HE provides the memory controller for the system. The main memory interface consists of two concurrent 100 MHz SDRAM channels. These channels run to a connector called the Memory Expansion Card Connector (MECC).

The 100 MHz SDRAM channels to the MECC connect to four MADP repeater devices on the memory expansion card to interface to PC-100 Registered ECC SDRAM DIMMs. Main memory sizes from 256 MB to 16 GB are supported with 72-bit, four-way interleaved PC-100 Registered SDRAM DIMMs. The ECC algorithm used during main memory accesses is capable of correcting single-bit errors and detecting all double-bit errors.

The interface between the CNB20HE and the 4 MADP devices on the MEC is a proprietary interface. This interface provides 1.6 GB/second bandwidth to/from main memory. For details on the Memory Expansion Card, see Section titled SKA4 SDRAM Memory Board.

2.3.2 ServerWorks ServerSet II HE Chipset System I/O Architecture Overview

The CNB20HE, CIOB, and OSB4 chips provide the pathway between processor and I/O systems. The CNB20HE is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to one of the PCI buses or legacy I/O locations. If the cycle is directed to one of the 64-bit PCI segments, the HE communicates with the CIOB through a private interface called the IMB. If the cycle is directed to the 32-bit PCI segment or to the OSB4, the cycle is output on the HE's 32-bit PCI bus. The CIOB translates the IMB bus operation to a 64-bit PCI Rev. 2.1-compliant signaling environment operating at either 66 MHz or 33 MHz.

The IMB bus consists of two data paths, one upstream (to the CNB20HE from the CIOB) and one downstream (from the CNB20HE to the CIOB). The interface is 16 bits wide and operates at 133 MHz with double pumped data, providing over 1 GB per second of bandwidth or 533 MB per second in each direction concurrently.

All I/O for the SKA4 boardset, including PCI- and PC-compatible, is directed through the CNB20HE and then through either the CIOB or the HE provided 32-bit/33-MHz PCI bus.

The HE provides a 32-bit/33-MHz PCI bus hereafter called P32-C.

- The CIOB provides a 64-bit/66-MHz PCI bus hereafter called P64-A, and the 64-bit/33-MHz PCI bus hereafter called P64-B.

This independent bus structure allows all three PCI buses to operate concurrently and provides 1.2 GB per second of I/O bandwidth.

2.3.3 CNB20HE

The Champion North Bridge Rev 2.0 High End (CNB20HE) is the third generation product in ServerWork's Champion North Bridge Technology. The CNB20HE uses the proven components of previous generations like the Pentium Pro Bus interface unit, the PCI interface unit, and the SDRAM memory interface unit. In addition to the above-mentioned units, the CNB20HE incorporates an Intra Module Bus (IMB) Interface. The 1 MB interface enables the CNB20HE to directly interface with the CIOB20. The CNB20HE also increases the main memory interface bandwidth and maximum memory configuration with a 144-bit wide memory interface.

The CNB20HE is a 644-pin ball-grid array (BGA) device. The CNB20HE integrates three main functions:

- An integrated high performance main memory subsystem
- An IMB bus interface that provides a high-performance data flow path between the Pentium Pro bus and the I/O subsystem
- A PCI interface that provides an interface to the compatibility PCI bus segment and the OSB4 (South Bridge).

Other features provided by the CNB20HE include the following:

- Full support of ECC on the processor bus.
- Full support of ECC on the memory interface.
- Eight deep in-order queue.
- Full support of registered PC-100 ECC SDRAM DIMMs.
- Support for 16 GB of 4-way interleaved SDRAM.
- Memory scrubbing.

2.3.3.1 P32-C I/O Subsystem

The CNB20HE also provides the legacy 32-bit PCI subsystem. The CNB20HE acts as the central resource on this PCI interface. P32-C supports the following embedded devices and connectors:

- Two 120-pin, 32-bit PCI expansion connectors numbered P32-C1 and P32-C2.
- OSB4 – Open South Bridge.
- PCI network interface controller—Intel 82559 Fast Ethernet Controller.
- 3D/2D Graphics Accelerator —ATI RAGE IIC Video Controller.
- PCI narrow/wide Ultra SCSI controller—Adaptec AIC-7880 SCSI Controller.

See Section 3, Baseboard PCI I/O Subsystem for details on this I/O segment.

2.3.4 CIOB

The Champion I/O Bridge (CIOB) provides an integrated I/O bridge that provides a high-performance data flow path between the IMB and the 64-bit I/O subsystem. This subsystem supports peer 64-bit PCI segments. Having multiple PCI interfaces, the CIOB is able to provide large and efficient I/O configurations. The CIOB functions as the bridge between IMB and the multiple 64-bit PCI I/O segments.

The IMB interface is capable of supporting 512 megabyte per second (MBps) of data bandwidth in both the upstream and downstream direction simultaneously. The internal PCI arbiter implements the Least Recently Used algorithm to grant access to requesting masters. The CIOB is a 352-pin ball-grid array device.

2.3.4.1 P64-A I/O Subsystem

P64-A supports the following embedded devices and connectors:

- Two 184-pin, 3.3 V keyed, 64-bit PCI expansion slot connectors, numbered P64-A1 and P64-A2, supporting both 66-MHz and 33-MHz 3.3 V-compliant PCI adapters.
- One DesotoE2 Hot-plug PCI controller.

All of the slots on segment P64-A support PCI Hot-plug and conform to the *PCI Hot-Plug Specification, Revision 1.0*. For specifics on this I/O bus, see Section 3.

2.3.4.2 P64-B I/O Subsystem

P64-B supports the following embedded devices and connectors:

- One Adaptec 7899 dual channel SCSI-3 Ultra 160/m SCSI controller.
- Four 184-pin, 5 V keyed, 64-bit PCI expansion slot connectors, numbered P64-B1, P64-B2, P64-B3, and P64-B4, supporting 33-MHz 5V PCI compliant PCI adapters.
- One DesotoE2 Hot-plug PCI controller.

All slots on segments P64-B support PCI Hot-plug and conform to the *PCI Hot-Plug Specification*, *Revision 1.0*. For specifics on this I/O bus, see Section 3.

2.3.5 OSB4

The OSB4 is a PCI device that provides multiple PCI functions in a single package: PCI-to-ISA bridge, PCI IDE interface, PCI USB controller, and power management controller. Each function within the OSB4 has its own set of configuration registers; once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

The OSB4 is a 352-pin ball-grid array BGA device. On the SKA4 baseboard, the primary role of the OSB4 is to provide the gateway to all PC-compatible I/O devices and features. The SKA4 baseboard uses the following OSB4 features:

- PCI interface.
- IDE interface, with Ultra DMA 33 capability.
- USB interface.

- PC-compatible timer/counters and DMA controllers.
- Baseboard Plug and Play support.
- General purpose I/O.
- Power management.
- APIC and 8259 interrupt controller.
- Host interface for AT compatible signaling.
- Internal only ISA bus (no ISA expansion connectors) bridge for communication with Super I/O, BIOS flash and BMC.

The following sections describe each supported feature as used on the SKA4 baseboard.

2.3.5.1 PCI Interface

The OSB4 fully implements a 32-bit PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Revision 2.1*. On the SKA4 baseboard, the PCI interface operates at 33 MHz, using the 5V-signaling environment.

2.3.5.2 PCI Bus Master IDE Interface

The OSB4 acts as a PCI-based Fast IDE controller that supports programmed I/O transfers (transfer rates up to 14 MBps) and bus master IDE transfers (transfer rates up to 33 MBps). While the OSB4 supports two IDE channels, supporting two drives each (drives 0 and 1), the SKA4 baseboard uses only the primary IDE channel. A single IDE connector, featuring 40 pins (2 x 20), is provided on the baseboard.

The SKA4 IDE interface supports “Ultra DMA/33” Synchronous DMA Mode Transfers.

2.3.5.3 USB Interface

The OSB4 contains a USB controller and USB hub. The USB controller moves data between main memory and the three USB connectors provided.

The SKA4 baseboard provides a dual external USB connector interface on the back. Both ports function identically and with the same bandwidth. The external connector is defined by the *USB Specification, Revision 1.0*.

2.3.5.4 Compatibility Interrupt Control

The OSB4 provides the functionality of two 82C59 PIC devices, for ISA-compatible interrupt handling.

2.3.5.5 APIC

The OSB4 integrates a 16-entry IO APIC that is used to distribute 16 PCI interrupts. It also includes an additional 16-entry IO APIC for distribution of legacy ISA interrupts.

2.3.5.6 Power Management

One of the embedded functions of OSB4 is a power management controller. The SKA4 baseboard uses this to implement ACPI-compliant power management features. The SKA4 supports sleep states S0, S1, S4, and S5.

2.3.6 MADP

The SKA4 Memory board utilizes four MADP components in the HE-Classic mode. In this configuration the MADP provides signal buffering to expand the two memory interface channels on the CNB20HE to four independent channels, expanding the maximum memory configuration to 16GB and 16 DIMM sites.

The MADP is a 256-pin ball-grid array BGA device.

2.4 Chipset Support Components

2.4.1 Legacy I/O (Super I/O) National* PC97317VUL

The National* PC97317VUL Super I/O Plug and Play Compatible with ACPI Compliant Controller / Extender is used on the SKA4 baseboard. This device provides

- The system real-time clock (RTC)
- Two serial ports
- One parallel port
- A floppy disk controller
- A PS/2-compatible keyboard and mouse controller
- General purpose I/O pins
- Plug and Play functions
- A power management controller.

The SKA4 baseboard provides the connector interface for the floppy, dual serial ports, parallel port, PS/2 mouse, and the PS/2 keyboard. Upon reset, the SIO reads the values on GPO pins to determine its boot-up address configuration.

2.4.1.1 Serial Ports

Two 9-pin connectors in D-Sub housing are provided for serial port A and serial port B. Both ports are compatible with 16550A and 16450 modes, and both are re-locatable. Each serial port can be set to one of four different COM-x ports, and each can be enabled separately. When enabled, each port can be programmed to generate edge- or level-sensitive interrupts. When disabled, serial port interrupts are available to add-in cards. The pinout is shown below:

Table 2-2: Serial Port Connector Pinout

Pin	Name	Description
1	DCD	Data Carrier Detected
2	RXD	Receive Data

Pin	Name	Description
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Request to Send
8	CTS	Clear to Send
9	RIA	Ring Indication Active

2.4.1.2 Parallel Port

The SKA4 baseboard provides a 25-pin parallel port connector. The SIO provides an IEEE 1284-compliant 25-pin bi-directional parallel port. BIOS programming of the SIO registers enables the parallel port and determines the port address and interrupt. When disabled, the interrupt is available to add-in cards. The pinout is shown below:

Table 2-3: Parallel Port Connector Pinout

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

2.4.1.3 Floppy Port

The FDC in the SIO is functionally compatible with floppy disk controllers CMOS 765B and 82077AA. The baseboard provides the 24-MHz clock, termination resistors, and chip selects. All other FDC functions are integrated into the SIO, including analog data separator and 16-byte FIFO. The pinout is shown below:

Table 2-4: Floppy Port Connector Pinout

Pin	Name	Pin	Name
1	GND	18	FD_DIR_L
2	FD_DENSEL	19	GND

Pin	Name	Pin	Name
3	GND	20	FD_STEP_L
4	n/c	21	GND
5	Key	22	FD_WDATA_L
6	FD_DRATE0	23	GND
7	GND	24	FD_WGATE_L
8	FD_INDEX_L	25	GND
9	GND	26	FD_TRK0_L
10	FD_MTR0_L	27	FD_MSEN0
11	GND	28	FD_WPROT_L
12	FD_DR1_L	29	GND
13	GND	30	FD_RDATA_L
14	FD_DR0_L	31	GND
15	GND	32	FD_HDSEL_L
16	FD_MTR1_L	33	GND
17	FD_MSEN1	34	FD_DSKCHG_L

2.4.1.4 Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single stacked housing. The mouse connector is stacked over the keyboard connector. External to the board they appear as two connectors. The keyboard controller is functionally compatible with the 8042A. The keyboard and mouse connectors are PS/2-compatible. The pinouts are shown below:

Table 2-5: Keyboard Connector Pinout

Pin	Signal	Description
1	KEYDAT	Keyboard Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	KEYCLK	Keyboard Clock
6	(NC)	

Table 2-6: Mouse Connector Pinout

Pin	Signal	Description
1	MSEDAT	Mouse Data
2	(NC)	
3	GND	Ground
4	FUSED_VCC	+5 V, fused
5	MSECLK	Mouse Clock
6	(NC)	

2.4.1.5 Real-time Clock

The PC97317VUL contains an MC146818-compatible real-time clock with external battery backup. The device also contains 242 bytes of general purpose battery-backed CMOS RAM.

2.4.1.6 Plug and Play Functions / ISA Data Transfers

The PC97317VUL contains all signals for ISA compatible interrupts and DMA channels. It also provides ISA control, data, and address signals to transfer data to/from the BMC and the BIOS flash device. This ISA subsystem transfers all SIO peripheral control data to the OSB4 south bridge as well.

2.4.1.7 Power Management Controller

The PC97317VUL contains functionality that allows various events to allow the power-on and power-off of the system. This can be from PCI Power Management Events or from the BMC or front panel. This circuitry is powered off stand-by voltage present anytime the system is plugged into the AC outlet.

2.4.2 BIOS Flash

The SKA4 baseboard incorporates an Intel® 5V FlashFile™ 28F008SA Flash Memory component. The 28F008SA component is high-performance 8 megabit memory organized as 1 MB of 8 bits each. There are sixteen 64 KB blocks.

The 8-bit flash memory provides 1024K x 8 of BIOS and non-volatile storage space. The flash device is directly addressed as 8-bit ISA memory.

3. Baseboard PCI I/O Subsystem

3.1 Overview

The primary I/O bus for the SKA4 baseboard is PCI, with three PCI bus segments. All of the PCI buses comply with the *PCI Local Bus Specification, Revision 2.1*. All of the 64-bit slots on the SKA4 support PCI Hot-plug and comply with the *PCI Hot-Plug Specification, Revision 1.0*. The table below lists the characteristics of the three PCI bus segments.

Table 3-1: PCI Bus Segment Characteristics

PCI Bus Segment	Width	Speed	Type	Add-in PCI Slot Support, Total Eight Slots
P64-A	64 bit	66/33 MHz	Peer bus	2 slots (64-bit 66/33-MHz) Full-length cards
P64-B	64 bit	33 MHz	Peer bus	4 slots (64-bit/33-MHz) Full-length cards
P32-C	32 bit	33 MHz	Peer bus	2 slots (32-bit/33-MHz) 1 slot 5.6” and 1 slot 6.3” in length

3.2 64-bit / 66-MHz PCI Subsystem

P64-A supports these embedded devices and connectors:

- Two 184-pin, 3.3 V, 64-bit PCI expansion connectors, numbered P64-A1 and P64-A2.
- One DesotoE2 Hot Plug PCI Controller.

3.2.1 Device IDs (IDSEL)

All slots on segment A support PCI Hot-plug and conform to the *PCI Hot-Plug Specification,* Revision 1.0. Each device under the PCI host bridge has its IDSEL signal connected to one bit of AD[31::16], which acts as a chip select on the PCI bus segment. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P64-A devices and the corresponding device number.

Table 3-2: P64-A Configuration IDs

IDSEL Value	Device
29	PCI Slot P64-A1
30	PCI Slot P64-A2
23	DesotoE2 PHPC

3.2.2 P64-A Arbitration

P64-A supports four PCI masters (slots P64-A1, P64-A2, DesotoE2 PHP Controller and the CIOB). All PCI masters must arbitrate for PCI access, using resources supplied by the CIOB. The host bridge PCI interface (CIOB) arbitration lines **REQx*** and **GNTx*** are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

Table 3-3: P64-A Arbitration Connections

Baseboard Signals	Device
PA_REQ0*/P_GNT0*	P64-A Slot P64-A1
PA_REQ1*/P_GNT1*	P64-A Slot P64-A2
PA_REQ2*/P_GNT2*	DesotoE2 PHPC

3.2.3 DesotoE2 Hot-Plug Controller

The DesotoE2 is a PCI device that is located on P64-A PCI bus. The DesotoE2 is the PCI Hot-plug Controller (PHPC) for the PHP slots.

The PHPC contains the PHPC Megacell that Compaq designed for compatibility with existing PHP drivers. The DesotoE2 contains the necessary memory index and access registers located in PCI configuration space to permit access to the PHPC functions. Such access is required to support ACPI PHP functionality.

3.2.4 P64-A Hot Plug Support

The two P64-A slots comply with the *PCI Hot-Plug Specification, Revision 1.0*. The slots support 3.3V, 64-bit and 32-bit, 66- or 33-MHz PCI adapters.

The bus operating speed is determined during the system's Power-on Self-Test (POST). If an installed PCI adapter does not support 66-MHz operation, the bus speed will be adjusted to run at 33 MHz. If no adapters are installed, the bus segment can be selected to operate at either 66 MHz or 33 MHz based on the BIOS SETUP option.

Note: To comply with the published PCI specification, the PCI bus segment must be reset when the bus speed is changed. This may be done only when the system is reset. Therefore, once the speed of the P64-A bus segment is set during POST, it may not be changed while the system is running.

If a 33 MHz PCI adapter is hot-plugged into the P64-A bus segment while the bus is running at 66 MHz, the PCI hot-plug controller and operating system driver will not allow the newly added PCI adapter online.

3.2.5 P64-A Slot Specifics

The PCI slots support the PME# and 3.3VAUX signals as described in the *PCI Bus Power Management Interface Specification*.

The 3.3VAUX signal is a limited current 3.3V supply maintained even when the system power is turned off.

> **Warning: The SKA4 baseboard only supports one slot consuming 375mA of Standby current on the 3.3V AUX power line, although it can be any of the eight PCI slots. All other slots can consume a maximum of 20mA each. The system will not operate correctly if this limit is exceeded.**

CAUTION: To minimize the possibility of hot-plug damage, PCI adapter cards should only be added or removed under one of the two following conditions:

- System is off and all of the AC line cord(s) are unplugged from the system.
- System is on and the PCI Hot-plug slot to be accessed is disabled.

3.3 64-bit/33-MHz PCI Subsystem

PCI segments A and B are peer buses. P64-B supports the following embedded devices and connectors:

- One Adaptec 7899 dual channel SCSI-3 Ultra 160/m SCSI controller.
- Four 184-pin, 5 V, 64-bit PCI expansion connectors, numbered P64-B1, B2, B3, and B4.
- One DesotoE2 Hot Plug PCI Controller.

3.3.1 Device IDs (IDSEL)

All slots on segment B support PCI Hot-plug and conform to the *PCI Hot-Plug Specification, Revision 1.0*. The PCI IDSEL signal connections to PCI AD[31::11] lines for P64-B devices are shown in the following table.

Table 3-4: P64-B Configuration IDs

IDSEL Value	Device
24	PCI Slot P64-B1
25	PCI Slot P64-B2
26	PCI Slot P64-B3
27	PCI Slot P64-B4
22	7899 SCSI Controller
21	DesotoE2* PHPC

3.3.2 P64-B Arbitration

P64-B supports six PCI masters: slots P64-B1 through P64-B4, wide SCSI controller and the DesotoE2 PHP Controller. All PCI masters must arbitrate for PCI access using resources supplied by the CIOB. The CIOB interface arbitration connections are internal to the device. The following table defines the external arbitration connections:

Table 3-5: P64-B Arbitration Connections

Baseboard Signals	Device
S_REQ0*/S_GNT0*	PCI Slot P64-B1
S_REQ1*/S_GNT1*	PCI Slot P64-B2
S_REQ2*/S_GNT2*	PCI Slot P64-B3
S_REQ3*/S_GNT3*	PCI Slot P64-B4
S_REQ4*/S_GNT4*	Wide SCSI Controller
S_REQ5*/S_GNT5*	DesotoE2* PHPC

3.3.3 DesotoE2 Hot-Plug Controller

The DesotoE2 is a PCI device that is located on P64-B PCI bus. The DesotoE2 is the PCI Hot-Plug Controller (PHPC) for the PHP slots.

The PHPC contains the PHPC Megacell, designed by Compaq, for compatibility with existing PHP drivers. The DesotoE2 contains the necessary memory index and access registers located in PCI configuration space to permit access to the PHPC functions. Such access is required to support ACPI PHP functionality.

3.3.4 P64-B Slot Specifics

The PCI slots support the PME# and 3.3VAUX signals as described in the *PCI Bus Power Management Interface Specification*.

The 3.3VAUX signal is a limited current 3.3 V supply maintained even when the system power is turned off.

Warning: The SKA4 baseboard supports only one slot that consumes 375mA of Standby current on the 3.3V AUX power line. This can be any of the eight PCI slots. All other slots can consume a maximum of 20mA each. The system will not operate correctly if these limits are exceeded.

CAUTION: To minimize the possibility of hot-plug damage, PCI adapter cards should only be added or removed under one of the two following conditions:

- System is off and all of the AC line cord(s) are unplugged from the system.
- System is on and the PCI Hot-plug slot to be accessed is disabled.

3.3.5 Ultra 160/m SCSI Controller (Adaptec* 7899)

The SKA4 provides an embedded dual-function Adaptec AIC-7899 PCI SCSI host adapter on the P64-B segment. The AIC-7899 controller contains two independent SCSI controllers that share a single PCI bus master interface as a multifunction device, packaged in a 352-pin ball grid array BGA package. Internally, each controller is identical, capable of operations using either 16-bit SE or LVD SCSI providing 40 MBps (Ultra-wide SE), 80 MBps (Ultra 2), or 160 MBps (Ultra 160/m).

In the SKA4 baseboard implementation, both controller A and controller B attach to a 68-pin, 16-bit differential SCSI connector LVD interface. Each controller has its own set of PCI configuration registers and SCSI I/O registers. As a PCI bus master, the AIC-7899 supports

burst data transfers on PCI up to the maximum rate of 266 MBps using on-chip buffers. Refer to the *AIC-7899 PCI-Dual Channel SCSI Multi-Function Controller Data Manual* for more information on the internal operation of this device and for descriptions of SCSI I/O registers.

3.4 32-bit/33-MHz PCI Subsystem

All 32-bit, 33 MHz PCI I/O for the SKA4 baseboard, including PCI- and PC-compatible, is directed through the CNB20HE. The 32-bit, 33 MHz PCI segment created by the CNB20HE is called the P32-C segment. The P32-C segment supports the following embedded devices and connectors:

- Two 120-pin, 32-bit PCI expansion connectors, numbered P32-C1 and P32-C2.
- OSB4 I/O APIC, PCI-to-ISA bridge, IDE controller, USB controller, and power management.
- PCI Video Controller.
- PCI Network Interface Controller.
- PCI Legacy Ultra SCSI controller.

3.4.1 Device IDs (IDSEL)

Each device under the PCI hub bridge has an IDSEL signal that is connected to one bit of AD[31::16]. This acts as a chip select on the PCI bus segment in configuration cycles and determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached for P32-C devices, and the corresponding device number. For more information see “Chapter Six: Configuration Space” in Revision 2.1 of the *PCI Local Bus Specification*.

Table 3-6: P32-C Configuration IDs

IDSEL Value	Device
18	PCI Slot P32-C1
19	PCI Slot P32-C2
17	PCI 7880 SCSI
20	PCI NIC 82559
28	ATI RAGE* IIC Video Controller
31	OSB4; ISA Bridge, IDE, USB, SM Bus

3.4.2 Specifics of the P32-C Slot

The PCI slots support the PME# and 3.3VAUX signals as described in the *PCI Bus Power Management Interface Specification*.

The 3.3VAUX signal is a limited current 3.3V supply that is maintained even when the system power is turned off.

Warning: The SKA4 baseboard supports only one slot that consumes 375mA of Standby current on the 3.3V AUX power line. This can be any of the eight PCI slots. All other slots can

consume a maximum of 20mA each. The system will not operate correctly if these limits are exceeded.

These slots both have length and height restrictions as follows.

Table 3-7: P32-C Slot Use Restrictions

Slot #	Maximum Length	Maximum Component Height	
P32-C1	5.3”	.570”	
P32-C2	6.3”	.400”	.300” component height restriction from 5.3” to 6.3” length and up 1” from the baseboard in the CNB20HE heat sink area.

3.4.3 Legacy SCSI (Adaptec* 7880)

The SKA4 baseboard provides an embedded AIC-7880 SCSI host adapter on the P32-C bus. The AIC-7880 contains a single SCSI controller with a full-featured PCI bus master interface in a 160-pin PQFP. The 7880 supports either 8-bit or 16-bit Fast-10 SCSI providing 10 MBps or 20 MBps throughput, or Fast-20 SCSI that can burst data at 20 MBps or 40 MBps. As a PCI 2.1 bus master that complies with Revision 2.1 of the *PCI Local Bus Specification*, the AIC-7880 supports burst data transfers on PCI up to the maximum rate of 133 MBps using the on-chip 256-byte FIFO.

The AIC-7880 implementation on the SKA4 baseboard offers 8-bit or 16-bit SCSI connectors and operation at data transfer rates of 10, 20, or 40 MBps. The AIC-7880 also offers active negation outputs, controls for external differential transceivers, a disk activity output, and a SCSI terminator power-down control. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus, avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48-mA single-ended SCSI bus with no additional drivers. The SCSI segment can support up to 15 devices.

Because the AIC-7880 can be used as an 8-bit controller (via the narrow, 50-pin connector) and as a 16-bit controller (via the wide, 68-pin connector), the AIC-7880 is not always at one end of the SCSI bus, and termination is controlled through simple circuitry. The circuitry senses when a device is attached through the narrow, 50-pin connector or through the wide, 68-pin connector.

When devices are attached to both connectors, the termination is on for the upper 8 bits of data and the parity bit associated with these data lines. All other signals are not terminated on board and are terminated by the devices attached through the connector. When a device is on only one connector (either wide or narrow), all on-board termination is on.

3.4.4 Network Interface Controller (NIC)

The SKA4 baseboard supports a 10Base-T/100Base-TX network subsystem based on the Intel 82559 Fast Ethernet Multifunction PCI/CardBus Controller. This device is similar in architecture to its predecessor (the Intel® 82558 controller). The 82559 is a highly integrated PCI LAN controller in a 196-pin BGA supporting 10 or 100 megabits per second (Mbps) Fast Ethernet networks. As a PCI bus master, the 82559 can burst data at up to 132 MBps.

3.4.4.1 Supported Network Features

The 82559 includes an IEEE MII-compliant interface to the components necessary to implement an IEEE 802.3 100Base-TX network connection. The SKA4 baseboard supports the following features of the 82559 controller:

- Glueless 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with Revision 2.1 of the *PCI Local Bus Specification*.
- 82596-like chained memory structure, with improved dynamic transmit chaining for enhanced performance.
- Programmable transmit threshold for improved bus utilization.
- Early receive interrupt for concurrent processing of receive data.
- On-chip counters for network management.
- Autodetect and autoswitching for 10- or 100-Mbps network speeds.
- Support for both 10-Mbps and 100-Mbps networks, full or half duplex-capable, with back-to-back transmit at 100 Mbps.
- Integrated physical interface to TX magnetics.
- The magnetics component terminates the 100Base-TX connector interface. A flash device stores the network ID.

3.4.4.2 NIC Connector and Status LEDs

The 82559 drives LEDs on the network interface connector that indicate transmit/receive activity on the LAN, a valid link to the LAN, and 10- or 100-Mbps operation. The green LED (left) indicates network connection when on and TX/RX activity when blinking. The yellow LED indicates 100-Mbps operation when lit.

3.4.5 Video Controller

The SKA4 provides an ATI RAGE IIC VGA Graphics Accelerator, along with video SGRAM and support circuitry for an embedded SVGA video subsystem. The ATI RAGE IIC chip contains an SVGA video controller, clock generator, BitBLT engine, and RAMDAC in a 208-pin PQFP. One 256K x 32 SGRAM chip provides 2 MB of 10-ns video memory. The SVGA subsystem supports a variety of modes, up to 1600 x 1200 resolution, or up to 16.7 million colors. It also supports analog VGA monitors, single- and multi-frequency, interlaced and non-interlaced, up to 100 Hz vertical retrace frequency. The SKA4 provides a standard 15-pin VGA connector and video blanking logic for server management console redirection support.

3.4.5.1 Video Modes

The RAGE IIC chip supports all standard IBM VGA modes. The following tables show the modes that this implementation supports, including the number of colors, resolution, and refresh rates.

Table 3-8: Standard VGA Modes

Resolution	Max. Refresh Rate (Hz)	Colors
640x480	200	256
800x600	200	256
1024x768	150	256
1152x864	120	256
1280x1024	100	256
1600x1200	76	256
640x480	200	65K
800x600	200	65K
1024x768	150	65K
1152x864	120	65K
640x480	200	16.7M
800x600	160	16.7M

3.4.5.2 VGA Connector

The following table shows the pinout of the VGA connector. For more information, see the *ATI RAGE IIC Technical Reference Manual*.

Table 3-9: Video Port Connector Pinout

Pin	Signal	Description
1	RED	Analog color signal R
2	GREEN	Analog color signal G
3	BLUE	Analog color signal B
4	nc	No connect
5	GROUND	Video ground (shield)
6	GROUND	Video ground (shield)
7	GROUND	Video ground (shield)
8	GROUND	Video ground (shield)
9	nc	No connect[1]
10	GROUND	Video ground
11	nc	No connect
12	DDCDAT	Monitor ID data
13	HSYNC	Horizontal Sync
14	VSYNC	Vertical Sync
15	DDCCLK	Monitor ID clock

Note:
1. This no-connect pin is used to reduce EMI.

3.5 Interrupt Routing

The SKA4 interrupt architecture accommodates both PC-compatible PIC mode and APIC mode interrupts through use of the integrated I/O APICs in the OSB4.

3.5.1 Legacy Interrupt Routing, OSB4 Compatibility Interrupt Controller

For PC-compatible mode, the OSB4 provides two 82C59-compatible interrupt controllers embedded in the device. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The OSB4 contains configuration registers that define which interrupt source logically maps to I/O APIC INTx pins.

PCI and IRQ interrupts are both are handled by the OSB4. The OSB4 translates these to the APIC bus. The number in the table below indicates the OSB4 PCI interrupt input pin to which the associated device interrupt (INTA, INTB, INTC, INTD) is connected. The I/O APIC for the OSB4 exists on the I/O APIC bus with the processors.

Table 3-10: PCI Interrupt Routing/Sharing

Interrupt	INT A	INT B	INT C	INT D
P64A-Slot1	1	0	0	0
P64A-Slot2	3	2	2	2
DesotoE2-66*	14			
P64B-Slot1	5	4	4	4
P64B-Slot2	7	6	6	6
P64B-Slot3	9	8	8	8
P64B-Slot4	11	10	10	10
DesotoE2-33	14			
7899 Channel 1	8			
7899 Channel 2	8			
P32C-Slot1	12	12	12	12
P32C-Slot2	13	13	13	13
82559 NIC	15			
7880-SCSI	15			

3.5.2 APIC Interrupt Routing

For APIC mode, the SKA4 interrupt architecture incorporates two Intel® I/O APIC devices to manage and broadcast interrupts to local APICs in each processor. The I/O APICs monitor each interrupt on each PCI device including PCI slots in addition to the ISA compatibility interrupts IRQ(0-15). When an interrupt occurs, a message that corresponds to the interrupt is sent across a three-wire serial interface to the local APICs. The APIC bus minimizes interrupt latency time for compatibility interrupt sources. The I/O APICs can also supply greater than 16 interrupt levels to the processor(s). This APIC bus consists of an APIC clock and two bi-directional data lines.

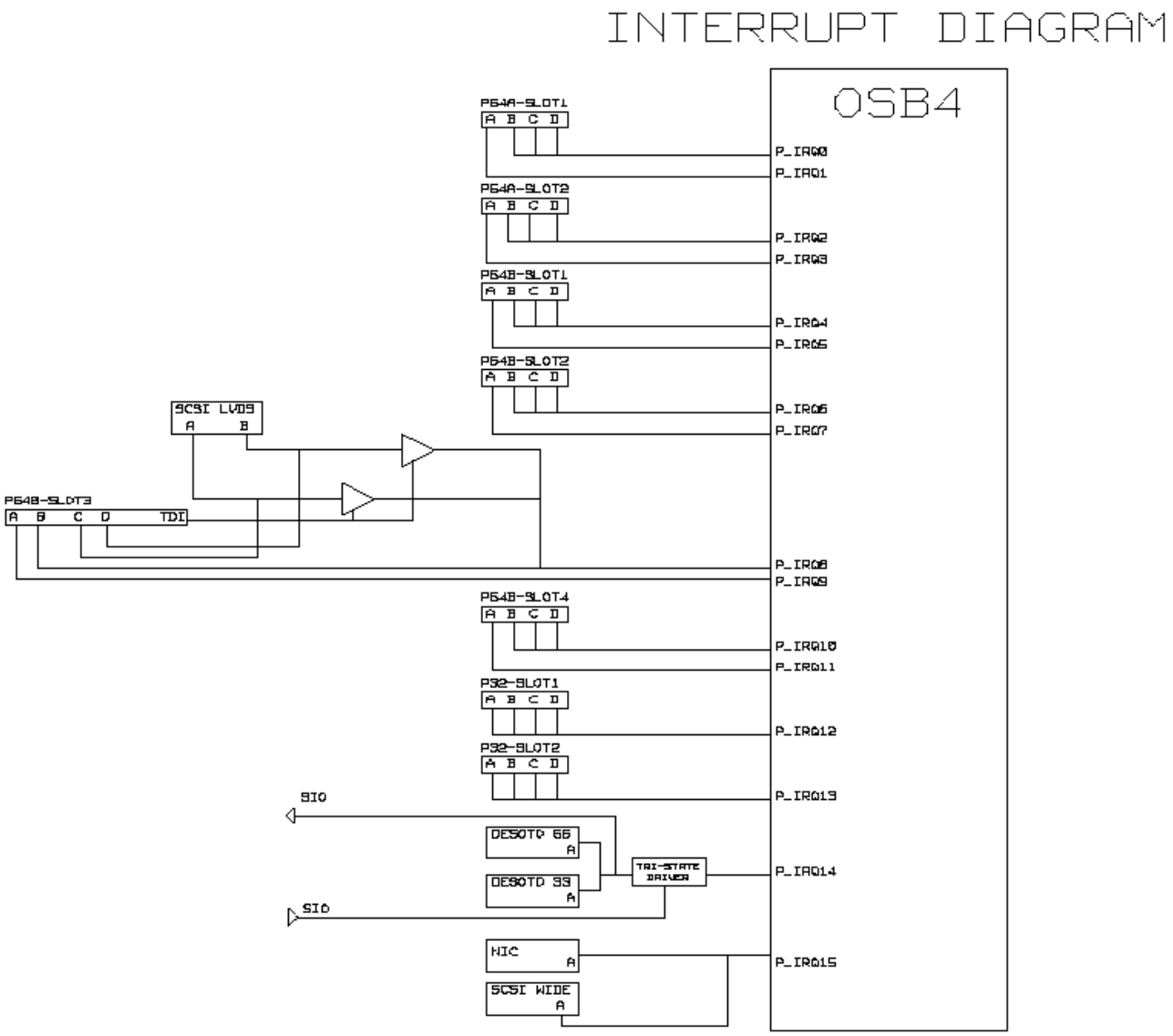

Figure 3-1: SKA4 Baseboard Interrupt Diagram

3.5.2.1 Legacy Interrupt Sources

The table below provides recommended logical interrupt mapping of interrupt sources on the SKA4 baseboard. The actual interrupt map is defined using configuration registers in the OSB4.

Table 3-11: Interrupt Definitions

ISA Interrupt	Description
INTR	Processor interrupt.
NMI	NMI to processor.
IRQ1	Keyboard interrupt.
IRQ3	Serial port A or B interrupt from SIO device, user-configurable.

ISA Interrupt	Description
IRQ4	Serial port A or B interrupt from SIO device, user-configurable.
IRQ5	Parallel port.
IRQ6	Floppy disk.
IRQ7	Parallel port.
IRQ8_L	Active low RTC interrupt.
IRQ9	
IRQ10	
IRQ11	
IRQ12	Mouse interrupt.
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1.
IRQ15	**Not supported for PCI devices**
SMI*	System Management Interrupt. General purpose indicator sourced by the PIIX4 and BMC to the processors.
SCI*	

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4. PCI Hot-plug

PCI Hot-plug (PHP) allows the user to add, remove, and replace PCI adapters installed in the PHP slots without interrupting normal operation or powering down the system. PHP technology improves Reliability, Availability, and Serviceability (RAS) for the system. The operating system must have the appropriate PHP driver and operating system installed to support PHP operation.

Hot plug support is provided on all six of the PCI slots on the 64-bit PCI bus segments (A and B). No hot plug support is provided on the 32-bit bus segment (C). Segment A can operate at either 66 MHz or 33 MHz; segment B operates only at 33 MHz. The logic for powering on and powering off the slots is controlled by the DesotoE2 ASIC. Only the CBL (Connect Bus Last) power sequence is supported.

4.1 PHP Functionality

In order to support PCI Hot-plug, systems require hot-plug hardware, a hot-plug compatible operating system, and hot-plug capable adapter drivers. To ensure backward compatibility, any combination of hot-plug and conventional versions of each of these components is permitted, including mixing both hot-plug and conventional adapter drivers. If a conventional driver is loaded under a hot-plug capable operating system, or if a hot plug driver is loaded under a conventional operating system, the driver will continue to have the same capability as it had in the conventional environment.

4.1.1 Power-Up

At first power-up, the BIOS is responsible for initializing the PHP controller. The initial slot power-up sequence occurs after this device initialization. The following power-up sequence is typical:

Power is applied to the slots one segment at a time, segment A followed by B. This can be observed on the HPIB: The two green LEDs for Segment A light up and turn off, then the four LEDs for Segment B light up and turn off. During initialization, the BIOS determines the presence and speed of the cards in the slots. Power remains on to slots containing a valid PCI card, and is turned off for empty slots.

4.1.2 Operating System

The initial steps involved in booting to an OS do not change because of PHP support. However, after the OS has booted, drivers are usually required to get PHP functionality. Three terms that are commonly used to describe PCI Hot-plug operations are Hot Replace, Hot Add, and Hot Upgrade.

- **Hot Replace** – The process or removing an adapter card and then inserting an identical adapter into the same slot. The replacement adapter card will use the same PCI resources that were assigned to the previous card and its driver will not be updated. Hot Replace is also commonly referred to as “Like-for-Like Replacement.”
- **Hot Add –** The process of inserting an adapter card into a previously unoccupied slot. This operation requires that a driver also be loaded for the added adapter. This operation requires that PCI resources have been reserved by the system BIOS for the added adapter card. Hot Add is also sometimes referred to as “Hot Expansion.”

- **Hot Upgrade –** The process of removing an adapter card and inserting an upgraded adapter (i.e., new revision) that requires different PCI resources than the original card. The adapter's driver may or may not use the same driver as the previous adapter.

"Hot Removal" and "Hot Insertion" refer to the sequence of steps involved in removing and inserting, respectively, a PCI card from a hot-pluggable PCI slot.

Not all of these operations are supported by every hot-plug capable operating system. Each operating system may implement these operations in a different manner. For example, the Windows NT 4.0 operating system supports only the Hot Replace operation. The following steps outline a typical enabling sequence:

1. After booting, load the needed drivers.

2. From the Windows NT menu bar, run the PHP graphical user interface (GUI) by clicking Start / Programs / PCI Hot Plug / PCI HP Utility.

   This GUI provides the adapter status to the hot-plug user interface and allows the user to control hot-plug functionality. The initial screen lists

   - LED Condition: green or amber
   - Location: logical slot number
   - Board: description, driver support
   - Status: normal or not ready

   Logical slot numbering starts at 3 and ends at 8, in increments of 1. Only slots containing a card with hot-plug capable drivers can be controlled from the GUI. Pressing the hardware or software power button for these slots powers them on and off. In response, the green LED lights up or turns off. Pressing the power button for an empty slot toggles its power condition (no drivers required).

4.1.3 Bus Speed Control

Segment A can be operated at 33 MHz or 66 MHz. In a PHP Hot Add (or Hot Upgrade) operation, it is possible that a user will attempt to add a card with a speed different than the existing bus speed. Logic on the baseboard ensures proper operation in compliance with the *PCI Local Bus Specification*. The possible bus speed scenarios are summarized in the following table:

Table 4-1: Bus Speed Control

	Original Speed (MHz)	Hot-added Card	Final Speed (MHz)	Notes
Empty Bus	33 or 66	N/A	No change	Setup selectable
Loaded Bus	33	33 or 66	33	
Loaded Bus	66	33	33	Error message
Loaded Bus	66	66	66	

Segment B is fixed at 33 MHz, regardless of the type of hot-added cards.

4.1.4 LED Control

Each slot has two LEDs. A green LED indicates the state of power on each slot. The amber LED is the slot attention indicator. The amber LED indicates an error condition with that slot. The following table summarizes typical LED states that may be encountered during operation:

Table 4-2: Slot State and Attention Indicators

LED States	Interpretation
Green On Amber Off	The slot is on and functioning normally
Green On Amber On	The slot is on and the card requires attention
Green Off Amber On	The slot is off and the card in it requires attention
Green Off Amber Off	The slot is off
Green blinking Amber off	Slot power transitioning (ON->OFF or OFF->ON)

4.1.5 Hardware Push Button

The Hardware push button is located on the hot-plug indicator board. It duplicates the functionality of the GUI-based Software button. A single push button is provided for each slot. Pressing the button normally initiates a power-on or power-off cycle (green LED blinking). A populated slot, under Windows NT 4.0, must have drivers before the push button will function properly. An empty slot can toggle power, without drivers under Windows NT 4.0, or in DOS.

4.1.6 Power Fault

A power fault condition is generated when an over current or under voltage condition is detected. Power to the slot is automatically removed in this case.

4.1.7 Interlock Switch Support

The SKA4 does not support a mechanical interlock switch. The switch input is permanently grounded (enabled) on the baseboard.

4.2 DesotoE2

The DesotoE2 is a 32-bit, 33 or 66 MHz PCI bus agent that manages PCI Hot-plug functionality on the PCI segment on which it resides. One DesotoE2 is on each 64-bit PCI segment (Segment A and Segment B). The DesotoE2 PHPC is ACPI compliant and compatible with Compaq's PHPC design to permit reuse of existing drivers. The DeSotoE2 supports either 3.3V or 5V PCI bus implementations. It is responsible for the following functions:

- Manage power application/removal to individual PCI slots.
- Properly reset newly added PCI cards prior to bringing the card online.

- Manage connection/disconnection of the PCI signals between the PCI bus and add-in card.
- Manage seamless addition/removal of individual PCI add-in cards without impacting bus functionality by generating dummy PCI cycles during transitions.

4.2.1 Configuration Registers

The DesotoE2 contains 256 PCI configuration space registers for access to the standard PCI configuration space. These registers are accessible according to the mapping of the IDSEL pin: device 7 (on segment A) and device 5 (on segment B).

The PHPC reserves a block of 256 memory mapped “I/O” registers specific to hot plug. The “Enable PCI Config Space Access to Hot Plug Registers” bit in the Misc Configuration Register (offset 40, bit 23) must first be set to “1”. This allows the index/access registers to become active.

The index and access registers are located in standard PCI configuration space at offset 50H and 54H, respectively. These registers can be used to access useful PCI hot plug functions, such as the Slot Enable Register (offset 00) and LED Control Register (offset 04). It is necessary to issue a SOGO (offset 00, set bit 16 to 1) before (modified) outputs are externally driven by the PHPC.

See the *Compaq PCI Hot-Plug Megacell Specification* for complete register descriptions and programming specifics.

4.2.2 Debug Tips

Possible problems / solutions are as follows:

- **Problem:** During boot-up, a populated slot powers up, then immediately powers off.

  Solution1: Verify that a valid PCI card is being used. A valid PCI card is one that supports PCI configuration space. Some test cards, such as LAI adapters, will need a valid PCI card installed in their onboard connector before they can be recognized and powered on.

  Solution2: A power fault condition can also produce this behavior. Correct the power fault condition.

- **Problem:** The PHP push button functions under DOS, but will not function under an OS.

  Solution: The PHP drivers specific to the OS are not loaded. Load the drivers.

5. SKA4 SDRAM Memory Board

The SKA4 memory board plugs into the Memory Expansion Card Connector on the SKA4 baseboard. It contains four MADPs (Memory Address Data Path), three clock buffers to provide 100-MHz clocks to the MADPs, and 16 DIMM sockets. The memory board includes four banks of memory and each bank includes four DIMMs. The banks are A, B, C and D. Bank A has A1, A2, A3 and A4 DIMMs, and so on. At least one bank of memory must be populated for the system to work.

The SKA4 memory board supports up to 16 GB of system memory using 1 GB PC-100 Registered DIMMs.

Below is a drawing of a populated SKA4 Memory board.

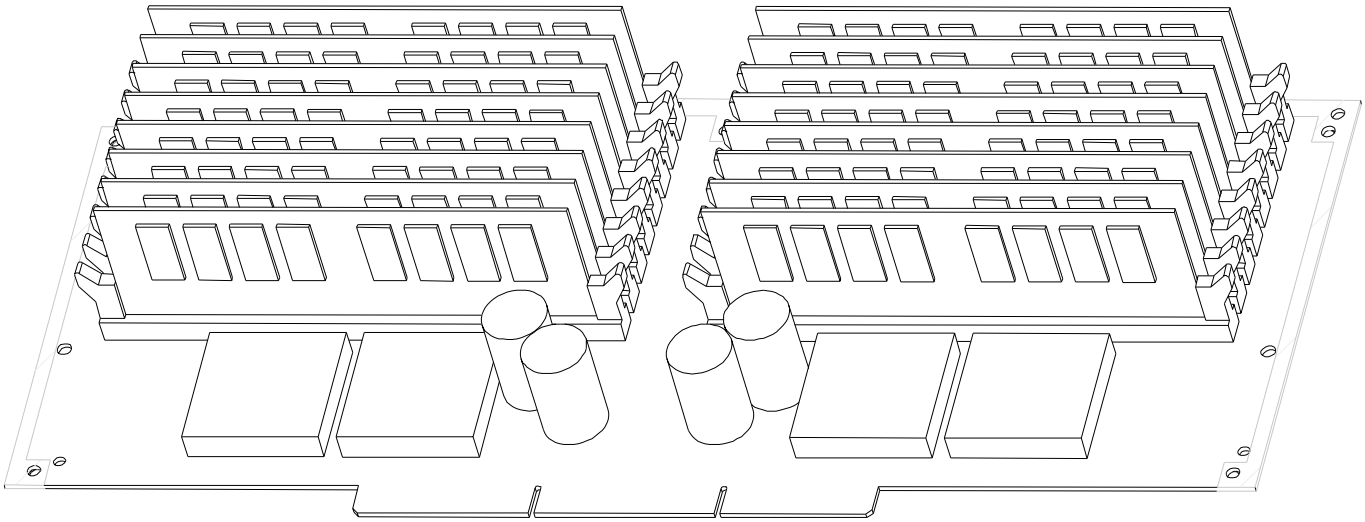

Figure 5-1: SKA4 Memory Board

5.1 Supported Memory

The SKA4 board set supports only DIMMs that are compliant with the PC-100 Registered DIMM specification version 1.2. The SKA4 board set is qualified only with ECC Registered DIMMs.

The minimum supported DIMM size is 64MB. Therefore, the minimum main memory configuration is 4 x 64 MB or 256 MB. The largest size DIMM supported is a 1 GB stacked registered PC-100 ECC DIMM based on 256 Megabit technology.

Note: The board set will support both stacked and un-stacked PC-100 compliant registered DIMMs, although thermal or power limitations of certain chassis may limit the configured system support. The OEM needs to conduct thermal testing to ensure the chassis provides adequate cooling to support the target memory configurations.

Note: Power dissipation of some un-stacked DIMMs exceeds that of some stacked DIMMs. The OEM needs to conduct thermal evaluations of all possible memory DIMMs to be populated.

5.2 SKA4 SDRAM Memory Board Components

5.2.1 MECC 330-pin Edge Connector

The memory board plugs into the MECC on the baseboard by the 330-pin edge connector. The 100 MHz interface between the CNB20HE and the four MADPs goes through this connector. The interface includes:

- Control signals (RAS, CAS, CS and Address)
- 144 bit of data and ECC
- A 100-MHz clock to the clock buffer
- A 100-MHz Read Clock that returns to the CNB20HE

Three separate IIC buses also go from the baseboard to the memory board.

Sufficient ground and power pins on the connector and bulk and high frequency decoupling capacitors on the memory board supply adequate voltages and currents to perform proper memory operations.

Note: A Slot 2 connector on the baseboard is used for the MECC. To protect the system from damage, logic on the baseboard prevents the system from powering up if a Slot 2 processor or a Slot 2 processor termination card is mistakenly plugged into the MECC.

5.2.2 MADP

The MADPs receive control signals from the CNB20HE and buffer them to the DIMMs. Therefore all of the control and address lines are common to all the DIMMs except for the CS signals where MADPs decode them. The CS lines are to select one bank (four DIMMs) out of the four banks of memory, as only one bank of memory is accessed at any given time. All the control lines including the CS lines are series terminated to protect the DIMM registers from excessive over/undershoot.

The MADPs transfer 4x72 bit of data and ECCs at one clock to/from four DIMMs (of a bank) and transfer 2x72 bit of data and ECCs to/from CNB20HE.

MADP has high and low strength settings, which are configured by the CNB20HE. If only the minimum required memory is installed (only one bank of non-stacked DIMM on the memory board), the strength is set to low for both the control and address lines and for the data lines. If more than one bank is populated, the CNB20HE sets the MADPs to high strength.

MADP has internal PLL to synchronize the MADPs-CNB20HE bus and MADPs-DIMMs bus.

The memory data is protected by ECC. The CNB20HE detects and corrects SBCEs (single-bit correctable errors). The CNB20HE also logs the syndrome bits and the bank where the error occurred. Based on that information, the BIOS can correctly identify the DIMM that has a bit error.

For MBEs (multiple-bit errors), the BIOS can point to two out of the four DIMMs in a bank (one of the two DIMMs caused errors).

5.2.3 DIMM Sockets

Data transfers between MADPs and DIMMs in a four-way interleaved fashion. Therefore, four DIMMs in a bank must be populated. At least one bank has to be fully populated in order for the system to boot. If additional banks have less than four DIMMs, the memory for that bank(s) will not be available to the system.

There are four banks of DIMMs on the memory board; they are A, B, C and D. Bank A contains DIMM A1, A2, A3 and A4, bank B contains DIMM B1, B2, B3 and B4, and so on. These identifications are marked with silk screen on the board next to each DIMM to label its bank number. DIMMs should be installed from bank A through D in alphabetical order to best optimized the memory subsystem for signal integrity/temperature cooling.

5.2.4 IIC Buses

Three IIC buses run from the baseboard to the memory board. Two of these connect 16 DIMM sites (one bus connects eight DIMMs each). The third bus connects to the FRU (field replaceable unit) EEPROM.

The DIMM's IIC buses are for the BIOS to retrieve information from each DIMM such as type, size, etc. to program the CNB20HE memory registers accordingly to boot the system. The FRU EEPROM contains useful information for field services.

The table below shows the IIC addresses for all of the devices. The SKA4 baseboard implements a multiplexer that allows the two DIMM I2C buses to share the SMB bus from the OSB4. The two different memory board I^2C buses are selected via GPIOs from the National 87317. The I^2C bus the FRU device resides on shares the baseboard's BMC primary private I^2C bus.

Table 5-1: I2C Addresses for Memory board SMB

Device	Address	GPIO 11	GPIO 12	Selected Bus #
DIMM A3	0xA0h	1	0	1
DIMM C3	0xA1h	1	0	1
DIMM B3	0xA2h	1	0	1
DIMM D3	0xA3h	1	0	1
DIMM A1	0xA4h	1	0	1
DIMM C1	0xA5h	1	0	1
DIMM B1	0xA6h	1	0	1
DIMM D1	0xA7h	1	0	1
DIMM A4	0xA0h	0	1	2
DIMM C4	0xA1h	0	1	2
DIMM B4	0xA2h	0	1	2
DIMM D4	0xA3h	0	1	2
DIMM A2	0xA4h	0	1	2
DIMM C2	0xA5h	0	1	2
DIMM B2	0xA6h	0	1	2
DIMM D2	0xA7h	0	1	2
FRU EEPROM	0xACh	N/A	N/A	3

5.2.5 Clocks

Three clock buffers on the memory board generate zero delay, low skew, and low jitter for the MADPs and DIMMs. The ICS2509 is a zero-delay buffer that takes the 100 MHz input clock from the baseboard and generates four 100-MHz clocks to the MADPs. One Read Clock returns to the CNB20HE.

The MADPs in turn generate 100-MHz clocks to drive the two ICS2510 low skew buffers. These two buffers drive 100-MHz clocks to the DIMMs and Read Clock back to the MADPs. Note that only two MADP output clocks are used to drive the two buffers. MADP has its own PLL and the design uses this PLL for zero-delay (instead of the PLL inside the ICS2510) between the MADP's outputs to the 100-MHz clocks to the DIMMs and the MADP's Read Clocks. Refer to Section 6, Clock Generation and Distribution, for details.

5.3 SKA4 Memory Board Functional Block Diagram

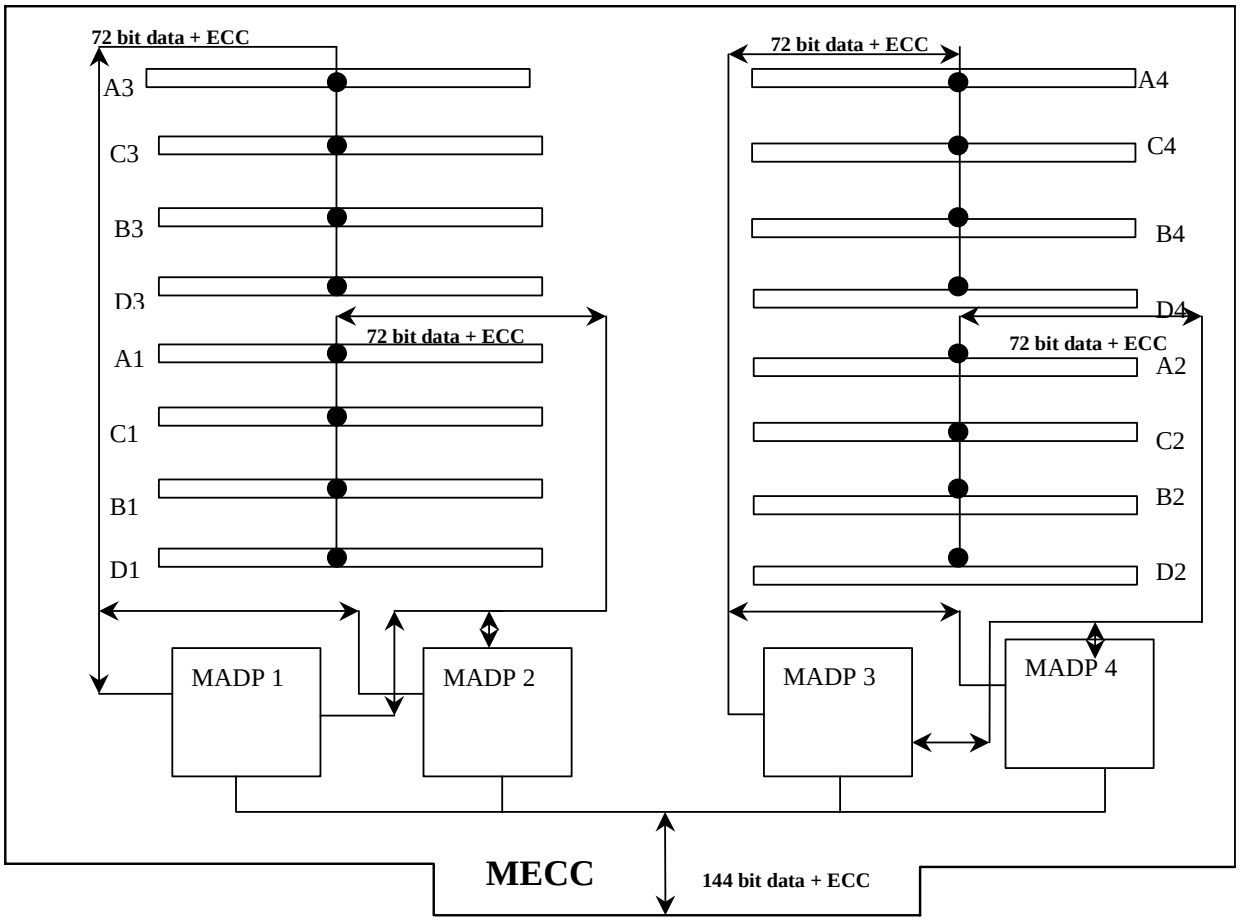

Figure 5-2: SKA4 Memory Board Functional Block Diagram

6. Clock Generation and Distribution

All buses on the SKA4 baseboard operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 100 MHz at 2.5V logic levels — For Slot 2 connectors, the CNB20HE, and the ITP port.
- 66 MHz at 3.3V logic levels — For CNB20HE, CIOB and the CIOB PCI clock.
- 33.3 MHz at 3.3V logic levels — Reference clock for the PCI bus clock driver.
- 16.67 MHz at 2.5V logic levels — Processor and the OSB4 APIC bus clocks.
- 14.318 MHz at 3.3V logic levels — OSB4, Super I/O, and video clocks.

The synchronous clock sources on the SKA4 baseboard are:

- 100-MHz host clock generator for processors, the CNB20HE, and the ITP.
- 66-MHz clock for CNB20HE and the CIOB PCI clocks.
- 48-MHz clock for OSB4 USB.
- 33.3-MHz PCI reference clock.
- 16.67-MHz APIC.
- 14.318-MHz OSB4, Super I/O, and video clocks.

For information on processor clock generation, see the *CK133-WS Synthesizer/Driver Specification*.

The SKA4 baseboard also provides asynchronous clock generators:

- 40-MHz clock for the embedded SCSI controllers.
- 32-KHz clock for the OSB4 RTC.
- 22.1-MHz clock for the BMC.

The following figure illustrates clock generation and distribution on the SKA4 baseboard.

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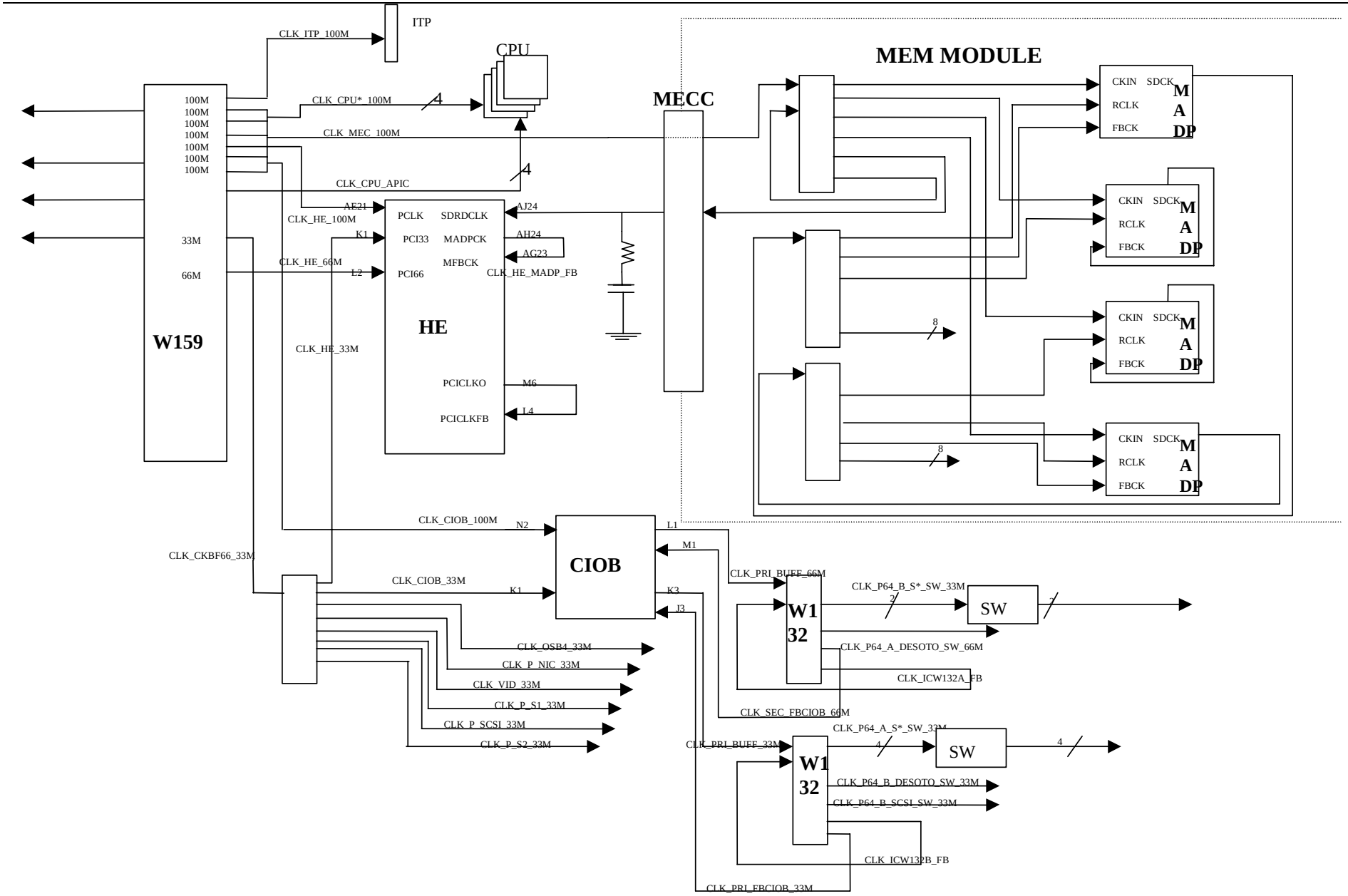

Figure 6-1: SKA4 Baseboard Clock Distribution

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7. SKA4 ACPI Implementation

7.1 ACPI

An ACPI-aware operating system (OS) generates an SMI to request that the system be switched into ACPI mode. The BIOS responds by sending the appropriate command to the BMC to enable ACPI mode. The system automatically returns to legacy mode upon hard reset or power-on reset.

The SKA4 platform supports S0, S1, S4, and S5 states. When the system is operating in ACPI mode, the OS retains control of the system and OS policy determines the entry methods and wakeup sources for each sleep state. Sleep entry and wakeup event capabilities are provided by the hardware but are enabled by the OS.

7.1.1 Front Panel Switches

SKA4 supports up to four front panel buttons (via the front panel connector): the power button, the sleep button, the reset button, and the NMI button

The power button input (FP_PWR_BTN*) in the SKA4 design is a request that is forwarded by the BMC to the power state machines in the National PC97317 Super I/O. It is monitored by the BMC and does not directly control power on the power supply.

The power button input and the sleep button input (FP_SLP_BTN*) behave differently depending on whether the operating system supports ACPI. The sleep switch has no effect unless an operating system with ACPI support is running. If the operating system supports ACPI and the system is running, pressing the sleep switch causes an event. The OS causes the system to transition to the appropriate system state depending on the user settings.

Power Switch Off to On: The OSB4 and SIO may be configured to generate wakeup events for several different system events: Wake on LAN*, PCI Power Management Interrupt, and Real Time Clock Alarm are examples of these events. The BMC monitors the power button and wakeup event signals from the OSB4 and SIO. A transition from either source results in the BMC starting the power-up sequence. Since the processors are not executing, the BIOS does not participate in this sequence. The OSB4 and SIO receive power good and reset from the BMC and then transition to an ON state.

On to Off (Legacy): The SIO is configured to generate an SMI due to a power button event. The BIOS services this SMI and sets the state of the machine in the OSB4 and SIO to the OFF state. The BMC monitors power state signals from the SIO and deasserts PS_PWR_ON to the power supply. As a safety mechanism, the BMC automatically powers off the system in 4-5 seconds, if the BIOS fails to service the SMI.

On to Off (ACPI): If an ACPI operating system is loaded, the power button switch generates a request (via SCI) to the OS to shutdown the system. The OS retains control of the system and OS policy determines what sleep state (if any) the system transitions into.

On to Sleep (ACPI): If an ACPI operating system is loaded, the sleep button switch generates a request (via SCI) to the OS to place the system in “sleep” mode. The OS retains control of the system and OS policy determines what sleep state (if any) the system transitions into.

Sleep to On (ACPI): If an ACPI operating system is loaded, the sleep button switch generates a wake event to the OSB4 and a request (via SCI) to the OS to place the system in the “On” state. The OS retains control of the system and OS policy determines what sleep state (if any) the system can wake from.

7.1.2 Wake Up Sources (ACPI and Legacy)

The SKA4 hardware is capable of wake up from several sources under a non-ACPI configuration, e.g., when the operating system does not support ACPI. The wake up sources are defined in the table below. Under ACPI, the operating system programs the OSB4 and the SIO to wake up on the desired event, but in legacy mode the BIOS enables/disables wake up sources based on a switch in Setup.

The operating system or a driver must clear any pending wake up status bits in the associated hardware (such as the Wake-on-LAN status bit in the LAN application specific integrated circuit (ASIC), or PCI power management event (PME) status bit in a PCI device). The legacy wake up feature is disabled by default.

Table 7-1: Supported Wake Events

Wake Event	Supported via ACPI (by sleep state)	Supported Via Legacy Wake
Power Button	Always wakes system	Always wakes system
Sleep Button	S1	No
Ring indicate from COMA	S1, S4, S5	Yes
Ring indicate from COMB	S1, S4, S5	Yes
PME from PCI 32/33	S1, S4, S5	Yes
PME from PCI 64/33	S1, S4, S5	Yes
PME from PCI 64/66	S1, S4, S5	Yes
BMC source (i.e. EMP)	Simulated as power button	Simulated as power button
RTC Alarm	S1, S4, S5	Yes
Mouse	S1	No
Keyboard	S1	No
USB	No	No

8. SKA4 System Bus Error Monitoring

This section documents the types of system bus error conditions monitored by the SKA4 board set and how they propagate to SMI#.

8.1.1 Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors on the SKA4, which can be disabled and enabled individually or as a group, can be categorized as follows:

- PCI bus.
- Processor bus errors.
- Memory single- and multi-bit errors.
- General Server Management sensors.

On the SKA4 platform, general server management sensors are managed by the BMC. See Section 9, Server Management, for specifics on these sensors.

8.1.2 PCI Bus Errors

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled by BIOS.

8.1.3 Pentium® III Xeon™ Processor Bus Errors

The CNB20HE supports all the data integrity features supported by the Pentium Pro bus including Address, Request and Response parity. The CNB20HE always generates ECC data while it is driving the processor data bus although data bus ECC can be disabled or enabled by BIOS (enabled by default). The CNB20HE generates MIRQ# on SBEs (Single Bit Errors) and generates SALERT# on uncorrectable errors. In addition, the CNB20HE can generate BERR# on unrecoverable ECC errors detected on the processor bus. Unrecoverable errors are routed to NMI by BIOS.

In the case of irrecoverable errors on the host processor bus, proper execution of the SMI handler cannot be guaranteed and the SMI handler cannot be relied upon to log such conditions. The BIOS SMI handler will record the error to the system event log (SEL) only if the system has not experienced a catastrophic failure that compromises the integrity of the SMI handler. The BIOS always enables the error correction and detection capabilities of the processors by setting appropriate bits in processor model specific register (MSR).

8.1.4 Memory Bus Errors

The CNB20HE is programmed to generate an SMI on single-bit data errors in the memory array if ECC memory is installed. The CNB20HE performs the scrubbing. The SMI handler records the error and the DIMM location to the system event log. Double-bit errors in the memory array are mapped to the SMI because the BMC cannot determine the location of the bad DIMM. The double-bit errors may have corrupted the contents of SMRAM. The SMI handler logs the failing

DIMM number to the BMC if the SMRAM contents are still valid. Unrecoverable errors are routed to NMI by BIOS.

If more than ten single-bit errors occur in less than one hour, the BIOS SMI handler stops logging SBEs to avoid filling the event log. The BIOS also prevents further single-bit errors from generating SMIs to avoid a condition known as SMI shock. SMI shock is a condition in which the processors spend all their time servicing SMIs because of a stream of single-bit errors. Note that the chip set will continue to correct single-bit errors and the system will continue to work correctly even if one of the data lines on a DIMM gets stuck. The BIOS enables logging and SMIs the next time the system is rebooted.

8.1.5 Error Event Propagation to SMI#

The diagram below shows how specific error signals are propagated to SMI# on the SKA4 board set.

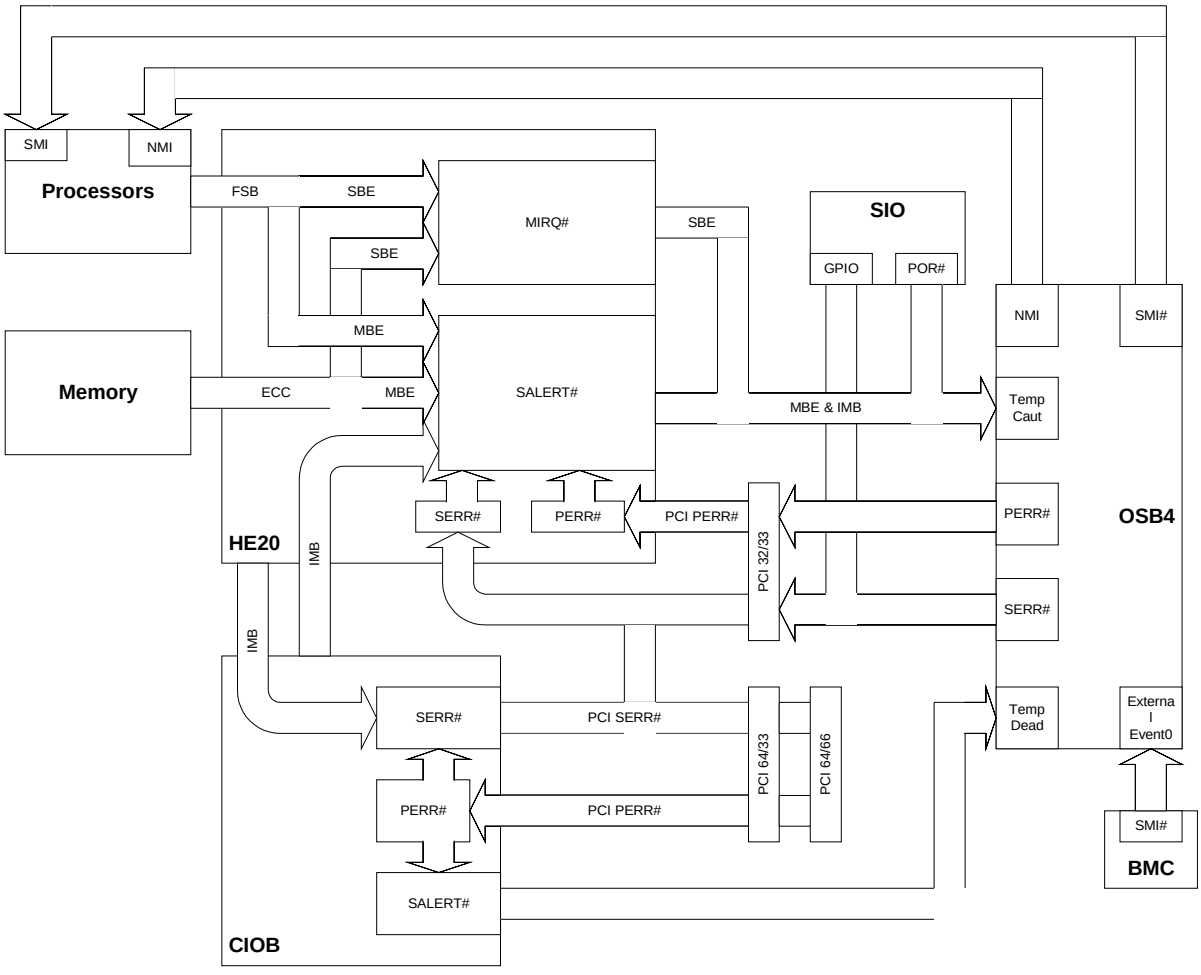

Figure 8-1: SKA4 Error Signal Propagation to SMI#

9. Server Management

The SKA4 server management features are implemented with a Dallas* 80CH11 controller. The following diagram illustrates the SKA4 server management architecture. A description of the hardware architecture follows.

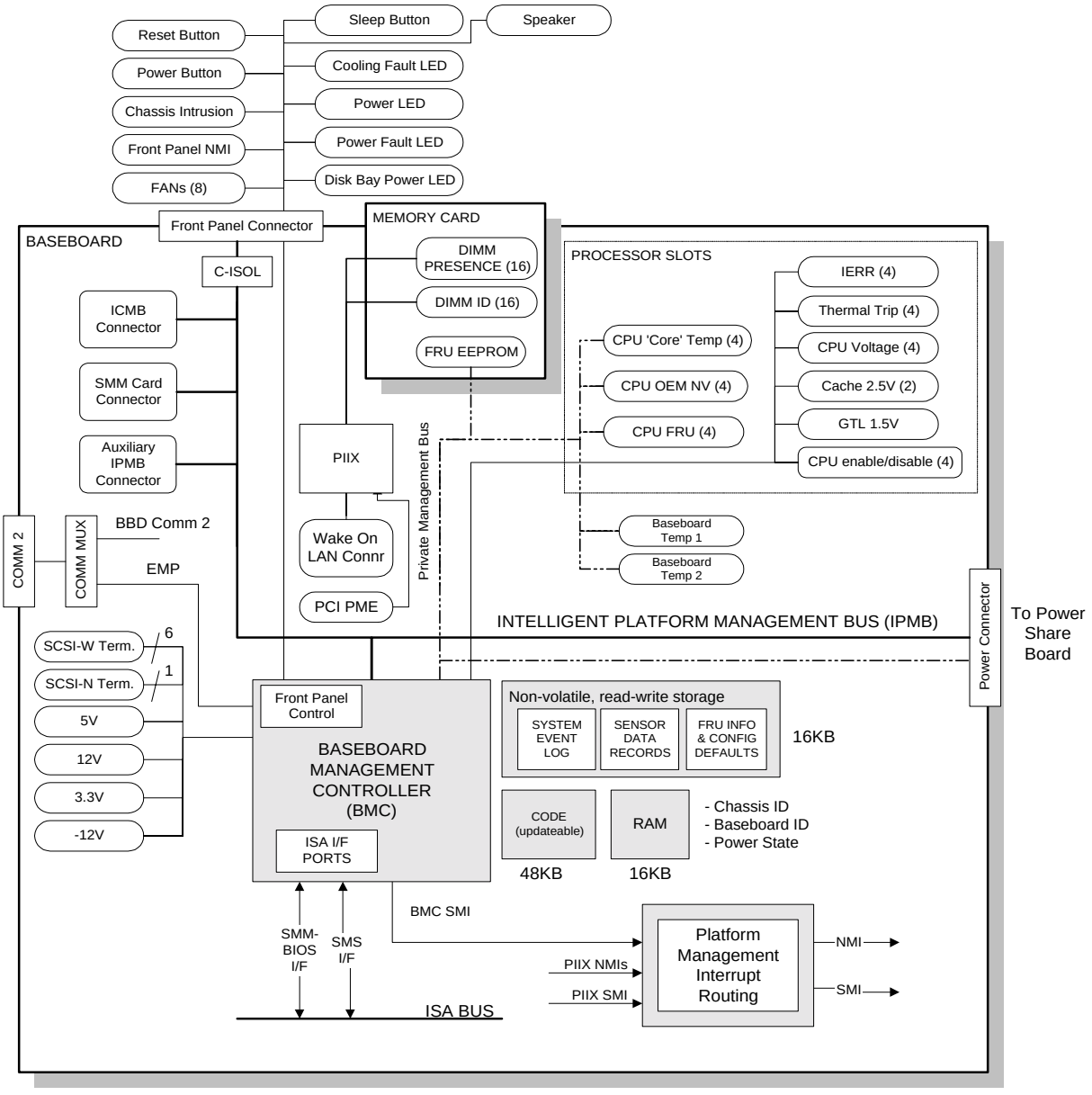

Figure 9-1: SKA4 Server Management Block Diagram

9.1 Baseboard Management Controller

The BMC is an 8051-compatible micro-controller used to monitor the system for critical events. The BMC monitors all power supplies, including those generated by the external power supplies and those regulated locally on the baseboard. The BMC also monitors SCSI termination voltages, fan tachometers for detecting a fan failure, and system temperature. The temperature is measured on each of the processors and at two locations on the baseboard farthest from the fans. When any monitored parameter is outside defined thresholds, the BMC logs an event in its System Event Log (SEL).

The BMC uses three types of memory: flash, SRAM, and serial EEPROM (SEEPROM). The flash and SRAM reside on the BMC external data bus, and the SEEPROM resides on the primary private I^2C bus. The BMC is limited to supporting 64 KB of addressable space on the external data bus. Therefore, two GPIO bits were defined to allow more memory space to be used. The memory address space is selected using the MEM_MODE<0.1> bits to swap between two 64-KB data segments of the flash, and/or swap the flash and SRAM between code and data spaces:

- Memory mode bit 0 selects whether the flash and SRAM are in code space or data space. When bit M0 is logic 1, the flash is in the code space and the SRAM in the data space. Toggling bit M0 will swap the flash and SRAM between the two memory spaces.
- Memory mode bit 1 selects whether the upper or lower half of the 128 KB flash is being used.

The following table contains the memory map for the two devices on this bus. M0 and M1 are the memory mode bits.

Table 9-1: BMC Memory Map

128K Flash			32K SRAM	
Address	**Block**	**Memory Mode**	**Address**	**Block**
0x1FFFF 0x18000	BMC Operational Code	0	0x1FFFF 0x18000	Unused
0x17FFF 0x10000	BMC Operational Code	0	0x17FFF 0x10000	Mirrored SRAM blocks from below
0x0FFFF 0x0A000	System Event Log	1	0x0FFFF 0x08000	Unused
0x09FFF 0x04000	Sensor Data Record / Parameter Access Code	1	0x07FFF 0x02000	XBUS Variables, Parameter Access Code
0x03FFF 0x00000	Boot Block	1	0x01FFF 0x00000	Boot Loader, Flash Update, Mode Switching

The 80CH11 has ten 8-bit I/O ports. The following tables describe the functions.

Table 9-2: BMC Port Connections

Port	Type	Connection
Port 0, bits 7::0	in/out	Multiplexed address/data bus, bits 7::0
Port 1, bits 1::0	out	Memory Mode bits
Port 1, bit 2	in/out	I^2C clock IPMB
Port 1, bit 3	in/out	I^2C data IPMB
Port 1, bit 4	in/out	I^2C clock, BMC primary private bus
Port 1, bit 5	in/out	I^2C data, BMC primary private bus
Port 1, bit 6	in/out	I^2C clock, BMC secondary private bus
Port 1, bit 7	in/out	I^2C data, BMC secondary private bus
Port 2, bits 7::0	out	Address bus, bits 15::8
Port 3, bit 0	in	EMP serial in
Port 3, bit 1	out	EMP serial out
Port 3, bit 2	in	Sleep S5_L (a.k.a. SUSC_L)
Port 3, bit 3	in	RTC clock from SIO, 1Hz
Port 3, bit 4	In	Fan MUX input
Port 3, bit 5	out	Speaker data
Port 3, bit 6	out	BMC write operation
Port 3, bit 7	out	BMC read operation
Port 4, bit 0	in	Front panel power button
Port 4, bit 1	in	Front panel reset button
Port 4, bit 2	in	Front panel NMI button
Port 4, bit 3	in	Front panel sleep button
Port 4, bit 4	in	Power supply power good
Port 4, bit 5	in	Narrow SCSI termination enable
Port 4, bit 6	in	SMM feature connector reset
Port 4, bit 7	in	SMM feature connector power control
Port 5, bit 0	in	Analog: +2.5V
Port 5, bit 1	in	Analog: -12V
Port 5, bit 2	in	Analog: +3.3V
Port 5, bit 3	in	7899 SCSI B Terminators Enabled
Port 5, bit 4	in	Analog: 7880 N SCSI term 0
Port 5, bit 5	in	Analog: 7800 N SCSI term 1
Port 5, bit 6	in	Analog MUX input
Port 5, bit 7		7899 SCSI A Terminators Enabled
Port 6, bit 0	in	Processor presence
Port 6, bit 1	out	BMC Memory Mode Signal #2
Port 6, bit 2	in	NIC SMB alert
Port 6, bit 3	in	Suspend status from OSB4
Port 6, bit 4	in	FRB timer halt
Port 6, bit 5	in	EMP DCD signal
Port 6, bit 6	out	BMC CMOS clear
Port 6, bit 7	out	Power button signal to the SIO
Port 7, bit 0	out	Cooling fault LED
Port 7, bit 1	out	System power fault LED
Port 7, bit 2	out	Power LED

Port	Type	Connection
Port 7, bit 3	out	Video blank signal
Port 7, bit 4	out	Main system reset signal
Port 7, bit 5		Available
Port 7, bit 6	In/out	BMC NMI
Port 7, bit 7	out	Enable EMP
Port 8, bit 0	out	Request to Power supply to turn on
Port 8, bit 1	out	OSB4 sleep
Port 8, bit 2	out	Floppy disk read only
Port 8, bit 3		Available
Port 8, bit 4	out	Stop processor 1
Port 8, bit 5	out	Stop processor 2
Port 8, bit 6	out	Stop processor 3
Port 8, bit 7	out	Stop processor 4
Port 9, bit 0	out	MUX select line 0
Port 9, bit 1	out	MUX select line 1
Port 9, bit 2	out	MUX select line 2
Port 9, bit 3	in/out	BMC SMI_L
Port 9, bit 4	in	Secure mode keyboard
Port 9, bit 5	out	Forced update mode
Port 9, bit 6	out	Digital MUX input 1
Port 9, bit 7	out	EMP ring indicate signal
Port 10, bit 0	in	Processor IERR 1
Port 10, bit 1	in	Processor IERR 2
Port 10, bit 2	in	Processor IERR 3
Port 10, bit 3	in	Processor IERR 4
Port 10, bit 4	in	Processor OCVR Okay 1
Port 10, bit 5	in	Processor OCVR Okay 2
Port 10, bit 6	in	Processor OCVR Okay 3
Port 10, bit 7	in	Processor OCVR Okay 4

Table 9-3: BMC MUX Input Selection

Signal	BMC_MUXSEL(2:0)	Input selected
BMC_FAN_MUX	000	Fan 1
	001	Fan 2
	010	Fan 3
	011	Fan 4
	100	Fan 5/Processor Fan 1
	101	Fan 6/Processor Fan 2
	110	Fan 7/Processor Fan 3
	111	Fan 8/Processor Fan 4
ANALOG_MUX_IN	000	VCC Processor 3
	001	VCC Processor 4
	010	VCC Cache 1,2
	011	VCC Cache 3,4
	100	7899 SCW A Termination 0
	101	7899 SCWA Termination 1

Signal	BMC_MUXSEL(2:0)	Input selected
	110	7899 SCWB Termination 0
	111	7899 SCWB Termination 1
BMC_DINPUT0	000	Host SMI_L In
	001	PCI hot plug power state 5
	010	PCI hot plug attention 0
	011	PCI hot plug attention 1
	100	PCI hot plug attention 2
	101	PCI hot plug attention 3
	110	PCI hot plug attention 4
	111	PCI hot plug attention 5

An ADM1024 is attached to the secondary I^2C bus for monitoring the two system temperatures (one internal and one external to the part) and additional analog voltages. The table below describes these added signals. The ADM1024 device also provides a digital-to-analog converter for use in fan speed control. The output is 0-2.5V and is connected to the power subsystem for proper conversion of the fan voltage rails.

Table 9-4: BMC ADM1024 Input Definition

ADM1024 Pin	Type	Attached Signal
9	Analog Input	+3.3V standby
16	Analog Input	+5V
15	Analog Input	+12V
6	Analog Input	+1.5V
19	Analog Input	VCC Processor 1
5	Analog Input	VCC Processor 2
11	Analog Output	Fan speed control
17	Analog Input	Unused
18	Analog Input	Unused
13,14	Temperature In	Baseboard Temperature 2
20	Digital Input	PCI hot-plug power state 0
21	Digital Input	PCI hot-plug power state 1
22	Digital Input	PCI hot-plug power state 2
23	Digital Input	PCI hot-plug power state 3
24	Digital Input	PCI hot-plug power state 4
7	Digital Input	Chassis Intrusion

9.1.1 Fault Resilient Booting

The BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If the default bootstrap processor (BSP) fails to complete the boot process, FRB attempts to boot using an alternate processor.

- FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.
- FRB level 2 is for recovery from a Watchdog timeout during POST. The Watchdog timer for FRB level 2 detection is implemented in the BMC.

- FRB level 3 is for recovery from a Watchdog timeout on Hard Reset/Power-up. Hardware functionality for this level of FRB is provided by the BMC.

9.1.1.1 FRB-1

In a multiprocessor system, the BIOS registers the application processors in the MP table and in the ACPI APIC tables. If an application processor (AP) fails to complete initialization after it is started by the boot-strap processor (BSP), it is assumed to be nonfunctional.

If the BIOS detects that an application processor has failed BIST or is nonfunctional, it requests that the BMC disable that processor. The BMC generates a system reset while disabling the processor and the BIOS will not see the bad processor in the next boot cycle. The failing AP is not listed in the MP table (refer to Revision 1.4 of the *Multi-Processor Specification*), nor in the ACPI APIC tables, and it is invisible to the OS.

If the BIOS detects that the BSP has failed BIST, it sends a request to BMC to disable the processor and make an alternate processor the BSP. If no alternate processor is available, the BMC beeps the speaker and halts the system. If BMC can identify another processor, BSP ownership is transferred to that processor via a system reset.

The BIOS sets the second watchdog timer (FRB-2) in the BMC for approximately six minutes. This is designed to guarantee that the system completes BIOS POST. The FRB-2 timer is enabled before the FRB-3 timer is disabled to prevent any “unprotected” window of time.

Near the end of POST, before the option ROMs are initialized, the BIOS disables the FRB-2 timer in the BMC. If the system contains more than 1 GB of memory and the user chooses to test every DWORD of memory, the watchdog timer is disabled before the extended memory test starts, because the memory test can take more than six minutes under this configuration.

If the system hangs during POST, the BIOS does not disable the timer in the BMC, which generates an asynchronous system reset (ASR). For more details, refer to *SKA4 Server Management EAS* and the *Baseboard Management Controller Interface Specification.*

9.1.1.2 FRB-3

The first timer (FRB-3) begins counting down when the system comes out of hard reset, which takes about five seconds. If the BSP successfully resets and starts executing, the BIOS disables the FRB-3 timer in the BMC by de-asserting the FRB_TIMER_HLT* signal (GPIO) and the system continues with the POST.

If the timer expires because the BSP fails to fetch or execute BIOS code, the BMC resets the system and disables the failed processor. The system continues to change the bootstrap processor until the BIOS POST gets past disabling the FRB-3 timer in the BMC. The BMC sounds beep codes on the speaker, if it fails to find a good processor. The process of cycling through all the processors is repeated upon system reset or power cycle.

9.2 System Reset Control

Reset circuitry on the SKA4 baseboard looks at resets from the front panel, OSB4, ITP, and processor subsystem to determine proper reset sequencing for all types of reset. The reset

logic is designed to accommodate a variety of ways to reset the system, which can be divided into the following categories:

- Power-up reset.
- Hard reset.
- Soft (programmed) reset.

The following subsections describe each category of reset.

9.2.1 Power-up Reset

When the system is disconnected from AC power, all logic on the baseboard is powered off. When a valid input (AC) voltage level is provided to the power supply, 5-volt standby power is be applied to the baseboard. A power monitor circuit on 5-volt standby asserts the **RST_BMC** signal, causing the BMC to reset. The BMC is powered by the 5-volt standby and monitors and controls key events that are related to reset and power control.

After the system is turned on, the power supply assert the **PWR_GD_PS** signal after all voltage levels in the system have reached valid levels. The BMC receives **PWR_GD_PS** and after 500 ms it asserts **P6_PWR_GOOD,** which indicates to the processors and OSB4 that the power is stable. Upon the assertion of the **P6_PWR_GOOD** signal, the OSB4 toggles PCI reset.

The **P6_PWR_GOOD** signal is also used for isolation control of the Intelligent Platform Management Bus (IPMB) via the front panel. For more details, see Section 9.3.

9.2.2 Hard Reset

Hard reset can be initiated by software, by the user resetting the system through the front panel switch, or through the Server Management Module (SMM). For front panel or SMM resets, the BMC de-asserts **P6_PWR_GOOD**. After 600 ms, it is reasserted, and the Power-up Reset sequence is done (see Section 9.2.1).

The BMC is not reset by a hard reset. It may be reset at power-up.

9.2.3 Soft Reset

A soft reset causes the processors to begin execution in a known state without flushing the caches or internal buffers. Soft resets can be generated by the keyboard controller located in the SIO or by the OSB4. The output of the SIO (**RST_KB_L**) is input to the OSB4.

9.3 Intelligent Platform Management Buses

Management controllers and sensors communicate on the I^2C-based Intelligent Platform Management Bus. A bit protocol, defined by the *I^2C Bus Specification*, and a byte-level protocol, defined by the *Intelligent Platform Management Bus Communications Protocol Specification*, provide an independent interconnect for all devices operating on this I^2C bus. The IPMB extends throughout the baseboard and system chassis. An added layer in the protocol supports transactions between multiple servers on inter-chassis I^2C bus segments.

The IPMB connects to various devices that are external to the baseboard. The IPMB connectors outside of the baseboard (Auxiliary IPMB, remote management card, and ICMB) cannot load the bus without power because to do so would prevent bus communication. For devices that are attached through the front panel connector, an isolation circuit disconnects the bus from the BMC when power good is inactive. The table below lists all baseboard connections to the IPMB.

Table 9-5: IPMB Bus Devices

IPMB I^2C Addresses				
Function	**Voltage**	**Supply**	**Address**	**Notes**
ICMB	5	standby	0x28	
BMC controller	5	standby	0x20	
SMM card connector	5	standby	not assigned	
Auxiliary IPMB connector	5	standby	not assigned	
SCSI hot swap controller	5	standby	TBD	
FDB FRU SEEPROM	5	standby	0xAA	AT24C02
FDB Fan Fail Indicator	5	standby	0x4E	PCF8574
FDB Fan Fail Indicator	5	standby	0x46	PCF8574
FDB Temp Sense	5	standby	0x9A	DS1621

Besides the “public” IPMB, the BMC also has two private I^2C buses. The BMC is the only master on the private bus. The table below lists all baseboard connections to the BMC private I^2C buses.

Table 9-6: BMC Primary Private I^2C Bus Devices

Primary Private Bus				
Function	**Voltage**	**Supply**	**Address**	**Notes**
Power Distribution Board (PDB) - Heceta 3	5	standby	0x5A	Connects to SSI HS Power Supplies
PDB FRU SEEPROM	5	standard	0xA6	AT24C02
PS 1 FRU SEEPROM	5	standard	0xA0	AT24C02
PS 2 FRU SEEPROM	5	standard	0xA2	AT24C02
PS 3 FRU SEEPROM	5	standard	0xA4	AT24C02
BMC SEEPROM	5	standby	0xAE	AT24C08
Memory Board FRU SEEPROM	3.3	standard	0xAC	AT24C02
CPU Speed Mux (Write)	3.3	standard	0x9C	PCF8550
CPU Speed Mux (Read)	3.3	standard	0x9D	PCF8550

Table 9-7: BMC Secondary Private I²C Bus Devices

Secondary Private Bus				
Function	**Voltage**	**Supply**	**Address**	**Notes**
Baseboard Heceta 3	3.3	standby	0x58	Placed near the PCI slots; monitors two baseboard temps, five analog voltages, and chassis intrusion.
CPU1 SEEPROM	3.3	standby	0xA0	VID information and OEM access.
CPU1 RO SEEPROM	3.3	standby	0xA2	
CPU1 temp	3.3	standby	0x30	Core temperature reading.
CPU2 SEEPROM	3.3	standby	0xA4	
CPU2 RO SEEPROM	3.3	standby	0xA6	
CPU2 temp	3.3	standby	0x98	
CPU3 SEEPROM	3.3	standby	0xA8	
CPU3 RO SEEPROM	3.3	standby	0xAA	
CPU3 temp	3.3	Standby	0x34	
CPU4 SEEPROM	3.3	Standby	0xAC	
CPU4 RO SEEPROM	3.3	Standby	0xAE	
CPU4 temp	3.3	Standby	0x9C	

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10. Jumpers

10.1 Hardware Configuration (J9F2, J9F1, J9G1)

This section describes jumper options on the baseboard. Refer to the *SKA4 Basic Input Output System (BIOS) EPS* for information on configuration and initialization as done by BIOS and POST code, using configuration registers.

Four 3-pin jumper blocks control various configuration options, as shown in the figure below. The shaded areas show the default jumper placement for each configurable option.

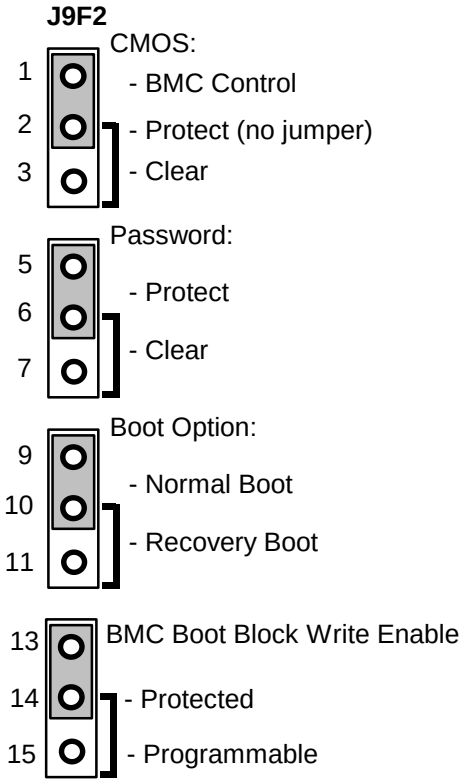

Figure 10-1: SKA4 Configuration Jumpers

The following table describes each jumper option.

Table 10-1: Configuration Jumper Options

Option	Description
CMOS	If pins 1 and 2 of J9F2 are jumpered (default), the contents of NVRAM are preserved through system reset unless the user clears them through the front panel (by holding down the Power and Reset buttons together for four seconds). If pins 2 and 3 of J9F2 are jumpered, NVRAM contents are set to manufacturing default during system reset. If the jumper is removed, NVRAM contents are preserved through system reset.
Password	If pins 5 and 6 of J9F2 are jumpered (default), the current system password is maintained during system reset. If pins 6 and 7 of J9F2 are jumpered, the password is cleared on reset.
Boot Option	If pins 9 and 10 of J9F2 are jumpered (default), BIOS will jump to a protected area of the flash part containing the "Recovery BIOS." If the normal BIOS gets corrupted, and you are unable to reload a fresh copy from the floppy disk, install the jumper between pins 10 and 11 of J9F2, which enables the system to boot from the Recovery BIOS. This code expects a fresh copy of the normal BIOS to be located on a floppy disk present in the floppy drive. See the *SKA4 Basic Input Output System (BIOS) EPS* for more detailed information.
BMC Boot Block Write Enable	This jumper provides protection for the BMC flash boot block. If pins 13 and 14 of J9F2 are jumpered (default), the BMC boot block is protected. If pins 14 and 15 of J9F2 are jumpered, writes to the BMC boot block are allowed.

11. Connections

11.1 Connector Locations

The diagram below identifies the connector locations.

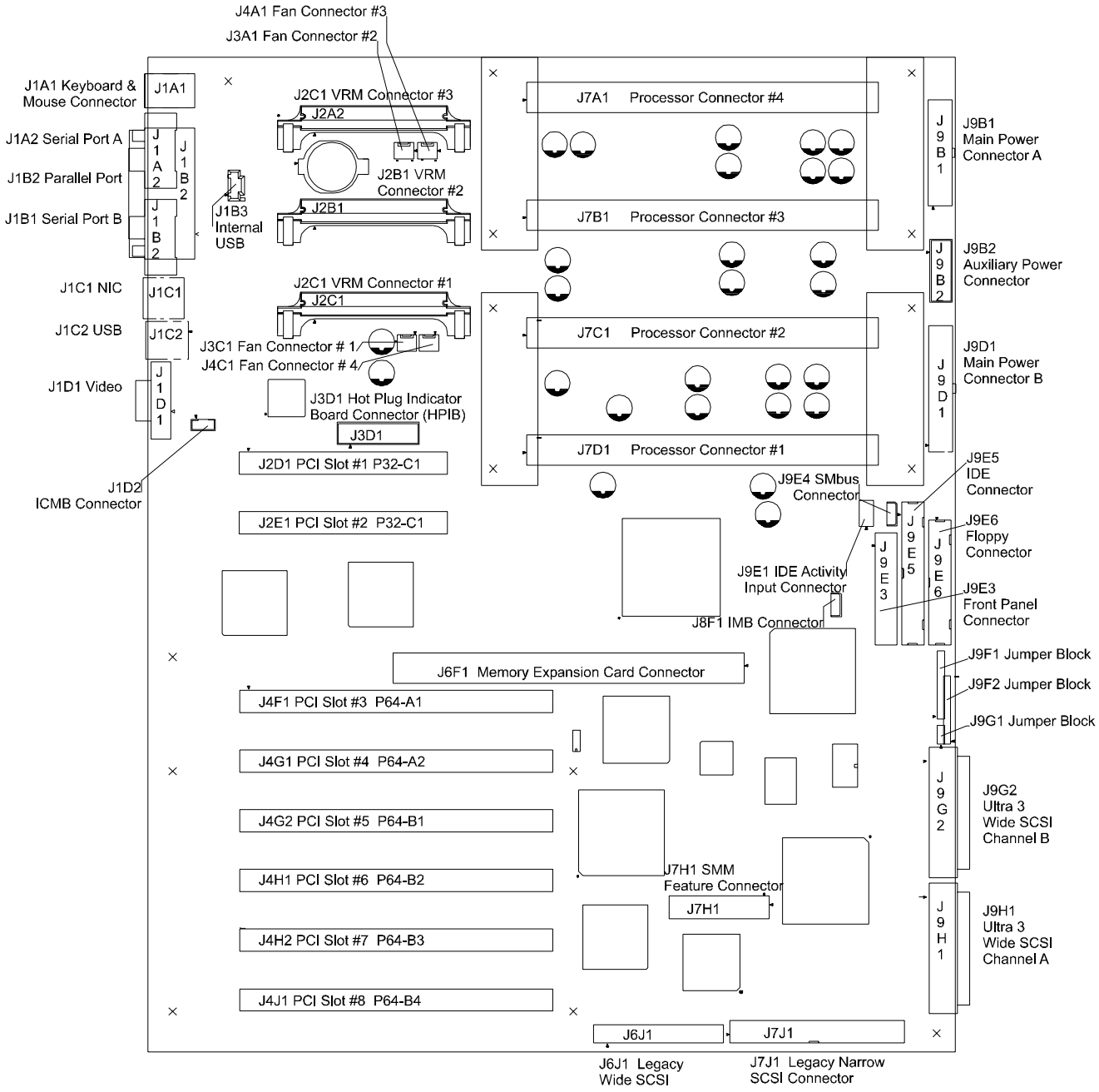

Figure 11-1: SKA4 Baseboard Connector Identification and Locations

11.2 Power Distribution Board Interface Connectors (J9B1, J9D1, J9B2)

The SKA4 Baseboard and Memory board receive their main power through two primary and one auxiliary power connectors. The two main power connectors are identified as J9B1 and J9D1. The auxiliary power connector, identified as J9B2, provides a power subsystem communication path, control signals, power supply sense connections and other miscellaneous signals defined below.

Table 11-1: Main Power Connector A (J9B1)

Pin	Signal	Type[1]	Current Carrying Capability	Description
1	12V	power	6 Amps	Power supply 12V
2	Ground	ground	6 Amps	Ground return connection
3	Ground	ground	6 Amps	Ground return connection
4	Ground	ground	6 Amps	Ground return connection
5	Ground	ground	6 Amps	Ground return connection
6	VCC	power	6 Amps	Power supply 5V
7	VCC	power	6 Amps	Power supply 5V
8	VCC	power	6 Amps	Power supply 5V
9	VCC	power	6 Amps	Power supply 5V
10	VCC	power	6 Amps	Power supply 5V
11	SB5V	power	6 Amps	Power supply 5V standby
12	Ground	ground	6 Amps	Ground return connection
13	Ground	ground	6 Amps	Ground return connection
14	Ground	ground	6 Amps	Ground return connection
15	Ground	ground	6 Amps	Ground return connection
16	VCC	power	6 Amps	Power supply 5V
17	VCC	power	6 Amps	Power supply 5V
18	VCC	power	6 Amps	Power supply 5V
19	VCC	power	6 Amps	Power supply 5V
20	VCC	power	6 Amps	Power supply 5V

Note:
1. Type (in, out, in/out, power, ground) is from the perspective of the baseboard.

Table 11-2: Main Power Connector B (J9D1)

Pin	Signal	Type[1]	Current Carrying Capability	Description
1	VCC3	power	6 Amps	Power supply 3.3V
2	VCC3	power	6 Amps	Power supply 3.3V
3	VCC3	power	6 Amps	Power supply 3.3V
4	VCC3	power	6 Amps	Power supply 3.3V
5	VCC3	power	6 Amps	Power supply 3.3V
6	VCC3	power	6 Amps	Power supply 3.3V
7	Ground	ground	6 Amps	Ground return connection

Pin	Signal	Type[1]	Current Carrying Capability	Description
8	Ground	ground	6 Amps	Ground return connection
9	Ground	ground	6 Amps	Ground return connection
10	Ground	ground	6 Amps	Ground return connection
11	Ground	ground	6 Amps	Ground return connection
12	12V	power	6 Amps	Power supply 12V
13	VCC3	power	6 Amps	Power supply 3.3V
14	VCC3	power	6 Amps	Power supply 3.3V
15	VCC3	power	6 Amps	Power supply 3.3V
16	VCC3	power	6 Amps	Power supply 3.3V
17	VCC3	power	6 Amps	Power supply 3.3V
18	VCC3	power	6 Amps	Power supply 3.3V
19	Ground	ground	6 Amps	Ground return connection
20	Ground	ground	6 Amps	Ground return connection
21	Ground	ground	6 Amps	Ground return connection
22	Ground	ground	6 Amps	Ground return connection
23	Ground	ground	6 Amps	Ground return connection
24	12V	power	6 Amps	Power supply 12V

Note:
1. Type (in, out, in/out, power, ground) is from the perspective of the baseboard.

Table 11-3: Auxiliary Power Connector (J9B2)

Pin	Signal	Type[1]	Current Carrying Capability	Description
1	Ground	ground		Ground return connection
2	5V Sense	out	N/A	Sense line feedback to power supply
3	3.3V Sense	out	N/A	Sense line feedback to power supply
4	BMC FAN SPD CTL	out	N/A	
5	SM PRI 5VSB SCL	In/out	N/A	Server Management I2C bus - clock
6	SM PRI 5VSB SDA	In/out	N/A	Server Management I2C bus - data
7	Ground	ground		Ground return connection
8	PWRGD PS	In	N/A	Signal from power subsystem indicating power is stable
9	PS PWR ON_L	Out	N/A	Control signal from baseboard to power supply
10	Ground	ground		Ground return connection
11	-12V	power		Power supply negative 12V
12	Key		N/A	
13	12V	power		Power supply 12V
14	Ground	ground		Ground return connection

Note:
1. Type (in, out, in/out, power, ground) is from the perspective of the baseboard.

11.3 Front Panel Interface (J9E3)

A 30-pin header is provided that attaches to the system front panel. The header contains reset, NMI, sleep, and power control buttons, LED indicators, and an IPMB connection. The table below summarizes the front panel signal pins, including the signal mnemonic, name, and a brief description.

Table 11-4: Front Panel Connector (J9E3)

Pin	Signal	Type[1]	Description
1	SPKR_FP	out	SPEAKER DATA for the front panel/chassis mounted speaker.
2	GROUND	ground	GROUND is the power supply ground.
3	CHASSIS_INTRUSION	in	CHASSIS INTRUSION is connected to the BMC and indicates that the chassis has been opened. CHASSIS_INTRUSION is pulled high to +5 V standby on the baseboard.
4	FP_HD_ACT*	out	HARD DRIVE ACTIVITY indicates there is activity on one of the hard disk controllers in the system.
5	+5V	power	+5 V is the 5 volt power supply.
6	FP_SLP_BTN*	in	FRONT PANEL SLEEP is connected to the BMC and causes the system to be put to sleep if supported by the operating system. FP_SLP_BTN* is pulled high to +5 V on the baseboard and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front.
7	COOL_FLT_LED*	out	COOLING FAULT LED indicates that either a fan failure has occurred or the system is approaching an over-temperature situation. COOL_FLT_LED* is an output of the BMC.
8	PWR_LED*	out	POWER PRESENT LED.
9	PWR_FLT_LED*	out	SYSTEM FAULT indicates that either a power fault or SCSI drive failure has occurred in the system.
10	GROUND	ground	GROUND is the power supply ground.
11	SM_IMB_SDA	in/out	I^2C DATA is the data signal for the Intelligent Platform Management Bus.
12	FP_NMI_BTN*	in	FRONT PANEL NMI is connected to a BMC input port, allowing the front panel to generate an NMI. FP_NMI_BTN* is pulled high to +5 V on the baseboard and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front panel.
13	SM_IMB_SCL	in/out	I^2C CLOCK is the clock signal for the Intelligent Platform Management Bus.
14	FP_RST_BTN*	in	FRONT PANEL RESET is connected to the BMC and causes a hard reset to occur, resetting all baseboard devices except for the BMC and BMC. FP_RST_BTN* is pulled high to +5V on the baseboard, and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front panel.
15	+5V standby	power	+5 V STANDBY is the standby 5 volt power supply.
16	FP_PWR_BTN*	in	FRONT PANEL POWER CONTROL is connected to the BMC and causes the power to toggle (on → off, or off → on). FP_PWR_BTN* is pulled high to +5 V standby on the baseboard and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front panel.
17	SM_FP_ISOL	in	SM_FP_ISOL, when asserted, isolates the front panel SM bus.
18	GROUND	ground	GROUND is the power supply ground.
19	FAN_TACH(0)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
20	FAN_TACH(1)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.

Pin	Signal	Type[1]	Description
21	FAN_TACH(2)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
22	FAN_TACH(3)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
23	FAN_TACH(4)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
24	FAN_TACH(5)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
25	FAN_TACH(6)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
26	FAN_TACH(7)	in	FAN_TACH signal is connected to the BMC to monitor the FAN speed.
27	RJ45_ACTLED_R	in	NIC activity LED.
28	reserved	-	Reserved.
29	SM_PRI_SCL	in/out	I^2C CLOCK is the clock signal for the Primary Private Bus.
30	SM_PRI_SDA	in/out	I^2C DATA is the data signal for the Primary Private Bus.

Notes:
1. Type (in, out, in/out, power, ground) is from the perspective of the baseboard.

11.4 Hot-plug PCI Indicator Board Interface (J3D1)

The Hot-plug PCI Indicator Board (HPIB) contains the necessary LEDs and push button switches to help the user run PCI Hot-plug operations.

Each PHP slot contains a green LED and an amber LED to indicate slot status. The actual interpretation of the LEDs depends on the operating system running on the system.

Each PHP slot also has a momentary push button switch used to notify the operating system that a PHP operation on the respective slot is requested. If PHP operation is supported by the operating system, the user momentarily presses the switch and then waits for the operating system to signal via the LEDs that the PHP slot has been disabled. The user can then perform the desired PHP operation on the slot, such as replacing, removing, or adding a PCI adapter. When the user wants the operating system to enable and initialize the PHP slot, the user momentarily presses the switch again.

This (Active Low) push button switch for the respective slot is routed to the PRSNT1# input to the PCI Hot-plug controller. This switch should not be confused with slot-interlock switches, which are used in conjunction with mechanical lever designs to prevent access to an energized PHP slot. The slot interlock inputs into the PHPC are permanently pulled down to ground and are not accessible through the Hot-plug PCI Indicator Board Interface.

The Hot-plug PCI Indicator Board Interface contains the signals necessary to drive the LEDs and receive the push button signals.

A 20-pin connector is provided on the baseboard for connection to the external HPIB. The pinout for this connector is as follows:

Table 11-5: Hot-plug Indicator Board Connector Pinout (J3D1)

Connector Contact	Signal Name	Connector Contact	Signal Name
1	Vcc	2	GROUND
3	P64_A_SWITCH<0>	4	P64_A_GRN_LED<1>

Connector Contact	Signal Name	Connector Contact	Signal Name
5	P64_A_AMB_LED<0>	6	P64_A_SWITCH<1>
7	P64_A_GRN_LED<1>	8	P64_A_AMB_LED<1>
9	P64_B_SWITCH<0>	10	P64_A_GRN_LED<0>
11	P64_B_AMB_LED<0>	12	P64_B_SWITCH<1>
13	P64_B_GRN_LED<1>	14	P64_A_AMB_LED<1>
15	P64_B_SWITCH<2>	16	P64_A_GRN_LED<2>
17	P64_A_AMB_LED<2>	18	P64_B_SWITCH<3>
19	P64_A_GRN_LED<3>	20	P64_A_AMB_LED<3>

11.5 Memory Board Interface (J6F1)

Table 11-6: Memory Board Connector Pinout (J6F1)

Pin[1]	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A001	GND	B001	PIN_B1	A084	GND	B084	MAA9
A002	GND	B002	VCC3	A085	MAA10	B085	VCC3
A003	GND	B003	SYNTH_OUT_MADPCLK	A086	MAA11	B086	MAA12
A004	GND	B004	VCC3	A087	GND	B087	MAA13
A005	ASCLK	B005	VCC3	A088	MAA14	B088	VCC3
A006	CMD0	B006	ASDATA	A089	MCD_MUXSEL	B089	VCC3
A007	GND	B007	CMD16	A090	GND	B090	VCC3
A008	CMD1	B008	VCC3	A091	BSCLK	B091	VCC3
A009	CMD2	B009	CMD3	A092	MECC12	B092	BSDATA
A010	GND	B010	CMD19	A093	GND	B093	MECC14
A011	CMD17	B011	VCC3	A094	MECC13	B094	VCC3
A012	CMD4	B012	CMD20	A095	MECC15	B095	CMD97
A013	GND	B013	CMD6	A096	GND	B096	CMD96
A014	CMD18	B014	VCC3	A097	CMD112	B097	VCC3
A015	CMD5	B015	CMD21	A098	CMD113	B098	CMD98
A016	GND	B016	CMD23	A099	GND	B099	CMD99
A017	CMD8	B017	VCC3	A100	CMD114	B100	VCC3
A018	CMD7	B018	CMD22	A101	CMD100	B101	CMD116
A019	GND	B019	CMD9	A102	GND	B102	CMD115
A020	CMD25	B020	VCC3	A103	CMD101	B103	VCC3
A021	CMD26	B021	CMD24	A104	CMD117	B104	CMD102
A022	GND	B022	CMD10	A105	GND	B105	CMD103
A023	CMD12	B023	VCC3	A106	CMD118	B106	VCC3
A024	CMD28	B024	CMD11	A107	CMD119	B107	CMD104
A025	GND	B025	CMD27	A108	GND	B108	CMD120
A026	CMD29	B026	VCC3	A109	CMD105	B109	VCC3
A027	CMD14	B027	CMD30	A110	CMD121	B110	CMD106
A028	GND	B028	CMD13	A111	GND	B111	CMD107
A029	CMD15	B029	VCC3	A112	CMD122	B112	VCC3
A030	CMD31	B030	MECC0	A113	CMD123	B113	CMD108
A031	GND	B031	MECC1	A114	GND	B114	CMD124

Pin[1]	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A032	MECC2	B032	VCC3	A115	CMD109	B115	VCC3
A033	MECC3	B033	CKE_0	A116	CMD125	B116	CMD110
A034	GND	B034	0_RAS	A117	GND	B117	CMD126
A035	0_WE[3]	B035	VCC3	A118	GND	B118	VCC3
A036	0_CAS	B036	0_CS0	A119	GND	B119	VCC3
A037	GND	B037	0_CS1	A120	CMD111	B120	VCC3
A038	0_CS2	B038	VCC3	A121	CMD127	B121	CKE_1
A039	0_CS3	B039	0_MCDOE[3]	A122	GND	B122	1_RAS
A040	GND	B040	MEMPRSNT	A123	1_WE[3]	B123	VCC3
A041	0_MCDSEL[3]	B041	VCC3	A124	1_CAS	B124	1_CS0
A042	GND	B042	TMD0	A125	GND	B125	1_CS1
A043	GND	B043	VCC3	A126	1_CS2	B126	VCC3
A044	CMD34	B044	VCC3	A127	1_CS3	B127	1_MCDOE[3]
A045	CMD50	B045	CMD49	A128	GND	B128	1_MCDSEL[3]
A046	GND	B046	CMD54	A129	CMD80	B129	VCC3
A047	CMD52	B047	VCC3	A130	MECC8	B130	MECC10
A048	CMD51	B048	CMD33	A131	GND	B131	CMD64
A049	GND	B049	CMD32	A132	CMD81	B132	VCC3
A050	CMD40	B050	VCC3	A133	MECC9	B133	MECC11
A051	CMD38	B051	CMD53	A134	GND	B134	CMD65
A052	GND	B052	CMD36	A135	CMD66	B135	VCC3
A053	CMD35	B053	VCC3	A136	CMD82	B136	CMD85
A054	CMD42	B054	CMD58	A137	GND	B137	CMD67
A055	GND	B055	CMD39	A138	CMD83	B138	VCC3
A056	GND	B056	VCC3	A139	CMD84	B139	CMD68
A057	GND	B057	VCC3	A140	GND	B140	CMD71
A058	CMD55	B058	VCC3	A141	CMD87	B141	VCC3
A059	CMD37	B059	CMD43	A142	CMD70	B142	CMD86
A060	GND	B060	CMD57	A143	GND	B143	CMD69
A061	CMD56	B061	VCC3	A144	CMD73	B144	VCC3
A062	CMD62	B062	CMD63	A145	CMD89	B145	CMD72
A063	GND	B063	CMD61	A146	GND	B146	CMD88
A064	CMD44	B064	VCC3	A147	CMD76	B147	VCC3
A065	CMD60	B065	CMD41	A148	CMD92	B148	CMD75
A066	GND	B066	MECC6	A149	GND	B149	CMD91
A067	CMD47	B067	VCC3	A150	CMD74	B150	VCC3
A068	CMD48	B068	CMD59	A151	CMD90	B151	CMD78
A069	GND	B069	CMD45	A152	GND	B152	CMD77
A070	CMD46	B070	VCC3	A153	CMD94	B153	VCC3
A071	MECC7	B071	MECC4	A154	CMD93	B154	CMD79
A072	GND	B072	MECC5	A155	GND	B155	CMD95
A073	GND	B073	VCC3	A156	GND	B156	VCC3
A074	MADPCLK_FB_DLY	B074	VCC3	A157	GND	B157	VCC3
A075	GND	B075	BCLK_MADP_OUT	A158	GND	B158	VCC3
A076	MAA0	B076	VCC3	A159	GND	B159	VCC3
A077	MAA1	B077	VCC3	A160	GND	B160	VCC3
A078	GND	B078	SDRDCLK_HE_DLY	A161	GND	B161	VCC3
A079	MAA2	B079	VCC3	A162	GND	B162	RESERVED162

Pin[1]	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A080	MAA3	B080	MAA4	A163	GND	B163	VCC
A081	GND	B081	MAA5	A164	GND	B164	VCC
A082	MAA6	B082	VCC3	A165	PIN_A165	B165	VCC
A083	MAA7	B083	MAA8	A166	NC	B166	NC

Note:
1. Pins are numbered with respect to the cartridge edge connector. Axx signals appear on the front (processor side) of the processor card. For mechanical specifications, see Section 12.
2. Signals that have no connection except for a pullup resistor to 2.5 volts are labeled with the signal mnemonic followed by "(pu)."
3. Signal is active low.

11.6 Processor Cartridge Support

11.6.1 Processor Cartridge Connector (J7A1, J7B1, J7C1, J7D1)

Table 11-7: Processor Card Connector Pinout (J7A1, J7B1, J7C1, J7D1)

Pin[1]	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A001	RESERVED (nc)	B001	PWR_EN1	A084	GND	B084	RESERVED (nc)
A002	VCC_TAP	B002	VCCP	A085	D11[3]	B085	VCCP
A003	RESERVED (nc)	B003	OCVR_OK[3]	A086	D10[3]	B086	D17[3]
A004	GND	B004	TEST_VSS_B4	A087	GND	B087	D15[3]
A005	VTT	B005	VCCP	A088	D14[3]	B088	VCCP
A006	VTT	B006	VTT	A089	D9[3]	B089	D12[3]
A007	SELFSB1	B007	VTT	A090	GND	B090	D7[3]
A008	RESERVED_A8	B008	VCCP	A091	D8[3]	B091	VCCP
A009	RESERVED_A9	B009	RESERVED (nc)	A092	D5[3]	B092	D6[3]
A010	GND	B010	FLUSH[3]	A093	GND	B093	D4[3]
A011	TEST_GND (pd)	B011	VCCP	A094	D3[3]	B094	VCCP
A012	IERR[3]	B012	SMI[3]	A095	D1[3]	B095	D2[3]
A013	GND	B013	INIT[3]	A096	GND	B096	D0[3]
A014	A20M[3]	B014	VCCP	A097	BCLK	B097	VCCP
A015	FERR[3]	B015	STPCLK[3]	A098	TEST_VSS (pd)	B098	RESET[3]
A016	GND	B016	TCK	A099	GND	B099	FRCERR
A017	IGNNE[3]	B017	VCCP	A100	BERR[3]	B100	VCCP
A018	TDI	B018	SLP[3]	A101	A33[3]	B101	A35[3]
A019	GND	B019	TMS	A102	GND	B102	A32[3]
A020	TDO	B020	VCCP	A103	A34[3]	B103	VCCP
A021	PWRGOOD	B021	TRST[3]	A104	A30[3]	B104	A29[3]
A022	GND	B022	RESERVED (nc)	A105	GND	B105	A26[3]
A023	TEST_25 (pu)[2]	B023	VCCP	A106	A31[3]	B106	VCCL2
A024	THERMTRIP[3]	B024	RESERVED (nc)	A107	A27[3]	B107	A24[3]
A025	GND	B025	RESERVED (nc)	A108	GND	B108	A28[3]
A026	OCRV_EN	B026	VCCP	A109	A22[3]	B109	VCCL2
A027	INTR	B027	TEST_VCCP (pu)	A110	A23[3]	B110	A20[3]
A028	GND	B028	NMI	A111	GND	B111	A21[3]
A029	PICD0	B029	VCCP	A112	A19[3]	B112	VCCL2
A030	PREQ[3]	B030	PICCLK	A113	A18[3]	B113	A25[3]

Pin[1]	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A031	GND	B031	PICD1	A114	GND	B114	A15[3]
A032	BP3[3]	B032	VCCP	A115	A16[3]	B115	VCC_L2
A033	BMP0[3]	B033	BP2[3]	A116	A13[3]	B116	A17[3]
A034	GND	B034	RESERVED (nc)	A117	GND	B117	A11[3]
A035	BINIT[3]	B035	VCCP	A118	A14[3]	B118	VCC_L2
A036	DEP0[3]	B036	PRDY[3]	A119	GND	B119	A12[3]
A037	VSS	B037	BPM1[3]	A120	A10[3]	B120	VCCL2
A038	DEP1[3]	B038	VCCP	A121	A5[3]	B121	A8[3]
A039	DEP3[3]	B039	DEP2[3]	A122	GND	B122	A7[3]
A040	GND	B040	DEP4[3]	A123	A9[3]	B123	VCCL2
A041	DEP5[3]	B041	VCCP	A124	A4[3]	B124	A3[3]
A042	DEP6[3]	B042	DEP7[3]	A125	GND	B125	A6[3]
A043	GND	B043	D62[3]	A126	RESERVED (nc)	B126	VCCL2
A044	D61[3]	B044	VCCP	A127	BNR[3]	B127	AERR[3]
A045	D55[3]	B045	D58[3]	A128	GND	B128	REQ0[3]
A046	GND	B046	D63[3]	A129	BPRI[3]	B129	VCCL2
A047	D60[3]	B047	VCCP	A130	TRDY[3]	B130	REQ1[3]
A048	D53[3]	B048	D56[3]	A131	GND	B131	REQ4[3]
A049	GND	B049	D50[3]	A132	DEFER[3]	B132	VCCL2
A050	D57[3]	B050	VCCP	A133	REQ2[3]	B133	LOCK[3]
A051	D46[3]	B051	D54[3]	A134	GND	B134	DRDY[3]
A052	GND	B052	D59[3]	A135	REQ3[3]	B135	VCCL2
A053	D49[3]	B053	VCCP	A136	HITM[3]	B136	RS0[3]
A054	D51[3]	B054	D48[3]	A137	GND	B137	HIT[3]
A055	GND	B055	D52[3]	A138	DBSY[3]	B138	VCCL2
A056	CPU_SENSE	B056	VCCP	A139	RS1[3]	B139	RS2[3]
A057	GND	B057	L2_SENSE	A140	GND	B140	RP[3]
A058	D42[3]	B058	VCCP	A141	BR2[3]	B141	VCCL2
A059	D45[3]	B059	D41[3]	A142	BR0[3]	B142	BR3[3]
A060	GND	B060	D47[3]	A143	GND	B143	BR1[3]
A061	D39[3]	B061	VCCP	A144	ADS[3]	B144	VCCL2
A062	TEST_25 (pu)[2]	B062	D44[3]	A145	AP0[3]	B145	RSP[3]
A063	GND	B063	D36[3]	A146	GND	B146	AP1[3]
A064	D43[3]	B064	VCCP	A147	VID2_CORE	B147	VCCL2
A065	D37[3]	B065	D40[3]	A148	VID1_CORE	B148	RESERVED (nc)
A066	GND	B066	D34[3]	A149	GND	B149	VID3_CORE
A067	D33[3]	B067	VCCP	A150	VID4_CORE	B150	VCCL2
A068	D35[3]	B068	D38[3]	A151	RESERVED (nc)	B151	VID0_CORE
A069	GND	B069	D32[3]	A152	GND	B152	VID0_L2
A070	D31[3]	B070	VCCP	A153	VID2_L2	B153	VCCL2
A071	D30[3]	B071	D28[3]	A154	VID1_L2	B154	VID4_L2
A072	GND	B072	D29[3]	A155	GND	B155	VID3_L2
A073	D27[3]	B073	VCCP	A156	VTT	B156	VCCL2
A074	D24[3]	B074	D26[3]	A157	VTT	B157	VTT
A075	GND	B075	D25[3]	A158	GND	B158	VTT
A076	D23[3]	B076	VCCP	A159	SA2	B159	VCCL2
A077	D21[3]	B077	D22[3]	A160	VCC3.3	B160	SCLK
A078	GND	B078	D19[3]	A161	GND	B161	SDAT
A079	D16[3]	B079	VCCP	A162	SA1	B162	VCCL2

Pin[1]	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A080	D13[3]	B080	D18[3]	A163	SA0	B163	RESERVED (nc)
A081	GND	B081	D20[3]	A164	GND	B164	RESERVED (nc)
A082	TEST_VTT (pu)	B082	VCCP	A165	PWR_EN0	B165	RESERVED (nc)
A083	RESERVED (nc)	B083	RESERVED (nc)				

Notes:
4. Pins are numbered with respect to the cartridge edge connector. Axx signals appear on the front (processor side) of the processor card. For mechanical specifications, see Section 12.
5. Signals that have no connection except for a pullup resistor to 2.5 volts are labeled with the signal mnemonic followed by "(pu)."
6. Signal is active low.

11.6.2 Processor Termination/Regulation/Power

The termination circuitry required by the Intel Pentium III Xeon processor bus (AGTL+) signaling environment, and the circuitry to set the AGTL+ reference voltage, are implemented directly on the processor cards.

The baseboard provides 1.5V AGTL+ termination power (VTT), and VRM 8.3-compliant DC-to-DC converters to provide processor power (VCCP) at each connector. The baseboard provides three embedded sockets and three VRM sockets to power the processors, which derive power from the +5V and 12V supplies. Each processor has a separate VRM to power its core; however, two processors share a VRM to power their cache. For more information, see the *VRM 8.3 DC-DC Converter Specification.*

11.6.3 Processor Voltage Regulator Module Connectors (J2A2, J2B1, J2C1)

Table 11-8: Add-in VRM Connector Pin Listing

Pin	Signal	Type †	Description
A1	P5VIN1	POWER	
A2	P5VIN2	POWER	
A3	P5VIN3	POWER	
A4	P12VIN1	POWER	
A5	P12VIN3	POWER	
A6	P1SHARE		
A7	VID0	OUT	
A8	VID2	OUT	
A9	VID4	OUT	
A10	VCCP1	POWER	
A11	VSS1	POWER	
A12	VCCP2	POWER	
A13	VSS2	POWER	
A14	VCCP3	POWER	
A15	VSS3	POWER	
A16	VCCP4	POWER	
A17	VSS4	POWER	
A18	VCCP5	POWER	

Pin	Signal	Type †	Description
A19	VSS5	POWER	
A20	VCCP6	POWER	
B1	P5VIN4	POWER	
B2	P5VIN5	POWER	
B3	P5VIN6	POWER	
B4	P12VIN2	POWER	
B5	RES		
B6	OUTEN	OUT	
B7	VID1	OUT	
B8	VID3	OUT	
B9	PWRGOOD		
B10	VSS6	POWER	
B11	VCCP7	POWER	
B12	VSS7	POWER	
B13	VCCP8	POWER	
B14	VSS8	POWER	
B15	VCCP9	POWER	
B16	VSS9	POWER	
B17	VCCP10	POWER	
B18	VSS10	POWER	
B19	VCCP11	POWER	
B20	VSS11	POWER	

11.6.4 Termination Card

Caution: A termination card *must* be installed in any vacant processor card slot to ensure reliable system operation.

The termination card contains AGTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector. The system will not boot unless all slots are occupied with a processor or termination card.

For signal descriptions, see the specific processor EMTS.

11.7 System Management Interfaces

11.7.1 Server Monitor Module Connector (J7H1)

The baseboard supports the Server Monitor Module feature connector. The table below shows the pinout of the 26-pin baseboard connector.

Note: On the SKA4 baseboard, pins 1, 9, 15, and 17 are connected to **SMI_L**, **NMI**, **SECURE_MODE**, and **CHASSIS_INTRUSION**, but these signals are not monitored on any existing or planned SM module.

Table 11-9: Server Monitor Module Connector Pinout

Pin	Signal	Type[1]	Description—SKA4 Implementation
1	SMI_L	out	System Management Interrupt: not supported on SMM
2	I2C_SCL	in	I^2C clock line
3	CONP_L	out	Connector Present: tied to ground on the baseboard
4	Reserved		Reserved pin: NC on baseboard
5	PWR_CNTL_L	in	Power supply on/off control: allows SMM to control system power
6	I2C_SDA	in/out	I^2C serial data line
7	5VSTNDBY	out	+5V standby: monitored by SMM to determine if AC power is applied
8	Reserved		Pulled up to 5V through 10k on baseboard
9	NMI	out	Non-maskable interrupt: not supported on SMM
10	HOST_AUX	out	Baseboard voltage monitored by the remote management card: connected to 3.3 V
11	RESET_L	in	Baseboard reset signal from Server Monitor Module
12	GROUND	ground	Ground
13	GROUND	ground	Ground
14	Key		No connect on baseboard
15	SECURE_MODE	out	Secure mode indication: not supported on SMM
16	GROUND	ground	Ground
17	CHASSIS_INTRUSION	out	Chassis intrusion indication: not supported on SMM
18	Reserved		Reserved pin: NC on baseboard
19	Reserved		Reserved pin: NC on baseboard
20	GROUND	ground	Ground
21	Reserved		Reserved pin: NC on baseboard
22	Reserved		Reserved pin: NC on baseboard
23	Reserved		Reserved pin: NC on baseboard
24	Reserved		Reserved pin: NC on baseboard
25	key		No connect on baseboard
26	Reserved		Reserved pin: NC on baseboard

Note:
1. Type (in/out) is from the perspective of the baseboard.

11.7.2 SM Bus Connector (J9E4)

The SM bus connector allows connection to the Memory board I^2C bus on which the DIMMs EEPROMs reside. See Section 5 for more details on this I^2C bus.

WARNING: A shorted I^2C connection at the SM Bus I^2C connector will prevent the system BIOS from sizing and configuring main memory.

Table 11-10: SMB Connector (J9E4)

Pin	Signal	Description
1	Local I2C SDA	OSB4 SM Bus Data Line
2	GROUND	
3	Local I2C SCL	OSB4 SM Bus Clock Line

11.7.3 ICMB Connector (J1D2)

The external Intelligent Management Bus (ICMB) provides external access to IMB devices that are within the chassis. This makes it possible to externally access chassis management functions, alert logs, post-mortem data, etc. It also provides a mechanism for chassis power control. As an option, the server can be configured with an ICMB adapter board to provide two SEMCONN 6-pin connectors to allow daisy chained cabling. Additional information about ICMB can be found in the *External Intelligent Management Bus Bridge External Program Specification*.

Table 11-11: ICMB Connector Pinout (J1D2)

Pin	Signal	Type	Description
1	SDA	Signal	IPMB I^2C Data
2	Ground	Power	
3	SCL	Signal	IPMB I^2C Clock
4	5 V standby	Power	

11.7.4 Auxiliary I^2C Connector (J9E4)

The baseboard provides a 3-pin auxiliary I^2C connector for OEM access to the IPMB. This connector is not isolated when power is off. Any devices connected must remain powered in this state or the BMC will not work properly.

WARNING: A shorted I^2C connection at the auxiliary I^2C connector will prevent restoration of main power because the BMC needs the bus to boot the server from standby power.

Table 11-12: IMB Connector Pinout (J8F1)

Pin	Signal	Description
1	Local I2C SDA	BMC IMB 5VSTNDBY Clock Line
2	GROUND	
3	Local I2C SCL	BMC IMB 5VSTNDBY Data Line

11.8 Baseboard Fan Connectors (J3C1, J3A1, J4A1, J4C1)

Four fan connectors are on the baseboard. These connectors are to be used for additional processor cooling if needed.

Note: The SKA4 board set supports monitoring a total of eight tachometer fan inputs. The front panel connector provides connections to all eight tachometer fan inputs. The tachometer signals from these four processor fan connectors are connected to the same tachometer fan signals FAN_TACH(4), FAN_TACH(5), FAN_TACH(6), FAN_TACH(7) provided on the front panel connector J9E3. Therefore, care should be taken to ensure only one connection is used at a time.

Table 11-13: Processor Fan Connector #1 (J3C1)

Pin	Signal	Type[1]	Description
1	Ground	power	GROUND is the power supply ground
2	12V	Power	Power Supply 12V
3	Fan Tach	out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

Note:
1. Type (in/out) is from the perspective of the baseboard.

Table 11-14: Processor Fan Connector #2 (J3A1)

Pin	Signal	Type[1]	Description
1	Ground	power	GROUND is the power supply ground
2	12V	Power	Power Supply 12V
3	Fan Tach	out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

Note:
1. Type (in/out) is from the perspective of the baseboard.

Table 11-15: Processor Fan Connector #3 (J4A1)

Pin	Signal	Type[1]	Description
1	Ground	power	GROUND is the power supply ground
2	12V	Power	Power Supply 12V
3	Fan Tach	out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

Note:
1. Type (in/out) is from the perspective of the baseboard.

Table 11-16: Processor Fan Connector #4 (J4C1)

Pin	Signal	Type[1]	Description
1	Ground	power	GROUND is the power supply ground
2	12V	Power	Power Supply 12V
3	Fan Tach	out	FAN_TACH signal is connected to the BMC to monitor the FAN speed

Note:
1. Type (in/out) is from the perspective of the baseboard.

11.9 Internal I/O Bus Connections

11.9.1 Internal Disk Drive LED Connection

This connector allows external drive controllers the ability to blink the front panel disk drive activity LED.

Table 11-17: Internal USB Connector (J1B3)

Pin	Signal	Description

1	NC	No Connect
2	Activity Signal	5V, High True Activity Signal
3	Activity Signal	Same as Pin 2 (Shorted to pin 2)
4	NC	No Connect

11.10 Standard I/O Panel

The following diagram shows the locations of serial, parallel, video, keyboard, and mouse connector interfaces on the system I/O panel, as viewed from the rear of the system.

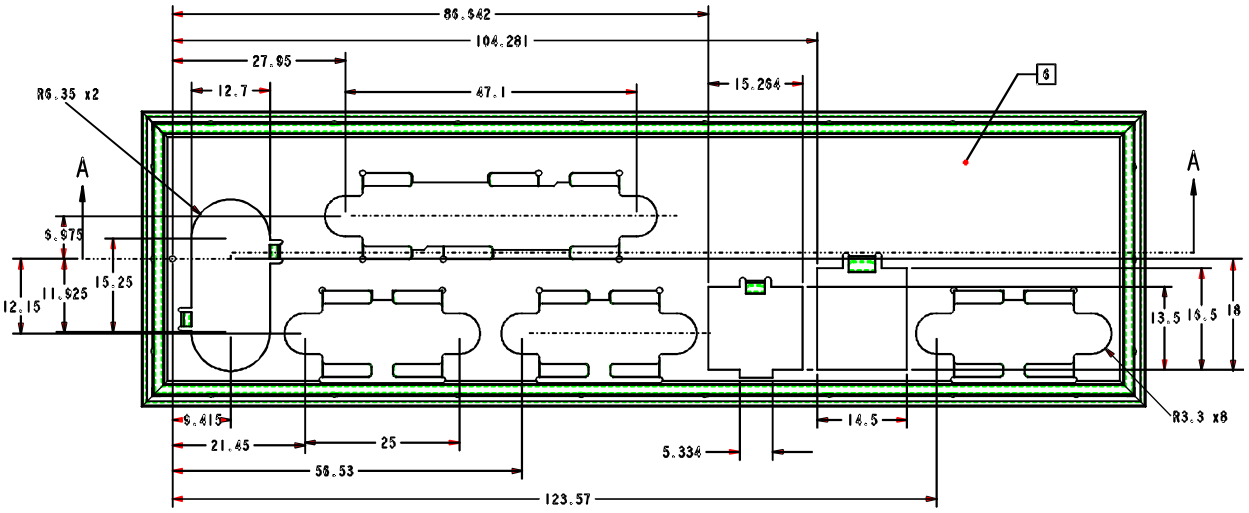

Figure 11-2: SKA4 I/O Panel Connector Location Dimensions

The following diagram shows a graphical representation with identification of the physical connections at the I/O panel.

Figure 11-3: SKA4 I/O Panel Connector Graphical Locations

11.10.1 Universal Serial Bus (USB) Interface

The baseboard provides two stacked USB ports (Port 0 on top, Port 1 on bottom). The built-in USB ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports.

Table 11-18: Dual USB Connector

Pin	Signal
A1	Fused VCC (+5V /w over current monitor of both port 0 and 1)
A2	DATAL0 (Differential data line paired with DATAH0)
A3	DATAH0 (Differential data line paired with DATAL0)
A4	GND
B1	Fused VCC (+5V /w over current monitor of both port 0 and 1)
B2	DATAL1 (Differential data line paired with DATAH1)
B3	DATAH1 (Differential data line paired with DATAL1)
B4	GROUND

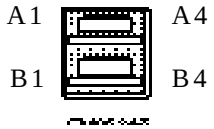

Figure 11-4: Dual USB Connector

11.10.2 Ethernet Connector

The system supports one 10/100Mbps TX-based on-board Ethernet connection.

Table 11-19: Ethernet Connector

Pin	Signal
1	TXP
2	TXM
3	RXP
4	
5	
6	RXM
7	
8	

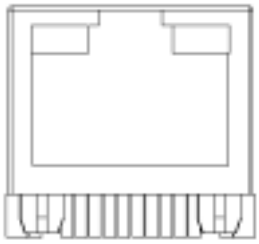

Figure 11-5: Ethernet Connector

The 82559 drives LEDs on the network interface connector that indicate transmit/receive activity on the LAN, a valid link to the LAN, and 10- or 100-Mbps operation. The green LED (left) indicates network connection when on and TX/RX activity when blinking. The yellow LED indicates 100 Mbps operation when lit.

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12. Electrical and Thermal Specifications

This section specifies the operational parameters and physical characteristics for SKA4 server board. This is a board-level specification only. System specifications are beyond the scope of this document.

12.1 Absolute Maximum Electrical and Thermal Ratings

The operation of the SKA4 board set at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 12-1: Absolute Maximum Electrical and Thermal Specifications

Operating Temperature	5°C to +50°C[1]
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V[2]
3.3V supply voltage with respect to ground	-0.3 to +3.63V
5V supply voltage with respect to ground	-0.3 to +5.5V

Notes:
1. Chassis design must provide proper airflow to avoid exceeding Pentium II Xeon processor 100 MHz FSB maximum case temperature.
2. V_{DD} means supply voltage for the device.

The table lists the maximum component case temperatures for base board components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the motherboard.

Caution: An ambient temperature that exceeds the board's maximum operating temperature by 5°C to 10°C might cause components to exceed their maximum case temperature. When determining system compliance, considerations should be given for maximum rated ambient temperatures.

Table 12-2: Thermal Specification for Key Components

Component	Maximum Temperature
Pentium® III Xeon™ 1M & 2M Cache 100 MHz FSB processor	65°C (thermal plate)
CNB20HE	80°C (case)
CIOB	80°C (case)
MADP	90°C (case)
ROSB4	90°C (case)
Lithium battery	70°C (case)

12.2 Airflow Specification for CIOB and HE

- HE Heat Sink:
- Maximum Operating Ambient: 40C
- Minimum Airflow Requirement: 1.5m/s
- CIOB Heat Sink:
- Maximum Operating Ambient: 44C
- Minimum Airflow Requirement: 1m/s

12.3 Electrical Specifications

DC and AC specifications for SKA4 are summarized here.

12.3.1 Power Consumption

The following table shows the power consumed on each supply line for a combined SKA4 server baseboard and memory board. These numbers are for budgetary use and are calculated based on worst case use. These numbers do not include any processors, memory or add-in peripherals or cards.

Note: The three onboard voltage regulators for the primary processor's VCC core and all four processors VCC cache are derived for the 5V rail. These regulators are budgeted at 85% efficiency. Therefore, all power consumed on these pins (P1 VCC core and P1, P2, P3 & P4 VCC cache) will result in a 15% power loss not reflected in the below numbers.

Table 12-3: SKA4 Baseboard and Memory Board Power Consumption

Voltage Rails	3.3V	+5V	+12V	-12V	5V Standby
Maximum Current (A)	12.2A	7A + VRM inefficiency (see note above table)	1.5A	.1A	1.3A

For specific system or configured calculations, add the power consumed by all devices plugged into the board set.

12.3.2 Power Supply Specifications

This section provides power supply design guidelines for the SKA4-based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 12-4: SKA4 Server Power Supply Voltage Specification

Item	Min	Nom	Max	Units	Tolerance
3.3 Volts	3.15	3.30	3.46	V	+/- 5%
5 Volts	4.75	5.00	5.25	V	+/- 5%
+12 Volts	11.40	12.00	12.60	V	+/- 5%
-12 Volts	-11.40	-12.00	-12.60	V	+/- 5%
-5 Volts	-4.75	-5.00	-5.25	V	+/- 5%
5 Volts Standby	+4.75	+5.00	+5.25	V	+/- 5%

12.3.3 Power Timing

Following are the timing requirements for single power supply operation.

The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 200ms. The +3.3V, +5V and +12V output voltages should start to rise approximately at the same time. All outputs must rise monotonically. The +5V output needs to be greater than the +3.3V output during any point of the voltage rise, however, never by more than 2.25V. Each output voltage shall reach regulation within 100ms (T_{vout_on}) of each other and begin to turn off within 100ms (T_{vout_on}) of each other. The table below shows the output voltage timing parameters.

The second table below shows the timing requirements for a single power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied. The ACOK$^{\#}$ signal is not being used to enable the turn on timing of the power supply.

Table 12-5: Voltage Timing Parameters

Item	Description	Min	Max	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	200	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		100	msec

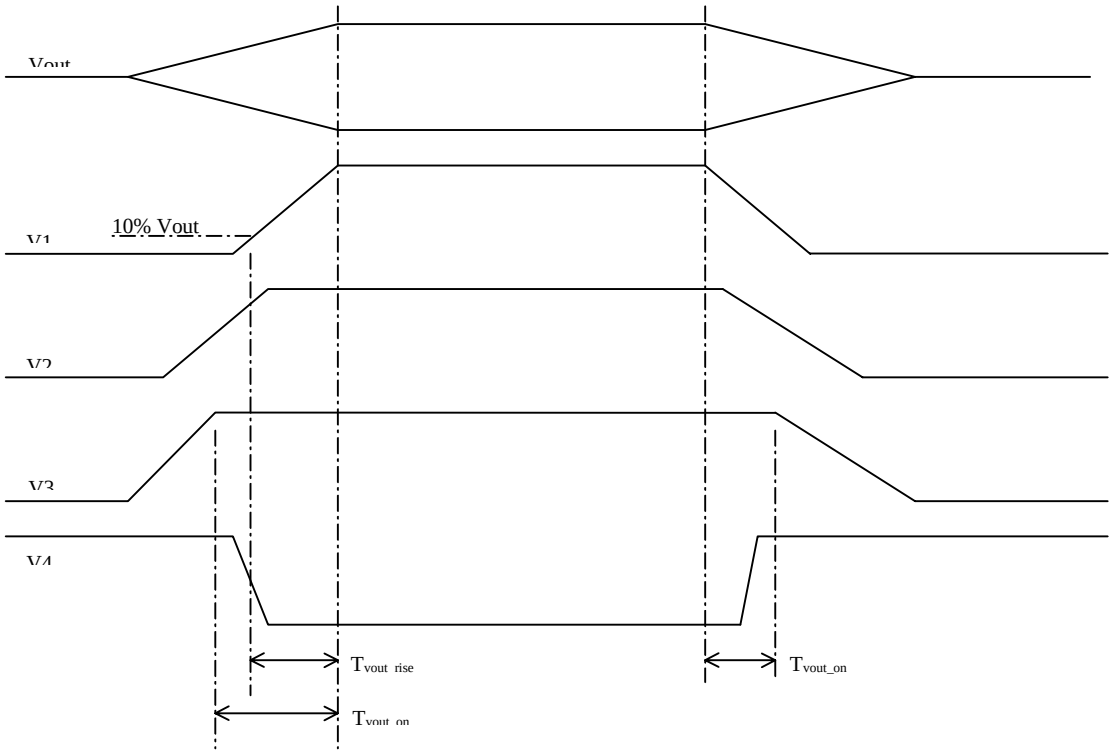


Figure 12-1: Output Voltage Timing

Table 12-6: Turn On/Off Timing

Item	Description	Min	Max	Units
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.			msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	msec
T_{vout_holdup}	Time all output voltages, including 5VSB, stay within regulation after loss of AC.	21		msec
T_{pwok_holdup}	Delay from loss of AC to deassertion of PWOK.	20		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSON# deactive to PWOK being deasserted.		50	msec
T_{acok_delay}	Delay from loss of AC input to deassertion of ACOK#.	20		msec
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T_{pwok_off}	Delay from PWOK deasserted to output voltages (3.3V, 5V, 12V, -12V, 5VSB) dropping out of regulation limits.	1	200	msec
T_{pwok_low}	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON signal.	100		msec

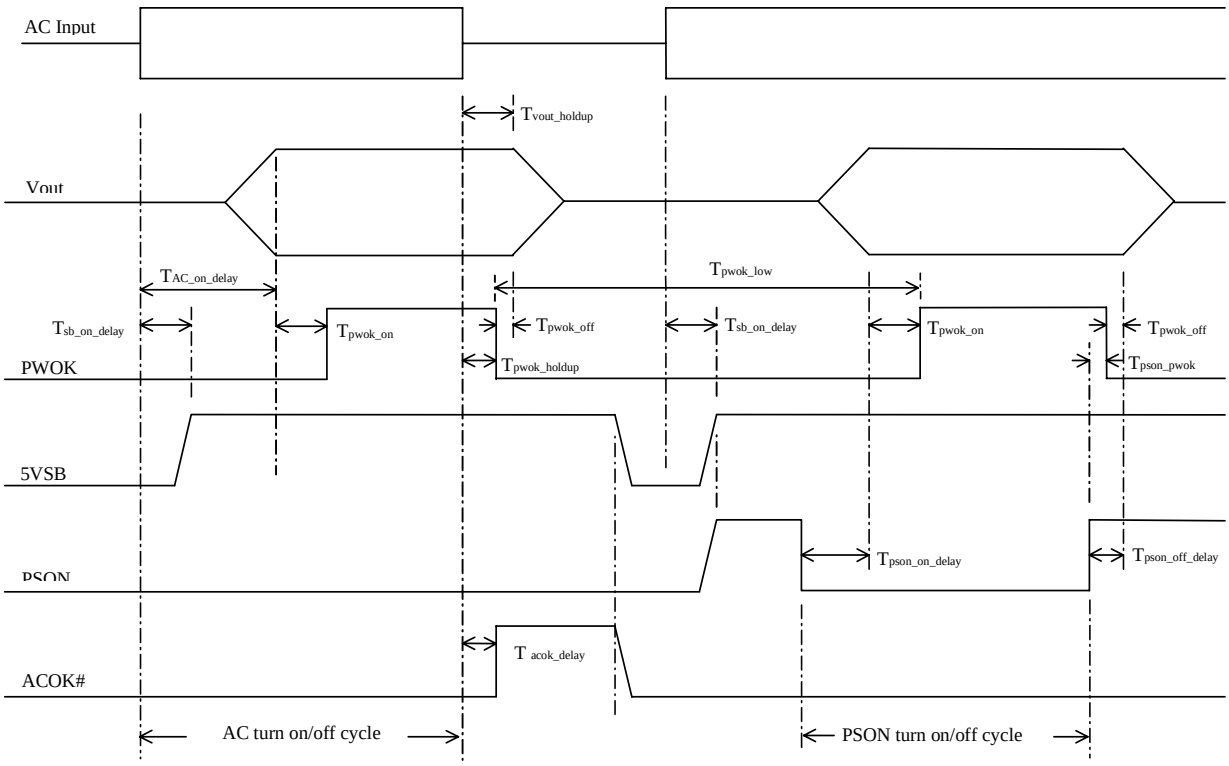


Figure 12-2: Turn On/Off Timing

12.3.4 Voltage Recovery Timing Specifications

The power supply must conform to the following specifications for voltage recovery timing under load changes:

1. Voltage shall remain within +/- 5% of the nominal set voltage on the +5V, +12V, 3.3V, -5V and -12V outputs, during instantaneous changes in load shown in the table below.

2. Voltage regulation limits shall be maintained over the entire AC input range and any steady state temperature and operating conditions specified.

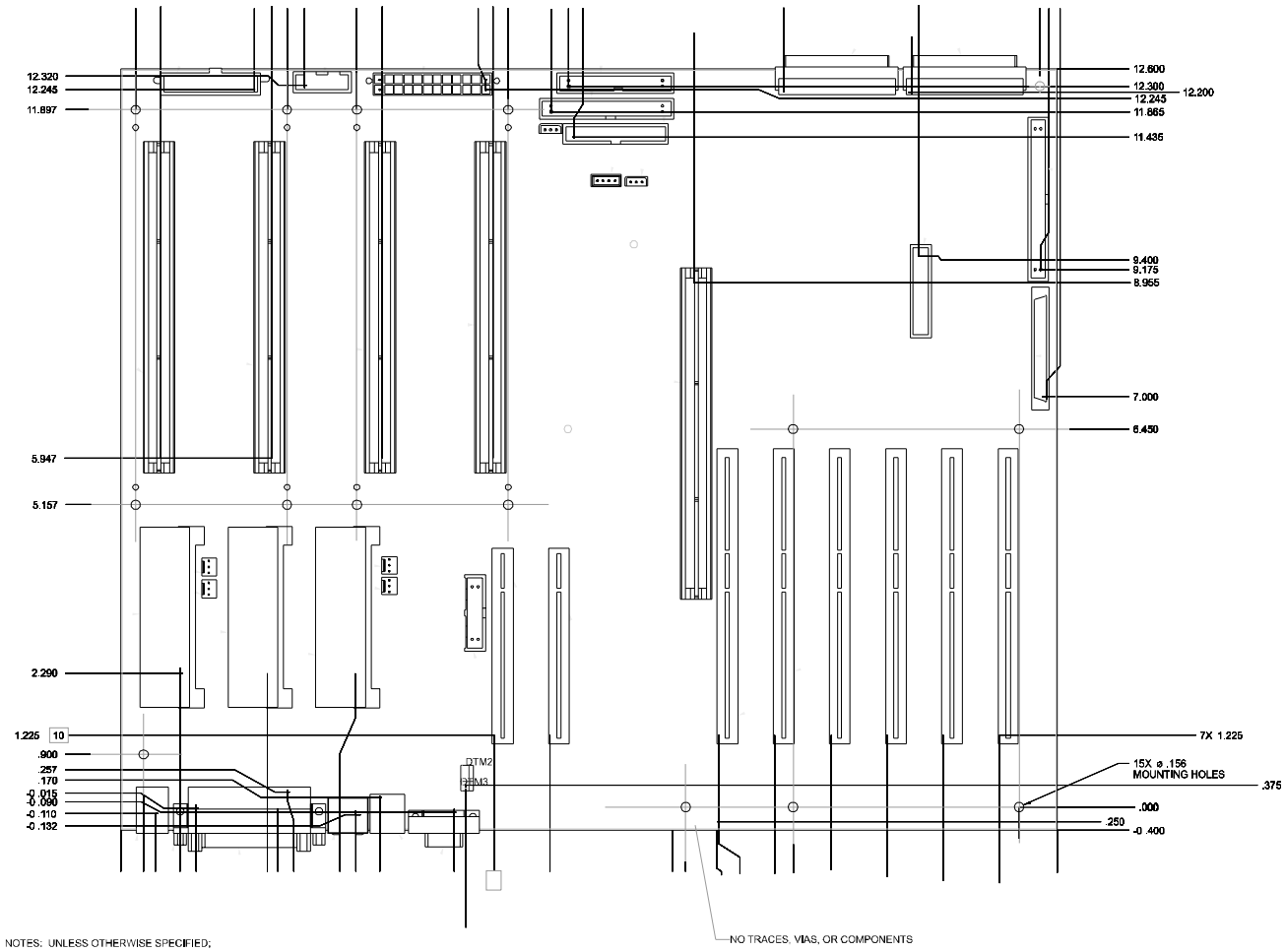
3. Voltages shall be stable as determined by bode plot and transient response. The combined error of peak overshoot, set point, regulation, and undershoot voltage shall be less than or equal to +/-5% of the output voltage setting. The transient response measurements shall be made with a load changing repetition rate of 50Hz to 5kHz. The load slew rate shall not be greater than 0.2A/µs.

Table 12-7: Transient Load Requirements

Output	Step Load Size	Starting Level	Finishing Level	Slew Rate
+3.3V	8.0 A	Min. Load	Min. load + 8.0A and step up to max. load	0.50A/µs
+5V	6.0 A	Min. Load	Min. load + 6.0A and step up to max. load	0.50 A/µs
+12V	7.0A	Min. Load Min. Load	Min. load + 7.0A and step up to max. load	0.50 A/µs
+5VSB	150mA	Min. Load	Min. load + 150mA and step up to max. load	0.1 A/us
-12V	250mA	Min. Load	Min load +250mA and step up to max. load	0.1 A/us

13. Mechanical Specifications

The following diagrams show the mechanical specifications of the SKA4 server baseboard. All dimensions are given in inches, and are dimensioned per ANSI Y15.4M. Connectors are dimensioned to pin 1.

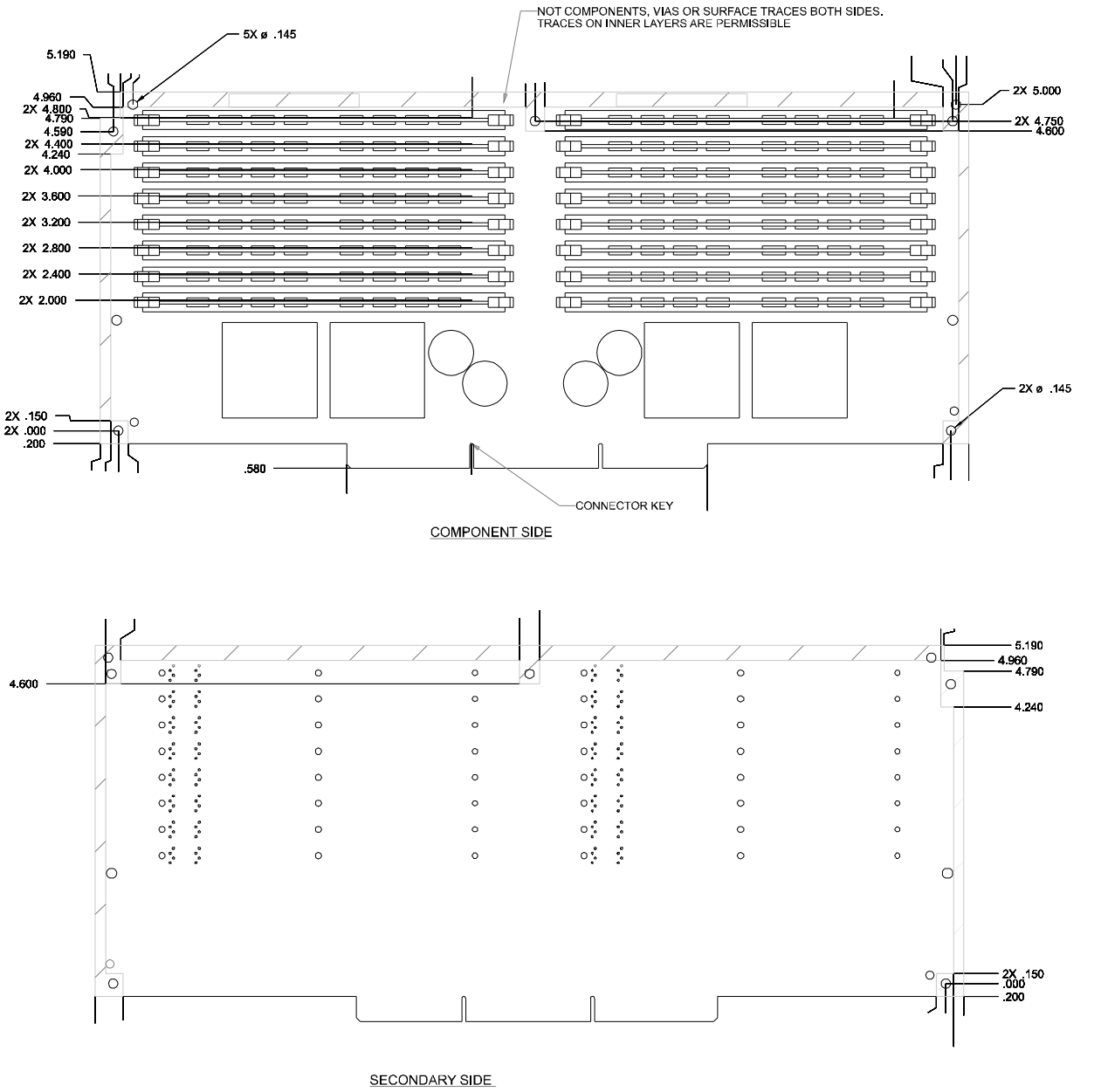


NOTES: UNLESS OTHERWISE SPECIFIED;

1. THIS DOCUMENT DEFINES THE MECHANICAL REQUIREMENTS FOR THE KOA BASEBOARD. ALL DIMENSIONS, UNLESS LISTED AS REFERENCE ARE CRITICAL AND MUST BE ADHERED TO BY BOARD DESIGN TO ENSURE COMPATABILITY WITH THE CHASSIS.
2. PRIMARY SIDE COMPONENT .550 MAXIMUM UNLESS OTHERWISE SPECIFIED.
3. SECONDARY SIDE LEAD PROTRUSION AND COMPONENT HEIGHT .100 MAXIMUM.
4. CONNECTORS ARE DIMENSIONED TO PIN NUMBER 1.
5. ELECTRONIC DATA FILE FOR THIS DOCUMENT EXISTS ON PDMS.
6. TOLERANCES, UNLESS SPECIFIED, PER INTEL PB FAB SPEC 454979.
7. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M.
8. SHADED AREAS ON THE SECONDARY SIDE SHALL BE FREE OF COMPONENTS.
9. SECONDARY SIDE LEAD PROTRUSION AND COMPONENT HEIGHT .100 MAXIMUM.

10 BOARD SECONDARY PLACEMENT DATUM LOCATION FOR PCI CONNECTORS

Figure 13-1: SKA4 Baseboard Mechanical Diagram



NOTES: UNLESS OTHERWISE SPECIFIED:

1. THIS DOCUMENT DEFINES THE MECHANICAL REQUIREMENTS OF THE KOA MEMORY BOARD. ALL DIMENSIONS, UNLESS LISTED AS REFERENCE ARE CRITICAL AND MUST BE ADHERED TO BY BOARD DESIGN TO ENSURE COMPATABILITY WITH CHASSIS.
2. PRIMARY SIDE COMPONENT 1.875 MAXIMUM UNLESS OTHERWISE SPECIFIED.
3. SECONDARY SIDE LEAD PROTRUSION AND COMPONENT HEIGHT .100 MAXIMUM.
5. ELECTRONIC DATE FILE FOR THIS DOCUMENT EXISTS IN PDMS.
4. COMPONENTS ARE DIMENSIONS TO PIN NUMBER 1.
6. TOLERANCE, UNLESS SPECIFIED, PER INTEL PB FAB SPEC 454979.
7. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M.
8. SHADED AREARS ON THE SECONDARY SIDE SHALL BE FREE OF COMPONENTS.
9 SEE INTEL DOCUMENT 695467 FOR BOARD EDGE DETAILS.

Figure 13-2: SKA4 Memory Board Mechanical Diagram

14. Errata

1. **System will not wake after an AC power cycle:** The WOL feature will not work because an AC power cycle clears the PME# enable bit in the PC CFG space 0E0h. DC power cycles will WOL as expected.

2. **IRQ 15 Is Not Available For PCI Devices:** SSU is unable to free IRQ 15 for customer PCI devices. The RCC chipset contains one dual channel IDE controller. SKA4 contains only one IDE connector. Hence, the primary IDE channel is accessible via the server board. The OSB4 component does not provide a "disable" option for the secondary IDE. To be compatible with Windows 2000, IRQ15 must be reserved for the secondary IDE channel even though it is not used.

3. **Unable to Read the SM BIOS information from the SM BIOS Table:** The FRUSDR utility is searching for a _SM _signature starting in the 0E000h segment of memory. The SMBIOS specification indicates the search should occur in the 0F000h segment. The FRUSDR utility locates an _SM_ header in the 0E000h segment and apparently does not perform a checksum operation on the SMBIOS Entry Point Structure before attemping to use it. While there is a *SM* signature in the 0E000h block, the checksum of this structure this structure is not valid and therefore should not be used It is expected the FRUSDR utility to only search the 0f000h segment for the _SM_ header and also perform a checksum of the entry point structure before attempting to use it. This is a FRUSDR utility issue with no fix

4. **If Platform Event Paging, PEP, fans areenabled; The system generates an invalid page on power up.** PEP event is generated when a system is booting up. A SEL event is recorded and this event triggers a PEP event if the fans are selected an event, which will cause a page. There is no fix for this issue.

5. **Processor serial number reporting is turned on by default.** The BIOS Setup option for controlling the reporting of the processor serial number is turned on by default. OEM's can change the default by using the "Custom Defaults " feature This is consistents with documents provided by Intel.

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Appendix A: Glossary

Term	Definition
BMC	Baseboard Management Controller
BSP	Bootstrap Processor
CIOB	PCI 64-bit hub
CNB20HE	Processor CIOB memory interface device, and legacy PCI bridge (P32-C)
FRB	Fault Resilient Booting
HPIB	Hot-plug Indicator Board
IMB	Intra Module Bus
IPMB	Intelligent Platform Management Bus
MADP	Memory Address and Data Path
MEC	Memory Expansion Card
MECC	Memory Expansion Card Connector
MP	Multiprocessor
NIC	Network Interface Card
NMI	Non-maskable Interrupt
OSB4	Legacy I/O controller hub
P32-C	32-bit/33 MHz PCI bus
P32-C1/ P32-C2	32-bit/33-MHz PCI bus add-in connectors
P64-A	64-bit/66-MHz PCI bus segment
P64-A1/ P64-A2	64-bit/66-MHz PCI bus add-in connectors
P64-B	64-bit/33-MHz bus segment
P64-B1/ P64-B2/ P64-B3/ P64-B4	64-bit/33-MHz PCI bus add-in connectors
PBGA	Pin Ball Grid Array
PHP	PCI Hot-plug
PHPC	PCI Hot-plug Controller
POST	Power On Self Test
SEC	Single Edge Contact
SEL	System Event Log
SGRAM	Synchronous Graphics RAM
SHV	Standard High Volume
SM	Server Management
SMM	Server Management Module
TAP	Test Access Port
TBD	To Be Determined
USB	Universal Serial Bus
ZCR	Zero Channel RAID

Appendix B: Reference Documents

Refer to the following documents for additional information:

- *PCI Hot-plug Specification*, Revision 1.0.
- *PCI Local Bus Specification*, Revision 2.1.
- *USB Specification*, Revision 1.0.
- *PCI Bus Power Management Interface Specification*.
- *AIC-7899 PCI-Dual Channel SCSI Multi-function Controller Data Manual*.
- *ATI RAGE IIC Technical Reference Manual*.
- *I^2C Bus Specification*.
- *Intelligent Platform Management Bus Communications Protocol Specification*.
- *Compaq PCI Hot-Plug Megacell Specification*, Draft Copy, Rev. AX. (from Compaq).
- *CK133-WS Synthesizer/Driver Specification*.
- *VRM 8.3 DC-DC Converter Specification*.
- *Adaptec AIC-7899 PCI Bus Master Dual-channel Ultra 160/M SCSI Host Adapter Chip Data Book*.
- *Adaptec AIC-7880 PCI Bus Master Single-chip SCSI Host Adapter Data Book*.
- *ATI-264 VT4 Graphics Controller Technical Reference Manual*.
- *Intel® 82559 Fast Ethernet Multifunction PCI/CardBus Controller Datasheet*.
- *Intelligent Platform Management Interface (IPMI) Specification*.
- *PCI Hot-Plug Application and Design*, Alan Goodrum, ISBN 0-929392-60-4, March 1998.
- *SSI Midrange Power Supply Specification*.

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