Intelligent Chassis Management Bus (ICMB) Bridge Card

Technical Product Specification

Revision 1.0

February 17, 2000

Enterprise Server Group

Revision History

Date	Revision Number	Modifications
2/17/00	1.0	Initial release.

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The Intelligent Chassis Management Bus Bridge Card may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata will be available on request.

I^2C is a two-wire communications bus/protocol developed by Philips. SMBus is a subset of the I^2C bus/protocol and was developed by Intel. Implementations of the I^2C bus/protocol or the SMBus bus/protocol may require licenses from various entities, including Philips Electronics N.V. and North American Philips Corporation.

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1. Introduction

This document establishes the physical size and general requirements for the design and manufacture of the server Intelligent Chassis Management Bus (ICMB) Board.

1.1 Features

- Enables RS485 communication to other ICMB compliant devices.
- Communicates to the baseboard IPMB via a four-conductor pin and socket connector.
- 5V standby powered for offline access.
- 5V Flash for firmware upgrade.

1.2 Goals

- Provide a method to communicate with other devices without using primary power and in a simple manner.
- Meets requirements for Design for Manufacturability (DFM)/Design for Testability (DFT).

1.3 Physical Description

The printed circuit board will have the dimensions, mounting hole placements, and connector placements as shown in the *ICMB Board Mechanical Drawing* document. The board has dimensions of 2.3” x 3.875”.

1.4 Printed Circuit Board

The board must be built per the Intel document *Printed Board Fabrication*. The current densities on the board must be kept low enough to allow no more than a 20°C rise on the PC board traces.

1.5 Physical Environment

The ICMB Bridge Card mounts to a standard PCI card I/O panel opening or to a custom chassis punch out. The I/O panel shield must be replaced with the “punch out” mounting bracket for direct to chassis mounting.

1.5.1 Temperature

Operating Temperature 0°C to 50°C.

Storage Temperature -40°C to 70°C.

2. Interface Descriptions

2.1 Electrical Connections

Interfacing is provided by the following connectors:

- Baseboard goldfingers.
- SEMCONN* connectors.

2.2 Baseboard Connector

Table 1: Baseboard Connector

Pin	Signal
1	VCC_STDBY
2	IMB_5V_SCL
3	GND
4	IMB_5V_SDA

2.3 SEMCONN* Connectors

Table 2: SEMCONN* Connectors

Pin	Signal
1	GND
2	No Connect
3	Tx/Rx +
4	Tx/Rx -
5	No Connect
6	No Connect

Notes:
Pinout conforms to ICMB 1.0 specification. Previous ESG ICMB products have Pin 3 and 4 swapped.

3. Functional Architecture

The basic function of the ICMB Bridge Card is to provide access to chassis information/control by the Intelligent Management Bus Protocol using RS485. Physically it consists of a 652 controller with a 32KB RAM and 32KB Flash and an RS485 driver. This is powered from 5V standby such that a communication channel is available under normal power-down state.

The 652 proxies for an internal I2C bus, ICMBI2C. On this bus is a 256-byte FRU EEPROM at address AA/AB. Potentially there is a temperature sensor at address 90.

The two SEMCONN connectors are used for RS485 communication. Two are used to daisy chain the communications network and are functionally identical.

4. Electrical, Environmental, Mechanical Specifications

4.1 Marking and Identification

4.1.1 Internal System Marking

A label must be on the printed board assembly in the position indicated on the assembly drawing. This label must include the following Intel required information. This information and how it must be shown is detailed in the Marking and Bar Code Labeling specifications.

Intel requirements are:Text showing vendor's name, vendor's part number, vendor's serial number and vendor's lot date code. Also included on this label may be the Intel® part number and revision level along with agency markings.

2. Four bar code marking for Intel part number, vendor code number, date code, and vendor serial number. The shipping container shall also have the Intel part number bar code. The bar code markings for the Intel part number with a space between the vendor code will be contained as one scan input. The bar code markings for the date code with a space between the serial number will be contained as one scan input.

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Appendix A: Glossary

Term	Definition
DFM	Design for Manufacturability
DFT	Design for Testability
ESG	Enterprise Server Group
ICMB	Intelligent Chassis Management Bus

Appendix B: Reference Documents

Refer to the following documents for additional information:

- *Intelligent Platform Management Interface Specification*, Version 1.0, Revision 1.0, Intel Corporation.
- *Intelligent Chassis Management Bus Bridge Specification*, Version1.0, Revision 0.6, Intel Corporation.
- *ICMB Board Mechanical Drawing*, Intel Corporation.