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Table of Contents

| | |
|--|-----------|
| 1. Introduction | 11 |
| 1.1 Audience..... | 11 |
| 2. Server Board SE7500CW2 Overview | 12 |
| 2.1 Feature Set..... | 12 |
| 3. Functional Architecture | 14 |
| 3.1 Processor and Memory Subsystem..... | 14 |
| 3.1.1 Processor Support | 14 |
| 3.1.2 Memory Subsystem | 16 |
| 3.2 Intel E7500 Chipset | 19 |
| 3.2.1 MCH Memory Architecture Overview | 20 |
| 3.2.2 MCH North Bridge..... | 21 |
| 3.2.3 P64H2 | 21 |
| 3.2.4 ICH3-S | 22 |
| 3.3 Super I/O | 24 |
| 3.3.1 Serial Ports..... | 24 |
| 3.3.2 BIOS Flash..... | 25 |
| 4. Included PCI Devices | 26 |
| 4.1 ATA-100 RAID | 26 |
| 4.2 Video Controller..... | 27 |
| 4.3 Network Interface Controller (NIC) | 29 |
| 4.4 Optional SCSI Card | 30 |
| 4.5 Interrupt Routing..... | 30 |
| 4.5.1 Legacy Interrupt Routing..... | 30 |
| 4.5.2 APIC Interrupt Routing | 31 |
| 4.5.3 Serialized IRQ Support | 32 |
| 4.5.4 IRQ Scan for PCIIRQ | 32 |
| 5. Hardware Monitoring | 36 |
| 5.1 LANDesk* Client Manager..... | 38 |
| 6. System BIOS..... | 39 |
| 6.1.1 System Flash ROM Layout | 39 |
| 6.2 System Configuration and Initialization..... | 40 |
| 6.2.1 Memory | 40 |
| 6.2.2 Processors | 42 |

| | | |
|-----------|--|-----------|
| 6.2.3 | Extended System Configuration Data (ESCD), Plug and Play (PnP) | 43 |
| 6.2.4 | Legacy ISA Configuration | 44 |
| 6.2.5 | Automatic Detection of Video Adapters | 44 |
| 6.2.6 | Keyboard / Mouse Configuration..... | 44 |
| 6.2.7 | Floppy Drives | 45 |
| 6.2.8 | Universal Serial Bus (USB)..... | 45 |
| 6.3 | BIOS Supported Server Management Features..... | 46 |
| 6.3.1 | Advanced Configuration and Power Interface (ACPI)..... | 46 |
| 6.3.2 | Wake Events | 47 |
| 6.3.3 | Wired For Management (WFM) | 49 |
| 6.3.4 | Console Redirection..... | 50 |
| 6.3.5 | Serial Ports..... | 53 |
| 6.3.6 | System Management BIOS (SMBIOS) | 53 |
| 6.3.7 | Windows Compatibility | 54 |
| 6.4 | BIOS Serviceability Features | 55 |
| 6.4.1 | Flash Update Utility | 56 |
| 6.5 | BIOS and BIOS Setup | 58 |
| 6.5.1 | BIOS Setup Utility | 58 |
| 6.5.2 | Entering the BIOS Setup Utility | 59 |
| 6.5.3 | Keyboard Command Bar..... | 59 |
| 6.5.4 | Menu Selection Bar..... | 61 |
| 6.5.5 | Main Menu | 62 |
| 6.5.6 | Advanced Menu | 64 |
| 6.5.7 | Security Menu | 74 |
| 6.5.8 | Power Menu | 75 |
| 6.5.9 | Boot Menu..... | 76 |
| 6.5.10 | System Menu..... | 77 |
| 6.5.11 | Exit Menu..... | 78 |
| 6.6 | BIOS Security Features | 79 |
| 6.6.1 | Operating Model..... | 79 |
| 6.6.2 | Password Protection | 79 |
| 7. | Error Reporting and Handling | 81 |
| 7.1 | POST Codes, Error Messages, and Error Codes..... | 81 |
| 7.1.1 | Port 80 Codes | 81 |
| 7.1.2 | BIOS POST Beep Codes | 86 |

| | | |
|------------|---|------------|
| 7.1.3 | BIOS Recovery Beep Codes..... | 88 |
| 7.1.4 | POST Error Codes and Messages..... | 88 |
| 7.1.5 | Memory Error Codes..... | 91 |
| 8. | Connectors and Jumper Blocks | 92 |
| 8.1 | Main Power Connector | 92 |
| 8.2 | Memory Module Connector | 93 |
| 8.3 | Processor Heat Syncs | 94 |
| 8.4 | Processor Socket..... | 94 |
| 8.5 | System Management Headers | 96 |
| 8.5.1 | I ² C Header..... | 96 |
| 8.6 | PCI Slot Connector | 97 |
| 8.7 | Front Panel Connectors..... | 99 |
| 8.8 | VGA Connector..... | 100 |
| 8.9 | NIC Connectors | 100 |
| 8.10 | ATA Connectors | 101 |
| 8.11 | USB Connector..... | 102 |
| 8.12 | Floppy Connector | 103 |
| 8.13 | Serial Port Connectors | 104 |
| 8.14 | Keyboard and Mouse Connector..... | 105 |
| 8.15 | Miscellaneous Headers and Jumpers | 106 |
| 8.15.1 | Fan Headers..... | 106 |
| 8.15.2 | System Recovery and Update Jumpers | 106 |
| 9. | General Specifications..... | 108 |
| 9.1 | Absolute Maximum Ratings | 108 |
| 9.2 | Power Budget | 108 |
| 9.3 | Mean Time Between Failures (MTBF) Test Results..... | 110 |
| 9.4 | Power Supply Constraints | 110 |
| 9.4.1 | Server Chassis SC5200 Timing Requirements with the ICH3-S | 110 |
| 9.4.2 | BIOS <F2> “Stay off” Switch Limitations..... | 110 |
| 9.5 | Power Supply Specifications | 110 |
| 9.5.1 | Power Timing | 111 |
| 9.5.2 | Voltage Recovery Timing Specifications..... | 113 |
| 9.6 | Shock and Vibe Test Results..... | 113 |
| 10. | Product Regulatory Compliance..... | 114 |
| 10.1.1 | Product Safety Compliance | 114 |

| | | |
|------------|--|------------|
| 10.1.2 | Product EMC Compliance | 114 |
| 10.1.3 | Product Regulatory Compliance Markings | 114 |
| 10.2 | Electromagnetic Compatibility Notices | 115 |
| 10.2.1 | Europe (CE Declaration of Conformity) | 115 |
| 10.2.2 | Australian Communications Authority (ACA) (C-Tick Declaration of Conformity) | 115 |
| 10.2.3 | Ministry of Economic Development (New Zealand) Declaration of Conformity | 115 |
| 10.2.4 | BSMI (Taiwan)..... | 115 |
| 10.3 | Replacing the Back-Up Battery | 116 |
| 11. | Mechanical Specifications..... | 117 |
| 11.1 | Mechanical Specifications | 117 |
| | Appendix A: SE7500CW2 Integration and Usage Tips | 119 |
| | Appendix B: Errata | 120 |
| | Glossary..... | 129 |
| | Reference Documents | 132 |

List of Tables

| | |
|--|----|
| Table 1. Intel Server Board SE7500CW2 Processor Support Matrix..... | 14 |
| Table 2. Memory Bank Labels | 18 |
| Table 3. Supported DDRs..... | 20 |
| Table 4. ATA-100 RAID Level..... | 26 |
| Table 5. Video Modes | 28 |
| Table 6. Optional Intel® 53C1000B1 SCSI card pin-out(J1)..... | 30 |
| Table 7. PCI Interrupt Routing/Sharing..... | 31 |
| Table 8. Interrupt Definitions..... | 31 |
| Table 9. Monitored Components..... | 36 |
| Table 10: Allowed Combinations of Floppy Drive and Floppy Media..... | 45 |
| Table 11: Supported Wake Events | 47 |
| Table 12: Non-ASCII Key Mappings | 51 |
| Table 13: ASCII Key Mappings..... | 52 |
| Table 14: SMBIOS Header Structure..... | 53 |
| Table 15: Setup Utility Screen | 59 |
| Table 16: Keyboard Commands | 60 |
| Table 17: Menu Selection Bar..... | 61 |
| Table 18: Main Menu | 62 |
| Table 19: Primary/Secondary, Master/Slave Submenu | 63 |
| Table 20: Advanced Menu | 64 |
| Table 21: I/O Device Configuration Submenu | 66 |
| Table 22: On Board Device Submenu | 68 |
| Table 23: PCI Configuration Submenu | 69 |
| Table 24. Option ROM Scan Submenu | 70 |
| Table 25: Server Menu Submenu | 70 |
| Table 26: Console Redirection Submenu | 71 |
| Table 27: Event Logging Submenu..... | 72 |
| Table 28: Hardware Monitor Submenu | 73 |
| Table 29: Security Menu | 74 |
| Table 30: Power Menu..... | 75 |
| Table 31: Boot Menu..... | 76 |
| Table 32: System Menu | 77 |
| Table 33: Exit Menu | 78 |

| | |
|--|-----|
| Table 34: Security Features Operating Model | 79 |
| Table 35: System ROM BIOS POST task point..... | 81 |
| Table 36: Crisis Disk Boot Block BIOS POST Task Point | 86 |
| Table 37: POST Error Beep Codes | 87 |
| Table 38. BIOS Recovery Beep Codes | 88 |
| Table 39: Post Error Message | 88 |
| Table 40: Memory Error Codes..... | 91 |
| Table 41. Power Connector (J26)..... | 92 |
| Table 42. Auxiliary Signal Connector (J24)..... | 92 |
| Table 43. Auxiliary CPU Power Connector (J20)..... | 92 |
| Table 44. DIMM Connectors (J37, J38, J39, J40) | 93 |
| Table 45: Processor Heat Sync data – replacement information..... | 94 |
| Table 46. Socket 604 Processor Socket..... | 94 |
| Table 47. SCSI HDD Header (J25)..... | 96 |
| Table 48. P32-A 5V 32-bit/33 MHz PCI Slot..... | 97 |
| Table 49. P64-B/P64-C 3.3V 64-bit/ 100MHz/133MHz PCI-X Slot..... | 97 |
| Table 50. Front Panel 34-Pin Header (J3)..... | 99 |
| Table 51. VGA Connector (J42)..... | 100 |
| Table 52. RJ-45 Connector (J47)..... | 100 |
| Table 53. ATA-100 40-pin Connectors (J4, J5, J6, J7)..... | 101 |
| Table 54. USB Connectors (J43)..... | 102 |
| Table 55. Optional USB Connection Header (J11)..... | 102 |
| Table 56. Legacy 34-pin Floppy Connector (J10)..... | 103 |
| Table 57. External DB9 Serial 1 Port (J44)..... | 104 |
| Table 58. 9-pin Header Serial 2 Port (J28) | 104 |
| Table 59. Keyboard and Mouse PS/2 Connector (J46) | 105 |
| Table 60. Three-pin Fan Headers (J1, J2, J15, J16, J29, J30)..... | 106 |
| Table 61. Configuration Jumper Options | 107 |
| Table 62. Absolute Maximum Ratings | 108 |
| Table 63. Power Budget | 109 |
| Table 64. SE7500CW2 Static Power Supply Voltage Specification | 110 |
| Table 65. SE7500CW2 Dynamic Power Supply Voltage Specification | 111 |
| Table 66. Voltage Timing Parameters | 112 |
| Table 67. Turn On / Off Timing | 112 |
| Table 68. Transient Load Requirements..... | 113 |

| | |
|---|-----|
| Table 69. Server Board Connector Specifications | 118 |
| Table 70. Errata Summary | 120 |

List of Figures

| | |
|---|-----|
| Figure 1. Server Board Block Diagram | 13 |
| Figure 2. Memory Sub-system Block Diagram..... | 16 |
| Figure 3. Memory Bank Label Definition | 18 |
| Figure 4. ATA-100 RAID Level | 27 |
| Figure 5. Interrupt Routing Diagram (ICH3-S Internal) | 33 |
| Figure 6. Interrupt Routing Diagram | 34 |
| Figure 7. PCI Interrupt Mapping Diagram | 35 |
| Figure 8. Hardware Monitoring | 37 |
| Figure 9. Configuration Jumpers (J106) | 106 |
| Figure 10. Output Voltage Timing | 111 |
| Figure 11. Turn on / off Timing..... | 112 |
| Figure 12. Mechanical Drawing | 117 |

1. Introduction

The Server Board SE7500CW2 Technical Product Specification (TPS) provides a high level technical description for the Intel® Server Board SE7500CW2. It details the architecture and feature set for all functional sub-systems that make up the server board.

This document is divided into the following main categories:

Chapter 2: Server Board SE7500CW2 Overview

Chapter 3: Functional Architecture

Chapter 4: Included PCI Devices

Chapter 5: Hardware Monitoring

Chapter 6: System BIOS

Chapter 7: Error Handling and Reporting

Chapter 8: SE7500CW2 Connectors and Jumper Blocks

Chapter 9: General Specifications

Chapter 10: Product Regulatory Compliance

Chapter 11: Mechanical Specifications

1.1 Audience

This document is for technical personnel who want a technical overview of the Server Board SE7500CW2. Familiarity with the personal computer, Intel server architecture, Intel processor architecture, memory technologies and the Peripheral Component Interconnect (PCI) local bus architecture is assumed.

2. Server Board SE7500CW2 Overview

The Server Board SE7500CW2 is a monolithic printed circuit board with features that were designed to support the general-purpose server market. The architecture is based around the Intel® E7500 chipset and is capable of supporting one or two Intel® Xeon™ processors with 512k L2 cache and up to 4GB¹ of memory.

2.1 Feature Set

The Server Board SE7500CW2 supports the following feature set:

- Dual Intel Xeon processors using the 603-pin INT mPGA package.
- 400 MHz Front Side Bus
- Intel E7500 server chipset
 - MCH memory controller
 - P64H2 64-bit I/O hub
 - ICH3-S I/O controller
 - FWH Firmware Hub
- Support for up to four DDR200 or DDR266 compliant ECC DDR DIMMs providing up to 4GB¹ of memory support.
- Three separate and independent PCI buses:
 - Segment A: 32-bit, 33 MHz, 5 V (P32-A) with four embedded devices:
 - 2D/3D graphics controller: ATI Rage* XL with 8 MB of SDRAM
 - Two Intel® 10/100 82550PM Fast Ethernet Controllers
 - ATA-100 RAID controller: Promise Technology* PDC20267
 - Two PCI slots capable of supporting full length PCI add-in cards
 - Segment B: PCI-X 64-bit, 66MHz, 3.3 V, (P64-B) with the following configuration:
 - Two PCI slots capable of supporting full length PCI add-in cards
 - Segment C: PCI-X 64-bit, 133 MHz, 3.3 V (P64-C) with the following device:
 - One PCI slot capable of supporting full length PCI add-in cards
- LPC (Low Pin Count) bus segment with two embedded devices:
 - Super I/O controller chip providing all PC-compatible I/O (floppy, serial, keyboard, mouse) as well as integrated hardware monitoring.
 - Flash ROM device for system BIOS: Intel® 8Mbit N82802AC Flash ROM.
- Three external Universal Serial Bus (USB) ports with an additional internal header providing one optional USB ports for front panel support.
- Two IDE connectors, supporting up to four ATA-100 compatible devices
- Support for up to four system fans and two processor fans.
- SSI-compliant connectors for SSI interface support: front panel and power connectors.

¹ As of the writing of this document, testing with 2GB DIMM modules was not complete and therefore not yet supported. 2GB DIMM support would allow for up to 8GB of main memory. For updates on support of 2GB DIMM modules, see <http://support.intel.com/support/motherboards/server/se7500cw2>.

The figure below shows the functional blocks of the server board and the plug-in modules that it supports.

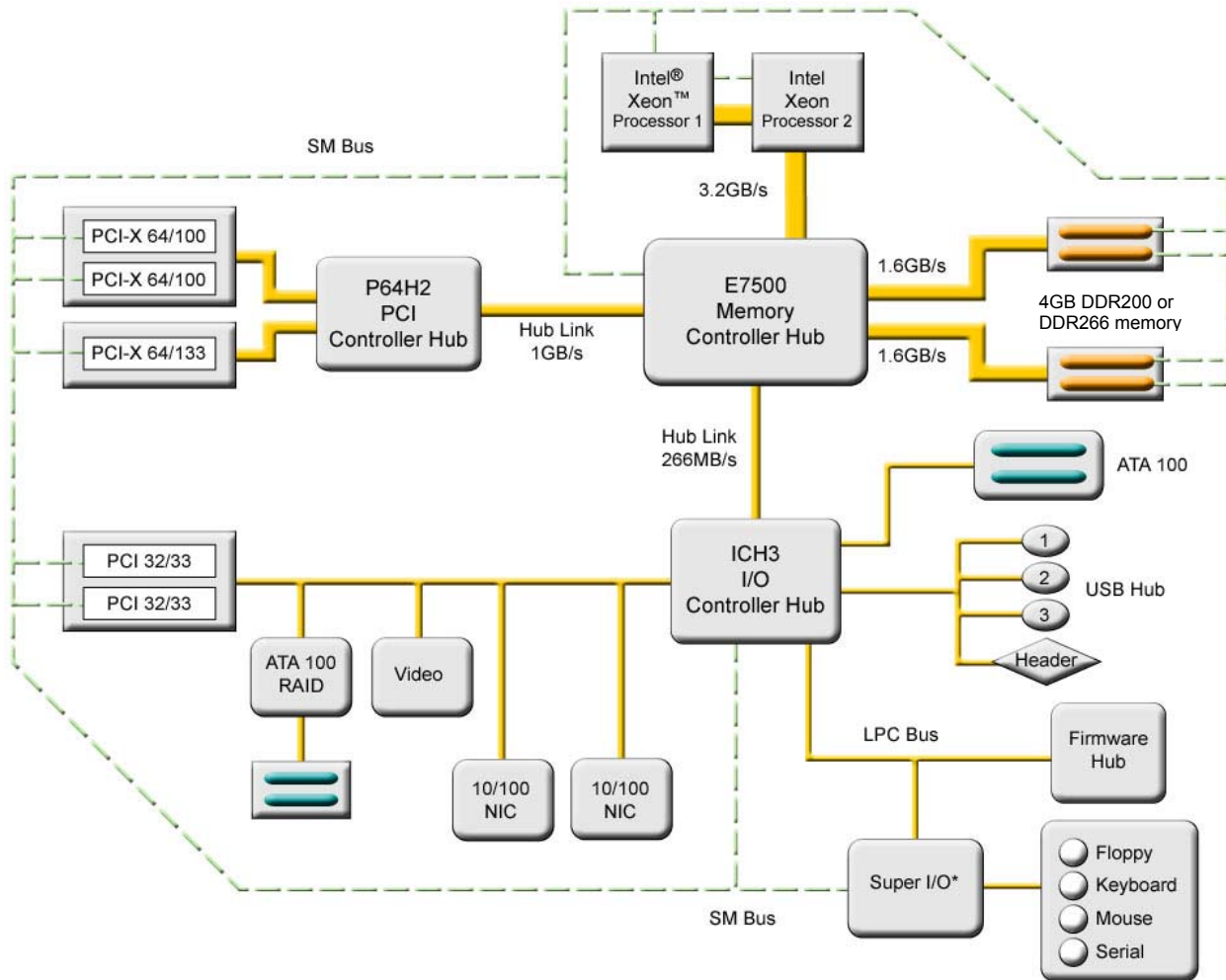


Figure 1. Server Board Block Diagram

3. Functional Architecture

This chapter provides a high-level description of the functionality distributed between the architectural blocks of the Intel Server Board SE7500CW2.

3.1 Processor and Memory Subsystem

The Intel® E7500 Chipset provides a 36-bit address, 64-bit data processor host bus interface, operating at 400MHz in the AGTL+ signaling environment. The MCH component of the chipset provides an integrated memory controller, an 8-bit Hub Interface, and three 16-bit hub interfaces.

The Hub Interface provides the interface to two 64-bit, 133/100/66/33-MHz, Rev 2.2 compliant PCI-X bus via the P64H2. The Intel® Server Board SE7500CW2 directly supports up to 4GB¹ of ECC memory, using four DDR200 or DDR266 compliant ECC DIMMs. The ECC implementation in the MCH can detect and correct single-bit errors, and it can detect multiple-bit errors, and supports 'Chip Kill' feature with DIMMs using x4 technology not x8.

3.1.1 Processor Support

The Intel® Server Board SE7500CW2 supports one or two Intel Xeon processors in the Socket604 FCPGA2 package. When two processors are installed, all processors must be of identical revision, core voltage, and bus/core speed. When only one processor is installed, it should be in the socket labeled CPU1 and the other socket must be empty. The support circuitry on the server board consists of the following:

- Dual 604-pin processor sockets supporting 400 MHz FSB.
- Processor host bus AGTL+ support circuitry.

Table 1. Intel Server Board SE7500CW2 Processor Support Matrix

| <i>Processor Family</i> | <i>Package Type</i> | <i>Frequency</i> | <i>Cache Size</i> | <i>Support</i> |
|-------------------------|---------------------|------------------|-------------------|----------------|
| Intel® Xeon™ | FCPGA | 1.8GHz | 512KB | Yes |
| Intel Xeon | FCPGA | 2.0GHz | 512KB | Yes |
| Intel Xeon | FCPGA | 2.2GHz | 512KB | Yes |
| Intel Xeon | FCPGA | 2.4GHz | 512KB | Yes |

Notes:

- Processors must be populated in the sequential order. That is, processor socket #1 must be populated before processor socket #2.
- The Server Board SE7500CW2 is designed to provide up to 65A per processors. Processors with higher current requirements are not supported.

¹ As of the writing of this document, testing with 2GB DIMM modules was not complete and therefore not yet supported. 2GB DIMM support would allow for up to 8GB of main memory. For updates on support of 2GB DIMM modules, see <http://support.intel.com/support/motherboards/server/se7500cw2>.

In addition to the circuitry described above, the processor subsystem contains the following:

- Reset configuration logic.
- Processor module presence detection logic.
- APIC bus.
- Server monitoring registers and sensors.

3.1.1.1 Processor VRD

The Server Board SE7500CW2 has a single VRD (Voltage Regulator Down) to support two processors. It is compliant with the VRM 9.1 specification and provides a maximum of 130 AMPs, which is capable of supporting current supported processors as well as those supported in the future.

The board hardware and PMC must read the processor VID (voltage identification) bits for each processor before turning on the VRD. If the VIDs of the two processors are not identical, then the PMC will not turn on the VRD and a beep code is generated.

3.1.1.2 Reset Configuration Logic

The BIOS determines the processor stepping, cache size, etc through the CPUID instruction. The requirements are as follows:

- All processors in the system must operate at the same frequency, have the same cache sizes, and same VID. No mixing of product families is supported.
- Processors run at a fixed speed and cannot be programmed to operate at a lower or higher speed.

Note: The processor speed is the processor power on reset default value.

The processor information is read at every system power-on.

Note: No manual processor speed setting options exist either in the form of a BIOS setup option or jumpers.

3.1.1.3 Processor Module Presence Detection

Logic is provided on the baseboard to detect the presence and identity of installed processors. The PMC checks the logic and will not turn on the system DC power unless the VIDs of both the processors match in a DP configuration.

3.1.1.4 Interrupts and APIC

Interrupt generation and notification to the processors is done by the APICs in the ICH3 and the P64H2 using messages on the front side bus.

3.1.2 Memory Subsystem

The Intel® Server Board SE7500CW2 supports up to four DIMM slots for a maximum memory capacity of 4GB¹. The DIMM organization is x72, which includes eight ECC check bits. The memory interface runs at 200MT/s. The memory controller supports memory scrubbing, single-bit error correction and multiple-bit error detection and chip kill support with DIMMS built on x4 technology. Memory can be implemented with either single sided (one row) or double-sided (two row) DIMMs.

The figure below provides a block diagram of the memory sub-system implemented on the Intel® Server Board SE7500CW2.

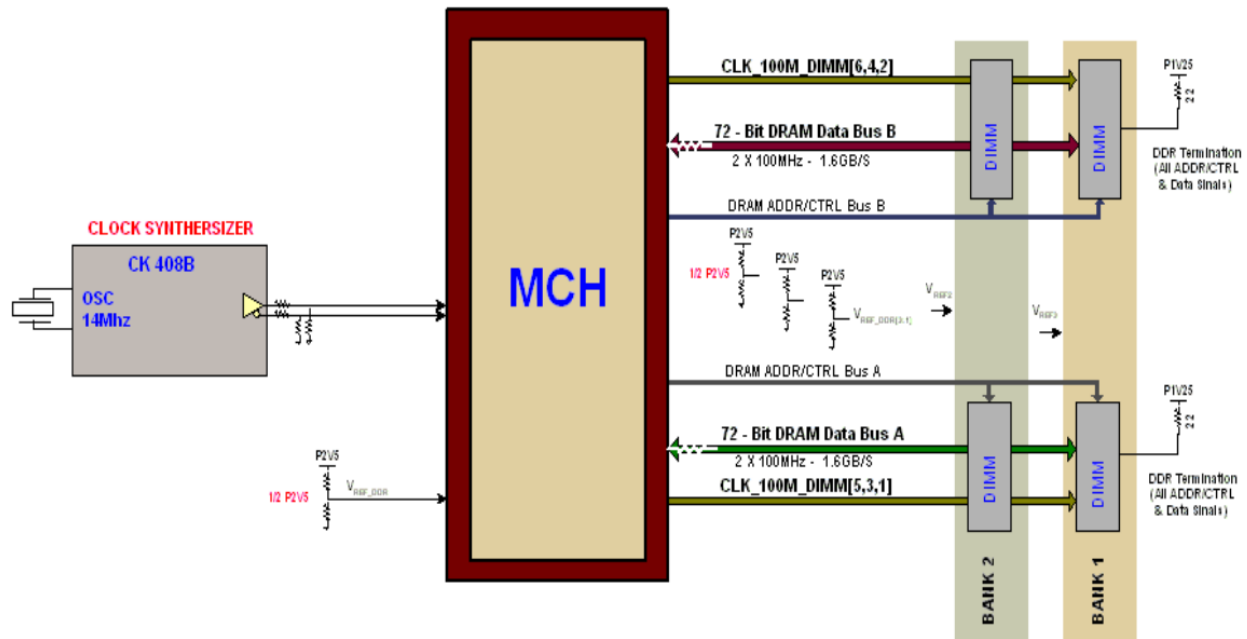


Figure 2. Memory Sub-system Block Diagram

¹As of the writing of this document, testing with 2GB DIMM modules was not complete and therefore not yet supported. 2GB DIMM support would allow for up to 8GB of main memory. For updates on support of 2GB DIMM modules, see <http://support.intel.com/support/motherboards/server/se7500cw2>.

3.1.2.1 Memory DIMM Support

The Server Board SE7500CW2 supports DDR200 compliant registered ECC DIMMs and DDR266 compliant ECC DIMMS operating at 200MT/s. Only DIMMs tested and qualified by Intel or a designated memory test vendor are supported on the Server Board SE7500CW2. A list of qualified DIMMs will be made available. Note that all DIMMs are supported by design, but only fully qualified DIMMs will be supported.

The minimum supported DIMM size is 128 MB. Therefore, the minimum main memory configuration is 2 x 128 MB or 256 MB. The largest size DIMM supported is a 2GB¹ registered DDR200 or DDR266 ECC DIMM based on 512-megabit technology.

- Only registered DDR200 or DDR266 compliant, ECC, DDR memory 2 will be supported
- ECC single-bit errors will be corrected and multiple-bit error will be detected. The Server Board SE7500CW2 also supports Intel® x4 Single Device Data Correction feature with x4 DIMMs.
- The maximum memory capacity is 8 GB
- The minimum memory capacity is 256MB

3.1.2.2 Memory Configuration

Memory interface between the MCH and DIMMs is 144 bit wide. This requires that two DIMMs be populated per bank in order for the system to operate. At least one bank has to be populated in order for the system to boot. If additional banks have less than two DIMMs, the memory for that bank(s) will not be available to the system.

There are two banks of DIMMs, labeled 1 and 2. Bank 1 contains DIMM locations 1A and 1B and bank 2 contains 2A and 2B. DIMM socket identifiers are marked with silkscreen next to each DIMM socket on the baseboard. Note that the sockets associated with any given bank are located next to each other.

The baseboard's signal integrity and cooling are optimized when memory banks are populated in order. Therefore, bank one must be populated before bank two.

DIMM and memory configurations must adhere to the following::

- DDR200 or DDR266 ECC, registered, DDR DIMM modules
- DIMM organization: x72 ECC
- Pin count: 184
- DIMM capacity: 128 MB, 256 MB, 512 MB, 1 GB, and 2 GB DIMMs
- Serial PD: JEDEC Rev 2.0
- Voltage options: 2.5V (VDD/VDDQ)
- Interface: SSTL2
- Two DIMMs must be populated in a bank for a 144-bit wide memory data path.
- Any or all memory banks may be populated

¹ As of the writing of this document, testing with 2GB DIMM modules was not complete and therefore not yet supported. 2GB DIMM support would allow for up to 8GB of main memory. For updates on support of 2GB DIMM modules, see <http://support.intel.com/support/motherboards/server/se7500cw2>.

Table 2. Memory Bank Labels

| Memory DIMM | Bank |
|------------------------------|------|
| J39 (DIMM 1B), J40 (DIMM 1A) | 1 |
| J37 (DIMM 2B), J38 (DIMM 2A) | 2 |

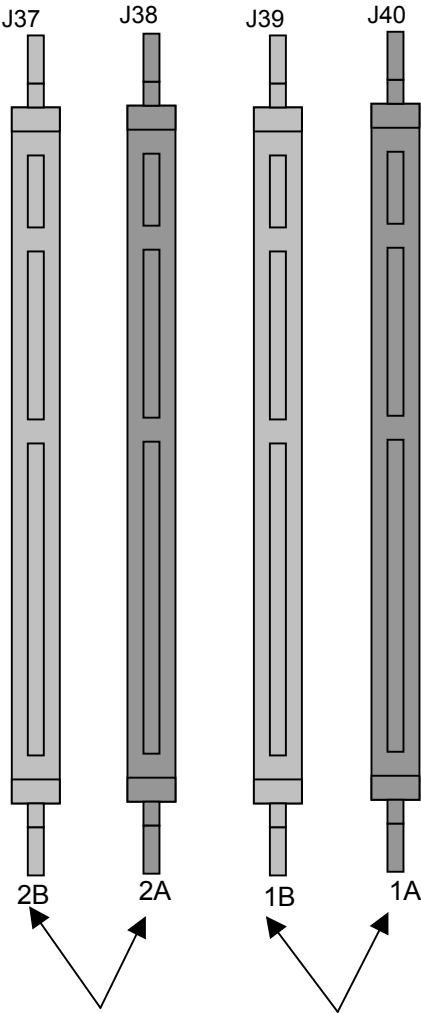


Figure 3. Memory Bank Label Definition

3.1.2.3 I²C Bus

The I²C bus is used by the system BIOS to retrieve DIMM information needed to program the MCH memory registers which are required to boot the system.

3.1.2.4 DRAM ECC

The ECC used for DRAM provides Intel® x4 Single Device Data Correction technology protection for x4 SDRAM modules. DRAM modules that are x8 use the same algorithm but will not have Intel® x4 Single Device Data Correction technology protection, since at most only four bits can be corrected with this ECC.

3.2 Intel E7500 Chipset

The Server Board SE7500CW2 is designed around the Intel E7500 chipset. The chipset provides an integrated I/O bridge and memory controller, and a flexible I/O subsystem core (PCI-X). This is targeted for multiprocessor systems and standard high-volume servers. The Intel E7500 chipset consists of three components:

- **MCH: Memory Control Hub North Bridge.** The MCH North Bridge accepts access requests from the host (processor) bus and directs those accesses to memory or to one of the PCI buses. The MCH monitors the host bus, examining addresses for each request. Accesses may be directed to a memory request queue for subsequent forwarding to the memory subsystem, or to an outbound request queue for subsequent forwarding to one of the PCI buses. The MCH also accepts inbound requests from the P64H2 and the ICH3-S. The MCH is responsible for generating the appropriate controls to control data transfer to and from memory.
- **P64H2: PCI-X 64bit Hub 2.0 I/O Bridge.** The P64H2 provides the interface for two 64-bit, 133-MHz Rev. 2.2 compliant PCI-X buses (implemented on Intel® Server Board SE7500CW2 as one bus with one 64-bit, 133MHz slot and one bus with two 64-bit, 100MHz slots). The P64H2 is both master and target on both PCI-X buses.
- **ICH3-S: IO Control Hub South Bridge.** The ICH3-S controller has several components. It provides the interface for a 32-bit, 33-MHz Rev. 2.2-compliant PCI bus. The ICH3-S can be both a master and a target on that PCI bus. The ICH3-S also includes a USB controller and an IDE controller. The ICH3-S is also responsible for much of the power management functions, with ACPI control registers built in. The ICH3-S also provides a number of GPIO pins and has the LPC bus to support low speed legacy I/O.

The MCH, P64H2, and ICH3-S chips provide the pathway between processor and I/O systems. The MCH is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to one of the PCI buses or legacy I/O locations. If the cycle is directed to one of the 64-bit PCI segments, the MCH communicates with the P64H2 through a private interface called the HI (Hub Interface). If the cycle is directed to the ICH3-S, the cycle is output on the MCH's 8bit HI 1.5 bus. The P64H2 translates the HI 2.0 bus operation to a 64-bit PCI Rev. 2.1-compliant signaling environment operating at from 133MHz to 33 MHz.

The HI 2.0 bus is 16 bits wide and operates at 66 MHz with 512MT/s, providing over 1 GB per second of bandwidth.

All I/O for the Server Board SE7500CW2, including PCI and PC-compatible, is directed through the MCH and then through either the P64H2 or the ICH3-S provided PCI buses.

- The ICH3-S provides a 32-bit/33-MHz PCI bus hereafter called P32-A.
- The P64H2 provides two independent 64-bit, 133-MHz PCI-X buses hereafter called P64-B, and P64-C.

This independent bus structure allows all three PCI buses to operate independently.

3.2.1 MCH Memory Architecture Overview

The MCH supports a 144-bit Memory Sub-system that can support a maximum of 4GB¹ (using 2GB DIMMs). This configuration needs external registers for buffering the memory address and control signals. In this configuration MCH support four DDR200 compliant registered for maximum of 8GB¹. The four chip selects are registered inside MCH and need no external registers for chip selects.

The memory interface runs at 200MT/s. The memory interface supports a 144-bit wide memory array. It uses fifteen address lines (BA[1:0] and MA[12:0]) and supports 64Mb, 128Mb, 256Mb, 512Mb DRAM densities. The DDR DIMM interface supports memory scrubbing, single-bit error correction, and multiple bit error detection and chip kill with x4 DIMMs.

3.2.1.1 DDR Configurations

The DDR interface supports up to 4GB¹ of main memory and supports single- and double-density DIMMs. The DDR can be any industry-standard DDR. The following table shows the DDR DIMM supported.

Table 3. Supported DDRs

| DIMM Capacity | DIMM Organization | SDRAM Density | SDRAM Organization | # SDRAM Devices/rows/Banks | # Address bits rows/Banks/column |
|---------------|-------------------|---------------|--------------------|----------------------------|----------------------------------|
| 128MB | 16M x 72 | 64Mbit | 16M x 4 | 18/1/4 | 12/2/10 |
| 128MB | 16M x 72 | 64Mbit | 8M x 8 | 18/2/4 | 12/2/9 |
| 128MB | 16M x 72 | 128Mbit | 16M x 8 | 9/1/4 | 12/2/10 |
| 256MB | 32M x 72 | 64Mbit | 16M x 4 | 36/2/4 | 12/2/10 |
| 256MB | 32M x 72 | 128Mbit | 32M x 4 | 18/1/4 | 12/2/11 |
| 256MB | 32M x 72 | 128Mbit | 16M x 8 | 18/2/4 | 12/2/10 |
| 256MB | 32M x 72 | 256Mbit | 32M x 8 | 9/1/4 | 13/2/10 |
| 512MB | 64M x 72 | 128Mbit | 32M x 4 | 36/2/4 | 12/2/11 |
| 512MB | 64M x 72 | 256Mbit | 64M x 4 | 18/1/4 | 13/2/11 |
| 512MB | 64M x 72 | 256Mbit | 32M x 8 | 18/2/4 | 13/2/10 |
| 512MB | 64M x 72 | 512Mbit | 64M x 8 | 9/1/4 | 13/2/11 |
| 1GB | 128M x 72 | 256Mbit | 64M x 4 | 36/2/4 | 13/2/11 |
| 1GB | 128M x 72 | 512Mbit | 64M x 8 | 18/2/4 | 13/2/11 |

¹As of the writing of this document, testing with 2GB DIMM modules was not complete and therefore not yet supported. 2GB DIMM support would allow for up to 8GB of main memory. For updates on support of 2GB DIMM modules, see <http://support.intel.com/support/motherboards/server/se7500cw2>.

| | | | | | |
|-----|-----------|---------|----------|--------|---------|
| 1GB | 128M x 72 | 512Mbit | 128M x 4 | 18/1/4 | 13/2/12 |
| 2GB | 256M x 72 | 512Mbit | 64M x 8 | TBD | TBD |
| 2GB | 256M x 72 | 512Mbit | 128M x 4 | TBD | TBD |
| 2GB | 256M x 72 | 512Mbit | 128M x 4 | TBD | TBD |

3.2.2 MCH North Bridge

The Intel E7500 Chipset MCH North Bridge (MCH) is a 1005 ball FC-BGA device and uses the proven components of previous generations like the Intel Xeon processor bus interface unit, the Hub Interface unit, and the DDR memory interface unit. In addition, the MCH incorporates a Hub Interface (HI). The HI interface enables the MCH to directly interface with the P64H2. The MCH also increases the main memory interface bandwidth and maximum memory configuration with a 144-bit wide memory interface.

The MCH integrates three main functions:

- An integrated high performance main memory subsystem.
- An HI 2.0 bus interface that provides a high-performance data flow path between the host bus and the I/O subsystem.
- A HI 1.5 bus which provides an interface to the ICH3-S (South Bridge).

Other features provided by the MCH include the following:

- Full support of ECC on the processor bus.
- Full support of Intel® x4 Single Device Data Correction on the memory interface with x4 DIMMs.
- Twelve deep in-order queue.
- Full support of registered DDR200 and DDR266 ECC DIMMs.
- Support for 8GB¹ of DDR DIMMs.
- Memory scrubbing.

3.2.3 P64H2

The P64H2 is a 567 ball FC-BGA device and provides an integrated I/O bridge that provides a high-performance data flow path between the HI 2.0 and the 64-bit I/O subsystem. This subsystem supports peer 64-bit PCI-X segments. Because it has two PCI interfaces, the P64H2 can provide large and efficient I/O configurations. The P64H2 functions as the bridge between the HI and the two 64-bit PCI-X I/O segments. The HI interface can support 1 GB/s of data bandwidth.

¹As of the writing of this document, testing with 2GB DIMM modules was not complete and therefore not yet supported. 2GB DIMM support would allow for up to 8GB of main memory. For updates on support of 2GB DIMM modules, see <http://support.intel.com/support/motherboards/server/se7500cw2>.

3.2.3.1 PCI Bus P64-B I/O Subsystem

P64-B supports the following embedded devices and connectors:

- Two 184-pin, 3.3-volt keyed, 64-bit PCI expansion slot connectors running at 100MHz. Both slots support 184-pin, 3.3V keyed, 64-bit PCI-X expansion slots. Both slots support full-length PCI add-in cards.

The BIOS is responsible for setting the bus speed of P64-B. The bus speed will always be set up to run at the speed of the slowest card installed.

3.2.3.2 PCI Bus P64-C I/O Subsystem

P64-C supports the following embedded devices and connectors:

- One 184-pin, 3.3-volt keyed, 64-bit PCI expansion slot connector running at 133MHz. This slot is capable of supporting a full length add-in PCI card.
- This expansion slot can be used for riser card, should this board be integrated into a high-density chassis. The slot is designed to support up to 3 PCI slots on the riser, however actual number of slots and slot speeds will be determined by the signal integrity of the riser card used.

The BIOS is responsible for setting the bus speed of P64-C. The bus speed will always be set up to run at the speed of the slowest card installed.

3.2.4 ICH3-S

The ICH3-S is a multi-function device, housed in a 421-pin BGA device, providing a HI 1.5 to PCI bridge, a PCI IDE interface, a PCI USB controller, and a power management controller. Each function within the ICH3-S has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

On the Server Board SE7500CW2, the primary role of the ICH3-S is to provide the gateway to all PC-compatible I/O devices and features. The Server Board SE7500CW2 uses the following ICH3-S features:

- 32-bit PCI bus interface
- 16-bit LPC bus interface
- IDE interface, with Ultra DMA 100 capability
- Universal Serial Bus (USB) interface
- PC-compatible timer/counter and DMA controllers
- APIC and 8259 interrupt controller
- Power management
- System RTC
- General purpose I/O

The following are the descriptions of how each supported feature is used on Server Board SE7500CW2.

3.2.4.1 PCI Bus P32-A I/O Subsystem

The ICH3-S provides a legacy 32-bit PCI subsystem and acts as the central resource on this PCI interface.

P32-A supports the following embedded devices and connectors:

- An ATI* Rage* XL video controller with 3D/2D graphics accelerator
- Promise Technology* PDC20267 dual channel ATA-100 RAID controller.
- Two Intel 82550PM network controllers
- Two 5V keyed expansion slots capable of supporting full length PCI add-in cards operating at 33MHz

3.2.4.2 PCI Bus Master IDE Interface

The ICH3-S acts as a PCI-based Ultra DMA/100 IDE controller that supports programmed I/O transfers and bus master IDE transfers. The ICH3-S supports two IDE channels, supporting two drives each (drives 0 and 1). The Server Board SE7500CW2 provides two SSI compliant 40-pin (2x20) IDE connectors to access the IDE functionality.

The Server Board SE7500CW2 IDE interface supports Ultra DMA/100 Synchronous DMA Mode transfers on each 40-pin connector.

3.2.4.3 USB Interface

The ICH3-S contains three USB revision 1.1 controllers and four USB hubs. The USB controller moves data between main memory and the six USB connectors. All six ports function identically and with the same bandwidth. The Server Board SE7500CW2 implements 4 of the 6 ports on the board.

The Server Board SE7500CW2 provides three external USB ports at the rear of the server board. The triple stack USB connector is located within the standard ATX I/O panel area next to the keyboard and mouse housing. The USB specification defines the external connectors.

The fourth USB ports is optional and can be accessed by cabling from the internal 9-pin connector located on the baseboard to external USB ports located either in front or the rear of a given chassis.

3.2.4.4 Compatibility Interrupt Control

The ICH3-S provides the functionality of two 82C59 PIC devices for ISA-compatible interrupt handling.

3.2.4.5 APIC

The ICH3-S integrates an APIC that is used to distribute 24 interrupts.

3.2.4.6 Power Management

One of the embedded functions of the ICH3-S is a power management controller. The Server Board SE7500CW2 uses this to implement ACPI-compliant power management features. The Server Board SE7500CW2 supports sleep states S0, S4, and S5.

3.3 Super I/O

The Windbond* 83627HF Super I/O device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, PS/2-compatible keyboard and mouse, and hardware monitor controller. The Server Board SE7500CW2 supports the following features:

- GPIOs
- Two serial ports
- Floppy
- Keyboard and mouse
- Local hardware monitoring
- "Wake-on" control

3.3.1 Serial Ports

The Server Board SE7500CW2 provides two serial ports, an external serial port, and an internal serial header. The following sections provide details on the use of the serial ports.

3.3.1.1 Serial 1

Serial 1 is a standard DB9 interface located at the rear I/O panel of the server board, to the left of the video connector below the parallel port connector. Serial port 1 is designated by silkscreen "Serial 1" and reference designator J44.

3.3.1.2 Serial 2

Serial 2 is an optional port, accessed through a 9-pin internal header (J28). A standard DH-10 to DB9 cable can be used to direct serial 2 to an external connector on any given chassis. The serial 2 interface follows the standard RS232 pin out. The baseboard has a "Serial 2" silkscreen label next to the connector. The serial number 2 connector is located just below PCI slot 5.

3.3.1.3 Floppy Disk Controller

The floppy disk controller (FDC) in the SIO is functionally compatible with floppy disk controllers in the DP8473 and N844077. All FDC functions are integrated into the SIO including analog data separator and 16-byte FIFO. The Server Board SE7500CW2 provides a standard 36-pin interface for the floppy disk controller.

3.3.1.4 Keyboard and Mouse

Two external PS/2 ports, located on the back of the baseboard, are provided to access the keyboard or mouse functions. The two ports are interchangeable and will automatically detect and configure a keyboard or mouse plugged into either port.

3.3.1.5 Wake-on Control

The Super I/O contains functionality that allows various events to control the power-on and power-off the system.

3.3.2 BIOS Flash

The Server Board SE7500CW2 incorporates an Intel® N82802AC (FWH8) Flash memory component. The N82802AC is a high-performance 8-megabit memory component that provides 1024K x 8 of BIOS and non-volatile storage space. The flash device is connected through the LPC Bus from the ICH3-S from the SIO.

4. Included PCI Devices

4.1 ATA-100 RAID

The Intel® Server Board SE7500CW2 provides an embedded dual channel ATA-100 bus through the use of the Promise* Technology PDC20267 ASIC. The PDC20267 ATA-100 controller contains two independent ATA-100 channels that share a single 32-bit, 33-MHz PCI bus master interface as a multifunction device, packaged in a 128-pin PQFP.

The ATA-100 controller supports the following features:

- The scatter / gather mechanism supports both DMA and PIO IDE drives and ATAPI devices
- Support for ATA and ATAPI proposal PIO Mode 0, 1, 2, 3, 4, DMA Mode 0, 1, 2, and Ultra DMA Mode 0, 1, 2, 3, 4, 5
- The IDE drive transfer rate is capable of up to 100 MB/sec per channel
- The host interface complies with PCI Local Bus Specification, Revision 2.2
- 32-bit, 33-MHz bus speed and 132 MB/sec sustained transfer rate

The Promise PDC20267 supports IDE RAID through dual ATA-100 Channels. In a RAID configuration, multiple IDE hard drives are placed into one or more arrays of disks. Each array is seen as an independent disk, though the array may include upwards of two, three, or four drives. The IDE RAID can be configured as followings:

Table 4. ATA-100 RAID Level

| RAID Level | Performance | Capacity | # of Drives |
|--------------------------|--------------------|--------------------------|--------------------|
| RAID 0 (Striping) | Highest | # Drives x Smallest Size | 2 to 4 |
| RAID 1 (Mirroring) | Normal | 50% min | 2 |
| RAID 0+1 (Stripe/Mirror) | High | 50% min | 4 |
| JBOD (Spanning) | Normal | 100% of all drives | 2 to 4 |

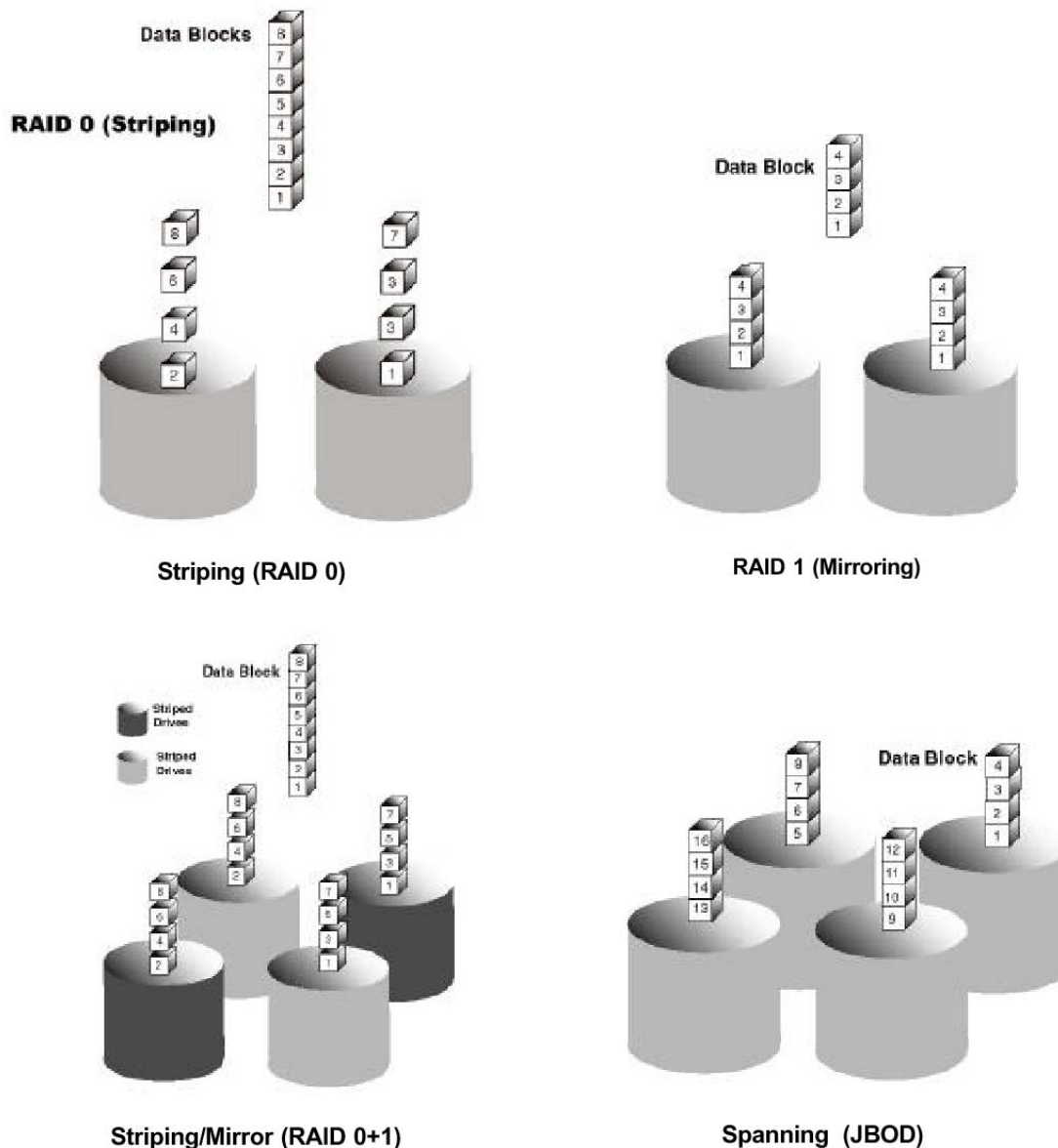


Figure 4. ATA-100 RAID Level

RAID 0 configurations are used for high performance applications, as it doubles the sustained transfer rate of its drives. RAID 1 configurations primarily used for data protection. It creates an identical drive backup to a secondary drive. Whenever a disk write is performed, the controller sends data simultaneously to a second drive located on a different data channel. With four drives attached to dual ATA-100 channels, two striped drive pairs can mirror each other (RAID 0+1) for storage capacity and data redundancy.

4.2 Video Controller

The Intel® Server Board SE7500CW2 provides an ATI Rage XL PCI graphics accelerator, along with 8 MB of video SDRAM and support circuitry for an embedded SVGA video subsystem. The ATI Rage XL chip contains a SVGA video controller, clock generator, 2D and 3D engine, and RAMDAC in a 272-pin PBGA. One 2Mx32 SDRAM chip provides 8 MB of video memory.

The SVGA subsystem supports a variety of modes, up to 1600 x 1200 resolution in 8/16/24/32 bpp modes under 2D, and up to 1024 x 768 resolution in 8/16/24/32 bpp modes under 3D. It also supports both CRT and LCD monitors up to 100 Hz vertical refresh rate.

The Intel® Server Board SE7500CW2 provides a standard 15-pin VGA connector and supports disabling of the on-board video through the BIOS setup menu or when a plug in video card is installed in any of the PCI slots.

4.2.1.1 Video Modes

The ATI Rage XL chip supports all standard IBM VGA modes. The following table shows the 2D/3D modes supported for both CRT and LCD. The table specifies the minimum memory requirement for various display resolution, refresh rates and color depths.

Table 5. Video Modes

| 2D Mode | Refresh Rate (Hz) | 2D Video Mode Support | | | |
|---|---------------------|--|-----------|-----------|-----------|
| | | 8 bpp | 16 bpp | 24 bpp | 32 bpp |
| 640x480 | 60, 72, 75, 90, 100 | Supported | Supported | Supported | Supported |
| 800x600 | 60, 70, 75, 90, 100 | Supported | Supported | Supported | Supported |
| 1024x768 | 60, 72, 75, 90, 100 | Supported | Supported | Supported | Supported |
| 1280x1024 | 43, 60 | Supported | Supported | Supported | Supported |
| 1280x1024 | 70, 72 | Supported | – | Supported | Supported |
| 1600x1200 | 60, 66 | Supported | Supported | Supported | Supported |
| 1600x1200 | 76, 85 | Supported | Supported | Supported | – |
| 3D Video Mode Support with Z Buffer Enabled | | | | | |
| 3D Mode | Refresh Rate (Hz) | 3D Video Mode Support with Z Buffer Enabled | | | |
| 640x480 | 60,72,75,90,100 | Supported | Supported | Supported | Supported |
| 800x600 | 60,70,75,90,100 | Supported | Supported | Supported | Supported |
| 1024x768 | 60,72,75,90,100 | Supported | Supported | Supported | Supported |
| 1280x1024 | 43,60,70,72 | Supported | Supported | – | – |
| 1600x1200 | 60,66,76,85 | Supported | – | – | – |
| 3D Video Mode Support with Z Buffer Disabled | | | | | |
| 3D Mode | Refresh Rate (Hz) | 3D Video Mode Support with Z Buffer Disabled | | | |
| 640x480 | 60,72,75,90,100 | Supported | Supported | Supported | Supported |
| 800x600 | 60,70,75,90,100 | Supported | Supported | Supported | Supported |
| 1024x768 | 60,72,75,90,100 | Supported | Supported | Supported | Supported |
| 1280x1024 | 43,60,70,72 | Supported | Supported | Supported | – |
| 1600x1200 | 60,66,76,85 | Supported | Supported | – | – |

4.2.1.2 Video Memory Interface

The memory controller subsystem of the ATI Rage XL arbitrates requests from direct memory interface, the VGA graphics controller, the drawing coprocessor, the display controller, the video scalar, and hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

The server board supports an 8MB (512Kx32bitx4 Banks) SDRAM device for video memory.

4.3 Network Interface Controller (NIC)

The Server Board SE7500CW2 supports two 10Base-T/100Base-TX Network Interface Controllers (NICs) based on the Intel 82550PM NIC. The 82550PM is a highly integrated PCI LAN controller in a thin BGA 15mm package. The controller's baseline functionality is equivalent to that of the Intel 82559, with the addition of Alert-on-LAN functionality. The Server Board SE7500CW2 supports independent disabling of the two NIC controllers using the BIOS Setup menu.

The 82550PM supports the following features:

- Glueless 32-bit PCI, CardBus master interface (Direct Drive of Bus), compatible with *PCI local Bus Specification, Revision 2.2*.
- Integrated IEEE 802.3 10Base-T and 100Base-TX compatible PHY.
- IEEE 820.3u auto-negotiation support.
- Full duplex support at both 10 Mbps and 100 Mbps operation.
- Integrated UNDI ROM support.
- MDI/MDI-X and HWI support.
- Low power +3.3 V device.

4.3.1.1 NIC Connector and Status LEDs

The 82550PM drive two LEDs located on each network interface connector. The amber LED indicates network connection when on, and transmit/receive activity when blinking. The yellow LED indicates 100-Mbps operating mode when lit, and 10-Mbps when off.

4.4 Optional SCSI Card

Certain versions of the Server Board SE7500CW2 include an add-in Ultra-160 SCSI card. This card has the following specifications:

- Ultra 160 single channel based on the LSI 53C1000 SCSI controller
- PCI 2.2 compliant
- PCI 64-bit/66MHz operation
- Universal PCI card edge connector
- Low profile form factor, shipping with full-size PCI bracket attached and low profile bracket in packaging
- Internal and external connectors (internal standard 68-pin, external VHDI interface)
- Termination: universal (LVD/SE) termination, automatic cable detection, software disable
- 4 pin header for off board LEDs

Pin-out for the card is as follows:

Table 6. Optional Intel® 53C1000B1 SCSI card pin-out(J1)

| Pin | Signal Name |
|-----|-------------|
| 1 | +5V |
| 2 | LED1_L |
| 3 | LED1_L |
| 4 | +5V |

4.5 Interrupt Routing

The Server Board SE7500CW2 interrupt architecture accommodates both PC-compatible PIC mode and APIC mode interrupts through use of the integrated I/O APICs in the ICH3-S.

4.5.1 Legacy Interrupt Routing

For PC-compatible mode, the ICH3-S provides two 82C59-compatible interrupt controllers. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The ICH3-S contains configuration registers that define which interrupt source logically maps to I/O APIC INTx pins.

Interrupts, both PCI and IRQ types, are handled by the ICH3-S. The ICH3-S then translates these to the APIC bus. The numbers in the table below indicate the ICH3-S PCI interrupt input pin to which the associated device interrupt (INTA, INTB, INTC, INTD) is connected. The ICH3-S' I/O APIC exists on the I/O APIC bus with the processors.

Table 7. PCI Interrupt Routing/Sharing

| Interrupt | INT A | INT B | INT C | INT D |
|----------------------------|----------------------------|--------------|--------------|--------------|
| ATI Rage SL | ICH3_PIRQF_L | | | |
| Promise ATA-100 Controller | ICH3_PIRQG_L | | | |
| 82550PM #2 | ICH3_PIRQE_L | | | |
| 82550PM #1 | ICH3_PIRQH_L | | | |
| P64H2 BT INTR# | ICH3_PIRQC# (for PIC mode) | | | |
| P64-C Slot 1 | P1_IRQ0_L | P1_IRQ1_L | P1_IRQ2_L | P1_IRQ3_L |
| P64-B Slot 2 | P2_IRQ0_L | P2_IRQ1_L | P2_IRQ2_L | P2_IRQ3_L |
| P64-B Slot 3 | P2_IRQ4_L | P2_IRQ5_L | P2_IRQ6_L | P2_IRQ7_L |
| P32-A Slot 4 | ICH3_PIRQB_L | ICH3_PIRQC_L | ICH3_PIRQB_L | ICH3_PIRQC_L |
| P32-A Slot 5 | ICH3_PIRQD_L | ICH3_PIRQA_L | ICH3_PIRQD_L | ICH3_PIRQA_L |

4.5.2 APIC Interrupt Routing

For APIC mode, the Server Board SE7500CW2 interrupt architecture incorporates three Intel I/O APIC devices to manage and broadcast interrupts to local APICs in each processor. The Intel I/O APICs monitor each interrupt on each PCI device including PCI slots in addition to the ISA compatibility interrupts IRQ(0-15). When an interrupt occurs, a message corresponding to the interrupt is sent across a three-wire serial interface to the local APICs. The APIC bus minimizes interrupt latency time for compatibility interrupt sources. The I/O APICs can also supply greater than 16 interrupt levels to the processor(s). This APIC bus consists of an APIC clock and two bi-directional data lines.

4.5.2.1 Legacy Interrupt Sources

The table below recommends the logical interrupt mapping of interrupt sources on the Server Board SE7500CW2. The actual interrupt map is defined using configuration registers in the ICH3-S.

Table 8. Interrupt Definitions

| ISA Interrupt | Description |
|---------------|---|
| INTR | Processor interrupt. |
| NMI | NMI to processor. |
| IRQ0 | System timer |
| IRQ1 | Keyboard interrupt. |
| IRQ2 | Slave PIC |
| IRQ3 | Serial port 1 or 2 interrupt from SIO device, user-configurable. |
| IRQ4 | Serial port 1 or 2 interrupt from SIO device, user-configurable. |
| IRQ5 | Parallel Port / Generic |
| IRQ6 | Floppy disk. |
| IRQ7 | Parallel Port / Generic |
| IRQ8_L | Active low RTC interrupt. |
| IRQ9 | SCI* |
| IRQ10 | Generic |
| IRQ11 | Generic |
| IRQ12 | Mouse interrupt. |
| IRQ13 | Floppy processor. |
| IRQ14 | Compatibility IDE interrupt from primary channel IDE devices 0 and 1. |
| IRQ15 | Secondary IDE Cable |
| SMI* | System Management Interrupt. General purpose indicator sourced by the ICH3-S to the processors. |

4.5.3 Serialized IRQ Support

The Intel® Server Board SE7500CW2 supports a serialized interrupt delivery mechanism. Serialized Interrupt Requests (SERIRQ) consists of a start frame, a minimum of 17 IRQ / data channels, and a stop frame. Any slave device in the quiet mode may initiate the start frame. While in the continuous mode, the start frame is initiated by the host controller.

4.5.4 IRQ Scan for PCIIRQ

The IRQ / data frame structure includes the ability to handle up to 32 sampling channels with the standard implementation using the minimum 17 sampling channels. The Server Board SE7500CW2 has an external PCI interrupt serializer for PCIIRQ scan mechanism of ICH3-S to support 16 PCI IRQs.

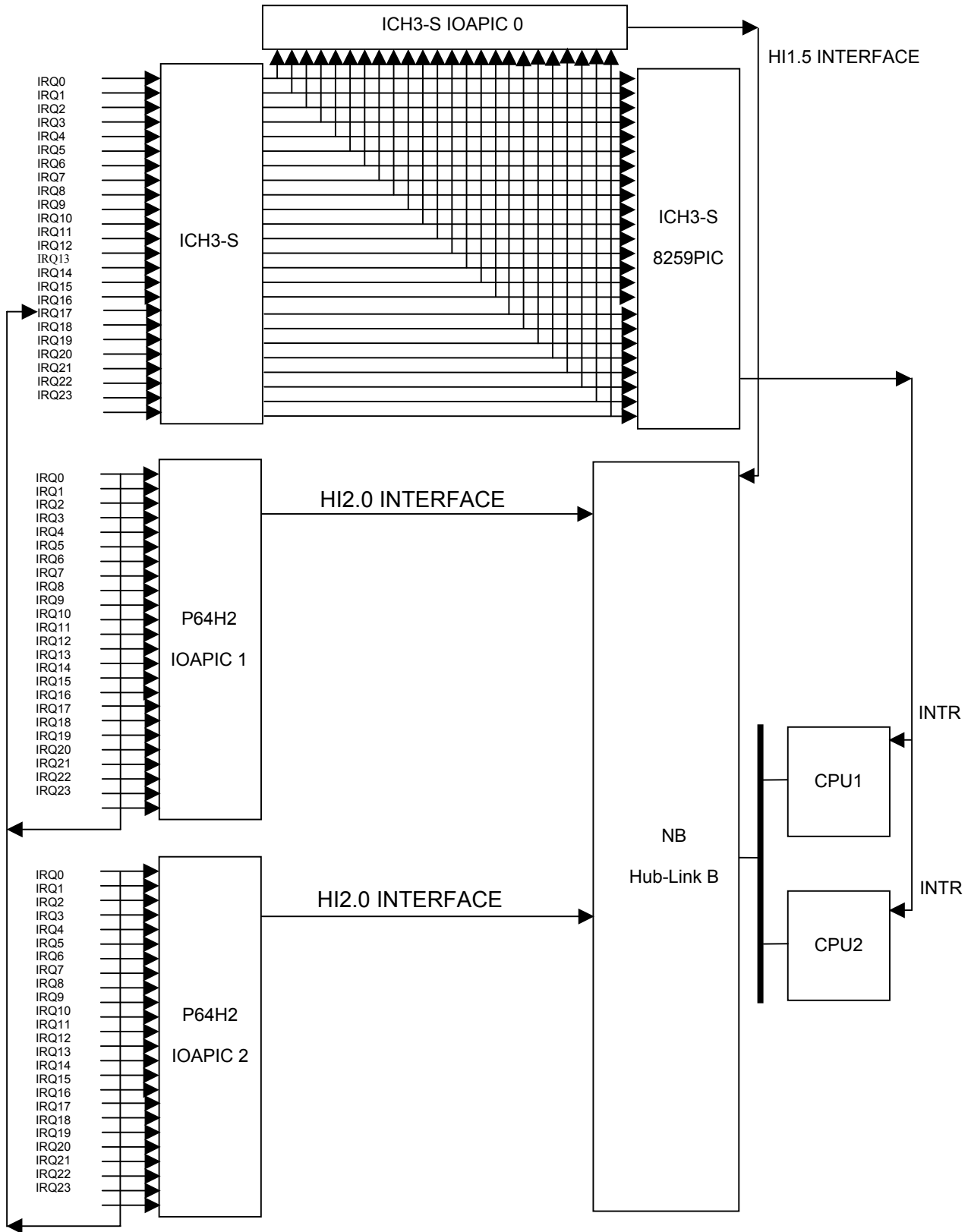


Figure 5. SE7500CW2 Interrupt Routing Diagram (ICH3-S Internal)

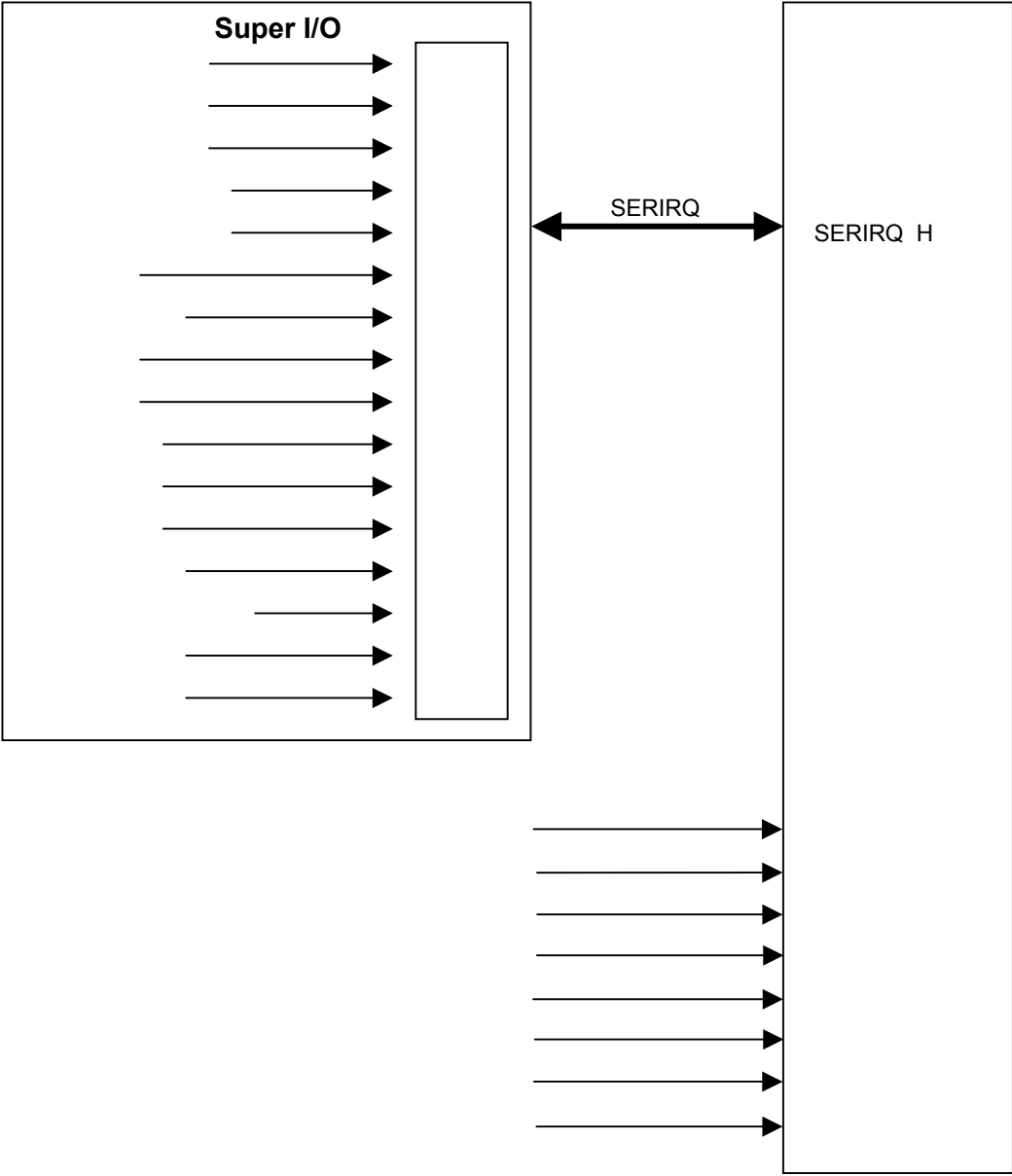
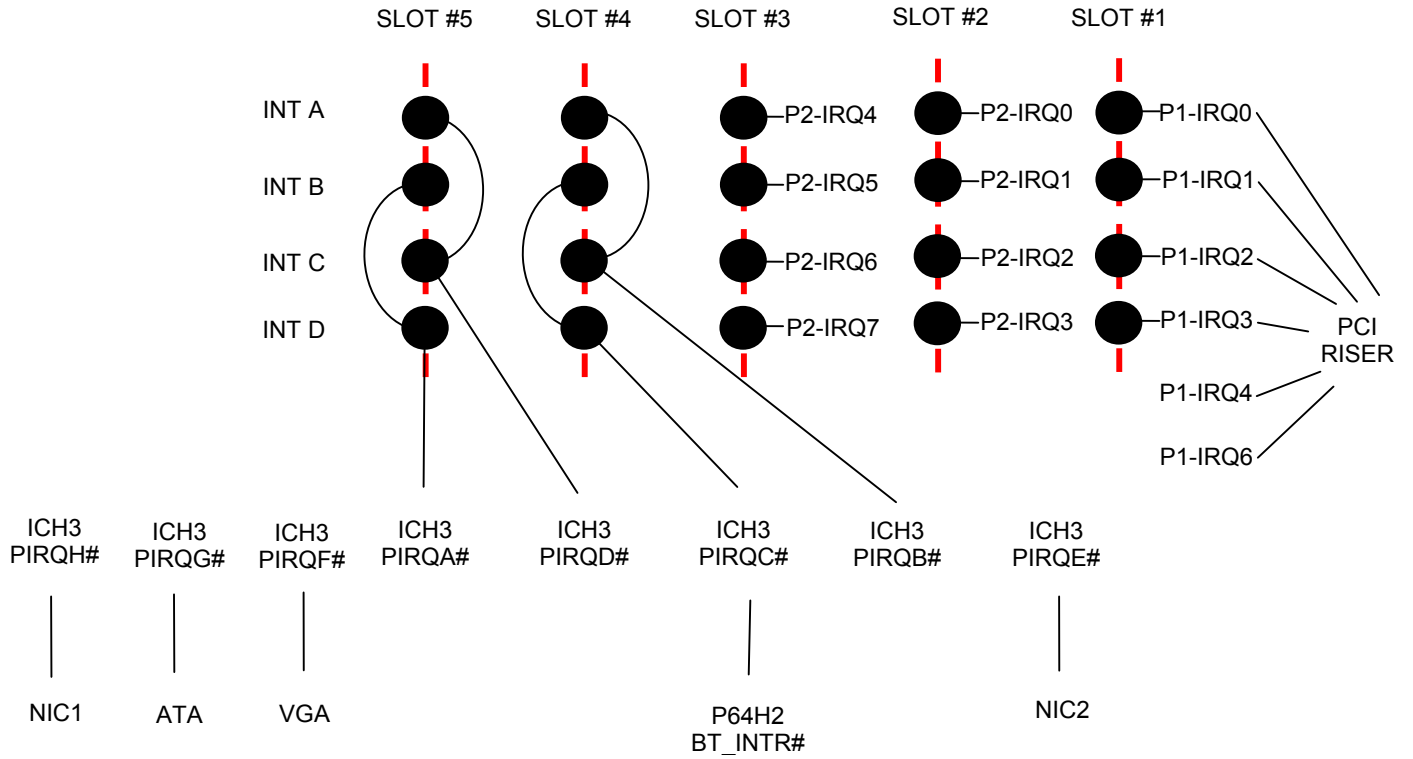


Figure 6. Interrupt Routing Diagram



Note: P1 is P64H2 PCI-bus A, P2 is P64H2 PCI-bus B

Figure 7. PCI Interrupt Mapping Diagram

5. Hardware Monitoring

The Server Board SE7500CW2 has an integrated Winbond* 83627HF SIO controller with integrated hardware monitoring and a MAX6651 controller both of which provide basic hardware monitoring capabilities. These controllers use the I²C bus to communicate to all the sensors integrated on the baseboard.

Below is a table of monitored headers and sensors on the Server Board SE7500CW2.

Table 9. Monitored Components

| | Item | Description |
|-------------|---------------------|---|
| Voltage | Vcpu | Monitors processor voltage. (sIO) |
| | 1.8V | Monitors +1.8V. (sIO) |
| | 3.3V | Monitors +3.3V. (sIO) |
| | 5V | Monitors 5VSB (Internal). (sIO) |
| | AUX3V | Monitors +12Vin. (sIO) |
| | ENG12V | Monitors -12Vin (should be same as 12V @ Power-Supply). (sIO) |
| | 2.5V | Monitors -5V. (sIO) |
| | Vbat | Monitors battery voltage (sIO) |
| | AUX5V | Monitors 5VSB. (sIO) |
| | Fan Speed | PWM1 |
| PWM2 | | Controls 2 rear system fans (sIO) |
| PWM3 | | Controls 2 CPU fans (MAX6651) |
| FanIO1 | | Monitors front fan (sIO) |
| FanIO2 | | Monitors front fan (sIO) |
| TACH0 | | Monitors rear fan (MAX6651) |
| TACH1 | | Monitors rear fan (MAX6651) |
| TACH2 | | Monitors CPU fan (MAX6651) |
| TACH3 | | Monitors CPU fan (MAX6651) |
| Temperature | | CPU1 |
| | CPU2 | Monitors secondary processor temperature. (sIO) |
| | Ambient Temperature | Monitors Ambient temperature (sIO) |

Below is a diagram explaining what the Winbond* W83627HF chip and MAX6651 chip monitor on the Intel[®] Server Board SE7500CW2 and how the monitoring is accomplished.

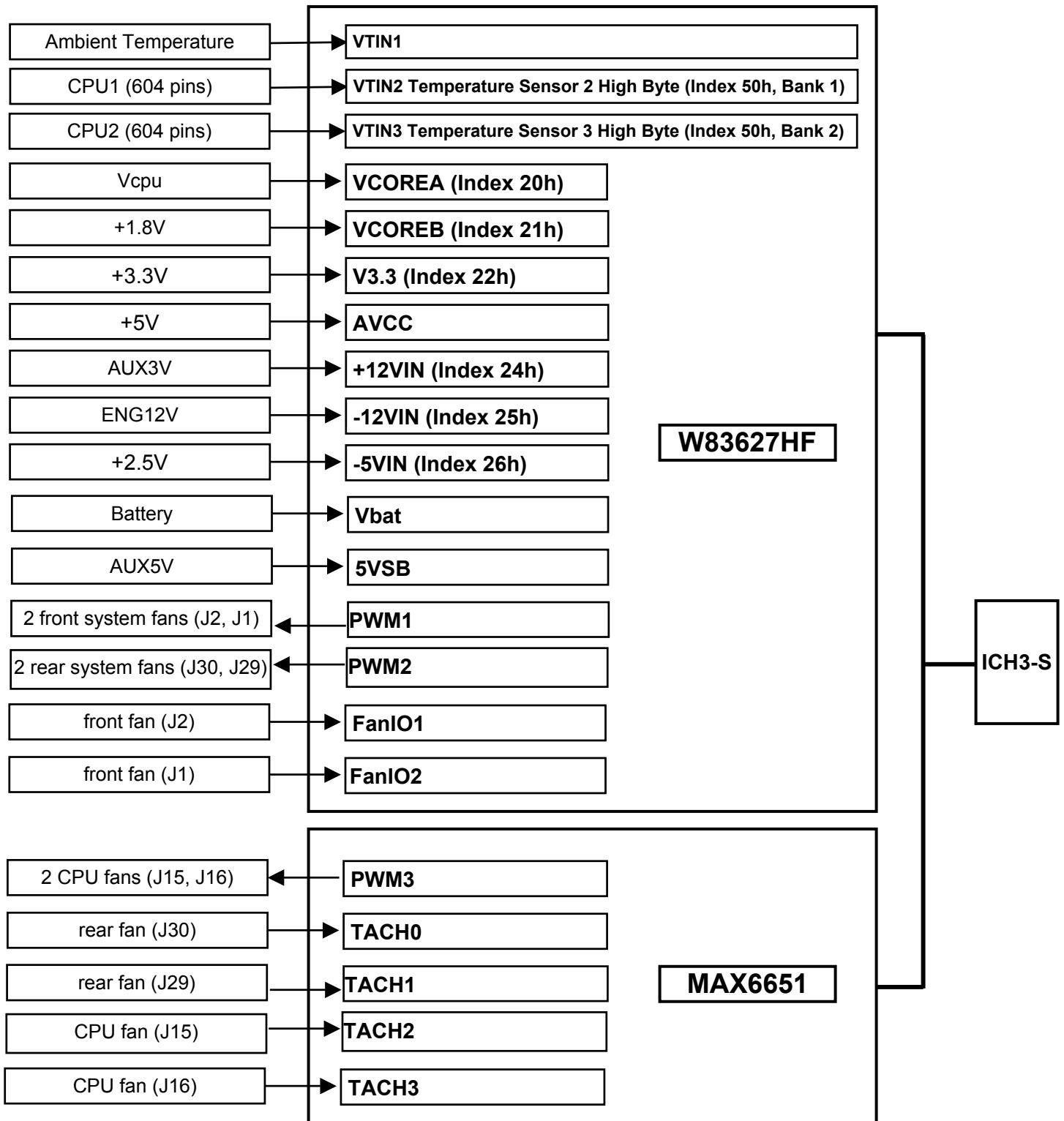


Figure 8. Hardware Monitoring

5.1 LANDesk* Client Manager

Included with the Server Board SE7500CW2 is a copy of the LANDesk Client Manager (LDCM) software. This software utilizes the management controllers on the server board to display real-time status of the sensors on the baseboard and provide alerts if sensors go outside their pre-determined thresholds. The software runs on the Microsoft* Windows* 2000 operating system and provides a graphical user interface (GUI) for monitoring the health of the server system.

The initial version of the software that shipped on the first boards was only capable of monitoring critical sensors on the board. Updated versions of the software files to allow for additional monitoring capability will be posted to the Server Board SE7500CW2 support website at <http://support.intel.com/support/motherboards/server/se7500cw2>. Please check this web site for updates to the software prior to installing and using it. Additionally, documentation on how to install and use the LDCM software is provided on the Server Board SE7500CW2 resource CD and on the support website at this URL.

6. System BIOS

The Server Board SE7500CW2 contains the following on-board Application Specific Integrated Circuits (ASICs) that require BIOS support:

- Intel E7500 MCH North Bridge with Memory Controller
- Intel ICH3 Source Bridge integrate USB controller, IDE controller, SMBUS controller, LPC Bridge, and RTC
- P64H2 PCI bridge support PCI bridging and PCI hot plug
- 1MB FWH provide the BIOS code storage
- Windbond* W83627F Super I/O integrate Serial Port/Parallel port/PS2 KB/mouse/Floppy and H/W Monitor functionality
- Dual Channel Promise PDC20267 ATA-100 with RAID 0, 1 & 1+0 support
- ATI Rage XL with 8MB SDRAM support

6.1.1 System Flash ROM Layout

The flash ROM contains system initialization routines, the BIOS Setup Utility, and runtime support routines. The exact layout is subject to change, as determined by Intel. The flash ROM also contains initialization code in compressed form for on-board peripherals, like ATA-100 RAID, PXE ROM and video controllers.

The complete ROM is visible, starting at physical address 4 GB minus the size of the flash ROM device. Only BIOS needs to know the exact map. The BIOS image contains all of the BIOS components at appropriate locations. The Flash Memory Update utility loads the BIOS image minus the recovery block to the flash.

Because of shadowing, none of the flash blocks is visible at the aliased addresses below 1 MB.

A 64KB block is dedicated for boot block code which is to provide the ROM disaster recovery when the System ROM is destroyed by some unexpected reasons, like power failure while update the BIOS.

A 8 KB parameter block in the flash ROM is dedicated to storing configuration data that controls the system configuration (ESCD). Application software must use standard APIs to access these areas; application software cannot access the data directly.

6.2 System Configuration and Initialization

6.2.1 Memory

The following is a list of memory specifications that the system BIOS supports:

- Only registered DDR200 or DDR266 memory is supported. When populated with more than 4 GB of memory, the memory between 4 GB and 4 GB minus min. 128 MB is not accessible for use by the OS and may be lost to the user. This area is reserved for BIOS, APIC configuration space, PCI adapter interface, and virtual video memory space. This memory space is also lost if the system is populated with memory configurations between max. 3.872 GB and 4 GB. This size has the ability to expand by 128MB multiples if cards demand more space.

Note: The minimum DIMM size is 128M, and it will expand automatically based on the PCI Card resource claims.

The system BIOS supports registered DIMMs with CL=3 components and CL=2 components when available.

- The baseboard is hard-wired for dual channel memory support.
- The system BIOS supports only Error Correcting Code (ECC) memory.
- DIMMs must be populated in pairs with the same size. Memory timing defaults to the slowest DIMM.
- x4/x8 DIMM mixing Read Error Sighting.

All DIMMs must use SPD EEPROM or they will not be recognized by BIOS. Mixing vendors of DIMMs will be supported, but is not recommended as the system will default to the slowest speed that will work with all of the vendors.

The Server Board SE7500CW2 server BIOS is responsible for configuring and testing the system memory. Configuring system memory involves probing the memory modules for their characteristics and programming the chipset for optimum performance. The BIOS also verifies that the memory subsystem is functional.

When the system comes out of reset, the main memory is not usable. The BIOS has knowledge of the memory subsystem and it knows the type of memory, the number of DIMM sites, and their locations.

6.2.1.1 Memory Configuration

The server board uses the Intel E7500 MCH chipset to configure the system baseboard memory. The BIOS is responsible for configuring and testing the system memory. The configuration of the system memory involves probing the memory modules for their characteristics and programming the chipset for optimum performance.

When the system comes out of reset, the main memory is not usable. The BIOS verifies that the memory subsystem is functional. It has knowledge of the memory subsystem and it knows the type of memory, the number of DIMM sites, and their locations.

6.2.1.2 Memory Sizing and Initialization

During POST, the BIOS tests and sizes memory, and configures the memory controller. The BIOS determines the operational mode of the Intel E7500 based on the number of DIMMs installed and the type, size, speed, and memory attributes found on the on-board EEPROM or Serial Presence Detect (SPD) of each DIMM.

The memory system is based on rows. Since the Server Board SE7500CW2 supports dual channel memory, DIMMs must be populated in pairs with the same size. This means two DIMMs are required to constitute a row. Although DIMMs within a row must be identical, the BIOS supports various DIMM sizes and configurations allowing the rows of memory to be different. Memory sizing and configuration is guaranteed only for qualified DIMMs approved by Intel.

The memory-sizing algorithm determines the size of each row of DIMMs. The BIOS tests extended memory according to the option selected in the BIOS Setup Utility. The total amount of configured memory can be found using INT 15h, AH = 88h; ¹INT 15h, function E801h;² or INT 15h, function E820h.³ Refer to Section 1.1 for other nonstandard INT 15h functions supported by the system BIOS.

Because the system is designed to support up to 8 GB of memory, the BIOS creates a hole just below 4 GB to accommodate the system BIOS flash, APIC memory, and memory-mapped I/O located on 32-bit PCI devices. The size of this hole depends upon the number of PCI cards and the memory mapped resources requested by them. It is typically less than 128 MB.

6.2.1.3 ECC Initialization

Because only ECC memory is supported, the BIOS will need to initial the ECC before using it. The BIOS will initial the E7500 chipset Hardware scrubbing function to initialize the ECC function. While initializing base memory, the BIOS must cover the SMRAM and shadow area (0c000h – 0ffffh).

Note: ECC memory initialization cannot be aborted and may result in a noticeable delay, depending on the amount of memory in the system.

6.2.1.4 Memory Test

Memory can be classified as base memory or extended memory. Base memory is defined as the part of memory that is required for early BIOS code. Typically, 1 MB of memory is used for this. Most of the BIOS code and data is stored in a compressed form inside the BIOS flash and is decompressed into the base memory. The base memory must be available before the BIOS can stack or shadow itself.

Extended memory is the memory above the top of base memory (1 MB through the total memory size). Extended memory may be contiguous or it can have one or more holes.

The memory test consists of two steps: a base memory test and an extended memory test. The base memory test must be run before video is initialized. The video provides a key visual indication that the system is functional, so enabling video as early as possible during POST is a

¹ INT 15h, AH=88h can report a maximum of 64 MB of contiguous memory.

² INT 15h, function E801h can report a maximum of 4096 MB of contiguous memory.

³ INT 15h, function E820h can report up to $2^{65} - 1$ bytes of memory including non-contiguous memory regions.

priority. It is possible to test the entire memory in one step, but the memory test and initialization can be a time consuming process. Therefore, the BIOS tests only the minimum amount of memory (1 MB) before video is displayed and it tests the remaining memory after video is initialized. In addition, the BIOS displays the status of extended memory test on the console if diagnostic messages are enabled.

The Server Board SE7500CW2 server BIOS implements a 32-bit, fast, enhanced memory test. The code supports page table extensions as defined in the Pentium® Pro processor specifications. It is capable of accessing memory above 4 GB and skipping the memory hole. The user can select the coverage for extended memory tests by selecting the desired memory test option in the BIOS Setup Utility. The BIOS can test every location (extensive), one “interleave width” per KB of memory (sparse), or one “interleave width” per MB of memory (quick), depending on user preference.

The “interleave width” of a memory subsystem depends on the chipset configuration. For 2:1 interleave, the interleave width is 128-bits. By default, the BIOS tests one “interleave width” per MB of memory for base as well as extended memory. This default was selected to reduce the time spent in POST. The extended memory test can be aborted by pressing the <ESC> key anytime during the test.

6.2.1.5 Memory Error Detection

During POST memory testing, the detection of single-bit and multi-bit errors in DRAM banks is enabled. If a single-bit error (SBE) or multiple-bit error (MBE) is detected, the location within a 4K chunk will be allocated and reported by E7500 MCH and BIOS which will log the error event to NVRAM. This is done by BIOS automatically. In addition, with multi-bit error, BIOS will stop the remaining memory test, and record the current test memory as the total memory installed.

If the MBE (Multi-Bit Error) is in the first bank of memory, the system will hang and have no video.

MBE/SBE (Single-Bit Error) errors are handled by SMI handler, When either MBE or SBE errors are generated, the SMI will be triggered, and the event will be logged into the Flash Rom (in Some cases, the MBE may not be logged due to the access area is error. A user can view the event in the <F2> Setup | Advanced | Event Logging | View Event Log). In addition, the system will hang after the event is logged if it is a MBE error.

6.2.2 Processors

The BIOS determines the processor stepping, cache size, etc through the CPUID instruction. The requirements are as follows:

- All processors in the system must operate at the same frequency and have the same cache sizes, and the same VID. No mixing of product families supported.
- Processors run at a fixed speed and cannot be programmed to operate at a lower or higher speed.

6.2.2.1 Processor Initialization

The Server Board SE7500CW2 can support up to two Intel Xeon processors with 512KB L2 cache. The system BIOS must perform the various initialization sequences to program each processor cache, APIC and MTRRs.

6.2.2.2 Processor Microcode Updates

All Intel Xeon processors can correct specific errata by loading an Intel-supplied data block (also called the “update”). The BIOS is responsible for storing the update in a non-volatile memory block and loading it into each processor during the POST sequence.

The Intel Xeon processor with 512KB L2 Cache processor has the same capability for updating the processor microcode as previous Intel processors. The Server Board SE7500CW2 supports all microcode patches available for the supported processor steppings, plus an additional two empty slots are available for updates.

6.2.3 Extended System Configuration Data (ESCD), Plug and Play (PnP)

The system BIOS supports industry standards for making the system Plug-and-Play ready.

6.2.3.1 Resource Allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Intel servers. The BIOS scans for the following, in order:

1. ISA devices: Although add-in ISA devices are not supported on these systems, some standard PC peripherals may require ISA-style resources. Resources for these devices are reserved as needed.
2. When the VGA add-on card is detected, the on-board VGA will be disabled automatically. Only add-on VGA will work in such situation.
3. PCI devices: The BIOS allocates resources according to the parameters set up by the BIOS Setup and as required by the *PCI Local Bus Specification*, Revision 2.1.

The system BIOS Power-on Self Test (POST) guarantees there are no resource conflicts prior to booting the system. Note that PCI device drivers are required to support the sharing IRQs, which should not be considered a resource conflict.

6.2.3.2 PnP ISA Auto-Configuration

The system BIOS does the following:

- Supports relevant portions of the *Plug and Play ISA Specification*, Revision 1.0a and the *Plug and Play BIOS Specification*, Revision 1.0A.
- Assigns I/O, memory, direct memory access (DMA) channels, and IRQs from the system resource pool to the embedded PnP Super I/O device.
- Does not support add-in PnP ISA devices.

6.2.3.3 PCI Auto-Configuration

The system BIOS supports the INT 1Ah, AH = B1h (16 bit and 32 bit mod) functions, in conformance with the *PCI Local Bus Specification*, Revision 2.1. The system BIOS also supports the 16- and 32-bit protected mode interfaces as required by the *PCI BIOS Specification*, Revision 2.1.

Beginning at the lowest device, the BIOS uses a “depth-first” scan algorithm to enumerate the PCI buses. Each time a bridge device is located, the bus number is incremented and scanning continues on the secondary side of the bridge until all devices on the current bus are scanned.

The BIOS then scans for PCI devices using a “breadth-first” search. All devices on a given bus are scanned from lowest to highest before the next bus number is scanned.

The system BIOS POST maps each device into memory¹ and/or I/O space, and assigns IRQ channels² as required. The BIOS programs the PCI-ISA interrupt routing logic in the chipset hardware to steer PCI interrupts to compatible ISA IRQs.

The BIOS dispatches any option ROM code for PCI devices to the DOS compatibility hole (C0000h to E7FFFh³) and transfers control to the entry point. Because the DOS compatibility hole is a limited resource, system configurations with a large number of PCI devices may encounter a shortage of this resource. If the BIOS runs out of option ROM space, some PCI option ROMs are not executed and a POST error is generated. Drivers and/or the OS can detect installed devices and determine resource consumption using the defined PCI, legacy PnP BIOS, and/or ACPI BIOS interface functions.

The non-volatile RAM (NVRAM) API and the PCI data records are not supported by the system BIOS. The configuration information of the PCI devices is stored in ESCD.

6.2.4 Legacy ISA Configuration

Legacy ISA add-in devices are not supported.

6.2.5 Automatic Detection of Video Adapters

The BIOS detects video adapters in the following order:

1. Off-board PCI or an external device.
2. On-board PCI or the onboard ATI Rage XL component.

The on-board (or off-board) video BIOS is shadowed, starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to off-board devices.

No BIOS <F2> switch is present to disable external PCI devices. Though no switch exists in BIOS the onboard device will automatically be disabled if an add-in video card is added according to the order mentioned above.

6.2.6 Keyboard / Mouse Configuration

The BIOS will support both a mouse and keyboard attached to the PS/2 connectors at the I/O panel on the board. The use of each device is detected during POST and the KBC is programmed accordingly. Hot plugging of mouse and keyboard from the PS/2 connector is not supported by the system and may have unpredictable results. The BIOS will support the keyboard or mouse in either PS/2 location.

¹ The BIOS does not support devices behind PCI-to-PCI bridges that require mapping to the first 1 MB of memory space due to PCI architectural limitations (refer to the *PCI-to-PCI Bridge Architecture Specification*).

² PCI IRQ assignments may be overridden using the System Setup Utility.

³ Note that the BIOS size may increase thereby limiting the area used by option ROMs to 0C0000h – 0E0000h.

By BIOS automatic detection and swap during POST, Both PS2 port can either support the Mouse or Keyboard, but cannot support the two of the same devices (two keyboards or two mice) at the same time.

6.2.6.1 Boot without Keyboard and/or Mouse

The system can boot with or without a keyboard and/or mouse. Setup does not include an option to disable them. The presence of the keyboard and mouse is detected automatically during POST, and, if present, the keyboard is tested. The BIOS displays the message "Keyboard Detected" if it detects a keyboard during POST and it displays the message "Mouse Initialized" if it detects a mouse during POST. The system does not halt for user intervention on errors if either the keyboard or the mouse is not detected.¹

6.2.7 Floppy Drives

The Server Board SE7500CW2 server BIOS supports floppy controllers and floppy drives that are compatible with IBM* XT/AT standards. Most floppy controllers have support for two floppy drives although such configurations are rare. At a minimum, the Server Board SE7500CW2 BIOS supports 1.44 MB and 2.88 MB floppy drives. LS-120 floppy drives are attached to the IDE controller and are covered elsewhere.

The BIOS does not attempt to auto-detect the floppy drive because there is no reliable algorithm for detecting the floppy drive type if no media is installed. The BIOS auto-detects the floppy media if the user specifies the floppy drive type through setup.

The BIOS also support the selection in Set-Up for user to make the choice for the 1.44/2.88 MB or disabled. See the following table for details on various floppy types supported by each floppy drive.

Table 10: Allowed Combinations of Floppy Drive and Floppy Media

| Floppy Drive | Floppy Format | Note |
|--------------------|---------------|--|
| 1.44 MB (ordinary) | 1.44 MB | DENSEL pin is ignored by these floppy drives |
| 2.88 MB (ordinary) | 1.44 MB | The DENSEL pin is ignored by these floppy drives |
| | 2.88 MB | |

Note: The recovery BIOS requires a 1.44 MB media in a 1.44 MB floppy drive.

6.2.8 Universal Serial Bus (USB)

The Server Board SE7500CW2 server BIOS supports a USB keyboard, mouse and boot devices. The Server Board SE7500CW2 server platforms contains three USB host controller. Each host controller includes the root hub and two USB ports. Only 4 USB ports are supported in this platform. During POST, the BIOS initializes and configures the root hub ports and looks for a keyboard, mouse, boot device, and the USB hub and enables them.

The BIOS implements legacy USB keyboard support. USB legacy support in BIOS translates commands that are coming from USB KB/Mouse and translates it into the format the PS2 device generated then sent to the KB controller to emulate the PS2 behavior. It makes the USB keystrokes and the USB mouse movements appear as if they originated from the standard PS/2 devices.

¹ IRQ 12 is not available for other devices if a mouse is not present.

Emulation is transparent to the software. Legacy support is required if the system does not contain a PS/2 keyboard and mouse. BIOS support is not meant to replace a USB driver but will enable the system to allow the USB driver to control these devices.

The PS/2 keyboard/mouse port is considered the primary connection for these input devices. USB ports are treated as a contingency. Use of legacy USB emulation is not encouraged, because USB legacy support involves many SMIs (System Management Interrupts) and slows the POST and OS loader.

- USB legacy support involves many SMIs and slows the POST and operating system loader.
- It is possible to breach system security with a USB keyboard and mouse. Security features are covered in Section 6.6.

In addition, BIOS also support USB Floppy/CDROM/HD boot. With this functionality, system can work without the legacy device support to achieve legacy-free requirement.

6.3 BIOS Supported Server Management Features

The Server Board SE7500CW2 server BIOS supports many standards-based server management features and several proprietary features.

This section describes the implementation of the standard and the proprietary features including console redirection, The BIOS owns console redirection over a serial port.

6.3.1 Advanced Configuration and Power Interface (ACPI)

The primary role of the ACPI BIOS is to supply the ACPI Tables. POST creates the ACPI tables and locates them above 1 MB in extended memory. The location of these tables is conveyed to the ACPI-aware OS through a series of tables located throughout memory. The format and location of these tables is documented in the publicly available ACPI specification. To prevent conflicts with a non-ACPI-aware OS, the memory used for the ACPI tables is marked as “reserved” in the INT 15h, function E820h.

As described in the ACPI specification, an ACPI-aware OS generates an SMI to request that the system be switched into ACPI mode. The BIOS responds by setting up all system (chipset) specific configuration required to support ACPI and sets the SCI_EN bit as defined by the ACPI specification. The system automatically returns to legacy mode on hard reset or power-on reset.

There are three runtime components to ACPI:

- **ACPI Tables:** These tables describe the interfaces to the hardware. ACPI tables can make use of a p-code type of language, the interpretation of which is performed by the OS. The OS contains and uses an AML (ACPI Machine Language) interpreter that executes procedures encoded in AML and stored in the ACPI tables; ACPI Machine Language is a compact, tokenized, abstract machine language. The tables contain information about power management capabilities of the system, APICs, and the bus structure. The tables also describe control methods that the operating system uses to change PCI interrupt routing, control legacy devices in Super I/O, and find the cause of wake events.

- **ACPI Registers:** ACPI registers are the constrained part of the hardware interface, described (at least in location) by the ACPI tables.
- **ACPI BIOS:** This is the code that boots the machine and implements interfaces for sleep, wake, and some restart operations. The ACPI BIOS also provides the ACPI Description Tables.

The Server Board SE7500CW2 supports S0, S4, and S5 states. The ACPI specification defines the sleep states and requires the system to support at least one of them.

While entering the S4 state, the operating system saves the context to the disk and most of the system is powered off. The system can wake from such a state on various inputs depending on the hardware. Most platforms wake on a power button press, or a signal received from a wake-on-LAN compliant LAN card (or on-board LAN), modem ring, PCI power management interrupt, or RTC alarm. The BIOS performs complete POST upon a wake from S4 and it initializes the platform. The S4 ACPI BIOS state is not supported.

The wake sources are enabled by the ACPI operating systems with co-operation from the drivers; the BIOS has no direct control over the wake sources when an ACPI OS is loaded. The role of the BIOS is limited to describing the wake sources to the OS and controlling secondary control/status bits via a Differentiated System Description Table (DSDT).

The S5 state is equivalent to an OS shutdown. No system context is saved.

6.3.2 Wake Events

The system BIOS is capable of configuring the system to wake up from several sources under a non-ACPI configuration, such as when the operating system does not support ACPI. The typical wakes up sources are described in table 5. Under ACPI, the operating system programs the hardware to wake up on the desired event. The BIOS describes various wake sources to the operating system.

The BIOS always enables the wakeup source, WOL & WOR, in the legacy mode.

Table 11: Supported Wake Events

| Wake Event | Support Wake Events | Support Via Legacy Wake |
|---|---|-------------------------|
| Power Button | Always wakes system. The Power Button can be configurable to different functions under the ACPI mode. | Always wakes system |
| Ring indicate from COM-A | Wakeup from S4/S5 if the system in the S4/S5 state | Yes |
| Ring indicate from COM-B | Wake up from S4/S5 if system in the S4/S5 state If COM-B is used for emergency management port, COM-B wakeup is disabled. | Yes |
| PME (Power Management Event) from PCI cards | May support wake from S4/S5 if PCI card supports the PME generation function. | Yes |
| RTC Alarm | Always wakes the system up from S4. | Yes |

6.3.2.1 Front Panel Switches

The BIOS supports up to three front panel buttons: the power button, the reset button, and the NMI button. The NMI button is not accessible on all front panel designs.

The power switch behaves differently depending on whether the operating system supports ACPI. If the operating system supports ACPI the power button can be configured as a sleep button via OS power management option. The OS causes the system to transition to the appropriate system state depending on the user settings.

6.3.2.1.1 Power Switch Off to On

The chipset may be configured to generate wake up events for several system events: Wake-on-LAN, PCI Power Management Interrupt, and the Real-Time Clock Alarm are examples of these events. If the operating system is ACPI-aware, it programs the wake sources before shutdown. In non-ACPI mode, the BIOS performs the configuration. A transition from power switch results in the SIO W83627 signal the ICH3 starting the power-up sequence. Since the processors are not executing, the BIOS does not participate in this sequence. The hardware receives power good and reset signal then transition to an ON state.

6.3.2.1.2 On to Off (Legacy)

The SIO is configured to generate an SMI due to a power button event. The BIOS services this SMI and sets the state of the machine in the chipset to the OFF state, then de-asserts the PS.

6.3.2.1.3 On to Off (ACPI)

If an ACPI operating system is loaded, the power button switch generates a request via SCI to the OS to shutdown the system. The OS retains control of the system and OS policy determines the sleep state, if any, into which the system transitions.

6.3.2.1.4 On to Sleep (ACPI)

If an ACPI operating system is loaded and the power button is configured as a sleep button, the sleep button switch generates a request via SCI to the OS to place the system into sleep mode. The OS retains control of the system and OS policy determines the sleep state, if any, into which the system transitions.

6.3.2.1.5 Sleep to On (ACPI)

If an ACPI operating system is loaded and the power button is configured as a sleep button, the sleep button switch generates a wake event to the ACPI chipset and a request via SCI to the OS to place the system in the On state. The OS retains control of the system and OS policy determines the sleep state, if any, and the sleep sources from which the system can wake.

6.3.3 Wired For Management (WFM)

Wired for Management (WFM) is an industry-wide initiative to increase overall manageability and reduce the total cost of ownership. WFM allows a server to be managed over a network. The system BIOS supports revision 2.0 of the *Wired For Management Baseline Specification*. It also supports the pre-boot execution environment, as outlined in the WFM baseline specification, if the system includes an embedded WFM compliant network device.

The system BIOS supports version 2.3.1 of the *System Management BIOS Reference Specification* to help higher-level instrumentation software meet the WFM requirements. The higher level software can use the information provided by the system management (SM)BIOS to instrument desktop management interface (DMI) standard groups that are specified in the WFM specification.

The BIOS also configures the SYSID table as described in the *Network PC System Design Guidelines, Revision 1.0*. This table contains the globally unique ID (GUID) of the baseboard. The mechanism that sets the GUID in the factory is defined in the *SYSID BIOS Support Interface Requirement Specification, Version 1.2*. The caller must provide the correct security key for this call to succeed.

When in S4/S5 mode, PCI device can use PME# signal to wake up the machine. It is an essential element in ACPI.

6.3.3.1 PXE BIOS Support

This section discusses host system BIOS support required for PXE compliance and how PXE boot devices (ROMs) and PXE Network Boot Programs (NBPs) use it.

6.3.3.2 BIOS Requirements

PXE-compliant BIOS implementations must:

- Locate and configure all PXE-capable boot devices (UNDI Option ROMs) in the system, both built-in and add-ins.
- Supply a PXE according to this specification if the system includes a built-in network device.
- Implement the following specifications:
 - Plug-and-Play BIOS Specification v1.0a or later.
 - System Management BIOS (SMBIOS) Reference Specification v2.2 or later.
 - The requirements defined in Sections 3 and 4 of the BIOS Boot Specification (BBS) v1.01 or later, to support network adapters as boot devices.
 - Supply a valid UUID and Wake-up Source value for the system via the SMBIOS structure table.

6.3.3.3 BIOS Recommendations

To be PXE 2.1-compliant the BIOS should implement the following:

- *POST Memory Manager Specification v1.01* or later is strongly recommended. PMM provides a straightforward way for LAN on Motherboard PXE implementations to move their ROM image from UMB to extended memory. While methods to do this exist outside of PMM, their use is undefined and unreliable. Placing PXE ROM images into UMB space reduces the available UMB space by approximately 32 KB. This is sufficient to compromise or even prevent successful operation of some downloaded programs

The Server Board SE7500CW2 is compliant with PXE 2.1. It implements the *Post Memory Manager Specification v1.01*.

6.3.4 Console Redirection

The BIOS supports redirection of both video and keyboard via a serial link (COM 1 or COM 2). When console redirection is enabled, the local (host server) keyboard input and video output are passed both to the local keyboard and video connections, and to the remote console via the serial link. Keyboard inputs from both sources are valid and video is displayed to both outputs. As an option, the system can be operated without a keyboard or monitor attached to the host system and run entirely from the remote console. Setup and any other text-based utilities can be accessed through console redirection.

6.3.4.1 Operation

When redirecting the console through a modem as opposed to a null modem cable, the modem needs to be configured with the following:

- Auto-answer (for example, ATSO=2, to answer after two rings).
- Modem reaction to DTR set to return to command state (e.g., AT&D1). Failure to provide this results in the modem either dropping the link when the server reboots (as in AT&D0) or becoming unresponsive to server baud rate changes (as in AT&D2).
- The BIOS Setup option for handshaking must be set to CTS.

Console redirection is exclusive with Logo display which is determined by the configuration menu "Boot-time Diagnostic Screen", When "Boot time Diagnostic Screen" is enabled, the Console redirection is enabled. On the contrary, when the "Boot time Diagnostic Screen" is disabled, the console re-direction is disabled and the logo screen is used instead.

6.3.4.2 Keystroke Mappings

Phoenix* based BIOS uses a serial port interrupt to send the Video RAM data to remote console and receive the remote input. When the data is received from the remote site by serial port, it will be put into the KB buffer by int16 to simulate it comes from the local KB by INT9.

During console redirection, the remote terminal sends keystrokes to the local server. The remote terminal may be a dumb terminal or a system with a modem running a communication program, such as ProComm*. The local server passes video back over the same link.

For keys that have an ASCII mapping, such as A and Ctrl-A, the remote terminal sends the ASCII character. For keys that do not have an ASCII mapping, such as F1 and Alt-A, the remote must send a string of characters, as defined in the tables below. The strings are based on the ANSI terminal standard. Since the ANSI terminal standard does not define all keys on the standard 101 key U.S. keyboard, mappings for these keys were created, such as F5 – F12, Page Up, and Page Down.

Alt key combinations are created by sending the combination `^[]` followed by the character to be modified. Once this Alt key combination is sent, the next keystroke is translated into its Alt key mapping. In other words, if `^[]` is mapped to Shift-F1, then pressing Shift-F1 followed by the letter 'a' would send an Alt-a to the server.

The remote terminal can force a refresh of its video by sending `^[{`. Combinations outside of the ANSI mapping and not listed in the table below are not supported.

Table 12: Non-ASCII Key Mappings

| Key | Normal | Shift | Ctrl | Alt | Key | Normal | Shift | Ctrl | Alt |
|--------------|-------------------|-------|------|-----|-------------|--------------------|-------|------|-----|
| ESC | <code>^[</code> | NS | NS | NS | Scroll Lock | NS | NS | NS | NS |
| F1 | <code>^[OP</code> | NS | NS | NS | Pause | NS | NS | NS | NS |
| F2 | <code>^[OQ</code> | NS | NS | NS | Insert | <code>^[[L</code> | NS | NS | NS |
| F3 | <code>^[OR</code> | NS | NS | NS | Delete | (7Fh) | NS | NS | NS |
| F4 | <code>^[OS</code> | NS | NS | NS | Home | <code>^[[H</code> | NS | NS | NS |
| F5 | <code>^[OT</code> | NS | NS | NS | End | <code>^[[K</code> | NS | NS | NS |
| F6 | <code>^[OU</code> | NS | NS | NS | Pg Up | <code>^[[M</code> | NS | NS | NS |
| F7 | <code>^[OV</code> | NS | NS | NS | Pg Down | <code>^[[2J</code> | NS | NS | NS |
| F8 | <code>^[OW</code> | NS | NS | NS | Up Arrow | <code>^[[A</code> | NS | NS | NS |
| F9 | <code>^[OX</code> | NS | NS | NS | Down Arrow | <code>^[[B</code> | NS | NS | NS |
| F10 | <code>^[OY</code> | NS | NS | NS | Right Arrow | <code>^[[C</code> | NS | NS | NS |
| F11 | <code>^[OZ</code> | NS | NS | NS | Left Arrow | <code>^[[D</code> | NS | NS | NS |
| F12 | <code>^[O1</code> | NS | NS | NS | Tab | (09h) | NS | NS | NS |
| Print Screen | NS | NS | NS | NS | | | | | |

NS = Not supported, (xxh) = ASCII character xx

Table 13: ASCII Key Mappings

| Key | Normal | Shift | Ctrl | Alt |
|----------------|--------|-----------|----------------|--------------------|
| Backspace | (08h) | (08h) | (7Fh) | ^ [] (08h) |
| (accent) ` | ` | (tilde) ~ | NS | ^ [] ` |
| 1 | 1 | ! | NS | ^ [] 1 |
| 2 | 2 | @ | NS | ^ [] 2 |
| 3 | 3 | # | NS | ^ [] 3 |
| 4 | 4 | \$ | NS | ^ [] 4 |
| 5 | 5 | % | NS | ^ [] 5 |
| 6 | 6 | ^ | NS | ^ [] 6 |
| 7 | 7 | & | NS | ^ [] 7 |
| 8 | 8 | * | NS | ^ [] 8 |
| 9 | 9 | (| NS | ^ [] 9 |
| 0 | 0 |) | NS | ^ [] 0 |
| (dash) - | - | (under) _ | (1Fh) | ^ [] - |
| = | = | + | NS | ^ [] = |
| a to z | a to z | A to Z | (01h) to (1Ah) | ^ [] a to ^ [] z |
| [| [| { | (1Bh) | ^ [] [|
|] |] | } | (1Dh) | ^ []] |
| \ | \ | | (1Ch) | ^ [] \ |
| (semi-colon) ; | ; | (colon) : | NS | ^ [] ; |
| (apostrophe) ' | ' | (quote) " | NS | ^ [] ' |
| (comma) , | , | < | NS | ^ [] , |
| (period) . | . | > | NS | ^ [] . |
| / | / | ? | NS | ^ [] / |
| (space) | (20h) | (20h) | (20h) | ^ [] (20h) |

NS = not supported, (xxh) = ASCII character xx

6.3.4.3 Limitations

Console redirection is a real-mode BIOS extension. It does not operate outside of real mode. In addition, console redirection will not function if the OS or a driver, such as EMM386*, takes the processor into protected mode. If an application moves the processor in and out of protected mode, it should inhibit redirection before entering protected mode and restart redirection when it returns to real mode.

Scanning and sending changes in text video memory redirect video. Therefore, console redirection is unable to redirect video in graphics mode. Since the BIOS scans the text video memory, an additional limitation exists if the system does not contain a video graphics adapter or a proprietary means of buffering the video memory. The BIOS may not have a method to send changes in text video memory if an application such as an option ROM writes directly to video memory.

Phoenix* BIOS uses the serial port interrupt to send the Video RAM data to remote console and receive the remote input. When the data receive from the Remote site by serial port, it will be put into the KB buffer by int16 to simulate it comes from the local KB by INT9.

Software that bypasses this handler does not receive redirected keystrokes.

6.3.5 Serial Ports

The Server Board SE7500CW2 has two serial ports, an internal 9-pin header for COM2, and an external COM1 serial port that can be used. Refer to sections 3.3 and 8.13 for additional serial port information.

6.3.6 System Management BIOS (SMBIOS)

This section references the System Management BIOS Reference Specification, Version 2.3.1.

The *Desktop Management Interface Specification* and its companion, the *DMTF Systems Standard Groups Definition*, define "...manageable attributes that are expected to be supported by DMI-enabled computer systems." Many of these attributes do not have a standard interface to the management software, but are known by the system BIOS. The system BIOS provides this interface via data structures through which system attributes are reported.

The system administrator can use SMBIOS to obtain the types, capabilities, operational status, installation date, and other information about the system components. The Server Board SE7500CW2 BIOS provides the SMBIOS structures via a table-based method. The table convention, provided as an alternative to the calling interface, allows the SMBIOS structures to be accessed under 32-bit protected-mode operating systems such as Windows 2000. This convention provides a searchable entry-point structure that contains a pointer to the packed SMBIOS structures residing somewhere in 32-bit physical address space. The SMBIOS entry-point structure described below can be located by application software by searching for the anchor-string on paragraph (16-byte) boundaries within the physical memory address range 000F0000h to 000FFFFFFh. This entry point encapsulates an intermediate anchor string, which is used by some existing browsers.

The total number of structures can be obtained from the SMBIOS entry-point structure. The system information is presented to an application as a set of structures that are obtained by traversing the SMBIOS structure table referenced by the SMBIOS entry-point structure. The following table describes the types of SMBIOS structures supported by the system BIOS.

Table 14: SMBIOS Header Structure

| Structure Type | Supported | Comments |
|--|-----------|--|
| BIOS Information (Type 0) | Yes | One record for the system BIOS. SMBIOS 2.3 does not allow the use of type 0 records to describe the option ROMs. The system BIOS version string is described in Section 1.1 |
| System Information (Type 1) | Yes | |
| Baseboard Information (Type 2) | Yes | |
| Chassis Information (Type 3) | Yes | |
| Processor Information (Type 4) | Yes | One for every processor slot. |
| Memory Controller Information (Type 5) | No | Browsers should use Type 16 records. |
| Memory Module Information (Type 6) | No | Browsers should use Type 17 records. |
| Cache Information (Type 7) | Yes | Two records for every processor. One record describes L1 cache and the second one describes L2 cache. The disabled bit in the cache configuration field is set if the corresponding processor is absent or disabled. |
| Port Connector Information (Type 8) | Yes | Describes the baseboard connectors including IDE, floppy, keyboard, mouse, COM ports, and parallel port. |

| | | |
|--|-----|--|
| System Slots (Type 9) | Yes | One record for each PCI slot. The number of PCI slots is determined by a supported 1U or 2U chassis part number. |
| On-board Device Configuration (Type 10) | Yes | One for each on-board device, like video controller etc. |
| OEM Strings (Type 11) | Yes | From OEM GPNV area. |
| System Configuration Options (Type 12) | Yes | Describes the baseboard jumper settings. |
| BIOS Language Information (Type 13) | Yes | |
| Group Association (Type 14) | No | None required. |
| Physical Memory Array (Type 16) | Yes | |
| Memory Device (Type 17) | Yes | One record for each memory device slot, six total. |
| Memory Error Information (Type 18) | No | Much more extensive information available in the system event log. |
| Memory Array Mapped Addresses (Type 19) | Yes | |
| Memory Device Mapped Addresses (Type 20) | Yes | |
| Built-in Pointing Devices (Type 21) | No | Applies only to mobile platforms. |
| Portable Battery (Type 22) | No | Applies only to mobile platforms. |
| System Reset (Type 23) | No | |
| Hardware Security (Type 24) | Yes | |
| Out-of-band Remote Access (Type 30) | No | |
| System Boot Information (Type 32) | Yes | |
| Structure Not In Effect (Type 126) | Yes | Indicates software should ignore this structure. These structures may be present. |
| End of Table (Type 127) | Yes | Structure indicating end of table. |

6.3.7 Windows Compatibility

The Server Board SE7500CW2 is compliant with the *Hardware Design Guide v3.0*.

The Hardware Design Guide (HDG) for a Windows* NT* platform is intended for systems that are designed to work with Windows NT class operating systems. Each specification classifies the systems further and has different requirements based on the intended usage for that system. For example, a server system used in small home/office environments has different requirements than one which is used for enterprise applications.

The Server Board SE7500CW2 server BIOS meets the applicable requirements as specified in version 3.0 of the HDG specification.

6.3.7.1 Quiet Boot

Version 3.0 of the Hardware Design Guide for Windows NT requires that the BIOS provide minimal startup display during BIOS POST. The system start-up must only draw the user's attention in case of errors or when there is a need for user interaction. By default, the system must be configured so the screen display does not display memory counts, device status, etc, but presents a "clean" BIOS start-up. The only screen display allowed is the OEM splash screen, which can include information such as copyright notices.

The Server Board SE7500CW2 server BIOS supports the <ESC> and <F2> hot-keys during POST, giving the user the ability temporarily disable the splash screen to view all diagnostic and initialization messages for the current boot. The splash screen can be disabled for all subsequent boot up sequences by going into the BIOS setup utility and disabling the "Boot Time

Diagnostic Screen” option under Advanced screen and it should be disabled when using BIOS console redirection, since it cannot redirect the video if configured for graphics mode.

The BIOS may temporarily remove the splash screen when the user is prompted for a password during POST. The BIOS also allows an OEM to override the standard Intel splash screen with a custom one. The OEM logo replacing procedure is below.

Step 1: Download the logo update package from support at <http://support.intel.com>.

Step 2: Create a logo for your company. The logo may be no more that 16 colors from the 16-color palette. Refer to the instructions included with the update utility for exact limitations.

Step 3: Execute the oemlogo.exe file downloaded from the support site to extract the content to a diskette. The diskette will include 3.bat, B2P.exe, checkBMP.exe, Logoupd.exe and Logoupd.txt.

Step 4: Make the diskette bootable and boot to it.

Step 5: Execute the command “3.bat Filename.bmp” where Filename.bmp is your custom logo.

Note: All files must be in the same directory, and you must be working in a pure DOS environment.

The BIOS maintains the splash screen during option ROM initialization. Since option ROMs expect the video to be in text mode, the BIOS emulates text mode.

6.4 BIOS Serviceability Features

The CMOS configuration RAM may be reset by two methods:

1. The CMOS clear jumper located on the baseboard at jumper J106. The CMOS clear can also be set to a default setting through the BIOS Setup.

There are 5 steps involved to clear the CMOS by CMOS clear Jumper:

- 1) Power off the system
 - 2) Plug the jumper from pins 9 & 10 (storage location) onto pins 5 & 6 of J106 and power on the system
 - 3) Power the system off once it begins beeping
 - 4) Replace the jumper onto pins 9 & 10
 - 5) Power on the system
2. It will automatically be reset if it becomes corrupted.

When the BIOS detects a CMOS clear request, CMOS defaults are loaded during POST sequence. Note that non-volatile storage for embedded devices may or may not be affected by the clear CMOS operation, depending on the available hardware support. The system must be rebooted without the CMOS clear jumper being in the “clear”.

Note: If the jumper is not removed and the machine is powered on, then the BIOS fail with 3 long beeps, wait 3 seconds, and then repeat the cycle.

6.4.1 Flash Update Utility

The Flash Memory Update utility (Phlash.exe) loads a fresh copy of the BIOS into flash ROM. The loaded code and data include the following:

- On-board video BIOS, ATA-100 RAID BIOS, and PXE option ROMs for the devices embedded on the system board
- The Setup utility
- The System BIOS.

Note: The Phlash utility must be run without the presence of a 386 protected mode control program, such as Windows or EMM386*. Phlash uses the processor's flat addressing mode to update the Flash component.

6.4.1.1 Loading the System BIOS

The release will include following files :

| | |
|--------------|-----------------------------------|
| BIOS.ROM | - 512KB/1MB BIOS ROM Image |
| PHLASH.EXE | - Phlash Utility |
| 1.BAT | - Batch file for the phlash ROM |
| 2.BAT | - Batch file for the phlash ROM |
| Autoexec.bat | - Calls options.bat |
| Platform.bin | - Flash configuration file |
| Oemphl.exe | - Phlash Utility |
| Options.bat | - Runs the BIOS update procedure. |

The BIOS update procedure is as follows:

- 1) Create a bootable DOS diskette (i.e. format /u /s A:)
- 2) Execute the "BIOS.EXE a:" command at a DOS prompt which will copy the 1.bat, 2.bat, autoexec.bat, options.bat, phlash.exe, platform.bin, oemphl.exe and update BIOS.rom to a 1.44 bootable floppy diskette.
- 3) Boot from the BIOS bootable diskette created in step 2.
- 4) Two options should appear on the screen.
 - a) Type <1> and press <enter> to automatically update the System BIOS. Refer to steps 5 thru 7.
 - b) Type <2> and press <enter> to manually update the System BIOS. Refer to steps 8 thru 13.
- 5) Execute A:> 1.bat
- 6) When BIOS phlash is over, it will show a message that indicates the update was successful and beep.
- 7) The machine will reboot automatically.
- 8) Execute A:> 2.bat
- 9) There are two ways to update Flash Memory or System BIOS.

- A) The first is to highlight the option that reads “Update Flash Memory from a File” and press <Enter>.
- B) At the screen that asks you to enter the name of the file select BIOS.ROM and press <Enter>.
- 10) The second is to highlight the option that reads “Update System BIOS” and press ENTER. The system will give you a warning that BIOS is about to be updated. Verify the BIOS version is correct and press <Enter> to continue.
- 11) Once the BIOS has been successfully loaded, remove the floppy diskette from the drive. Press ENTER at the prompt to reboot the system, or power off and power on.

Note: The BIOS DOS Boot disk must be a non-HIMEM management environment

BIOS flash updates all CMOS information with the exception of the baseboard, CMOS Custom Defaults and some SMBIOS items like serial number and product code.

6.4.1.2 Splash Screen Update

The baseboard includes an area in flash for implementation-specific OEM. Splash Screen update. With this functionality, user can update his/her own splash screen. See section 6.3.7.1 for more details.

6.4.1.3 BIOS Recovery Mode

If BIOS image is corrupt, or if an update to the system BIOS is not successful, or if the system fails to complete POST and is unable to boot an operating system, it may be necessary to run the BIOS recovery procedure.

Note: BIOS Recovery Mode supports onboard VGA Video.

There are 2 ways to enter the Recovery Mode – Automatic Detection Mode and Force Mode

- 1) Automatic Detection Recovery Mode:
 - a. Create a bootable BIOS recovery diskette from the crisis.zip file available on the <http://support.intel.com> website for the Server Board SE7500CW2 board.
 - b. Insert the BIOS recovery floppy into the diskette drive.
 - c. Reboot the system.
 - d. At this point you will hear one long beep followed by two short beeps.
 - e. The beeping sequence will repeat while BIOS attempts to read the recovery diskette.
 - f. Follow any instructions from the recovery diskette. If successful the recovery diskette will notify you when completed.

2) Force Recovery Mode:

- a. Shutdown the system and unplug the power cable.
- b. Insert the jumper into pin 3-4 of the J106 connector on the baseboard. This connector is near the onboard NICs. Refer to the Quick Start Guide if you need further assistance locating it.
- c. Insert recovery diskette into the floppy diskette drive. (See step “a” above under “Automatic Detection Recovery Mode” for details on creating the recovery diskette.)
- d. Plug in the power cable and power on system.
- e. System will beep during recovery.
- f. Once you hear two high-pitched beeps the recovery is considered successful. Otherwise, if the recovery is unsuccessful you will hear a series of short beeps. The whole process will take 2-4 minutes to complete.
- g. Power off and unplug the system.
- h. Remove the jumper from J106 pin 3-4 on the motherboard.
- i. Plug in the power cord and power the system on.

6.5 BIOS and BIOS Setup

BIOS embeds a set-up utility to configure BIOS and system resources. On-board devices are configured with the BIOS Setup utility that is embedded in flash ROM. BIOS Setup provides enough configuration functionality to boot an operating system image.

The configuration utilities allow the user to modify the CMOS RAM and NVRAM. The actual hardware configuration is accomplished by the BIOS POST routines and the BIOS Plug-N-Play auto-configuration manager. The configuration utilities update a checksum for both areas, so potential data corruption is detected by the BIOS before the hardware configuration is saved. If the data is corrupted, the BIOS request that the user reconfigure the system and reboot.

6.5.1 BIOS Setup Utility

This section describes the ROM-resident setup utility that provides the means to configure the platform. The BIOS Setup utility is part of the system BIOS and allows limited control over on-board resources.

The user can disable embedded PCI devices through the setup menus. When these devices are disabled through setup, their resources are freed.

The following embedded devices can be disabled through setup menus, making them invisible to a plug-and-play operating system that scans the PCI bus:

- Embedded video ATI Rage
- Each embedded NIC (2) 82550
- Embedded ATA RAID

Note: the BIOS options described in this section may or may not be present in pre-production versions of the system BIOS. This section describes the BIOS utility as it is planned to be at production and is subject to change. Option locations, in a given menu of the BIOS Setup utility as described in this section, may be different from those observed on any one pre-production version of the system BIOS.

The BIOS Setup utility screen is divided into four functional areas. Table 15 describes each area:

Table 15: Setup Utility Screen

| Functional Area | Description |
|---------------------------|--|
| Keyboard Command Bar | Located at the bottom of the screen or as part of the help screen. This bar displays the keyboard commands supported by the setup utility. |
| Menu Selection Bar | Located at the top of the screen. Displays the various major menu selections available to the user. The Server Setup utility major menus are: Main Menu, Advanced Menu, Security Menu, Boot Menu, System Menu and the Exit Menu. |
| Options Menu | Each Option Menu occupies the left and center sections of the screen. Each menu contains a set of features. Selecting certain features within a major Option Menu drops you into sub-menus. |
| Item Specific Help Screen | An item-specific Help screen is located at the right side of the screen . |

6.5.2 Entering the BIOS Setup Utility

During the BIOS POST operation, the user is prompted to use the F2 function key to enter Setup as follows:

Press <F2> to enter Setup

A few seconds might pass before Setup is entered. This is the result of POST completing test and initialization functions that must be completed before Setup can be entered. When Setup is entered, the Main Menu options page is displayed.

6.5.3 Keyboard Command Bar

The bottom portion of the Setup screen provides a list of commands that are used to navigate through the Setup utility. These commands are displayed at all times.

Each menu page contains a number of configurable options and/or informational fields. Depending on the level of security in affect, configurable options may or may not be changed. If an option cannot be changed due to the security level, its selection field is made inaccessible.

The Keyboard Command Bar supports the following:

Table 16: Keyboard Commands

| Key | Option | Description | | | | | | |
|--|-----------------|---|---------------------------|--|--|--|--------------|-------------|
| Enter | Execute Command | The Enter key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected option has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu. | | | | | | |
| ESC | Exit | The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered. When the ESC key is pressed in any sub-menu, the parent menu is re-entered. When the ESC key is pressed in any major menu, the exit confirmation window is displayed and the user is asked whether changes can be discarded. If "No" is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before ESC was pressed without affecting any existing settings. If "Yes" is selected and the Enter key is pressed, Setup is exited and the BIOS continues with POST. | | | | | | |
| ↑ | Select Item | The up arrow is used to select the previous value in a pick list, or the previous options in a menu item's option list. The selected item must then be activated by pressing the Enter key. | | | | | | |
| ↓ | Select Item | The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the Enter key. | | | | | | |
| ←→ | Select Menu | The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed. | | | | | | |
| Tab | Select Field | The Tab key is used to move between fields. For example, Tab can be used to move from hours to minutes in the time item in the main menu. | | | | | | |
| - | Change Value | The minus key on the keypad is used to change the value of the current item to the previous value. This key scrolls through the values in the associated pick list without displaying the full list. | | | | | | |
| + | Change Value | The plus key on the keypad is used to change the value of the current menu item to the next value. This key scrolls through the values in the associated pick list without displaying the full list. On 106-key Japanese keyboards, the plus key has a different scan code than the plus key on the other keyboard, but will have the same effect | | | | | | |
| F9 | Setup Defaults | Pressing F9 causes the following to appear: <table border="1" data-bbox="516 1318 1312 1432"> <tr> <td colspan="2" style="text-align: center;">Setup Confirmation</td> </tr> <tr> <td colspan="2" style="text-align: center;">Load default configuration now?</td> </tr> <tr> <td style="text-align: center;">[Yes]</td> <td style="text-align: center;">[No]</td> </tr> </table> If "Yes" is selected and the Enter key is pressed, all Setup fields are set to their default values. If "No" is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before F9 was pressed without affecting any existing field values | Setup Confirmation | | Load default configuration now? | | [Yes] | [No] |
| Setup Confirmation | | | | | | | | |
| Load default configuration now? | | | | | | | | |
| [Yes] | [No] | | | | | | | |

| | | | | | | | | |
|---|---------------|--|---------------------------|--|---|--|--------------|-------------|
| F10 | Save and Exit | <p>Pressing F10 causes the following message to appear:</p> <table border="1" data-bbox="516 262 1312 373"> <tr> <td colspan="2" style="text-align: center;">Setup Confirmation</td> </tr> <tr> <td colspan="2" style="text-align: center;">Save Configuration changes and exit now?</td> </tr> <tr> <td style="text-align: center;">[Yes]</td> <td style="text-align: center;">[No]</td> </tr> </table> <p>If “Yes” is selected and the Enter key is pressed, all changes are saved and Setup is exited. If “No” is selected and the Enter key is pressed, or the ESC key is pressed, the user is returned to where they were before F10 was pressed without affecting any existing values.</p> | Setup Confirmation | | Save Configuration changes and exit now? | | [Yes] | [No] |
| Setup Confirmation | | | | | | | | |
| Save Configuration changes and exit now? | | | | | | | | |
| [Yes] | [No] | | | | | | | |

6.5.4 Menu Selection Bar

The Menu Selection Bar is located at the top of the screen and displays the major menu selections available to the user. The menu bar is shown below.

| | | | | | | |
|------|----------|----------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
|------|----------|----------|-------|------|--------|------|

Table 17: Menu Selection Bar

| Main | Advanced | Security | Power | Boot | System | Exit |
|---|--|---|--|--|---|--|
| Allocates resources for hardware components | Configures advanced features available through the chipset | Sets and clears passwords and security features | Allows system to disable ACPI reboot and disable power button. | Selects boot options and power supply controls | Information on vendor, processor, memory, peripherals, and BIOS | Saves or discards changes to Setup program options |

6.5.5 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

| | | | | | | |
|------------------|----------|----------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
| Primary Master | | | | | | |
| Primary Slave | | | | | | |
| Secondary Master | | | | | | |
| Secondary Slave | | | | | | |

Table 18: Main Menu

| Feature | Choices | Description |
|-------------------|---|--|
| System Time | HH:MM:SS | Sets the system time (hour, minutes, seconds, on a 24-hour clock). |
| System Date | MM/DD/YYYY | Sets the system date (month, day, year). |
| Legacy Diskette A | Not installed 1.44MB, 3 1/2" (default) 2.88MB 3 1/2" | Selects the diskette type. Japanese media format. To support this type of media format requires a 3.5-inch, 3-mode diskette drive. |
| Primary Master | Select to display submenu | Displays IDE device selection. |
| Primary Slave | Select to display submenu | Displays IDE device selection. |
| Secondary Master | Select to display submenu | Displays IDE device selection. |
| Secondary Slave | Select to display submenu | Displays IDE device selection. |

6.5.5.1 Primary/Secondary, Master/Slave Submenus

To access this sub-menu select Main on the menu bar and then the master or slave to be configured.

| | | | | | | |
|-------------------------|----------|----------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
| Primary Master | | | | | | |
| Primary Slave | | | | | | |
| Secondary Master | | | | | | |
| Secondary Slave | | | | | | |

There are four IDE submenus: primary master, primary slave, secondary master, and secondary slave. Table 19 shows the format of the IDE submenus. For brevity, only one example is shown.

Table 19: Primary/Secondary, Master/Slave Submenu

| Feature | Choices | Description |
|------------------------|-------------------------------|---|
| Type | No options | Automatically detects the type of IDE device installed. 1-39 = |
| Multi-Sector Transfers | No options | Specifies the number of sectors that are transferred per block during multiple sector transfers. This option is disabled by default. |
| LBA Mode Control | No options | Enables Large Block Addressing (LBA) instead of cylinder, head, sector addressing. This option is disabled by default. |
| 32 Bit I/O | Disabled (default) Enabled | Enables 32-bit IDE data transfers. |
| Transfer Mode | No options | Selects the method of moving data to and from the hard drive. Automatically set to <i>Standard</i> , which selects the optimum transfer mode. |
| Ultra DMA Mode | Disabled Enabled (default) | Enables Ultra DMA mode. |

6.5.6 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

| | | | | | | |
|------|--------------------------|----------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
| | I/O Device Configuration | | | | | |
| | On Board Device | | | | | |
| | PCI Configuration | | | | | |
| | Server Menu | | | | | |
| | Console Redirection | | | | | |
| | Event Logging | | | | | |
| | Hardware Monitor | | | | | |

Table 20 list the selections available on the Advanced menu. This menu configures advanced features available through the chipset.

Table 20: Advanced Menu

| Feature | Choices | Description |
|-----------------------------|--|--|
| I/O Device Configuration | Select to display submenu | Configures the I/O ports. |
| On Board Device | Select to display submenu | Configures the onboard RAID, network, and USB controllers. |
| PCI Configuration | Select to display submenu | Configures the onboard PCI or RAID devices. |
| Server Menu | Select to display submenu | Sets options for server features. |
| Console Redirection | Select to display submenu | Provides additional options to configure the console |
| Event Logging | Select to display submenu | Displays the event logs. |
| Hardware Monitor | Select to display submenu | Displays voltages, temperatures, and fan speeds for the system. |
| Installed O/S | Win2000/.NET (default) NT4 Other | Specifies the operating system installed on your system that you will use most often. An incorrect setting can cause some operating systems to behave erratically. Note: If you select <i>NT4</i> , an additional submenu item, <i>NT4 Installation Workaround</i> , will appear. It is disabled by default. To install Windows NT 4.0, you need to change the <i>NT4 Installation Workaround</i> option to <i>Enabled</i> . Disable it to install pertinent service packs. |
| Boot-time Diagnostic Screen | Enabled Disabled (default) | Enables or disables the boot-time diagnostic screen. <i>Disabled</i> will display the splash screen over the diagnostic screen. This splash screen can be changed to show and OEM based logo. |
| Reset Configuration Data | No (default) Yes | Specifies if the extended server configuration data will be reset during the next boot. Yes clears the extended server configuration data during the next boot. The system automatically resets this field to <i>No</i> during the next boot. |

| Feature | Choices | Description |
|------------------------|---|---|
| Large Disk Access Mode | Other DOS (default) | UNIX†, NetWare†, and other operating systems require this option be set to <i>Other</i> . If you install an operating system and the hard drive fails to install, change this setting and try again. Different operating systems require different representations of drive geometries. |
| PS/2 Mouse | Disabled Enabled Auto Detect (default) | Configures the PS/2 mouse. <i>Disabled</i> prevents any installed PS/2 mouse from functioning but frees up IRQ 12, <i>Enabled</i> forces the PS/2 mouse port to be enabled even if a mouse is not present. <i>Auto Detect</i> will enable the PS/2 mouse only if one is present. |
| Summary Screen | Disabled Enabled (default) | Enables or disables the boot-time hardware/BIOS summary screen. |
| Legacy USB Support | Disabled Enabled (default) | Enables support for legacy USB. May be necessary to “Disable” in order to install NetWare 6.0 SP1. |
| PXE Support | Disabled (default) NIC2 NIC1 | Enables support for onboard PXE. |
| Hyper-Threading | Disabled Enabled (default) | Allows Intel Xeon processors to run in hyper-threading mode. Enabling this setting will improve throughput significantly on certain applications. |

6.5.6.1 I/O Device Configuration Submenu

To access this submenu, select Advanced on the menu bar at the top of the screen and then I/O Device Configuration.

| | | | | | | |
|------|---------------------------------|----------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
| | I/O Device Configuration | | | | | |
| | On Board Device | | | | | |
| | PCI Configuration | | | | | |
| | Server Menu | | | | | |
| | Console Redirection | | | | | |
| | Event Logging | | | | | |
| | Hardware Monitor | | | | | |

Table 21 lists the options available through the I/O Device Configuration submenu. This submenu configures the I/O ports on the board.

Table 21: I/O Device Configuration Submenu

| Feature | Choices | Description |
|---|---|---|
| Serial port A | Disabled Enabled (default) | Enables or disables serial port A. Two devices cannot share the same IRQ. Choosing <i>Disabled</i> makes serial port A unusable. |
| Base I/O Address (This feature is present only when Serial Port A is set to enabled) | 3F8 (default) 2F8 3E8 2E8 | Sets the base I/O address for serial port A. |
| Interrupt (This feature is present only when Serial Port A is set to enabled) | IRQ3 IRQ4 (default) | Sets the interrupt for serial port A. |
| Serial port B | Disabled Enabled (default) | Enables or disables onboard serial port 2. Two devices cannot share the same IRQ. Choosing <i>Disabled</i> makes serial port B unusable. |
| Base I/O Address (This feature is present only when Serial Port B is set to enabled) | 3F8 2F8 (default) 3E8 2E8 | Sets the base I/O address for serial port B. |
| Interrupt (This feature is present only when Serial Port B is set to enabled) | IRQ3 (default) IRQ4 | Sets the interrupt for serial port B. |
| Parallel port | Disabled Enabled (default) | Enables or disables the onboard parallel port. Two devices cannot share the same IRQ. Also, choosing <i>Disabled</i> makes the parallel port unusable. Auto is the recommended setting. |

| Feature | Choices | Description |
|---|--|--|
| Mode (This feature is present only when Parallel Port is set to enabled) | Output only Bi-directional EPP ECP (default) | Sets the mode for the parallel port. <i>Output only</i> is the standard printer connection mode. <i>Bi-directional</i> is the standard bidirectional mode. <i>EPP</i> is Enhanced Parallel Port mode, a high-speed bidirectional mode. Selection based on what EPP version the printer supports. Only choose a mode that the parallel port device (such as a printer) supports. Check the parallel port device documentation for this information. If this information cannot be located, use the default setting. <i>ECP</i> is Extended Capabilities Port mode, a high-speed bidirectional mode. |
| Base I/O Address (This feature is present only when Parallel Port is set to enabled) | 378 (default) 278 3BC | Sets the base I/O address for the parallel port. |
| Interrupt (This feature is present only when Parallel Port is set to enabled) | IRQ5 IRQ7 (default) | Sets the interrupt for the parallel port. |
| DMA channel (This feature is present only when Parallel Port is set to enabled) | DMA 1 DMA 3 (default) | Sets the DMA channel for the parallel port. |
| Floppy disk controller | Disabled Enabled (default) | Enables or disables the onboard diskette controller. |

6.5.6.2 On Board Device Submenu

To access this submenu, select Advanced on the menu bar at the top of the screen and then On Board Device.

| | | | | | | |
|------|--------------------------|----------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
| | I/O Device Configuration | | | | | |
| | On Board Device | | | | | |
| | PCI Configuration | | | | | |
| | Server Menu | | | | | |
| | Console Redirection | | | | | |
| | Event Logging | | | | | |
| | Hardware Monitor | | | | | |

Table 22 lists the options available through the On Board Device submenu. This submenu configures the RAID, network, and USB controllers on the board.

Table 22: On Board Device Submenu

| Feature | Choices or Display Only | Description |
|---------------|--------------------------------------|--|
| Onboard RAID | Disabled Enabled (default) | Enables the onboard PCI Promise PDC20267 controller. |
| Onboard NIC 1 | Disabled Enabled (default) | Enables the onboard PCI Intel 82550PM Controller (Device 5). |
| Onboard NIC 2 | Disabled Enabled (default) | Enables the onboard PCI Intel 82550PM Controller (Device 4). |
| Onboard USB | Disabled Enabled (default) | Enables the ICH3 USB controllers. |

6.5.6.3 PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar at the top of the screen and then PCI Configuration.

| Main | Advanced | Security | Power | Boot | System | Exit |
|------|--------------------------|----------|-------|------|--------|------|
| | I/O Device Configuration | | | | | |
| | On Board Device | | | | | |
| | PCI Configuration | | | | | |
| | Onboard RAID | | | | | |
| | PCI Device, Slot #1 | | | | | |
| | PCI Device, Slot #2 | | | | | |
| | PCI Device, Slot #3 | | | | | |
| | PCI Device, Slot #4 | | | | | |
| | PCI Device, Slot #5 | | | | | |
| | Server Menu | | | | | |
| | Console Redirection | | | | | |
| | Event Logging | | | | | |
| | Hardware Monitor | | | | | |

Table 23 lists the options available through the PCI Configuration submenu. This submenu configures the option ROM area for onboard RAID and PCI devices.

Table 23: PCI Configuration Submenu

| Feature | Choices or Display Only | Description |
|---------------------|---------------------------|--|
| Onboard RAID | Select to display submenu | Configures the onboard RAID option ROM area. |
| PCI Device, Slot #1 | Select to display submenu | Configures the specific PCI device expansion ROM.. |
| PCI Device, Slot #2 | Select to display submenu | Configures the specific PCI device expansion ROM.. |
| PCI Device, Slot #3 | Select to display submenu | Configures the specific PCI device expansion ROM.. |
| PCI Device, Slot #4 | Select to display submenu | Configures the specific PCI device expansion ROM.. |
| PCI Device, Slot #5 | Select to display submenu | Configures the specific PCI device expansion ROM.. |

Table 24 lists the options available on the Option ROM Scan submenu. This submenu appears for each of the options available on the Advanced PCI Configuration submenu above (see Table 23). For brevity, only one example is shown.

Table 24. Option ROM Scan Submenu

| Feature | Choices or Display Only | Description |
|-----------------|--------------------------------------|---------------------------------------|
| Option ROM Scan | Enabled (default) Disabled | Initializes the device expansion ROM. |

6.5.6.4 Server Menu Submenu

To access this submenu, select Advanced on the menu bar at the top of the screen and then Server Menu.

| Main | Advanced | Security | Power | Boot | System | Exit |
|------|--------------------------|----------|-------|------|--------|------|
| | I/O Device Configuration | | | | | |
| | On Board Device | | | | | |
| | PCI Configuration | | | | | |
| | Server Menu | | | | | |
| | Console Redirection | | | | | |
| | Event Logging | | | | | |
| | Hardware Monitor | | | | | |

Table 25 lists the options available through the Server Menu submenu. This submenu allows you to set options for server features.

Table 25: Server Menu Submenu

| Feature | Choices | Description |
|-------------|--------------------------------------|--|
| NMI on PERR | Disabled (default) Enabled | Enables or disables non-maskable interrupts (NMI) on parity errors on the PCI bus (PERRs). |
| NMI on SERR | Disabled Enabled (default) | Enables or disables NMI on system errors on the PCI bus (SERRs). |

6.5.6.5 Console Redirection Submenu

To access this submenu, select Advanced on the menu bar at the top of the screen and then Console Redirection.

| | | | | | | |
|------|----------------------------|----------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
| | I/O Device Configuration | | | | | |
| | On Board Device | | | | | |
| | PCI Configuration | | | | | |
| | Server Menu | | | | | |
| | Console Redirection | | | | | |
| | Event Logging | | | | | |
| | Hardware Monitor | | | | | |

Table 26 lists the options available through the Console Redirection submenu. This submenu provides additional options to configure the console.

Table 26: Console Redirection Submenu

| Feature | Choices | Description |
|--------------------------|---|--|
| COM Port Address | Disabled (default) On-board COM A On-board COM B | When enabled, console redirection uses the I/O port specified. All keyboard/mouse and video will be directed to this port. This setting is designed to be used only under DOS in text mode. |
| Baud Rate | 300 1200 2400 9600 19.2k (default) 38.4k 57.6K 115.2k | When console redirection is enabled, specifies the baud rate to be used. |
| Console Type | PC ANSI (default) VT100 | Enables the specified console type. |
| Flow Control | None XON/XOFF CTS/RTS (default) | <i>None</i> disallows flow control. XON/XOFF is software-based asynchronous flow control. CTS/RTS is hardware-based flow control. When EMP is sharing the COM port as console redirection, the flow control must be set to <i>CTS/RTS</i> . |
| Console Connection | Direct (default) Via modem | Indicates whether the console is connected directly to the system or whether a modem is used. |
| Continue C.R. after POST | Off (default) On | Enables console redirection (C.R.) after the operating system has been loaded. |

6.5.6.6 Event Logging Submenu

To access this submenu, select Advanced on the menu bar at the top of the screen and then Event Logging.

| | | | | | | |
|------|--------------------------|----------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
| | I/O Device Configuration | | | | | |
| | On Board Device | | | | | |
| | PCI Configuration | | | | | |
| | Server Menu | | | | | |
| | Console Redirection | | | | | |
| | Event Logging | | | | | |
| | Hardware Monitor | | | | | |

Table 27 lists the options available through the Event Logging submenu. This submenu allows you to view the event logs.

Table 27: Event Logging Submenu

| Feature | Choices | Description |
|----------------------|--------------------------------------|---|
| Event log validity | No options | Indicates if the contents of the event log are valid. |
| Event log capacity | No options | Indicates if there is space available in the event log. |
| View event log | <Enter> | Select <Enter> to display the current event log. Only SBE and MBE events are supported. No Windbond 83627HF Super-I/O information is available. |
| Event Logging | Disabled Enabled (default) | Enables logging of events. |
| ECC Event Logging | Disabled Enabled (default) | Enables logging of ECC events. |
| Clear all event logs | No (default) Yes | Clears the event log after booting. Must be set to Yes if the Event Log Validity option is invalid. |

6.5.6.7 Hardware Monitor Submenu

To access this submenu, select Advanced on the menu bar at the top of the screen and then Hardware Monitor.

| | | | | | | |
|------|--------------------------|----------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
| | I/O Device Configuration | | | | | |
| | On Board Device | | | | | |
| | PCI Configuration | | | | | |
| | Server Menu | | | | | |
| | Console Redirection | | | | | |
| | Event Logging | | | | | |
| | Hardware Monitor | | | | | |

Table 28 lists the options available in the Hardware Monitor submenu. This submenu displays temperature, voltages, and fan speeds for the onboard Super I/O Windbond* ASIC. Use the up and down arrow keys to scroll through the readings. Note: the exact values for each sensor will vary depending on electrical and environmental conditions.

Table 28: Hardware Monitor Submenu

| Feature | Choices | Description |
|------------------------------------|------------|-------------|
| | No options | |
| Hardware Monitor IO Base: 0295h | No options | |
| VCC_CPU_A =1.45V | | |
| +1_8V_A =1.79V | | |
| +C_CV_A =3.24V | | |
| AVCC =5.02V | | |
| +12V_A =11.59V | | |
| +12ENG_1 =12.01V | | |
| +2_5V_A =2.49V | | |
| AUX5V =4.94V | | |
| Vbat =2.92V | | |
| Ambiance =35c/95F | | |
| CPU1 =51C/123F | | |
| CPU2 =34C/93F | | |
| System FAN 1 speed=5260RPM | | |
| System FAN 2 speed=4560RPM | | |
| System FAN 3 speed=4560RPM | | |
| System FAN 4 speed=4560RPM | | |
| CPU FAN 1 speed =4560RPM | | |
| CPU FAN 2 speed =4560RPM | | |

6.5.7 Security Menu

To access this menu, select Security on the menu bar at the top of the screen.

| | | | | | | |
|------|----------|-----------------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
|------|----------|-----------------|-------|------|--------|------|

Table 29 lists the options available on the Security menu. Enabling the Supervisor Password field requires a password for entering Setup. The passwords are not case-sensitive.

Table 29: Security Menu

| If no password entered previously: | | |
|------------------------------------|--------------------------------------|--|
| Feature | Choices | Description |
| Set User Password | <Enter> | <p>The user password controls access to the system at boot. When the <Enter> key is pressed, you are prompted for a password; press the ESC key to abort.</p> <p>The supervisor password must be set if a user password is to be used.</p> <p>NOTE: Entering Setup with a supervisor password provides full access to all BIOS Setup utility menus.</p> |
| Set Supervisor Password | <Enter> | <p>The supervisor password controls access to the BIOS Setup utility. When the <Enter> key is pressed, you are prompted for a password; press the ESC key to abort.</p> <p>This password can be set only if a supervisor password is entered.</p> <p>When the user has entered his or her name but the supervisor is not logged in, only the following information is accessible:</p> <p>Supervisor password is set to <i>Enabled</i>.</p> <p>User password is set to <i>Enabled</i>.</p> <p>Set user password [press enter] to enter a user password.</p> <p>Password on boot is set to <i>Enabled/Disabled</i> (whichever is in effect). This option is not allowed to change.</p> |
| Password on boot | Disabled Enabled (default) | Requires password entry before boot. System will remain in secure mode until password is entered. If a user or supervisor password is not entered, the operating system cannot be accessed. |
| Diskette access | User (default) Supervisor | <p>Controls who can access diskette drives.</p> <p><i>Supervisor</i> limits access to the diskette drive to the supervisor, who must enter a password.</p> <p><i>User</i> allows access to the diskette drive by entering either the supervisor or the user password.</p> <p>Whatever setting is chosen, it becomes functional only if both a supervisor password and a user password have been set (if the User setting is chosen).</p> |

Note: This feature appears only if a user password has been set.

6.5.8 Power Menu

To access this menu, select Power on the menu bar at the top of the screen.

| | | | | | | |
|------|----------|----------|--------------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
|------|----------|----------|--------------|------|--------|------|

Table 30 lists the options available on the Power menu. This menu is designed to disable ACPI automatic reboot in the S0 or S4 states. If these submenus are enabled and AC power is lost, the server power and its operating system will remain off.

Table 30: Power Menu

| | Device | Description |
|--------------------|---|---|
| Power Loss Control | Stay Off Last State (default) | Specifies the power level the system returns to after AC power is lost. <i>Stay Off</i> leaves the server power disabled and ACPI does not function to reboot the server in the event of a power failure.. <i>Last State</i> reboots the system according to ACPI standards.. |
| Power Button | Disable Enable (default) | Enables or disables the power button functionality. |

6.5.9 Boot Menu

To access this menu, select Boot on the menu bar at the top of the screen.

| | | | | | | |
|------|----------|----------|-------|-------------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
|------|----------|----------|-------|-------------|--------|------|

Table 31 lists the options available on the Boot menu. This menu allows you to set the boot priority of devices installed in the system. Use the following key combinations to navigate between or view the devices and change the boot priority:

1. <Enter> expands or collapses devices with a “+” or “-.”
2. <CTRL + Enter> expands all devices.
3. <Shift+I> enables or disables devices.
4. <+> and <-> moves the device up or down.
5. <n> May move the removable device between the hard drive or removable disk.
6. <d> Removes a device that is not installed.

Table 31: Boot Menu

| Boot Priority | Device | Description |
|-----------------------------|-------------------|--|
| 1 st Boot Device | Removable Devices | <p>Specifies the boot sequence according to the device type. The computer will attempt to boot from up to five devices as specified here five devices as specified here. Only one of the devices can be an IDE hard disk drive.</p> <p>The default settings for the first through fourth boot devices are, respectively:</p> <p>Removable Devices: Attempts to boot from the diskette drive or removable device like the floppy.</p> <p>Hard Drive: Attempts to boot from a hard drive device.</p> <p>CD-ROM Drive: Attempts to boot from a CD-ROM drive containing bootable media. This entry appears if there is a bootable CD-ROM that is in a BIOS Boot Specification-compliant SCSI CD-ROM.</p> <p>Network Boot – This is the old network boot ROM via hook Interrupt 19H or Interrupt 18H. If there exists a string “\$PnP” in the network card ROM it will be the correct BBS. Thus it will be displayed on the boot menu as an independent device. Otherwise it will use the “Boot/Network Boot” menu.</p> |
| 2 nd Boot Device | Hard Drive | |
| 3 rd Boot Device | CD-ROM Drive | |
| 4 th Boot Device | Network Boot | |
| | Disabled | |

6.5.10 System Menu

To access this menu, select System on the menu bar at the top of the screen.

| | | | | | | |
|------|----------|----------|-------|------|--------|------|
| Main | Advanced | Security | Power | Boot | System | Exit |
|------|----------|----------|-------|------|--------|------|

Table 32 lists the options available on the System menu. This menu displays

Table 32: System Menu

| Feature | Choices | Description |
|----------------|---------|--|
| Machine Vendor | <Enter> | Provides basic information on the machine vendor: Manufacturer: Intel Corporation Product: SE7500CW2 Version: 1.00 Serial Number: 12345678 |
| CPU | <Enter> | Provides basic information on the processor. Boot Strap Processor: Installed Speed: 1.8 GHz (for example) Socket Name: BSP Manufacturer: Genuine Intel Version: Intel(R) XEON(TM) CPUID: 3FEBFBFF00000F24 L2 Cache: 512KB Application Processor: Installed Speed: 1.8 GHZ (for example) Socket Name: AP Manufacturer: Genuine Intel Version: Intel(R) XEON(TM) CPUID: 3FEBFBFF00000F24 L2 Cache: 512KB |
| Memory | <Enter> | Provides basic information on the memory: System Memory: 640 KB Extended Memory: 1023 MB (BIOS based memory) Shadow RAM: 384 KB Cache RAM: 512 KB Installed Size—DIMM 1A, 1B, 2A, and 2B: DIMM size in MB |
| Peripherals | <Enter> | None of these can be modified in user mode. (I.E. J44-COM1; j- Parallel; J46 – PS/2 Keyboard; J4 & J5 – IDE; J6 & J7 – ATA 100 IDE; j47 – NIC1, NIC2; J43 – USB2 and USB1). |
| BIOS | <Enter> | ROM SIZE: 1024 KB Vendor: Phoenix Technologies LTD Version: 1.14 Release Date: 2/22/2002 – creation date |

6.5.11 Exit Menu

To access this menu, select Exit on the menu bar at the top of the screen.

| | | | | | | |
|------|----------|----------|-------|------|--------|-------------|
| Main | Advanced | Security | Power | Boot | System | Exit |
|------|----------|----------|-------|------|--------|-------------|

Table 33 lists the options available in the Exit menu. Select an option using the up or down arrow keys; then press <Enter> to execute the option. Pressing <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit.

Table 33: Exit Menu

| Choices | Description |
|-------------------------|---|
| Exit Saving Changes | Exits after writing all modified Setup item values to CMOS. |
| Exit Discarding Changes | Exits leaving CMOS unmodified. User is prompted if any of the setup fields were modified. |
| Load Setup Defaults | Loads default values for all Setup items. |
| Discard Changes | Reads a previous value of all Setup items from CMOS. |
| Save Changes | Writes all Setup item values to CMOS. |
| Load Custom Default | Loads custom default values for all setup items. |
| Save Custom Default | Saves all Setup item values to NVRAM as a custom default. |

6.6 BIOS Security Features

The Server Board SE7500CW2 server BIOS provides a number of security features. This section describes the security features and operating model.

Note: The Server Board SE7500CW2 has the ability to boot from a device attached to the USB port, such as a floppy disk, disk drive or CD-ROM, or ZIP* drive, even if it is attached through a hub. The security model is not supported when booting to a USB device.

6.6.1 Operating Model

The following table summarizes the operation of the security features supported by the Server Board SE7500CW2 server BIOS.

Table 34: Security Features Operating Model

| Mode | Entry Method/Event | Entry Criteria | Behavior | Exit Criteria | After Exit |
|------------------|--------------------|---|---|---------------|---|
| Password on boot | Power On/Reset | User Password set and password on boot enabled and in Setup | System halts for User Password before scanning option ROMs. No mouse or keyboard input is accepted except the password. | User Password | Front panel switches are re-enabled. PS/2 Keyboard and PS/2 mouse inputs are accepted. The system boots normally. Boot sequence is determined by Setup options. |

6.6.2 Password Protection

The BIOS uses passwords to prevent unauthorized tampering with the system. Once secure mode is entered, access to the system is allowed only after the correct password(s) has been entered. Both the user and Supervisor passwords are supported by the BIOS. User password can only be set with the Supervisor priority. The maximum length of the password is eight characters. The password cannot have characters other than alphanumeric (a-z, A-Z, 0-9). The user and supervisor passwords are not case sensitive.

Once set, a password can be cleared by changing it to a null string. Entering the user password allows the user to modify the time, date, user password, secure mode timer, and secure mode hot-key setup fields. Other setup fields can be modified only if the supervisor password is entered. The user password also allows the system to boot if secure boot is enabled. If only one password is set, this password is required to enter Setup. The supervisor has control over all fields in the setup including the ability to clear user password.

If the user enters three wrong passwords in a row during the boot sequence, the system will be placed into a halt state. This feature makes it difficult to break the password by “trial and error” method. When entering a password, the backspace key is accepted as a character of the password.

6.6.2.1 Supervisor/User Passwords and F2 Setup Usage Model

Note:

1. Visible = option string is active and changeable
 2. Shaded = option string is grayed-out and view-only
-

6.6.2.1.1 Three Scenarios

Scenario# 1

| | |
|-----------------------------------|----------------------|
| Supervisor Password | Not Installed |
| User Password | Not Installed |
| Login Type: N/A | |
| Set User Password (shaded) | |
| Set Supervisor Password (visible) | |
| Password on boot (Shaded) | |
| Diskette Access (Shaded) | |

Note: User Access Level option will be Full and Shaded as long as the supervisor password is not installed.

Scenario# 2

| | |
|-----------------------------------|------------------|
| Supervisor Password | Installed |
| User Password | Installed |
| Login Type: Admin/Supervisor | |
| Set User Password (visible) | |
| Set Supervisor Password (Visible) | |
| Password on boot (visible) | |
| Diskette Access (visible) | |
| Login Type: User | |
| Set User Password (visible) | |
| Set Supervisor Password (shaded) | |
| Password on boot (shaded) | |
| Diskette Access (shaded) | |

Scenario# 3

| | |
|------------------------------------|----------------------|
| Supervisor Password | Installed |
| User Password | Not Installed |
| Login Type: Supervisor | |
| Set User Password (visible) | |
| Set Supervisor Password (Visible) | |
| User Access Level [Full] (visible) | |
| Password on boot (shaded) | |
| Diskette Access (shaded) | |

7. Error Reporting and Handling

7.1 POST Codes, Error Messages, and Error Codes

The BIOS indicates the current testing phase during POST by writing a hex code to I/O location 80h. If errors are encountered, error messages or codes will either be displayed to the video screen, or if an error has occurred prior to video initialization, errors will be reported through a series of audio beep codes.

The error codes are defined by Intel and whenever possible are backward compatible with error codes used on earlier platforms.

7.1.1 Port 80 Codes

BIOS will send a 1-byte hex code to port 80 before each task is performed.

The purpose of the port 80 codes is to provide a troubleshooting method in the event of a system hang during the POST. Below is the table of the Port 80 codes and their corresponding task description.

Note: Warm start only tasks are shaded, the Cold Start only tasks have heavy border.

Table 35: System ROM BIOS POST task point

| Tpoint | Description |
|---------------|---|
| 02h | Verify Real Mode. If the CPU is in protected mode, turn on A20 and pulse the reset line, forcing a shutdown 0. NOTE: Hook routine should not alter DX, which holds the power up CPU ID. |
| 03h | Disable Non-Maskable Interrupts. |
| 04h | Get CPU type from CPU registers and other methods. Save CPU type in NVRAM. NOTE: Hook routine should not alter DX, which holds the power up CPU ID. |
| 06h | Initialize system hardware. Reset the DMA controllers, disable the videos, clear any pending interrupts from the real-time clock and set up port B register. |
| 07h | Disable system ROM shadowed start to execute ROMEXEC code from the flash part. This task is pulled into the build only when the ROMEXEC relocation is installed. |
| 08h | Initialize chip set registers to their initial POST values. |
| 09h | Set in-POST flag in CMOS that indicates we are in POST. This bit determines if the current configuration causes the BIOS to hang. If so, the BIOS, on the next POST, uses default values for its configuration. |
| 0Ah | Initialize CPU registers |
| 0Bh | Enable CPU cache. Set bits in CMOS related to cache. |
| 0Ch | Set the initial POST values of the cache registers if not integrated into the chipset. |
| 0Eh | Set the initial POST values for registers in the integrated I/O chip. |
| 0Fh | Enable the local bus IDE as primary or secondary depending on other drives detected. |
| 10h | Initialize Power Management. |
| 11h | General dispatchers for alternate register initialization. Set initial POST values for other hardware devices defined in the register tables. |
| 12h | Restore the contents of the CPU control word whenever the CPU is reset. |
| 13h | Early reset of PCI devices required to disable bus master. Assumes the presence of a stack |

| Tpoint | Description |
|---------------|--|
| | and running from decompressed shadow memory. |
| 14h | Verify that the 8742 keyboard controller is responding. Send a self-test command to the 8742 and wait for results. Also read the switch inputs from the 8742 and write the keyboard controller command byte. |
| 16h | Verify that the ROM BIOS checksums to zero |
| 17h | Initialize external cache before auto-sizing memory. |
| 18h | Initialize all three of the 8254 timers. Set the clock timer (0) to binary count, mode 3 (square wave mode), and read/write LSB then MSB. Initialize the clock timer to zero. Set the RAM refresh timer (1) to binary count, mode 2 (Rate Generator), and read/write LSB only. Set the counter to 12H to generate the refresh at the proper rate. Set sound timer (2) to binary count, mode 3, and read/write LSB, then MSB. |
| 1Ah | Initialize DMA command register with these settings: <ol style="list-style-type: none"> 1. Memory to memory disabled 2. Channel 0 hold address disabled 3. Controller enabled 4. Normal timing 5. Fixed priority 6. Late write selection 7. DREQ sense active 8. DACK sense active low. Initialize all 8 DMA channels with these settings: <ol style="list-style-type: none"> 1. Single mode 2. Address increment 3. Auto initialization disabled (channel 4 - Cascade) 4. Verify transfer |
| 1Ch | Initialize the 8259 interrupt controller with these settings: <ol style="list-style-type: none"> 1. ICW4 needed 2. Cascade 3. Edge-triggered mode. |
| 20h | Verify that DRAM refresh is operating by polling the refresh bit in PORTB. |
| 22h | Reset the keyboard. |
| 24h | Set segment-register addressability to 4 GB |
| 28h | Using the table of configurations supplied by the specific chipset module, test each DRAM configuration to see if that particular configuration is valid. Then program the chipset to its auto-sized configuration. Before auto-sizing, disable all caches and all shadow RAM. |
| 29h | Initialize the POST Memory Manager |
| 2Ah | Zero the first 512K of RAM |
| 2Ch | Test 512K base address lines |
| 2Eh | Test first 512K of RAM. |
| 2Fh | Initialize external cache before shadowing. |
| 32h | Compute CPU speed. |
| 33h | Initialize the Phoenix Dispatch Manager |
| 36h | Vector to proper shutdown routine. |
| 38h` | Shadow the system BIOS. |
| 3Ah | Auto-size external cache and program cache size for enabling later in POST. |
| 3Ch | Set chipset registers to their CMOS values if CMOS is valid, unless auto configuration is enabled, in which case load the chipset registers from the Setup default table. |
| 3Dh | Load alternate registers with CMOS values. Register-table pointers are in the altreg table segment. |
| 41h | Initialize extended memory for RomPilot. |
| 42h | Initialize interrupt vectors 0 thru 77h to the BIOS general interrupt handler. |
| 45h | Initialize all motherboard devices. |
| 46h | Verify the ROM copyright notice |

| Tpoint | Description |
|---------------|--|
| 47h | Initialize support I2O by initializing global variables used by the I2O code. Paused POST table processing if CMOS bit is set. |
| 48h | Verify that the equipment specified in the CMOS matches the hardware currently installed. If the monitor type is set to 00 then a video ROM must exist. If the monitor type is 1 or 2 set the video switch to CGA. If monitor type 3, set the video switch to mono. Also specify in the equipment byte that disk drives are installed. Set appropriate status bits in CMOS or the BDA if configuration errors are found. |
| 49h | Perform these tasks: 1. Size the PCI bus topology and set bridge bus numbers. 2. Set the system max bus number. 3. Write a 0 to the command register of every PCI device. 4. Write a 0 to all 6 base registers in every PCI device. 5. Write a -1 to the status register of every PCI device. |
| 4Ah | Initialize all video adapters in system |
| 4Bh | Initialize Quiet Boot if it is installed. Enable both keyboard and timer interrupts (IRQ0 and IRQ1). If your POST tasks require interrupts off, preserve them with a PUSHF and CLI at the beginning and a POPF at the end. If you change the PIC, preserve the existing bits. |
| 4Ch | Shadow video BIOS ROM if specified by Setup, and CMOS is valid and the previous boot was OK. |
| 4Eh | Display copyright notice. |
| 4Fh | Initialize Multi-Boot. Allocate memory for old and new MultiBoot history tables. |
| 50h | Display CPU type and speed |
| 51h | Checksum CMOS and initialize each EISA slot with data from the initialization data block. |
| 52h | Verify keyboard test. |
| 54h | Initialize keystroke clicker if enabled in Setup. |
| 55h | Enabled USB device. |
| 58h | Test for any unexpected interrupts. First do an STI for hot interrupts. Secondly, test the NMI for an unexpected interrupt. Thirdly, enable the parity checkers and read from memory, checking for an unexpected interrupt. |
| 59h | Register POST Display Services, fonts, and languages with the POST Dispatch Manager. |
| 5Ah | Display prompt "Press F2 to enter SETUP" |
| 5Bh | Disable CPU cache. |
| 5Ch | Test RAM between 512K and 640K. |
| 60h | Determine and test the amount of extended memory available. Determine if memory exists by writing to a few strategic locations and see if the data can be read back. If so, perform an address-line test and a RAM test on the memory. Save the total extended memory size in the CMOS at cmosExtended. |
| 62h | Perform an address line test on A0 to the amount of memory available. This test is dependent on the processor, since the test will vary depending on the width of memory (16 or 32 bits). This test will also use A20 as the skew address to prevent corruption of the system memory. |
| 64h | Jump to UserPatch1. See "The POST Component." |
| 66h | Set cache registers to their CMOS values if CMOS is valid, unless auto configuration is enabled, in which case load cache registers from the Setup default table. |
| 67h | Quick initialization of all Application Processors in a multi-processor system. |
| 68h | Enable external cache and CPU cache if present. Configure non-cacheable regions if necessary. NOTE: Hook routine must preserve DX, which carries the cache size to the Display CacheSize J routine. |
| 6Ah | Display external cache size on the screen if it is non-zero. NOTE: Hook routine must preserve DX, which carries the cache size from the cache Configure J routine. |
| 6Bh | If CMOS is bad, load Custom Defaults from flash into CMOS. If successful, reboot. |
| 6Ch | Display shadow message |

| Tpoint | Description |
|---------------|---|
| 6Eh | Display the starting offset of the non-disposable segment of the BIOS |
| 70h | Check flags in CMOS and in the BIOS data area for errors detected during POST. Display error messages on the screen. |
| 72h | Check status bits to see if configuration problems were detected. If so, display error messages on the screen. |
| 76h | Check status bits for keyboard-related failures. Display error messages on the screen. |
| 7Ch | Initialize the hardware interrupt vectors from 08 to 0F and from 70h to 77H. Also set the interrupt vectors from 60h to 66H to zero. |
| 7Eh | The Coprocessor initialization test. Use the floating-point instructions to determine if a coprocessor exists instead of the ET bit in CR0. |
| 80h | Disable onboard COM and LPT ports before testing for presence of external I/O devices.. |
| 81h | Run late device initialization routines. |
| 82h | Test and identify RS232 ports |
| 83h | Configure Fisk Disk Controller |
| 84h | Test and identify Parallel port. |
| 85h | Display any ESCD read errors and configure all PnP ISA devices. |
| 86h | Initialize onboard I/O and BDA according to CMOS and presence of external devices. |
| 87h | Initialize motherboard configurable devices. |
| 88h | Initialize interrupt controller. |
| 89h | Enable non-maskable interrupts. |
| 8Ah | Initialize Extended BIOS Data Area and initialize the mouse. |
| 8Bh | Setup interrupts vector and present bit in Equipment byte. |
| 8Ch | Initialize both of the floppy disks and display an error message if failure was detected. Check both drives to establish the appropriate diskette types in the BIOS data area. |
| 8Fh | Count the number of ATA drives in the system and update the number in bdaFdiskcount. |
| 90h | Initialize hard-disk controller. If the CMOS ram is valid and intact, and fixed disks are defined, call the fixed disk init routine to initialize the fixed disk system and take over the appropriate interrupt vectors. |
| 91h | Configure the local bus IDE timing register based on the drives attached to it. |
| 92h | Jump to UserPatch2. See "The POST Component". |
| 93h | Build the MPTABLE for multi-processor boards |
| 95h | <ol style="list-style-type: none"> 1. Check CMOS for CD-ROM drive present 2. Activate the drive by checking for media present 3. Check sector 11h (17) for Boot Record Volume Descriptor 4. Check the boot catalog for validity 5. Pick a boot entry 6. Create a Specification Packet |
| 96h | Reset segment-register addressability from 4GB to normal 64K by generating a Shutdown 8. |
| 97h | Create pointer to MP table in Extended BDA. |
| 98h | Search for option ROMs. Rom scan the area from C800h for a length of BCP_ROM_Scan_Size (or to E000h by default) on every 2K boundry, looking for add on cards that need initialization. |
| 99h | Check support status ROMs. Rom scan the area from C800h for a length of BCP_ROM_Scan_Size(or to E000h by default) on every 2K boundary, looking for add on cards that need initialization. |
| 9Ah | Shadow miscellaneous ROMs if specified by Setup and CMOS is valid and the previous boot was OK. |
| 9Ch | Set up Power Management. Initiate power -management state machine. |
| 9Dh | Initialize Security Engine. |
| 9Eh | Enable hardware interrupts |
| 9Fh | Check the total number of Fast Disks (ATA and SCSI) and update the bdaFdiskCount. |
| A0h | Verify that the system clock is interrupting. |
| A2h | Setup Numlock indicator. Display a message if key switch is locked. |
| A4h | Initialize typematic rate |
| A8h | Overwrite the "Press F2 for Setup" prompt with spaces, erasing it from the screen. |
| Aah | Scan the key buffer to see if the F2 key was struck after keyboard interrupts were enabled. If an F2 |

| Tpoint | Description |
|--------|---|
| | keystroke is found, set a flag. |
| ACh | Enter SETUP. If (F2 was pressed) go to SETUP Else if (errors were found) display "Press F1 or F2" prompt if (F2 is pressed) go to setup else if (F1 is pressed) boot Else boot |
| AEh | Clear ConfigFailedBit and InPostBit in CMOS. |
| B0h | Check for errors. If (errors were found) beep twice display "F1 or F2" message if (F2 keystroke) go to SETUP if (F1 keystroke) go to BOOT |
| B2h | Change status bits in CMOS and/or the BIOS data area to reflect the fact that POST is complete. |
| B4h | One quick beep |
| B5h | Turn off <Esc> and <F2> key checking. IF (VGA adapter is present) IF (OEM screen is still up) Note OEM screen is gone. Fade out OEM screen. Reset video: clear screen, reset cursor, reload DAC. ENDIF ENDIF |
| B6h | If password on boot is enabled, a call is made to Setup to check password. If the user does not enter a valid password, Setup does not return. |
| B7h | Initialize ACPI BIOS. |
| B9h | Clear all screen graphics before booting. |
| BAh | Initialize the SMBIOS header and sub-structures. |
| BCh | Clear parity-error latch |
| BDh | Display Boot First menu if MultiBoot is installed. |
| BEh | If BCP option is enabled, clear the screen before booting. |
| BFh | Check virus and backup reminders. Display System Summary. |
| C0h | Try to boot with INT 19 |
| C1h | Initialize the Post Error Manager. |
| C2h | Write PEM errors. |
| C3h | Display PEM errors. |

Note: Warm start only tasks are shaded, the Cold Start only tasks have heavy border.

Table 36: Crisis Disk Boot Block BIOS POST Task Point

| Tpoint | Description |
|---------------|------------------------------------|
| 80h | Initialize the chipset |
| 81h | Initialize the bridge. |
| 82h | Initialize the CPU. |
| 83h | Initialize system timer. |
| 84h | Initialize system I/O |
| 85h | Check force recovery boot. |
| 86h | Check sum BIOS ROM. |
| 87h | Go to BIOS |
| 88h | Initialize Multi Processor. |
| 89h | Set Huge Segment. |
| 8Ah | Initialize OEM special code. |
| 8Bh | Initialize PIC and DMA. |
| 8Ch | Initialize Memory type. |
| 8Dh | Initialize Memory size. |
| 8Eh | Shadow Boot Block. |
| 8Fh | System memory test. |
| 90h | Initialize interrupt vector. |
| 91h | Initialize Run Time Clock. |
| 92h | Initialize video. |
| 93h | Initialize System Management Mode. |
| 94h | Output one beep |
| 95h | Boot to Mini DOS. |
| 96h | Clear Huge Segment |
| 97h | Boot to Full DOS |

7.1.2 BIOS POST Beep Codes

The following tables lists POST error beep codes. Prior to system video initialization, the BIOS uses these beep codes to inform users of error conditions.

The beep code occurs only when a critical error or BIOS fails to boot to the operating system. Please note that not all error conditions are supported by BIOS Beep codes.

The following list contains some of the beep codes used in SE7500CW2 platform:

- Memory error: A unique beep-code is derived from the port 80h code as follows:
 - The 8-bit error code is broken down to four 2-bit groups.
 - Each group is made one-based (through 4)
 - Short beeps are generated for the number of times in each group.

Example:

Port 80h = 0E1h is divided into:
11 10 00 01 or 4-3-1-2 beep code

- Two short beeps: CMOS checksum bad been found and load default.
- Five short beeps: Clear CMOS SW is on.
- One short beep: BIOS will boot to the operating system.

Table 37: POST Error Beep Codes

| Beeps | Reason |
|--------------|----------------------------------|
| 4-3-1-2 | No memory DIMM(s) |
| 4-3-1-3 | Memory type is mismatch |
| 4-3-1-4 | No DIMM Pair(s) in System |
| 4-3-3-1 | Memory Error Row Address Bits |
| 4-3-3-2 | Memory Error Internal Banks |
| 4-3-3-3 | Memory Error Timing |
| 4-3-3-4 | Memory Error Register CAS 3 |
| 4-3-4-1 | Memory Error Register NonReg Mix |
| 4-3-4-2 | Memory Error CAS Latency |
| 4-3-4-3 | Memory Error Size Not Supported |

7.1.3 BIOS Recovery Beep Codes

Table 38. BIOS Recovery Beep Codes

| Beeps | Reason |
|-------|---|
| 1 | One long beep – Video is active. |
| 1-2 | One long beep and two short beeps – The system is requesting the the user to insert the BIOS recovery diskette. |

7.1.4 POST Error Codes and Messages

The following table defines POST error codes and their associated messages. The BIOS prompts the user to press a key in case of serious errors. The string “Error” to highlight the fact that the system might be malfunctioning precedes some of the error messages.

During the POST, BIOS will show some human-readable information on the screen to get the attention of the user when some errors have been run into. The table below list the possible error number user may encounter and the related meaning. Most information here show the HW device issue (failure or not found), some may include the initialization status.

If your system displays one of the messages marked below with an asterisk (*), write down the message and contact Intel Customer Support. If your system fails after you make changes in the Setup menus, reset the computer, enter Setup and install Setup defaults or correct the error.

Table 39: Post Error Message

| | | |
|--------|---|---|
| 0200 | Failure Fixed Disk | Fixed disk is not working or not configured properly. Check to see if fixed disk is attached properly. Run Setup. Find out if the fixed-disk type is correctly identified. |
| 0210 | Stuck key | Stuck key on keyboard. |
| 0211 | Keyboard error | Keyboard not working. |
| * 0212 | Keyboard Controller Failed | Keyboard controller failed test. May require replacing keyboard controller. |
| 0213 | Keyboard locked - Unlock key switch | Unlock the system to proceed. |
| * 0230 | Shadow Ram Failed at offset: nnnn | Shadow RAM failed at offset nnnn of the 64k block at which the error was detected. |
| * 0231 | System RAM Failed at offset: nnnn | System RAM failed at offset nnnn of in the 64k block at which the error was detected. |
| * 0232 | Extended RAM Failed at address line: nnnn | Extended memory not working or not configured properly at offset nnnn |
| 0250 | System battery is dead - Replace and run SETUP | The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system. |
| 0251 | System CMOS checksum bad - Default configuration used | System CMOS has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. The BIOS installed Default Setup Values. If you do not want these values, enter Setup and enter your own values. If the error |

- persists, check the system battery or contact your dealer.
- * 0260 System timer error
The timer test failed. Requires repair of system board.
 - * 0270 Real time clock error
Real-Time Clock fails BIOS hardware test. May require board repair.
 - 0271 Check date and time settings
BIOS found date or time out of range and reset the Real-Time Clock. May require setting legal date (1991-2099).
 - 0280 Previous boot incomplete - Default configuration used
Previous POST did not complete successfully. POST loads default values and offer to run Setup. If the failure was caused by incorrect values and they are not corrected, the next boot will likely fail. On systems with control of **wait states**, improper Setup settings can also terminate POST and cause this error on the next boot. Run Setup and verify that the wait-state configuration is correct. This error is cleared the next time the system is booted.
 - 0281 Memory Size found by POST differed from EISA CMOS
Memory size found by POST differed from CMOS.
 - 02B0 Diskette drive A error
Drive A: is present but fails the BIOS POST diskette tests. Check to see that the drive is defined with the proper diskette type in Setup and that the diskette drive is attached correctly.
 - 02B2 Incorrect Drive A type - run SETUP
Type of floppy drive A: not correctly identified in Setup.
 - 02D0 System cache error - Cache disabled
RAM cache failed and BIOS disabled the cache. On older boards, check the cache jumpers. You may have to replace the cache. See your dealer. A disabled cache slows system performance considerably.
 - 02F0 CPU ID:
CPU socket number for Multi-Processor error.
 - * 02F4 EISA CMOS not writeable
Cannot write to EISA CMOS.
 - * 02F5 DMA Test Failed
Cannot write to extend **DMA** (Direct Memory Access) registers.
 - * 02F6 Software NMI Failed
Cannot generate software NMI (Non-Maskable Interrupt).
- Device Address Conflict
Address conflict for specified **device**.
- Allocation Error for device
Run ISA or EISA Configuration Utility to resolve resource conflict for the specified **device**.
- CD ROM Drive
CD ROM Drive identified
- Entering SETUP ...
Starting Setup program
- Fixed Disk n
Fixed disk n (0-3) identified
- Invalid System Configuration Data
Problem with NVRAM (CMOS) data.
- IO device IRQ conflict
I/O device IRQ conflict error.
- PS/2 Mouse Boot Summary Screen
PS/2 Mouse installed.

nnnnM Extended RAM Passed

Where **nnnn** is the amount of RAM in megabytes successfully tested.

nnnnK Cache SRAM Passed

Where **nnnn** is the amount of system cache in kilobytes successfully tested.

nnnnK Shadow RAM Passed

Where **nnnn** is the amount of shadow RAM in kilobytes successfully tested.

nnnnK System RAM Passed

Where **nnnn** is the amount of system RAM in kilobytes successfully tested.

One or more I2O Block Storage Devices were excluded from the Setup Boot Menu

There was not enough room in the IPL table to display all installed I2O block-storage devices.

Operating system not found

Operating system cannot be located on either drive A: or drive C:.. Enter Setup and see if fixed disk and drive A: are properly identified.

Parity Check 1 nnnn

Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays **????**. Parity is a method for checking errors in binary data. A parity error indicates that some data has been corrupted.

Parity Check 2 nnnn

Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays **????**.

Press <F1> to resume, <F2> to Setup

Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change the settings.

Press <F2> to enter SETUP

Optional message displayed during POST.

Mouse initialized

Mouse identified

Run the I2O Configuration Utility

One or more unclaimed block storage devices have the Configuration Request bit set in the LCT. Run an I2O Configuration Utility (e.g. the SAC utility).

System BIOS shadowed

System BIOS copied to shadow RAM.

Video BIOS shadowed

Video BIOS successfully copied to shadow RAM.

7.1.5 Memory Error Codes

If memory errors occur the POST the user will see the following error codes and messages.

Table 40: Memory Error Codes

| Tpoint | Description |
|---------------|----------------------------------|
| 0E1h | No memory DIMM(s) |
| 0E2h | Memory type is mismatch |
| 0E3h | No DIMM Pair(s) in System |
| 0E8h | Memory Error Row Address Bits |
| 0E9h | Memory Error Internal Banks |
| 0EAh | Memory Error Timing |
| 0EBh | Memory Error Register CAS 3 |
| 0ECh | Memory Error Register NonReg Mix |
| 0EDh | Memory Error CAS Latency |
| 0EEh | Memory Error Size Not Supported |

8. Connectors and Jumper Blocks

8.1 Main Power Connector

The main power supply connection is obtained using the 24-pin connector. The following table defines the pin-outs of the connector.

Table 41. Power Connector (J26)

| Pin | Signal | Color | Pin | Signal | Color |
|-----|------------|--------|-----|---------|--------|
| 1 | +3.3V | Orange | 13 | +3.3V | Orange |
| 2 | +3.3V | Orange | 14 | +12V | Blue |
| 3 | GND | Black | 15 | GND | Black |
| 4 | +5V | Red | 16 | DC_ON_L | Green |
| 5 | GND | Black | 17 | GND | Black |
| 6 | +5V | Red | 18 | GND | Black |
| 7 | GND | Black | 19 | GND | Black |
| 8 | PWR_GOOD_H | Gray | 20 | | White |
| 9 | AUX5V | Purple | 21 | +5V | Red |
| 10 | +12V | Yellow | 22 | +5V | Red |
| 11 | +12V | Yellow | 23 | +5V | Red |
| 12 | +3.3V | Orange | 24 | GND | Black |

Table 42. Auxiliary Signal Connector (J24)

| Pin | Signal | Color |
|-----|---------|--------|
| 1 | SCL_H | Green |
| 2 | SDA_H | Yellow |
| 3 | ALTER_L | Red |
| 4 | GND | Black |
| 5 | 3.3V | Orange |

Note: Typical COM2 server cables cross signals, unlike desktop boards.

Table 43. Auxiliary CPU Power Connector (J20)

| Pin | Signal | Pin | Signal |
|-----|--------|-----|---------|
| 1 | GND | 5 | +12VENG |
| 2 | GND | 6 | +12VENG |
| 3 | GND | 7 | +12VENG |
| 4 | GND | 8 | +12VENG |

8.2 Memory Module Connector

The Server Board SE7500CW2 has four DDR DIMM connectors and supports registered ECC DDR modules.

Table 44. DIMM Connectors (J37, J38, J39, J40)

| Pin | Front | Pin | Front | Pin | Front | Pin | Back | Pin | Back | Pin | Back |
|-----|--------|-----|-------|-----|-------|-----|-------|-----|------|-----|--------|
| 1 | VREF | 32 | A5 | 62 | VDDQ | 93 | VSS | 124 | VSS | 154 | /RAS |
| 2 | DQ0 | 33 | DQ24 | 63 | /WE | 94 | DQ4 | 125 | A6 | 155 | DQ45 |
| 3 | VSS | 34 | VSS | 64 | DQ41 | 95 | DQ5 | 126 | DQ28 | 156 | VDDQ |
| 4 | DQ1 | 35 | DQ25 | 65 | /CAS | 96 | VDDQ | 127 | DQ29 | 157 | /CS0 |
| 5 | DQS0 | 36 | DQS3 | 66 | VSS | 97 | DM0 | 128 | VDDQ | 158 | */CS1 |
| 6 | DQ2 | 37 | A4 | 67 | DQS5 | 98 | DQ6 | 129 | DM3 | 159 | DM5 |
| 7 | VDD | 38 | VDD | 68 | DQ42 | 99 | DQ7 | 130 | A3 | 160 | VSS |
| 8 | DQ3 | 39 | DQ26 | 69 | DQ43 | 100 | VSS | 131 | DQ30 | 161 | DQ46 |
| 9 | NC | 40 | DQ27 | 70 | VDD | 101 | NC | 132 | VSS | 162 | DQ47 |
| 10 | /RESET | 41 | A2 | 71 | */CS2 | 102 | NC | 133 | DQ31 | 163 | */CS3 |
| 11 | VSS | 42 | VSS | 72 | DQ48 | 103 | *A13 | 134 | CB4 | 164 | VDDQ |
| 12 | DQ8 | 43 | A1 | 73 | DQ49 | 104 | VDDQ | 135 | CB5 | 165 | DQ52 |
| 13 | DQ9 | 44 | CB0 | 74 | VSS | 105 | DQ12 | 136 | VDDQ | 166 | DQ53 |
| 14 | DQS1 | 45 | CB1 | 75 | */CK2 | 106 | DQ13 | 137 | CK0 | 167 | NC |
| 15 | VDDQ | 46 | VDD | 76 | *CK2 | 107 | DM1 | 138 | /CK0 | 168 | VDD |
| 16 | *CK1 | 47 | DQS8 | 77 | VDDQ | 108 | VDD | 139 | VSS | 169 | DM6 |
| 17 | */CK1 | 48 | A0 | 78 | DQS6 | 109 | DQ14 | 140 | DM8 | 170 | DQ54 |
| 18 | VSS | 49 | CB2 | 79 | DQ50 | 110 | DQ15 | 141 | A10 | 171 | DQ55 |
| 19 | DQ10 | 50 | VSS | 80 | DQ51 | 111 | *CKE1 | 142 | CB6 | 172 | VDDQ |
| 20 | DQ11 | 51 | CB3 | 81 | VSS | 112 | VDDQ | 143 | VDDQ | 173 | NC |
| 21 | CKE0 | 52 | BA1 | 82 | VDDID | 113 | *BA2 | 144 | CB7 | 174 | DQ60 |
| 22 | VDDQ | KEY | | 83 | DQ56 | 114 | DQ20 | KEY | | 175 | DQ61 |
| 23 | DQ16 | 53 | DQ32 | 84 | DQ57 | 115 | A12 | 145 | VSS | 176 | VSS |
| 24 | DQ17 | 54 | VDDQ | 85 | VDD | 116 | VSS | 146 | DQ36 | 177 | DM7 |
| 25 | DQS2 | 55 | DQ33 | 86 | DQS7 | 117 | DQ21 | 147 | DQ37 | 178 | DQ62 |
| 26 | VSS | 56 | DQS4 | 87 | DQ58 | 118 | A11 | 148 | VDD | 179 | DQ63 |
| 27 | A9 | 57 | DQ34 | 88 | DQ59 | 119 | DM2 | 149 | DM4 | 180 | VDDQ |
| 28 | DQ18 | 58 | VSS | 89 | VSS | 120 | VDD | 150 | DQ38 | 181 | SA0 |
| 29 | A7 | 59 | BA0 | 90 | NC | 121 | DQ22 | 151 | DQ39 | 182 | SA1 |
| 30 | VDDQ | 60 | DQ35 | 91 | SDA | 122 | A8 | 152 | VSS | 183 | SA2 |
| 31 | DQ19 | 61 | DQ40 | 92 | SCL | 123 | DQ23 | 153 | DQ44 | 184 | VDDSPD |

8.3 Processor Heat Syncs

Table 45: Processor Heat Sync data – replacement information

| | |
|------------------------------------|--|
| eatsink (Crimped Hybrid-Fin) | Vendor: Furikawa: Part Number A53376-001 |
| Heatsink (Folded-Fin) | Vendor: Fujikura: Part Number A30041-001 |
| Heatsink Clips | Vendor: Foxconn: Part Number A34614-002 |
| Thermal Grease or Pads | Vendor: MicroSi: Part Number A34404-001 |

8.4 Processor Socket

The Server Board SE7500CW2 has two 604-pin processor sockets. The following table provides the processor socket pin numbers and pin names:

Table 46. Socket 604 Processor Socket

| Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name |
|--------|----------|--------|----------|--------|----------|--------|----------|--------|----------|
| A1 | Reserved | D29 | VCC | K3 | VCC | T29 | VSS | AB3 | BSEL1 |
| A2 | VCC | D30 | VSS | K4 | VSS | T30 | VCC | AB4 | VCCA |
| A3 | SKTOCC# | D31 | VCC | K5 | VCC | T31 | VSS | AB5 | VSS |
| A4 | Reserved | E1 | VSS | K6 | VSS | U1 | VCC | AB6 | D63# |
| A5 | VSS | E2 | VCC | K7 | VCC | U2 | VSS | AB7 | PWRGOOD |
| A6 | A32# | E3 | VID1 | K8 | VSS | U3 | VCC | AB8 | VCC |
| A7 | A33# | E4 | BPM5# | K9 | VCC | U4 | VSS | AB9 | DBI3# |
| A8 | VCC | E5 | IERR# | K23 | VCC | U5 | VCC | AB10 | D55# |
| A9 | A26# | E6 | VCC | K24 | VSS | U6 | VSS | AB11 | VSS |
| A10 | A20# | E7 | BPM2# | K25 | VCC | U7 | VCC | AB12 | D51# |
| A11 | VSS | E8 | BPM4# | K26 | VSS | U8 | VSS | AB13 | D52# |
| A12 | A14# | E9 | VSS | K27 | VCC | U9 | VCC | AB14 | VCC |
| A13 | A10# | E10 | AP0# | K28 | VSS | U23 | VCC | AB15 | D37# |
| A14 | VCC | E11 | BR2#1 | K29 | VCC | U24 | VSS | AB16 | D32# |
| A15 | Reserved | E12 | VCC | K30 | VSS | U25 | VCC | AB17 | D31# |
| A16 | Reserved | E13 | A2 | K31 | VCC | U26 | VSS | AB18 | VCC |
| A17 | LOCK# | E14 | A24# | L1 | VSS | U27 | VCC | AB19 | D14# |
| A18 | VCC | E15 | VSS | L2 | VCC | U28 | VSS | AB20 | D12# |
| A19 | A7# | E16 | COMP1 | L3 | VSS | U29 | VCC | AB21 | VSS |
| A20 | A4# | E17 | VSS | L4 | VCC | U30 | VSS | AB22 | D13# |
| A21 | VSS | E18 | DRDY# | L5 | VSS | U31 | VCC | AB23 | D9# |
| A22 | A3# | E19 | TRDY# | L6 | VCC | V1 | VSS | AB24 | VCC |
| A23 | HITM# | E20 | VCC | L7 | VSS | V2 | VCC | AB25 | D8# |
| A24 | VCC | E21 | RS0# | L8 | VCC | V3 | VSS | AB26 | D7# |
| A25 | TMS | E22 | HIT# | L9 | VSS | V4 | VCC | AB27 | VSS |
| A26 | Reserved | E23 | VSS | L23 | VSS | V5 | VSS | AB28 | SM_EP_A2 |
| A27 | VSS | E24 | TCK | L24 | VCC | V6 | VCC | AB29 | SM_EP_A1 |
| A28 | VCC | E25 | TDO | L25 | VSS | V7 | VSS | AB30 | VCC |
| A29 | VSS | E26 | VCC | L26 | VCC | V8 | VCC | AB31 | VSS |
| A30 | VCC | E27 | FERR# | L27 | VSS | V9 | VSS | AC1 | Reserved |
| A31 | VSS | E28 | VCC | L28 | VCC | V23 | VSS | AC2 | VSS |
| B1 | Reserved | E29 | VSS | L29 | VSS | V24 | VCC | AC3 | VCC |

| | | | | | | | | | |
|-----|----------|-----|-----------|-----|-----|-----|-----------|------|-----------|
| B2 | VSS | E30 | VCC | L30 | VCC | V25 | VSS | AC4 | VCC |
| B3 | VID4 | E31 | VSS | L31 | VSS | V26 | VCC | AC5 | D60# |
| B4 | VCC | F1 | VCC | M1 | VCC | V27 | VSS | AC6 | D59# |
| B5 | OTDEN | F2 | VSS | M2 | VSS | V28 | VCC | AC7 | VSS |
| B6 | VCC | F3 | VID0 | M3 | VCC | V29 | VSS | AC8 | D56# |
| B7 | A31# | F4 | VCC | M4 | VSS | V30 | VCC | AC9 | D47# |
| B8 | A27# | F5 | BPM3# | M5 | VCC | V31 | VSS | AC10 | VCC |
| B9 | VSS | F6 | BPM0# | M6 | VSS | W1 | VCC | AC11 | D43# |
| B10 | A21# | F7 | VSS | M7 | VCC | W2 | VSS | AC12 | D41# |
| B11 | A22# | F8 | BPM1# | M8 | VSS | W3 | Reserved | AC13 | VSS |
| B12 | VCC | F9 | GTLREF | M9 | VCC | W4 | VSS | AC14 | D50# |
| B13 | A13# | F10 | VCC | M23 | VCC | W5 | BCLK1 | AC15 | DP2# |
| B14 | A12# | F11 | BINIT# | M24 | VSS | W6 | TESTHI0 | AC16 | VCC |
| B15 | VSS | F12 | BR1# | M25 | VCC | W7 | TESTHI1 | AC17 | D34# |
| B16 | A11# | F13 | VSS | M26 | VSS | W8 | TESTHI2 | AC18 | DP0# |
| B17 | VSS | F14 | ADSTB1# | M27 | VCC | W9 | GTLREF | AC19 | VSS |
| B18 | A5# | F15 | A19# | M28 | VSS | W23 | GTLREF | AC20 | D25# |
| B19 | REQ0# | F16 | VCC | M29 | VCC | W24 | VSS | AC21 | D26# |
| B20 | VCC | F17 | ADSTB0# | M30 | VSS | W25 | VCC | AC22 | VCC |
| B21 | REQ1# | F18 | DBSY# | M31 | VCC | W26 | VSS | AC23 | D23# |
| B22 | REQ4# | F19 | VSS | N1 | VCC | W27 | VCC | AC24 | D20# |
| B23 | VSS | F20 | BNR# | N2 | VSS | W28 | VSS | AC25 | VSS |
| B24 | LINT0 | F21 | RS2# | N3 | VCC | W29 | VCC | AC26 | D17# |
| B25 | PROCHOT# | F22 | VCC | N4 | VSS | W30 | VSS | AC27 | DBI0# |
| B26 | VCC | F23 | GTLREF | N5 | VCC | W31 | VCC | AC28 | SM_CLK |
| B27 | VCCSENSE | F24 | TRST#TAP | N6 | VSS | Y1 | VSS | AC29 | SM_DAT |
| B28 | VSS | F25 | VSS | N7 | VCC | Y2 | VCC | AC30 | VSS |
| B29 | VCC | F26 | THERMTRIP | N8 | VSS | Y3 | Reserved | AC31 | VCC |
| B30 | VSS | F27 | A20M# | N9 | VCC | Y4 | BCLK0 | AD1 | Reserved |
| B31 | VCC | F28 | VSS | N23 | VCC | Y5 | VSS | AD2 | VCC |
| C1 | VSS | F29 | VCC | N24 | VSS | Y6 | TESTHI3 | AD3 | VSS |
| C2 | VCC | F30 | VSS | N25 | VCC | Y7 | VSS | AD4 | VCCIOPLL |
| C3 | VID3 | F31 | VCC | N26 | VSS | Y8 | RESET# | AD5 | TESTHI5 |
| C4 | VCC | G1 | VSS | N27 | VCC | Y9 | D62# | AD6 | VCC |
| C5 | Reserved | G2 | VCC | N28 | VSS | Y10 | VCC | AD7 | D57# |
| C6 | RSP# | G3 | VSS | N29 | VCC | Y11 | DSTBP3# | AD8 | D46# |
| C7 | VSS | G4 | VCC | N30 | VSS | Y12 | DSTBN3# | AD9 | VSS |
| C8 | A35# | G5 | VSS | N31 | VCC | Y13 | VSS | AD10 | D45# |
| C9 | A34# | G6 | VCC | P1 | VSS | Y14 | DSTBP2# | AD11 | D40# |
| C10 | VCC | G7 | VSS | P2 | VCC | Y15 | DSTBN2# | AD12 | VCC |
| C11 | A30# | G8 | VCC | P3 | VSS | Y16 | VCC | AD13 | D38# |
| C12 | A23# | G9 | VSS | P4 | VCC | Y17 | DSTBP1# | AD14 | D39# |
| C13 | VSS | G23 | LINT1 | P5 | VSS | Y18 | DSTBN1# | AD15 | VSS |
| C14 | A16# | G24 | VCC | P6 | VCC | Y19 | VSS | AD16 | COMP0 |
| C15 | A15# | G25 | VSS | P7 | VSS | Y20 | DSTBP0# | AD17 | VSS |
| C16 | VCC | G26 | VCC | P8 | VCC | Y21 | DSTBN0# | AD18 | D36# |
| C17 | A8# | G27 | VSS | P9 | VSS | Y22 | VCC | AD19 | D30# |
| C18 | A6# | G28 | VCC | P23 | VSS | Y23 | D5# | AD20 | VCC |
| C19 | VSS | G29 | VSS | P24 | VCC | Y24 | D2# | AD21 | D29# |
| C20 | REQ3# | G30 | VCC | P25 | VSS | Y25 | VSS | AD22 | DBI1# |
| C21 | REQ2# | G31 | VSS | P26 | VCC | Y26 | D0# | AD23 | VSS |
| C22 | VCC | H1 | VCC | P27 | VSS | Y27 | Reserved | AD24 | D21# |
| C23 | DEFER# | H2 | VSS | P28 | VCC | Y28 | Reserved | AD25 | D18# |
| C24 | TDI | H3 | VCC | P29 | VSS | Y29 | SM_TS1_A1 | AD26 | VCC |
| C25 | VSS | H4 | VSS | P30 | VCC | Y30 | VCC | AD27 | D4# |
| C26 | IGNNE# | H5 | VCC | P31 | VSS | Y31 | VSS | AD28 | SM_ALERT# |
| C27 | SMI# | H6 | VSS | R1 | VCC | AA1 | VCC | AD29 | SM_WP |
| C28 | VCC | H7 | VCC | R2 | VSS | AA2 | VSS | AD30 | VCC |
| C29 | VSS | H8 | VSS | R3 | VCC | AA3 | BSEL0 | AD31 | VSS |
| C30 | VCC | H9 | VCC | R4 | VSS | AA4 | VCC | AE2 | VSS |

| | | | | | | | | | |
|-----|----------|-----|-----|-----|-----|------|-----------|------|----------|
| C31 | VSS | H23 | VCC | R5 | VCC | AA5 | VSSA | AE3 | VCC |
| D1 | VCC | H24 | VSS | R6 | VSS | AA6 | VCC | AE4 | Reserved |
| D2 | VSS | H25 | VCC | R7 | VCC | AA7 | TESTHI4 | AE5 | TESTHI6 |
| D3 | VID2 | H26 | VSS | R8 | VSS | AA8 | D61# | AE6 | SLP# |
| D4 | STPCLK# | H27 | VCC | R9 | VCC | AA9 | VSS | AE7 | D58# |
| D5 | VSS | H28 | VSS | R23 | VCC | AA10 | D54# | AE8 | VCC |
| D6 | INIT# | H29 | VCC | R24 | VSS | AA11 | D53# | AE9 | D44# |
| D7 | MCERR# | H30 | VSS | R25 | VCC | AA12 | VCC | AE10 | D42# |
| D8 | VCC | H31 | VCC | R26 | VSS | AA13 | D48# | AE11 | VSS |
| D9 | AP1# | J1 | VSS | R27 | VCC | AA14 | D49# | AE12 | DBI2# |
| D10 | BR3#1 | J2 | VCC | R28 | VSS | AA15 | VSS | AE13 | D35# |
| D11 | VSS | J3 | VSS | R29 | VCC | AA16 | D33# | AE14 | VCC |
| D12 | A29# | J4 | VCC | R30 | VSS | AA17 | VSS | AE15 | Reserved |
| D13 | A25# | J5 | VSS | R31 | VCC | AA1 | D24# | AE16 | Reserved |
| D14 | VCC | J6 | VCC | T1 | VSS | AA19 | D15# | AE17 | DP3# |
| D15 | A1# | J7 | VSS | T2 | VCC | AA20 | VCC | AE18 | VCC |
| D16 | A17# | J8 | VCC | T3 | VSS | AA21 | D11# | AE19 | DP1# |
| D17 | A9# | J9 | VSS | T4 | VCC | AA22 | D10# | AE20 | D28# |
| D18 | VCC | J23 | VSS | T5 | VSS | AA23 | VSS | AE21 | VSS |
| D19 | ADS# | J24 | VCC | T6 | VCC | AA24 | D6# | AE22 | D27# |
| D20 | BR0# | J25 | VSS | T7 | VSS | AA25 | D3# | AE23 | D22# |
| D21 | VSS | J26 | VCC | T8 | VCC | AA26 | VCC | AE24 | VCC |
| D22 | RS1# | J27 | VSS | T9 | VSS | AA27 | D1# | AE25 | D19# |
| D23 | BPRI# | J28 | VCC | T23 | VSS | AA28 | SM_TS1_A0 | AE26 | D16# |
| D24 | VCC | J29 | VSS | T24 | VCC | AA29 | SM_EP_A0 | AE27 | VSS |
| D25 | Reserved | J30 | VCC | T25 | VSS | AA30 | VSS | AE28 | SM_V |
| D26 | VSSSENSE | J31 | VSS | T26 | VCC | AA31 | VCC | AE29 | SM_V |
| D27 | VSS | K1 | VCC | T27 | VSS | AB1 | VSS | | |
| D28 | VSS | K2 | VSS | T28 | VCC | AB2 | VCC | | |

1. These are “Reserved” pins on the Intel Xeon processor. In systems utilizing the Intel Xeon processor, the system designer must terminate these signals to the processor V CC.

2. Baseboards treating AA3 and AB3 as Reserved will operate correctly with a bus clock of 100 MHz.

8.5 System Management Headers

8.5.1 I²C Header

Table 47. SCSI HDD Header (J25)

| Pin | Signal Name | Description |
|-----|-------------|-------------|
| 1 | 3VSB SDA | Data Line |
| 2 | GND | |
| 3 | 3VSB SCL | Clock Line |
| 4 | +5VSB | |

8.6 PCI Slot Connector

There are three PCI buses implemented on the Server Board SE7500CW2 board. PCI segment A supports 5V 32-bit/33MHz PCI, segment B supports 3.3V PCI-X 64-bit/100MHz, and segment C supports 3.3V PCI-X 64-bit/133MHz operation. All segments supports full-length PCI add-in cards. The pin-out for each segment is below.

Table 48. P32-A 5V 32-bit/33 MHz PCI Slot

| Pin | Side B | Side A | Pin | Side B | Side A |
|-----|-----------|-----------|-----|---------------|-----------|
| 1 | -12V | TRST# | 32 | AD[17] | AD[16] |
| 2 | TCK | +12V | 33 | C/BE[2]# | +3.3V |
| 3 | Ground | TMS | 34 | Ground | FRAME# |
| 4 | TDO | TDI | 35 | IRDY# | Ground |
| 5 | +5V | +5V | 36 | +3.3V | TRDY# |
| 6 | +5V | INTA# | 37 | DEVSEL# | Ground |
| 7 | INTB# | INTC# | 38 | Ground | STOP# |
| 8 | INTD# | +5V | 39 | LOCK# | +3.3V |
| 9 | PRSNT1# | Reserved | 40 | PERR# | SMBCLK |
| 10 | Reserved | +5V (I/O) | 41 | +3.3V | SMBDAT |
| 11 | PRSNT2# | Reserved | 42 | SERR# | Ground |
| 12 | Ground | Ground | 43 | +3.3V | PAR |
| 13 | Ground | Ground | 44 | C/BE[1]# | AD[15] |
| 14 | Reserved | 3.3Vaux | 45 | AD[14] | +3.3V |
| 15 | Ground | RST# | 46 | Ground | AD[13] |
| 16 | CLK | +5V (I/O) | 47 | AD[12] | AD[11] |
| 17 | Ground | GNT# | 48 | AD[10] | Ground |
| 18 | REQ# | Ground | 49 | Ground | AD[09] |
| 19 | +5V (I/O) | PME# | 50 | CONNECTOR KEY | |
| 20 | D[31] | AD[30] | 51 | CONNECTOR KEY | |
| 21 | AD[29] | +3.3V | 52 | AD[08] | C/BE[0]# |
| 22 | Ground | AD[28] | 53 | AD[07] | +3.3V |
| 23 | AD[27] | AD[26] | 54 | +3.3V | AD[06] |
| 24 | AD[25] | Ground | 55 | AD[05] | AD[04] |
| 25 | +3.3V | AD[24] | 56 | AD[03] | Ground |
| 26 | C/BE[3]# | IDSEL | 57 | Ground | AD[02] |
| 27 | AD[23] | +3.3V | 58 | AD[01] | AD[00] |
| 28 | Ground | AD[22] | 59 | +5V (I/O) | +5V (I/O) |
| 29 | AD[21] | AD[20] | 60 | ACK64# | REQ64# |
| 30 | AD[19] | Ground | 61 | +5V | +5V |
| 31 | +3.3V | AD[18] | 62 | +5V | +5V |

Table 49. P64-B/P64-C 3.3V 64-bit/ 100MHz/133MHz PCI-X Slot

| Pin | Side B | Side A | Pin | Side B | Side A |
|-----|--------|--------|-----|--------|----------|
| 1 | -12V | TRST# | 49 | M66EN | AD[09] |
| 2 | TCK | +12V | 50 | Ground | Ground |
| 3 | Ground | TMS | 51 | Ground | Ground |
| 4 | TDO | TDI | 52 | AD[08] | C/BE[0]# |
| 5 | +5V | +5V | 53 | AD[07] | +3.3V |
| 6 | +5V | INTA# | 54 | +3.3V | AD[06] |

| | | | | | |
|----|---------------|-------------|----|---------------|-------------|
| 7 | INTB# | INTC# | 55 | AD[05] | AD[04] |
| 8 | INTD# | +5V | 56 | AD[03] | Ground |
| 9 | PRSNT1# | Reserved | 57 | Ground | AD[02] |
| 10 | Reserved | +3.3V (I/O) | 58 | AD[01] | AD[00] |
| 11 | PRSNT2# | Reserved | 59 | +3.3V (I/O) | +3.3V (I/O) |
| 12 | CONNECTOR KEY | | 60 | ACK64# | REQ64# |
| 13 | CONNECTOR KEY | | 61 | +5V | +5V |
| 14 | Reserved | 3.3Vaux | 62 | +5V | +5V |
| 15 | Ground | RST# | | CONNECTOR KEY | |
| 16 | CLK | +3.3V (I/O) | | CONNECTOR KEY | |
| 17 | Ground | GNT# | 63 | Reserved | Ground |
| 18 | REQ# | Ground | 64 | Ground | C/BE[7]# |
| 19 | +3.3V (I/O) | PME# | 65 | C/BE[6]# | C/BE[5]# |
| 20 | AD[31] | AD[30] A | 66 | C/BE[4]# | +3.3V (I/O) |
| 21 | AD[29] | +3.3V | 67 | Ground | PAR64 |
| 22 | Ground | AD[28] | 68 | AD[63] | AD[62] |
| 23 | AD[27] | AD[26] | 69 | AD[61] | Ground |
| 24 | AD[25] | Ground | 70 | +3.3V (I/O) | AD[60] |
| 25 | +3.3V | AD[24] | 71 | AD[59] | AD[58] |
| 26 | C/BE[3]# | IDSEL | 72 | AD[57] | Ground |
| 27 | AD[23] | +3.3V | 73 | Ground | AD[56] |
| 28 | Ground | AD[22] | 74 | AD[55] | AD[54] |
| 29 | AD[21] | AD[20] | 75 | AD[53] | +3.3V (I/O) |
| 30 | AD[19] | Ground | 76 | Ground | AD[52] |
| 31 | +3.3V | AD[18] | 77 | AD[51] | AD[50] |
| 32 | AD[17] | AD[16] | 78 | AD[49] | Ground |
| 33 | C/BE[2]# | +3.3V | 79 | +3.3V (I/O) | AD[48] |
| 34 | Ground | FRAME# | 80 | AD[47] | AD[46] |
| 35 | IRDY# | Ground | 81 | AD[45] | Ground |
| 36 | +3.3V | TRDY# | 82 | Ground | AD[44] |
| 37 | DEVSEL# | Ground | 83 | AD[43] | AD[42] |
| 38 | PCIXCAP | STOP# | 84 | AD[41] | +3.3V (I/O) |
| 39 | LOCK# | +3.3V | 85 | Ground | AD[40] |
| 40 | PERR# | SMBCLK | 86 | AD[39] | AD[38] |
| 41 | +3.3V | SMBDAT | 87 | AD[37] | Ground |
| 42 | SERR# | Ground | 88 | +3.3V (I/O) | AD[36] |
| 43 | +3.3V | PAR | 89 | AD[35] | AD[34] |
| 44 | C/BE[1]# | AD[15] | 90 | AD[33] | Ground |
| 45 | AD[14] | +3.3V | 91 | Ground | AD[32] |
| 46 | Ground | AD[13] | 92 | Reserved | Reserved |
| 47 | AD[12] | AD[11] | 93 | Reserved | Ground |
| 48 | AD[10] | Ground | 94 | Ground | Reserved |

8.7 Front Panel Connectors

A standard SSI 34-pin header (J3) is provided to support a system front panel. The header contains reset, NMI, power control buttons, and LED indicators. The following table details the pin out of this header.

Table 50. Front Panel 34-Pin Header (J3)

| Signal Name | Pin | Pin | Signal Name |
|---------------------|-----|-----|-------------------|
| ACPI_LEDgrn_H | 1 | 2 | AUX5V |
| KEY | 3 | 4 | *FAN1_FAULT_LED_H |
| ACPI_LEDamber_H | 5 | 6 | *FAN1_FAULT_LED_L |
| HDD_LED_H | 7 | 8 | *FAN2_FAULT_LED_H |
| HDD_LED_L | 9 | 10 | *FAN2_FAULT_LED_L |
| ACPI switch | 11 | 12 | NIC-1_ACT_LED_H |
| ACPI switch (GND) | 13 | 14 | NIC-1_ACT_LED_L |
| RESET switch | 15 | 16 | SMB_SDA |
| RESET switch (GND) | 17 | 18 | SMB_SCL |
| *Sleep switch | 19 | 20 | INTRUDER |
| *Sleep switch (GND) | 21 | 22 | NIC-2_ACT_LED_H |
| NMI switch | 23 | 24 | NIC-2_ACT_LED_L |
| Key | 25 | 26 | Key |
| Unused | 27 | 28 | Unused |
| Unused | 29 | 30 | Unused |
| Unused | 31 | 32 | Unused |
| Unused | 33 | 34 | Unused |

* => NC (No Connect) in this project

8.8 VGA Connector

The following table details the pin-out of the VGA connector.

Table 51. VGA Connector (J42)

| Pin | Signal Name |
|-----|-------------------------------|
| 1 | Red (analog color signal R) |
| 2 | Green (analog color signal G) |
| 3 | Blue (analog color signal B) |
| 4 | No connection |
| 5 | GND |
| 6 | GND |
| 7 | GND |
| 8 | GND |
| 9 | Fused VCC(+5V) |
| 10 | GND |
| 11 | No connection |
| 12 | DDCDAT |
| 13 | HSYNC (horizontal sync) |
| 14 | VSYNC (vertical sync) |
| 15 | DDCCLK |

8.9 NIC Connectors

The Server Board SE7500CW2 supports two NIC RJ45 connectors. The following table details the pin-out of the connector.

Table 52. RJ-45 Connector (J47)

| Signal Name | Pin | Pin | Signal Name |
|--------------------|-----|-----|---------------------|
| TXP (Primary) | 1 | 9 | PRI_SPEEDLED |
| TXM (Primary) | 2 | 10 | SB3V |
| RXP (Primary) | 3 | 11 | PRI_LILED |
| Connected to Pin 5 | 4 | 12 | PRI_ACTLED_FB |
| Connected to Pin 4 | 5 | 13 | TXP (Secondary) |
| RXM (Primary) | 6 | 14 | TXM (Secondary) |
| GND | 7 | 15 | RXP (Secondary) |
| GND | 8 | 16 | Connected to Pin 17 |

8.10 ATA Connectors

The Server Board SE7500CW2 provides two 40-pin ATA-100 connectors and two 40-pin ATA-100 RAID connectors . The pin-out for all four connectors is identical and is listed in the following table.

Table 53. ATA-100 40-pin Connectors (J4, J5, J6, J7)

| Pin | Signal Name | Pin | Signal Name |
|-----|--------------|-----|-------------|
| 1 | RESET_L | 2 | GND |
| 3 | DD7 | 4 | IDE_DD8 |
| 5 | DD6 | 6 | IDE_DD9 |
| 7 | DD5 | 8 | IDE_DD10 |
| 9 | DD4 | 10 | IDE_DD11 |
| 11 | DD3 | 12 | IDE_DD12 |
| 13 | DD2 | 14 | IDE_DD13 |
| 15 | DD1 | 16 | IDE_DD14 |
| 17 | DD0 | 18 | IDE_DD15 |
| 19 | GND | 20 | KEY |
| 21 | IDE_DMAREQ | 22 | GND |
| 23 | IDE_IOW_L | 24 | GND |
| 25 | IDE_IOR_L | 26 | GND |
| 27 | IDE_IORDY | 28 | GND |
| 29 | IDE_DMAACK_L | 30 | GND |
| 31 | IRQ_IDE | 32 | Test Point |
| 33 | IDE_A1 | 34 | DIAG |
| 35 | IDE_A0 | 36 | IDE_A2 |
| 37 | IDE_DCS0_L | 38 | IDE_DCS1_L |
| 39 | IDE_HD_ACT_L | 40 | GND |

8.11 USB Connector

The following table provides the pin-out for the three external USB connectors.

Table 54. USB Connectors (J43)

| Pin | Signal Name |
|-----|--|
| 1 | Fused VCC (+5V /w over current monitor of both port 0 and 1) |
| 2 | DATAL0 (Differential data line paired with DATAH0) |
| 3 | DATAH0 (Differential data line paired with DATAL0) |
| 4 | GND |

A header on the server board provides an option to support one additional USB connector. The pin-out of the header is detailed in the following table.

Table 55. Optional USB Connection Header (J11)

| Pin | Signal Name | Description |
|-----|-------------|---|
| 1 | Unused | |
| 2 | LUSB3+5V | Front Panel USB Power |
| 3 | Unused | |
| 4 | LUSB3N_H | Front Panel USB Negative Signal |
| 5 | Unused | |
| 6 | LUSB3P_H | Front Panel USB Positive Signal |
| 7 | Ground | |
| 8 | Ground | |
| 9 | Key | |
| 10 | Unused | Front Panel USB Overcurrent signal (Ports 0,1). This signal is not used |

8.12 Floppy Connector

The Server Board SE7500CW2 provides a standard 34-pin interface to the floppy drive controller.

The following tables detail the pin-out of the 34-pin legacy floppy connector.

Table 56. Legacy 34-pin Floppy Connector (J10)

| Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|
| 1 | GND | 2 | FDDENSEL_H |
| 3 | GND | 4 | Unused |
| 5 | KEY | 6 | FDDRATE0_H |
| 7 | GND | 8 | FDINDEX_L |
| 9 | GND | 10 | FDMTR0_L |
| 11 | GND | 12 | FDR1_L |
| 13 | GND | 14 | FDR0_L |
| 15 | GND | 16 | FDMTR1_L |
| 17 | Unused | 18 | FDDIR_H |
| 19 | GND | 20 | FDSTEP_L |
| 21 | GND | 22 | FDWDATA_L |
| 23 | GND | 24 | FDWGATE_L |
| 25 | GND | 26 | FDTRK0_L |
| 27 | Unused | 28 | FLWP_L |
| 29 | GND | 30 | FRDATA_L |
| 31 | GND | 32 | FHDSEL_L |
| 33 | GND | 34 | FDSKCHG_L |

8.13 Serial Port Connectors

Two serial ports are provided on the server board.

- A standard, external DB9 serial connector is located on the back edge of the baseboard to supply a Serial 1 interface
- Serial 2 port is provided through a 9-pin header on the server board.

The following tables detail the pin-outs of these two ports.

Table 57. External DB9 Serial 1 Port (J44)

| Pin | Signal Name | Description |
|-----|-------------|---|
| 1 | OCDCD1_L | Carrier Detect or Data Set Ready ¹ |
| 2 | OCSIN1_H | Receive Data |
| 3 | OCSOUT1_H | Transmit Data |
| 4 | OCSTR1_L | Data Terminal Ready |
| 5 | GND | Signal Ground |
| 6 | OCDSR1_L | Request To Send |
| 7 | OCRST1_L | Carrier Detect or Data Set Ready ¹ |
| 8 | OCCTS1_L | Clear to send |
| 9 | OCRI1_L | Ring Indicate |

Table 58. 9-pin Header Serial 2 Port (J28)

| Pin | Signal Name |
|-----|--------------------------------|
| 1 | OCDCD2_L (carrier detect) |
| 2 | OCDSR2_L (Data Set Ready) |
| 3 | OCSIN2_H (Receive Data) |
| 4 | OCRST2_L Clear to Send) |
| 5 | OCSOUT2_H (Transmit Data) |
| 6 | OCCTS2_L (Request to Send) |
| 7 | OCSTR2_L (Data Terminal Ready) |
| 8 | OCRI2_L (Ring Indicate) |
| 9 | (Ground) |
| 10 | Missing pin |

Note: Please note this is the pin-out on the board and typical com2 server cables cross signals unlike desktop boards.

8.14 Keyboard and Mouse Connector

Two PS/2 ports are provided for use by a keyboard and a mouse. The following table details the pin-out of the PS/2 connector.

Table 59. Keyboard and Mouse PS/2 Connector (J46)

| PS/2 Connectors | Pin | Signal Name |
|-----------------|----------------|----------------|
| Keyboard | 1 | Keyboard Data |
| | 2 | Key |
| | 3 | GND |
| | 4 | Fused VCC |
| | 5 | Keyboard Clock |
| | 6 | Key |
| Mouse | 7 | Mouse Data |
| | 8 | Key |
| | 9 | GND |
| | 10 | Fused VCC |
| | 11 | Mouse Clock |
| | 12 | Key |
| | 13,14,15,16,17 | GND |

8.15 Miscellaneous Headers and Jumpers

8.15.1 Fan Headers

The Server Board SE7500CW2 provides six 3-pin fan headers. All fans provide variable speed control. The fan headers are labeled, CPU Fan 1, CPU Fan 2, SysFan 1, SysFan 2, SysFan 3, SysFan 4.

Table 60. Three-pin Fan Headers (J1, J2, J15, J16, J29, J30)

| Pin | Signal Name | Type | Description |
|-----|-------------|-------|---|
| 1 | Ground | Power | GROUND is the power supply ground |
| 2 | Fan Power | Power | Fan Power |
| 3 | Fan Tach | Out | FAN_TACH signal is connected to the SI/O and MAX6651 to monitor the FAN speed |

8.15.2 System Recovery and Update Jumpers

One 8-pin header (J106), located near the NIC 1 connector, provides a total of five 2-pin jumper blocks that are used to configure several system recovery and update options. The figure below shows the jumper pins and their functions. The factory defaults are set to a protected mode for each function. A jumper stored on pins 9-10 and needs to be moved to the location to perform the particular function desired. For normal operation, the jumper should be on the storage pins. An additional jumper is located at pins 7-8 to protect the Boot block of the BIOS code. This jumper should be in place at all times and only removed when directed to by the release notes in the BIOS update.

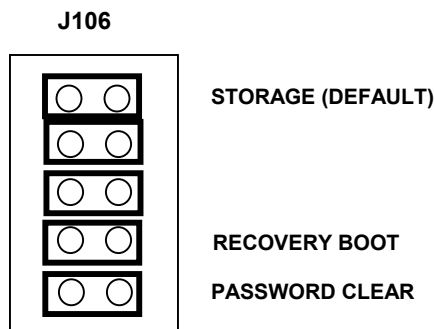


Figure 9. SE7500CW2 Configuration Jumpers (J106)

The following table describes each jumper option.

Table 61. Configuration Jumper Options

| Pin Number | Option | Description |
|------------|--------------------|--|
| 10-9 | Storage | No connect. Default position for jumper storage. |
| 8-7 | BIOS Boot Block WP | Pins 7 and 8 should be jumpered to protect the BIOS bootblock from being flashed. |
| 6-5 | Clear CMOS | If pins 5 and 6 are jumpered CMOS contents are set to factory defaults during system reset. |
| 4-3 | Recovery Mode | If pins 3 and 4 are jumpered, the BIOS will attempt a recovery boot, loading BIOS code from a floppy disk into the Flash device. This is typically used when the BIOS code has been corrupted. |
| 2-1 | Clear Password | If pins 1 and 2 are jumpered, administrator and user passwords areas in the CMOS are cleared and set back to the factory default of null. |

9. General Specifications

9.1 Absolute Maximum Ratings

Operating the baseboard at conditions beyond those shown in the following table may cause permanent damage to the system. The table is provided for stress testing purposes only. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 62. Absolute Maximum Ratings

| | |
|--|--|
| Operating Temperature | 5 degrees C to 50 degrees C ¹ |
| Storage Temperature | -55 degrees C to +150 degrees C |
| Voltage on any signal with respect to ground | -0.3 V to Vdd + 0.3V ² |
| 3.3 V Supply Voltage with Respect to ground | -0.3 V to 3.63 V |
| 5 V Supply Voltage with Respect to ground | -0.3 V to 5.5 V |

Notes:

- Chassis design must provide proper airflow to avoid exceeding Intel Xeon processor maximum case temperature.
- VDD means supply voltage for the device

9.2 Power Budget

The following table shows the power consumed on each supply line for the Server Board SE7500CW2 that is configured with two processors (each 30W max), >1GHz FMB @ 75% usage. This configuration includes four DIMMs stacked burst at 70% max. The numbers provided in the table should be used for reference purposes only. Different hardware configurations will produce different numbers. The numbers in the table reflect a common usage model operating at a higher than average stress levels.

Table 63. Power Budget

| Items | Q'ty | Max Power | Utilize factor | Average power | Output Max Current (V) | | | | | Output Average Current (V) | | | | | | |
|------------------------------------|------|-----------|----------------|---------------|------------------------|------|-------|-----|----|----------------------------|--------------|--------------|--------------|-----|----|--------------|
| | | | | | +5 | +3.3 | +12 | -12 | -5 | +5 VSB | +5 | +3.3 | +12 | -12 | -5 | +5 VSB |
| Mother Board | | | | | | | | | | | | | | | | |
| Processor Vcore¹ | 2 | 178.49 | | 142.00 | | | 18.59 | | | | | | 14.79 | | | |
| Processor VRD Eff@ 80% | | 35.70 | 20% | 28.40 | | | | | | | | | | | | |
| NB (E7500 MCH) | | | | | | | | | | | | | | | | |
| Vtt (1.175V~1.575V) / 2A | 1 | 2.75 | 80% | 2.20 | | | 0.29 | | | | | | 0.23 | | | |
| E7500 Vcore (1.2V / 3.1A) | 1 | 3.72 | 65% | 2.42 | | 1.41 | | | | | | 0.92 | | | | |
| Vddr (2.5V/ 5.8 A) | 1 | 14.50 | 65% | 9.43 | 3.63 | | | | | 2.36 | | | | | | |
| 1.375 V VRD Eff @80% | | 0.55 | 20% | 0.44 | | | | | | | | | | | | |
| 1.2 V VRD Eff @80% | | 0.74 | 20% | 0.48 | | | | | | | | | | | | |
| 2.5 V VRD Eff @80% | | 2.90 | 20% | 1.89 | | | | | | | | | | | | |
| SB (ICH3) | | | | | | | | | | | | | | | | |
| Vcc 3.3 V | | 1.60 | 65% | 1.04 | | 0.48 | | | | | | 0.315 | | | | |
| Vcc 1.8 V (SC 1548) | | 0.82 | 65% | 0.53 | | 0.45 | | | | | | 0.295 | | | | |
| 1.8 V VRD Eff @80% | | 0.16 | 20% | 0.11 | | | | | | | | | | | | |
| Vcc cpu | 1 | 0.08 | 65% | 0.05 | | | 0.05 | | | | | | 0.03 | | | |
| Memory DDR 266² | 4 | | | | | | | | | | | | | | | |
| DDR 2.5V (FAN 5091) | | 51.88 | 70% | 36.31 | 12.969 | | | | | 9.08 | | | | | | |
| Vtt 1.25V (FAN 5066) | | 7.75 | 70% | 5.43 | | 2.94 | | | | | | 2.055 | | | | |
| 2.5 V VRD Eff @80% | | 10.38 | 20% | 7.26 | | | | | | | | | | | | |
| 1.25 V VRD Eff @80% | | 1.55 | 20% | 1.09 | | | | | | | | | | | | |
| P64H2 | | | | | | | | | | | | | | | | |
| Vcc 3.3V | 2 | 13.20 | 70% | 9.24 | | 2.00 | | | | | | 1.400 | | | | |
| Vcc1.8V (SC 1548) | 2 | 6.34 | 70% | 4.44 | | 1.76 | | | | | | 1.232 | | | | |
| 1.8 V VRD Eff @80% | | 1.27 | 20% | 0.89 | | | | | | | | | | | | |
| VGA RAGE II XL | 1 | 1.15 | 80% | 0.92 | 0.23 | 0.39 | | | | | 0.18 | 0.312 | | | | |
| Super I/O (W83627HF) | 1 | 0.75 | 80% | 0.60 | | 0.23 | | | | 0.15 | | 0.181 | | | | 0.121 |
| NIC 82559 Network chip | 2 | 1.95 | 80% | 1.25 | | | | | | 0.39 | | | | | | 0.250 |
| CLK3.3 (CY28329 Generator) | 1 | 1.35 | 80% | 1.08 | | 0.27 | | | | | | 0.216 | | | | |
| Video RAM (2MX 32) | 1 | 0.99 | 80% | 0.79 | | 0.30 | | | | | | 0.240 | | | | |
| System ROM (FWH) | 1 | 0.04 | 80% | 0.03 | | 0.01 | | | | | | 0.010 | | | | |
| Others | | 7.50 | 50% | 3.75 | 1.50 | | | | | | 0.75 | | | | | |
| USB | 2 | 5.00 | 50% | 2.50 | 1.00 | | | | | | 0.50 | | | | | |
| Keyboard | 1 | 0.75 | 50% | 0.38 | 0.15 | | | | | | 0.08 | | | | | |
| Mouse | 1 | 0.63 | 50% | 0.31 | 0.13 | | | | | | 0.06 | | | | | |
| System Fan | 4 | 9.90 | 75% | 7.43 | | | 1.98 | | | | | | 1.49 | | | |
| CPU Fan | 2 | 4.80 | 75% | 3.60 | | | 0.48 | | | | | | 0.36 | | | |
| Board Level output current | | | | | | | | | | | 13.01 | 7.171 | 16.90 | | | 0.484 |

Notes:

- Intel Xeon FMB: 1.311~ 1.394V/ 65A
Intel Xeon DP: 71W
Assumed VRM Eff. = 80%
From processor Vcore
From 1.8V regulator
From 2.5V regulator
- 4 *DDR 200: $(7.2*2 + 1.1*2) = 16.6A$
4 *DDR 266: $(9*2 + 1.375*2) = 20.75A$
DDR Vtt 6.2A

9.3 Mean Time Between Failures (MTBF) Test Results

This section provides results of MTBF as supplied by non-Intel testing. MTBF is a common server board testing that validates server boards for reliability and performance under extreme working conditions. Time between failures was measured at 108,621 hours when tested at 40 degrees Centigrade.

9.4 Power Supply Constraints

9.4.1 Server Chassis SC5200 Timing Requirements with the ICH3-S

The Server Chassis SC5200 Base front panel power switch will not power on if held between 1-4 seconds, because the timing of the ICH3-S component of the E7500 chipset reads power in 1 and 4 second cycles. In other words, if you hold the power button for 1, 2, 3, or 4, seconds the power will not power on, POST will not occur, and the Operating System will not boot. If pressing the power button does not power on the server it is recommend that you press a second time to guarantee successful power on. If you press the power button for less than 1 second it will power on. These exceptions may require special attention to the baseboard when power-cycling.

9.4.2 BIOS <F2> “Stay off” Switch Limitations

BIOS setup <F2> switch “Power | Power Loss Control | Stay Off” has a built in limitation, which may be seen under rare brown-out (i.e. blackout) situations. What may happen if power to the power-supply is off for less than 3 seconds the reactivated “Stay Off” switch will allow the server to boot although the Microsoft Windows operating system may not be loaded. This is by design but may cause confusion to system administrators when the server starts to reboot, and the POST states that the “Operating System not found”, despite being told to remain off in BIOS with the “Stay Off” switch. Also, since BIOS interacts differently with different power supplies it was determined to leave this small limitation of the “Stay Off” switch. If power is lost for more that 3 seconds then the BIOS switch will work correctly and always leave the server without power.

9.5 Power Supply Specifications

This section provides power supply design guidelines for an Intel® Server Board SE7500CW2-based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 64. SE7500CW2 Static Power Supply Voltage Specification

| Parameter | Min | Nom | Max | Units | Tolerance |
|-----------|--------|--------|--------|------------------|------------|
| +3.3 V | +3.25 | +3.30 | +3.35 | V _{rms} | +1.5/-1.5% |
| +5 V | +4.90 | +5.00 | +5.10 | V _{rms} | +2/-2% |
| +12 V | +11.76 | +12.00 | +12.24 | V _{rms} | +2/-2% |
| -12 V | -11.40 | -12.20 | -13.08 | V _{rms} | +9/-5% |
| +5 VSB | +4.85 | +5.00 | +5.20 | V _{rms} | +4/-3% |

Table 65. SE7500CW2 Dynamic Power Supply Voltage Specification

| Output | Min | Max | Tolerance |
|---------|---------|--------|-----------|
| +3.3 V | 3.20 V | 3.46 V | +5 / -3 % |
| +5 V | 4.80 V | 5.25 V | +5 / -4 % |
| +12 V | 11.52 V | 12.6 V | +5 / -4 % |
| +5 V SB | 4.80 V | 5.25 V | +5 / -4% |

9.5.1 Power Timing

This section discusses the timing requirements for operation with a single power supply. The output voltages must rise from 10% to within regulation limits ($T_{\text{vout_rise}}$) within 5 ms to 70 ms. The +3.3 V, +5 V and +12 V output voltages start to rise approximately at the same time. All outputs must rise monotonically. The +5 V output must be greater than the +3.3 V output during any point of the voltage rise, however, never by more than 2.25 V. Each output voltage shall reach regulation within 50 ms ($T_{\text{vout_on}}$) of each other and begin to turn off within 400 ms ($T_{\text{vout_off}}$) of each other. The following figure shows the output voltage timing parameters.

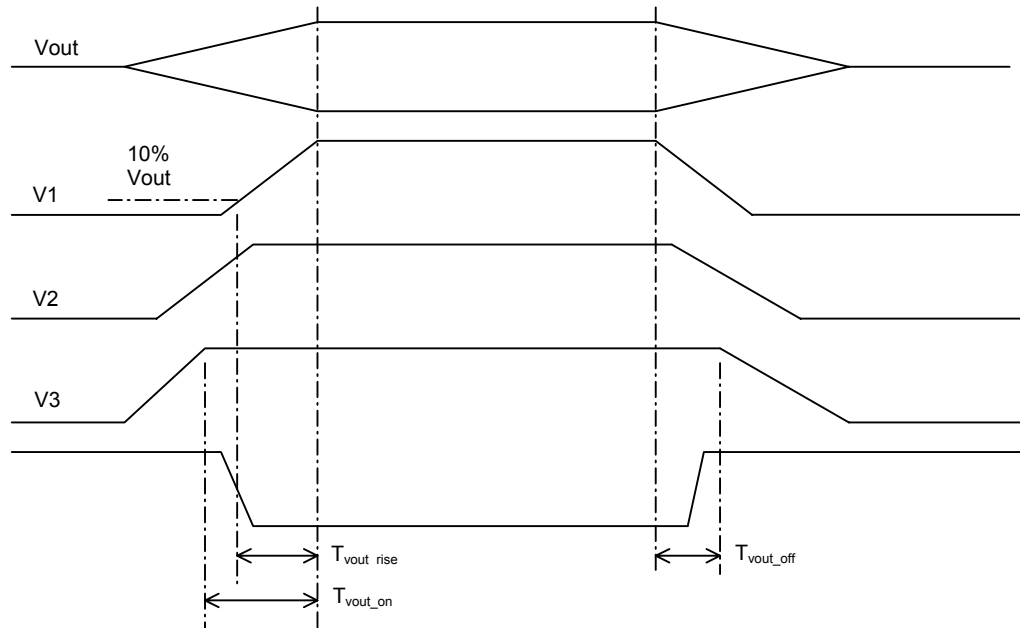


Figure 10. Output Voltage Timing

| Item | Description | Min | Max | Units |
|------------------------|---|-----|------|-------|
| T _{pson_pwok} | Delay from PSON# deactive to PWOK being de-asserted. | | 50 | msec |
| T _{pwok_on} | Delay from output voltages within regulation limits to PWOK asserted at turn on. | 100 | 1000 | msec |
| T _{pwok_off} | Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits. | 2 | | msec |
| T _{pwok_low} | Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal. | 100 | | msec |
| T _{sb_vout} | Delay from 5 V SB being in regulation to O/Ps being in regulation at AC turn on. | 50 | 1000 | msec |

9.5.2 Voltage Recovery Timing Specifications

The power supply must conform to the following specifications for voltage recovery timing under load changes:

- Voltage shall remain within +/- 5% of the nominal set voltage on the +5 V, +12 V, 3.3 V, -5 V and -12 V output, during instantaneous changes in load shown in the following table.
- Voltage regulation limits shall be maintained over the entire AC input range and any steady state temperature and operating conditions specified.
- Voltages shall be stable as determined by bode plot and transient response. The combined error of peak overshoot, set point, regulation, and undershoot voltage shall be less than or equal to +/-5% of the output voltage setting. The transient response measurements shall be made with a load changing repetition rate of 50 Hz to 5 kHz. The load slew rate shall not be greater than 0.2 A / μ s.

Table 68. Transient Load Requirements

| Output | Step Load Size | Starting Level | Finishing Level | Slew Rate |
|--------|----------------|----------------|---|-----------------|
| +3.3 V | 4.8 A | 30Min. Load | Min. load + 4.8 A and step up to max. load | 0.50 A/ μ s |
| +5 V | 3.0 A | 30Min. Load | Min. load + 3.0 A and step up to max. load | 0.50 A/ μ s |
| +12 V | 10.4 A | Min. Load | Min. load + 10.4 A and step up to max. load | 0.50 A/ μ s |
| +5 VSB | 500 mA | Min. Load | Min. load + 500 mA and step up to max. load | 0.50 A/ μ s |
| -12 V | 325 mA | Min. Load | Min load +325 mA and step up to max. load | 0.50 A/ μ s |

9.6 Shock and Vibe Test Results

Shock and vibe testing is a rigorous set of tests which test board strength and durability under extreme conditions. The Server Board SE7500CW2 board has been tested in the Intel® Server Chassis SC5200 Base with the 450W power-supply and the results are as follows:

- Shock operation test passed
- Shock non-operating test failed. Intel is currently investigating this issue at this time.
- Vibration operating test passed.
- Vibration non-operating test passed.

10. Product Regulatory Compliance

10.1.1 Product Safety Compliance

The Server Board SE7500CW2 complies with the following safety requirements:

- UL 1950 - CSA 950 (US/Canada)
- EN 60 950 (European Union)
- IEC60 950 (International)
- CE – Low Voltage Directive (73/23/EEC) (European Union)
- EMKO-TSE (74-SEC) 207/94 (Nordics)
- GOST R 50377-92 (Russia)

10.1.2 Product EMC Compliance

The Server Board SE7500CW2 has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations when installed in a compatible Intel host system. For information on compatible host system(s), contact your local Intel representative.

- FCC (Class A Verification) – Radiated & Conducted Emissions (USA)
- ICES-003 (Class A) – Radiated & Conducted Emissions (Canada)
- CISPR 22 (Class A) – Radiated & Conducted Emissions (International)
- EN55022 (Class A) – Radiated & Conducted Emissions (European Union)
- EN55024 (Immunity) (European Union)
- CE – EMC Directive (89/336/EEC) (European Union)
- AS/NZS 3548 (Class A) – Radiated & Conducted Emissions (Australia / New Zealand)
- RRL (Class A) Radiated & Conducted Emissions (Korea)
- BSMI (Class A) Radiated & Conducted Emissions (Taiwan)

10.1.3 Product Regulatory Compliance Markings

This product is provided with the following product certification markings:

- cURus Recognition Mark
- CE Mark
- Russian GOST Mark
- Australian C-Tick Mark
- Korean RRL MIC Mark
- Taiwan BSMI DOC Mark and BSMI EMC Warning

10.2 Electromagnetic Compatibility Notices

10.2.1 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE mark to illustrate its compliance.

10.2.2 Australian Communications Authority (ACA) (C-Tick Declaration of Conformity)

This product has been tested to AS/NZS 3548, and complies with ACA emission requirements. The product has been marked with the C-Tick mark to illustrate its compliance.

10.2.3 Ministry of Economic Development (New Zealand) Declaration of Conformity

This product has been tested to AS/NZS 3548, and complies with New Zealand's Ministry of Economic Development emission requirements.

10.2.4 BSMI (Taiwan)

The BSMI DOC Mark is silk screened on the component side of the server board; and the following BSMI EMC warning is marked on the server board.

警告使用者：

這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策。

10.3 Replacing the Back-Up Battery

The lithium battery on the server board powers the RTC for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.



WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.



ADVARSEL!

Lithiumbatteri - Eksplosjonsfare ved feilagtig håndtering. Utskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.



ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.



WARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.



VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

11. Mechanical Specifications

11.1 Mechanical Specifications

The following figure shows the server board mechanical drawing.

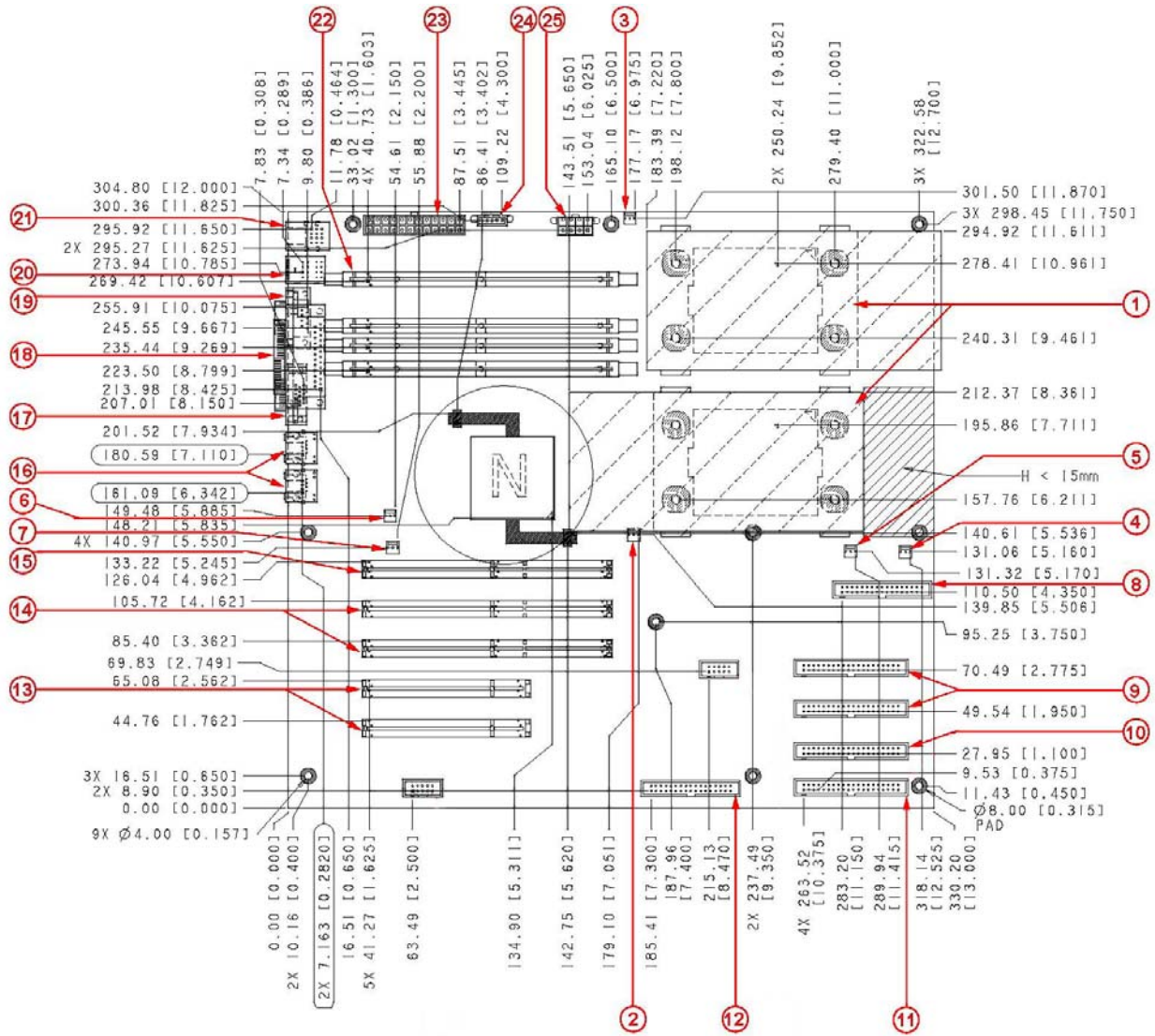


Figure 12. Mechanical Drawing

Table 69. Server Board Connector Specifications

| Item | Q'ty | Manufacturer and Part Number | Description |
|-------------|-------------|-------------------------------------|-------------------------------------|
| 1 | 2 | AMP 1489688-1 | 604P Socket 603/604 |
| 2 | 1 | Lotes F1366RB5L | 3P CPU Fan 1 |
| 3 | 1 | Lotes F1366RB5L | 3P CPU Fan 2 |
| 4 | 1 | Lotes F1366RB5L | 3P System Fan 1 |
| 5 | 1 | Lotes F1366RB5L | 3P System Fan 2 |
| 6 | 1 | Lotes F1366RB5L | 3P System Fan 3 |
| 7 | 1 | Lotes F1366RB5L | 3P System Fan 4 |
| 8 | 1 | AMPHENOL G821A234PAAM02 | 24P Front Panel Connector |
| 9 | 2 | AMPHONEL G821A340PAAG01 | 40P IDE RAID Connector |
| 10 | 1 | AMPHENOL G821A240PAAG01 | 40P Secondary IDE Connector |
| 11 | 1 | AMPHONEL G821A440PAAG01H | 40P Primary IDE Connector |
| 12 | 1 | AMPHONEL G821A234PAAM01 | 34P Floppy Connector |
| 13 | 2 | AMP 0-0011299-6 | 120P PCI 33MHz Slot |
| | | Foxconn EH06007-GL-V | |
| 14 | 2 | AMP 1-145165-2 | 184P PCI-X 100MHz Slot |
| 15 | 1 | FOXCONN EH09247-GY-V | 184P PCI-X 133MHz Slot |
| 16 | 2 | KDS AT49 | 8P NIC Connector |
| 17 | 1 | Lotes D2415CB3S | 15P Video Connector |
| | | Amphenol G17DH1500232PT | |
| 18 | 1 | FOX DM11351-PR3 | 25P Parallel Connector |
| 19 | 1 | FOX DT10121-P5T | 9P COM 1 Connector (Serial 1) |
| 20 | 1 | Amphenol GSB12311 | 12P USB Connector |
| 21 | 1 | FOX MH11061-PD2 | 12P PS/2 Connector (Keyboard/Mouse) |
| 22 | 4 | AMP 390241-1 | 184P DIMM Connector |
| 23 | 1 | Foxconn HM20120 | 24P Main Power Connector |
| | | Lotes C8566SB5N | |
| | | MOLEX 3928-1243 | |
| 24 | 1 | MOLEX 70545-0039 | 5P AUX Power Connector |
| 25 | 1 | MOLEX 44472-0854 | 8P +12V CPU Power Connector |

Appendix A: SE7500CW2 Integration and Usage Tips

Keep the following in while assembling and configuring your server:

- Only DP capable Intel Xeon processors with 512K cache are supported on the Server Board SE7500CW2.
- Processors must be populated in the sequential order; that is, processor Socket #1 must be populated before processor Socket #2
- You do not need to populate a terminator in an unused processor socket.
- Memory DIMMs must be installed in pairs. DIMM pairs are located adjacent to one another – see the board silkscreen
- When creating a RAID array using the Promise ATA 100 RAID controller, keep in mind redundancy can only be obtained when your drives are spread across the two channels. You cannot obtain redundancy if you have a Master / Slave configuration on a single channel. In order for a redundant array to be valid, a Master / Master configuration should be used or a Master w/ Slave & Master w/ Slave configuration. If you have a Master / Slave on a single channel and the master driver goes off-line, your slave drive will also go off-line. Data will not be lost, but your RAID array will be and this could cause unwanted downtime on your server.

Appendix B: Errata

Table 70. Errata Summary

| No. | Plans | Description of Errata |
|-----|---------------|---|
| 1. | Fixed | Intel Xeon processors 2.6 GHz and 2.8 GHz C1 stepping not supported in BIOS 1.14. |
| 2. | Fixed | LDCM 6.3 reported processor speeds change after a system reboot. |
| 3. | Fixed | I can't get my Adaptec 2100S RAID card to clear POST. |
| 4. | Fixed | NetWare 6.0 Service Pack 2 will not install with Hyper-threading enabled in BIOS. |
| 5. | NoFix | Disabling PXE support in BIOS does not correctly disable Network boot support with a PCI NIC add-in card. |
| 6. | NoFix | BIOS is unable to select IDE CD-ROM or USB CDROM as a boot device. |
| 7. | Fixed | LDCM 6.3 build 211 Wake on LAN does not reboot the server. |
| 8. | Fixed | Windows 2000 will not install on a Maxtor D540X-4G 137GIG ATA hard-drive. |
| 9. | Investigating | Adaptec 2100S, 2110S, and 3410S, RAID cards cause LILO to hang with Red Hat 7.3. |
| 10. | Fixed | LDCM 6.3 build 211 incorrectly lowers processor fan speed. |
| 11. | Fixed | BIOS EBDA area disabled in BIOS 1.17. |
| 12. | Fixed | Disable NIC in BIOS incorrectly disables incorrect NIC number. |
| 13. | Fixed | UUID not programmed on all PBA # A87967-506 and older boards. |
| 14. | Fixed | Logical processors not listed in BIOS POST if hyper-threading is enabled in F2 BIOS setup. |
| 15. | Investigating | BIOS memory count with over 2 GB of system memory installed takes more than 2 minutes. |
| 16. | NoFix | "init 0" fails to power off system on Red Hat 8.0 |
| 17. | Fix | Windows 2000 will not display the full size of ATA hard-drives larger than 137GB |
| 18. | Fix | Intel Xeon processors with D1 stepping will not operate under BIOS 1.27 and below. |
| 19. | Fix | Microsoft Windows 2003 does not appear to be supported. |
| 20. | Fix | Ambient temperature seems to be 5-8 degrees Celsius too warm. |

1. Intel Xeon processors 2.6 GHz and 2.8 GHz C1 stepping not supported in BIOS 1.14

- Problem** The Server Board SE7500CW2 BIOS 1.14 does not support Intel Xeon processors running at 2.6 Ghz, and 2.8 GHz.
- Implication** Intel Xeon processors running at 2.6GHz and 2.8GHz will not boot with the currently supported production BIOS 1.14. In other words, this BIOS does not support the C1 stepping that is required by these processors.
- Workaround** None.
- Status** These processor speeds are now supported with BIOS 1.16 and above. Please check <http://support.intel.com> download details. Also available on PBA # -505 and above.

2. LANDesk Client Manger (LDCM) 6.3 reports different processor speeds after a rebooting Windows 2000

- Problem** Intel Xeon processor speeds change in the LDCM 6.3 after a reboot.
- Implication** The speed that LDCM reports may be incorrect, and change after a reboot. Also, the speed may be slightly slower or faster than actual processor speed.
- Workaround** Use the processor speed listed in BIOS <F2> setup under the “System – CPU” sub-menu.
- Status** Intel is investigating the possibility of fixing this erratum.

3. My server system will not boot to DOS with an Adaptec* card installed

- Problem** Server system boots to the Adaptec SMOR utility instead of booting into DOS
- Implication** When running the Adaptec card in “EBDA relocation” mode the system will not boot. If Adaptec’s card “EBDA Relocation” mode is disabled on SE7500CW2 BIOS 1.12 the card will perform correctly under some circumstances.
- Workaround** Create boot disks using Windows 98 DOS instead of DOS 6.22 or the ROM-DOS shipped on the resource CD.
- Status** This issue is resolved with a new release of the Adaptec BIOS and SE7500CW2 BIOS 1.16. The Adaptec BIOS v1.30 should work correctly. BIOS 1.16 and 1.17 are now available for the Server Board SE7500CW2. Both should work properly with this card.

4. NetWare Service Pack 2 will not allow BIOS to enable hyper-threading functionality

- Problem** The acpidrv.psm and scpica.nlm files included support pack 2 do not allow for hyper-threading enabling in BIOS v1.17 and below. The PSM fails to load with the following error: "GPEO block overlaps the GPE1 block. Error initializing the ACPI system."
- Implication** Processor performance of some applications will be hindered without hyper-threading support. Hence, NetWare 6.0 will only be able to use one virtual processor.
- Workaround** The workaround is to use NetWare 6.0 Service Pack 1 if the hyper-threading performance enhancement is required. The ACPI functionality in this service pack works correctly.
- Status** This has been fixed in BIOS 1.18.

5. Disabling PXE support in BIOS does not correctly disable network boot support with a PCI NIC add-in card

- Problem** After setting BIOS <F2> setup "Advanced" sub-menu's "PXE Support" to disabled and rebooting, the <F2> boot menu still incorrectly displays the "Network Boot" as a boot option. The "Boot" menu then incorrectly displays the "Network Boot" device as "Intel UNDI, PXE-1.0 (Build Dev)."
- Implication** Users may incorrectly expect that the "Network" boot is still available since it is listed in the <F2> setup "Boot" sub-menu.
- Workaround** None
- Status** No fix. This is a limitation of the core Pheonix* BIOS. The "Network Boot" selected item in the "Boot" Menu is an unsupported legacy network boot ROM. The "PXE Support" (BBS) enabling no longer concurrently updates the "Boot" Menu in this core Pheonix* BIOS.

6. BIOS Boot menu does not differentiate between an IDE CD-ROM and USB CDROM boot device

- Problem** BIOS is unable to display the difference between a IDE CD-ROM and a USB CDROM. Both devices will be displayed as a "CD-ROM Drive" under <F2> setup "BOOT" sub-menu.
- Implication** If you concurrently install an IDE and an USB CD-ROM on SE7500CW2 you will be unable to determine which device is first in the boot-order in BIOS 1.17 and below.

Workaround Install the USB and IDE CD-CDROM separately. Between the installation of first device, say the USB CD-ROM, take note that this is the first device listed in the boot menu. Reboot and install the IDE CD-ROM. This will now be the second CD-ROM listed. Devices will be listed according to the order of installation.

Status Intel is investigating the possibility of fixing this erratum.LDCM 6.3 Wake on LAN not rebooting the server.

7. Wake on LAN functioning incorrectly

Problem Wake on LAN may not reboot the server in the event of a Wake on LAN event.

Implication LDCM may not send or receive Wake on LAN events. This will result in the server not being powered on as expected.

Workaround Make sure that both NICs are connected to the network. After doing this “Wake on LAN” will perform as designed.

Status **This has been fixed on resource CD A86445-008 and higher. It is also available for download at support.intel.com.**

8. Windows 2000 will not install on a Maxtor D540X-4G 137GIG ATA hard-drive

Problem Larger than 137GIG Maxtor ATA hard-drives do not give proper disk space information in Windows 2000 and are not recognized during the installation process.

Implication Windows 2000 installation will not find this 137GIG hard-drive. The current Promise drivers will not allow for this hard-drive to be recognized.

Workaround None

Status This has been fixed in BIOS 1.27 or above. This is available at <http://support.intel.com/support/motherboards/server/se7500cw2/>. Also, please check Microsoft’s Windows 2000 support web-site for additional operating system related issues.

9. Adaptec 2100S, 2110S, or 3410S, RAID cards cause LILO to hang during POST with Red Hat 7.3

Problem Red Hat Linux 7.3 will fail to boot when an Adaptec 2100S, 2110S, or 3410S, RAID card is installed and running Adaptec BIOS 1.60.

| | |
|--------------------|---|
| Implication | When running the Adaptec* card in “EBDA relocation” mode the system will not boot with Adaptec BIOS 1.60. Running Adaptec* BIOS v1.62 in conjunction with BIOS 1.17 will provide support for Adaptec* RAID cards mentioned above. Once installed it is still necessary to disable “EBDA relocation” in the Adaptec* RAID setup. |
| Workaround | None |
| Status | Pending production release of BIOS from Adaptec*, please contact Adaptec for availability. |

10. LDCM 6.3 build 211 incorrectly lowers processor fan speeds from 6000 RPM to fewer than 2000 RPM

| | |
|--------------------|--|
| Problem | LDCM 6.3 build 211 incorrectly lowers fan speeds on the Server Board SE7500CW2 only. |
| Implication | Installing and configuring LDCM 6.3 build 211 could possibly create thermal overheating issues. |
| Workaround | See Technical Advisory 612-01 for more details and patch availability. |
| Status | This has been fixed in on resource CD A86335-008 or higher. It is also available for download at http://support.intel.com/support/motherboards/server/se7500cw2/ta_612.htm . |

11. BIOS 1.17 incorrectly sets the BIOS EDBA memory area to 0 bytes.

| | |
|--------------------|---|
| Problem | Without EBDA BIOS memory allocation, PCI-based cards that require this space may have inconsistent performance. |
| Implication | Certain cards like High-Availability adapters may fail. |
| Workaround | None |
| Status | Fixed in BIOS 1.23. |

12. BIOS 1.17, 1.18 NIC disabling switch turns off the wrong NIC

| | |
|--------------------|--|
| Problem | If you disable NIC1 in F2 BIOS then NIC2 is turned off. If you disable NIC2 in F2 BIOS NIC1 is turned off. You will see this with the NIC LEDs on rear and on the SC5200 front panel NIC lights. |
| Implication | The wrong NIC could be disabled accidentally. |

Workaround None

Status Fixed in BIOS 1.23.

13. UUID not programmed on TA A88031-505, A88029-004, and A88030-003 below boards (PBA A87967-506)

Problem SyMBIOS UUID (unique board identifier) has not been programmed at the factory. This may make it difficult for such programs like Linux High Performance Clusters (HPC) to work properly.

Implication The only way to uniquely identify a SE7500CW2 board is by reading the bar code number sticker next to the Onboard Promise* RAID chip (PDC20267). An example of the unique identifier would be BPCW23701091.

Workaround none.

Status Fixed on PBA (A87967-507), A88031-507, A88029-007, and A88030-006, or higher. See PCN #103036-01 (ECO #6052488) for more details.

14. Logical processors are no longer listed in BIOS POST if hyper-threading is enabled in F2 BIOS setup

Problem Logical processors are not listed in BIOS 1.18 and above even if hyper-threading is enabled in BIOS. Logical processors are no longer mentioned with the text string of “4 Logical Intel Xeon 2.8 Ghz processors” if hyper-threading is enabled with two processors populated.

Implication There may be confusion as to whether hyper-threading is really working.

Workaround None

Status The change has been implemented in BIOS 1.23 and above. This is by design and now the text string reads “Intel Xeon Processors 2.8GHz” even if hyper-threading is enabled. The number of logical processors is no longer listed. Only the printed POST string has changed, but the functionality of hyper-threading remains identical in BIOS and on the board.

15. Memory count takes over 2 minutes with 2 GB of memory

Problem There is no “QuickBoot” F2 BIOS switch in BIOS Advanced menus that other platforms have.

Implication It is necessary to wait up to two minutes to count the memory if the <ESC> is not selected.

Workaround Use the <ESC> key during the memory count to disable the memory count. This step must be done each time the server board is reset or powered on.

Status Intel is investigating the possibility of fixing this erratum.

16. Server board fails to power off server after “init 0” under Red Hat Linux 8.0

Problem The power does not power off, though the system has shutdown and hangs at the “power off” message after downing all the Linux daemons.

Implication Power remains connected.

Workaround None

Status Intel will not fix this erratum. This is a limitation in Red Hat 8.0 which only shutdowns the server but will no disconnect the AC power.

17. Windows 2000 will not display the full size of ATA hard-drives larger than 137GB

Problem Windows 2000 will not display the full size of ATA hard-drives larger that 137GB. This is not a problem on other operating systems like NetWare 6.0, or Red Hat 8.0 Linux.

Implication Drives will boot, but will not display the full hard-drive size.

Workaround None

Status Fixed. Please download and upgrade to web-posted BIOS v1.27 found at (<http://support.intel.com>) or http://downloadfinder.intel.com/scripts-df/Detail_Desc.asp?agr=N&ProductID=858&DwnldID=5515 .

18. Intel Xeon processors with D1 stepping will not operate under BIOS 1.27 and below.

| | |
|--------------------|---|
| Problem | BIOS microcode is not included in all production BIOSes between v1.10 to 1.27. Newer processors which support the new D1 stepping will not work with BIOS v1.27, or below, since it contains unsupported BIOS microcode. Intel® Xeon processors with older C1 stepping will continue to work even when a newer BIOS microcode is available. Only processors with the D1 stepping will fail to work on BIOSes below v1.27. |
| Implication | As of June 13, when Intel Xeon processors that support D1 stepping are available. It is necessary to upgrade to BIOS v1.28 for D-1 stepping based processors only. Typically Intel BIOSes support +/-1 processor steppings. In other, words C-1 and D-1 stepping processors will work with BIOS v1.28. |
| Workaround | None |
| Status | Intel plans to support the new D1 stepping in BIOS v1.28. At this time the Server Board SE7501CW2 will support D1 stepping Intel Xeon processors. Please download on existing Server Board SE7501CW2 when available in late Q2 2003 at http://support.intel.com/support/motherboards/server/se7501cw2/ |

19. Microsoft Windows 2003 is not supported on the Server Board SE7500CW2

| | |
|--------------------|---|
| Problem | Microsoft Windows Server 2003 drivers and adapters may fail on Server Board SE7500CW2. |
| Implication | Microsoft Windows Server 2000 drivers may not all work correctly. |
| Workaround | Consider using the Server Board SE7501CW2 as an alternate solution. This server board includes support for Microsoft Windows Server 2003. |
| Status | Support for Windows 2003 we be ready early Q3, 2003. The latest information is available at http://support.intel.com/support/motherboards/server/win2003.htm |

20. Ambient temperature appears to be too warm by over 5 degrees Celsius

| | |
|----------------|---|
| Problem | All BIOS revisions prior to BIOS 1.27 incorrectly reported the ambient temperature as 5 degrees too warm. This was reported incorrectly in both <F2> Advanced Hardware Monitor Ambient temperature, and LANDesk Client Manager 6.3. |
|----------------|---|

Implication Potentially LANDesk Client Manger could send a system alert and even shut-down a server too early.

Workaround None

Status Fixed in production BIOS V1.27. Please upgrade and follow instructions as listed at: <http://support.intel.com/support/motherboards/server/se7501cw2/>

Glossary

| Term | Definition |
|------------------|---|
| ACPI | Advanced Configuration and Power Interface |
| ANSI | American National Standards Institute |
| AP | Application Processor |
| ASIC | Application Specific Integrated Circuit |
| ASR | Asynchronous Reset |
| BGA | Ball-grid Array |
| BIOS | Basic input/output system |
| BIST | Built-in self test |
| Bridge | Circuitry connecting one computer bus to another, allowing an agent on one to access the other. |
| BSP | Bootstrap Processor |
| Byte | 8-bit quantity. |
| CIOB | PCI 64-bit hub |
| CMOS | In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board. |
| CSB5 | Legacy I/O controller hub |
| DCD | Data Carrier Detect |
| DMA | Direct Memory Access |
| DMTF | Distributed Management Task Force |
| ECC | Error Correcting Code |
| EMC | Electromagnetic Compatibility |
| EMP | Emergency management port. |
| EPS | External Product Specification |
| ESCD | Extended System Configuration Data |
| FDC | Floppy Disk Controller |
| FIFO | First-In, First-Out |
| FRB | Fault resilient booting |
| FRU | Field replaceable unit |
| GB | 1024 MB. |
| GPIO | General purpose I/O |
| GUID | Globally Unique ID |
| Hz | Hertz (1 cycle/second) |
| HDG | Hardware Design Guide |
| I ² C | Inter-integrated circuit bus |
| IA | Intel® architecture |
| ICMB | Intelligent Chassis Management Bus |
| IERR | Internal error |
| IMB | Inter Module Bus |
| IP | Internet Protocol |
| IPMB | Intelligent Platform Management Bus |
| IPMI | Intelligent Platform Management Interface |
| IRQ | Interrupt Request |
| ISC | Intel® Server Control |
| ITP | In-target probe |

| Term | Definition |
|---------|--|
| KB | 1024 bytes |
| KCS | Keyboard Controller Style |
| LAN | Local area network |
| LBA | Logical Block Address |
| LCD | Liquid crystal display |
| LPC | Low pin count |
| LSB | Least Significant Bit |
| LVD | Low-Voltage Differential |
| LVDS | Low-Voltage Differential SCSI |
| MB | 1024 KB |
| MBE | Multi-Bit Error |
| Ms | milliseconds |
| MSB | Most Significant Bit |
| MTBF | Mean Time Between Failures |
| Mux | multiplexor |
| NIC | Network Interface Card |
| NMI | Non-maskable Interrupt |
| OEM | Original equipment manufacturer |
| Ohm | Unit of electrical resistance |
| P32-A | 32-bit PCI Segment |
| P64-B | Full Length 64/66 MHz PCI Segment |
| P64-C | low-profile 64/66 MHz PCI Segment |
| PBGA | Pin Ball Grid Array |
| PDB | Power Distribution Board |
| PEF | Platform Event Filtering |
| PERR | Parity Error |
| PET | Platform Even Trap |
| PIO | Programmable I/O |
| PMB | Private Management Bus |
| PMC | Platform Management Controller |
| PME | Power Management Event |
| PnP | Plug and Play |
| POST | Power-on Self Test |
| PWM | Pulse-Width Modulator |
| RAIDIOS | RAID I/O Steering |
| RAM | Random Access Memory |
| RI | Ring Indicate |
| RISC | Reduced instruction set computing |
| RMCP | Remote Management Control Protocol |
| ROM | Read Only Memory |
| RTC | Real Time Clock |
| SAF-TE | SCSI Accessed Fault-Tolerant Enclosure Specification |
| SBE | Single-Bit Error |
| SCI | System Configuration Interrupt |
| SDR | Sensor Data Record |

| Term | Definition |
|--------|--|
| SDRAM | Synchronous Dynamic RAM |
| SEL | System event log |
| SERIRQ | Serialized Interrupt Requests |
| SERR | System Error |
| SM | Server Management |
| SMI | Server management interrupt. SMI is the highest priority nonmaskable interrupt |
| SMM | System Management Mode |
| SMS | System Management Software |
| SNMP | Simple Network Management Protocol |
| SPD | Serial Presence Detect |
| SSI | Server Standards Infrastructure |
| SSU | Server Setup Utility |
| TPS | Technical Product Specification |
| UART | Universal asynchronous receiver and transmitter |
| USB | Universal Serial Bus |
| VGA | Video Graphic Adapter |
| VID | Voltage Identification |
| VRM | Voltage Regulator Module |
| Word | 16-bit quantity |
| ZCR | Zero Channel RAID |

Reference Documents

Refer to the following documents for additional information:

- *PCI Local Bus Specification* Revision 2.2 (www.pcisig.org)
- *ATI RAGE XL Graphics Controller Specifications, Technical Reference Manual*, Rev 2.01 (www.ati.com)
- SE7500CW2 BIOS External Product Specification rev 1.0¹
- SE7500CW2 Baseboard External Product Specification 1.0¹
- Windbond** 83627HF Super I/O Controller Technical Reference, rev 1.0 (www.Windbond*.com)

¹ Please contact your Intel field person for information on how to obtain this document.