SCB2 Server Board

Technical Product Specification

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Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
8/1/01	.05	First preliminary release.
10/05/01	1.0	First production level release.
12/31/01	1.1	Added Riser Card appendix, added PCI riser pin-out tables,
8/20/02	2.0	Added Appendix C: SCB2 Errata; modified BIOS setup section to reflect options in most recent BIOS; added items to Appendix A; updated POST code table

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1. Introduction

The SCB2 Technical Product Specification (TPS) provides a high level technical description for the Intel® SCB2 Server Board. It details the architecture and feature set for all functional subsystems that make up the server board.

This document is sub-divided into the following main categories:

Chapter 2: Hardware Overview

Chapter 3: Hardware Architecture

Chapter 4: Platform Management Architecture

Chapter 5: System BIOS

Chapter 6: Error Handling and Reporting

Chapter 7: Connectors and Jumper Blocks

Chapter 8: General Specifications

The contents of this document are derived from several of the SCB2's External Product Specifications (EPS). For a more detailed, lower level description of a particular functional subsystem, the EPS for the sub-system should be ordered from your Intel field representative. The EPS documents available for the SCB2 server board include the following:

- SCB2 BIOS EPS
- SCB2 Baseboard Management Controller EPS
- Sahallee Core BMC EPS for IPMI v1.5
- SCB2 Server Management EAS
- Platform Instrumentation EPS
- Direct Platform Control EPS
- FRUSDR Loader EPS
- LAN Alert Viewer EPS

The SCB2 server board supports the Intel® Server Control Version 3.5 server management software. Several additional EPS documents are available to provide technical detail on the feature set of the server management software. These include:

- ISC Console EPS
- ISC Install EPS
- Service Partition EPS
- Client System Setup Uility EPS
- ISC Customization Guide

2.   SCB2 Server Board Overview

The SCB2 server board is a monolithic printed circuit board with features that were designed to support the high-density 1U and 2U server market.

2.1   SCB2 Feature Set

There are two different SCB2 server boards available, each offering a different onboard hard drive controller. One will provide an embedded Ultra-160* SCSI interface and the other will provide an embedded ATA-100* "Valu-Raid" interface. Both boards support the following feature set:

- Dual Intel® Pentium III® processors with 256 KB[1] or 512 KB L2 cache
- 133 MHz Front Side Bus
- ServerWorks ServerSet* III HE-SL chipset
    - HE-SL North Bridge
    - CIOB20 I/O Bridge
    - CSB5 South Bridge

- Support for up to six PC-133 compliant registered ECC SDRAM DIMMs providing up to 6 GB of memory
- Three separate and independent PCI buses:
    - Segment A: 32-bit, 33 MHz, 5 V (P32-A) with four embedded devices:
        1. 2D/3D graphics controller: ATI Rage* XL Video Controller with 8 MB of SDRAM
        2. Two Intel10/100 82550PM Fast Ethernet Controllers
        3. ATA-100 controller: Promise Technology* PDC20267 *(ATA-100 version only)*
    - Segment B: 64-bit, 66 MHz, 3.3 V, (P64-B) supporting the following configuration:
        4. One PCI I/O riser slot capable of supporting full length PCI add-in cards
        5. Dual-channel Adaptec* AIC-7899W wide Ultra-160 SCSI Controller providing one internal and one high density external channel support:*(SCSI version only)*
        6. Zero Channel RAID (ZCR) support. *(SCSI version only)*

    - Segment C: 64-bit, 66/33 MHz, 3.3 V (P64-C) supporting the following device:
        7. One PCI I/O riser slot capable of supporting low-profile PCI add-in cards

- LPC (Low Pin Count) bus segment with two embedded devices:
    - Platform Management Controller (PMC) providing monitoring, alerting, and logging of critical system information obtained from embedded sensors on the server board
    - Super I/O controller chip providing all PC-compatible I/O (floppy, serial, keyboard, mouse)

- X-Bus segment with one embedded device:

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[1] The SCB2 server board supports Intel Pentium III processors with 256 KB or 512 KB L2 cache that use the socket370 FCPGA2 processor package. Intel Pentium III processors with 256 KB L2 cache, that use the FCPGA processor package, are not supported on the SCB2.

- Flash ROM device for system BIOS: Intel 32 megabit 28F320C3 Flash ROM

- Two external Universal Serial Bus (USB) ports with an additional internal header providing two optional USB ports for front panel support. (USB 1.1 Compatible)

- One external low-profile RJ45 serial 2 port, with an optional serial 2 interface for front panel support. An internal header is also available providing an optional serial 1 (COM1) port.

- One IDE connector, supporting one or two ATA-33 compatible devices

- Support for up to six system fans

- Fault/Status LEDs throughout the server board

- Multiple server management headers providing on-board interconnects to server management features

- SSI-compliant connectors for SSI interface support: front panel, floppy, and ATA-33

The figure below shows the functional blocks of the server board and the plug-in modules that it supports.
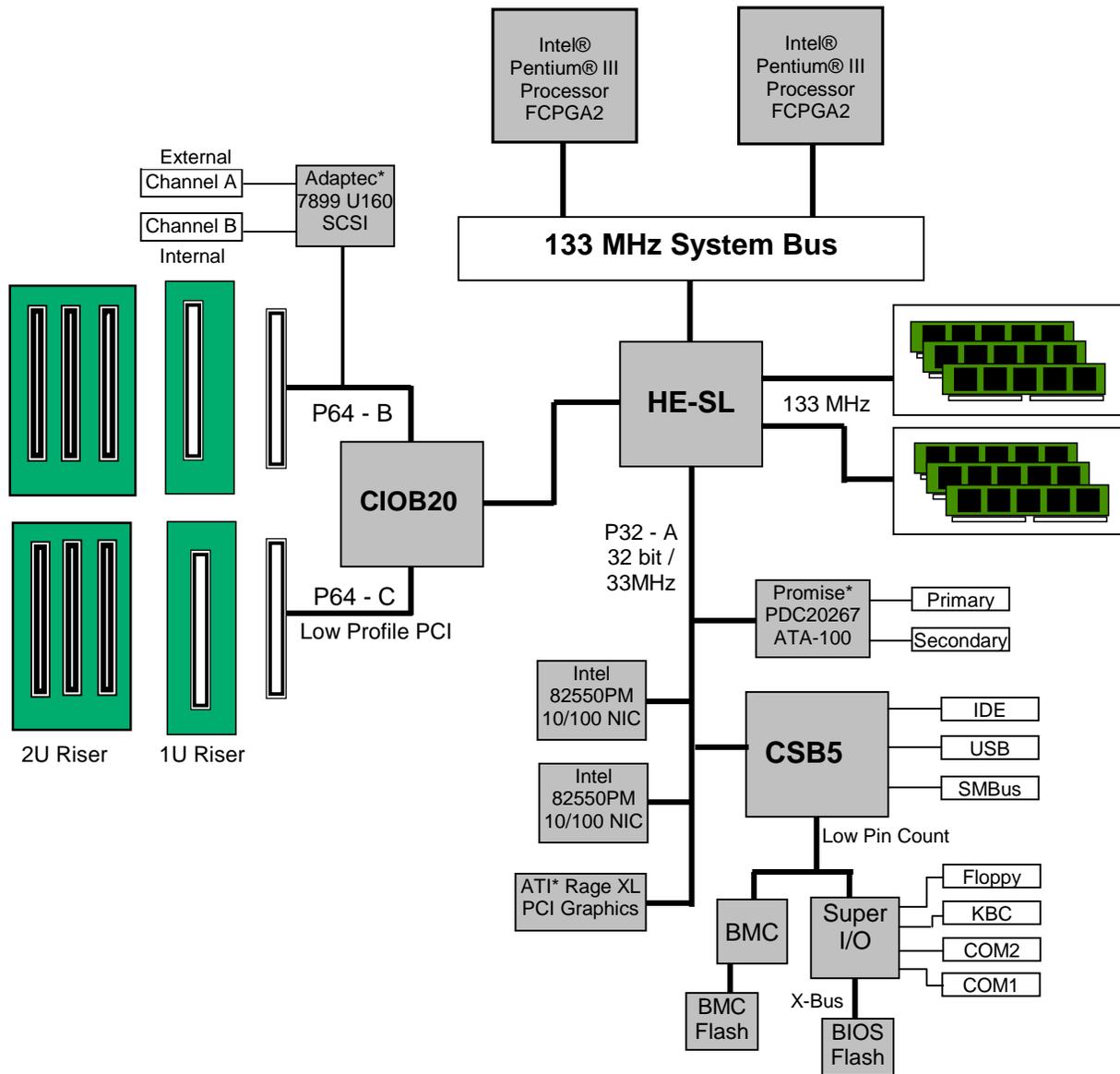
Figure 1. SCB2 Server Board Block Diagram

3.   Functional Architecture

This chapter provides a high-level description of the functionality distributed between the architectural blocks of the SCB2 server board.

3.1   Processor and Memory Subsystem

The ServerSet III HE-SL chipset provides a 36-bit address, 72-bit data (64-bit data + 8-bit ECC) processor host bus interface, operating at 133 MHz in the AGTL signaling environment. The HE-SL component of the chipset provides an integrated memory controller, the interface to a 32-bit, 33-MHz, Rev 2.2-compliant PCI bus, and two Inter-Module Bus (IMB) interfaces.

The IMB provides the interface to two 64-bit, 66-MHz, Rev 2.2-compliant PCI buses via the CIOB20. The SCB2 server board directly supports up to 6 GB of ECC memory, using six PC/133-compliant registered SDRAM DIMMs. The ECC implementation in the HE-SL can detect and correct single-bit errors, and it can detect multiple-bit errors.

3.1.1   Processor Support

The SCB2 server board supports one or two Intel Pentium III processors with 256 KB[2] or 512 KB L2 cache. The server board will support all versions of the Pentium III DP processor that use the Socket370 FCPGA2 package. When two processors are installed, all processors must be of identical revision, core voltage, and bus/core speed. When only one processor is installed, the other socket must have an AGTL terminator card installed. The support circuitry on the server board consists of the following:

- Dual Socket370 FCPGA2 CPU sockets supporting 133 MHz FSB (if using one processor, an AGTL terminator card goes in the empty socket).
- Processor host bus AGTL support circuitry, including termination power supply.

Table 1. SCB2 Processor Support Matrix

Processor Family	Package Type	Processor Code Name	Frequency	Cache Size	Single/Dual Processor Capable	SCB2 Support
Intel Pentium III	FCPGA	Coppermine (A – D step)	866 MHz – 1GHz	256KB	Dual	**No**
Intel Pentium III	FCPGA2	Coppermine-T	1 GHz and faster	256KB	Dual	Yes
Intel Pentium III	FCPGA2	Tualatin	All	256KB	Single	Yes
Intel Pentium III	FCPGA2	Tualatin	All	512KB	Dual	Yes

Notes: All processor sockets must be populated with either a processor or a termination module. The BMC will not allow DC power to be applied to the system unless both processor sockets contain a properly seated processor or termination module.
Processors must be populated in sequential order. That is, processor socket #1 must be populated before processor socket #2.

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[2] The SCB2 server board supports Intel Pentium III processors with 256 KB or 512 KB L2 cache that use the socket370 FCPGA2 processor package. Intel Pentium III processors with 256 KB L2 cache, that use the FCPGA processor package, are not supported on the SCB2.

In addition to the circuitry described above, the processor subsystem contains the following:

- Reset configuration logic.
- Processor module presence detection logic.
- APIC bus.
- Server management registers and sensors.

3.1.1.1   Processor VRM

The SCB2 baseboard has a single VRM (voltage regulator module) to support two processors. It is compliant with the VRM 8.5 specification and provides a maximum of 60 AMPs, which is capable of supporting current supported processors as well as those supported in the future.

The board hardware and BMC must read the processor VID (voltage identification) bits for each processor before turning on the VRM. If the VIDs of the two processors are not identical, then the BMC will not turn on the VRM and a beep code is generated.

3.1.1.2   Reset Configuration Logic

The BIOS determines the processor stepping, cache size, etc. through the CPUID instruction. The requirements are as follows:

- All processors in the system must operate at the same frequency and have the same cache sizes. No mixing of product families is supported.

- Processors run at a fixed speed and cannot be programmed to operate at a lower or higher speed.

Note: When the CMOS clear function is enabled, the BIOS defaults the processor frequency to a safe mode at 533 MHz when <u>pre-production</u> unlocked processors are used.

On the SCB2 platform, the BIOS is responsible for configuring the processor speeds. The BIOS uses CMOS settings to determine which speed to program into the speed setting device (I^2C^*-based EEPROM Mux).

The processor information is read at every system power-on. The EEMUX is set to correspond to the speed of the slowest processor installed.

Note: No manual processor speed setting options exist either in the form of a BIOS Setup option or jumpers when using production level processors.

3.1.1.3   Processor Module Presence Detection

Logic is provided on the baseboard to detect the presence and identity of installed processors or termination card. The BMC checks the logic and will not turn on the system DC power until the processor bus is terminated properly.

3.1.1.4   APIC Bus

Interrupt notification and generation for the processors are done using an independent path between local APICs in each processor and the I/O APIC in the CSB5 located on the baseboard. This independent bus consists of two data signals and one clock line.

3.1.1.5   Server Management Registers and Sensors

The baseboard management controller manages registers and sensors associated with the processor / memory subsystem.

3.1.2   Memory Subsystem

The SCB2 server board provides six DIMM slots and supports a maximum memory capacity of 6 GB. The DIMM organization is x72 which includes eight ECC check bits. ECC from the DIMMs are passed through to the processor's front side bus. The SDRAM interface runs at the same frequency as the processor bus. The memory controller supports memory scrubbing, single-bit error correction and multiple-bit error detection. Memory can be implemented with either single-sided (one row) or double-sided (two row) DIMMs.

Note: Due to the use of vertical or 90 degree DIMM slots, only low profile DIMMs can be supported in a 1U server chassis.

Data transfers between the HE-SL and DIMMs in a two-way interleaved fashion. This requires that two DIMMs be populated per bank in order for the system to operate. At least one bank has to be fully populated in order for the system to boot. If additional banks have less than two DIMMs, the memory for that bank(s) will not be available to the system. The smallest supported DIMM size is 64 MB. Therefore, the minimum main memory configuration is 2 x 64 MB or 128 MB. The largest size DIMM supported is a 1-GB stacked registered PC-133 ECC DIMM based on 256-Mbit technology.

The figure below provides a block diagram of the memory sub-system implemented on the SCB2 server board.
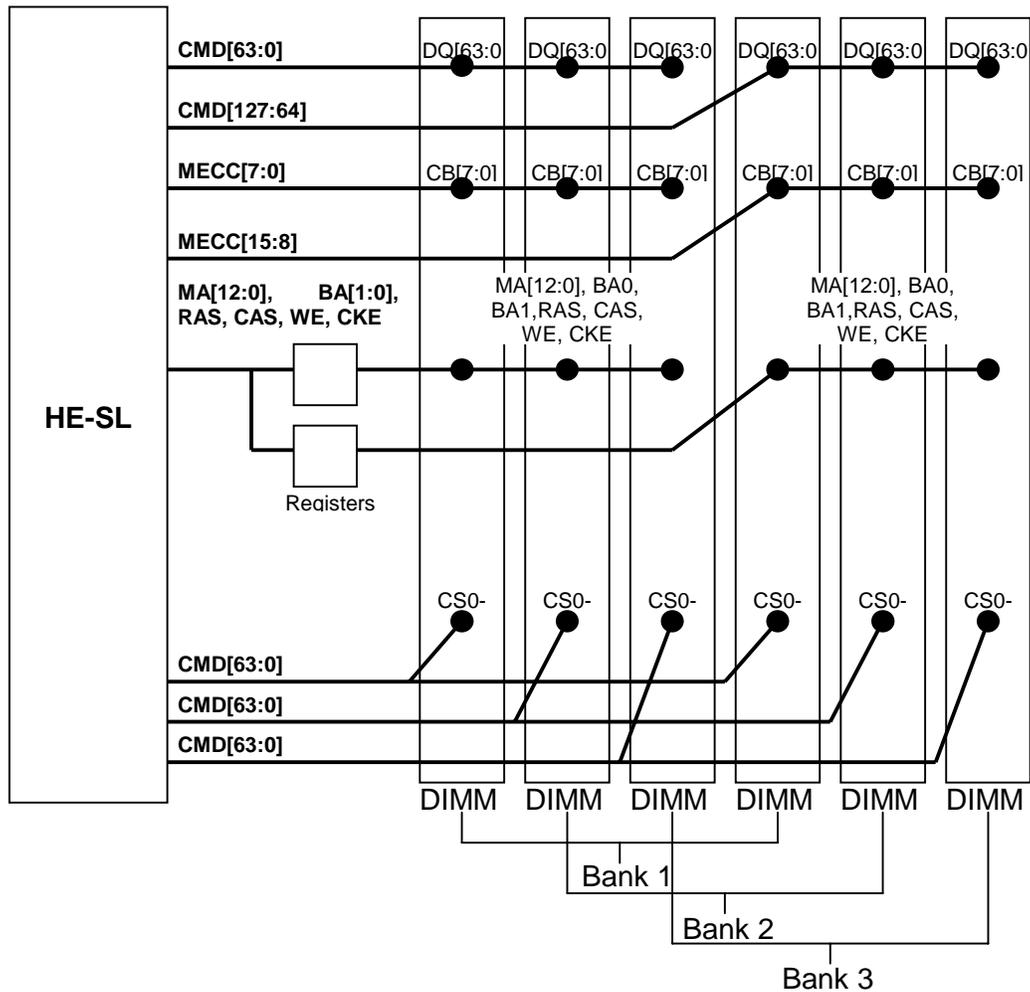
Figure 2. Memory Sub-system Block Diagram

There are three banks of DIMMs; labeled as 1, 2, and 3. Bank 1 contains DIMM locations 1A and 1B, bank 2 contains 2A and 2B, and bank 3 contains 3A and 3B. DIMM socket identifiers are marked with a silk screen next to each DIMM socket on the baseboard. Note that the sockets associated with any given bank are NOT located next to each other.

The baseboard's signal integrity and cooling are optimized when memory banks are populated in order. Therefore, when installing memory, DIMMs should be installed starting with bank 1 and ending with bank 3.

Table 2. Memory Bank Labels

Memory DIMM	Bank	Row
J5E1 (DIMM 1A), J6E2 (DIMM 1B)	1	0, 3
J5E2 (DIMM 2A), J6E3 (DIMM 2B)	2	1, 4
J6E1 (DIMM 3A), J7E1 (DIMM 3B)	3	2, 5
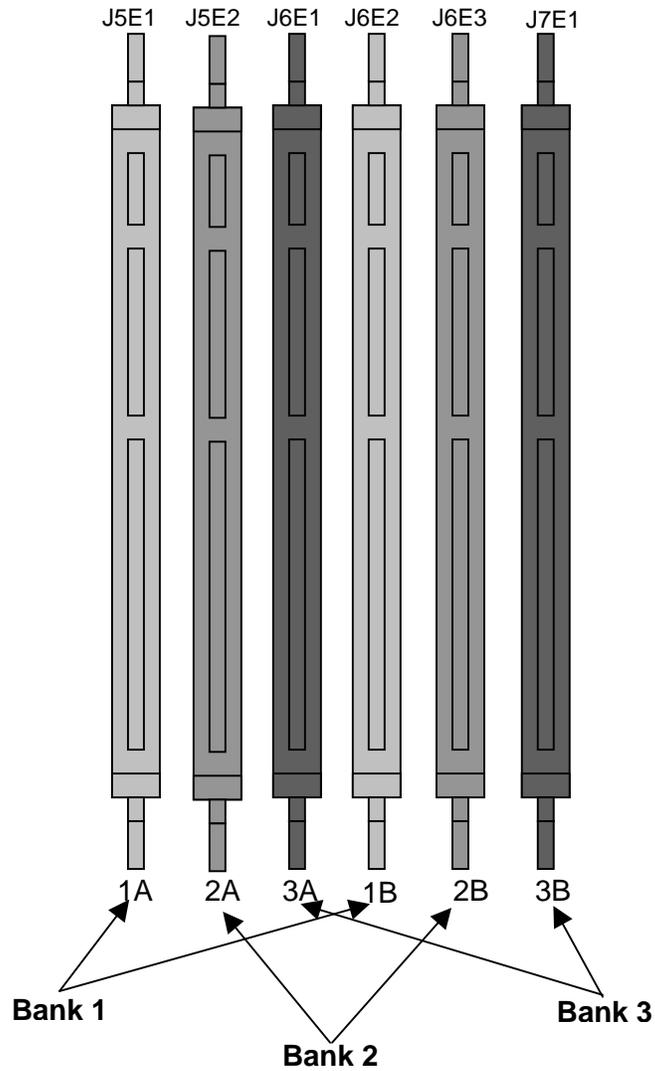
Figure 3. Memory Bank Label Definition

DIMM and memory configurations must adhere to the following:

- PC133 SDRAM registered ECC DIMM modules
- DIMM organization: x72 ECC
- Pin count: 168
- DIMM capacity: 64 MB, 128 MB, 256 MB, 512 MB, 1 GB DIMMs
- Serial PD: JEDEC Rev 2.0
- Voltage Options: 3.3 V (VDD/VDDQ)
- Interface: LVTTL
- Two DIMMs must be populated in a bank for a x144 wide memory data path.
- Any or all memory banks may be populated

Only DIMMs tested and qualified by Intel or a designated memory test vendor will be supported on the SCB2 server board. A list of qualified memory can be downloaded from the following web site: http://support.intel.com/support/motherboards/server/scb2/scb2_mem.htm .

Note that all DIMMs are supported by design, but only fully qualified DIMMs will be supported.

3.1.2.1   I^{2}C* Bus

An I^{2}C bus is between the Baseboard Management Controller (BMC) and the six DIMM slots. This bus is used by the system BIOS to retrieve DIMM information needed to program the HE-SL memory registers which are required to boot the system.

3.2   ServerWorks ServerSet* III HE-SL Chipset

The SCB2 server board is designed around the ServerWorks ServerSet III HE-SL chipset. The chipset provides an integrated I/O bridge and memory controller and a flexible I/O subsystem core (PCI), targeted for multiprocessor systems and standard high-volume servers. The ServerWorks ServerSet III chipset consists of three components:

- **HE-SL: Champion North Bridge.** The HE-SL North Bridge accepts access requests from the host (processor) bus and directs those accesses to memory or to one of the PCI buses. The HE-SL monitors the host bus, examining addresses for each request. Accesses may be directed to a memory request queue for subsequent forwarding to the memory subsystem, or to an outbound request queue for subsequent forwarding to one of the PCI buses. The HE-SL also accepts inbound requests from the CIOB20 and the legacy PCI bus. The HE-SL is responsible for generating the appropriate controls to control data transfer to and from memory.

- **CIOB20: Champion I/O Bridge.** The CIOB20 provides the interface for two 64-bit, 66-MHz Rev. 2.2-compliant PCI buses. The CIOB is both master and target on both PCI buses.

- **CSB5: South Bridge.** The CSB5 controller has several components. It provides the interface for a 32-bit, 33-MHz Rev. 2.2-compliant PCI bus. The CSB5 can be both a master and a target on that PCI bus. The CSB5 also includes a USB controller and an IDE controller. The CSB5 is also responsible for much of the power management

functions, with ACPI control registers built in. The CSB5 also provides a number of GPIO pins and has the LPC bus to support a low-speed legacy I/O.

The CNB20HE-SL, CIOB, and CSB5 chips provide the pathway between processor and I/O systems. The CNB20HE-SL is responsible for accepting access requests from the host (processor) bus, and directing all I/O accesses to one of the PCI buses or legacy I/O locations. If the cycle is directed to one of the 64-bit PCI segments, the HE-SL communicates with the CIOB through a private interface called the IMB. If the cycle is directed to the 32-bit PCI segment or to the CSB5, the cycle is output on the HE-SL's 32-bit PCI bus. The CIOB translates the IMB bus operation to a 64-bit PCI Rev. 2.1-compliant signaling environment operating at either 66 MHz or 33 MHz.

The IMB bus consists of two data paths, one upstream (to the CNB20HE-SL from the CIOB) and one downstream (from the CNB20HE-SL to the CIOB). The interface is 16 bits wide and operates at 133 MHz with double pumped data, providing over 1 GB per second of bandwidth or 533 MB per second in each direction concurrently.

All I/O for the SCB2, including PCI and PC-compatible, is directed through the CNB20HE-SL, and then through either the CIOB or the HE-SL provided PCI buses.

- The HE provides a 32-bit, 33-MHz PCI bus hereafter called P32-A.
- The CIOB provides two independent 64-bit, 66-MHz PCI buses hereafter called P64-B, and P64-C.

This independent bus structure allows all three PCI buses to operate concurrently and provides 1.2 GB per second of I/O bandwidth.

3.2.1   CNB20HE-SL Champion North Bridge

The Champion North Bridge Rev 2.0 High End Super Lite (CNB20HE-SL) is the third generation product in ServerWorks's Champion North Bridge Technology. The CNB20HE-SL is a 644-pin ball-grid array (BGA) device and uses the proven components of previous generations like the Pentium® Pro Bus interface unit, the PCI interface unit and the SDRAM memory interface unit. In addition, the CNB20HE-SL incorporates an Intra Module Bus (IMB) Interface. The IMB interface enables the CNB20HE-SL to directly interface with the CIOB20. The CNB20HE-SL also increases the main memory interface bandwidth and maximum memory configuration with a 144-bit wide memory interface.

The CNB20HE-SL integrates three main functions:

- An integrated, high performance main memory subsystem
- An IMB bus interface that provides a high-performance data flow path between the processor bus and the I/O subsystem
- A PCI interface which provides an interface to the compatibility PCI bus segment and the CSB5 (South Bridge).

Other features provided by the CNB20HE include the following:

- Full support of ECC on the processor bus.
- Full support of ECC on the memory interface.

- Eight deep in-order queue.
- Full support of registered PC-133 ECC SDRAM DIMMs.
- Support for 6 GB of 2-way interleaved SDRAM
- Memory scrubbing

3.2.1.1   Memory Architecture Overview

The CNB20HE-SL supports a 2-way interleaved memory sub-system that can support a maximum of 6 Gbytes (using 1GB DIMMs). The memory interface runs at 133 MHz, matching that of the processor front side bus. The memory interface supports a 144-bit wide memory array. It uses fifteen address lines (BA[1:0] and MA[12:0]) and supports 1Mx72, 2Mx72, 4Mx72, 8Mx72, 16Mx72, 32Mx72, 64Mx72, and stacked 128Mx72 DIMMs. The SDRAM DIMM interface supports memory scrubbing, single-bit error correction, and multiple-bit error detection.

3.2.1.2   PCI Bus P32-A I/O Subsystem

The CNB20HE-SL provides a legacy 32-bit PCI subsystem and acts as the central resource on this PCI interface.

P32-A supports the following embedded devices and connectors:

- CSB5 - South Bridge.
- Two Intel 82550PM 10/100 Fast Ethernet PCI network interface controllers
- An ATI Rage* XL video controller with 3D/2D graphics accelerator
- Promise Technology* PDC20267 Dual channel ATA-100 Controller. (ATA-100 board only)

3.2.2   CIOB

The Champion I/O Bridge (CIOB) is a 352-pin ball-grid array device and provides an integrated I/O bridge that provides a high-performance data flow path between the IMB and the 64-bit I/O subsystem. This subsystem supports peer 64-bit PCI segments. Having multiple PCI interfaces, the CIOB is able to provide large and efficient I/O configurations. The CIOB functions as the bridge between the IMB and the multiple 64-bit PCI I/O segments.

The IMB interface is capable of supporting 512 MB/s of data bandwidth in both the upstream and downstream direction simultaneously.

The internal PCI arbiter implements the Least Recently used algorithm to grant access to requesting masters.

3.2.2.1   PCI Bus P64-B I/O Subsystem

P64-B supports the following embedded devices and connectors:

- One 184-pin, 5-volt keyed, 64-bit PCI expansion slot connector. The expansion slot can be used for either a 1-slot or a 3-slot PCI riser card. The riser cards both support 184-pin, 3.3V keyed, 64-bit PCI expansion slots. The PCI slots on the P64-B PCI bus support both full-length PCI cards and low-profile PCI cards with the appropriate face plate.

- One Adaptec 7899 dual channel Ultra-160 SCSI controller. (**SCB2-SCSI Only)

- Support for ZCR or M-ROMB that allows the on-board SCSI controller to be "hidden" from the system and used by the RAID processor on the add-in card. (**SCB2-SCSI board only)

3.2.2.2   PCI Bus P64-C I/O Subsystem

P64-C supports one 184-pin, 5-Volt keyed, 64-bit PCI expansion slot connector. The expansion slot can be used for either a 1-slot or a 3-slot PCI riser card. Both riser cards support 184-pin, 3.3V keyed, 64-bit PCI expansion slots. The PCI slots on the P64-C PCI bus support only low-profile PCI cards due to component interferences on the server board.

3.2.3   CSB5

The CSB5 is a multi-function PCI device, housed in a 272-pin BGA device, providing a PCI-to-LPC bridge, a PCI IDE interface, a PCI USB controller, and a power management controller. Each function within the CSB5 has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface.

On the SCB2 server board, the primary role of the CSB5 is to provide the gateway to all PC-compatible I/O devices and features. The SCB2 uses the following CSB5 features:

- 32-bit/33MHz PCI bus interface
- LPC bus interface
- IDE interface, with Ultra DMA 33 capability
- USB interface
- PC-compatible timer/counter and DMA controllers
- APIC and 8259 interrupt controller
- Power management
- General purpose I/O (GPIO)

The following are the descriptions of how each supported feature is used on SCB2.

3.2.3.1   PCI Bus Interface

The CSB5 provides a 32-bit 33 MHz PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Revision 2.2*.

3.2.3.2   PCI Bus Master IDE Interface

The CSB5 acts as a PCI-based Ultra DMA/33 IDE controller that supports programmed I/O transfers and bus master IDE transfers. The SCB2 provides two separate but common interfaces to the IDE controller which can support up to two drives. The first interface is a single SSI compliant 40-pin (2x20) IDE connector located on the edge of the baseboard next to the main power connector. The second interface is provided through the high-density 100-pin floppy / IDE / front panel connector that is used with Intel's SR1200 and SR2200 server chassis.

Note: Using both the SSI IDE connector and the high-density "Floppy/IDE/Front Panel" connector in a common configuration is not supported. Using both connectors in a common configuration may result in unreliable data transfers and can cause data corruption.
The SCB2 IDE interface supports Ultra DMA/33 Synchronous DMA Mode transfers.

3.2.3.3   USB Interface

The CSB5 contains a USB controller and four USB hubs compliant with the USB 1.1 specification. The USB controller moves data between main memory and the four USB connectors. All four ports function identically and with the same bandwidth.

The SCB2 provides two external USB ports located on the back edge of the server board. The first external connector is located within the standard ATX* I/O panel area while the second is located directly behind the P64-B full-length PCI card slot. The USB specification defines the external connectors.

The third and fourth USB ports are optional and can be accessed by cabling the internal 9-pin connector located on the baseboard (J10G1) to external USB ports located either in front or the back of a given chassis.

3.2.3.4   Compatibility Interrupt Control

The CSB5 provides the functionality of two 82C59 PIC devices for ISA-compatible interrupt handling.

3.2.3.5   APIC

The CSB5 integrates a 32-entry I/O APIC that is used to distribute 32 PCI interrupts. It also includes an additional 16-entry I/O APIC for distribution of legacy ISA interrupts.

3.2.3.6   General Purpose Input and Output Pins

The CSB5 provides a number of general purpose input and output pins. Many of these pins have alternate functions and are not available.

3.2.3.7   Power Management

One of the embedded functions of the CSB5 is a power management controller. The SCB2 server board uses this to implement ACPI-compliant power management features. The SCB2 supports sleep states S0, S1, S4, and S5.

3.3   Super I/O

The National Semiconductor* PC87417 Super I/O device contains the system Real Time Clock (RTC), all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. The SCB2 server board supports the following features:

- GPIOs
- Two Serial Ports
- Floppy Disk

- Keyboard and mouse through a single PS/2 connector
- System Real Time Clock
- Wake Up Control

Note: The SCB2 does not support a parallel port.

3.3.1   GPIOs

The National Semiconductor PC87417 Super I/O provides a number of GPIO pins. The following table identifies which functions are utilized on the SCB2:

Table 3. Super I/O GPIO Usage Table

Description
Power Supply Off button
Diagnostic LED strobe
Current Sleep S5 State
SIO Requested Power Off
Sleep Button from SIO
Diagnostics LED Data
Board ID 0– Used to identify revision of board
Board ID 1– Used to identify revision of board
Board ID 2– Used to identify revision of board
Front Panel Power Idicator
PME# from P64-B
PME from NICs

3.3.2   Real-time Clock

The Super I/O contains an RTC with an external battery backup. The device also contains 242 bytes of general purpose, battery-backed CMOS RAM.

3.3.3   Serial Ports

The SCB2 server board provides two serial ports, Serial 1 and Serial 2. Serial 1 is optional with its signals accessed through an internal connector on the baseboard. Serial 2 has multiple interfaces and is typically used to access the server management features of the baseboard.

Note: In order to comply with Microsoft* WHQL requirements, all references to serial ports utilizing an RJ-45 type of connector will be denoted as "Serial 2 Port" only. References to the RJ45 serial port as "COM2" will not be used.

3.3.3.1   Serial 1 Port

Serial 1 is an optional port, accessed through a 9-pin internal connector (J9B2). A standard DH-10 to DB9 cable can be used to direct Serial 1 signals out the back of a given chassis. The Serial 1 interface follows the standard RS232 pinout. The baseboard has a "COM1" silkscreen label next to the connector as well as a location designator of J9B2. The Serial 1 connector is located next to the P64-C low-profile PCI riser slot.

Table 4. COM1 Pin-out

Pin	Signal Name	COM1 Pin-out
1	DCD	
2	DSR	
3	RX	
4	RTS	
5	TX	
6	CTS	
7	DTR	
8	RI	
9	GND	
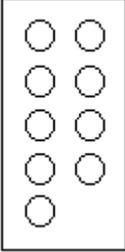
3.3.3.2   Serial 2 Port(s)

The SCB2 provides three common interfaces for accessing the Serial 2 port signals: an external low profile 8-pin RJ45 connector is located on the back edge of the baseboard, with the second and third interfaces accessed through two high-density front panel connectors on the baseboard. References to the different Serial 2 interfaces will be denoted as "Back" and "Front".

The front Serial 2 port is for direct connect or PC-to-PC server management access only with no modem support, since it lacks a Ring Indicate (RI) signal.

3.3.3.2.1   Back RJ45 Serial 2 Port

The back RJ45 Serial 2 port can support any standard serial device. An RJ45 type connector was chosen in order to support serial port concentrators which are widely used in the high-density server market and which typically use RJ45 type connectors.

To give support for either of two serial configuration standards used by serial port concentrators, the J6A2 jumper block, located directly behind the rear RJ45 serial port, must be jumpered appropriately according to which standard is desired.

Note: By default, as configured in the factory, the SCB2 baseboard will have the back RJ45 serial port configured to support a DSR signal which is compatible with the Cisco* standard.

For serial devices that require a DSR signal (default), the J6A2 jumper block must be configured as follows: the DSR jumper in position 1 and 2, and the DCD jumper in position 1 and 2. Pin 1, on the jumper, is denoted by an arrow directly next to the jumper block.

DSR to Pin#7	▢●●○
DCD to Pin#7	▢●●○
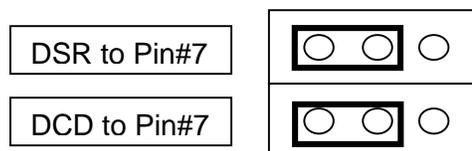
Figure 4. J6A2 Jumper Block for DSR Signal

For serial devices that require a DCD signal, the J6A2 jumper block must be configured as follows: The DCD jumper in position 2 and 3, and the DSR jumper in position 2 and 3. Pin 1, on the jumper, is denoted by an arrow directly next to the jumper block. The following diagram provides the jumper block pinout for this configuration.

DSR to Pin#7	○▢●●
DCD to Pin#7	○▢●●
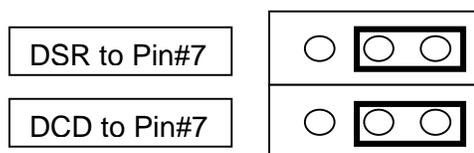
Figure 5. J6A2 Jumper Block for DCD Signal

For those serial devices that require a DB9 type of serial connector, an 8-pin RJ45-to-DB9 adapter must be used. The following table provides the pinout required for the adapter to provide RS232 support.

Table 5. Back Serial 2 Port Adapter Pinout

RJ45	Signal	Abbr.	DB9
1	Request to Send	RTS	7
2	Data Terminal Ready	DTR	4
3	Transmitted Data	TD	3
4	Signal Ground	SGND	5
5	Ring Indicator	RI	9
6	Received Data	RD	2
7	DCD or DSR	DCD/DSR	1 or 6*
8	Clear To Send	CTS	8

Notes:
1. The RJ45-to-DB9 adapter used should match both the signal requirements of the serial device and the external RJ45 serial port. The external RJ45 serial port provides all standard serial port signals, however having only 8 pins, Pin #7 can be manually configured to support either a DCD or DSR signal by setting the J6A2 jumper block appropriately.
2. For systems configured with both a front and back RJ45 serial connectors, the adapters used for the back connector cannot be used with the front connector, as the pin-out for both RJ45 ports are different.

Usage Example: When using an external modem to access the server management features of the baseboard, you must first set the J6A2 jumper to support a DCD signal and make or choose the appropriate RJ-45-to-DB9 adapter.

| DSR to Pin#7 |
| DCD to Pin#7 |
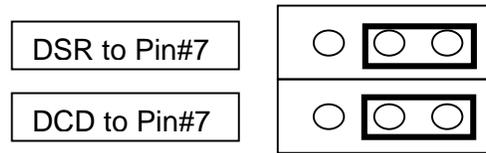
Figure 6. J6A2 Jumper Block for DCD Signal

If you choose to develop your own RJ-45-to-DB9 adapter, see *Table 5. Back Serial 2 Port Adapter Pinout* for the appropriate pinout configuration.

Notes:

- Only the back Serial 2 port has modem support

- Intel provides an orderable accessory kit for (Intel order number AXXRJ45DB9) which contains all three RJ45-to-DB9 adapters: rear DSR peripherals, rear DCD modem, and front Emergency Management Port (EMP).

3.3.3.2.2   Front RJ45 Serial 2 Port

Some server chassis may support a second RJ45 Serial 2 port on the front of the chassis, which share common signals with the back RJ45 Serial 2 port. The signals for the front Serial 2 port are accessed through either of two high-density front panel connectors on the baseboard. These connectors are found at locations J2H1, labeled FLOPPY/FP/IDE, and J1J2, labeled FRONT PANEL.

The intended usage model for a front panel mounted serial port is to provide a direct connect or PC-to-PC serial communications to access the server management features of the baseboard.

By default, the front Serial 2 port is disabled whenever there is no cable or adapter is installed. When a cable or adapter is installed, the port is enabled and the back Serial 2 port is disabled. This is accomplished by grounding pin 5 of the front 8-pin RJ45 connector.

For a direct connect or PC-to-PC serial communication, either an 8-pin RJ45-to-DB9 adapter or a cable supporting both DB-9 and RJ45 connectors will be necessary. The following table provides a pinout for the front RJ45-to-DB9 adapter or cable.

Table 6. Front RJ45 Serial 2 Port Adapter Pinout

Signal Name	RJ45	DB9
No connect	N/A	1
SIN	6	2
SOUT	3	3
DTR	2	4
GRND	4	5*
DSR	7	6
RTS	1	7
CTS	8	8
RIN	5	5*
No connect		9

Note: The use of a modem on this port cannot be supported due to the lack of an RI signal.

3.3.3.3   Floppy Drive Support

The floppy disk controller (FDC) in the SIO is functionally compatible with floppy disk controllers in the DP8473 and N844077. All FDC functions are integrated into the SIO, including analog data separator and 16-byte First-In, First-Out (FIFO). The SCB2 provides two separate interfaces for the floppy disk controller. The first is a Server Standards Infrastructure- (SSI) compliant 36-pin connector (J4G1), and the second is through the high-density 100-pin floppy / front panel /IDE connector (J2H1).

Note: Using both floppy drive controller interfaces in a common configuration is not supported.

3.3.3.4   Keyboard and Mouse Support

One external PS/2 port located on the back edge of the baseboard is provided to support a standard keyboard or mouse. A PS/2 Y-cable can be used to provide simultaneous support for both a keyboard and mouse.

3.3.3.5   Wake-up Control

The Super I/O contains functionality that allows various events to control the power-on and power-off of the system.

3.3.4   BIOS Flash

The SCB2 server board incorporates an Intel 3-Volt Advanced+ Boot Block 28F320C3 flash memory component. The 28F320C3 is a high-performance 32-megabit memory component that provides 2048K x 16 of BIOS and non-volatile storage space. The flash device is connected through the X-bus from the SIO.

3.4   Clock Generation and Distribution

All buses on the SCB2 baseboard operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 133 MHz at 2.5 V logic levels. For FCPGA2 sockets, the HE-SL, and the ITP port.
- 66 MHz at 3.3 V logic levels: For HE-SL, CIOB and the CIOB PCI clock.
- 33.3 MHz at 3.3 V logic levels: Reference clock for the PCI bus clock driver.
- 16.67 MHz at 2.5 V logic levels: Processor and the CSB5 APIC bus clocks.
- 14.318 MHz at 3.3V logic levels: CSB5, Super I/O, and video clocks.

The synchronous clock sources on the SCB2 baseboard are:

- 133-MHz host clock generator for processors, the HE-SL, Memory DIMMs, and the ITP.
- 66-MHz clock for HE-SL and the CIOB PCI clocks.
- 48-MHz clock for CSB5 USB.
- 33.3-MHz PCI reference clock.
- 16.67 MHz APIC.
- 14.318 MHz CSB5, Super I/O, and video clocks.

The SCB2 baseboard also provides asynchronous clock generators:

- 40-MHz clock for the embedded SCSI controller.
- 25-MHz clock for the embedded network interface controllers.
- 29.4989-MHz clock for the embedded video controller.
- 32-KHz clock for the CSB5 RTC.
- 40-MHz clock for the Baseboard Management Controller (BMC).

3.5   PCI I/O Subsystem

The primary I/O bus for the SCB2 server board is PCI, with three independent PCI bus segments. The PCI buses comply with the *PCI Local Bus Specification, Rev 2.2*. The P32-A bus segment is directed through the HE-SL North Bridge, while the two 64-bit segments, P64-B and P64-C, are directed through the CIOB20 I/O Bridge. The table below lists the characteristics of the three PCI bus segments.

Table 7. PCI Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Speed	Type	PCI I/O Riser Slots
P32-A	5 V	32-bits	33 MHz	Peer Bus	–
P64-B	5 V	64-bits	66/33 MHz	Peer Bus	Supports full-length cards, 3.3V bus
P64-C	5 V	64-bits	66/33 MHz	Peer Bus	Supports low-profile cards, 3.3V bus

3.5.1   P32-A: 32-bit, 33-MHz PCI Subsystem

All 32-bit, 33-MHz PCI I/O for the SCB2 server board is directed through the HE-SL North Bridge. The 32-bit, 33-MHz PCI segment created by the HE-SL is known as the P32-A segment. The P32-A segment supports the following embedded devices and connectors:

- 2D/3D Graphics Accelerator: ATI Rage XL Video Controller.
- Two 10/100 Network Interface Controllers: Intel 82550PM Fast Ethernet Controller.
- ATA-100 controller: Promise Technology PDC20267. (SCB2-ATA Only)
- CSB5 South Bridge (PCI-to-LPC bridge).

Each of the embedded devices listed above, with exception to the CSB5 South Bridge, will be allocated a GPIO to disable the device.

3.5.1.1   Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD[31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following table shows each IDSEL value for P32-A devices and the corresponding device description.

Table 8. P32-A Configuration IDs

IDSEL Value	Device
28	ATI Rage* XL Video Controller
19	Intel® 82550PM Fast Ethernet Controller
20	Intel 82550PM Fast Ethernet Controller
18	ATA-100* controller Promise Technology* PDC20267
31	CSB5 South Bridge

3.5.1.2   P32-A Arbitration

P32-A supports six PCI masters (ATA Rage XL, two Intel 82550s, Promise ATA-100 Controller, the CSB5, and the HE-SL). All PCI masters must arbitrate for PCI access, using resources supplied by the HE-SL. The host bridge PCI interface (HE-SL) arbitration lines REQx and GNTx are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

3.5.2   P64-B and P64-C: 64-bit, 66-MHz PCI Subsystem

There are two peer 64-bit, 66-MHz PCI bus segments directed through the CIOB20 I/O Bridge. The first PCI segment, P64-B, provides a single I/O riser slot capable of supporting full-length, full-height PCI cards. The PCI cards must meet the PCI specification for height, inclusive of cable connections and memory.

The second PCI segment, P64-C, provides a second I/O riser slot, capable of supporting only low-profile PCI cards.

3.5.2.1   Device IDs (IDSEL)

Each device under the PCI hub bridge has its IDSEL signal connected to one bit of AD[31:16], which acts as a chip select on the PCI bus segment in configuration cycles. This determines a unique PCI device ID value for use in configuration cycles. The following tables show IDSEL values and descriptions for devices attached to the P64-B and P64-C PCI buses.

Table 9. P64-B Configuration IDs

IDSEL Value	Device
23	On-board SCSI controller (SCSI board only).
24	First slot of the riser card.
25	Second slot of the riser card. For 3-slot riser card.
26	Third slot of the riser card. For 3- slot riser card.

Table 10. P64-C Configuration IDs

IDSEL Value	Device
24	First slot of the riser card.
25	Second slot of the riser card. For 3-slot riser card.
26	Third slot of the riser card. For 3-slot riser card.

3.5.2.2   P64-B Arbitration

P64-B supports five PCI masters: on-board SCSI controller (when present), up to 3 PCI slots (using 1-slot or 3-slot riser cards), and the CIOB. All PCI masters must arbitrate for PCI access using resources supplied by the CIOB. The host bridge PCI interface (CIOB) arbitration lines, REQx and GNTx, are a special case in that they are internal to the host bridge. The following table defines the arbitration connections.

3.5.2.3   P64-C Arbitration

P64-C supports four PCI masters: up to 3 PCI slots (using 1-slot or 3-slot riser cards), and the CIOB. All PCI masters must arbitrate for PCI access, using resources supplied by the CIOB. The host bridge PCI interface (CIOB) arbitration lines, REQx and GNTx, are a special case in that they are internal to the host bridge.

3.5.2.4   Zero Channel RAID (ZCR) Capable Riser Slot

The SCSI version of the SCB2 server board is capable of supporting either of two ZCR controllers, the Intel SRCMR RAID Adapter and the Adaptec* ASR-2000S RAID adapter.

Note: Zero Channel RAID cards are only supported in the first slot of either the 1-slot or 3-slot PCI riser cards used on the P64-B PCI segment.

The ZCR add-in cards leverage the on-board SCSI controller along with their own built-in intelligence to provide a complete RAID controller subsystem on-board. The riser card and baseboard use an implementation commonly referred to as RAID I/O Steering (RAIDIOS),

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specification version 0.92, to support this feature. If either of these supported RAID cards are installed, then the SCSI interrupts are routed to the RAID adapter instead of to the PCI interrupt controller. In addition, the IDSEL of the SCSI controller is not driven to the controller, and therefore will not be recognized as an on-board device. The host-based I/O device is effectively hidden from the system.

3.5.3   Ultra 160* SCSI

The SCSI version of the SCB2 server board provides an embedded dual-channel SCSI bus using the Adaptec* AIC-7899W SCSI controller, which is capable of supporting up to 160 MB/sec SCSI transfers. The AIC-7899W controller contains two independent SCSI controllers that share a single 64-bit, 66-MHz PCI bus master interface as a multifunction device, packaged in a 456-pin BGA.

Internally, each controller is identical and is capable of operations using either 16-bit SE or Low-Voltage Differential (LVD) SCSI providing 40 MBps (Ultra-wide SE), 80 MBps (Ultra 2), or 160 MBps (Ultra 160/m). Each controller has its own set of PCI configuration registers and SCI I/O registers.

The SCB2 server board provides active terminators, termination voltage, a resetable fuse, and a protection diode for both SCSI channels. By design, the on-board termination will always be enabled. No ability will be provided to disable termination. Each of the two SCSI channels has a connector interface. Channel A is an external high-density connector located on the back edge of the baseboard, and Channel B is a standard 68-pin internal connector. The on-board SCSI controller can be disabled through the BIOS Setup menu.

3.5.4   ATA-100

The ATA-100 version of the SCB2 server board provides an embedded dual channel ATA-100 bus using the Promise Technology* PDC20267 ASIC. The PDC20267 ATA-100 controller contains two independent ATA-100 channels that share a single 32-bit, 33-MHz PCI bus master interface as a multifunction device, packaged in a 128-pin PQFP.

The ATA-100 controller supports the following features:

- The scatter / gather mechanism supports both Direct Memory Access (DMA) and Programmable I/O (PIO) IDE drives.
- Support for ATA PIO Mode 0, 1, 2, 3, 4, DMA Mode 0, 1, 2, and Ultra DMA Mode 0, 1, 2, 3, 4, 5.
- The IDE drive transfer rate is capable of up to 100 MB/sec per channel.
- The host interface complies with *PCI Local Bus Specification Revision 2.2*.
- 32-bit, 33-MHz bus speed and 132 MB/sec sustained transfer rate.

The Promise PDC20267 supports IDE RAID through dual ATA-100 Channels. In a RAID configuration, mutiple IDE hard drives are placed into one or more arrays of disks. Each array is seen as an independent disk, though the array may include upwards of two, three, or four drives. The IDE RAID can be configured as followings:

- RAID 0:   Stripping one to four drives.
- RAID 1:   Mirroring two drives.

- RAID 1 +:   Spare drive (three drives).
- RAID 0 +:   One to four drives are required.

RAID 0 configurations are used for high-performance applications, as it doubles the sustained transfer rate of its drives. RAID 1 configurations are primarily used for data protection. It creates an identical drive backup to a secondary drive. Whenever a disk write is performed, the controller sends data simultaneously to a second drive located on a different data channel. With four drives attached to dual ATA-100 channels, two striped drive pairs can mirror each other (RAID 0+1) for storage capacity and data redundancy.

3.5.5   Video Controller

The SCB2 server board provides an ATI Rage XL PCI graphics accelerator, along with 8 MB of video SDRAM and support circuitry for an embedded SVGA video subsystem. The ATI Rage XL chip contains a SVGA video controller, clock generator, 2D and 3D engine, and RAMDAC in a 272-pin PBGA. One 2Mx32 SDRAM chip provides 8 MB of video memory.

The SVGA subsystem supports a variety of modes, up to 1600 x 1200 resolution in 8/16/24/32 bpp modes under 2D, and up to 1024 x 768 resolution in 8/16/24/32 bpp modes under 3D. It also supports both CRT and LCD monitors up to 100 Hz vertical refresh rate.

The SCB2 server board provides a standard 15-pin VGA connector and supports disabling of the on-board video through the BIOS Setup menu or when a plug-in video card is installed in any of the PCI slots.

3.5.5.1   Video Modes

The Rage XL chip supports all standard IBM VGA modes. The following table shows the 2D/3D modes supported for both CRT and LCD. The table specifies the minimum memory requirement for various display resolution, refresh rates, and color depths.

Table 11. Video Modes

2D Mode	Refresh Rate (Hz)	SCB2 2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
640x480	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
800x600	60, 70, 75, 90, 100	Supported	Supported	Supported	Supported
1024x768	60, 72, 75, 90, 100	Supported	Supported	Supported	Supported
1280x1024	43, 60	Supported	Supported	Supported	Supported
1280x1024	70, 72	Supported	–	Supported	Supported
1600x1200	60, 66	Supported	Supported	Supported	Supported
1600x1200	76, 85	Supported	Supported	Supported	–
3D Mode	Refresh Rate (Hz)	SCB2 3D Video Mode Support with Z Buffer Enabled			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	–	–

2D Mode	Refresh Rate (Hz)	SCB2 2D Video Mode Support			
		8 bpp	16 bpp	24 bpp	32 bpp
1600x1200	60,66,76,85	Supported	–	–	–
3D Mode	Refresh Rate (Hz)	SCB2 3D Video Mode Support with Z Buffer Disabled			
640x480	60,72,75,90,100	Supported	Supported	Supported	Supported
800x600	60,70,75,90,100	Supported	Supported	Supported	Supported
1024x768	60,72,75,90,100	Supported	Supported	Supported	Supported
1280x1024	43,60,70,72	Supported	Supported	Supported	–
1600x1200	60,66,76,85	Supported	Supported	–	–

3.5.5.2   Video Memory Interface

The memory controller subsystem of the Rage XL arbitrates requests from a direct memory interface, the VGA graphics controller, the drawing coprocessor, the display controller, the video scalar, and hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/coprocessor drawing performance.

The SCB2 supports an 8 MB (512Kx32bitx4 Banks) SDRAM device for video memory.

3.5.6   Network Interface Controller (NIC)

The SCB2 server board supports two 10Base-T/100Base-TX Network Interface Controllers (NICs) based on the Intel 82550PM NIC. The 82550PM is a highly integrated PCI LAN controller in a thin BGA 15mm package. The controller's baseline functionality is equivalent to that of the Intel 82559, with the addition of Alert-on-LAN functionality. The SCB2 server board supports independent disabling of the two NIC controllers using the BIOS Setup menu.

The 82550PM supports the following features:

- Glueless 32-bit PCI, CardBus master interface (Direct Drive of Bus), compatible with *PCI local Bus Specification, Revision 2.2.*
- Integrated IEEE 802.3 10Base-T and 100Base-TX compatible PHY.
- IEEE 820.3u auto-negotiation support.
- Full duplex support at both 10 Mbps and 100 Mbps operation.
- Integrated UNDI ROM support.
- MDI/MDI-X and HWI support.
- Low power +3.3 V device.

3.5.6.1   NIC Connector and Status LEDs

The 82550 drives two LEDs located on each network interface connector. The amber LED indicates network connection when on, and transmit/receive activity when blinking. The Geen LED indicates 100-Mbps operation when lit, and 10-Mbps when off.

3.6 Interrupt Routing

The SCB2 interrupt architecture accommodates both PC-compatible PIC mode and APIC mode interrupts through use of the integrated I/O APICs in the CSB5.

3.6.1   Legacy Interrupt Routing

For PC-compatible mode, the CSB5 provides two 82C59-compatible interrupt controllers. The two controllers are cascaded with interrupt levels 8-15 entering on Level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The CSB5 contains configuration registers that define which interrupt source logically maps to I/O APIC INTx pins.

Interrupts, both PCI and IRQ types, are handled by the CSB5. The CSB5 then translates these to the APIC bus. The numbers in the table below indicate the OSB4 PCI interrupt input pin to which the associated device interrupt (INTA, INTB, INTC, INTD) is connected. The CSB5's I/O APIC exists on the I/O APIC bus with the processors.

Table 12. PCI Interrupt Routing/Sharing

Interrupt	INT A	INT B	INT C	INT D
ATI Rage* SL	2			
Promise ATA-100 Controller*	3			
Intel® 82550PM #2	4			
82550PM #1	5			
P64-C Riser Slot 3	7	6	9	8
P64-C Riser Slot 2	8	7	6	9
P64-C Riser Slot 1	9	8	7	6
P64-B Riser Slot 3	13	12	15	14
P64-B Riser Slot 2	14	13	12	15
P64-B Riser Slot 1	15	14	12	11
7899-SCSI Ch.A	11			
7899-SCSI Ch.B		10		

3.6.2   APIC Interrupt Routing

For APIC mode, the SCB2 interrupt architecture incorporates three Intel I/O APIC devices to manage and broadcast interrupts to local APICs in each processor. The I/O APICs monitor each interrupt on each PCI device, including PCI slots, in addition to the ISA compatibility interrupts IRQ(0-15). When an interrupt occurs, a message corresponding to the interrupt is sent across a three-wire serial interface to the local APICs. The APIC bus minimizes interrupt latency time for compatibility interrupt sources. The I/O APICs can also supply greater than 16 interrupt levels to the processor(s). This APIC bus consists of an APIC clock and two bidirectional data lines.

3.6.2.1   Legacy Interrupt Sources

The table below recommends the logical interrupt mapping of interrupt sources on the SCB2 server board. The actual interrupt map is defined using configuration registers in the CSB5.

Table 13. Interrupt Definitions

ISA Interrupt	Description
INTR	Processor interrupt.
NMI	NMI to processor.
IRQ1	Keyboard interrupt.
IRQ3	Serial port 1 or 2 interrupt from SIO device, user-configurable.
IRQ4	Serial port 1 or 2 interrupt from SIO device, user-configurable.
IRQ5	
IRQ6	Floppy disk.
IRQ7	
IRQ8_L	Active low RTC interrupt.
IRQ9	
IRQ10	
IRQ11	
IRQ12	Mouse interrupt.
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1.
IRQ15	
SMI*	System Management Interrupt. General purpose indicator sourced by the CSB5 and BMC to the processors.
SCI*	

3.6.3   Serialized IRQ Support

The SCB2 server board supports a serialized interrupt delivery mechanism. Serialized Interrupt Requests (SERIRQs) consists of a start frame, a minimum of 17 IRQ / data channels, and a stop frame. Any slave device in the quiet mode may initiate the start frame. While in the continuous mode, the start frame is initiated by the host controller.

3.6.4   IRQ Scan for PCIIRQ

The IRQ / data frame structure includes the ability to handle up to 32 sampling channels with the standard implementation, using the minimum 17 sampling channels. The SCB2 server board has an external PCI interrupt serializer for a PCIIRQ scan mechanism of CSB5 to support 16 PCIIRQs.

Super I/O

Serialized IRQ Interface
Timer →
Keyboard →
Cascade →
Serial Port2/ISA →
Serial Port1/ISA →
ISA →
Floppy/ISA →
ISA →
RTC →
SCI/ISA →
ISA →
ISA →
Mouse/ISA →
Coprocessor Error →
P_IDE/ISA →
Not Used →

SERIRQ

CSB5 Interrupt Routing

PCI Clock
33 MHz

PCI IRQ Serializer

PCI32 INTA →	PCIIRQ0
PCI32 INTB →	PCIIRQ1
VGA →	PCIIRQ2
ATA-100 →	PCIIRQ3
NIC2 →	PCIIRQ4
NIC1 →	PCIIRQ5
LP PCI INTD →	PCIIRQ6
LP PCI INTC →	PCIIRQ7
LP PCI INTB →	PCIIRQ8
LP PCI INTA →	PCIIRQ9
SCSI PORT B →	PCIIRQ10
SCSI PORT A →	PCIIRQ11
F/L PCI INTD →	PCIIRQ12
F/L PCI INTC →	PCIIRQ13
F/L PCI INTB →	PCIIRQ14
F/L PCI INTA →	PCIIRQ15

PIRQ1

PIRQ_LATCH

Figure 7. SCB2 Interrupt Routing Diagram

SLOT #3   SLOT #2   SLOT #1

INT A   PCIIRQ9

INT B   PCIIRQ8

INT C   PCIIRQ7

INT D   PCIIRQ6
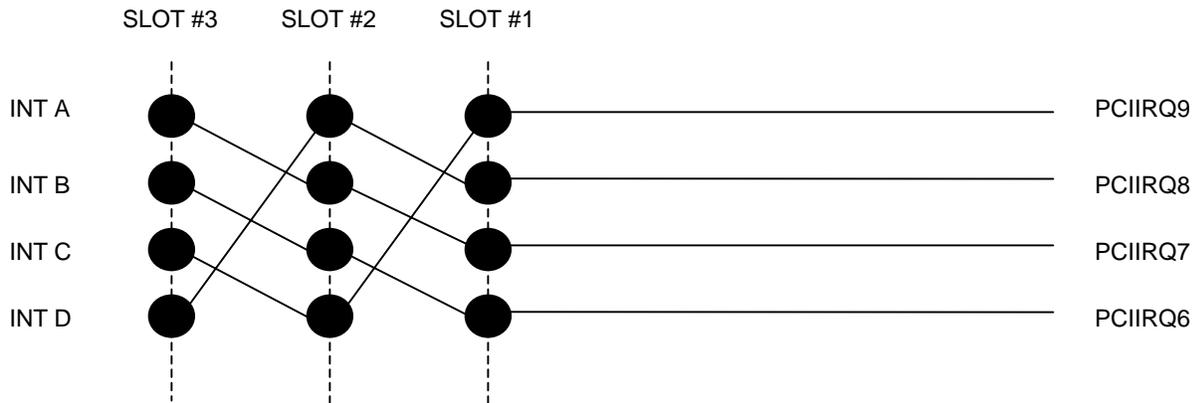
Figure 8. SCB2 PCI64-C Interrupt Mapping Diagram

SLOT #3   SLOT #2   SLOT #1

INT A   PCIIRQ15

INT B   FET Switches   PCIIRQ14

INT C   PCIIRQ13

INT D   PCIIRQ12

Pin# B4

Pin# B2

ZCR Present

PORT A   PCIIRQ11

SCSI Controller

PORT B   PCIIRQ10
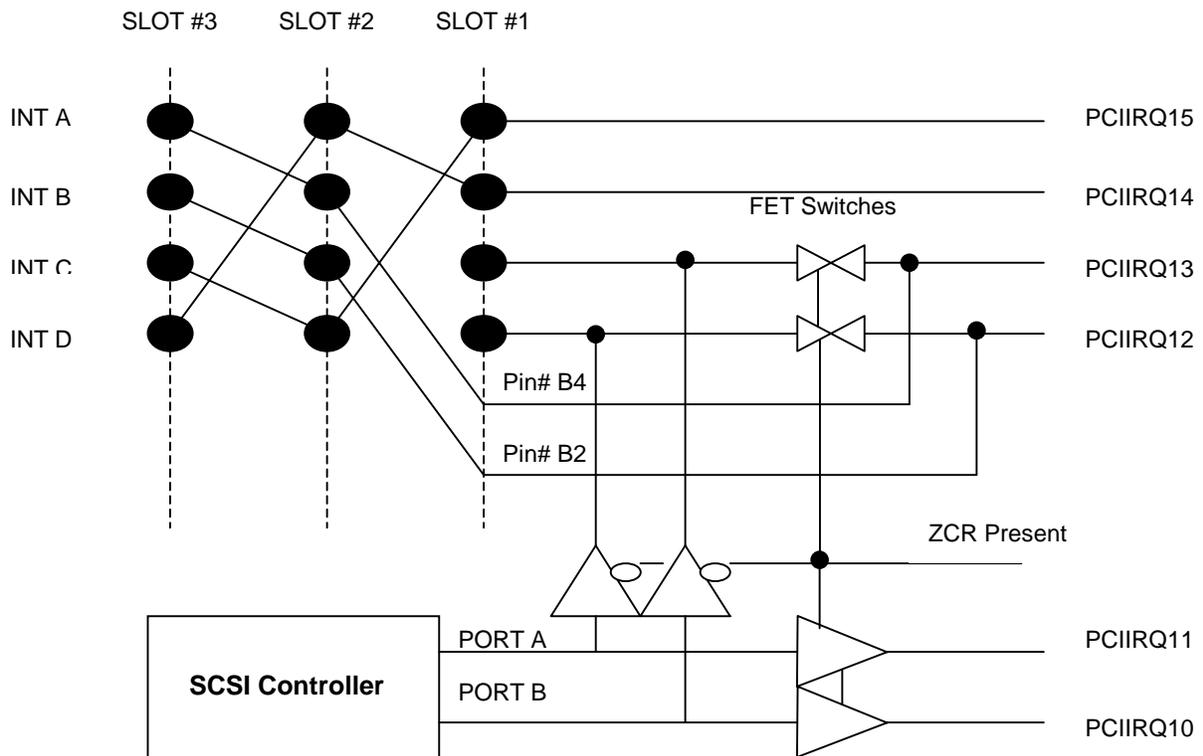
Figure 9. SCB2 PCI64-B Interrupt Mapping Diagram

3.7   System Reset Control

Reset circuitry on the SCB2 server board looks at resets from the front panel, CSB5, ITP, and the processor subsystem to determine proper reset sequencing for all types of resets. The reset logic is designed to accommodate several methods to reset the system, which can be divided into the following categories:

- Power-up reset
- Hard reset
- Soft (programmed) reset

The following subsections describe each type of reset.

3.7.1   Power-up Reset

When the system is disconnected from AC power, all logic on the server board is powered off. When a valid input (AC) voltage level is provided to the power supply, 5 volt standby power will be applied to the server board. The baseboard has a 5 volt to 3.3 volt regulator to produce 3.3 volt standby voltage. A power monitor circuit on 3.3 volt standby will assert BMCRST_L, causing the BMC to reset. The BMC is powered by 3.3 volt standby, and monitors and controls key events in the system related to reset and power control.

After the system is turned on, the power supply will assert the RST_PWRGD_PS signal after all voltage levels in the system have reached valid levels. The BMC receives RST_PWRGD_PS and, after 500 ms, asserts RST_P6_PWR_GOOD, which indicates to the processors and CSB5 that the power is stable. Upon RST_P6_PWR_GOOD assertion, the CSB5 will toggle PCI reset.

3.7.2   Hard Reset

A hard reset can be initiated by resetting the system through the front panel switch. During the reset, the Sahalee BMC de-asserts RST_P6_PWR_GOOD. After 500 ms, it is reasserted, and the power-up reset sequence is completed.

The Sahalee BMC is not reset by a hard reset. It is only reset when AC power is applied to the system.

3.7.3   Soft Reset

A soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers. Soft resets can be generated by the keyboard controller located in the SIO, by the CSB5, or by the operating system.

4.   Platform Management Architecture

The following list defines the major elements of the platform management architecture for the SCB2 server board.

IPMI v1.5 specification-based management, including:

- IPMI messaging, commands, and abstractions
- Baseboard Management Controller (BMC)
- Sensors
- Sensor data records (SDRs) and sensor data record repository
- Field replaceable unit (FRU) information
- Autonomous event logging
- System Event Log (SEL): At least 8 KB, holding over 400 events
- BMC watchdog timer, covering BIOS and run-time software
- IPMI channels and sessions
- Emergency management port (EMP): IPMI messaging over serial / modem. This feature is also referred to as DPC (Direct Platform Control) over serial/modem.
- Serial / modem paging
- Serial / modem alerting over PPP using the platform event trap (PET) format
- Direct Platform Control: IPMI messaging over LAN (available via both on-board network controllers)
- LAN alerting using PET
- Platform event filtering (PEF)
- ICMB (Intelligent Chassis Management Bus): IPMI messaging between chassis
- PCI Management Bus support

Additional management features, including:

- Fault resilient booting
- Magic Packet* and Wake-on-LAN* (WOL) / Power-on-LAN support
- Wake-on-Ring* (WOR) support

These elements, and the functionality and features that they provide, are described in the following sections.

The following figure shows a logical block diagram of the platform management architecture implemented on the SCB2 server board.
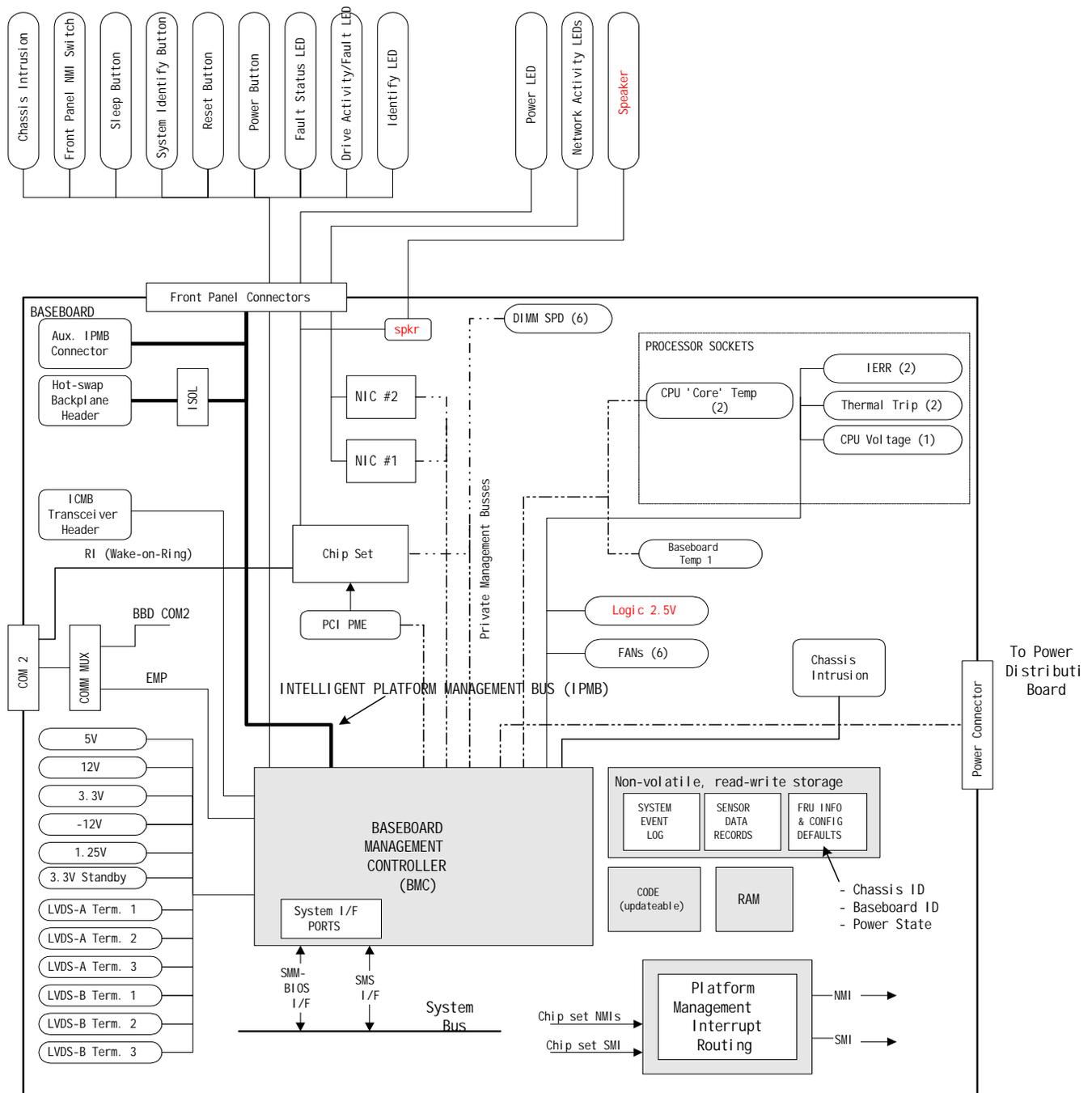
Figure 10. SCB2 Baseboard Management Block Diagram

4.1   IPMI Messaging, Commands, and Abstractions

The IPMI 1.5 specification defines a standardized, abstracted, message-based interface between software and the platform management subsystem, and a common set of messages (commands) for performing operations such as accessing temperature, voltage, and fan sensors, setting thresholds, logging events, and controlling a watchdog timer.

IPMI also includes a set of records called sensor data records (SDRs) that make the platform management subsystem self-descriptive to system management software. The SDRs include software information such as how many sensors are present, what type they are, and what events they generate. The SDRs also include information, such as minimum and maximum ranges, sensor type, and accuracy and tolerance, that guides software in interpreting and presenting sensor data.

Together, IPMI messaging and the sensor data records provide a self-descriptive, abstracted platform interface that allows management software to automatically configure itself to the number and types of platform management features on the system. In turn, this enables one piece of management software to be used on multiple systems. Since the same IPMI messages are used over the serial/modem and LAN interfaces, a software stack designed for in-band (local) management access can readily be re-used as an out-of-band remote management stack by changing the underlying communications layer for IPMI messaging.

4.2   Sahalee Baseboard Management Controller(BMC)

The Sahalee BMC is an Application-Specific Integrated Circuit (ASIC) packaged in a 156-pin BGA that contains a 32-bit Reduced Instruction Set Computing (RISC) microcontroller and associated peripherals that provides the intelligence at the heart of the intelligent platform management architecture.

The primary purpose of the BMC is to autonomously monitor system sensors for system platform management events, such as over temperature, out-of-range voltages, and fan failures, and log their occurrence in the non-volatile SEL. The BMC also provides the interface to the sensors and the SEL, so system management software can poll and retrieve the present status of the platform.

The log contents can be retrieved post mortem in order to provide failure analysis information to field service personnel. It is also accessible by system management software, such as Intel Server Control (ISC), running under the OS.

The SCB2 BMC includes the ability to generate a selectable action, such as a system power-off or reset, when a match occurs to one of a configurable set of events. This capability is called platform event filtering (PEF). One of the PEF actions is to trigger the BMC to dial and generate an alert. This can be a telephone page using an external modem, or a LAN alert, or even LAN and modem alerts to multiple destinations. More information on platform event filtering and alerting is provided in later sections.

The BMC includes recovery control functions that allow local or remote software to request actions, such as power on/off, power cycle, and system hard resets, plus an IPMI watchdog timer, that can be used by BIOS or run-time management software as a way to detect software hangs.

The BMC also provides out-of-band remote management interfaces providing access to the platform health, event log, and recovery control features via serial/modem, LAN, IPMB, PCI Management Bus, and ICMB interfaces. These interfaces remain active on standby power, providing a mechanism where the system event log, sensor data record, and recovery control features can be accessed even when the system is powered down.

Because the BMC operates independently from the main processors, the BMC monitoring and logging functions, and the out-of-band interfaces can remain operative even under failure conditions that cause the main processors, OS, or local system software to stop.

The BMC also provides the interface to the non-volatile SDR repository. IPMI sensor data records provide a set of information that system management software can use to automatically configure itself for the number and type of IPMI sensors (e.g. temperature sensors, voltage sensors, etc.) in the system. This information allows management software to automatically adapt itself to the particular system, enabling the development of management software that can work on multiple platforms without requiring the software to be modified.

The SCB2 uses the Sahalee microcontroller as its baseboard management controller. Sahalee is a custom ARM7-TDMI based microcontroller designed for baseboard management applications on Intel server boards. The following is a list of the major functions that are managed by the BMC. Sensors and sensor polling include:

- Baseboard temperature
- Processor temperature
- Processor presence (with power lockout if processors are not populated correctly)
- Processor IERR
- Fan speed
- Baseboard voltages
- Processor voltages
- SCSI termination voltage
- Chassis intrusion

- Field Replaceable Unit (FRU) Information Access. Field replaceable unit information is non-volatile storage for serial number, part number, asset tag, and other inventory information for the baseboard and chassis. The FRU implementation on the SCB2 includes write support for OEM-specific records.

- Autonomous event logging. The baseboard management controller autonomously polls baseboard sensors and generates IPMI platform events, also called event messages, when an event condition is detected. The events are automatically logged to the SEL.

- System event log (SEL). Non-volatile storage for platform health events. Events can be autonomously logged by the BMC, or by sending event messages to the BMC via the system interface or Intelligent Platform Management Bus (IPMB). This enables BIOS, software, and add-in cards to also log events.

- Sensor data record (SDR) repository. Non-volatile storage holding records describing the number and type of management sensors on the baseboard and in the chassis. Includes write support for OEM-specific records and sensors.

- SDR/SEL Timestamp Clock. A clock internally maintained by the BMC that is used for time-stamping events and recording when sensor data record and system event log contents have changed.

- Intelligent Platform Management Bus (IPMB). The IPMB is a two-wire, multi-master serial bus that provides a point for extending the baseboard management to include chassis management features, and for enabling add-in cards to access the baseboard management subsystem.

- Watchdog timer with selectable timeout actions (power off, power cycle, reset, or NMI) and automatic logging of timeout event.

- LAN remote management connection.

- LAN alerting via Platform Event Trap (PET) format SNMP trap.

- Serial/Modem Remote Management Connection.

- Serial/Modem Event Paging/Alerting.

- Platform event filtering (PEF).

- Keyboard Controller Style (KCS) IPMI-System Interface.

- Intelligent Chassis Management Bus (ICMB) support

  - Remote Boot Control
  - Local and Remote Power On/Off/Reset Control
  - Local and Remote Diagnostic Interrupt (NMI) Control

- Fault-Resilient Booting.

- Front Panel LED Control.

- Platform Management Interrupt Routing.

- Power Distribution Board (PDB) monitoring.

- Updateable BMC firmware.

- System management power control (including providing sleep/wake and power push-button interfaces).

- Platform event filtering (PEF).

- Baseboard fan speed control and failure monitoring. The baseboard supports monitoring either via individual connectors for six (6) tach fans, or via a fan pack connector that supports up to five (5) fans.

- Speaker beep capability (used to indicate conditions such as power lockout if processors are not populated correctly).

- Processor bus speed setting.

- Baseboard FRU information interface.

- FRU replacement LEDs for processors, DIMMs, and FANs.

- Diagnostic interrupt (front panel NMI) handling.

- SMI/NMI status monitor.

- System interface to the IPMB (via system interface ports).

- System interface to the PCI management bus (via system interface ports).

- Secure mode control, including video blank and floppy write-protect option monitoring and control, and front panel lock/unlock initiation.

- IPMI v1.5 management controller initialization agent function.

- EMP serial/modem platform management interface.

- DPC LAN platform management interface, supported via both on-board network controllers.

- Serial/modem and LAN alerting.

4.2.1   Watchdog Timer

The BMC implements a watchdog timer that is used for a number of system time-out functions. The timer can be used by system management software (SMS), or by the BIOS. This timer is used for several purposes. During POST, it functions as the reset timer for FRB-2 implementation.

The watchdog timer can also be used during the OS-boot interval as an OS load watchdog timer. In this mode, the timer is started by BIOS before POST is concluded. System management software, or the OS, must stop the timer, or a system reset or other selection watchdog time-out action will occur (see below).

Note: OS load watchdog operation is not supported in the standard SCB2 BIOS.

During run-time, system management software uses it as an OS watchdog timer. An OEM watchdog configuration is also supported.

When used as an OS watchdog timer, SMS starts the timer and then periodically resets it to keep it from expiring. This periodic action serves as a heartbeat that indicates that the OS (or at least the SMS task) is still functioning. If SMS hangs, the timer will expire and the BMC will log a watchdog time-out event message and generate a system reset or other watchdog timer action (see below).

The BMC retains status information that the BIOS can read after the system comes out of reset. This information indicates whether the reset was caused by a watchdog timer time-out, and if so, whether it was being used for FRB-2, OEM, OS load watchdog, or OS watchdog operation at the time. This allows the BIOS to display an appropriate notification message, or take other actions.

The watchdog timer is implemented as a 16-bit timer with 100 ms per count. Further specifications for the timer can be found in the *SCB2 Baseboard Management Controller EPS* and the *Intelligent Platform Management Interface v1.5 Specification.*

4.2.1.1   Watchdog Time-out Actions

The following actions are available on expiration of the watchdog timer:

- System reset on time-out.

- System power down on time-out.

- System power cycle on time-out. The BMC also provides a command that allows the off interval, for the power cycle, to be configured. The interval can be set to be from 1 to 255 seconds. This setting is saved in the BMC's non-volatile storage.

- Interrupt on time-out. The BMC can be configured to generate an NMI, SCI, or SMI interrupt at a configurable interval prior to the time-out. If one of the above actions is selected (Reset, Power Down, or Power Cycle) the action will occur when the timer expires. If the pre-timeout interval is set to 0, the selected action and interrupt will occur simultaneously. The default pre-timeout interrupt interval is one (1) second.

The Reset, Power Down, and Power Cycle action selections are mutually exclusive. The interrupt may be selected in combination with any one of the Reset, Power Down, or Power Cycle actions. By default, the BMC will automatically log a corresponding event for any of these time-outs.

4.3 Sensors

The following sections list the baseboard sensors that are provided on the SCB2.

Note: Many of the fan, temperature and voltage sensors listed in the following sections are only found when the SCB2 is integrated into an Intel SR1200 or SR2200 server chassis. These sensors may or may not be present when the SCB2 is integrated into a third-party reference chassis. After assembly, the SCB2-based server must be configured to read the appropriate sensors for proper server management monitoring to occur.

4.3.1   Temperature Sensors

The BMC implements 8-bit, threshold-based analog sensors, with high/low critical and non-critical thresholds as specified for the following system temperatures.

Processor temperature sensors only implement upper-critical and upper non-critical thresholds when temperature threshold auto-configuration is used.

Temperature Sensor	Description	Resolution	Accuracy
Baseboard1	Baseboard Temperature sensor 1. Located in airflow for chip set or hot-spot selected according to thermal design.	8-bit	+/- 3% or better
Front Panel Ambient	Located on front panel board of the Intel® SR1200 and SR2200 server chassis.	8-bit	+/- 3% or better

Processor 1	Processor #1 thermal sensor	8-bit	+/- 3% or better
Processor 2	Processor #2 thermal sensor	8-bit	+/- 3% or better

4.3.2   Voltage Sensors

The BMC implements 8-bit, threshold-based analog sensors, with high/low critical and non-critical thresholds for the following system voltages:

Sensor	Description	Resolution	Accuracy
+5V	Baseboard +5V	8-bit	+/- 3% or better
+12V	Baseboard +12V	8-bit	+/- 3% or better
+3.3V	Baseboard +3.3V	8-bit	+/- 3% or better
-12V	Baseboard -12V	8-bit	+/- 3% or better
Processor VRM	Processor VRM voltage monitor	8-bit	+/- 3% or better
2.5V	Logic 2.5V	8-bit	+/- 3% or better
GTL (1.25V)	Processor bus logic voltage	8-bit	+/- 3% or better
1.2V	Chip set logic 1.2V	8-bit	+/- 3% or better
+3.3V Standby	Standby voltage to PCI slots and other subsystems	8-bit	+/- 3% or better
5V Standby	Source of standby voltage for BMC and other subsystems and 3.3V Standby	8-bit	+/- 3% or better

4.3.3   Processor Voltage Threshold Auto-configuration

For processor types that solely use the on-board Voltage Regulator Modules (VRMs), the BMC reads the VID (Voltage ID) bits and automatically configures the thresholds for processor voltage monitoring according to the normal range values from the VID bits. These values will be adjusted by the BMC according to the accuracy and tolerance of the voltage sensing circuitry.

4.3.4   Processor Voltage Mismatch

The SCB2 processors share a single Voltage Regulator Module (VRM). The BMC will issue a beep code and prevent the system from powering up if it detects a difference between the processor VIDs.

4.3.5   SCSI Terminator Voltage Sensors

The SCB2 BMC is able to monitor for failure of the SCSI terminators on the baseboard. Failure, in this case, is defined as the termination voltage source being out-of-range with respect to the terminator device specification. Each SCSI terminator has two operating voltage ranges, one for single-ended operation, and one for Low Voltage Differential SCSI (LVDS). The BMC produces a digital failure status and corresponding event when it detects that the termination voltage has transitioned to a value that is outside of both of those ranges.

Each on-board SCSI channel supports three SCSI terminators. The BMC provides the following SCSI termination voltage monitoring sensors.

Sensor	Description	Resolution	Accuracy
LVDS-A T1	LVD / Single-ended SCSI channel 1, Terminator 1	digital	+/- 3% or better on reading used for comparison result.
LVDS-A T2	LVD / Single-ended SCSI channel 1, Terminator 2	digital	+/- 3% or better on reading used for comparison result.
LVDS-B T1	LVD / Single-ended SCSI channel 2, Terminator 1	digital	+/- 3% or better on reading used for comparison result.
LVDS-B T2	LVD / Single-ended SCSI channel 2, Terminator 2	digital	+/- 3% or better on reading used for comparison result.

4.3.6   Fan Sensors and Fan Speed Control

The SCB2 provides support for up to six system fans connected to the baseboard. Each fan connection accepts either a tach fan or a digital fan. The tach or digital signals from the fan connectors, for each fan, are individually monitored by the BMC.

The baseboard supports fan monitoring either via individual connectors for six system fans, or via a fan pack connector that supports up to five (5) fans. These options are mutually exclusive. Sensor data records are used to determine which fan connectors are used.

For tach fans, the BMC implements a threshold-based RPM sensor with an 8-bit reading that is proportional to the fan's RPM. The BMC generates an event if the RPM drops below a critical threshold associated with the sensor. Digital fans are implemented as a digital failure sensor. The BMC shall generate an event when the fan signal indicates that the fan has detected its performance is lagging.

The number of active fan sensors is configured using the sensor data records. The various fan sensors are initially disabled and are enabled when the initialization agent function, in the BMC, is executed on system power ups and hard resets.

4.3.6.1   Temperature-based Fan Speed Control Sensor

When the SCB2 server board is integrated into an Intel® SR1200 or Intel® SR2200 chassis, the BMC implements an ambient temperature-based fan speed control that is part of *normal system operation.* The feature allows the SCB2 baseboard to drive different fan speeds, based on ambient temperature, in order to lower the acoustic noise of the SCB2/SR1200 or SCB2/SR2200 system.

The ambient temperature thresholds, at which the fan speed increases, does not correspond to a non-critical (warning) condition for the fan, since the fan's state is still OK from the system point-of-view.

The SCB2 baseboard has a fan speed signal that is driven from a pulse-width modulator (PWM) circuit controlled by the BMC. This signal can be driven to several levels according to the ambient temperature measurement. An Intel server-defined OEM SDR is used to hold parameters that set the temperature thresholds and corresponding PWM duty cycles. This SDR

is loaded as part of the FRUSDR utility configuration. Information on the SDR can be found in the *SCB2 Baseboard Management Controller EPS*.

The BMC firmware gets the ambient temperature reading from the front panel temperature sensor in the SR1200 and SR2200 server chassis. Other third-party chassis may or may not have this support.

4.3.6.2   Fan Speed-up on Fan Failure

The BMC will simultaneously speed up all fans, under its control, to high speed when any of its fan sensors enter a lower-critical, going-low threshold crossing state.

The BMC accepts a *Set Fault Indication* command that allows other management controllers in the system to communicate their temperature monitoring status. The BMC will speed up the fans if any other controllers use this command to indicate that they have had a critical fan fault.

The *fan speed up on fan failure* and *fan speed up on over-temperature* features may be viewed as being OR'd together. The fan speed up will occur if either or both determine conditions that meet their fan speed-up criteria.

Fan speed will return to low speed when all fan sensor event status has returned to a non-critical or OK, and after all other controllers, that had reported a fan critical condition, report a non-critical or OK status, provided no *fan speed up on over-temperature conditions* are in effect.

The *fan speed up on fan failure* state is not held across AC power cycles. The controllers must re-assess a critical fan fault state before the speed up will re-occur. The SDRs tell the BMC how many fans are supposed to be present in the system, and which connectors they should be attached to. This is necessary for the firmware to be able to discriminate between intentionally unpopulated fan connector positions and accidentally unpopulated or disconnected fan connector positions.

If the SDRs indicate that a fan should be installed on a particular connector, the platform management subsystem considers a disconnected fan as a failed fan.

4.3.6.3   Fan Kick Start

Some fans may not begin rotating unless started at high speed. To ensure that the fans start, the BMC will start and run the fans at high speed for a brief interval following system power up.

4.3.7   Missing Processor/Terminator Module Detection

The BMC checks to see if all sockets are populated by modules (regardless of whether they are populated with processor or termination modules). The BMC will generate a series of beep codes when the user attempts to power up the system and one or both sockets are empty.

4.3.8   Other Sensors

The following additional sensors shall be monitored by the BMC unless otherwise specified.

Sensor	Description / Requirements
Processor 1 Sensor. Monitors:	
Processor 1 Presence	Processor is present in processor module socket.
Processor 1 IERR [1]	Digital monitor of the state of the IERR signal from the processor socket.
Processor 1 Thermal Trip [1]	Digital monitor of the state of the Thermal Trip signal from the processor socket.
Processor 2 Sensor. Monitors:	
Processor 2 Presence [1]	Processor is present in processor module socket.
Processor 2 IERR [1]	Digital monitor of the state of the IERR signal from the processor socket.
Processor 2 Thermal Trip [1]	Digital monitor of the state of the Thermal Trip signal from the processor socket.
DIMM Presence (6)	Digital sensors return which on-board DIMM slots are populated.
Chassis Intrusion	Chassis Intrusion signal from the Front Panel Connector. This signal shall indicate insecure if the line on the connector is left floating. Signal polarity shall match that used for the SR1200 chassis.

Note:

1. These are combined into a single Processor Status sensor for each processor.

4.3.9   Other Monitored Signal Status

The following additional signal status can be obtained via commands to the BMC.

Signal	Description
Power Button	This signal shall be monitored by the BMC.
Reset Button	This signal shall be monitored by the BMC.
Diagnostic Interrupt (Front Panel NMI)	This signal goes to the BMC to allow Diagnostic Interrupt events to be logged. A present reading status is not provided. The BMC drives a separate output signal that goes into the baseboard NMI circuitry.
Keyboard Secure Mode [1]	Also known as Secure_Mode_KB. This signal from the keyboard controller directs the BMC to activate its Secure Mode options. See Section 4.15, Secure Mode Control, for more information. The present state of this signal can be read via a command to the BMC.
SMI signal state	This is the digital state of the bussed SMI signal to the processors. The BMC provides a command that allows a Remote Management Card to retrieve this signal state via the IPMB.
NMI signal state	This is the digital state of the bussed NMI signal to the processors. The BMC provides a command that allows a Remote Management Card to retrieve this signal state via the IPMB.
System Firmware Progress (POST Error)	This sensor holds the last System Firmware Progress code received from BIOS.
Power On Hours	The BMC supports the IPMI *Get POH Counter* command. This command allows software to determine the number of hours that a system has powered up. This information can be used for preventive maintenance scheduling purposes.

Note:

1. These are combined into a single processor status sensor for each processor.

4.3.10   Additional Events

In addition to the voltage, temperature, chassis intrusion, and other platform management events, the following events are included in SCB2/SR1200/SR2200. Some of the events generate beep codes, some cause events to be logged, and some do both. The Sensor Type, Event/Reading Type, and Event Offset codes are from the *Intelligent Platform Management Interface v1.5 Specification*.

Table 14. Additional Events for SCB2

New Events	Beep Code?	Sensor Type	Event / Reading Type	Event Offset(s)	OEM Data 1
Processor Operating Voltage Mismatch	Yes	none	none	no event	–
Missing Processor Terminator Module	Yes	07h processor	08h digital inserted / removed	no event	–
Power Lost (controller logs event when AC returns)	No	09h power unit	E6h sensor specific deassertion	04h A/C restored	–

4.3.11   POST Error Logging

During POST, if certain errors occur BIOS will log them to the SEL by sending an IPMI event message to the BMC.

4.3.12   POST Progress FIFO

The SCB2 BIOS uses a special command to the BMC to write numeric checkpoint information that indicates the entry of various phases of the system startup and boot process. These checkpoint values are referred to as *progress codes.* The progress code values can be useful in diagnosing system problems if they occur during system startup.

The BMC maintains a RAM FIFO of the last 16 post progress codes that it has received. Accompanying this FIFO is a timestamp that indicates when the last code was received.

By default, the BMC rejects duplicate codes that are received; however, the command interface allows BIOS to explicitly indicate that the code should be stored, regardless of whether the previous code was a duplicate.

A corresponding command allows system software to be able to retrieve the contents of the FIFO. This command can be executed via the internal and external interfaces to the BMC. The POST progress FIFO is volatile. It is cleared whenever the system loses AC power, is powered-down (ACPI S4 or S5), or is reset.

4.3.13   Control Capabilities

The BMC has the following system control capabilities:

BMC_FP_NMI	The BMC is able to drive a Diagnostic Interrupt (front panel NMI) signal into the baseboard interrupt routing logic. This signal can be driven by the BMC in response to the assertion of the Diagnostic Interrupt signal from the front panel connector. Or it can be driven in response to a *Pulse Front Panel NMI* command to the BMC.
System Power On/Off	The BMC can initiate a system power on or power down via the *PS-ON* signal to the power subsystem.
System Power Cycle	The BMC is able to initiate a system power cycle via the *PS-ON* signal. The off duration is stored as a non-volatile configuration parameter in the BMC.
SMI	The BMC can generate an SMI signal into the system interrupt logic. The SMI can be generated as the result of a watchdog timer time-out. Note that an SMI handler must be installed to handle the interrupt, or a system hang could occur.
SCI	The BMC is able to generate an SCI (system configuration interrupt) signal into the chip set. This is a provision in case a firmware maintenance update requires cooperation with ACPI.
System Hard Reset	The BMC can generate a system hard reset under firmware control. The BMC itself is *not* hardware reset by a system hard reset.
Processor Power Good	The BMC can control the *deassertion* of the *Power Good* signals to the processor slots. This is required as part of the processor disable process for fault resilient booting.
Processor Stop Clock	The BMC can individually control the *assertion* of the individual *Stop Clock* signals to the processor slots. This is required as part of the processor disable process for fault resilient booting.
Processor/Bus Clock Generator Default	The BMC can force the processor/bus clock generator to its default value. *See Section 4.3.11,* POST Error Logging.
Cooling Fault LED	The BMC can control the front panel connector's *Cooling Fault LED* signal. This is used in conjunction with the *Power Fault LED* signal to drive the System Status LED.
Power Fault LED	The BMC can control the front panel connector's *Power Fault LED* signal. This capability must be provided when the system is on 5V standby and when the system is powered up. This is used in conjunction with the *Power Fault LED* signal to drive the System Status LED.

Speaker   The BMC can control the baseboard speaker signal. This is used for communicating errors where the processors are unable to run, and there is no corresponding fault LED indication. For example, if there is an empty processor slot (see *Section 4.3.4, Processor Voltage Mismatch* and *Section 4.3.7, Missing Processor*/Terminator Module Detection).

Front Panel Lockout   The BMC provides command interfaces that implement a lockout of power-down and reset via the front panel power and reset push-buttons, respectively. See *Section 4.15, Secure Mode Control,* for more information.

Floppy Write Protect   The BMC is able to activate a control function that, while asserted, forces the on-board floppy interface to be write protected. See *Section 4.15, Secure Mode Control,* for more information.

Video Blank   The BMC can drive a signal that, while asserted, causes the on-board video to be blanked. See *Section 4.15, Secure Mode Control,* for more information.

4.4   Platform Management Connectors

The following describes the SCB2 baseboard connectors and connections for platform management.

4.4.1   Auxiliary IPMB Connector

The SCB2 baseboard provides an auxiliary IPMB connector. The auxiliary IPMB connector is a 3-pin, CD-style shrouded header that is provided for future add-in cards and potential OEM use.

The pin-out and type of connector is compatible with the auxiliary IPMB connector specified in the *Intelligent Platform Management Bus Protocol Specification.* Refer to the SCB2 Hardware EPS for any additional specifications on the allowable current sink/source, voltage level, and capacitive loading specifications for the auxiliary IPMB connector.

Devices that connect to the auxiliary IPMB connector must meet the loading requirements, specified in the Intelligent Platform Management Bus Communications Protocol v1.0 and must not short out the IPMB when they are unpowered. This requirement is to ensure that the BMC can be accessed via the isolated IPMB while the system is powered down an on 5V standby. This enables a remote management card to use the IPMB to access the BMC when the system is powered down.

4.4.2   ICMB Transceiver Header

The SCB2 baseboard contains an ICMB transceiver header. This header provides a connection to system 5V standby, ground, and to signal lines on one of the BMC's built-in serial ports for the purpose of connecting the ICMB transceiver card.

Since the BMC is also powered by 5V standby this allows the ICMB to be used to access system power control functions and to provide access to the system event logs and SDR information, regardless of whether the system is powered up or not.

4.4.2.1   ICMB Transceiver Power

If the ICMB transceiver card is added, it will require additional power beyond the 5V standby power requirements for the baseboard. Refer to the SCB2 Hardware EPS for more information.The ICMB header provides the connection point for the optional ICMB transceiver card.

4.5   Chassis Management Interconnection

The SCB2 baseboard uses the IPMB and specific front panel connector and power connector signals to merge chassis management features into the baseboard management features. Common front panel features, such as the power and reset push-buttons, power supply fault LED, fan failure LED, consolidated drive fault LED, and chassis intrusion signals are provided via direct signals in order to avoid the need to have active circuitry for the front panel.

Other, more sophisticated functions, such as hot-swap backplane interfaces and power supply monitoring, are integrated into the platform management via connection to the IPMB or private management bus (private management busses are described in Section 4.9).

4.5.1   IPMB Routing

IPMB connections are provided on the auxiliary IPMB connector. The auxiliary IPMB connection provides a standardized extension point for integrating chassis and add-in card management functions with the baseboard platform management subsystem.

The always-active portion of the IPMB is routed to the auxiliary IPMB connector. Devices that attach to this portion of the bus must remain active or go into a high-impedance state when the system is powered down. This is necessary to ensure that the always-active portion remains operative when on 5V standby power.

4.5.2   ICMB Connection

An ICMB transceiver board (optional on SCB2) provides transceivers and two keyed RJ-45, Type B ICMB connectors to enable the BMC to provide an external ICMB connection. The SCB2 supports the addition of this optional device via the ICMB header on the baseboard.

The ICMB is an inter-chassis management bus that provides management functions for clustered or grouped host systems and external peripheral chassis by transferring IPMI messages between different chassis. Since ICMB provides a way to deliver IPMI messages to the BMC, functions such as power and reset control, SEL, SDR, FRU, and sensor access are available, along with the ability to deliver IPMI messages to other BMC interfaces such as the system interface and IPMB. Refer to the *Intelligent Chassis Management Bus Bridge Specification v1.0* for additional information.

If the ICMB transceiver card is added, it will require additional 5V standby power beyond the 5V standby power requirements for the baseboard.

4.5.3   PCI Management Bus Connection

The PCI management bus is an SMBus 2.0 connection between the BMC and the SCB2 baseboard's PCI slots. The connection provides an IPMB-like ability for add-in management cards to communicate with the BMC using IPMI messaging per the *Intelligent Platform Management Interface v1.5 Specification.* By sending the appropriate IPMI commands to the BMC, an add-in card can access functions such as power and reset control, BMC sensors, and SEL, SDR, and baseboard field replaceable unit data.

4.5.4   Power Control Signals

Main power control is accomplished via the PS-ON signal from the baseboard to the power supply. When this signal is asserted (driven high), system power is commanded ON. When this signal is deasserted (High-impedance, or driven Low), system power is commanded OFF.

4.5.5   Hot-swap Backplane Management

A chassis that contains a hot-swap backplane can provide a management controller that allows the system SCSI or RAID controller to communicate RAID fault status via the SCSI connection to that backplane, and for that status to be able to be read back via the IPMB. For Ultra- and LVDS- SCSI busses, the SAF-TE (SCSI Accessed Fault-Tolerant Enclosures) interface is used.

SAF-TE provides a mechanism that enables RAID fault information to be sent to the hot-swap backplane via SCSI. The hot-swap controller then uses that information to control the drive fault lights. SAF-TE is also used as an in-band mechanism to retrieve information about the backplane such as local voltage, fan failure, and drive presence.

4.6   Field Replaceable Unit Information

The SCB2 platform management architecture supports providing FRU information for the baseboard and major replaceable modules in the chassis. Major modules, in this case, are defined as any circuit board in the system containing active electronic circuitry.

FRU information includes board serial number, part number, name, asset tag, and other information. Refer to the *Platform Management FRU Information Storage Definition* for the specification and format of the FRU information.

FRUs that contain a management controller use the controller to provide access to the FRU information. FRUs that lack a management controller can make their FRU information available via a SEEPROM directly connected to the IPMB. This allows the system integrator to provide a chassis FRU device without having to implement a management controller.

The SCB2 baseboard's FRU information is kept in non-volatile storage that is accessed via the BMC.

4.6.1   System Interface Ports

The BMC has two-sets of built-in ports that are mapped into system I/O space. One set of ports provides the system interface to the BMC for SMS use. The SMS interface is also used by the BIOS. The other set provides a private interface for System Management Mode (SMM) access by the SMI handler.

The system interface ports and BMC also function together to form the I^{2}C controller interface that allows system software to access the IPMB and private management buses. The SMS interface is compatible with the KCS interface specified in the *Intelligent Platform Management Interface Specification.*

4.6.2   BMC Front Panel Control

The BMC provides the main front panel control functions. These include control of system Power, Reset, Diagnostic Interrupt, and Identify push-buttons, the Status LED, and the Hard Drive fault LED. The Status LED and Identify LEDs are both provided when the system is powered down and only 5V standby power is available, and when the system is powered up. Front panel control also includes the front-panel lockout features.

4.6.2.1   Power Cycle Control

The BMC can drive a system power cycle from the following sources:

- Power-cycle via IPMI command received from EMP, DPC, IPMB, ICMB, PCI Management Bus, or the System Interface.
- Power-cycle from BMC watchdog timer expiration.
- Event generated power-cycle from platform event filtering.

4.6.2.2   Power Up Control

The BMC also drives system power up from the additional sources listed below. Note that power up / wake can also be initiated by Wake-on-LAN / Power On LAN / Magic Packet signals from an add-in network controller to the chip set, as well as Wake-on-Ring via the RI signal from Serial 2.

- Front panel push-button.
- IPMI *Chassis Control* command received from EMP, DPC, IPMB, ICMB, PCI management bus, or the system interface.
- AC power restore. The BMC can be configured to return system power to the state it was in when AC power was lost.
- Time of Day power up request from ACPI / system real-time clock.
- RI signal from back Serial 2 port.

4.6.2.3   Power Down Control

The BMC also drives system power down from the following sources:

- Front panel push-button (power down blocked if Secure Mode active).
- Power down from BMC watchdog timer.
- IPMI *Chassis Control* command to BMC received from EMP, DPC, IPMB, ICMB, PCI Management Bus, or the system interface.
- Event generated power down from platform event filtering.
- ACPI power down initiated by OS via chip set.

4.6.2.4   Hard Reset Control

The BMC drives system hard reset from the following sources:

- Front panel push-button (if Secure Mode deasserted).
- IPMI *Chassis Control* command to BMC received from EMP, DPC, IPMB, ICMB, PCI Management Bus, or the system interface.
- BMC watchdog timer.
- Fault-resilient booting timer (FRB-3) time-out.

4.6.2.5   Identify Push-button and LED Control

The SCB2 front panel connection supports a *Chassis Identify* push-button and a corresponding chassis identify LED. A second chassis identify connection is provided on the SCB2 baseboard to support a second Identify LED (LED1A1 - Blue) at the rear of the chassis.

The LED can provide a mechanism for identifying one system out of a group of identical systems. This can be particularly useful if the SCB2 baseboard is used in a rack-mount chassis in a high-density, multiple-system application.

The Chassis Identify LED can either be turned on locally via the push-button signal, or by local or remote software using the IPMI *Chassis Identify* command. The following list summarizes the Chassis Identify Push-button and LED operation:

- The Identify signal state is preserved on standby power across system power-on/off and system hard resets. It is not preserved if A/C power is removed. The LED state is off when A/C power is applied.

- The *Chassis Identify* command can also be used to control the LED. If a *Chassis Identify* command is used to turn on the LED, the command will automatically time out and turn off the LED unless another *Chassis Identify* command, to turn on the LED, is received. The default timeout for the command is 15 seconds. The SCB2 supports the optional command parameter to allow the timeout to be set anywhere from 1 to 255 seconds.

- The optional timeout parameter in the *Chassis Identify* command also allows software to tell the LED to go off immediately.

- The Chassis Identify push-button works using a "push-on/push-off" operation. Each press of the push-button toggles the LED signal state between on and off. If the pushbutton is used to turn the LED on, it will stay on indefinitely, until either the button is pressed again or a *Chassis Identify* command causes the LED to go off.

4.6.2.6   Front Panel Lockout

The BMC monitors a *Secure Mode* signal from the keyboard controller on the baseboard. When the system is powered up, and the *Secure Mode* signal is asserted, the BMC locks out the ability to power down or reset the system using the power or reset push-buttons, respectively. Secure Mode also blocks the ability to initiate sleep requests from the front panel. Secure Mode does not lock out powering up the system or waking the system from an ACPI sleep state.

The BMC generates a *Secure Mode Violation Attempt Event* message if an attempt it made to power-down, sleep, or reset the system using the push-buttons while Secure Mode is active.

The BMC also provides options for blanking the on-board video, and write-protecting the on-board floppy interface when Secure Mode is active, plus provides commands for setting these options. In addition, the commands can be used by software to force the Secure Mode options to be asserted, even when the Secure Mode signal is not asserted.

4.7   Intelligent Platform Management Buses (IPMB)

The IPMB is a multi-master, open-drain, serial bus that is routed between the major system boards. The internal version of the IPMB is electrically and timing compatible with the 100 kbps version of the I^2C bus specification. Other management controllers can be connected to this bus. These controllers can be used to provide monitoring and control functions for system management.

A communication protocol has been defined on the IPMB. This protocol is specified in the *Intelligent Platform Management Bus Communications Protocol Specification*. The protocol is used for communication between management controllers on the IPMB. The IPMB also supports low-level I^2C read/write operations for non-intelligent devices such as FRU SEEPROMs and OEM value-add devices that do not use the protocol.

The IPMB is primarily intended for the connection of management controllers, emergency out-of-band management access to platform sensors, add-in FRU information, and chassis-specific information that does not require polling at a high rate. Thus, the SDR repository, SEL, and sensors are placed behind the BMC in order to keep their traffic off the IPMB.

The IPMB protocol includes provisions for checksums and retries that provide additional data integrity that is lacking in typical non-intelligent devices. By placing non-intelligent devices behind a controller, they effectively inherit the IPMB protocol integrity mechanisms. Placing managed devices behind the BMC also frees up the I^2C addresses those devices would have used up on the IPMB.

The same approach should be used for OEM add-on management devices. To keep the IPMB free for event messages and management controller access, system integrators should implement their additional sensors behind management controllers and avoid placing non-intelligent I^2C devices directly on the IPMB. FRU information should also be behind a management controller when possible.

4.8   PCI Management Bus

The PCI Management Bus is an SMBus 2.0 connection between the BMC and the SCB2 baseboard PCI slots. The connection provides an IPMB-like ability for add-in remote management cards to communicate with the BMC using IPMI messaging per the *Intelligent Platform Management Interface v1.5 Specification.*

By sending the appropriate IPMI commands to the BMC, an add-in card can access functions such as power and reset control, BMC sensors, SEL, SDR, and baseboard FRU data. The bus operates at up to 100 kbps and remains active on standby power so that add-in cards can communicate with the BMC during any system power state.

Refer to the *Intelligent Platform Management Interface v1.5 Specification*, the *System Management Bus (SMBus) Specification Version 2.0*, and the *PCI Engineering Change Notice – Addition of the SMBus to the PCI Connector* for additional information.

4.9   Private Management Buses

A Private Management Bus (PMB) is a single-master I^2C bus that is controlled by the BMC. Access to any of the devices on the PMB is accomplished indirectly via commands to the BMC, via the IPMB or system interfaces. PMB is a common mechanism used for accessing temperature sensors, system processor information, and other baseboard monitoring devices that are located in various locations in the system.

The devices on the PMB are isolated from traffic on the IPMB. Since devices, such as temperature sensors, are polled by the BMC, this gets the polling traffic off the public IPMB bus. This also increases the reliability of access to the information, since issues with IPMB bus arbitration and message retries are avoided. Furthermore, placing managed I^2C devices on the PMB frees up the I^2C addresses that those devices would have used up on the IPMB.

4.10   Wake-on-LAN / Power On LAN and Magic Packet Support

The SCB2 baseboard supports Wake-on-LAN / Power-On-LAN capability using the on-board network interface chips or an add-in network interface card. An add-in network card can deliver the wake signal to the baseboard via the Power Management Event (PME) signal on the PCI bus. The actual support for Magic Packet and/or packet filtering for Wake-on-LAN / Power-On-LAN is provided by the NIC. The baseboard handles the corresponding wake signal.

4.10.1   Wake-on-LAN in S4/S5

The SCB2 contains a configuration option that allows the on-board NICs to be enabled to wake the system in an S4/S5 state, even if the operating system disabled Wake-On-LAN when it powered down the system. This provides an option for users who want to use standard, but non-secure, Wake-on-LAN capability for operations such as after-hours maintenance. Note that the DPC LAN capability provides a secure system power-up, plus the ability to provide BIOS boot options, by sending authenticated IPMI messages directly to the BMC via the on-board NICs.

4.11 Emergency Management Port (EMP)

Emergency Management Port refers to the Intel implementation of IPMI v1.5 serial port sharing and IPMI messaging over serial/modem interface. On the SCB2, the serial 2 port connection can be configured for use as an EMP, where the serial connector can be shared between the BMC and the baseboard Universal Asynchronous Receiver Transmitter (UART).

This connection provides a level of systems management via RS-232 during powered-down, pre-boot, and OS-down situations. This can be used in legacy management environments that utilize point-to-point RS-232-based management, or to provide simple emergency management using an external modem. The EMP is designed to work with serial modems that support the TIA-602 command set.

The basic management features offered by the EMP are:

- System power up/down control.
- System reset and diagnostic interrupt (front panel NMI) control.
- Ability to set temporary BIOS boot options, that include the ability to signal BIOS to initiate boot from alternative sources such as a diagnostic partition or PXE (see the *SCB2 BIOS EPS* for more information).
- System chassis intrusion, cooling, and power subsystem status.
- Access to the system event log.
- Access to the sensor data record repository.
- Access to sensors managed by the BMC and other management controllers on IPMB.
- Access to the baseboard field replaceable unit inventory information managed by the BMC and other management controllers on the IPMB.

A challenge/response -based authentication can be enabled to provide security for accessing the interface via the ISC management software. Other security options are available for customers that write their own interface software. Refer to Section *4.11.2, Serial/Modem Channel Specifications* for a list of the security authentication types supported by the SCB2 BMC.

4.11.1   Serial/Modem Alerting

There are two types of serial/modem alerting supported in the BMC: dial page, and PPP alert. Serial/modem and LAN alerting are triggered via platform event filtering.

Dial Page   This is a numeric page. The BMC uses an external modem to dial keypad numbers in order to call a paging service and deliver a page via a user-configured paging string. The paging string directs the modem to deliver a fixed number to the paging service. This is often used to deliver the phone number of the system that is generating the alert. An administrator receiving the string can then call the system with a management application such as Intel Server Control, and use the EMP to retrieve system status and more detailed information about the alert.

PPP Alert   The BMC dials a PPP account, makes an Internet Protocol (IP) connection and delivers a PET alert to a management application at a given IP address on that network. The PET is a standardized Simple Network Management Protocol (SNMP) trap that contains information about the type of event that generated the alert. The event data encoding follows the format of an IPMI event message. See

[PET] for more information. The PPP account can be local or remote, based on whether the emergency management port is configured for direct mode or modem mode, respectively. If the account is remote, the BMC uses user-configurable, non-volatile parameters that hold the phone number and user login information necessary to connect to the remote network.

Serial/modem alerting is triggered when the BMC receives (or internally generates) an event that matches one of a set of pre-configured patterns, called event filters (see Section Platform Event Filtering and Alerting), where the selected action is Alert.

Associated with the alert action is an alert policy that determines what type of alert (e.g., dial page or PPP alert) should be sent and which serial/modem and/or LAN destinations the alert should be sent to. The alert policy also determines whether the BMC will stop alerting when an alert to a destination is successful.

4.11.2   Serial/Modem Channel Specifications

The following table presents the minimum support that will be provided. Note that system management software and utilities may only utilize a subset of the available BMC options. For detailed technical information on the operation of the LAN channel operation and LAN alerting, refer to the *Intelligent Platform Management Interface v1.5 Specification.*

Table 15. Serial/Modem Channel Specifications

Configuration Capability	Options	Description/Notes
Connection Type support	direct connect, modem	The type of connection between the remote console and the serial port: Direct Connect Supports direct cable connection to the serial port without going through a modem. Modem Supports using a TIA-602 compatible external modem for remote management.
Connection Mode	Basic Mode, PPP Mode	Determines the type of protocol used for IPMI messaging with the remote console. Basic Mode IPMI messages are sent over the serial interface using a low-overhead IPMI-specific serial packet format. PPP Mode IPMI messages are encapsulated in a Univesal Datagram Packet (UDP) datagram format compatible with the RMCP packet format specified in the *DMTF Pre-OS Working Group Alerting Specification*.
Channel Access Modes	pre-boot, always-active, disabled	This option determines when the BMC is allowed to take control of the serial port.
Serial Port	"COM2"	
Bit Rates	9600 bps, 19.2 kbps, 38.4 kbps, 57.6 kbps	
bits	8	
stop bits	1	
parity	none	
Flow Control options	hardware (RTS/CTS), none	
Serial Port Sharing	Yes	Ability to share the serial connector between the BMC and the baseboard UART.
Number of Sessions	1	The number of simultaneous sessions that can be supported is

Configuration Capability	Options	Description/Notes
		shared across the LAN and serial/modem channels.
Number of Users	4	User information is a resource that is shared across the LAN and serial/modem channels.
Configurable User Names	Yes	
Configurable User Passwords	Yes	
Privilege Levels	Callback, User, Operator, Administrator	
IPMI Message Authentication Type Support	MD2, MD5, Straight Password, none	
Alerting Support	Dial Page, PPP Alerting	
Combined number of Alert and Callback phone numbers	6	Number of destinations and dial strings
PPP Dial-in Link Authentication Support	PAP, CHAP, MS CHAP-V1 and V2, none	
PPP Dial-out Link Authentication Support	PAP, CHAP, MS CHAP-V1 and V2, none	
PPP Destination Accounts	2	
Number of PPP Alert Destination IP Addresses	4	
PET Acknowledge support	Yes	PET traps are only used with PPP Alerting
Callback Security	Yes	

4.11.3   BMC-Emergency Management Port Connection

Logic on the SCB2 baseboard allows the transmit data (TxD) and receive data signals, for the Serial 2 port connector, to be switched to the BMC or to the baseboard serial port controller under control of the BMC. The port transceivers are powered from 5V standby power so that communication with the BMC can occur while the system is powered down.

4.11.4   Emergency Management Port Direct Connect and Modem Connect Options

The system BIOS provides a setup interface that allows the user to select Direct Connect or Modem Connect operation. *Direct Connect* mode is for applications that connect the port directly to another computer system, while *Modem* mode is for applications where the port is connected to an external modem.

4.11.5   Emergency Management Port Access Mode Options

BMC non-volatile storage retains a configuration option for the selection of several access modes. These modes allow the system user to provide differing levels of security and features. These are summarized in the table below. Refer to the *SCB2 BIOS EPS* for more information on the BIOS Setup options.

If the EMP is enabled, it will be activated (serial connector routed to the BMC) while the system is powered down, on system power up transition, and on system hard resets.

Pre-boot only   In this access mode, the port is only available while the machine is powered-off and during POST. Just prior to booting the OS, the system BIOS switches the serial connection to the baseboard serial port controller. This switch occurs regardless of whether the EMP was in use at the time.

At this point, the serial connection is dedicated to normal OS use. During OS operation, the EMP will not be automatically activated by the BMC. The BMC will not activate the EMP until the next system power-down or hard reset, unless directed to by system management software. See *4.11.13, System Management Software Activation of the Emergency* Management Port for more information.

Note that platform event filtering and serial / modem alerting are controlled separately. The BMC can take over the port in order to send an alert.

Always Available   In this access mode, the EMP remains able to be activated even after the system has booted. When *Always Available* mode is selected, BIOS typically dedicates the on-board Serial 2 port to EMP use. Just prior to booting the OS, BIOS disables the on-board serial controller for the Serial 2 port. This allows the serial connection to be used for EMP operations without concern that it will be inadvertently accessed by OS applications that are unaware of the possible interactions between the on-board serial port controller and the EMP.

The EMP will also be automatically reactivated when the system is powered down, and on system hard resets. Note that if BIOS disables the on-board serial controller, console redirection will not be available after the on-board Serial 2 port has been disabled. Thus, console redirection would only be usable for monitoring POST progress and running BIOS F2 Setup routines remotely.

Shared   In this access mode, the BMC is allowed to answer the phone, but run-time software is able to use the serial connection when it is not being used by the BMC. BIOS can use the *Get Channel Access* command to see when the BMC is configured for shared mode. In this case, it can leave the serial port enabled for run-time software access. The serial/modem configuration parameters include a ring interval parameter that can be used to enable the BMC to only answer the phone if system software does not. This is accomplished by simply setting a ring interval for the BMC that is longer than the time it takes system software to answer.

Disabled   When the Disabled option is selected, the EMP will not be activated by BIOS during POST, nor will it be automatically activated when the system is powered down or on system hard resets. The BMC retains a non-volatile configuration parameter to retain this setting in case system AC power is lost.

Table 16. Emergency Management Port Access Options

	Disabled	Pre-boot Only	Always Available	Shared
Console Redirection Coverage	POST and run-time [1]	POST and run-time [1]	POST to start of boot	POST and run-time [1]
Baseboard Serial 2 available for normal O/S use	Yes	Yes	No	Yes [4]
EMP accessible during run-time	No [2]	No [2]	Yes	Yes [4]
EMP active during power-down	No	Yes	Yes	Yes
EMP activated on hard resets	No	Yes	Yes	Yes
EMP activated on Ring Indicate	No [2]	Only during pre-boot [2]	Yes	Yes [5]
EMP activated on DCD loss	No [2]	Only during pre-boot [2]	Yes	Yes [5]

Notes:

1. Run-time coverage provided as long as system uses *Text Video* mode.
2. Can be enabled during run-time by system management software.
3. Run-time auto-answer applications may not function.
4. For modem connections, the BMC and auto-answer applications need to be configured to answer on fewer rings than the BMC in order for this operation to be transparent to those applications. If auto-answer applications are not used, the BMC can be configured to always answer the phone.
5. These conditions can be individually enabled or disabled in the BMC configuration.

4.11.6   BIOS Console Redirection Interaction with the Emergency Management Port

The EMP can share the Serial 2 port with BIOS console redirection. When a remote EMP console application directs the system to reset or power up, it can also direct whether or not it stays connected to the BMC or transfers BIOS console redirection characters. Early in POST, BIOS console redirection requests that the serial connector be switched over to the baseboard serial controller. If the remote application directs the BMC to stay connected, the switch request will be denied. Otherwise, the request will be honored and console redirection traffic will go across the serial connection.

The BMC also has a command that allows BIOS to force the serial connector to be switched over to the baseboard serial controller. This command is provided to support the pre-boot only and disabled configurations of the EMP.

4.11.7   PPP Activation of the Emergency Management Port

The BMC can be configured to snoop the serial connection, while it is switched to the baseboard, and automatically takeover the serial port whenever it detects a PPP packet directed to the BMC's IP and UDP port address.

4.11.8   Callback Security Option

The BMC firmware on the SCB2 supports a callback configuration option that can be used with OEM-created console applications. The callback facility provides a mechanism to direct the BMC to call a pre-configured callback destination in order to establish an EMP session. The destination can be either a basic mode destination or a PPP account destination.

Once the phone connection has been made, the same user authentication and session activation steps are used as if the remote console had directly initiated the connection. The BMC sends a *Ping* message that indicates to the remote application that a BMC connection is available.

4.11.9   Microsoft* 'Headless' Console Escape Sequence Activation of the Emergency Management Port

For both PPP and Basic mode, the BMC can be configured to enable switching the connection when it sees an "<ESC>(" sequence. This sequence is defined by the Windows* Platform Design Notes as a sequence that directs the serial port to switch from the baseboard UART to service processor (BMC) connection.

Similarly, an "<ESC>Q" sequence can be enabled to switch the connection from the BMC back to the baseboard UART.

By default, recognition of these sequences are not enabled nor required, since a remote console utility would typically send a command directly to the BMC to accomplish the switch.

4.11.10   Ring Indicate and DCD Activation of the Emergency Management Port

The SCB2 BMC allows the EMP to be activated when the back Serial 2 port's *Ring Indicate* signal becomes asserted, or upon changes of the serial port's *DCD* (Data Carrier Detect) signal (the front connection to the SCB2 COM2 port does not support RI).

If enabled, the BMC will first monitor RI and will claim the serial connection after seeing the phone ring for the time specified by the Modem Ring Time parameter, in the serial/modem configuration parameters, and according to the selected access mode and connect mode (Direct Connect / Modem Mode). If DCD is already active, the BMC will monitor the incoming data stream for the start of an IPMI session. If DCD is not already present, the BMC initializes the modem by sending the initialization string. The BMC then listens for a "RING" result code from the modem and sends out an "ATA" to answer the phone.

4.11.11   Emergency Management Port Interaction with Wake-on-Ring

The same serial port that is used for the EMP can be separately enabled for Wake-on-Ring (WOR). It is recommended that the system has Wake-on-Ring disabled whenever the EMP is enabled. That way, system power up is always remotely controlled via the EMP. Since the EMP requires establishing a connection to the BMC, there is no concern that a wrong number powers up the system.

It may be desired to enable Wake-on-Ring and the EMP, such that both non-EMP remote applications and the EMP remote console applications can dial in to the system. In order to help enable this, the configuration options for the EMP to include a parameter that sets the time the BMC lets the phone ring before answering. This allows the ring time for the EMP to be set to a value that is longer than the ring timeout for the non-EMP application. This could be used as follows:

1. A remote non-EMP application attempts to call in to the system. Because the system is already powered down, the call wakes the system via Wake-on-Ring. The remote application times out and hangs up before the BMC answers the phone. The BMC

recognizes that ringing has stopped before its ring time interval has expired and therefore does not answer the phone.

2. The remote party assumes that the system was asleep and that it may take several minutes before the OS loads and is ready to accept a call. The remote party waits and then dials in again. This time, the OS application answers before the BMC answers the phone.

3. A problem occurs where the OS hangs. An EMP application will then be able to call in by letting the call ring until the BMC answers the phone.

4. Alternatively, if communication to the OS occurs in PPP mode, or it is known that the "<ESC>(" sequence does not occur in the data stream, the BMC can be configured to enable activating the EMP on those sequences. It would then be possible to have the remote EMP application switch the port over after the OS application had answered the phone.

If Wake-on-Ring is enabled with a ring time that is less than the timeout for the non-EMP remote application, users should be aware that the following scenario could occur:

1. A remote application attempts to use Wake-on-Ring to wake the system in order to connect to an application running under the OS.

2. Assume the system is powered down and configured to Pre-Boot Only mode. The BMC will answer the phone when the call comes in.

3. Because Wake-on-Ring is enabled, the system simultaneously powers up. Meanwhile, the BMC is waiting for a remote console application to establish a communication session with it.

4. The BMC times out waiting for a session to be activated and hangs up the phone.

5. If the EMP is set to Pre-Boot Only mode, the user can wait for the OS to load before they can call in again and establish communication with the OS. If the EMP is set to Always Available mode, and the BMC ring-time delay is less than the OS application's answer delay, the BMC will always answer the phone before the OS application can.

4.11.12   Activation of the Emergency Management Port during Console Redirection

The BMC can be configured to monitor the incoming serial stream for data patterns and escape sequences that will cause it to claim the serial connection when the EMP is enabled. In PPP mode, the BMC can be configured to automatically claim the connector when it sees a packet directed to its IP address and UDP port. In Basic mode, the BMC can be configured to look for an "<ESC>(" sequence.

4.11.13   System Management Software Activation of the Emergency Management Port

If the EMP is not configured for Shared mode, but either the *Disabled* or *Pre-Boot Only Access* option has been selected, local system management software can still elect to activate the EMP

during OS operation. This allows the EMP to be available for a remote management application should the system hang, while SMS can use the port for modem-based management functions, such as dial-out alerting and access to system instrumentation software.

To do this, SMS uses the O/S's communication interfaces to take ownership of COM2. SMS can then send commands to the BMC to activate the EMP.

Note: if the *Disabled* option has been selected, the EMP will be automatically deactivated on the next system hard reset or power-off.

4.11.14   Modem Setup

If configured for Modem mode, the BMC will send a modem configuration string prior to issuing the modem command to answer the call. This string is kept in non-volatile storage associated with the BMC. The configuration string content may be dependent on the type of modem used. SCB2 is factory pre-configured with a string that works with common TIA-602-compatible external modems. The string is user configurable via the Server Setup Utility (SSU).

4.11.15   Connection Timeout

If the serial connection is switched to the BMC, the BMC will terminate the IPMI messaging sessions and send a hang-up string to the modem if it has been more than two minutes since the remote EMP console application has provided a correct message via the EMP.

4.11.16   Emergency Management Port User Passwords

The emergency management port uses the IPMI Channels and Session model for authentication. This includes using the IPMI commands for configuring user access capabilities, privilege limits, and passwords.

The password is entered and used by the BMC as a 16-byte binary value. Thus, the password can be set to ASCII text, or a 16-byte binary key, based on what is supported by the configuration and remote console applications. In order to be able to change a password remotely, a user must have administrator privilege. The user does not have to enter the previous EMP password in order to change it.

The EMP user passwords are separate from the BIOS user and administrator passwords. Thus, knowing the EMP password does not automatically mean that the user can enter BIOS Setup.

4.11.17   Invalid Password Handling

If three successive invalid *Activate Session* commands are received on the EMP interface, the BMC will send the hang-up sequence (if in Modem mode) and delay 30 seconds prior to accepting another *Activate Session* command. The BMC will also log a Secure Mode Violation Attempt event to the system event log each time an invalid *Activate Session* command is received.

4.12 Direct Platform Control (IPMI over LAN)

Direct Platform Control (DPC) provides a mechanism for delivering IPMI messages directly to the BMC via a LAN connection. The NICs and the BMC remain active on standby power,

enabling the IPMI messaging when the system is powered up, powered down, and in a system sleep state. This allows a remote console application to be able to access the BMC's capabilities, including:

- Power on/off and reset control with the ability to set BIOS boot flags.
- Field replaceable unit, sensor data record, and system event log access.
- BMC configuration access.
- Ability to transfer IPMI messages between the LAN interface and other interfaces, such as the system interface, IPMB, and PCI management bus. This capability enables messages to be delivered to system management software, and provides the ability to access sensors and FRU information on other management controllers.

IPMI messages are encapsulated in a packet format called RMCP (Remote Management Control Protocol). The Distributed Management Task Force (DMTF) has defined RMCP for supporting pre-OS and OS-absent management. RMCP is a simple request-response protocol that can be delivered using UDP datagrams. IPMI-over-LAN uses version 1 of the RMCP protocol and packet format.

UDP port 26Fh is a well-known port address that is specified to carry RMCP-formatted UDP datagrams. The on-board Intel network interface controllers contain circuitry that enables detecting and capturing RMCP packets that are received on Port 26Fh and making them available to the BMC via a side-band interface that is separate from the PCI interface to the NIC. Similarly, the BMC can use the side-band interface to send packets from Port 26Fh, as shown in the following figure.
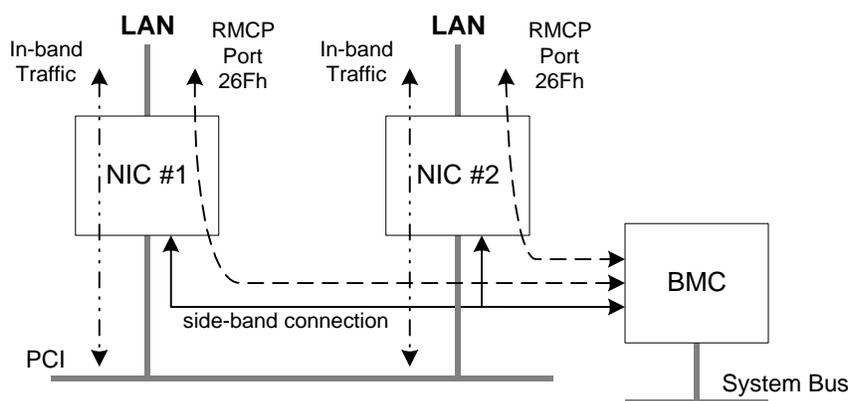
Figure 11. IPMI-over-LAN

RMCP includes a field that indicates the class of messages that can be embedded in an RMCP message packet. For RMCP version 1.0, the defined classes are IPMI, ASF, and OEM. IPMI-over-LAN uses the IPMI class to transfer IPMI messages encapsulated in RMCP packets. The *Intelligent Platform Management Interface v1.5 Specification* specifies the packet formats and commands used to perform IPMI messaging on LAN via RMCP.

4.12.1   LAN Channel Specifications

The following table presents the minimum support that will be provided. Note that system management software and utilities may not use all the available BMC options and capabilities. For detailed technical information on the operation of the LAN channel operation and LAN Alerting, refer to the *Intelligent Platform Management Interface v1.5 Specification.*

Table 17. LAN Channel Specifications

Configuration Capability	Options	Description/Notes
Channel Access Modes	Always-active, Disabled	This option determines when the BMC can be accessed via IPMI messaging over LAN.
Number of Sessions	4	The number of simultaneous sessions that can be supported is shared across the LAN and serial/modem channels.
Number of Users	4	User information is a resource that is shared across the LAN and serial/modem channels.
Configurable User Names	Yes	User information is a resource that is shared across the LAN and serial/modem channels.
Configurable User Passwords	Yes	
Privilege Levels	Callback, User, Operator, Administrator	Note that a callback level allows a LAN user to trigger a callback on the serial/modem channel.
IPMI Message Authentication Type Support	MD2, MD5, Straight Password, none	
Number of LAN Alert destinations	4	
PET Acknowledge support	Yes	
Gratuitous ARP Support	Yes	

4.12.2   Network Controller Teaming and Failover Restrictions

It is possible to use Intel networking drivers and software to operate the networking hardware in a teamed or fail-over arrangement. In these arrangements, the same IP address can be for more than one NIC. In the teaming case, this is used to gang the NICs in order to increase the bandwidth to/from the server at that IP address. In the fail-over case, one NIC is activated and takes over the IP address when a partner NIC fails.

Because the same IP address may be used on multiple NICs, there are certain teaming and fail-over arrangements that can cause situations where IPMI-over-LAN packets get received by an add-in NIC instead of the on-board NIC connected to the BMC.

Thus, there are certain restrictions to how IPMI-over-LAN can be used in teaming and fail-over arrangements:

- On-board NICs used for IPMI-messaging can only be teamed with or failed over to another on-board NIC (i.e., you can team the two on-board NICs together).

- Unless static IP addresses are used, the IP addresses for the LAN connections to the BMC will need to be set to the same value when teaming is in effect. Just loading the

teaming drivers may not be sufficient in some installations. In order to avoid networking issues, it may be necessary for local system management software to set the IP addresses when the two on-board NICs begin teamed operation.

- It is possible to use just one of the on-board NICs for IPMI messaging and alerting and use the other on-board NIC in a teaming or fail-over arrangement with one or more add-in cards. In this case, IPMI messaging and alerting should be disabled for any on-board NIC that is to be teamed, or used in a fail-over arrangement with, an add-in NIC. The SSU can be used to configure whether IPMI messaging and alerting are enabled for a given on-board NIC. Note that this configuration may not be supported with Intel-supplied system management software.

4.12.3   LAN Drivers and Setup

The IPMI-over-LAN feature must be used with the appropriate Intel NIC driver, and the NIC correctly configured in order for DPC LAN operation to occur transparently to the OS and network applications. If an incorrect driver or NIC configuration is used, it is possible to get driver timeouts when the IPMI-over-LAN feature is enabled.

4.12.4   BIOS Boot Flags

A remote console application can use the IPMI *Set Boot Options* command to configure a set of BIOS boot flags and boot initiator info parameters that are held by the BMC. These parameters include information that identify the party that initiated the boot, plus flags and other information, that can be used to direct the way booting proceeds after a system reset or power-up (e.g, whether the system should boot normally, boot using PXE, boot to a diagnostic partition, etc.). Refer to the *SCB2 BIOS EPS* for which particular boot options are supported.

4.12.5   Boot Flags and LAN Console Redirection

The SCB2 BIOS includes a LAN console redirection capability. This capability can only be directed to one IP address at a time. Thus, the boot flags and boot initiator information are also used to tell the BIOS where to send LAN console redirection. Refer to the *SCB2 BIOS EPS* for more information.

4.13 Platform Event Filtering and Alerting

PEF is an IPMI 1.5-specified capability that allows the BMC to be configured to take a selected action when a given event occurs.

The BMC maintains a table of patterns, called event filters, which select which events trigger a page (or other action). For each received event message (either externally or internally generated) the BMC compares the event against the entries in the event filter table. If there is a match, the BMC will perform the action or actions that have been pre-configured for the filter entry. Possible PEF actions include Power Off, Power Cycle, Reset, and Send Alert.

Event filter table entries (event filters) include wild-carding capability that enables a given filter to match up with a single event, a class of events, or even multiple types of events. It is typical to have more than one filter entry trigger a given action. It is also possible for the configuration to have overlap, where it is possible that an event would match more than one filter. The BMC scans all event filters, accumulating matches before taking any actions, acting on the highest

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priority actions first. Per the *Intelligent Platform Management Interface v1.5 Specification* the following table lists the prioritization of PEF actions.

Table 18. PEF Action Priorities

Action	Priority	Additional Information
power down	1	
power cycle	2	Will not be executed if a power-down action was also selected.
reset	3	Will not be executed if a power-down or power cycle action was also selected.
Send Alert	4	Send alerts in order based on the selected alert policy. Alert actions will be deferred until after the power down has completed. There is an additional prioritization within alerts being sent: based on the Alert Policy Table entries for the alert.

4.13.1   Pre-defined Event Filters

Event filters can be tagged as being either user-configurable or pre-defined for system use. System software is allowed to enable the user to set any values for the user-configurable filters.

The SCB2 baseboard is factory pre-configured with a number of manufacturer pre-defined event filters. This provides a common set that can be enabled and disabled using the SSU. Additional entries can be tagged as being reserved for system use. This allows a system integrator to configure and lock down additional pre-defined entries for their product, if desired.

Platform event filtering is independent of event logging. Event logging and PEF (and associated actions) are enabled/disabled independent of one another.

The SCB2 comes with the following pre-configured event filters. Note that Intel software and utilities may depend on these definitions; therefore, the initial set of pre-configured event filters should not be altered unless it can be done in a manner where the changes are in synch with the software.

These entries define a standard set of events for the filters. The factory default is to have no actions enabled. A utility application, such as the Intel system setup utility , allows the user to select which actions should be associated, if any, with the pre-configured event filters.

Table 19. Pre-configured Event Filters

Event Filter #	Events
0	Temperature Sensor out of range
1	Voltage Sensor out of range
2	FAN Failure
3	Chassis Intrusion [Security Violation]
4	Power Supply Fault
5	BIOS (SMI Handler): Uncorrectable ECC error
6	BIOS: POST Error Code

7	FRB Failures
8	Fatal NMI (NMI from source other than Front Panel NMI or Uncorrectable ECC Error).
9	Watchdog Timer reset, power down, or power cycle
10	System restart (reboot)
11	Reserved

4.13.2   Alert Policies

Associated with the alert action is an Alert Policy that determines what type of alert (e.g., dial page or PPP alert) should be sent and which serial/modem and/or LAN destinations the alert should be sent to.

The BMC maintains a non-volatile Alert Policy Table. This table holds alert policy entries. Each entry specifies a particular alert destination and the policy regarding whether the BMC will stop alerting when an alert to the destination is successful, or will continue and process other entries.

Each alert policy entry also contains a policy number that is used to bind multiple alert policy entries together into policy sets. When the action, for a given event filter table entry, is set to *Send Alert,* the policy number field for the filter identifies which alert policy entries should be used to send the alert. The BMC acts on each alert policy entry in order of appearance in the Alert Policy Table. Refer to the *Intelligent Platform Management Interface v1.5 Specification* for more information.

The entries in the Alert Policy Table are user configured. Since it is not know beforehand what types of destinations and alerts the user may want to send, the Alert Policy Table is unpopulated as shipped from the factory.

Table 20. Alerting Capability Specifications

Capability	Options
Alerting Types	PET LAN Alerting, Dial Page, PPP Alert
Alert Acknowledge support	Yes
Number of total PEF Event Filter Table Entries	20
Number of manufacturer pre-defined PEF Entries	12
Number of software-configurable PEF Entries	8
PEF Actions	power off, reset, power cycle, send alert
Number of Alert Policy Entries	20

4.13.3   Alert Destinations

As mentioned above, each alert policy entry identifies a single alert destination for the alert. In this case, the term *Alert Destination* refers to the set of parameters that provides information such as the alert type (e.g., LAN alert, PPP alert, dial page) as well as the addressing

information and communication parameters for a particular destination. Other information, such as alerting strings and PPP accounts, can also be associated with a destination.

Alert destination information for serial/modem and LAN alerts are kept in non-volatile storage as part of the configuration parameters for the serial/modem and LAN channels on a per-channel basis. Since the SCB2 can have two LAN channels, each channel can have different alert destinations configured for it. This can be useful if the LAN interfaces are connected to different LAN segments or subnets.

Each set of information, for an alert destination for a given channel, is identified with a number referred to as the destination selector. The alert policy entry contains fields for the destination selector and the channel number. Together these fields uniquely identify an alert destination.

4.13.4 Alert Destination Priorities

Alerts are handled according to the type of destination for the alert. LAN alerts are handled as soon as they are encountered in the alert policy. Serial/modem alerts, however, may be postponed if the serial/modem channel is already busy sending an alert to another destination.

Whether or not a serial/modem alert is postponed is based on the priority of its destination. This is done primarily to support sending multiple alerts to a given PPP account without requiring the BMC to hang-up the connection.

The connection to the PPP account will be maintained for a length of time determined by a *PPP Account Connection Hold Time* parameter that is associated with the configuration parameters for each PPP account. During this time, if more events occur, they will be delivered on the same connection, unless an alert is to be delivered to a higher priority destination, in which case the present connection will be terminated as soon as the present alert transmission completes. Refer to the *Intelligent Platform Management Interface v1.5 Specification* for more information.

Table 21. Serial/Modem Alert Destination Priorities

Destination Type	Priority (0 = highest)	Comments
PPP Account #1	1	All destinations behind a given PPP account are at equal priority. Destinations behind an account are handled in the order that they occur in the Alert Policy Table entry associated with the account.
PPP Account #2	2	
Dial Page	3	All dial page destinations are at equal priority. They are handled in the order that they occur in the entries for the given alert policy.

4.13.5 Alert Acknowledge

PET, PPP, and LAN alerts delivered in PET format can either be *acknowledged* or *unacknowledged.* SNMP traps are typically sent as datagrams where the alerting party does not get a positive confirmation that the trap has been received. IPMI includes a *PET Acknowledge* command that a remote console can use to provide a positive acknowledgement that the PET alert was received.

The success criterion for an alert policy entry is dependent on whether the alert has a positive confirmation or not. If the alert destination information indicates that the destination supports

PET acknowledge, then PEF will expect to receive a *PET Acknowledge* command and will consider the alert to have failed if an acknowledge is not received (note that the configuration information also supports a retry parameter for the alert).

4.13.6   System Identification in Alerts

Dial paging offers no special support for automatically providing a system identification value in the page. The user will need to configure this information into the page string manually, using an encoding of the system designation that is compatible with the selected paging service. One suggestion for numeric paging services is to include the phone number of the modem connected to the EMP.

The PET alert format used in PPP and LAN alerting contains a system Globally Unique ID (GUID) field that can be used to uniquely identify the system that raised the alert. In addition, since the PET is carried in a UDP packet, the alerting system's IP address is also present.

4.13.7   Platform Alerting Setup

The BMC provides commands via the system interface that support setting/retrieving the alerting configuration for serial/modem and LAN alerting in BMC NV storage.

The user does not typically deal with filter contents directly. Instead, the SSU provides a user interface that allows the user to select among a fixed set of pre-configured event filters.

The following list presents the type of alerting configuration options that are provided:

- Enabling/disabling PEF.
- Configuring alert actions.
- Selecting which pre-configured events trigger an alert.
- Generating a test event to allow the paging configuration to be checked.
- Configuring the serial/modem and PPP communication and link parameters.
- Configuring the alert destination information, including LAN addresses, phone numbers, alert strings, etc.
- Configuring the PPP accounts for PPP alerting (PPP accounts represent the phone number and user login information necessary to connect to a remote system via PPP).

4.13.8   Alerting On Power-Down Events

The BMC is capable of generating alerts while the system is powered down. A watchdog power-down event alert is sent after the power down so that the alert does not delay the power-down action.

4.13.9   Alerting On System Reset Events

Reset event alerts occur after the reset. The alerting process must complete before the system reset is completed. This is done to simplify timing interactions between BMC and BIOS initialization after a system reset.

4.13.10   Alert-in-Progress Termination

An alert in progress will be terminated by a system reset or power on, or by disabling alerting via commands to the BMC.

4.14 ACPI Support

The BMC management features are designed to work in conjunction with the ACPI BIOS and hardware features of the SCB2 baseboard. The following sub-sections summarize these capabilities.

4.14.1   ACPI Power Control Support

The BMC includes interfaces to ACPI, and the chip set that direct it, to operate in one of two power control modes during system operation: Legacy mode, and ACPI mode.

In Legacy mode, the Sleep push-button is ignored. The Power push-button is used to cause power-on and power-off of the system without OS involvement (power-off is disallowed if Secure mode front panel lockout is active).

In ACPI mode, the BMC works with the baseboard's chip set to implement ACPI-compatible power control. The BMC sits between the chip set and the push-buttons in order to support Secure mode front panel lockout, and to provide a mechanism for the BMC to synthesize button presses for controlling system power.

The BMC intercepts signals from the chip set that direct system power-up and power-down under ACPI. These same signals can be driven by the alarm function in the chip set RTC to cause an alarm-based power up.

Regardless of whether the system is using ACPI power management, the BMC still retains the ability to immediately control the system power state via the watchdog timer and IPMB commands.

Wake-on-LAN signals are another source of system power-up

4.14.2   One- and Two-Button Model

The SCB2 baseboard supports both the one-button and two-button models for ACPI power control as a configuration option.

The one-button model uses a single push-button for power on/off and sleep/wake functions. This button is referred to as the power push-button in this document. When the system is powered up (operating) a brief press of the power push-button is interpreted as a sleep request by the operating system. A >4 second press results in a power button override that directs the chip set to immediately power off the system.

The two-button model has a power push-button, which is used to power the system on and to request a power down of the system, and a sleep push-button that is used to wake the system and issue a sleep request. As with the one-button model, a >4 second press of the power push-button causes a power button override. **While a two-button option is generically supported in the BMC firmware, this capability may not be available from the SCB2 baseboard.**

4.14.3   Watchdog Timer Operation under ACPI Sleep

The BMC stops the watchdog timer when the system enters a sleep state. When the system wakes up, system management software must restart the timer to continue watchdog operation.

4.14.4   Fan Control under ACPI

The BMC provides an option for enabling/disabling whether the baseboard fans are turned off when the system is in an ACPI S1-S3 sleep state. The configuration of this option is handled via parameters on the BMC's *Set ACPI Mode* and *Get ACPI Mode Configuration* commands. Refer to the *SCB2 Baseboard Management Controller EPS* for more information.

4.14.5   ACPI Power State Notification

The BMC can be configured to notify other management controllers of the present sleep state of the system. This is accomplished by the BMC sending a *Set ACPI Power State* command via the IPMB. This command is sent to the controllers after the BMC detects a sleep state change. The BMC initialization agent uses SDR Type 12h, Management Controller Device Locator Record, to collect a list of the management controllers that require this notification.

4.14.6   Wake-Up Sources (ACPI and Legacy)

The SCB2 server board is capable of wake up from several sources under a non-ACPI configuration (e.g., when the operating system does not support ACPI). The wake-up sources are defined in the following table. Under ACPI, the operating system programs the CSB5 and SIO to wake up on the desired event, but in Legacy mode, the BIOS enables/disables wake-up sources based on an option in BIOS Setup. It is required that the operating system or a driver will clear any pending wake-up status bits in the associated hardware (such as the Wake-on-LAN status bit in the LAN ASIC, or PCI PME status bit in a PCI device). The legacy wake-up feature is disabled by default.

Table 22. Supported Wake Events

Wake Event	Supported via ACPI (by sleep state)	Supported Via Legacy Wake
Power Button	Always wakes system	Always wakes system
Sleep Button	S1	No
Ring indicate from COMA	S1, S4, S5	Yes
Ring indicate from COMB	S1, S4, S5	Yes
PME from PCI 32/33	S1, S4, S5	Yes
PME from PCI secondary 64/33	S1, S4, S5	No
PME from primary PCI 64/66	S1, S4, S5	Yes
BMC source (i.e. EMP)	Simulated as power button	Simulated as power button
RTC Alarm	S1, S4, S5	Yes
Mouse	S1	No
Keyboard	S1	No
USB	No	No

4.15 Secure Mode Control

The baseboard keyboard controller produces a Secure mode (SECURE_MOD_KB) output signal. BIOS can cause the signal to be asserted or deasserted by sending a command to the keyboard controller. It can also direct the keyboard controller to automatically activate it as part of the keyboard/mouse inactivity security feature.

The BMC includes commands that allow the Front Panel Lockout, Video Blank, and Floppy Write Protect actions to be individually enabled. This includes the ability to separately enable/disable the individual front panel push-buttons. The commands also include a secure mode override capability that allows the actions to be activated independent of the state of the SECURE_MOD_KB signal.

4.15.1   Front Panel Lockout

When the Secure mode signal is asserted, the BMC can be configured to lock-out the Power and Reset push-buttons, preventing system power off or resets via the push-buttons. When the Secure mode signal is deasserted, the BMC unlocks the Power and Reset push-buttons.

4.15.2   Video Blank and Floppy Write Protect

The BMC provides commands that configure individual *Video Blank on Secure Mode* and the *Floppy Write Protect on Secure Mode* options. These options allow on-board video to be blanked and/or the floppy drives connected to the on-board floppy controller to be write protected when the Secure mode signal becomes asserted. When Secure mode becomes deasserted, the BMC re-enables the video and write access to the floppy drives.

4.15.3   Keyboard / Mouse Inactivity Time-out

The BIOS Setup provides options for an inactivity time-out feature as part of its security options. When the keyboard and mouse have both been idle for the specified time-out interval, the keyboard controller will automatically activate the keyboard password and assert the SECURE_MOD_KB signal, causing the front panel Power and Reset push-buttons to be locked out. Depending on how the option is configured, this may also cause the on-board video to be blanked, and floppy drives write protected.

The inactivity time-out interval is configured using BIOS Setup and can be selected as a system configuration option under security. The keyboard password must first be set via the User Password option for these options to be available.

5.   System BIOS

The SCB2 server board contains the following on-board ASICs that will require BIOS support:

- ServerWorks Champion North Bridge 2.0 HE SuperLite (CNB20HE-SL).
- ServerWorks Champion I/O Bridge (CIOB20).
- Server Works Champion South Bridge (CSB5), PCI IDE controller (CSB5), USB controller (CSB5).
- 4-MB flash ROM Intel Flash (1-MB is programmable).
- Embedded video using ATI Rage XL on PCI 33Mhz Bus.
- Keyboard controller, peripheral I/O (floppy, two serial) using National Semiconductor PC87417 Super I/O.
- Dual Channel Adaptec SCSI controller on 64-bit, 66 MHz PCI bus using Adaptec AIC-7899W. (SCSI model only)
- ATA 100 Hardware RAID 1 and 0 using Promise PDC20358 (ATA model only).
- Sahalee BMC server management controller.

5.1.1   System Flash ROM Layout

The flash ROM contains system initialization routines, the BIOS Setup utility, and runtime support routines. The exact layout is subject to change, as determined by Intel. A 16-KB user block is available for user ROM code or custom logos. A 96-KB area is used to store the string database. The flash ROM also contains initialization code for on-board peripherals, like SCSI and video controllers, in compressed form.

The BIOS image contains all of the BIOS components at appropriate locations. The flash memory update utility loads the BIOS image, minus the recovery block to the flash.

5.2   System Configuration and Initialization

This section describes the configuration and initialization of various baseboard sub-systems as implemented on the SCB2 server board.

5.2.1   Memory

The following is a list of memory specifications that the system BIOS supports:

- Only registered 133-MHz SDRAM memory is supported. When populated with more than 4 GB of memory, the memory between 4 GB and 4 GB minus 256 MB is not accessible for use by the OS and may be lost to the user. This area is reserved for BIOS, APIC configuration space, PCI adapter interface, and virtual video memory space. This memory space is also lost if the system is populated with memory configurations between 3.75 GB and 4 GB.

  The system BIOS supports registered DIMMs with CL=3 components. CL=2 components may be used , however, they will only perform at a CL=3 levels.

- The baseboard is hard-wired for 2-way interleave and the system BIOS supports only 2-way interleaving.

- The system BIOS supports only Error Correcting Code (ECC) memory.

- Each bank of memory can have different size DIMMs. Memory timing defaults to the slowest DIMM.

All DIMMs must use an SPD EEPROM or they will not be recognized by BIOS. Mixing vendors of DIMMs will be supported, but is not recommended as the system will default to the slowest speed that will work with all of the vendors.

The SCB2 server BIOS is responsible for configuring and testing the system memory. Configuring system memory involves probing the memory modules for their characteristics and programming the chipset for optimum performance. The BIOS also verifies that the memory subsystem is functional.

When the system comes out of reset, the main memory is not usable. The BIOS has knowledge of the memory subsystem and it knows the type of memory, the number of DIMM sites, and their locations.

5.2.1.1   Memory Sizing and Initialization

During POST, the BIOS tests and sizes memory, and configures the memory controller. The BIOS determines the operational mode of the CNB20HE-SL based on the number of DIMMS installed and the type, size, speed, and memory attributes found on the on-board EEPROM or Serial Presence Detect (SPD) of each DIMM.

The memory system is based on rows. Since the SCB2 server board supports a 2-way interleave, DIMMs must be populated in pairs (i.e., two DIMMs are required to constitute a row). Although DIMMs within a row must be identical, the BIOS supports various DIMM sizes and configurations, allowing the rows of memory to be different. Memory sizing and configuration are guaranteed only for qualified DIMMs approved by Intel.

Refer to the *SDRAM Memory Module EPS* for procedures and restrictions on the addition of memory.

The memory-sizing algorithm determines the size of each row of DIMMs. The BIOS tests extended memory, per the option selected in the BIOS Setup utility. The total amount of configured memory can be found using INT 15h, AH = 88h;[3] INT 15h, function E801h;[4] or INT 15h, function E820h.

Because the system supports upto 6 GB of memory, the BIOS creates a hole just below 4 GB to accommodate the system BIOS flash, APIC memory, and memory mapped I/O located on 32-bit PCI devices. The size of this hole depends upon the number of PCI cards and the memory mapped resources requested by them. It is typically less than 128 MB.

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[3] INT 15h, AH=88h can report a maximum of 64 MB of contiguous memory.

[4] INT 15h, function E801h can report a maximum of 4096 MB of contiguous memory.

5.2.1.2 ECC Initialization

Because only ECC memory is supported, the BIOS is required to initialize all memory locations before using it. The BIOS fills the base memory before base memory testing, and it postpones the initialization of the rest of the memory until prior to the extended memory test. While initializing base memory, the BIOS must cover the SMRAM and shadow area (0c000h – 0fffffh).

Note: The ECC memory initialization cannot be aborted and may result in a noticeable delay, depending on the amount of memory in the system.

5.2.1.3 Memory Test

Memory can be classified as base memory and extended memory. Base memory is defined as the part of memory that is required for early BIOS code. Typically, 8 MB of memory is sufficient for this purpose. Most of the BIOS code and data is stored in a compressed form inside the BIOS flash and is decompressed into the base memory. The base memory must be available before the BIOS can stack or shadow itself. Extended memory is the memory above the top of base memory (8 MB – the total memory size). Extended memory may be contiguous or it may have one or more holes.

The memory test consists of two steps: a base memory test and an extended memory test. The base memory test must be run before video is initialized. The video provides a key visual indication that the system is functional, so enabling the video as early as possible during POST is a priority. It is possible to test the entire memory in one step, but the memory test and initialization can be a time consuming process. Therefore, the BIOS tests only the minimum amount of memory (8 MB) before the video is displayed and it tests the remaining memory after the video is initialized. If an LCD is present, the BIOS can display the status of the base and extended memory tests. In addition, the BIOS displays the status of the extended memory test on the console if diagnostic messages are enabled.

The SCB2 server BIOS implements a 32-bit, fast, enhanced memory test. The code supports page table extensions as defined in the Pentium Pro processor specifications. It is capable of accessing memory above 4 GB and skipping the memory hole. The user can select the coverage for base and extended memory tests by selecting the desired memory test option in the BIOS Setup utility. The BIOS may test every location (extensive), one "interleave width" per KB of memory (sparse), or one "interleave width" per MB of memory (quick), depending on user preference.

The "interleave width" of a memory subsystem depends on the chipset configuration. For 2:1 interleave, the interleave width is 128 bits. The coverage for base memory test and the extended memory test can be controlled independently. By default, the BIOS tests one interleave width per MB of memory for base as well as extended memory. This default was selected to reduce the time spent in POST. The extended memory test can be aborted by pressing the <Space> key anytime during the test.

5.2.1.4   Memory Remapping

During POST memory testing, the detection of single-bit and multi-bit errors in DRAM banks is enabled. If a single-bit error is detected, a single DIMM number will be identified, and if a multiple-bit error is detected, a row of DIMMs will be identified.[5] The BIOS logs all memory errors in to the SEL.

Once an error is detected, the BIOS will reduce the usable memory so that the byte containing the error is no longer accessible. This prevents a single-bit error (SBE) from becoming a multi-bit error (MBE) after the system has booted, and prevents SBEs from being detected and logged each time the failed location(s) are accessed. This is done automatically by the BIOS during POST and does not require user intervention.

Memory remapping may occur during base memory testing or extended memory testing. If remapping occurs during the base memory testing, the SEL event is not logged until after the BIOS remaps the memory and successfully configures and tests 8 MB of memory. In systems where all memory is found to be unusable, only the BIOS beep codes indicate the memory failure. Once the BIOS locates a functioning bank of memory, remapping operations and other memory errors are logged into the SEL and reported to the user at the completion of POST.

5.2.2   Processors

The BIOS determines the processor stepping, cache size, etc. through the CPUID instruction. The requirements are as follows:

- All processors in the system must operate at the same frequency, have the same cache sizes, and the same VID. No mixing of product families supported.

- Processors run at a fixed speed and cannot be programmed to operate at a lower or higher speed.

Note: When the CMOS clear function is enabled, the BIOS defaults the processor frequency to a safe mode at 533 MHz when pre-production unlocked processors are used.

5.2.3   Extended System Configuration Data (ESCD) and Plug and Play (PnP)

The system BIOS supports industry standards for making the system Plug and Play ready:

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[5] The BIOS reduces the memory size if either single-bit or multi-bit errors are detected during memory tests. Since BIOS does not "correct" either error (only reduces memory size to avoid the failing location,) both types of errors are reported as "uncorrectable ECC" errors in the SEL. Note that single-bit errors will be reported as "correctable ECC" errors when found and corrected at "runtime."

5.2.3.1   Resource Allocation

The system BIOS identifies, allocates, and initializes resources in a manner consistent with other Intel servers. The BIOS scans for the following, in order:

1. ISA devices: although add-in ISA devices are not supported on these systems, some standard PC peripherals may require ISA-style resources. Resources for these devices are reserved as needed.

2. Add-in video graphics adapter (VGA) devices: if found, the BIOS initializes and allocates resources to these devices.

3. PCI Devices: the BIOS allocates resources according to the parameters set up by the system setup utility and as required by the *PCI Local Bus Specification*, Revision 2.1.

The system BIOS Power-on Self Test (POST) guarantees that there are no resource conflicts prior to booting the system. Note that PCI device drivers are required to support the sharing of IRQs, which should not be considered a resource conflict. Only four legacy Interrupt Requests (IRQs) are available for use by PCI devices. Therefore, most of the PCI devices share legacy IRQs. In SMP mode, the I/O APICs are used instead of the legacy "8259-style" interrupt controller. There is very little interrupt sharing in SMP mode.

5.2.3.2   PnP ISA Auto-Configuration

The system BIOS does the following:

- Supports relevant portions of the *Plug and Play ISA Specification*, Revision 1.0a and the *Plug and Play BIOS Specification*, Revision 1.0A.
- Assigns I/O, memory, DMA channels, and IRQs from the system resource pool to the embedded PnP Super I/O device.
- Does not support add-in PnP ISA devices.

5.2.3.3   PCI Auto-Configuration

Beginning at the lowest device, the BIOS uses a "depth-first" scan algorithm to enumerate the PCI buses. Each time a bridge device is located, the bus number is incremented and scanning continues on the secondary side of the bridge until all devices are scanned on the current bus.

The BIOS then scans for PCI devices using a "breadth-first" search. All devices on a given bus are scanned from lowest to highest before the next bus number is scanned.

The system BIOS POST maps each device into memory[6] and/or I/O space, and assigns IRQ channels[7] as required. The BIOS programs the PCI-ISA interrupt routing logic in the chipset hardware to steer PCI interrupts to compatible ISA IRQs.

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[6] The BIOS does not support devices behind PCI-to-PCI bridges that require mapping to the first 1 MB of memory space due to PCI architectural limitations (refer to the *PCI-to-PCI Bridge Architecture Specification*).

[7] PCI IRQ assignments may be overridden using the system setup utility.

The BIOS dispatches any option ROM code for PCI devices to the DOS compatibility hole (C0000h to E7FFFh[8]) and transfers control to the entry point. The DOS compatibility hole is a limited resource. Therefore, system configurations with a large number of PCI devices may encounter a shortage of this resource. If the BIOS runs out of option ROM space, some PCI option ROMs are not executed and a POST error is generated. Scanning PCI option ROMs may be controlled on a slot-by-slot basis in the BIOS Setup.

Drivers and/or the OS can detect installed devices and determine resource consumption using the defined PCI, legacy PnP BIOS, and/or ACPI BIOS interface functions.

5.2.4   NVRAM API

The nonvolatile RAM (NVRAM) API and the PCI data records are not supported by system BIOS. The configuration information of the PCI devices is stored in ESCD. The system setup utility can update the ESCD to change the IRQ assigned to a PCI device.

5.2.5   Automatic Detection of Video Adapters

The BIOS detects video adapters in the following order:

1. Offboard PCI.
2. On-board PCI.

The on-board (or off-board) video BIOS is shadowed, starting at address C0000h, and is initialized before memory tests begin in POST. Precedence is always given to off-board devices.

5.2.6   Keyboard/Mouse Configuration

The BIOS will support either a mouse or keyboard in the single PS/2 connector. The BIOS will also support both the keyboard and mouse if a Y-cable is used with the single PS/2 connector. The use of each device is detected during POST and the KBC is programmed accordingly. Hot plugging of mouse and keyboard from the PS/2 connector is not supported by the system and may have unpredictable results.

5.2.6.1   Boot Without Keyboard and/or Mouse

The system can boot with or without a keyboard and/or mouse. Setup does not include an option to disable them. The presence of the keyboard and mouse is detected automatically during POST, and, if present, the keyboard is tested. The BIOS displays the message "Keyboard Detected" if it detects a keyboard during POST and displays the message "Mouse Initialized" if it detects a mouse during POST. The system does not halt for user intervention on errors if either the keyboard or the mouse is not detected.[9]

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[8] Note that the BIOS size may increase, thereby limiting the area used by option ROMs to 0C0000h – 0E0000h.
[9] IRQ 12 is not available for other devices if a mouse is not present.

5.2.7   Floppy Drives

The SCB2 server BIOS supports floppy controllers and floppy drives that are compatible with IBM* XT/AT standards. Most floppy controllers have support for two floppy drives, although such configurations are rare. At a minimum, the SCB2 BIOS supports 1.44 MB and 2.88 MB floppy drives. LS-120 floppy drives are attached to the IDE controller and are covered elsewhere.

The BIOS does not attempt to auto-detect the floppy drive because there is no reliable algorithm for detecting the floppy drive type if no media is installed. The BIOS auto-detects the floppy media if the user specifies the floppy drive type through setup.

See the following table for details on various floppy types supported by each floppy drive. The 1.25/1.2 MB format is primarily used in Japan. 1.25/1.2 MB floppies use the same raw media as the 1.44 MB floppies, but must be read using 3-mode drives. In order to access the 1.25/1.2 MB floppies, the BIOS must change the spindle speed to 360 rpm. Please note that the 1.44 MB media uses spindle speed 300 RPM. The DENSSEL (density select) pin on a 3-mode floppy drive selects the spindle speed. The spindle rotates at 300 RPM when DENSSEL signal is high. The BIOS will set the spindle speed to match the media.

Table 23. Allowed Combinations of Floppy Drive and Floppy Media

Floppy Drive	Floppy Format	Note
1.44 MB (3 mode)	1.25 MB (Toshiba) 1.25 MB (NEC PC98) 1.44 MB	Floppies formatted under 1.25 MB NEC* PC98 format require a special driver. The BIOS has native support for 1.25 MB Toshiba* format.
1.44 MB (ordinary)	1.44 MB	DENSSEL pin is ignored by these floppy drives
2.88 MB (3 mode)	1.25 MB (Toshiba) 1.25 MB (NEC PC98) 1.44 MB 2.88 MB	Floppies formatted under 1.25 MB NEC PC98 format require special driver. The BIOS has native support for 1.25 MB Toshiba format
2.88 MB (ordinary)	1.44 MB 2.88 MB	The DENSSEL pin is ignored by these floppy drives.

The BIOS provides a setup option to disable the floppy controller. In addition, some platforms support the 3-mode floppy BIOS extension specification, revision 1.0. This specification defines a 32-bit protected mode interface that can be invoked from a 32-bit operating system.

Note: The recovery BIOS requires a 1.44 MB media in a 1.44 MB floppy drive or LS-120 drive.

5.2.8   Universal Serial Bus (USB)

The SCB2 server BIOS supports a USB keyboard, mouse, and boot devices. The SCB2 server platforms contain one USB host controller. The host controller includes the root hub and four USB ports. During POST, the BIOS initializes and configures the root hub ports and looks for a keyboard, mouse, boot device, and the USB hub and enables them.

The BIOS implements legacy USB keyboard support. USB legacy support in BIOS translates commands that are sent to the PS/2 devices, into the commands that USB devices can

understand. It also makes the USB keystrokes and the USB mouse movements appear as if they originated from the standard PS/2 devices.

Emulation is transparent to the software. It is accomplished by trapping accesses to the PS/2 keyboard controller port and redirecting them to the appropriate USB device as a USB command. Legacy support is required if the system does not contain a PS/2 keyboard and mouse. BIOS support is not meant to replace a USB driver, but will enable the system to allow the USB driver to control these devices.

The PS/2 keyboard/mouse port is considered the primary connection for these input devices. USB ports are treated as a contingency. Use of legacy USB emulation is not encouraged, because USB legacy support involves many SMIs and slows the POST and OS loader.

Note: The use of Legacy USB requires that 16KB of base memory be used by the system BIOS. Some Linux based applications and loaders may not function unless Legacy USB is disabled in BIOS setup.

5.3   BIOS-Supported Server Management Features

5.3.1   Console Redirection

The BIOS supports redirection of both the video and keyboard via a serial link (Serial 1 or Serial 2). When console redirection is enabled, the local (host server) keyboard input and video output are passed both to the local keyboard and video connections, and to the remote console, via the serial link. The keyboard inputs, from both sources, are valid and video is displayed to both outputs. As an option, the system can be operated without a keyboard or monitor attached to the host system and can run entirely from the remote console. Setup, and any other text-based utilities, can be accessed through console redirection.[10]

5.3.1.1   Operation

When redirecting the console through a modem, as opposed to a null modem cable, the modem needs to be configured with the following:

- Auto-answer (for example, ATS0=2, to answer after two rings).

- Modem reaction to DTR set to return to command state (e.g., AT&D1). Failure to provide this results in the modem either dropping the link when the server reboots (as in AT&D0) or becoming unresponsive to server baud rate changes (as in AT&D2).

- The Setup/System Setup Utility option for handshaking must be set to CTS/RTS + CD for optimum performance. The CD refers to carrier detect.

- If the EMP is sharing the COM port with serial redirection, the handshaking must be set to Xon/Xoff + CD. In selecting this form of handshaking, the server is prevented from sending video updates to a modem that is not connected to a remote modem. If this is not selected, video update data being sent to the modem inhibits many modems from

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[10] BIOS setup operates in a graphics video mode when the Kanji language is selected and when the diagnostic screen is disabled. As a result, BIOS console redirection will not redirect the OEM splash screen, will not redirect Kanji screens to the remote terminal, nor receive Kanji characters from the remote terminal.

answering an incoming call. An EMP option utilizing CD should not be used if a modem is not used and the CD is not connected.

If the BIOS determines that console redirection is enabled, it reads the current baud rate from CMOS and passes this value to the appropriate management controller via the IPMB.

Once console redirection is selected via BIOS Setup or the System Setup Utility, redirection is loaded into memory and is activated during POST. While redirection cannot be removed without rebooting, it can be inhibited and restarted. When inhibited, the serial port is released from redirection and might be used by another application. Restarting reclaims the serial port and continues redirection.

Inhibiting/restarting is accomplished through an INT 16h mechanism. The standard INT 16h (keyboard handler) function ah=05h places a keystroke in the key buffer, as if an actual key has been pressed. Keystrokes buffered in this way are examined by redirection. If a valid command string has been sent, it is executed. The following commands are supported in this fashion:

- Esc-CDZ0 : Inhibit Console Redirection
- Esc-CDZ1 : Restart Console Redirection

To inhibit redirection, the software must call INT 16h, function ah=05h five times to place the five keys in the key buffer. Keystrokes sent to the INT 16h buffers, for purposes of invoking a command, are buffered and should be removed via the normal INT 16h calls. This prevents these keystrokes from being passed to another application.

5.3.1.2   Keystroke Mappings

During console redirection, the remote terminal sends keystrokes to the local server. The remote terminal may be a dumb terminal or a system with a modem running a communication program, such as ProComm*. The local server passes video back over the same link.

For keys that have an ASCII mapping, such as A and Ctrl-A, the remote terminal sends the ASCII character. For keys that do not have an ASCII mapping, such as F1 and Alt-A, the remote must send a string of characters, as defined in the tables below. The strings are based on the American National Standards Institute (ANSI) terminal standard. Since the ANSI terminal standard does not define all keys on the standard 101-key U.S. keyboard, mappings for these keys were created, such as F5 – F12, Page Up, and Page Down.

Alt-key combinations are created by sending the combination ^[} followed by the character to be modified. Once this Alt-key combination is sent, the next keystroke is translated into its Alt-key mapping. In other words, if ^[} is mapped to Shift-F1, then pressing Shift-F1 followed by the letter 'a' would send an Alt-a to the server.

The remote terminal can force a refresh of its video by sending ^[{. Combinations outside of the ANSI mapping and not listed in the table below are not supported.

Table 24. Non-ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
ESC	^[	NS	NS	NS
F1	^[OP	NS	NS	NS
F2	^[OQ	NS	NS	NS
F3	^[OR	NS	NS	NS
F4	^[OS	NS	NS	NS
F5	^[OT	NS	NS	NS
F6	^[OU	NS	NS	NS
F7	^[OV	NS	NS	NS
F8	^[OW	NS	NS	NS
F9	^[OX	NS	NS	NS
F10	^[OY	NS	NS	NS
F11	^[OZ	NS	NS	NS
F12	^[O1	NS	NS	NS
Print Screen	NS	NS	NS	NS
Scroll Lock	NS	NS	NS	NS
Pause	NS	NS	NS	NS
Insert	^[[L	NS	NS	NS
Delete	(7Fh)	NS	NS	NS
Home	^[[H	NS	NS	NS
End	^[[K	NS	NS	NS
Pg Up	^[[M	NS	NS	NS
Pg Down	^[[2J	NS	NS	NS
Up Arrow	^[[A	NS	NS	NS
Down Arrow	^[[B	NS	NS	NS
Right Arrow	^[[C	NS	NS	NS
Left Arrow	^[[D	NS	NS	NS
Tab	(09h)	NS	NS	NS

Note:

NS = Not supported

(xxh) = ASCII character xx

Table 25. ASCII Key Mappings

Key	Normal	Shift	Ctrl	Alt
backspace	(08h)	(08h)	(7Fh)	^[}(08h)
(accent) `	`	(tilde) ~	NS	^[}`
1	1	!	NS	^[}1
2	2	@	NS	^[}2
3	3	#	NS	^[}3
4	4	$	NS	^[}4
5	5	%	NS	^[}5
6	6	^	NS	^[}6
7	7	&	NS	^[}7
8	8	*	NS	^[}8
9	9	(	NS	^[}9
0	0	)	NS	^[}0
(dash) -	-	(under) _	(1Fh)	^[}-
=	=	+	NS	^[}=
a to z	a to z	A to Z	(01h) to (1Ah)	^[}a to ^[}z
[	[	{	(1Bh)	^[}[
]	]	}	(1Dh)	^[}]
\	\	|	(1Ch)	^[}\
(semi-colon) ;	;	(colon) :	NS	^[};
(apostrophe) '	'	(quote) "	NS	^[}'
(comma) ,	,	<	NS	^[},
(period) .	.	>	NS	^[}.
/	/	?	NS	^[}/
(space)	(20h)	(20h)	(20h)	^[}(20h)

Note:

NS = Not supported

(xxh) = ASCII character xx

5.3.1.3   Limitations

Console redirection is a real mode BIOS extension. It does not operate outside of real mode. In addition, console redirection will not function if the OS or a driver, such as EMM386*, takes the processor into protected mode. If an application moves the processor in and out of protected mode, it should inhibit redirection before entering protected mode and restart redirection when it returns to real mode.

Video is redirected by scanning and sending changes in text video memory. Therefore, console redirection is unable to redirect video in graphics mode. Since the BIOS scans the text video memory, an additional limitation exists if the system does not contain a video graphics adapter or a proprietary means of buffering the video memory. The BIOS may not have a method to send changes in text video memory if an application, such as an option ROM, writes directly to video memory.

Keyboard redirection operates through the use of the BIOS INT 16h handler. Software bypassing this handler does not receive redirected keystrokes.

5.3.2   Service Partition Boot

The SCB2 server BIOS supports a service partition boot. The service partition is installed as a separate file system partition on one of the local hard drives. It hosts a DOS based operating system, the system setup utility, and diagnostics agents and tests. The service partition communicates with remote console applications, and it can transfer files between the service partition over LAN, serial port, or a modem.

The BIOS provides setup options to configure the service partition type (the default is 98h), and the option for enabling and disabling the service partition boot. A remote agent can direct the BMC firmware to set the service partition boot request and reboot the system.

Upon rebooting, the system BIOS checks for a service partition boot request. On finding a boot request, the system searches for the service partition type starting from the highest disk number in the scan order. If a service partition is found, the system boots from it. The drive containing the service partition becomes the C: drive.

The drive numbers of all other drives are incremented by one, except for the drive that has a scan order that is higher than the service partition drive. The BIOS can be directed by the user to perform a one-time boot from the service partition. The service partition is serviced once per request. The service partition boot option is disabled upon each boot attempt.

The BIOS considers a service partition boot as a continuation of the BIOS POST. The BIOS does not hide the serial port that is used by console redirection or EMP if it is booting to the service partition. The state of all EMP functionality remains in the same state as in POST. The state of Pre-Boot and Always-Active EMP mode also do not change. The service partition is always scanned for presence, even if service partition booting is inactive.

The BIOS sets the watchdog timer inside BMC while it is attempting to boot from a service partition. This timer is reset upon booting of the service partition by an application. If the system hangs on booting, a reset brings the system out of the service partition boot and an error is logged.

The BIOS starts serial console redirection on a diagnostic boot. Console redirection is turned on with Serial 2, 19200 BAUD. Any reboot after a diagnostic boot reverts to the previous settings of serial console redirection. For example, if console redirection was turned off before the service boot, it reverts to disabled.

5.4   Windows* Compatibility

The SCB2 server board is compliant with the *Hardware Design Guide v3.0*.

The Hardware Design Guide (HDG) for a Windows NT platform is intended for systems that are designed to work with Windows NT class operating systems. Each specification classifies the systems further and has different requirements based on the intended usage for that system. For example, a server system used in small home/office environments has different requirements than one that is used for enterprise applications.

The SCB2 server BIOS meets the applicable requirements as specified in version 3.0 of the HDG specification.

5.4.1   Quiet Boot

Version 3.0, of the Hardware Design Guide for Windows NT, requires that the BIOS provide minimal startup display during BIOS POST. The system start-up must only draw the user's attention in case of errors or when there is a need for user interaction. By default, the system must be configured so the screen display does not display memory counts, device status, etc., but presents a "clean" BIOS start-up. The only screen display allowed is the OEM splash screen, which can include information such as copyright notices.

The SBC2 server BIOS supports the <ESC> and <F2> hot keys during POST, giving the user the ability to temporarily disable the splash screen to view all diagnostic and initialization messages for the current boot. The BIOS displays a message about the hot keys below the splash screen, at the bottom of the display. The splash screen can be disabled for all subsequent boot-up sequences by going into the BIOS Setup utility and disabling the *Quiet Boot* option found under the Boot menu. The *Quiet Boot* option should be disabled when using BIOS console redirection, since it cannot redirect the video if configured for graphics mode.

If the service partition boot is enabled, the BIOS turns off the splash screen for that boot and restores it during subsequent, normal boots. The BIOS may temporarily remove the splash screen when the user is prompted for a password during POST. The BIOS also allows an OEM to override the standard Intel splash screen with a custom one.

The SCB2 BIOS maintains the splash screen during option ROM initialization. Since option ROMs expect the video to be in text mode, the BIOS emulates text mode. The BIOS remembers the INT10 calls made by the option ROMs and displays the option ROM screen if the user presses the <Esc> key. The ROM screen is restored if the BIOS detects any key combination that includes the <Ctrl> or <Alt> key during option the ROM scan. This is because many option ROMs use one of these key combinations to enter setup.

The SCB2 BIOS displays a progress meter at the top of the screen. This meter provides a visual indication of percentage of POST completed. The BIOS measures the amount of time required for completing POST during every boot and uses that information to update the progress meter during the next boot.

Note: If the *Extended Memory Test* option in BIOS Setup is set for "Extensive", the progress meter may stop until the memory test has completed, causing the system to appear to be hung. Once the memory test has completed, the progress meter will continue as POST progresses. Depending on the amount of memory installed, the progress meter may stop anywhere from 15 seconds to several minutes.

5.5   BIOS Serviceabilty Features

5.5.1   CMOS Reset

The Complimentary Metal Oxide Silicon (CMOS) configuration RAM may be reset by one of two methods: the CMOS clear jumper located on the baseboard (J1E1), or the CMOS clear button sequence from the front panel. The CMOS can also be set to a default setting through the BIOS Setup. It will automatically be reset if it becomes corrupted.

Five steps are required to reset the CMOS through the buttons on the front panel:

1. Power the system off, but leave the AC power connected so the 5 V standby is available.
2. Assure that the CMOS clear jumper is in the 'not clear' position.
3. Hold down the Reset button for at least 4 seconds.
4. While the Reset button is still depressed, press the On/Off button.
5. Simultaneously release both the On/Off button and Reset buttons.

Upon completion of these steps, the BMC asserts the clear CMOS signal to emulate the movement of the clear CMOS jumper. The BIOS clears CMOS as if the user had moved the CMOS clear jumper on the baseboard. CMOS is cleared only once per front-panel button sequence. The BMC releases the CMOS clear line during the next system reset. Removing the CMOS clear jumper from the baseboard can disable the front panel CMOS reset function. The jumper should be retained in case the CMOS needs to be cleared using the baseboard header.

When the BIOS detects a reset CMOS request, CMOS defaults are loaded during the next POST sequence. Note that non-volatile storage for embedded devices may or may not be affected by the clear CMOS operation, depending on the available hardware support. The CMOS reset also forces all non-speed locked processors to operate in safe mode.[11] The system must be rebooted without the CMOS clear jumper being in the "clear" position to restore the proper processor speed.

5.5.2   Flash Update Utility

The Flash Memory Update Utility (IFlash) loads a fresh copy of the BIOS into Flash ROM. The loaded code and data include the following:

- On-board video BIOS, SCSI BIOS or ATA-100 BIOS depending on which SCB2 board is used, and other option ROMs for the devices embedded on the motherboard.
- The Setup utility.
- A user-definable Flash area (user binary area).
- A language file.

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[11] Safe mode forces processors to operate at a safe core:bus ratio (generally 2:1 or 4:1, depending on the processor) with cache disabled. Note that speed-locked processors cannot be forced into Safe mode. These processors will continue to operate at their rated frequencies.

When running IFlash in interactive mode, the user may choose to update a particular Flash area. Updating a Flash area reads a file, or a series of files, from a hard or floppy disk, and loads it in the specified area of Flash ROM. In interactive mode, IFlash can display the header information of the selected files.

Note: the IFlash utility must be run without the presence of a 386 protected mode control program, such as Windows* or EMM386*. IFlash uses the processor's flat addressing mode to update the Flash component.

5.5.2.1   Loading the System BIOS

The new BIOS is contained in .BIx files. The number of .BIx files is determined by the size of the BIOS area in the Flash part. The number of files is constrained by the fact that the image and the utilities fit onto a single, 1.44 MB DOS-bootable floppy. These files are named as follows:

- xxxxxxxx.BIO
- xxxxxxxx.BI1
- xxxxxxxx.BI2

The first eight letters of each filename can be any value, but the files cannot be renamed. Each file contains a link to the next file in the sequence. IFlash does a link check before updating to ensure that the process is successful. However, the first file in the list can be renamed, but all subsequent file names must remain unchanged.

Updating the system BIOS overwrites the language files. If a custom language file has been created, it must be flashed in after the system BIOS has been updated. The user binary area is also updated during a system BIOS update. The user binary can be updated independently from the system BIOS. CMOS is not cleared when the system BIOS is updated in normal or recovery mode. Configuration information, like ESCD, is not overwritten during BIOS flash update. The user is prompted to reboot after a BIOS update completes.

5.5.2.2   User Binary Area

The baseboard includes an area in Flash for implementation-specific OEM add-ons. The user binary area can be saved and updated as described above in the *System BIOS* section. For this update, only one file is needed. The valid extension for user files is .USR.

5.5.2.3   BIOS Recovery Mode

If a .BLX image is corrupt, or if an update to the system BIOS is not successful, or if the system fails to complete POST and is unable to boot an operating system, it may be necessary to run the BIOS recovery procedure.

To place the baseboard into recovery mode, move the "Recovery Boot" option jumper, located at jumper block J1F1 on the baseboard, to the recovery position. The BIOS is then able to execute the recovery BIOS (also known as the boot block) instead of the normal BIOS. The recovery BIOS is a self-contained image that exists solely as a fail-safe mechanism for installing a new BIOS image. The recovery BIOS boots from a 1.44 MB floppy diskette, as used

in one of the following devices: a standard 1.44 MB floppy drive, a USB 1.44 MB floppy drive, or an LS-120 removable drive.

Recovery mode requires at least 4 MB of RAM, and drive A: must be set up to support a 3.5 in. 1.44 MB floppy drive. This is the mode of last resort, used only when the main system BIOS will not come up. In recovery mode operation, IFlash (in non-interactive mode only) automatically updates only the main system BIOS. IFlash senses that the platform is in recovery mode and automatically attempts to update the system BIOS.

Note: The BIOS update floppy disk must be bootable. During recovery mode, video will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beeps. Failure is indicated by a long series of short beeps.

5.5.2.4   Performing BIOS Recovery

The follow procedure boots the recovery BIOS and flashes the normal BIOS:

1. Turn off the system power.

2. Move the BIOS Recovery Boot jumper to the recovery state. (J1F1 on the baseboard)

3. Insert a bootable BIOS recovery diskette containing the new BIOS image files.

4. Turn on the system power.

The recovery BIOS boots from the DOS-bootable recovery diskette and emits one beep when it passes control to DOS. DOS then executes a special AUTOEXEC.BAT that contains "IFlash" on the first line. If it is determined that the system is in recovery mode, IFlash will start the flash update without user intervention. IFlash reads the flash image and programs the necessary blocks. It emits one beep to indicate the beginning of the flash operation. After a period of time, the BIOS emits two beeps to indicate that the flash procedure was completed successfully. If the flash procedure fails, the BIOS emits a continuous series of beeps.

When the flash update completes:

1. Turn off the system power.
2. Remove the recovery diskette.
3. Restore the jumper to its original position.
4. Turn on the system power.
5. Re-flash any custom blocks, such as user binary or language blocks.

The system should now boot normally using the updated system BIOS.

5.6   BIOS and System Setup

There are two utilities used to configure BIOS and system resources, the BIOS Setup utility, and the System Setup Utility (SSU). On-board devices are configured with the BIOS Setup utility that is embedded in flash ROM. BIOS Setup provides enough configuration functionality

to boot an OS image or a CD-ROM containing the system setup utility. The system setup utility is used to configure most of the server management features of the baseboard. The system setup utility is released on diskette or CD-ROM. The BIOS Setup utility is always provided in flash for basic system configuration.

The configuration utilities allow the user to modify the CMOS RAM and NVRAM. The actual hardware configuration is accomplished by the BIOS POST routines and the BIOS Plug-N-Play auto-configuration manager. The configuration utilities update a checksum for both areas, so potential data corruption is detected by the BIOS before the hardware configuration is saved. If the data is corrupted, the BIOS requests that the user reconfigure the system and reboot.

5.6.1   BIOS Setup Utility

This section describes the ROM-resident setup utility that provides the means to configure the platform. The BIOS Setup utility is part of the system BIOS and allows limited control over on-board resources. The system setup utility must be used for configuring the on-board devices and add-in cards.

The user can disable embedded PCI devices through the setup menus. When these devices are disabled through setup, their resources are freed.

The following embedded devices can be disabled through setup menus, making them invisible to a Plug-and-Play operating system that scans the PCI bus:

- Embedded SCSI (SCSI version only).
- Embedded video.
- Each Embedded NIC (2).
- Embedded ATA RAID (ATA-100 version only).
- CSB5 USB Controller.

The ROM-resident BIOS Setup utility is only used to configure on-board devices.

The BIOS Setup utility screen is divided into four functional areas. *Table 26* describes each area.

Table 26. Setup Utility Screen

Functional Area	Description
Keyboard Command Bar	Located at the bottom of the screen or as part of the help screen. This bar displays the keyboard commands supported by the setup utility.
Menu Selection Bar	Located at the top of the screen. Displays the various major menu selections available to the user. The Server Setup utility major menus are: Main Menu, Advanced Menu, Security Menu, Server Menu, Boot Menu, and the Exit Menu.
Options Menu	Each Option Menu occupies the left and center sections of the screen. Each menu contains a set of features. Selecting certain features within a major Option Menu drops you into sub-menus.
Item-Specific Help Screen	An item-specific Help screen is located at the right side of the screen .

During the BIOS POST operation, the user is prompted to use the F2 function key to enter setup as follows:

```
Press <F2> to enter Setup
```

A few seconds might pass before the BIOS Setup Utility is entered. This is the result of POST completing test and initialization functions that must be completed before Setup can be entered. When Setup is entered, the Main Menu options page is displayed.

5.6.1.1   Keyboard Command Bar

The bottom portion of the Setup screen provides a list of commands that are used to navigate through the Setup utility. These commands are displayed at all times.

Each menu page contains a number of configurable options and/or informational fields. Depending on the level of security in affect, configurable options may or may not be changed. If an option cannot be changed due to the security level, its selection field is made inaccessible. The Keyboard Command Bar supports the following:

Key	Option	Description
Enter	Execute Command	The Enter key is used to activate sub-menus when the selected feature is a sub-menu, or to display a pick list if a selected option has a value field, or to select a sub-field for multi-valued features like time and date. If a pick list is displayed, the Enter key will undo the pick list, and allow another selection in the parent menu.
ESC	Exit	The ESC key provides a mechanism for backing out of any field. This key will undo the pressing of the Enter key. When the ESC key is pressed while editing any field or selecting features of a menu, the parent menu is re-entered.
		When the ESC key is pressed in any sub-menu, the parent menu is re-entered. When the ESC key is pressed in any major menu, the exit confirmation window is displayed and the user is asked whether changes can be discarded. If "No" is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before ESC was pressed without affecting any existing settings. If "Yes" is selected and the Enter key is pressed, Setup is exited and the BIOS continues with POST.
↑	Select Item	The up arrow is used to select the previous value in a pick list, or the previous options in a menu item's option list. The selected item must then be activated by pressing the Enter key.
↓	Select Item	The down arrow is used to select the next value in a menu item's option list, or a value field's pick list. The selected item must then be activated by pressing the Enter key.
↔	Select Menu	The left and right arrow keys are used to move between the major menu pages. The keys have no affect if a sub-menu or pick list is displayed.
F9	Setup Defaults	Pressing F9 causes the following to appear: <table><tr><td align="center">**Setup Confirmation**</td></tr><tr><td align="center">**Load default configuration now?**</td></tr><tr><td align="center">**[Yes]** **[No]**</td></tr></table> If "Yes" is selected and the Enter key is pressed, all Setup fields are set to their default values. If "No" is selected and the Enter key is pressed, or if the ESC key is pressed, the user is returned to where they were before F9 was pressed without affecting any existing field values

Key	Option	Description
F10	Save and Exit	Pressing F10 causes the following message to appear: <table><tr><td align="center">Setup Confirmation</td></tr><tr><td align="center">Save Configuration changes and exit now?</td></tr><tr><td align="center">[<u>Yes</u>] [No]</td></tr></table> If "Yes" is selected and the Enter key is pressed, all changes are saved and Setup is exited. If "No" is selected and the Enter key is pressed, or the ESC key is pressed, the user is returned to where they were before F10 was pressed without affecting any existing values.

5.6.1.2   Menu Selection Bar

The Menu Selection Bar is located at the top of the screen. It displays the various major menu selections available to the user:

- Main Menu.
- Advanced Menu.
- Security Menu.
- Server Menu.
- Boot Menu.
- Exit Menu.

These and associated sub-menus are described below.

5.6.1.3   Main Menu Selections

The following tables describe the available functions on the top-level menus and on various sub-menus. Default values are highlighted.

Table 27. Main Menu Selections

Feature	Option	Description
System Time	HH:MM:SS	Sets the System Time.
System Date	MM/DD/YYYY	Sets the System Date.
Floppy A	Not Installed **1.44/1.25 MB 3½"** 2.88 MB 3½"	Hidden if not detected.
Hard Disk Pre-delay	**Disabled** 3 seconds 6 seconds 9 seconds 12 seconds 15 seconds 21 seconds 30 seconds	Allows slower spin-up drives to come ready.
Primary IDE Master	Informational: Drive size CD-ROM ATAPI Removable	Also selects sub-menu
Primary IDE Slave	Informational: Drive size CD-ROM ATAPI Removable	Also selects sub-menu
Processor Configuration	N/A	Selects sub-menu
Language	**English (US)** Spanish Italian French German	Selects the language BIOS displays.

Table 28. Primary Master and Slave Adapters Sub-menu Selections

Feature	Option	Description
Type	None **Auto**	Auto allows the system to attempt auto-detection of the drive type. None informs the system to ignore this drive.
CHS format Cylinders	1 to 2048	Number of cylinders on drive. This field is only changeable for Type User. This field is informational only, for Type Auto. This option is viewable only if an IDE HDD is detected.
CHS format Heads	1 to 16	Number of read/write heads on Drive. This field is only available for Type User. This field is informational only, for Type Auto. This option is viewable only if an IDE HDD is detected.

Feature	Option	Description
CHS format Sectors	1 to 64	Number of sectors per track. This field is only available for Type User. This field is informational only, for Type Auto. This option is viewable only if an IDE HDD is detected.
CHS format Maximum Capacity	See description	Computed size of drive from cylinders, heads, and sectors entered. This field is only available for Type User. This field is informational only, for Type Auto. This option is viewable only if an IDE HDD is detected.
LBA Format Total Sectors	Information Only	Total number of sectors on the drive that are addressable in Logical Block Address (LBA) format. This option is viewable only if an IDE HDD is detected.
LBA Format Maximum Capacity	Information Only	Capacity of the drive while using LBA addressing. This value may be higher than the 'Maximum Capacity' above for drives bigger than 8.4 GB. This option is viewable only if an IDE HDD is detected.
LBA Mode Control	**Disabled** Enabled	Disabled by default if no devices are detected, otherwise the setting is auto detected This field is informational only, for Type Auto. Enabling LBA results in LBA to be used in place of cylinders, heads, and sectors.
Multi-Sector Transfer	**Disabled** 2 Sectors 4 Sectors 8 Sectors 16 Sectors	Determines the number of sectors per block for multiple sector transfers. This field is informational only, for Type Auto. Disabled by default if no devices are detected, otherwise the setting is auto detected This option is viewable only if an IDE HDD is detected.
PIO Mode	Informational Only	This field is informational only, for Type Auto.
Ultra DMA	Informational Only	This field is informational only, for Type Auto.

Table 29. Processor Configuration Sub-menu

Feature	Option	Description
Processor Type	Information Only	Displays the type of processor(s) installed
Processor POST Speed	Information Only	Displays the measured processor speed
Processor Retest	**Disabled** Enabled	If enabled, BIOS will clear historical processor status and retest all processors on the next boot.
Processor 1 CPUID	N/A	Reports CPUID for Processor 1.
Processor 1 L2 Cache Size	N/A	Reports L2 Cache Size for Processor 1.
Processor 2 CPUID	N/A	Reports CPUID of Processor 2.
Processor 2 L2 Cache Size	N/A	Reports L2 Cache Size for Processor 2.

5.6.1.4   Advanced Menu Selections

The following tables describe the menu options and associated sub-menus available on the Advanced Menu. Please note that the MPS 1.4/1.1 or LBA/CHS selection is no longer configurable. The BIOS will always build MPS 1.4 tables and will access IDE drives using LBA mode.

Table 30. Advanced Menu Selections

Feature	Option	Description
PCI Configuration	N/A	Selects sub-menu.
Peripheral Configuration	N/A	Selects sub-menu.
Memory Configuration	N/A	Selects sub-menu.
Advanced Chipset Control	N/A	Selects sub-menu. May not be present, if there are no advanced chipset settings under user control.
Reset Configuration Data	**No** Yes	Select 'Yes' if you want to clear the System Configuration Data during next boot. Automatically reset to 'No' in next boot.
Numlock	On **Off**	Sets power on Numlock state.

Table 31. PCI Configuration Sub-menu Selections

Feature	Option	Description
USB Function	N/A	Selects sub-menu
On-board NIC 1	N/A	Selects sub-menu
On-board NIC 2	N/A	Selects sub-menu
On-board SCSI	N/A	Selects sub-menu (viewable on SCSI board only)
Onboard R-IDE	N/A	Selects sub-menu (viewable on ATA-100 board only)
Onboard Video	N/A	Selects sub-menu
PCI Slot 1B ROM	**Enable** Disable	Enables or disables the option ROM for a PCI add-in card installed in this slot

Feature	Option	Description
PCI Slot 2B ROM	**Enable** Disable	Selects sub-menu (viewable when a 3-slot PCI riser is detected)
PCI Slot 3B ROM	**Enable** Disable	Selects sub-menu (viewable when a 3-slot PCI riser is detected)
PCI Slot 1C ROM	**Enable** Disable	Selects sub-menu
PCI Slot 2C ROM	**Enable** Disable	Selects sub-menu (viewable when a 3-slot PCI riser is detected)
PCI Slot 3C ROM	**Enable** Disable	Selects sub-menu (viewable when a 3-slot PCI riser is detected)

Table 32. PCI Configuration, Embedded PCI Devices

Feature	Option	Description
USB Function	Disabled **Enabled**	If disabled, the USB controller is turned off and the device resources are hidden from the system.
On-board NIC 1	Disabled **Enabled**	If disabled, embedded NIC 1 is turned off and the device resourses are hidden from the system.
On-board NIC 1 ROM	**Enabled** Disabled	If enabled, initialize NIC 1 expansion ROM.
On-board NIC 2	Disabled **Enabled**	If disabled, the embedded NIC 2 is turned offand the device resourses are hidden from the system.
On-board NIC 2 ROM	**Enabled** Disabled	If enabled, initialize NIC 2 expansion ROM.
On-board SCSI	Disabled **Enabled**	If disabled, the embedded SCSI device is turned off and the device resourses are hidden from the system. (This option is only present in the SCSI SKU).
On-board SCSI ROM	**Enabled** Disabled	If enabled, initialize embedded SCSI device expansion ROM.
On-board R-IDE	Disabled **Enabled**	If disabled, the embedded R-IDE device is turned off and the device resourses are hidden from the system. (This option is only present in the ATA SKU)
On-board R-IDE ROM	**Enabled** Disabled	If enabled, initialize embedded RIDE device expansion ROM.
On-board Video	**Enable** Disable	If disabled, the on-board video controller is turned off.

Table 33. Peripheral Configuration Sub-menu Selections

Feature	Option	Description
Serial Port 1 Address	Disabled **3F8h** 3E8h 2E8h	Selects the base I/O address for Serial port 1.
Serial Port 1 IRQ	**4** 3	Selects the IRQ for Serial port 1.
Serial Port 2 Address	Disabled **2F8h** 3E8h 2E8h	Selects the base I/O address for Serial port 2.
Serial Port 2 IRQ	4 **3**	Selects the IRQ for Serial port 2.
Diskette Controller	Disabled **Enabled**	If disabled, the diskette controller in the Super I/O is disabled.
Legacy USB support	Disabled Keyboard Only **Auto** Keybrd / Mouse	If disabled, legacy USB support is turned off at the end of the BIOS POST. Note: when enabled, System BIOS requires 16KB of base memory.
Front Panel USB	Disabled **Enabled**	If disabled, the front panel USB ports are inactive.

Table 34. Memory Configuration Menu Selections

Feature	Option	Description
Extended Memory Test	**Disabled** 1 MB 1 KB Every-Location	Selects the size of step to use during extended RAM tests.
Memory Bank #1	Installed Not Installed	Displays the current status of the memory bank.
Memory Bank #2	Installed Not Installed	Displays the current status of the memory bank.
Memory Bank #3	Installed Not Installed	Displays the current status of the memory bank
Memory Retest	**Disabled** Enabled	Causes BIOS to retest all memory on next boot.

Table 35. Advanced Chipset Control Sub-menu Selections

Feature	Option	Description
Wake On Ring	Enable **Disable**	Only controls legacy wake up. Determines the action of the system when the system power is off and the modem is ringing.
Wake On LAN	Enable **Disable**	Only controls legacy wake up. Determines the action of the system when a LAN wake-up event occurs.
Wake On PME	Enable **Disable**	Only controls legacy wake up. Determines the action of the system when a PCI power management enable wake-up event occurs.
Wake on RTC Alarm	Enable **Disable**	Legacy wake only. Determines the action of the system when a RTC alarm wake-up event occurs.

5.6.1.5   Security Menu Selections

Table 36. Security Menu Selections

Feature	Option	Description
User Password is	**Not Installed** Installed	Status only; user cannot modify. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Administrator Password is	**Not IInstalled** Installed	Status only; user cannot modify. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Set Administrative Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clear password jumper on board.
Set User Password	Press Enter	When the Enter key is pressed, the user is prompted for a password; press ESC key to abort. Once set, can be disabled by setting to a null string, or clear password jumper on board.
User Access Level	**Limited** No Access View Only Full	Sets the user accessible settings when a user password is set.
		Note: the following options are only viewable when the "User Password" is set.
Password on Boot	**Disabled** Enabled	If enabled, password entry is required before boot.
Secure Mode Timer	**1 min**, 2 min, 5 min, 10 min, 20 min, 60 min, 120 min	Period of key/PS/2 mouse inactivity specified for Secure mode to activate. A password is required for Secure mode to function. Has no effect unless at least one password is enabled.
Security Hot Key (Ctrl-Alt-)	[Z] **[L]**	Key assigned to invoke the secure mode feature. Cannot be enabled unless at least one password is enabled. Can be disabled by entering a new key followed by a backspace or by entering delete.
Secure Mode Boot	**Disabled** Enabled	System boots in Secure mode. The user must enter a password to unlock the system. Cannot be enabled unless at least one password is enabled.
Video Blanking	**Disabled** Enabled	Blank video when Secure mode is activated. A password is required to unlock the system. This cannot be enabled unless at least one password is enabled. This option is only present if the

Standard

Feature	Option	Description
		system includes an embedded video controller.
Power Switch Inhibit	**Disabled** Enabled	When enabled, the power switch is inoperable.

5.6.1.6   Server Menu Selections

Table 37. Server Menu Selections

Feature	Option	Description
System Management	N/A	Selects sub-menu.
Console Redirection	N/A	Selects sub-menu.
Event Log Configuration	N/A	Selects sub-menu.
Fault Resilient Booting	NA	Selects sub-menu
Service Boot	**Disabled** Enabled	This option will be automatically reset to disabled on the following system boot.
Assert NMI on PERR	**Disabled** Enabled	If enabled, PCI bus parity error (PERR) is enabled and is routed to NMI.
Assert NMI on SERR	**Enabled** Disabled	If enabled, PCI bus system error (SERR) is enabled and is routed to NMI.
After Power Failure	**Last State** Power On Stay Off	Sets the BMC power policy on power loss.
Temperature Sensor	**Disabled,** Enabled	If enabled, and one of the temerature sensors reports an over temperature condition during POST, BIOS will generate an error message and halt the boot process until the error is acknowledged or the system temperature reaches a normal level.
POST Error Pause	**Enabled,** Disabled	If enabled, the system will wait for user intervention on critical POST errors. If disabled, the system will boot with no intervention, if possible.
Platform Event Filtering	**Disabled** Enabled	Triggers for system events inside the baseboard management controller

Table 38. System Management Sub-menu Selections

Feature	Option	Description
Board Part Number	N/A	Information field only.
Board Serial Number	N/A	Information field only.
System Part Number	N/A	Information field only.
System Serial Number	N/A	Information field only.
Chassis Part Number	N/A	Information field only.
Chassis Serial Number	N/A	Information field only.
BIOS Version	N/A	Information field only. Full BIOS revision information.
BMC Firmware Revision	N/A	Information field only.
HSBP Revision	N/A	Information field only; this field is hidden if an Intel hot-swap backplane is not detected.

Table 39. Console Redirection Sub-menu Selections

Feature	Option	Description
Serial Console Redirection	**Disabled** Enabled	When enabled, console redirection uses the I/O port and IRQ specified. Choosing "Disabled" completely disables console redirection.
Serial Port	**COM1 3F8 IRQ4** COM2 2F8 IRQ3	Serial port and IRQ designated for server management features. These values should match those defined for Serial ports A and B.
Baud Rate	9600 **19.2k** 38.4k 115.2k	When console redirection is enabled, use the baud rate specified. When EMP is sharing the COM port as console redirection, the baud rate must be set to 19.2 k to match EMP baud rate, unless auto-baud feature is used.
Flow Control	No flow control **CTS/RTS** XON/XOFF CTS/RTS + CD	No flow control. CTS/RTS = Hardware based flow control. XON/XOFF = Software flow control. CTS/RTS +CD = Hardware based + Carrier Detect flow control. When EMP is sharing the COM port as console redirection, the flow control must be set to CTS/RTS or CTS/RTS+CD depending on whether a modem is used.

Table 40. Event Log Configuration Sub-menu Selections

Feature	Option	Description
Clear All Event Logs	**No** Yes	When 'Yes' is chosen, the BIOS will clear the system event log on the next boot.
Event Logging	Disabled **Enabled**	Enables/disables system event logging.
Critical Event Logging	**Enabled** Disabled	If enabled, BIOS will detect and log events for system critical errors. Critical errors are fatal to system operation. These errors include PERR, SERR, ECC memory errors, and NMI.

Table 41. Fault Resilient Booting

Feature	Option	Description
Late POST timeout	**Disabled** 05 minutes 10 minutes 15 minutes 20 minutes	This controls the time limit for add-in card detection. The system is reset on timeout.
Fault Resilient Booting	**Stay on** Reset Power Off	Controls the policy upon timeout. "Stay On" will take no overt action. "Reset" will force the system to reset. "Power Off" will force the system to power off.
Hard Disk OS Boot Timeout	Disabled 05 minutes 10 minutes 15 minutes 20 minutes	This controls the time limit allowed for booting an OS from a hard disk drive. The action taken upon timeout is determined by the FRB Timer policy setting.

Feature	Option	Description
PXE OS Boot timeout	**Disabled** 05 minutes 10 minutes 15 minutes 20 minutes	This controls the time limit allowed for booting an OS using PCE boot. The action taken on timeout is determined by the FRB timer policy setting.

5.6.1.7   Boot Menu Selections

Boot Menu options allow the user to select the boot device and determine what is displayed to the screen during POST.

Table 42. Boot Menu Selections

Feature	Option	Description
Quiet Boot	Disabled **Enabled**	If enabled, the BIOS will display the OEM logo during POST. This option is hidden if the BIOS does not detect a valid logo in the flash area reserved for this purpose.
Boot Device Priority	N/A	Selects sub-menu.
Hard Drive	N/A	Selects sub-menu.
Removable Devices	N/A	Selects sub-menu.
ATAPI CDROM Drives	N/A	Selects sub-menu.

The following table is an example of a list of devices ordered in a given priority. Items can be re-prioritized by using the up and down arrow keys to select the device, hitting the Enter key to display device options, and selecting the desired device in the specified priority field.

Table 43. Boot Device Priority Selections

Boot Priority	Device	Description
1	Removable Devices	Attempt to boot from a legacy floppy A: or removable media device like LS-120.
2	Hard Drive	Attempt to boot from a hard drive device.
3	ATAPI CD-ROM Drive	Attempt to boot from an ATAPI* CD-ROM drive.
4	(any) SCSI CD-ROM Drive	Attempt to boot from a SCSI CD-ROM containing bootable media. This entry will appear if there is a bootable CDROM that is controlled by a BIOS Boot Specification-compliant SCSI option ROM.
5	IBA 4.0.19 Slot 0003 (NIC 1)	Using onboard NIC1, attempt to boot from a network PXE server using IBA (Intel Boot Agent) 4.0.19
6	IBA 4.0.19 Slot 0004 (NIC 2)	Using onboard NIC2, attempt to boot from a network PXE server using IBA (Intel Boot Agent) 4.0.19

Table 44. Hard Drive Selections

Option	Description
1st Disk Drive (drive identifier string) Other bootable cards Additional entries for each drive that has a PnP header	Specifies the boot sequence from the available boot devices.

Table 45. Removable Devices Selections

Option	Description
1st removable device (Device identifer string)	Specifies the boot order from the available removable boot devices.

Table 46. ATAPI CDROM Drives*

Feature	Description
1st removable device (Device identifer string)	Specifies the boot order from the available ATAPI* CDROM drives.

5.6.1.8   Exit Menu Selections

The following menu options are available on the Exit menu. Use the up and down arrow keys to select an option, then press the Enter key to execute the option.

Table 47. Exit Menu Selections

Option	Description
Exit Saving Changes	Exits after writing all modified setup item values to CMOS.
Exit Discarding Changes	Exits leaving CMOS unmodified. User is prompted if any of the setup fields were modified.
Load Setup Defaults	Loads default values for all setup items.
Load Custom Defaults	Loads values of all setup items from previously saved custom defaults. Hidden if custom defaults are not valid to prevent.
Save Custom Defaults	Stores custom defaults in CMOS.
Discard Changes	Read previous values of all setup items from CMOS.

5.7   BIOS Security Features

The SCB2 server BIOS provides a number of security features. This section describes the security features and operating model.

Note: The SCB2 server board has the ability to boot from a device attached to the USB port, such as a floppy disk, disk drive, or CD-ROM, or Zip* drive, even if it is attached through a hub. *The security model is not supported when booting to a USB device.*

5.7.1   Operating Model

The following table summarizes the operation of security features supported by the SCB2 server BIOS.

Table 48: Security Features Operating Model

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Secure mode	Keyboard Inactivity Timer, Runtime activation of PS/2 keyboard controller hotkey	User Password enabled in Setup	On-board video goes blank (if enabled in Setup). All switches on the front panel except NMI are disabled. No PS/2 mouse or PS/2 keyboard input is accepted. Keyboard LEDs flash.	User Password	Video is restored. Front Panel switches are enabled. Keyboard and mouse inputs are accepted.
Secure boot	Power On/Reset	User Password and Secure Boot Enabled	Prompts for password, if booting from drive A. On-board video is blanked (if enabled in Setup). Enter Secure Mode just before scanning option ROMs. Keyboard LEDs flash, but video blanking and front panel lock is not invoked until OS boot. All the switches on the front panel are disabled except NMI. No input from PS/2 mouse or PS/2 keyboard is accepted; however, the mouse driver is allowed to load before a password is required. If booting from drive A, and the user enters correct password, the system boots normally.	User Password	Floppy writes are re-enabled. Front panel switches are re-enabled. PS/2 Keyboard and PS/2 mouse inputs are accepted. System attempts to boot from drive A. If the user enters correct password, and drive A is bootable, the system boots normally.

Mode	Entry Method/ Event	Entry Criteria	Behavior	Exit Criteria	After Exit
Password on boot	Power On/Reset	User Password set and password on boot enabled and Secure Boot Disabled in Setup	System halts for User Password before scanning option ROMs. The system is not in Secure Mode. No mouse or keyboard input is accepted except the password.	User Password	Front panel switches are re-enabled. PS/2 Keyboard and PS/2 mouse inputs are accepted. The system boots normally. Boot sequence is determined by Setup options.
Fixed disk boot sector	Power On/Reset	Set feature to Write Protect in Setup	Will write protect the master boot record of the IDE hard drives only if the system boots from a floppy. The BIOS will also write protect the boot sector of the drive C: if it is an IDE drive.	Set feature to Normal in Setup	Hard drive will behave normally.

5.7.2   Password Protection

The BIOS uses passwords to prevent unauthorized tampering with the system. Once Secure Mode is entered, access to the system is allowed only after the correct password(s) has been entered. Both the user and administrator passwords are supported by the BIOS. Each password can be independently set or cleared during system configuration using a setup. The maximum length of the password is seven characters. The password cannot have characters other than alphanumeric (a-z, A-Z, 0-9).

Once set, a password can be cleared by changing it to a null string. Entering the user password allows the user to modify the time, date, language, user password, Secure Mode timer, and Secure Mode hot-key Setup fields. Other Setup fields can be modified only if the administrator password is entered. The user password also allows the system to boot if secure boot is enabled. If only one password is set, this password is required to enter Setup. The administrator has control over all fields in the Setup including the ability to clear the user password.

If the user enters three wrong passwords in a row during the boot sequence, the system will be placed into a halt state. This feature makes it difficult to break the password by "trial and error" method.

BIOS Setup may provide an option for setting the EMP password. However, the EMP password is only utilized by the BMC, this password does not effect the BIOS security in any way, nor does the BIOS security engine provide any validation services for this password. EMP security is handled primarily through the BMC and EMP utilities.

5.7.2.1   Administrator/User Passwords and F2 Setup Usage Model

Notes:
- Visible=option string is active and changeable.
- Hidden=option string is inactive and not visible.
- Shaded=option string is gray-out and view-only.

Four scenarios:

- Scenario #1

Admin/Supervisor Password - Not Installed
User Password   - Not Installed
Login Type: N/A
Set Admin/Supervisor Password (visible) Set User Password (visible) User Access Level [Full] [1] (shaded) Clear User Password (hidden) Unattended Start (hidden)

Note: User Access Level option will be full and shaded as long as the administrator /supervisor password is not installed.

- Scenario #2

Admin/Supervisor Password - Installed
User Password   - Installed
Login Type: Admin/Supervisor
Set Admin/Supervisor Password (visible) Set User Password (visible) User Access Level [Full] (visible) Clear User Password (visible) Unattended Start (visible)
Login Type: User
Set Admin/Supervisor Password (hidden) Set User Password (visible) User Access Level [Full] (Shaded) Clear User Password (hidden) Unattended Start (visible)

- Scenario #3

Admin/Supervisor Password - Not Installed User Password   - Installed
Login Type: User
Set Admin/Supervisor Password (visible) Set User Password (visible) User Access Level [Full] [1] (shaded) Clear User Password (hidden) Unattended Start (visible)
Login Type: \<Enter\>
No Access

Notes: User Access Level option will be full and shaded as long as the administrator/supervisor password is not installed.

- Scenario #4

Admin/Supervisor Password - Installed User Password   - Not Installed
Login Type: Supervisor
Set Admin/Supervisor Password (visible) Set User Password (visible) User Access Level [Full] (visible) Clear User Password (hidden) Unattended Start (hidden)
Login Type: \<Enter\>
No Access

5.7.3   Inactivity Timer

If the inactivity timer function is enabled, and no keyboard or mouse actions have occurred for the specified time-out period, the following occurs until the user password is entered:

- PS/2 keyboard and PS/2 mouse input is disabled. PS/2 keyboard lights start blinking.
- On-board video is blanked (if selected in Setup).
- Floppy drive is write protected (if selected in Setup).
- Front panel reset, sleep (if present), and power switches are locked.

If a user password is entered, a time-out period must be specified in Setup.

5.7.4   Hot Key Activation

Rather than having to wait for the inactivity time-out to expire, a hot-key combination allows the user to activate secure mode immediately. The hot-key combination is configured through Setup. The following keys are valid hot keys: Ctrl-Alt L or Z>. Setup will not permit the user to choose any other key as the hot key. Note that the hot key will only work on PS/2 keyboards.

5.7.5   Password Clear Jumper

If the user or administrator password(s) is lost or forgotten, both passwords may be cleared by moving the password clear jumper, located at jumper block J1F1 on the baseboard, into the "clear" position. The BIOS determines if the password clear jumper is in the "clear" position during BIOS POST and clears any passwords if required. The password clear jumper must be restored to its original position before a new password(s) can be set.

5.7.6   Secure Mode (Unattended Start)

Secure Mode refers to a system state where many of the external inputs and outputs are disabled to prevent tempering. These include PS/2 ports, floppy, and on-board video.

5.7.7   Front Panel Lock

The front panel buttons, including power and reset, are always disabled when the system is in secure mode. If the system has a sleep switch, it will also be disabled while the system is in Secure Mode.

5.7.8   Video Blanking

If enabled in Setup, and a monitor is attached to the embedded VGA controller, the video will be blanked upon entering Secure Mode. This feature prevents unauthorized users from viewing the screen while system is in Secure Mode. Video monitors attached to add-in video adapters will not be blanked, regardless of the setting of the video blanking feature.

5.7.9   PS/2 Keyboard And Mouse Lock

Keyboard and/or mouse devices attached to the PS/2 connector are unavailable while the system is in Secure Mode. The keyboard controller will not pass any keystrokes or mouse movements to the system until the correct user password is entered.

Note: as Secure Mode has direct control of the keyboard controller and is able to secure access to the system via the PS/2 connector, the USB ports are not under Secure Mode control. USB ports are still functional when the system is in Secure Mode. It is recommended that all USB ports be "Disabled" in BIOS Setup if a Secure Mode environment is in use.

5.7.10   Secure Boot (Unattended Start)

Secure boot allows the system to boot and run the OS without requiring the user password, even if a user password is set. Secure boot is booting the system while keeping it in Secure Mode. However, until the user password is entered, mouse input, keyboard input, and activation of the enabled Secure Mode features described above are not accepted.

In secure boot mode, if the BIOS detects a floppy diskette in the A: drive at boot time, it displays a message and waits for the user password before booting. After the password is entered, the system can boot from the floppy and Secure Mode is disabled. Any of the Secure Mode triggers will cause the system to return to Secure Mode.

If there is no diskette in drive A, the system will boot from the next boot device and will automatically be placed into Secure Mode. The PS/2 keyboard and mouse are locked before option ROMs are scanned. Video is blanked and the front panel is locked immediately before the OS boots. If secure boot is enabled, the user cannot enter option ROM Setup unless the user password is entered. This prevents entering the configuration utilities in the option ROMs where it is possible to format drives, etc. The on-board video is not blanked until the end of the POST.

5.8   OEM Splash Screen

The SCB2 BIOS supports a splash screen during POST; a 16-KB region of Flash ROM is available to store the OEM logo in compressed format. The BIOS contains the standard Intel logo. This logo could be stored in the same area as the OEM logo or it could be in a separate area. Using the IFlash utility, this region can be updated with OEM-supplied logo image. The OEM logo must fit within 640 X 384 size to accommodate the progress meter at the top and hotkey messages at the bottom of the screen. If the OEM logo is flashed into the system, it will override the built-in Intel logo.

Intel supplies utilities that compress and convert a 16-color bitmap file into a logo file suitable for IFlash. Intel also supplies a blank logo. If the logo area is updated with a blank logo, the system behaves as if there is no logo and it will always display the POST diagnostic screen.

5.9   Localization

The SCB2 server BIOS supports English, Spanish, French, German, and Italian. Intel provides translations for all of the strings in the supported languages. The language can be selected using BIOS Setup. BIOS Setup can detect which languages are included in the language database and present the correct selections to the user

6.   Error Reporting and Handling

This section documents the types of system bus error conditions monitored by the SCB2 board set.

6.1   Error Sources and Types

One of the major requirements of server management is to correctly and consistently handle system errors. System errors, which can be disabled and enabled individually or as a group, can be categorized as follows:

- PCI bus.
- Memory single- and multi-bit errors.
- Sensors.
- Processor internal errors, bus/address errors, thermal trip errors, temperatures and voltages, and GTL voltage levels.
- Errors detected during POST, logged as 'POST errors'.

On the SCB2 platform, general server management sensors are managed by the Sahalee Baseboard Management Controller (BMC).

6.1.1   PCI Bus Errors

The PCI bus defines two error pins, PERR# and SERR#, for reporting PCI parity errors and system errors, respectively. In the case of PERR#, the PCI bus master has the option to retry the offending transaction, or to report it using SERR#. All other PCI-related errors are reported by SERR#. SERR# is routed to NMI if enabled by BIOS.

6.1.2   Processor Failure

The BIOS detects and logs any processor BIST failure. The failed processor can be identified by the first OEM data byte field in the log. For example, if processor 0 fails, the first OEM data byte will be 0. The BIOS depends on the BMC to log the watchdog timer reset event.

If an OS device driver is using the watchdog timer to detect software or hardware failures and that timer expires, an Asynchronous Reset (ASR) is generated, which is equivalent to a hard reset. The POST portion of the BIOS can query the BMC for the watchdog reset event as the system reboots and logs this event in the System Event Log (SEL).

6.1.3   Processor Bus Errors

The HE-SL supports the data integrity features supported by the Pentium Pro bus, including address, request, and response parity. The HE-SL always generates ECC data while it is driving the processor data bus, although the data bus ECC can be disabled or enabled by BIOS. It is enabled by default.

The HE-SL generates MIRQ# on single-bit errors, and generates SALERT# on uncorrectable errors. In addition, the HE-SL can generate BERR# on unrecoverable ECC errors detected on the processor bus. Unrecoverable errors are routed to an NMI by the BIOS.

6.1.4   Single-Bit ECC Error Throttling Prevention

The system detects, corrects, and logs correctable errors as long as these errors occur infrequently, the system should continue to operate without a problem.

Occasionally, correctable errors are caused by a persistent failure of a single component. Although these errors are correctable, continual calls to the error logger can throttle the system, preventing further useful work.

For this reason, the system counts certain types of correctable errors and disables reporting if errors occur too frequently. Error correction remains enabled, but calls to the error handler are disabled. This allows the system to continue running, despite a persistent correctable failure. The BIOS adds an entry to the event log to indicate that logging for that type of error has been disabled. This entry indicates a serious hardware problem that must be repaired at the earliest possible time.

The system BIOS implements this feature for correctable bus errors. If ten errors occur within an hour, the corresponding error handler disables further reporting of that type of error. The BIOS re-enables logging and SMIs the next time the system is rebooted.

6.1.5   Memory Bus Errors

The HE-SL is programmed to generate an SMI on single-bit data errors in the memory array if ECC memory is installed. The HE-SL performs the scrubbing. The SMI handler records the error and the DIMM location to the SEL. Double-bit errors in the memory array are mapped to SMI because the Sahalee BMC cannot determine the location of the bad DIMM.

6.2   Fault Resilient Booting

The SCB2 server management architecture implements Fault Resilient Booting (FRB) levels 1, 2, and 3. FRB allows the system to go ahead and boot even if one of the processors is non-functional (when using SCB2 as a multi-processor system).

- **FRB-1** In a multiprocessor system, the BIOS registers the application processors in the MP table and the ACPI APIC tables. When started by the Boot Strap Processor (BSP), if an Application Processor (AP) fails to complete initialization within a certain time, it is assumed nonfunctional. If the BIOS detects that an AP has failed the Built-In Self Test (BIST) or is nonfunctional, it requests that the BMC disable that processor. The BMC then generates a system reset while disabling the processor; the BIOS will not see the bad processor in the next boot cycle. The failing AP is not listed in the MP table (refer to the *Multi-Processor Specification, Rev. 1.4*), nor in the ACPI APIC tables, and is invisible to the OS. If the BIOS detects that the BSP has failed BIST, it sends a request to the BMC to disable the present processor. If there is no alternate processor available, the BMC beeps the speaker and halts the system. If the BMC can find another processor, BSP ownership is transferred to that processor via a system reset.

- **FRB-2** The second watchdog timer (FRB-2) in the BMC is set for approximately 6 minutes by BIOS and is designed to guarantee that the system completes BIOS POST. The FRB-2 timer is enabled before the FRB-3 timer is disabled to prevent any "unprotected" window of time. Near the end of POST, before the option ROMs are initialized, the BIOS disables the FRB-2 timer in the BMC. If the system contains more

than 1 GB of memory and the user chooses to test every DWORD of memory, the watchdog timer is disabled before the extended memory test starts, because the memory test can take more than 6 minutes under this configuration. If the system hangs during POST, the BIOS does not disable the timer in the BMC, which generates an ASR.

- **FRB-3** The first timer (FRB-3) starts counting down whenever the system comes out of hard reset, which is usually about 5 seconds. If the BSP successfully resets and starts executing, the BIOS disables the FRB-3 timer in the BMC by de-asserting the FRB3_TIMER_HLT* signal (GPIO) and the system continues with the POST. If the timer expires because of the BSP's failure to fetch or execute BIOS code, the BMC resets the system and disables the failed processor. The system continues to change the bootstrap processor until the BIOS POST gets past disabling the FRB-3 timer in the BMC. The BMC generates an audible beep code if it fails to find a good processor. The process of cycling through all the processors is repeated upon system reset or power cycle.

FRB relies on a deterministic BSP assignment mechanism between the processors and the baseboard. That is, for a given population of processors, the user will always know which is the BSP.

6.2.1   FRB Status Flags

The BMC maintains flags that indicate whether the reset source was an FRB-2 watchdog time-out, an FRB-3 time-out, or a non-FRB related watchdog timeout. This allows the BIOS to issue an appropriate notification message to the user during POST. The BMC also maintains flags that indicate which processors have an FRB-3 history and which processors are presently disabled, if any.

Assuming the system can run after the reset, BIOS can read the failure history status and present an error message to the user, as appropriate. The BMC provides a *Re-arm Sensor Events* command that is used for clearing the FRB failure history in the processor sensor after the failed processor has been replaced.

The FRB3 history bits and the present FRB status are available via the IPMB as well as over the system interface.

6.2.2   FRB-3 Retries

The FRB-3 algorithm will continue to run indefinitely, consecutively disabling processors until one of the processors runs long enough through POST to cause the FRB Timer Halt to be asserted. If the algorithm fails on all processors, it continues to cycle through the processors, with one enabled at a time. Once the FRB-3 algorithm has disabled a processor, the system will continue to run with that processor disabled until the FRB-3 history is cleared via (F2) the BIOS Setup Utility.

6.2.3   FRB-3 Processor Disable Sequencing

The SCB2 baseboard electronics ensures that, in a multi-processor configuration and with all processors enabled, Processor 1 will be the BSP.

If none of the processors has a failure history, the BMC will start by disabling Processor 1 on the first FRB-3 time-out. It then sequentially disables the processors until a processor successfully asserts FRB-3_TIMER_HALT.

6.2.4   FRB Log Limits

The BMC will automatically stop logging FRB Events after four (4) sequential FRB time-outs.

6.2.5   General Notes on FRB

The system/BIOS FRB algorithms will always allow one processor to run as the BSP even if all processors have been marked as failed.

Note: The BMC does not execute FRB-3 if it only detects the presence of one processor.

If FRB failures occur when the system is first plugged in, the BMC will only be able to timestamp FRB events with a power-up relative timestamp until a good BSP is found. At this time, BIOS will initialize the BMC Event Time, after which the BMC will be able to provide time-of-day-based timestamps on subsequent events.

6.3   System Fault & Status LEDs

The SCB2 provides system fault/status LEDs in many areas of the board. There are fault LEDs for the memory DIMMs, the fan headers, and processors, and status LEDs for 5-volt stand-by and system state. The BMC includes a *Set Fault Indication* command that allows satellite management controllers, such as a hot-swap controller, to OR in fault indication status, with the status monitored directly by the BMC.

The command includes information that is used to indicate the following:

- The particular source that issued the command (system management software or management controller).

- The fault condition (fan, temperature, drive slot, power supply).

- The fault level (OK, non-critical, critical, non-recoverable, degraded).

The BMC uses the fault condition and level of information to decide the LED state. The most critical state in effect for a given LED determines the LED state.

The default state for the fault LED signals is 'Off'. The default state is restored whenever the BMC is first powered up when 5V standby becomes available, and subsequently whenever the system is soft or hard reset. The default state for drive fault, temperature, and fan fault conditions is restored when the system is powered down. Power Supply Fault status is retained.

The BMC tracks the source of the command. Once a source has set a non-OK status for a given condition, the corresponding fault LED will turn 'On'. For the LED to be off, all sources that have set non-OK status for a condition must set the status to 'OK'. The exception to this is when the fault LEDs are returned to their default condition.

At least *four* individual sources of the *Set Fault Indication* command can be tracked. Sources are not tracked on a per-condition basis. That is, there are not four sources for fan faults, and another four for temperature faults. This tracking is cleared whenever the BMC detects a system soft or hard reset, and whenever the BMC powers down or powers up the system.

The BMC will accept the *Set Fault Indication* command while the system is powered up or powered down.

Satellite management controller devices that use the *Set Fault Indication* command are required to use the command to initialize or set the present state whenever they receive a *Set Event Receiver* command. This command is sent by the BMC after system power up, and on soft and hard resets, as part of the platform management initialization process.

To ensure this state information is received, the satellite management controller should retry the command until it gets a positive response from the BMC.

6.3.1   DIMM LEDs

There is one fault LED for each DIMM slot that is illuminated if the given DIMM has an uncorrectable or multi-bit memory error. The DIMM fault LEDs are labeled with the following reference designators: LED5G1, LED5G2, LED6G1, LED6G2, LED7G1, and LED7G2. These LEDs will maintain the same state across power switch, power down, or loss of AC.

6.3.2   CPU LEDs

There is a fault LED for each processor socket that is illuminated if a given processor has been disabled. They are labeled with the following reference designators LED7K1 and LED8K1. These LEDs will maintain the same state across power switch, power down, or loss of AC.

6.3.3   Fan LED's

There is one fault LED for each fan header that is illuminated if a given fan fails. They are labeled with the following reference designators: LED4K1, LED4K2, LED6K1, LED6K2, LED9K1, and LED9K2. These LEDs will maintain the same state across power switch, power down, or loss of AC.

6.3.4   5VSB Status LED

There is one single-color status LED located next to the IDE legacy connector (LED1K1) used to indicate the presence of 5-volt stand-by when AC power is applied to the system. AC is applied to the system as soon as the AC cord is plugged into the power supply.

6.3.5   System Status LED

The SCB2 has a system status LED on the baseboard (LED3A2) which can be found next to the PORT80 diagnostic LEDs located near the back edge of the baseboard. This LED is tied to the front panel system status LED and should reflect the same system condition. The LED is a multi-colored LED. The following table describes what each state signifies:

Note: At the completion of POST, the system status LED on the baseboard, along with the system status LED located on the front panel, will turn on green and stay on during normal operating conditions. A blinking green light, or an amber light, either solid or blinking, indicates a system fault.

LED	Color	State	Description
System Status [on standby power]	Green	ON	Running / Normal operation
		Blink	Degraded
	Amber	ON	Critical or Non-Recoverable Condition.
		Blink	Non-Critical condition.
	Off	OFF	POST / System Stop.

System Status Indications

Critical Condition

Any critical or non-recoverable threshold crossing associated with the following events:

- Temperature, voltage, or fan critical threshold crossing.
- Power subsystem failure. The BMC asserts this failure whenever it detects a power control fault (i.e., the BMC detects that the system power is remaining on even though the BMC has deasserted the signal to turn off power to the system).
- A hot-swap backplane would use the *Set Fault Indication* command to indicate when one or more of the drive fault status LEDs are asserted on the hot-swap backplane.
- The system is unable to power up due to an incorrectly installed processor(s), or processor incompatibility.
- Satellite controller sends a critical or non-recoverable state, via the *Set Fault Indication* command to the BMC.
- "Critical Event Logging" errors.

Non-Critical Condition

- Temperature, voltage, or fan non-critical threshold crossing.
- Chassis intrusion.
- Satellite controller sends a non-critical state, via the *Set Fault Indication* command, to the BMC.
- *Set Fault Indication* Command.

Degraded Condition

- Non-redundant power supply operation. This only applies when the BMC is configured for a redundant power subsystem. The power unit configuration is configured via OEM SDR records.

- A processor is disabled by FRB or BIOS.

- BIOS has disabled or mapped out some of the system memory.

6.3.6   ID LED

The blue "ID LED", located at the back edge of the baseboard near the speaker, is used to help locate a given platform requiring service when installed in a multi-system rack. The LED is lit when the front panel ID button is pressed, and is turned off when the button is pressed again. A user-defined interface can also be developed to activate the ID LED remotely.

Note: Intel Server Control (ISC) 3.5 does not have the ability to turn on or turn off the ID LED remotely.

6.4   POST Codes, Error Messages, and Error Codes

The BIOS indicates the current testing phase during POST by writing a hex code to I/O location 80h. If errors are encountered during POST, error messages or codes will either be displayed to the video screen, or if an error has occurred prior to video initialization, errors will be reported through a series of audio beep codes. POST errors are logged in to the SEL.

The error codes are defined by Intel and, whenever possible, are backward compatible with error codes used on earlier platforms.

6.4.1   Port-80 Diagnostic LEDs

To help diagnose POST failures, a set of four bi-color diagnostic LEDs is located on the back edge of the baseboard. Each of the four LEDs can have one of four states: off, green, red, or amber.

The LED diagnostics feature consists of a hardware decoder and four dual color LEDs. During POST, the LEDs will display all normal Port80 codes representing the progress of the BIOS POST. Each POST code will be represented by a combination of colors from the four LEDs. The LEDs are in pairs of green and red. The POST codes are broken into two nibbles, an upper and a lower nibble. Each bit in the upper nibble is represented by a red LED, and each bit in the lower nibble is represented by a green LED. If both bits are set in the upper and lower nibble, then both red and green LEDs are lit, resulting in an amber color. Likewise, if both bits are clear, then the red and green LEDs are off.

During the POST process, each LED sequence represents a specific Port-80 POST code. If a system should hang during POST, the diagnostic LEDs will present the last test executed before the hang. When reading the lights, the LEDs should be observed from the back of the system. The most significant bit (MSB) is the first LED on the left, and the least significant bit (LSB) is the last LED on the right.

Note: When comparing a diagnostic LED color string from the baseboard to those listed in the diagnostic LED decoder in the following tables, the LEDs on the baseboard should be referenced when viewed by looking into the system from the back. Reading the LEDs from left to right, the MSB is located on the left.

Table 49. POST Code Table – Port 80h Codes

Post Code	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			LSB	
D0h	R	R	Off	R	NMI is disabled. Start power-on delay. Initialization code checksum verified
D1h	R	R	Off	A	Initialze the DMA controller, perform the keyboard controller BAT test, strat memory refresh, and enter 4GB flat mode
D2h	R	R	G	R	Get start of initializationcode and check BIOS header
D3h	R	R	G	A	Memory sizing
D4h	R	A	Off	R	Test base 512KBB of memory. Retyn to real mode. Execute any OEM patches and set up the stack.
D5h	R	A	Off	A	Pass control to the uncompreesed code in shadow RAM. The initialization code is copied to segment 0 and contril will be transferred to segment 0
D6h	R	A	G	R	Control is in segment 0. Verify the system BIOOS checksum. If the system BIOS checksum is bad, go to checkpoint code E0h.
D7h	R	A	G	A	Pass control to the interface module.
D8h	A	R	Off	R	Decompress the main system BIOS runtime code.
D9h	A	R	Off	A	Pass control to the main system BIOS runtime code.
E0h	R	R	R	Off	Start of recovery BIOS. Initialize interrupt vectors, system timer, DMA controller, and interrupt controller.
E8h	A	R	R	Off	Initialize extra module if present
E9h	A	R	R	G	Initialize floppy controller
EAh	A	R	A	Off	Try to boot to floppy disk
EBh	A	R	A	G	If floppy boot fails, initialize ATAPI hardware
ECh	A	A	R	Off	Try booting from ATAPI CDROM drive
EEh	A	A	A	Off	Jump to boot sector
EFh	A	A	A	G	Disable ATAPI hardware
03h	Off	Off	G	G	The NMI is disabled. Check for a soft reset or a power-on condition. Enable big real mode
05h	Off	G	Off	G	Build the BIOS Stack. Disable USB controller. Disable cache
06h	Off	G	G	Off	Uncompress the POST code module. Pass control to the POST code module
07h	Off	G	G	G	Uncompress various BIOS modules.
08h	G	Off	Off	Off	Verify password checksum.
08h	G	Off	Off	Off	Verify CMOS checksum.
07h	Off	G	G	G	Read microcode updates from BIOS ROM.
07h	Off	G	G	G	Initializing the processors. Set up processor registers. Select least featured processor as the BSP.
0Bh	G	Off	G	G	Hook before the keyboard BAT command is issued.
0Ch	G	G	Off	Off	Keyboard Controller Test: the keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller
0Eh	G	G	G	Off	Init after keyboard test: the keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.

Post Code	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB			**LSB**	
0Fh	G	G	G	G	Write Command Byte 8042: the initialization after the keyboard controller BAT command test is done. The keyboard command byte will be written next.
10h	Off	Off	Off	R	Keyboard Init: the keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands
10h	Off	Off	Off	R	Disable and initialize 8259.
11h	Off	Off	Off	A	Detect configuration mode, such as CMOS clear.
13h	Off	Off	G	A	Chipset initialization before CMOS initialization.
19h	G	Off	Off	A	Init System Timer: the 8254 timer test is over. Starting the memory refresh test next.
1Ah	G	Off	G	R	Check Refresh Toggle: the memory refresh line is toggling. Checking the 15 second on/off time next.
23h	Off	Off	A	G	Setup Interrupt Vectors: reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24h	Off	G	R	Off	Before Vector: configuration is required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin.
25h	Off	G	R	G	Init interrupt Vectors: interrupt vector initialization is done.
F2h	R	R	A	R	Initialize SMM handler. Initialize USB emulation.
F5h	R	A	R	A	Validate NVRAM areas. Restore from backup if corrupted.
12h	Off	Off	G	R	Load defaults in CMOS RAM if bad checksum or CMOS clear jumper is detected.
12h	Off	Off	G	R	Initializing APP CMOS RAM for appliance servers only.
12h	Off	Off	G	R	Check point after CMOS initialized.
27h	Off	G	A	G	Validate date and time in RTC.
F4h	R	A	R	R	Load micro code to all CPUs.
F6h	R	A	A	R	Scan SMBIOS GPNV areas.
15h	Off	G	Off	A	8254 timer test on channel 2.
15h	Off	G	Off	A	Enable 8042.ve
15h	Off	G	Off	A	Keyboard reset.
26h	Off	G	A	Off	Initialize LCD, if supported.
28h	G	Off	R	Off	Set Video Mode: initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
29h	G	Off	R	G	Debugger hook.
2Ah	G	Off	A	Off	Init PCI devices and motherboard devices. Pass control to video BIOS. Start serial console redirection.
2Bh	G	Off	A	G	Platform hook.
2Dh	G	G	R	G	Initialize AMI display manager module. Initialize support code for headless system if no video controller is detected.
2Dh	G	G	R	G	Scan flash for logos and Initialize logo data areas.
30h	Off	Off	R	R	Detect PS/2 mouse.
30h	Off	Off	R	R	Hook after c000 ROM control.
2Eh	R	R	A	Off	Set up video parameters in BIOS data area.
37h	Off	G	A	A	Activate ADM: the display mode is set. Displaying the power-on message next.
37h	Off	G	A	A	Initialize language module. Display splash logo.
37h	Off	G	A	A	Display Sign-On Message, BIOS ID and processor information.
38h	G	Off	R	R	Detect USB mouse: initializing the bus input, and general devices next, if present.
34h	Off	G	R	R	Reset IDE controllers.
39h	G	Off	R	A	Displaying bus initialization error messages.

Post Code	Diagnostic LED Decoder				Description
	G=Green, R=Red, A=Amber				
	MSB			LSB	
3Ah	G	Off	A	R	Display Setup Message: the new cursor position has been read and saved. Displaying the hit setup message next.
40h	Off	R	Off	Off	Ensure timer keyboard interrupts are on.
4Bh	G	R	G	G	Memory Test: the amount of memory above 8 MB has been found and verified. Checking for a soft reset and clearing the memory below 8 MB for the soft reset next. If this is a power-on situation, going to checkpoint 4Eh next.
57h	Off	A	G	A	Chipset hook after memory size.
53h	Off	R	A	A	Display processor cache size.
54h	Off	A	Off	R	Disable parity and NMI reporting.
60h	Off	R	R	Off	Test 8237 DMA Controller: the DMA page register test passed. Performing the DMA Controller 1 base register test next.
65h	Off	A	R	G	Init 8237 DMA Controller: the DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
7Fh	G	A	A	A	Extended NMI Enable: extended NMI source enabling is in progress.
80h	R	Off	Off	Off	Enable Mouse and Keyboard: the keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81h	R	Off	Off	G	Keyboard Interface Test: a keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82h	R	Off	G	Off	Check Stuck Key Enable Keyboard: the keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83h	R	Off	G	G	Disable Parity NMI: the command byte was written and global data initialization has completed. Checking for a locked key next
84h	R	G	Off	Off	Verify RAM Size: checking for a memory size mismatch with CMOS RAM data next
84h	R	G	Off	Off	Check ATA cable type presence of ATAPI devices.
84h	R	G	Off	Off	Display keyboard message.
16h	Off	G	G	R	Display IDE mass storage devices.
17h	Off	G	G	A	Display USB mass storage devices.
85h	R	G	Off	G	Report the first set of POST errors to error manager.
86h	R	G	G	Off	Boot Password Check: the password was checked. Performing any required programming before Setup next.
8Dh	A	G	Off	G	OEM Patch 9.
8Dh	A	G	Off	G	Set Printer RS-232 timeout
8Dh	A	G	Off	G	Init FDD Devices: resetting the hard disk controller next.
95h	R	G	Off	A	Lock out PS/2 keyboard/mouse if unattended start is enabled.
92h	R	Off	G	R	Option ROM scan.
98h	A	Off	Off	R	Init Boot Devices: the adapter ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
9Bh	A	Off	G	A	Float Processor Initialize: performing any required initialization before the coprocessor test next.
9Eh	A	G	G	R	Enable Interrupts 0,1,2: checking the extended keyboard, keyboard ID, and NUM Lock key next. Issuing the keyboard ID command next.
A2h	R	Off	A	Off	Report second set of POST errors to error messenger.
86h	R	G	G	Off	Prepare And Run Setup: error manager displays and logs POST errors. Waits for user input for certain errors. Execute setup.
8Bh	A	Off	G	G	Set base expansion memory size.
8Ch	A	G	Off	Off	Adjust Setup: programming the Setup options next.
A5h	R	G	R	G	Set display mode.
A7h	R	G	A	G	OEM Patch 12.

Post Code	Diagnostic LED Decoder				Description
	G=Green, R=Red, A=Amber				
	MSB			**LSB**	
A7h	R	G	A	G	Build SMBIOS table and MP tables.
A7h	R	G	A	G	Program hot key and timeout settings in keyboard controller.
A7h	R	G	A	G	Processor initialization before boot.
A7h	R	G	A	G	Copy required language strings to shadow RAM.
AAh	A	Off	A	Off	Clear video screen.
000h	Off	Off	Off	Off	One beep to indicate end of POST. No beep if silent boot is enabled.
000h	Off	Off	Off	Off	POST completed. Passing control to INT 19h boot loader next.

6.4.2   POST Error Codes and Messages

During POST, if an error is detected, the BIOS will display an error code and message to the screen. The following table defines POST error codes and their associated messages. The BIOS prompts the user to press a key in case of serious errors. Some of the error messages are preceded by the string "Error" to highlight the fact that the system may be malfunctioning. All POST errors and warnings are logged in the System Event Log (SEL).

Note: all POST errors are logged to the SEL. The SEL is capable of holding over 400 entries. Once the SEL is full, no further errors will be logged.

Table 50. Standard POST Error Messages and Codes

Error Code	Error Message	Pause on Boot
100	Timer Channel 2 Error	Yes
101	Master Interrupt Controller	Yes
102	Slave Interrupt Controller	Yes
103	CMOS Battery Failure	Yes
104	CMOS Options not Set	Yes
105	CMOS Checksum Failure	Yes
106	CMOS Display Error	Yes
107	Insert Key Pressed	Yes
108	Keyboard Locked Message	Yes
109	Keyboard Stuck Key	Yes
10A	Keyboard Interface Error	Yes
10B	Sytstem Memory Size Error	Yes
10E	External Cache Failure	Yes
110	Floppy Controller Error	Yes
111	Floppy A: Error	Yes
112	Floppy B: Error	Yes
113	Hard disk 0 Error	Yes
114	Hard disk 1 Error	Yes
115	Hard disk 2 Error	Yes
116	Hard disk 3 Error	Yes
117	CD-ROM disk 0 Error	Yes
118	CD-ROM disk 1 Error	Yes
119	CD-ROM disk 2 Error	Yes
11A	CD-ROM disk 3 error	Yes
11B	Date/Time not set	Yes
11E	Cache memory bad	Yes
120	CMOS clear	Yes
121	Password clear	Yes
140	PCI Error	Yes
141	PCI Memory Allocation Error	Yes
142	PCI IO Allocation Error	Yes
143	PCI IRQ Allocation Error	Yes
144	Shadow of PCI ROM Failed	Yes
145	PCI ROM not found	Yes
146	Insufficient Memory to Shadow PCI ROM	Yes

Table 51. Extended POST Error Messages and Codes

Error Code	Error Message	Pause on Boot
8100	Processor 1 failed BIST	No
8101	Processor 2 failed BIST	No
8110	Processor 1 Internal error (IERR)	No
8111	Processor 2 Internal error (IERR)	No
8120	Processor 1 Thermal Trip error	No
8121	Processor 2 Thermal Trip error	No
8130	Processor 1 disabled	No
8131	Processor 2 disabled	No
8140	Processor 1 failed FRB-3 timer	No
8141	Processor 2 failed FRB-3 timer	No
8150	Processor 1 failed initialization on last boot.	No
8151	Processor 2 failed initialization on last boot.	No
8160	Processor 01: unable to apply BIOS update	Yes
8161	Processor 02: unable to apply BIOS update	Yes
8170	Processor P1 :L2 cache Failed	Yes
8171	Processor P2 :L2 cache Failed	Yes
8180	Bios does not support current stepping for Processor P1	Yes
8181	Bios does not support current stepping for Processor P2	Yes
8190	Watchdog Timer failed on last boot	No
8191	4:1 Core to bus ratio: Processor Cache disabled	Yes
8192	L2 Cache size mismatch	Yes
8193	CPUID, Processor Stepping are different	Yes
8194	CPUID, Processor Family are different	Yes
8195	Front Side Bus Speed mismatch. System Halted	Yes, Halt
8196	Processor Model are different	Yes
8197	Cpu Speed mismatch	Yes
8300	Baseboard Management Controller failed to function	Yes
8301	Front Panel Controller failed to Function	Yes
8305	Hotswap Controller failed to Function	Yes
8420	Intelligent System Monitoring Chassis Opened	Yes
84F1	Intelligent System Monitoring Forced Shutdown	Yes
84F2	Server Management Interface Failed	Yes
84F3	BMC in Update Mode	Yes
84F4	Sensor Data Record Empty	Yes
84FF	System Event Log Full	Yes

6.4.3   POST Error Beep Codes

During POST, before the BIOS initializes the onboard video, all post code errors will generate an audible beep code. Once BIOS initializes the onboard video, all POST code errors will be displayed to the monitor. The following tables lists all POST error beep codes.

Table 52. BMC Generated POST Beep Codes

Code	Description
1-5-1-1	FRB failure (processor failure)
1-5-2-1	Empty Processor
1-5-2-2	No Processor
1-5-4-2	Power fault: DC power unexpectedly lost (power control failures)
1-5-4-3	Chipset control failure
1-5-4-4	Power control failure

Table 53. BIOS Generated POST Error Beep Codes

Beeps	Error message	Description
1	Refresh timer failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity error	Parity can not be reset.
3	Base memory failure	Base memory test failure. See *Table 54. POST Memory Error 3-Beep Codes* for additional error details.
4	System timer	System timer is not operational.
5	Processor failure	Processor failure detected.
6	Keyboard controller Gate A20 failure	The keyboard controller may be bad. The BIOS cannot switch to protected mode.
7	Processor exception interrupt error	The CPU generated an exception interrupt.
8	Display memory read/write error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM checksum error	System BIOS ROM checksum error.
10	Shutdown register error	Shutdown CMOS register read/write error detected.
11	Invalid BIOS	General BIOS ROM error.

Table 54. POST Memory Error 3-Beep Codes

Beep Code	Debug port 80h error indicators	Diagnostic LED Decoder				Meanings
		G=Green, R=Red, A=Amber				
		Hi			Low	
3	00h	Off	Off	Off	Off	No memory was found in the system.
3	01h	Off	Off	Off	G	Memory mixed type detected.
3	02h	Off	Off	G	Off	EDO is not supported.
3	03h	Off	Off	G	G	First row memory test failure.
3	04h	Off	G	Off	Off	Mismatched DIMMs in a row.
3	05h	Off	G	Off	G	Base memory test failure.
3	06h	Off	G	G	Off	Failure on decompressing post module.

Beep Code	Debug port 80h error indicators	Diagnostic LED Decoder				Meanings
		G=Green, R=Red, A=Amber				
		Hi			Low	
3	07h-0Dh	Off	G	G	G	Generic memory error.
		G	Off	Off	Off	
		G	Off	Off	G	
		G	Off	G	Off	
		G	Off	G	G	
		G	G	Off	Off	
		G	G	Off	G	
3	0Eh	G	G	G	Off	SMBUS protocol error.
3	0F-FFh	All other combinations				Generic memory error.

6.4.3.1   BIOS Recovery Beep Codes

In rare cases, when the system BIOS has been corrupted, a BIOS recovery process must be followed to restore system operability. During recovery mode, the video controller will not be initialized. One high-pitched beep announces the start of the recovery process. The entire process takes two to four minutes. A successful update ends with two high-pitched beeps. In the event of a failure, two short beeps are generated and a flash code sequence of 0E9h, 0EAh, 0EBh, 0ECh, and 0EFh on the Port 80 diagnostic LEDs.

Table 55. BIOS Recovery Beep Codes

Beeps	Error message	IA32 port 80h indicators	Description
1	Recovery started		Start recovery process.
2	Recovery boot error	Flashing series of post codes: E9h, EAh, EBh, ECh, Efh	Unable to boot to floppy, ATAPI, or ATAPI CDROM. Recovery process will retry.
Series of long low-pitched single beeps	Recovery failed	Eeh	Unable to process valid BIOS recovery images. BIOS already passed control to OS and flash utility.
2 long high-pitched beeps	Recovery complete	Eeh	BIOS recovery succeeded, ready for power-down, reboot.

6.5   "POST Error Pause" option

In case of a POST error, BIOS will stop and wait for the user to press an appropriate key before booting the OS or entering BIOS Setup. The user can override this option by setting "POST Error Pause" to "Disabled" in the BIOS Setup server menu page. If the "POST Error Pause" option is selected to "Disabled", the system will boot the OS without user intervention. Option default value is set to "enabled".

7.   SCB2 Connectors and Jumper Blocks

7.1   Main Power Connector

The main power supply connection is obtained using the 24-pin connector. The following table defines the pin-outs of the connector.

Table 56. Power Connector Pin-out (J2K1)

Pin	Signal	Color	Pin	Signal	Color
1	+3.3Vdc	Orange	13	+3.3Vdc	Orange
2	+3.3Vdc	Orange	14	-12Vdc	Blue
3	COM	Black	15	COM	Black
4	+5Vdc	Red	16	PS_ON#	Green
5	COM	Black	17	COM	Black
6	+5Vdc	Red	18	COM	Black
7	COM	Black	19	COM	Black
8	PWR_OK	Gray	20	RSVD_(-5V)	White
9	5VSB	Purple	21	+5Vdc	Red
10	+12Vdc	Yellow	22	+5Vdc	Red
11	+12Vdc	Yellow	23	+5Vdc	Red
12	+3.3Vdc	Orange	24	COM	Black

Table 57. Power Supply Signal Connector (J1K1)

Pin	Signal	Color
1	5VSB_SCL	Green
2	5VSB_SDA	Yellow
3	PS_ALTER_L, Not used	Red
4	3.3V SENSE-	Black
5	3.3V SENSE+	Orange

7.2   PCI I/O Riser Slot Connector

There are two peer 64-bit, 66-MHz PCI buses implemented through the two separate I/O Riser slots. The first PCI segment, P64-B, supports full length, full height PCI cards. The PCI cards must meet the PCI specification for height, inclusive of cable connections and memory. The second PCI segment, P64-C, supports low-profile PCI cards. The I/O riser slot pin-outs are detailed in the following two tables.

Table 58. P64-B 5V 64-bit/66 MHz Full Length PCI Riser Slot Pin-out

Pin	Side B	Side A	Pin	Side B	Side A
1	-12 V	TRST#	49	M66EN	AD[09]
2	REQ1#	+12 V	50	**Connector Key**	**Connector Key**
3	Ground	TMS	51	**Connector Key**	**Connector Key**
4	GNT1#	TDI	52	AD[08]	C/BE[0]#
5	+5 V	+5 V	53	AD[07]	+3.3 V
6	+5 V	INTA#	54	+3.3 V	AD[06]
7	INTB#	INTC#	55	AD[05]	AD[04]
8	INTD#	+5 V	56	AD[03]	Ground
9	PRSNT1#	REQ3#	57	Ground	AD[02]
10	GNT2#	+5 V (I/O)	58	AD[01]	AD[00]
11	PRSNT2#	GNT3#	59	+5 V (I/O)	+5 V (I/O)
12	Z-spare	Ground	60	ACK64#	REQ64#
13	Ground	Z-i960RST#	61	+5 V	+5 V
14	REQ2#	3.3 V AUX	62	+5 V	+5 V
15	Ground	RST#		**Connector Key**	**Connector Key**
16	CLK	+5 V (I/O)		**Connector Key**	**Connector Key**
17	Ground	GNT#	63	Clock Slot2	Ground
18	REQ#	Ground	64	Ground	C/BE[7]#
19	+5 V (I/O)	PME#	65	C/BE[6]#	C/BE[5]#
20	AD[31]	AD[30]	66	C/BE[4]#	+5 V (I/O)
21	AD[29]	+3.3 V	67	Ground	PAR64
22	Ground	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Ground
24	AD[25]	Ground	70	+5 V (I/O)	AD[60]
25	+3.3 V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]#	IDSEL	72	AD[57]	Ground
27	AD[23]	+3.3 V	73	Ground	AD[56]
28	Ground	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	+5 V (I/O)
30	AD[19]	Ground	76	Ground	AD[52]
31	+3.3 V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Ground
33	C/BE[2]#	+3.3V	79	+5V (I/O)	AD[48]
34	Ground	FRAME#	80	AD[47]	AD[46]

Pin	Side B	Side A	Pin	Side B	Side A
35	IRDY#	Ground	81	AD[45]	Ground
36	+3.3 V	TRDY#	82	Ground	AD[44]
37	DEVSEL#	Ground	83	AD[43]	AD[42]
38	Ground	STOP#	84	AD[41]	+5 V (I/O)
39	LOCK#	+3.3 V	85	Ground	AD[40]
40	PERR#	SMBUS SCL	86	AD[39]	AD[38]
41	+3.3 V	SMBUS SDA	87	AD[37]	Ground
42	SERR#	Ground	88	+5V (I/O)	AD[36]
43	+3.3 V	PAR	89	AD[35]	AD[34]
44	C/BE[1]#	AD[15]	90	AD[33]	Ground
45	AD[14]	+3.3 V	91	Ground	AD[32]
46	Ground	AD[13]	92	Clock Slot 3	ZGNT#
47	AD[12]	AD[11]	93	ZREQ#	Z-SCSI INTB#
48	AD[10]	Ground	94	Z-SCSI INTA#	Clock ZION

Table 59. P64-C 3.3V 64-bit/ (66/33) MHz Low-Profile Riser Slot Pin-out

Pin	Side B	Side A	Pin	Side B	Side A
1	-12 V	TRST#	49	M66EN	AD[09]
2	REQ1#	+12 V	50	**Connector Key**	**Connector Key**
3	Ground	TMS	51	**Connector Key**	**Connector Key**
4	GNT1#	TDI	52	AD[08]	C/BE[0]#
5	+5 V	+5 V	53	AD[07]	+3.3 V
6	+5 V	INTA#	54	+3.3V	AD[06]
7	INTB#	INTC#	55	AD[05]	AD[04]
8	INTD#	+5 V	56	AD[03]	Ground
9	PRSNT1#	REQ3#	57	Ground	AD[02]
10	GNT2#	+5 V (I/O)	58	AD[01]	AD[00]
11	PRSNT2#	GNT3#	59	+5 V (I/O)	+5 V (I/O)
12	Ground	Ground	60	ACK64#	REQ64#
13	Ground	Ground	61	+5 V	+5 V
14	REQ2#	NC **	62	+5 V	+5 V
15	Ground	RST#		**Connector Key**	**Connector Key**
16	CLK	+5 V (I/O)		**Connector Key**	**Connector Key**
17	Ground	GNT#	63	Clock Slot2	Ground
18	REQ#	Ground	64	Ground	C/BE[7]#
19	+5 V (I/O)	PME#	65	C/BE[6]#	C/BE[5]#
20	AD[31]	AD[30]	66	C/BE[4]#	+5 V (I/O)
21	AD[29]	+3.3V	67	Ground	PAR64
22	Ground	AD[28]	68	AD[63]	AD[62]
23	AD[27]	AD[26]	69	AD[61]	Ground
24	AD[25]	Ground	70	+5 V (I/O)	AD[60]
25	+3.3 V	AD[24]	71	AD[59]	AD[58]
26	C/BE[3]#	IDSEL	72	AD[57]	Ground
27	AD[23]	+3.3 V	73	Ground	AD[56]

Pin	Side B	Side A	Pin	Side B	Side A
28	Ground	AD[22]	74	AD[55]	AD[54]
29	AD[21]	AD[20]	75	AD[53]	+5 V (I/O)
30	AD[19]	Ground	76	Ground	AD[52]
31	+3.3 V	AD[18]	77	AD[51]	AD[50]
32	AD[17]	AD[16]	78	AD[49]	Ground
33	C/BE[2]#	+3.3 V	79	+5 V (I/O)	AD[48]
34	Ground	FRAME#	80	AD[47]	AD[46]
35	IRDY#	Ground	81	AD[45]	Ground
36	+3.3 V	TRDY#	82	Ground	AD[44]
37	DEVSEL#	Ground	83	AD[43]	AD[42]
38	Ground	STOP#	84	AD[41]	+5 V (I/O)
39	LOCK#	+3.3 V	85	Ground	AD[40]
40	PERR#	SMBUS SCL	86	AD[39]	AD[38]
41	+3.3 V	SMBUS SDA	87	AD[37]	Ground
42	SERR#	Ground	88	+5 V (I/O)	AD[36]
43	+3.3 V	PAR	89	AD[35]	AD[34]
44	C/BE[1]#	AD[15]	90	AD[33]	Ground
45	AD[14]	+3.3 V	91	Ground	AD[32]
46	Ground	AD[13]	92	Clock Slot 3	Reserved
47	AD[12]	AD[11]	93	Reserved	Ground
48	AD[10]	Ground	94	Ground	Reserved

**Note: 3.3V Aux is not available on the low profile PCI riser slot. This means that you can not put a card that will wake the system from an S4 or S5 state in the low profile slot.

7.3 System Management Headers

7.3.1   ICMB Header

Table 60. ICMB Header Pin-out (J9B1)

Pin	Signal Name	Type	Description
1	5 V standby	Power	+5 V Standby
2	Transmit	Signal	UART signals
3	Transmit Enable	Signal	UART signals
4	Receive	Signal	UART signals
5	Ground	GND	

7.3.2   OEM IPMB Header

Table 61. IPMB Header Pin-out (J9D1)

Pin	Signal Name	Description
1	Local I2C SDA	BMC IMB 5 V Standby Clock Line
2	GND	
3	Local I2C SCL	BMC IMB 5 V Standby Data Line

7.3.3   SCSI IPMB Header

Table 62. IPMI Header Pin-out (J1H1)

Pin	Signal Name	Description
1	5VSB SDA	Data Line
2	GND	
3	5VSB SCL	Clock Line
4	Not used	

7.4   Front Panel Connectors

A high density, 33-pin header (J1J2) and an SSI standard 24-pin header (J1G1) are provided to support a system front panel. The headers contain reset, NMI, power control buttons, and LED indicators. In addition, the high-density header provides an optional serial interface to provide a COM2 interface to the front panel. The following tables detail the pin outs of the headers.

Table 63. High-Density Front Panel 34-Pin Header Pin Out (J1J2)

Pin	Signal Name	Pin	Signal Name
1	GND	2	FP_SYS_FLT_LED_R_L
3	FP_PWR_LED_R_L	4	FP_SYS_FLT_LED2_R_L
5	HDD_LED 5V-Anode	6	5VSB_Power
7	HDD_LED_ACT_R_L	8	FP_ID_LED_R_L
9	FP_PWR_BTN_L	10	NIC1_LED_3.3V -(LINK)
11	HDD_LED_FAULT_ON#	12	NIC1_LED_ON - (Activity)
13	RST_SW_Active#	14	I2C Data
15	GND	16	I2C Clk
17	FP_ID_BTN_L	18	Chassis Intrusion
19	GND	20	NIC2_LED_3.3V -(LINK)
21	Key	22	Key
23	NMI_SW_Active	24	NIC2_LED_ON - (Activity)
25	EMP_DSR2	26	EMP_INUSE_L
27	EMP_SIN2	28	EMP_SOUT2
29	EMP_RTS2	30	EMP_CTS2
31	EMP_DTR2	32	EMP_DCD2
33	Unused	34	Unused

Table 64. 34-pin Front Panel Connector signal descriptions

Signal	Type [1]	Description
SPKR_FP	Out	SPEAKER DATA for the front panel/chassis mounted speaker.
GROUND	ground	GROUND is the power supply ground.
CHASSIS_INTRUSION	In	CHASSIS INTRUSION is connected to the BMC and indicates that the chassis has been opened. CHASSIS_INTRUSION is pulled high to +5 V standby on the baseboard.
FP_HD_ACT*	Out	HARD DRIVE ACTIVITY indicates there is activity on one of the hard disk controllers in the system.
+5V	Power	+5 V is the 5-volt power supply.
FP_SLP_BTN*	In	FRONT PANEL SLEEP is connected to the BMC and causes the system to be put to sleep if supported by the operating system. FP_SLP_BTN* is pulled high to +5 V on the baseboard and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front.
COOL_FLT_LED*	Out	COOLING FAULT LED indicates that either a fan failure has occurred or the system is approaching an over-temperature situation. COOL_FLT_LED* is an output of the BMC.
PWR_LED*	Out	POWER PRESENT LED.

Signal	Type [1]	Description
PWR_FLT_LED*	Out	SYSTEM FAULT indicates that either a power fault or SCSI drive failure has occurred in the system.
GROUND	ground	GROUND is the power supply ground.
SM_IMB_SDA	in/out	I^{2}C* DATA is the data signal for the IPMB.
FP_NMI_BTN*	In	FRONT PANEL NMI is connected to a BMC input port, allowing the front panel to generate an NMI. FP_NMI_BTN* is pulled high to +5 V on the baseboard and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front panel.
SM_IMB_SCL	in/out	I^{2}C CLOCK is the clock signal for the Intelligent Platform Management Bus.
FP_RST_BTN*	In	FRONT PANEL RESET is connected to the BMC and causes a hard reset to occur, resetting all baseboard devices except for the BMC. FP_RST_BTN* is pulled high to +5 V on the baseboard, and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front panel.
+5V standby	Power	+5 V STANDBY is the standby 5-volt power supply.
FP_PWR_BTN*	In	FRONT PANEL POWER CONTROL is connected to the BMC and causes the power to toggle (on → off, or off → on). FP_PWR_BTN* is pulled high to +5 V standby on the baseboard and is intended to be connected to a momentary-contact push button (connected to GROUND when pushed) on the system front panel.
SM_FP_ISOL	In	SM_FP_ISOL, when asserted, isolates the front panel SM bus.
GROUND	ground	GROUND is the power supply ground.
RJ45_ACTLED_R	in	NIC activity LED.
reserved	-	Reserved.
SM_PRI_SCL	in/out	I^{2}C CLOCK is the clock signal for the primary private bus.
SM_PRI_SDA	in/out	I^{2}C DATA is the data signal for the primary private bus.

Notes: Type (in, out, in/out, power, ground) is from the perspective of the baseboard I/O connectors.

Table 65. SSI Compliant 24-pin Front Panel Connector Pinout (J1G1)

Pin	Signal Name	Pin	Signal Name
1	Power LED Anode	2	Test Point
3	Key	4	SB5V
5	Power LED Cathode	6	Cool Fault LED
7	HDD Activity LED Anode	8	SB5V
9	HDD Activity LED Cathode	10	System Fault LED
11	Power Switch	12	NIC#1 Activity LED
13	GND (Power Switch)	14	NIC#1 Link LED
15	Reset Switch	16	I2C SDA
17	GND (Reset Switch)	18	I2C SCL
19	ACPI Sleep Switch	20	Chassis Intrusion
21	GND (ACPI Sleep Switch)	22	NIC#2 Activity LED
23	NMI to CPU Switch	24	NIC#2 Link LED

7.4.1   High Density 100-Pin Floppy/FP/IDE Connector (J2H1)

The SCB2 serverboard has a multifunction connector that houses signals for a floppy drive, front panel with COM2 support, and an ATA-33 drive support into a single high-density, 100-pin

connector. The connector is used in Intel's SR1200 and SR2200 server chassis. It is used to transfer signals from the baseboard to the the chassis backplane using a single flex circuit type of cable, thus reducing the need for multiple legacy cables. The following table provides the pinout for this connector.

Table 66. High-Density 100-Pin FLOPPY/FP/IDE Connector Pin Out (J2H1)

Pin	Signal Name	Pin	Signal Name
A1	SPB_EMP_DTR_L	B1	SPB_EMP_DCD_L
A2	SPB_EMP_RTS_L	B2	SPB_EMP_CTS_L
A3	SPB_EMP_SIN	B3	SPB_EMP_SOUT
A4	SPB_EMP_DSR_L	B4	EMP_INUSE_L
A5	FP_NMI_BTN_L	B5	RJ45_SEC_ACTLED_R
A6	GND	B6	RJ45_SEC_LILED_R
A7	FP_ID_BTN_L	B7	FP_CHASSIS_INTRUSION
A8	GND	B8	PB1_5VSB_SCL
A9	FP_RST_BTN_L	B9	PB1_5VSB_SDA
A10	HDD_FAULT_R_L	B10	RJ45_PRI_ACTLED_R
A11	FP_PWR_BTN_L	B11	RJ45_PRI_LILED_R
A12	HDD_LED_ACT_R_L	B12	FP_ID_LED_R_L
A13	VCC	B13	SB5V
A14	FP_PWR_LED_R_L	B14	FP_SYS_FLT_LED2_R_L
A15	SB5V	B15	FP_SYS_FLT_LED_R_L
A16	RST_P6_PWR_GOOD	B16	IPMB_5VSB_SCL
A17	IPMB_5VSB_SDA	B17	GND
A18	GND	B18	FD_HDSEL_L
A19	FD_DSKCHG_L	B19	GND
A20	FD_WPD_L	B20	FD_RDATA_L
A21	FD_TRK0_L	B21	GND
A22	GND	B22	FD_WDATA_L
A23	FD_WGATE_L	B23	GND
A24	FD_DIR_L	B24	FD_STEP_L
A25	FD_DS0_L	B25	GND
A26	GND	B26	FD_MTR0_L
A27	FD_INDEX_L	B27	GND
A28	GND	B28	NC
A29	FD_DENSEL0	B29	GND
A30	GND	B30	IDE_RESET_L
A31	IDE_PDD<7>	B31	GND
A32	IDE_PDD<6>	B32	IDE_PDD<8>
A33	GND	B33	IDE_PDD<9>
A34	IDE_PDD<5>	B34	GND
A35	IDE_PDD<4>	B35	IDE_PDD<10>
A36	GND	B36	IDE_PDD<11>
A37	IDE_PDD<3>	B37	GND
A38	IDE_PDD<2>	B38	IDE_PDD<12>
A39	GND	B39	IDE_PDD<13>
A40	IDE_PDD<1>	B40	GND
A41	IDE_PDD<0>	B41	IDE_PDD<14>
A42	GND	B42	IDE_PDD<15>
A43	IDE_R_PDDREQ	B43	GND

Pin	Signal Name	Pin	Signal Name
A44	GND	B44	IDE_PDIOW_L
A45	IDE_PDDACK_L	B45	IDE_PDIOR_L
A46	GND	B46	IDE_R_PIORDY
A47	IDE_A<1>	B47	IRQ_R_PIDE
A48	IDE_A<0>	B48	IDE_A<2>
A49	IDE_PDCS0_L	B49	GND
A50	IDE_PRI_HD_ACT_L	B50	IDE_PDCS1_L

7.5   VGA Connector

The following table details the pin out of the VGA connector.

Table 67. VGA Connector Pin-out (J9A1)

Pin	Signal Name
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND
6	GND
7	GND
8	GND
9	Fused VCC(+5V)
10	GND
11	No connection
12	DDCDAT
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	DDCCLK

7.6   SCSI Connectors

The SCB2 server board provides two SCSI connectors, one for the high-density SCSI external (channel A) connector (located on the rear panel I/O), and the other for the internal wide SCSI connector (channel B). The two connectors have the same pin out. The following table details the pin out of the SCSI connectors.

Table 68. 68-pin VHDCI SCSI and Wide Connectors Pin Out (J1C1, J8A1)

Connector Contact Number	Signal Name	Signal Name	Connector Contact Number
1	+DB(12)	-DB(12)	35
2	+DB(13)	-DB(13)	36
3	+DB(14)	-DB(14)	37
4	+DB(15)	-DB(15)	38
5	+DB(P1)	-DB(P1)	39
6	+DB(0)	-DB(0)	40
7	+DB(1)	-DB(1)	41
8	+DB(2)	-DB(2)	42
9	+DB(3)	-DB(3)	43
10	+DB(4)	-DB(4)	44
11	+DB(5)	-DB(5)	45
12	+DB(6)	-DB(6)	46
13	+DB(7)	-DB(7)	47
14	+DB(P)	-DB(P)	48
15	GROUND	GROUND	49
16	GROUND	GROUND	50
17	RESERVED	RESERVED	51
18	RESERVED	RESERVED	52
19	RESERVED	RESERVED	53
20	GROUND	GROUND	54
21	+ATN	-ATN	55
22	GROUND	GROUND	56
23	+BSY	-BSY	57
24	+ACK	-ACK	58
25	+RST	-RST	59
26	+MSG	-MSG	60
27	+SEL	-SEL	61
28	+C/D	-C/D	62
29	+REQ	-REQ	63
30	+I/O	-I/O	64
31	+DB(8)	-DB(8)	65
32	+DB(9)	-DB(9)	66
33	+DB(10)	-DB(10)	67
34	+DB(11)	-DB(11)	68

7.7   NIC Connector

The SCB2 server board supports one stacked dual NIC RJ45 connector. The following table details the pin out of the connector.

Table 69. Stacked Dual RJ-45 Connector Pin Out (J7A1)

Pin	Signal Name	Pin	Signal Name
1	TXP (Primary)	17	Connected to Pin 16
2	TXM (Primary)	18	RXM (Secondary)
3	RXP (Primary)	19	GND (Secondary)
4	Connected to Pin 5	20	GND (Secondary)
5	Connected to Pin 4	21	SEC_SPEEDLED
6	RXM (Primary)	22	SB3V
7	GND	23	SEC_LILED
8	GND	24	SEC_ACTLED_FB
9	PRI_SPEEDLED	25	N/C
10	SB3V	26	N/C
11	PRI_LILED	27	GND
12	PRI_ACTLED_FB	28	GND
13	TXP (Secondary)	29	GND
14	TXM (Secondary)	30	GND
15	RXP (Secondary)	31	GND
16	Connected to Pin 17	32	GND

7.8   ATA Connectors

The ATA-100 SCB2 board provides two 40-pin, low-density ATA-100 connectors. The pin out for both connectors is identical and is listed in the following table.

Table 70. ATA-100, 40-pin Connectors Pin Out (J2F1, J2G1)

Pin	Signal Name	Pin	Signal Name
1	RESET_L	2	GND
3	DD7	4	IDE_DD8
5	DD6	6	IDE_DD9
7	DD5	8	IDE_DD10
9	DD4	10	IDE_DD11
11	DD3	12	IDE_DD12
13	DD2	14	IDE_DD13
15	DD1	16	IDE_DD14
17	DD0	18	IDE_DD15
19	GND	20	KEY
21	IDE_DMAREQ	22	GND

Pin	Signal Name	Pin	Signal Name
23	IDE_IOW_L	24	GND
25	IDE_IOR_L	26	GND
27	IDE_IORDY	28	GND
29	IDE_DMAACK_L	30	GND
31	IRQ_IDE	32	Test Point
33	IDE_A1	34	DIAG
35	IDE_A0	36	IDE_A2
37	IDE_DCS0_L	38	IDE_DCS1_L
39	IDE_HD_ACT_L	40	GND

Both the SCSI and ATA-100 versions of the SCB2 server board provide ATA-33 support. There are two separate interface connectors for ATA-33. The first is a low-density, 40-pin connector, and the second is embedded in the high-density, 100-pin floppy/FP/IDE connector.

Note: using both ATA-33 interfaces in a common system may result in unpredictable I/O failures and data corruption. This configuration is not supported.

The following table provides the pinout for the 40-pin legacy connector. See *Table 66* for the 100-pin floppy/FP/IDE connector pin out.

Table 71: ATA-33 Low-Density, 40-pin Connector Pin Out (J1J1)

Pin	Signal Name	Pin	Signal Name
1	RESET_L	2	GND
3	DD7	4	IDE_DD8
5	DD6	6	IDE_DD9
7	DD5	8	IDE_DD10
9	DD4	10	IDE_DD11
11	DD3	12	IDE_DD12
13	DD2	14	IDE_DD13
15	DD1	16	IDE_DD14
17	DD0	18	IDE_DD15
19	GND	20	KEY
21	IDE_DMAREQ	22	GND
23	IDE_IOW_L	24	GND
25	IDE_IOR_L	26	GND
27	IDE_IORDY	28	GND
29	IDE_DMAACK_L	30	GND
31	IRQ_IDE	32	Test Point
33	IDE_A1	34	Test Point
35	IDE_A0	36	IDE_A2
37	IDE_DCS0_L	38	IDE_DCS1_L
39	IDE_HD_ACT_L	40	GND

7.9   USB Connector

The following table provides the pin out for both external USB connectors.

Table 72. USB Connectors Pin Out (J5A1, J10A2)

Pin	Signal Name
1	Fused VCC (+5V /w over current monitor of both port 0 and 1)
2	DATAL0 (Differential data line paired with DATAH0)
3	DATAH0 (Differential data line paired with DATAL0)
4	GND

A header on the server board provides an option to support two additional USB connectors. The pin out of the header is detailed in the following table.

Table 73. Optional USB Connection Header Pin-out (J10G1)

Pin	Signal Name	Description
1	VREG_FP_USBPWR0	Front Panel USB Power (Ports 0,1)
2	VREG_FP_USBPWR0	Front Panel USB Power (Ports 0,1)
3	USB_FP_P0-	Front Panel USB Port 0 Negative Signal
4	USB_FP_P1-	Front Panel USB Port 1 Negative Signal
5	USB_FP_P0+	Front Panel USB Port 0 Positive Signal
6	USB_FP_P1+	Front Panel USB Port 1 Positive Signal
7	Ground	
8	Ground	
9	Key	
10	USB_FP_OC0	Front Panel USB Overcurrent signal (Ports 0,1)

7.10 Floppy Connector

The SCB2 server board provides two separate interfaces to the floppy drive controller. The first is a legacy 34-pin connector, and the second is embedded in the high-density, 100-pin floppy/FP/IDE connector.

Note: using both the 34-pin floppy connector and the 100-pin floppy/FP/IDE connectors in a common system is not a supported configuration.

The following tables detail the pin out of the 34-pin legacy floppy connector.

Table 74. Legacy 34-pin Floppy Connector Pin Out (J4G1)

Pin	Signal Name	Pin	Signal Name
1	GND	2	FD_DENSEL0
3	GND	4	Test Point
5	KEY	6	FD_DENSEL1
7	GND	8	FD_INDEX_L
9	GND	10	FD_MTR0_L
11	GND	12	FD_DS1_L
13	GND	14	FD_DS0_L
15	GND	16	FD_MTR1_L
17	Test Point	18	FD_DIR_L
19	GND	20	FD_STEP_L
21	GND	22	FD_WDATA_L
23	GND	24	FD_WGATE_L
25	GND	26	FD_TRK0_L
27	Test Point	28	VCC
29	GND	30	FD_RDATA_L
31	GND	32	FD_HDSEL_L
33	GND	34	FD_DSKCHG_L

7.11 Serial Port Connector

Two serial ports are provided on the server board.

- An external low-profile RJ45 connector is located on the back edge of the baseboard to supply a Serial 2 port with an optional Serial 2 interface provided through either of the two high-density front panel connectors. The rear Serial 2 port will support any standard serial device as well as providing support for a serial concentrator. For those server applications that require a DB9 type serial connector, an 8-pin RJ45 to DB9 adapter must be used. See Section 3.3.3.2 for more details on Serial 2 usage.

- A Serial 1 (COM1) port is provided through a 9-pin header on the server board.

The following tables detail the pin outs of these two ports.

Table 75. External Low-Profile RJ-45 Serial 2 Port Pin-out (J6A1)

Pin	Signal Name	Description
1	RTS	Request To Send
2	DTR	Data Terminal Ready
3	TD	Transmit Data
4	SGND	Signal Ground
5	RI	Ring Indicate
6	RD	Receive Data
7	DCD or DSR	Carrier Detect or Data Set Ready [1]
8	CTS	Clear to send

Note: This pin setting is dependant on a jumper block setting at location J6A2

Table 76. 9-pin Header Serial 1 Port Pin Out (J9B2)

Pin	Signal Name
1	DCD (carrier detect)
2	DSR (data set ready)
3	RD (receive data)
4	RTS (request to send)
5	TD (transmit data)
6	CTS (clear to send)
7	DTR (data terminal ready)
8	RI (ring indicate)
9	Ground
10	Missing pin

7.12 Keyboard and Mouse Connector

One PS/2 port is provided for use by either a keyboard or a mouse. For server applications that require both a PS/2-compatible keyboard and mouse, a PS/2 Y-cable can be used. The following table details the pin out of the PS/2 connector.

Table 77. Keyboard & Mouse PS/2 Connector Pin Out (J6A3)

Pin	Signal Name
1	Keyboard Data
2	Mouse Data
3	GND
4	VCC
5	Keyboard Clock
6	Mouse Clock

7.13 Miscellaneous Headers

7.13.1   Fan Headers

The SCB2 server board provides six 3-pin fan headers. The fans labeled "Aux Fan", "CPU1 Fan", and "CPU2 Fan", do not have variable speed fan power; they use direct 12 volts. They will only support fan types that do not require controlled speed, such as those used on processor fan heat sinks. The fans labeled "Sys Fan1", "Sys Fan2", and "Sys Fan3" will provide variable speed fan power and will support variable speed fans.

Table 78. Three-Pin Fan Headers Pin- Out (J4K1, J4K2, J6K1, J6K2, J9K1, J9K2)

Pin	Signal Name	Type	Description
1	Ground	Power	GROUND is the power supply ground
2	Fan Power	Power	Variable speed fan power (except Aux or CPU fans, straight 12 V)
3	Fan Tach	Out	FAN_TACH signal is connected to the BMC to monitor the fan speed

The SCB2 server board also provides a 1x7 fan pack header, which is used to support a 5 fan assembly as used in the Intel SR1200 server chassis, or can be used to reference 1U chassis applications.

Note: using both the 1x7 pin fan pack header, along with any of the individual processor or system fan headers in a common system, is not a supported configuration.

Table 79. Seven-Pin Fan Header Pin Out (J3K1)

Pin	Signal Name	Type	Description
1	Fan Tach5	Out	FAN_TACH signal of FAN5
2	Fan Tach4	Out	FAN_TACH signal of FAN4
3	Fan Tach3	Out	FAN_TACH signal of FAN3
4	Fan Tach2	Out	FAN_TACH signal of FAN2
5	Fan Tach1	Out	FAN_TACH signal of FAN1
6	Ground	Power	Power supply ground
7	12V	Power	Variable speed fan power

7.14 System Recovery and Update Jumpers

One 14-pin single inline header (J1E1), located on the edge of the baseboard next to the legacy IDE connector, provides a total of four 3-pin jumper blocks that are used to configure several system recovery and update options. The figure below shows the factory default locations for each jumper option. The factory defaults are set to a protected mode for each function. The shaded areas show the jumper placement for each configurable option when a given task is to be performed.

Example: the BMC Boot Block Write Protect jumper is set by the factory to protect anyone from writing over the BMC boot block. In order to write over the existing, or to restore the BMC boot block, the jumper must be set to the shaded position.

Note: updating the operational code of the BMC firmware does NOT require that the BMC Boot Block Write Protect jumper be moved. This jumper should ONLY be moved if the BMC boot block has been corrupted and needs to be restored, or the release notes of a given BMC firmware update specifies that a boot block update is necessary.
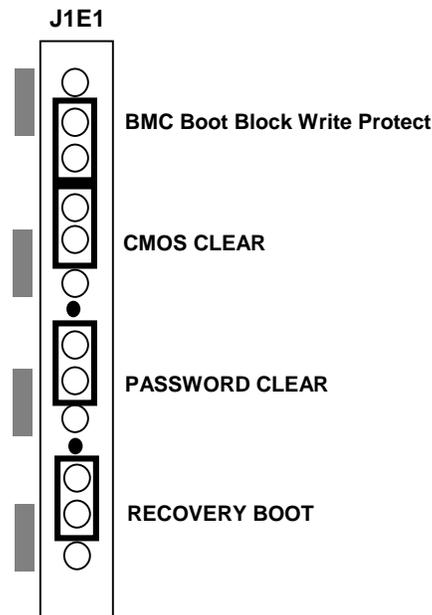
Figure 12. SCB2 Configuration Jumpers (J1E1)

The following table describes each jumper option.

Table 80. Configuration Jumper Options

Option	Description
BMC Boot Block Write Protect "BMC WP"	If pins 2 and 3 are jumpered (default), the BMC boot block is write-protected. If pins 1 and 2 are jumpered, the boot block is erasable and programmable. **WARNING:** Incorrect programming of the boot block will render the system unbootable. With this option set to its default factory setting, the BMC's operational code can still be programmed without moving the jumper.
CMOS Clear	If pins 1 and 2 are jumpered (default), preservation of configuration CMOS through system reset is controlled by the BMC. If pins 2 and 3 are jumpered, CMOS contents are set to manufacturing default during system reset.
Password Clear	If pins 1 and 2 are jumpered (default), the current system password is maintained during system reset. If pins 2 and 3 are jumpered, the password is cleared on reset.
Recovery Boot	If pins 1 and 2 are jumpered (default) the system will attempt to boot using the BIOS programmed in the flash memory. If pins 2 and 3 are jumpered, the BIOS will attempt a recovery boot, loading BIOS code from a floppy disk into the flash device. This is typically used when the BIOS code has been corrupted.

7.15 External RJ45 Serial Port Jumper Block

The jumper block, J6A1, located directly behind the external low-profile RJ45 serial port, is used to configure either a DSR or a DCD signal to the connector. See Section 3.3.3.2.1 for additional information on serial port usage.

8.   General Specifications

8.1   Absolute Maximum Ratings

Operating an SCB2 baseboard at conditions, beyond those shown in the following table, may cause permanent damage to the system. The table is provided for stress testing purposes only. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 81. Absolute Maximum Ratings

Operating Temperature	5 degrees C to 50 degrees C [1]
Storage Temperature	-55 degrees C to +150 degrees C
Voltage on any signal with respect to ground	-0.3 V to Vdd + 0.3V [2]
3.3 V Supply Voltage with Respect to ground	-0.3 V to 3.63 V
5 V Supply Voltage with Respect to ground	-0.3 V to 5.5 V

Notes:
- Chassis design must provide proper airflow to avoid exceeding the Intel® Pentium® III processor "Coppermine-T or Tualatin" maximum case temperature.
- VDD means supply voltage for the device.

8.2   SCB2 Power Budget

The following table shows the power consumed on each supply line for a SCB2 server board that is configured with two processors (each 30W max), >1GHz FMB @ 75% usage. This configuration includes six DIMMs stacked burst at 70% maximum. The numbers provided in the table should be used for reference purposes only. Different hardware configurations will produce different numbers. The numbers in the table reflect a common usage model operating at higher-than-average stress levels.

Table 82. SCB2 Power Budget

Device(s)	3.3V	+5V	+12V	-12V	5V Standby	
Processors	-	0.762A	4.414A	-	-	
Memory DIMMs	7.2A	-	-	-	-	
Server board	4.4A	2.7A	0.3A	0.05A	1.25A	
Fans	-	-	1.575A	-	-	
Keyboard/Mouse	-	0.5A	-	-	-	
PCI slots	6.1A	-	0.4A	0.2A	0.29A	
Peripheral	-	**3.1A**	**3.75A**	**-**	**-**	
Total Current	17.7A	7.06A	10.45A	0.25A	1.54A	**Total**
Total Power	58.41W	35.3W	125.4W	3W	7.7W	229.8W

8.3   Power Supply Specifications

This section provides power supply design guidelines for an SCB2-based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 83. SCB2 Static Power Supply Voltage Specification

Parameter	Min	Nom	Max	Units	Tolerance
+3.3 V	+3.25	+3.30	+3.35	V_{rms}	+1.5/-1.5%
+5 V	+4.90	+5.00	+5.10	V_{rms}	+2/-2%
+12 V	+11.76	+12.00	+12.24	V_{rms}	+2/-2%
-12 V	-11.40	-12.20	-13.08	V_{rms}	+9/-5%
+5 VSB	+4.85	+5.00	+5.20	V_{rms}	+4/-3%

Table 84. SCB2 Dynamic Power Supply Voltage Specification

Output	Min	Max	Tolerance
+3.3 V	3.20 V	3.46 V	+5 / -3 %
+5 V	4.80 V	5.25 V	+5 / -4 %
+12 V	11.52 V	12.6 V	+5 / -4 %
+5 V SB	4.80 V	5.25 V	+5/ -4%

8.3.1   Power Timing

This section discusses the timing requirements for operation with a single power supply. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}), within 5 ms to 70 ms. The +3.3 V, +5 V and +12 V output voltages start to rise approximately at the same time. All outputs must rise monotonically. The +5 V output must be greater than the +3.3 V output during any point of the voltage rise, but never by more than 2.25 V. Each output voltage shall reach regulation within 50 ms (T_{vout_on}) of each other and begin to turn off within 400 ms (T_{vout_off}) of each other. The following figure shows the output voltage timing parameters.
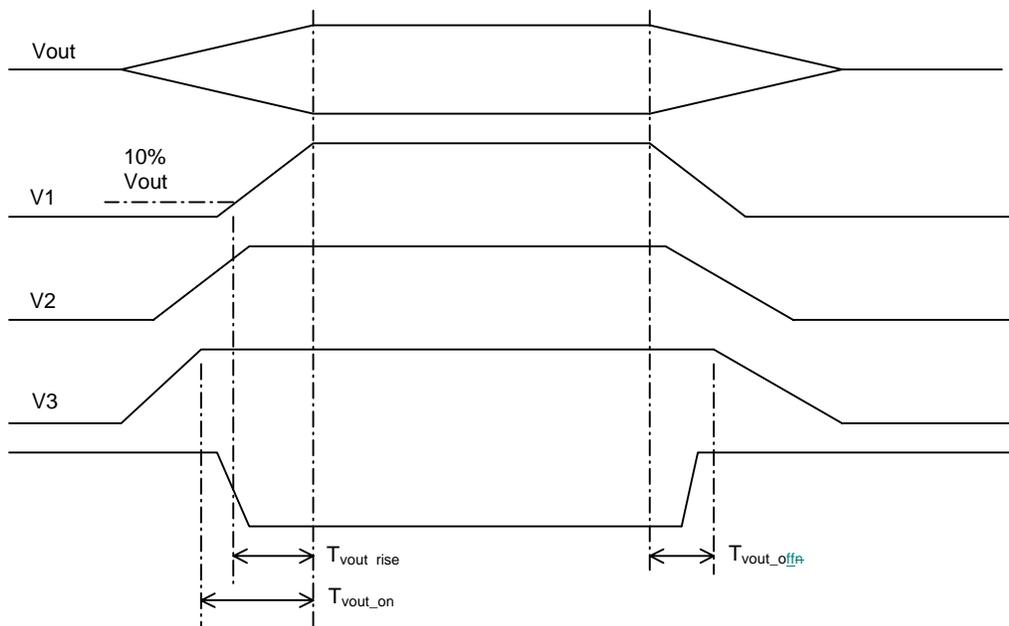
Figure 13. Output Voltage Timing

The following tables show the timing requirements for a single power supply being turned on and off via the AC input with PSON held low, and the PSON signal, with the AC input, applied. The ACOK# signal is not being used to enable to turn on timing of the power supply.

Table 85. Voltage Timing Parameters

Item	Description	Min	Max	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	70	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	msec
T_{vout_off}	All main outputs must leave regulation within this time.		400	msec

Table 86. Turn On / Off Timing

Item	Description	Min	Max	Units
$T_{sb\_on\_delay}$	Delay from AC being applied to 5 V standby being within regulation.		1500	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	msec
T_{vout_holdup}	Time all output voltages stay within regulation after loss of AC.	21		msec
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	20		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSON# deactive to PWOK being de-asserted.		50	msec
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T_{pwok_off}	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	2		msec
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		msec
T_{sb_vout}	Delay from 5 V standby being in regulation to O/Ps being in regulation at AC turn on.	50	1000	msec
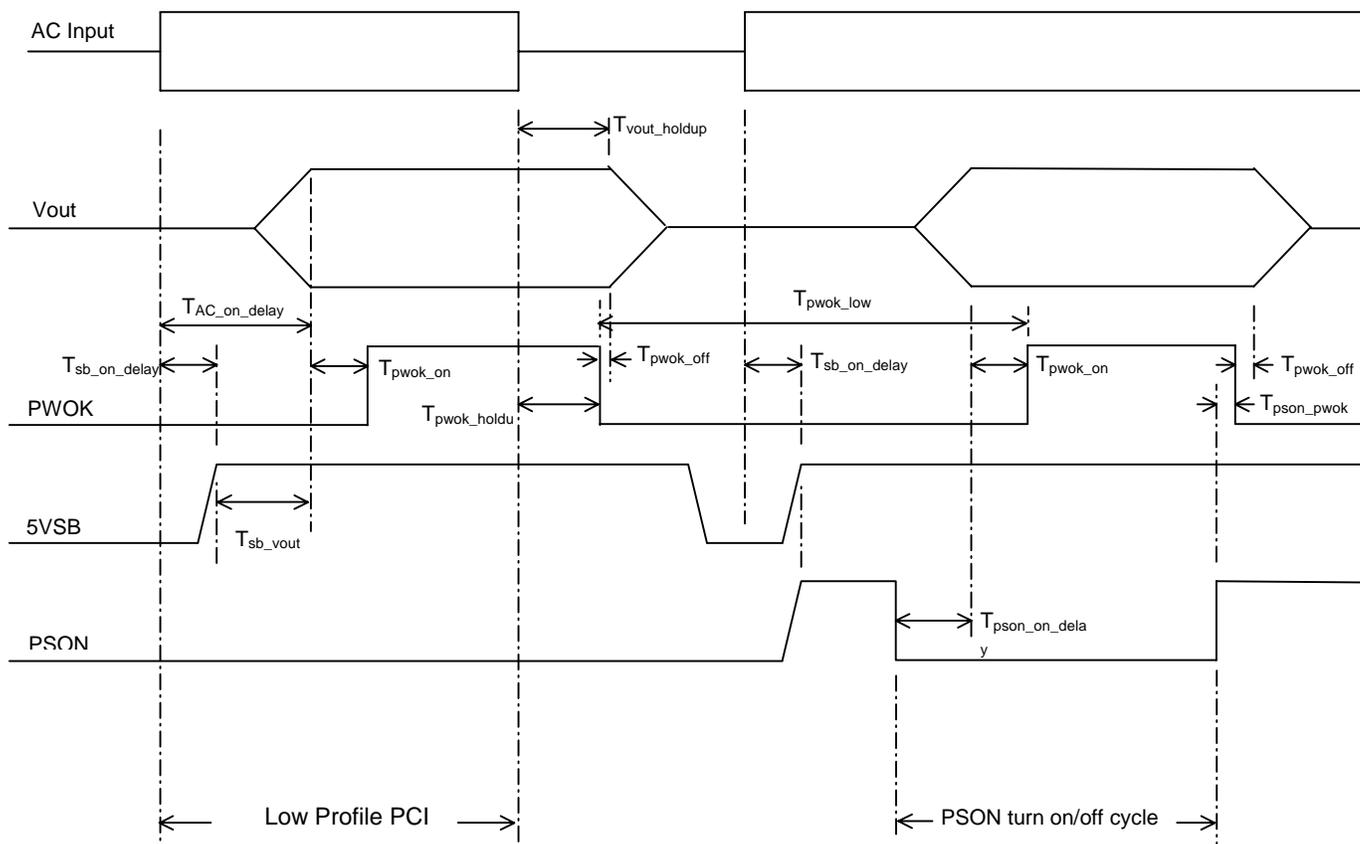
Figure 14. Turn on / off Timing

8.3.2   Voltage Recovery Timing Specifications

The power supply must conform to the following specifications for voltage recovery timing under load changes.

- Voltage shall remain within +/- 5% of the nominal set voltage on the +5 V, +12 V, 3.3 V, -5 V and -12 V output, during instantaneous changes in load shown in the following table.

- Voltage regulation limits shall be maintained over the entire AC input range and any steady state temperature and operating conditions specified.

- Voltages shall be stable as determined by bode plot and transient response. The combined error of peak overshoot, set point, regulation, and undershoot voltage shall be less than or equal to +/-5% of the output voltage setting. The transient response measurements shall be made with a load changing repetition rate of 50 Hz to 5 kHz. The load slew rate shall not be greater than 0.2 A/µs.

Table 87. Transient Load Requirements

Output	Step Load Size	Starting Level	Finishing Level	Slew Rate
+3.3 V	4.8 A	30Min. Load	Min. load + 4.8 A and step up to max. load	0.50 A/µs
+5 V	3.0 A	30Min. Load	Min. load + 3.0 A and step up to max. load	0.50 A/µs
+12 V	10.4 A	Min. Load	Min. load + 10.4 A and step up to max. load	0.50 A/µs
+5 VSB	500 mA	Min. Load	Min. load + 500 mA and step up to max. load	0.50 A/µs
-12 V	325 mA	Min. Load	Min load +325 mA and step up to max. load	0.50 A/µs

8.4   Product Regulatory Compliance

8.4.1   Product Safety Compliance

The SCB2 complies with the following safety requirements:

- UL 1950 - CSA 950 (US/Canada)
- EN 60 950 (European Union)
- IEC60 950 (International)
- CE – Low Voltage Directive (73/23/EEC) (European Union)
- EMKO-TSE (74-SEC) 207/94 (Nordics)
- GOST R 50377-92 (Russia)

8.4.2   Product EMC Compliance

The SCB2 has been has been tested and verified to comply with the following electromagnetic compatibility (EMC) regulations when installed in a compatible Intel host system. For information on compatible host system(s), contact your local Intel representative.

- FCC (Class A Verification) – Radiated & Conducted Emissions (USA)
- ICES-003 (Class A) – Radiated & Conducted Emissions (Canada)
- CISPR 22 (Class A) – Radiated & Conducted Emissions (International)
- EN55022 (Class A) – Radiated & Conducted Emissions (European Union)
- EN55024 (Immunity) (European Union)
- CE – EMC Directive (89/336/EEC) (European Union)
- AS/NZS 3548 (Class A) – Radiated & Conducted Emissions (Australia / New Zealand)
- RRL (Class A) Radiated & Conducted Emissions (Korea)
- BSMI (Class A) Radiated & Conducted Emissions (Taiwan)

8.4.3   Product Regulatory Compliance Markings

This product is provided with the following product certification markings:

- cURus Recognition Mark
- CE Mark
- Russian GOST Mark
- Australian C-Tick Mark
- Taiwan BSMI Certification Number 3902I904 and BSMI EMC Warning

8.5   Electromagnetic Compatibility Notices

8.5.1   Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE mark to illustrate its compliance.

8.5.2   Australian Communications Authority (ACA) (C-Tick Declaration of Conformity)

This product has been tested to AS/NZS 3548, and complies with ACA emission requirements. The product has been marked with the C-Tick mark to illustrate its compliance.

8.5.3   Ministry of Economic Development (New Zealand) Declaration of Conformity

This product has been tested to AS/NZS 3548, and complies with New Zealand's Ministry of Economic Development emission requirements.

8.5.4   BSMI (Taiwan)

The BSMI Certification number 3902I904 is silk screened on the component side of the server board; and the following BSMI EMC warning is located on solder side of the server board.

警告使用者：

這是甲類的資訊產品，在居住的環境中使用時，
可能會造成射頻干擾，在這種情況下，使用者會
被要求採取某些適當的對策。

8.6 Replacing the Back-Up Battery

The lithium battery on the server board powers the RTC for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

⚠️   WARNING
Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

⚠️   ADVARSEL**!**
Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

⚠️   ADVARSEL
Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

⚠️   VARNING
Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

⚠️   VAROITUS
Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

8.7   Calculated Mean Time Between Failures (MTBF)

Table 88. SCB2 MTBF

MTBF	Ambient Air Temperature	Air Temp. at Board for 15oC rise
(hours)	(oC)	(oC)
70,000	45	60
90,000	40	55
110,000	35	50
140,000	30	45
180,000	25	40

8.8   Mechanical Specifications

The following figure shows the server board mechanical drawing.
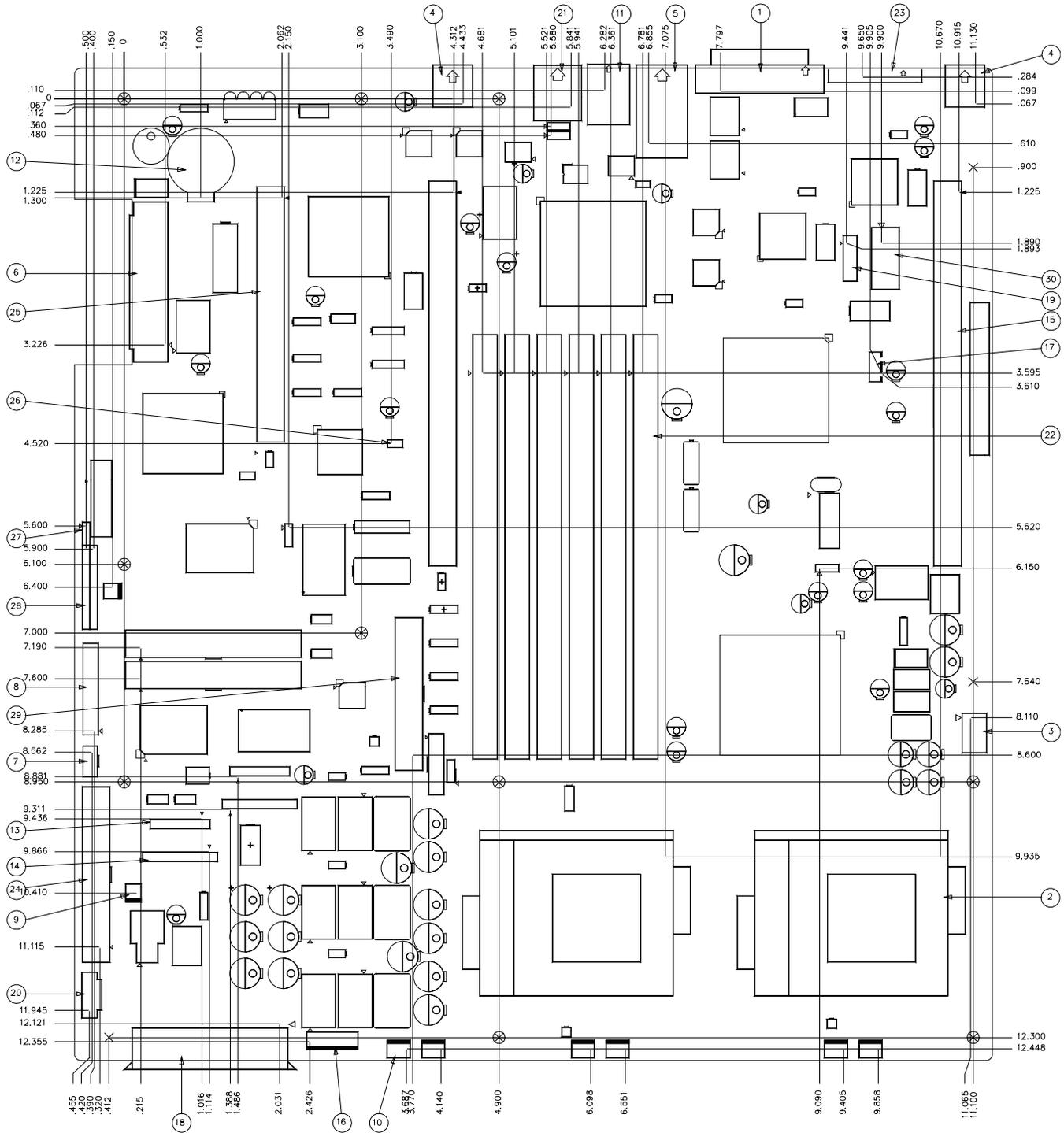
Figure 15. SCB2 Server Board Mechanical Drawing

Table 89. Server Board Connector Specifications

Item	Qty.	Manufacturer and Part Number	Description
1	1	AMP* 787254-1	68P VHDCI SCSI connector
2	2	AMP 98-2162-019-003	370P PGA370 socket
3	1	AMP 147706-1	9P header type dual USB connector
4	2	AMP 787616-1	4P jack type single USB connector
5	1	AMP 1368011-3	16P stacked dual NIC connector
6	1	Foxconn* QA11343-P1	68P angle SCSI connector
7	1	Foxconn HF55040-P1	4P external IPMB connector
8	1	Foxconn HC1912G-D5	24P front panel Ccnnector
9	2	Foxconn HF06021-P1	2P chassis intrusion and HDD LED connector
10	6	Foxconn HF08030-P1	3P fan connector
11	1	Foxconn MH11067-PH2	6P single PS/2 connector (keybd/mouse)
12	1	JAEE* JE920-2003	2P battery holder
13	2	Molex* 52559-3092	Does not exist on the server board
14	2	Molex 52559-4092	40P FDD&IDE FPC connector
15	2	Molex 89177-9250	184P 64bit PCI riser connector
16	1	Molex 53375-0710	7P FAN module connector
17	1	Molex 22-44-7031	3P SMB connector
18	1	Molex 15-24-9244	24P power connector
19	1	Molex 22-43-6050	5P ICMB connector
20	1	Molex 70543-0004	5P signal power connector
21	1	Molex 43202-8927	8P angle serial port connector
22	6	Nextron* 178-168-621-630-40	168P DIMM connector
23	1	SUYIN* 7535S-15G2T	15P video connector
24	3	WORWIN* W31-007-4020	40P IDE connector
25	1	Wooyoung* HDC-120-1.27D	120P 32bit PCI connector
26	1	Wooyoung SPS01-S02A	2P SHMOO connector
27	6	Wooyoung SPS01-S03A-5A1	3P jumper header
28	2	Wooyoung SPS01-S11A-5A3-R2	11P jumper header
29	1	Wooyoung BHS-33A-2.54D	34P FDD connector
30	1	Wooyoung BHS-9A-2.54D	10P straight serial port connector

8.8.1   PCI Riser Cards

The SCB2 server board supports two peer 64-bit, 66 MHz PCI buses. Each provides a PCI riser slot that is capable of supporting either a 1-slot PCI riser card or a 3-slot PCI riser card. This will allow PCI 2.2-compliant 3.3 V and universal expansion cards to be physically parallel with the server board.

8.8.1.1   1-Slot 3.3V PCI Riser Card

The 1-slot PCI riser card provides support for one 64-bit, 66 MHz, 3.3 V PCI card. The 1-slot riser card is used in either of the two available 5 V, 66 MHz, 64-bit, PCI 2.2-compliant PCI riser slots on the server board. All standard signals are connected from the 5 V connector to the 3.3 V connector.
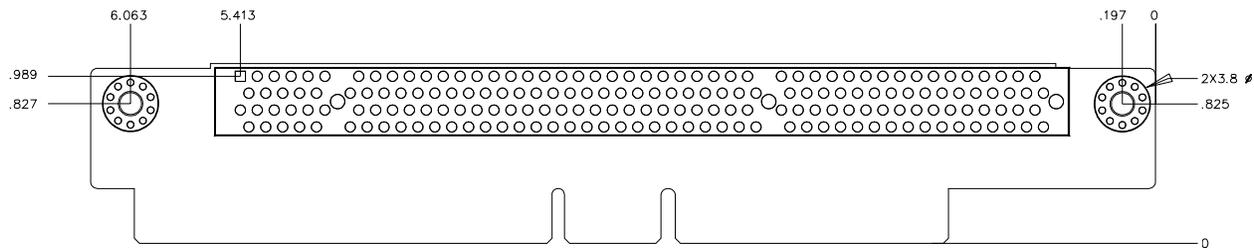
Figure 16. 1-Slot PCI Riser Mechanical Drawing

8.8.1.2   3-Slot 3.3V PCI Riser Card

The 3-slot PCI riser card provides support for three 64-bit, 66 MHz, 3.3 V PCI cards. The 3-slot riser card is used in either of the two available 5 V, 66 MHz, 64-bit, PCI 2.2-compliant PCI riser slots on the server board. All standard signals are connected from 5 V connector to the 3.3 V connectors.
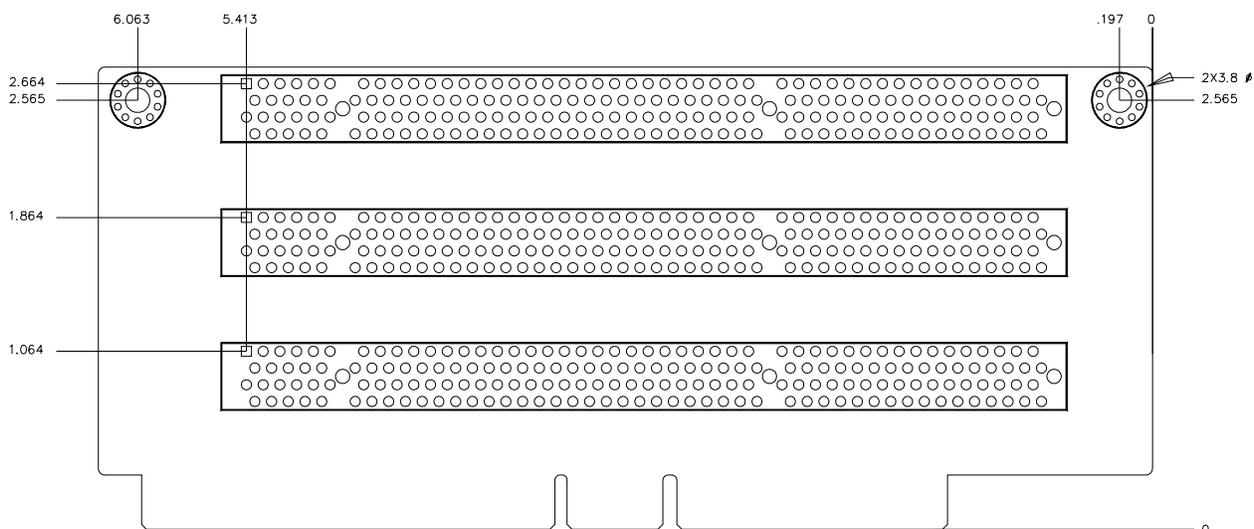
Figure 17. 3-Slot PCI Riser Mechanical Drawing

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Appendix A: SCB2 Integration and Usage Tips

This section provides a bullet list of useful information that is unique to the SCB2 server board and should be kept in mind while integrating and configuring your SCB2 based server.

- The SCB2 is available with 2 different hard drive interfaces, SCSI and ATA-100

- Only Intel Pentium III processors using FCPGA2 packaging is supported on SCB2 – see Section 3.1.1

- Processors must be populated in the sequential order; that is, processor Socket #1 must be populated before processor Socket #2

- Both processor slots must be populated. Socket #1 with a processor, and Socket #2 with either a processor or terminator

- Memory DIMMs must be installed in pairs. DIMM pairs are NOT located next to each other - see Section 3.1.2

- Only low profile DIMMs can be supported in a 1U server chassis.

- The SCB2 provides an external Serial 2 port that uses a low profile, 8-pin RJ45 connector. See Section 3.3.3.2 for usage information

- By default as configured in the factory, the SCB2 baseboard will have the back RJ45 Serial 2 port configured to support a DSR signal, which is compatible with the Cisco standard. To use a modem with this serial port, the J6A1jumper block must be configured properly. See Section 3.3.3.2.1.

- Using both the SSI IDE connector and the high-density "Floppy/IDE/Front Panel" connector in a common configuration is not supported.

- Using both the SSI floppy connector and the high-density "Floppy/IDE/Front Panel" connector in a common configuration is not supported.

- Zero Channel RAID cards are only supported in the first slot of either the 1-slot or 3-slot PCI riser cards used on the P64-B PCI segment. See Section 3.5.2.4.

- At the completion of POST, the system status LED on the baseboard, along with the system status LED located on the front panel, will turn on green and stay on during normal operating conditions. A blinking green light or an amber light, either solid or blinking, indicates a system fault.

- Using both the 1x7 pin fan pack header, along with any of the individual processor or system fan headers in a common system, is not a supported configuration.

- With legacy USB enabled, the system BIOS requires 16KB of conventional memory space. Some Linux applications and loaders may not function with this feature enabled.

- A five second delay should be used when cycling system power from on to off and back to on. A shorter delay may cause some hard disk drives to not be seen during POST.

- When installing the processor heat sink, care should be taken to ensure proper heat sink orientation. Heat sinks that are installed backwards may cause irreparable damage to the processor socket. The instruction sheet provided with the Intel® Pentium™ III boxed processor should be read before attempting to install the processor heat sink.

Appendix B: Riser Card Design Guide for Reference Chassis

The Intel® Server Board SCB2 utilizes a special PCI riser connector layout in order to achieve the triple slot, 64-bit/66MHz, 2U riser solution. This appendix is provided to assist chassis manufacturers or customers who would like to design their own chassis and riser card solution for the SCB2 server board.

Below are the riser card routing rules for the triple-slot riser. These rules need to be followed to create a riser card that will function reliably with the SCB2 baseboard. To design a single slot, 1U capable riser, the same design requirements apply, but only slot 1 would be used. Refer to the section on PCI risers for mechanical drawings and see the section on the connector pin definitions for exact pin-outs for the connectors on the board.

The diagram below is for the PCI segment B riser. The same routing rules apply to the PCI segment C riser, but the specific baseboard information can be ignored (i.e. distance to SCSI controller, etc.).

Specific routing information is available in the form of a gerber file. Please contact your Intel representative for specific information on how to obtain this document.

Routing Rules for SCB2 PCI-66MHz Riser Cards
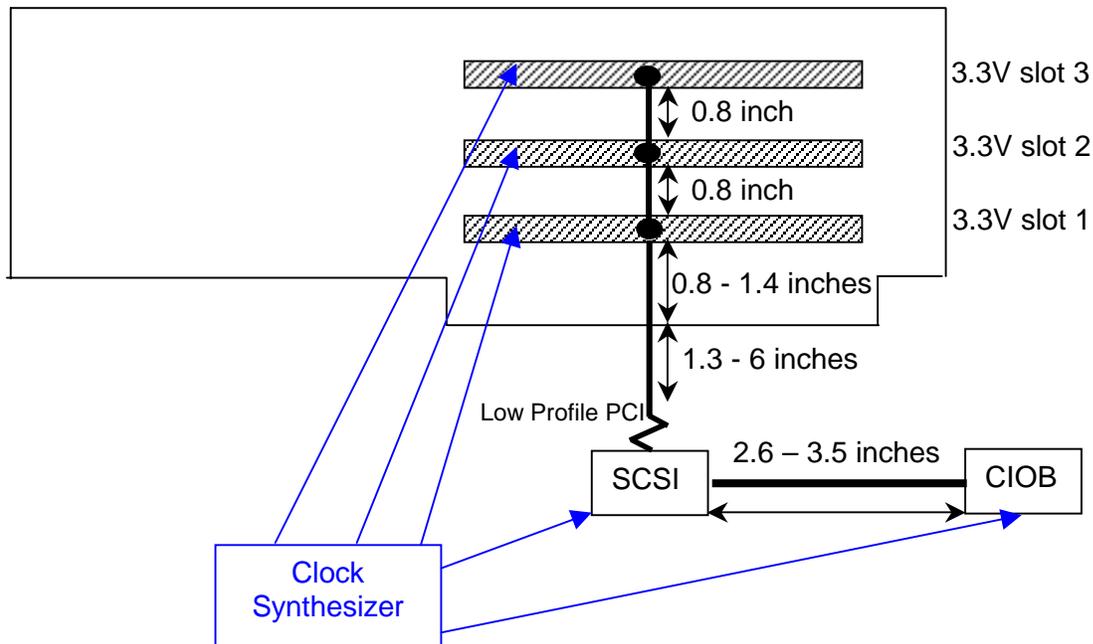
- All PCI signals must strictly adhere to the above lengths except for RESET, REQ, GNT, and clocks.

  - RESET is asynchronous and not length restricted.
  - REQ and GNT are point-to-point and may be slightly longer.
  - See below for clock requirements.

- The riser should be a 4-layer construction, with power and ground planes inside and signals routed on the outer layers.

- Characteristic impedance should be 60 Ohms +/- 10%.

- All clock lengths from synthesizer to receivers must match within 500ps. Clock traces on the riser should be 5.3 to 5.5 inches.

- Clock traces should be routed on the layer adjacent to the ground plane.

- The other traces should be staggered across the two sides of the board and routed as direct as possible to minimize crosstalk effects.

Appendix C: SCB2 Errata

The following is a list of known errata for the SCB2 server board. Errata listed in this section are classified as issues that cause the board to deviate from the published specifications for this board and that will not be addressed. For a complete list of errata for the SCB2 server board, including those that are planned to be addressed, please reference the SCB2/SR1200/SR2200 Monthly Specification Update posted to Intel's support web site.

http://support.intel.com/support/motherboards/server/SCB2/

1. The SCB2 Server board does not offer 57.6 kbps speed as an option for serial ports in the BIOS Setup Utility. Serial ports are limited to operate at speeds 9600, 19.2k, 38.4k, 115.2 kbps for all functions. Set speed to 115.2 Kbps and allow devices to autonegotiate to fastest mutually supported speed

2. If there are more than eight drives connected to the on-board SCSI of the SCB2 Server board, only the first eight SCSI hard drives are listed in BIOS Setup under Boot Order. SCSI option ROM supports a maximum of 8 HDD for boot order based on the BIOS Boot Specification. A bootable drive connected to the on-board SCSI controller must be configured to be between the first eight hard drives in order to be identified as bootable by BIOS.

3. The SCB2 Server board BIOS Utility does not interpret the row of numeric keys (above letters) in a standard QWERTY keyboard the same as numeric keys from a Num-Pad when entering/defining passwords. BIOS regards these as different characters; when entering a password, BIOS will not accept it as a valid password unless it is entered with the set of keys as it was defined.

4. A BIOS Recovery operation from an LS-120 drive is not supported. Only standard 3.5" 1.44MB Floppy removable devices are supported

5. The Promise* PDC20267 ATA-100 controller does not support the ATAPI command set. ATAPI devices attached to either of the ATA-100 channels on the SCB2-ATA board will not function

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Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
AP	Application Processor
ASIC	Application Specific Integrated Circuit
ASR	Asynchronous Reset
BGA	Ball-grid Array
BIOS	Basic input/output system
BIST	Built-in self test
BMC	Server board Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other.
BSP	Bootstrap Processor
Byte	8-bit quantity.
CIOB	PCI 64-bit hub
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
CSB5	Legacy I/O controller hub
DCD	Data Carrier Detect
DMA	Direct Memory Access
DMTF	Distributed Management Task Force
ECC	Error Correcting Code
EMC	Electromagnetic Compatibility
EMP	Emergency management port.
EPS	External Product Specification
ESCD	Extended System Configuration Data
FDC	Floppy Disk Controller
FIFO	First-In, First-Out
FRB	Fault resilient booting
FRU	Field replaceable unit
GB	1024 MB.
GPIO	General purpose I/O
GUID	Globally Unique ID
Hz	Hertz (1 cycle/second)
HDG	Hardware Design Guide
I^2C	Inter-integrated circuit bus
IA	Intel® architecture
ICMB	Intelligent Chassis Management Bus
IERR	Internal error
IMB	Inter Module Bus
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IRQ	Interrupt Request
ISC	Intel® Server Control

Term	Definition
ITP	In-target probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local area network
LBA	Logical Block Address
LCD	Liquid crystal display
LPC	Low pin count
LSB	Least Significant Bit
LVD	Low-Voltage Differential
LVDS	Low-Voltage Differential SCSI
MB	1024 KB
MBE	Multi-Bit Error
Ms	milliseconds
MSB	Most Significant Bit
MTBF	Mean Time Between Failures
Mux	multiplexor
NIC	Network Interface Card
NMI	Non-maskable Interrupt
OEM	Original equipment manufacturer
Ohm	Unit of electrical resistance
P32-A	32-bit PCI Segment
P64-B	Full Length 64/66 MHz PCI Segment
P64-C	low-profile 64/66 MHz PCI Segment
PBGA	Pin Ball Grid Array
PDB	Power Distribution Board
PEF	Platform Event Filtering
PERR	Parity Error
PET	Platform Even Trap
PIO	Programmable I/O
PMB	Private Management Bus
PMC	Platform Management Controller
PME	Power Management Event
PnP	Plug and Play
POST	Power-on Self Test
PWM	Pulse-Width Modulator
RAIDIOS	RAID I/O Steering
RAM	Random Access Memory
RI	Ring Indicate
RISC	Reduced instruction set computing
RMCP	Remote Management Control Protocol
ROM	Read Only Memory
RTC	Real Time Clock
SAF-TE	SCSI Accessed Fault-Tolerant Enclosure Specification
SBE	Single-Bit Error
SCI	System Configuration Interrupt

Term	Definition
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic RAM
SEL	System event log
SERIRQ	Serialized Interrupt Requests
SERR	System Error
SM	Server Management
SMI	Server management interrupt. SMI is the highest priority nonmaskable interrupt
SMM	System Management Mode
SMS	System Management Software
SNMP	Simple Network Management Protocol
SPD	Serial Presence Detect
SSI	Server Standards Infrastructure
SSU	Server Setup Utility
TPS	Technical Product Specification
UART	Universal asynchronous receiver and transmitter
USB	Universal Serial Bus
VGA	Video Graphic Adapter
VID	Voltage Identification
VRM	Voltage Regulator Module
Word	16-bit quantity
ZCR	Zero Channel RAID

Reference Documents

Refer to the following documents for additional information:

- *PCI Local Bus Specification* Revision 2.1

- *ATI RAGE XL Graphics Controller Specifications, Technical Reference Manual*, Rev 2.01

- SCB2 Hardware External Product Specification rev 1.0

- SCB2 Server Management External Architecture Specification rev 0.92

- SCB2 BIOS External Product Specification rev 1.0

- SCB2 Baseboard Management Controller External Product Specification rev 0.9

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