Enterprise Server Group
Intel R440FX UP Server

Technical Product Specification

Order Number 282958-001
October 1, 1996

The R440FX baseboard may contain design defects or errors known as errata. Characterized errata that may cause the R440FX baseboard's behavior to deviate from published specifications are documented in the R440FX Board Set Specification Update.

Revision History

Revision	Revision History	Date
Rev 0.9	Preliminary release of the R440FX UP Server Board Set Technical Product Specification	7/96

This product specification applies only to standard R440FX UP Server board set with BIOS identifier DM0. Information in this version of the summary applies to the BIOS 1.00.01 DM0. Different versions of the BIOS may look and behave differently.

Changes to this summary will be published in the R440FX UP Server Board Set Specification Update before being incorporated as a revision to this document.

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1. Board Set Description

1.1 Overview

The R440FX UP Server is a high integration uni-processing server providing an affordable entry-level path to Pentium® Pro processor-based performance. The R440FX UP Server system architecture uses a single motherboard based on the Pentium Pro microprocessor and Intel 82440FX chipset. The motherboard for the R440FX UP Server contains the processor, ECC memory, and PCI and ISA I/O systems (with embedded devices for video, network, and disk control). Featured subsystems and devices include:

- System design based on the Intel 82440FX chipset
- Support for up to 512MB of ECC memory using four 72-bit dual inline memory module (DIMM) devices. Support for Double sided DIMMs will provide support for up to 1GB of memory
- PCI I/O system, compliant with revision 2.1 of the PCI specification (5V signaling environment only), with three expansion slots, and embedded SCSI, IDE, Video, and LAN controllers
- ISA I/O system with two expansion slots and embedded PC-compatibility I/O support (serial, parallel, mouse, and keyboard)
- Server management features, including thermal/voltage monitoring and error handling
- Universal Serial Bus (USB) currently not implemented
- Flash BIOS support for all of the above
- Standard ATX form-factor motherboard, which fits into most ATX and AT compatible chassis (e.g. Galileo and Columbus-II)
- Single ZIF socket for installation of the Pentium Pro processor
- Onboard DC-to-DC converter for processor power
- PCI and Memory Controller (PMC) and Data Bus Accelerator (DBX) from 82440FX chipset
- PCI I/O system with three expansion connectors and the following embedded devices: PCI ISA/IDE Accelerator (PIIX3 from the 82440FX chipset) with PCI-to-ISA bridge, PCI IDE interface, and Universal Serial Bus (USB) controller function
- Integrated video, SCSI, and network controllers
- ISA I/O system with two expansion connectors
- National Semiconductor 87308VUL Super I/O chip providing all PC-compatible I/O
- Interrupt control and system management interrupt support
- Server management/monitoring support, and I^2C bus providing an independent communications path for onboard server management controllers.

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1.2 Product Positioning

The market for entry-level server platforms has been rapidly expanding over the last few years. Innovation and increased competition have driven traditional mid-range server features into a market which has been defined primarily by cost-driven consumers purchasing reconfigured desktop PCs. With new products entering the market designed specifically for use as a server, as well as an increasingly educated consumer base, the requirement to provide greater end-user value as well as to differentiate a product from comparative vendors has never been more difficult.

Intel's RC440FX entry server platform has been designed specifically for the cost-driven entry-level server market segment. The RC440FX provides a complete set of onboard controllers for network, disk and video to increase reliability and keep costs in check. Combine the integrated controller approach with Intel's Pentium Pro processor, and you have a powerful entry-level server which can tackle multiple application environments as well as grow with the future needs of consumers.

1.3 Performance Data

Information regarding performance data for the R440FX UP Server will be contained in the R440FX UP Server System Performance. The benchmarks covered in this document are: ServerBench†, NetBench†, WinBench†, Winstone†, and ICOMP® Index Rating.

1.4 Processor Subsystem

The processor subsystem contains the following:

- Pentium Pro processor ZIF socket
- Pentium Pro processor bus with GTL+ termination and termination power supply
- Clock generation
- Onboard DC-to-DC converter for processor power
- Thermal monitor (I^2C slave)

The following figure shows the functional blocks of the processor subsystem:

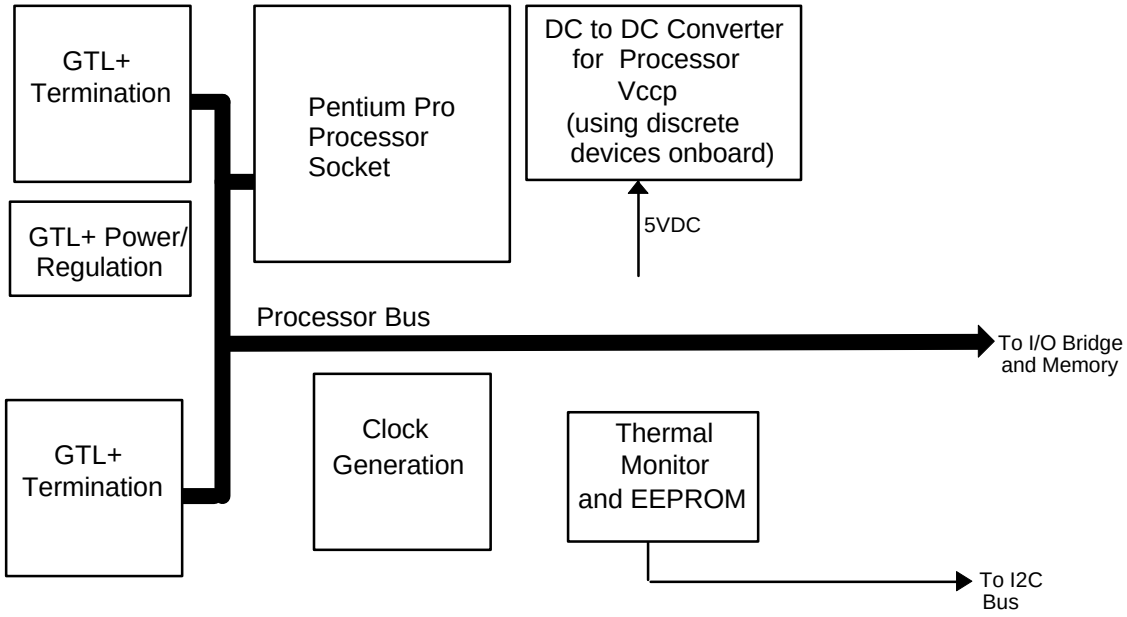

Figure1-1 Processor Subsystem Block Diagram

1.4.1 Pentium® Pro Processor

The Pentium Pro processor is the next generation of Intel architecture microprocessors. Currently, the processor package contains two devices: a CPU core with primary code and data caches (8KB each), and a 256KB secondary cache that communicates with the CPU core via a dedicated internal bus. In the R440FX UP Server, which supports one Pentium Pro processor, none of the local APIC support built into the device is used. Rather, the INTR and NMI pins operate as defined for the non-APIC configuration.

1.4.2 Processor Bus Termination/Regulation/Power

The termination circuitry required by the processor bus (GTL+) signaling environment, and 1.5V termination power is provided by onboard discrete devices. In addition, a DC-to-DC converter provides Vccp power that is derived from the +5V supply using discrete components onboard. The DC-to-DC converter allows the R440FX UP Server to adapt to new processors that may have different voltages.

1.4.3 Processor and PCI Clock Generation

The processor bus (66 MHz or 60 MHz) and PCI bus (33 MHz or 30 MHz) clocks are synthesized from a master clock. The PCI bus clock is replicated and distributed throughout the baseboard, with a copy provided to the PMC, for synchronous PCI operation. An SC3368 device, with low skew outputs, generates 3 copies of the processor clock and 8 copies of the PCI clock for distribution throughout the baseboard. Clock generation and distribution is designed so that the CPU clock leads the PCI clock at the PMC (as required by the PMC EDS).

The R440FX UP Server clock circuitry supports multiple processor core frequencies. Corresponding PCI and processor bus frequencies are shown in the following table.

Table1-1 Supported Clock and Bus Frequencies

Core Clock	Processor Bus Clock	PCI Clock
166 MHz	66 MHz	33 MHz
180 MHz**	60 MHz	30 MHz
200 MHz	66 MHz	33 MHz

**The 180 MHz frequency is available but is not tested or validated.

1.4.4 Thermal Monitor

The I^2C server management bus supports onboard thermal monitor devices for non-volatile storage of vital information. The processor temperature is monitored for the processor subsystem. Refer to the Server Management section later in this chapter for more information.

1.5 PCI Bridge and Memory Subsystem

All high-speed interconnections between the processor bus, PCI host bridge, and system memory are contained within a functional block, which contains the following:

- A PCI host bridge,
- A memory controller,
- Four DIMM sites capable of supporting up to 512MB of memory with single-banked DIMMs, or up to 1GB of memory using double-banked DIMMs.

1.5.1 PCI Host Bridge

The PMC and the DBX form the PCI host bridge for the R440FX UP Server. The host bridge supports the Pentium Pro processor at a bus frequency of up to 66 MHz, with 32-bit addressing, optimized 4-deep in-order and request queue (IOQ), dynamic deferred transaction support, and USWC[1] support. The host bridge translates address and data operations from the GTL+ signaling environment on the processor bus, to a 5V signaling environment that is PCI Rev. 2.1 compliant. Arbitration for PCI bus master access is handled by the PMC.

The PCI interface provides greater than 100MB/s data streaming for PCI to DRAM accesses while also supporting concurrent processor bus and PCI bus transactions to main memory. This is done using extensive data buffering with processor-to-DRAM and PCI-to-DRAM write data buffering and write-combining support for processor-to-PCI burst writes. Arbitration for PCI bus access is handled by the PMC for all PCI masters.

The host bridge also supports system management mode (SMM).

1.5.2 Memory Controller

The PMC also serves as the memory controller for the R440FX UP Server. The DBX provides a 72-bit non-interleaved pathway to main memory. Total installed memory from 8MB to 1GB is supported, using up to four DIMMs (single or double banked). The memory controller supports FPM and EDO DRAM.

ECC detects and corrects single-bit errors (SED/SEC) and detects all double-bit and some multiple-bit errors (DED). The R440FX UP Server does not support ECC on processor signals or parity checking; only memory ECC is supported. On power-up, ECC is disabled.

1.5.3 DRAM Array

The memory controller can automatically detect and initialize the memory array, depending upon the type, size, and speed of installed DIMM devices. Memory is partitioned as four banks of DRAM DIMMs, each providing 72-bits of non-interleaved memory: 64-bit main memory plus ECC. Two row address strobe (RAS) signals are provided for each DIMM. When using single banked DIMMs, one of the RAS lines is connected to both 36-bit “halves” of the DIMM. When using double-banked (a.k.a. quad RAS) DIMMs, both RAS lines are connected to two 36-bit “quarters” of the DIMM.

DIMM sockets can be populated in any order, and DIMM size can be mixed if necessary, although mixing is not recommended. Total installed memory is automatically sized, allocated by the PMC, and reported to the system via configuration registers. The following figure shows the correspondence between installed DIMMs, PMC RASn signals and DRAM row boundary (DRB) register values.

System memory begins at address 0 and is continuous (flat addressing) up to the maximum amount of DRAM installed. The only places where system memory is non-contiguous is in the ranges that are defined as memory holes using configuration registers.

Memory can be partitioned into regions with memory attributes. The regions are defined by configuration registers in the PMC. Regions may have read and write attributes assigned to them.

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[1] Uncacheable, speculatable, write-combining reads, useful for applications such as frame buffers. Refer to the *Pentium Pro External Bus Specification* for more information.

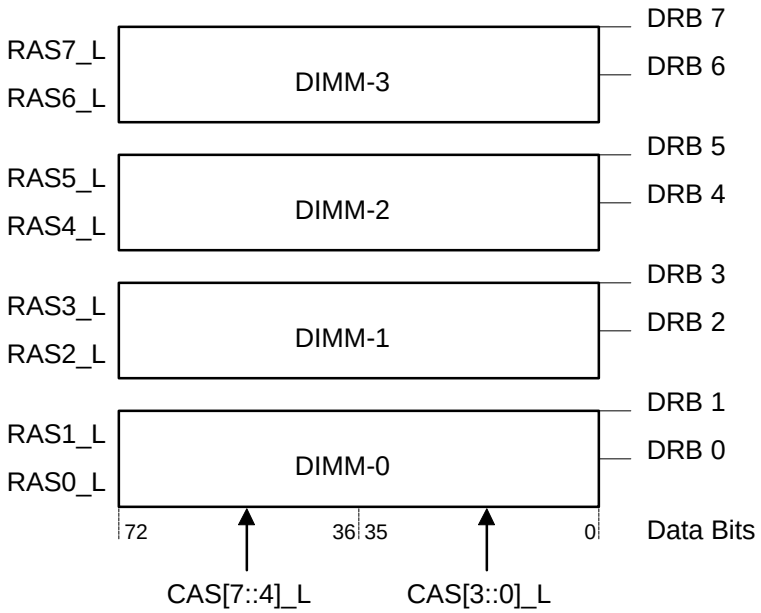

Figure1-2 DRAM DIMM, RASn, CASn, and DRAM Row Boundaries

1.6 PCI I/O Subsystem

All I/O for the R440FX UP Server is on the PCI bus, including PCI and PC-compatible I/O. The PCI bus supports the following embedded devices and connectors:

- Three 120-pin PCI expansion slot connectors
- PIIX3 PCI-to-ISA bridge and IDE controller subsystem
- Adaptec 7880 SCSI host adapter
- Intel 82557 PCI Fast Ethernet controller
- Cirrus Logic-GD54M40 VGA controller

Each device has its IDSEL signal connected to one bit out of AD[31::11] at the PMC. The IDSEL line acts as a chip select on the PCI bus during configuration cycles. The following table shows the AD bit to which each IDSEL signal is attached, and the corresponding device. The onboard SCSI device has been placed in between PCI slots 1 and 2, allowing the end user to choose to boot from an onboard device or an off board device: A hard disk controller in PCI slot 1 will be scanned before the onboard SCSI, while a hard disk controller in PCI slots 2 or 3 will be scanned after the onboard SCSI.

Table1-2 PCI Configuration IDs

IDSEL Value	Device
21	i82557 NIC
23	PCI Slot 1
24	AIC-7880 SCSI
25	PCI Slot 2
26	PCI Slot 3
29	PIIX3
31	CL-GD54M40 Video

1.6.1 PCI Arbitration

PCI supports six PCI masters that arbitrate for PCI access using PMC resources. Note that the onboard video controller is always a PCI slave, and therefore requires no arbitration connection.

1.6.2 PCI-to-ISA/IDE/USB Subsystem

The PIIX3, a multi-function PCI device of the 82440FX chipset, implements three PCI functions: PCI-to-ISA bridge, PCI IDE interface, and PCI USB controller. The PIIX3 provides the gateway to all PC-compatible I/O devices and features. Each function of the PIIX3 has its own set of registers, and once they are configured, they are recognized as distinct hardware controllers sharing the same PCI bus interface.

R440FX UP Server architecture uses the following PIIX3 functional blocks:

- PCI interface
- ISA bus interface
- IDE interface
- Universal Serial Bus (USB) interface (not implemented)
- System reset control
- ISA-compatible interrupt control and PCI interrupt steering
- PC-compatible timer/counters and DMA controllers
- Motherboard plug-n-play support
- System power management features

Following are descriptions of each functional block and related connector pin-outs. For complete information refer to the *PCI ISA IDE Xcelerator EDS*

1.6.2.1 PCI Interface

The PIIX3 implements a 32-bit PCI master/slave interface in accordance with the *PCI Local Bus Specification, Rev. 2.1*. On the R440FX UP Server, the PCI interface operates at up to 33 MHz, using the 5V signaling environment.

1.6.2.2 ISA Interface

A PCI-to-ISA bridge is provided as one of the PIIX3 functions. The PIIX3 provides an ISA bus interface that operates at up to 8.33 MHz and supports two ISA connectors, Flash memory, National Super I/O chip, and baseboard management controller ISA interface ASIC. Refer to “ISA I/O Subsystem”, and “Server Management” later in this chapter, for more information.

1.6.2.3 IDE Interface

The PIIX3 acts as a PCI-based Fast IDE controller that supports PIO and bus master IDE operations, Modes 0 - 4 timings, transfer rates to 22MB/s, buffering for PCI/IDE burst transfers, and master/slave IDE mode. The PIIX3 supports two IDE channels (primary and secondary), each with two drives (Master and Slave).

The R440FX UP Server provides two 40 pin (2 x 20) IDE connectors, one for each channel.

For proper IDE operation, note the cable length specified in the following figure. If no drives are present on an IDE channel, the cable must be removed. If only one drive is installed, it must appear at the end of the cable.

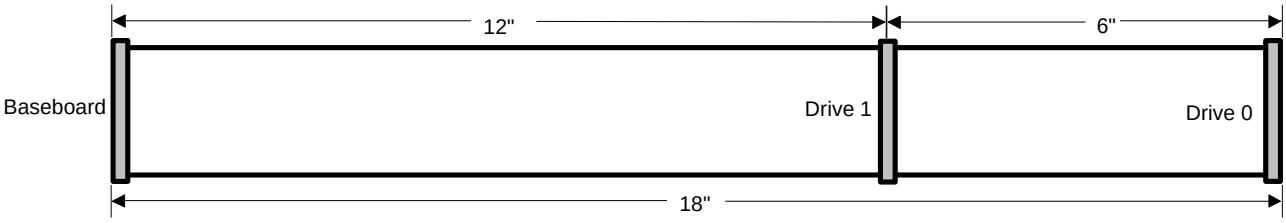

Figure1-3 IDE Cable Requirements

NOTE: *18" is the maximum total length for IDE cables.*

1.6.3 Boot Order

The system boot architecture was designed to allow for an add-in boot device. If this add-in device is installed in the PCI Slot 1 it will have a higher boot priority than the onboard SCSI device. The following table gives the boot sequence:

Table1-3 Boot Order

Boot Order	Device
1	Onboard IDE
2	PCI Slot 1 (Add-in Boot device)
3	Onboard AIC-7880 SCSI
4	PCI Slot 2
5	PCI Slot 3

1.6.3.1 USB Interface

The PIIX3 contains a PCI USB controller that supports two USB ports. The R440FX UP Server provides a stacked dual-USB connector interface as defined by the *USB Specification, Revision 0.9*. An interrupt signal is internally ORed with a PCI interrupt (PCI_INTA) for use in USB transactions.

On the R440FX UP Server, PIIX3 USB controller PCI configuration is provided as Function 2 on the PIIX3 device. At initial release this device will not be active, nor will it have a connector and components on the baseboard

1.6.3.2 Interrupt Control

The PIIX3 provides the functionality of two 82C59 PIC devices for ISA-compatible interrupt handling. The PIIX3 also performs PCI interrupt steering, which is controlled using PCI configuration registers. PCI interrupts (PCI_INTn) from PCI slots, onboard devices, and internal sources in the PIIX3 are routed by the PIIX3 to compatibility interrupts.

The PIIX3 and Super I/O (87308VUL) contain configuration registers that determine which interrupt source drives an interrupt pin. The PIIX3 controls PCI_INTn to IRQ mapping, and the 87308VUL controls which embedded function or device maps to an IRQ.

NMI, PERR, SERR, and other server management error events are routed to SMI and NMI via custom control logic. This logic is contained in the DISMIC, which is the ASIC that provides the ISA interface for the baseboard server management controller. This SMI control logic presents error signals from various sources on the R440FX UP Server that normally produce an NMI as SMI, and emulates SMI events as compatible NMI events. This logic, in combination with baseboard server management features, provides control of how NMI and SMI are asserted under various fatal error conditions. Refer to “Server Management” later in this chapter for more information. The following figure illustrates the interrupt connections on the R440FX UP Server, between the PIIX3 and 87308VUL.

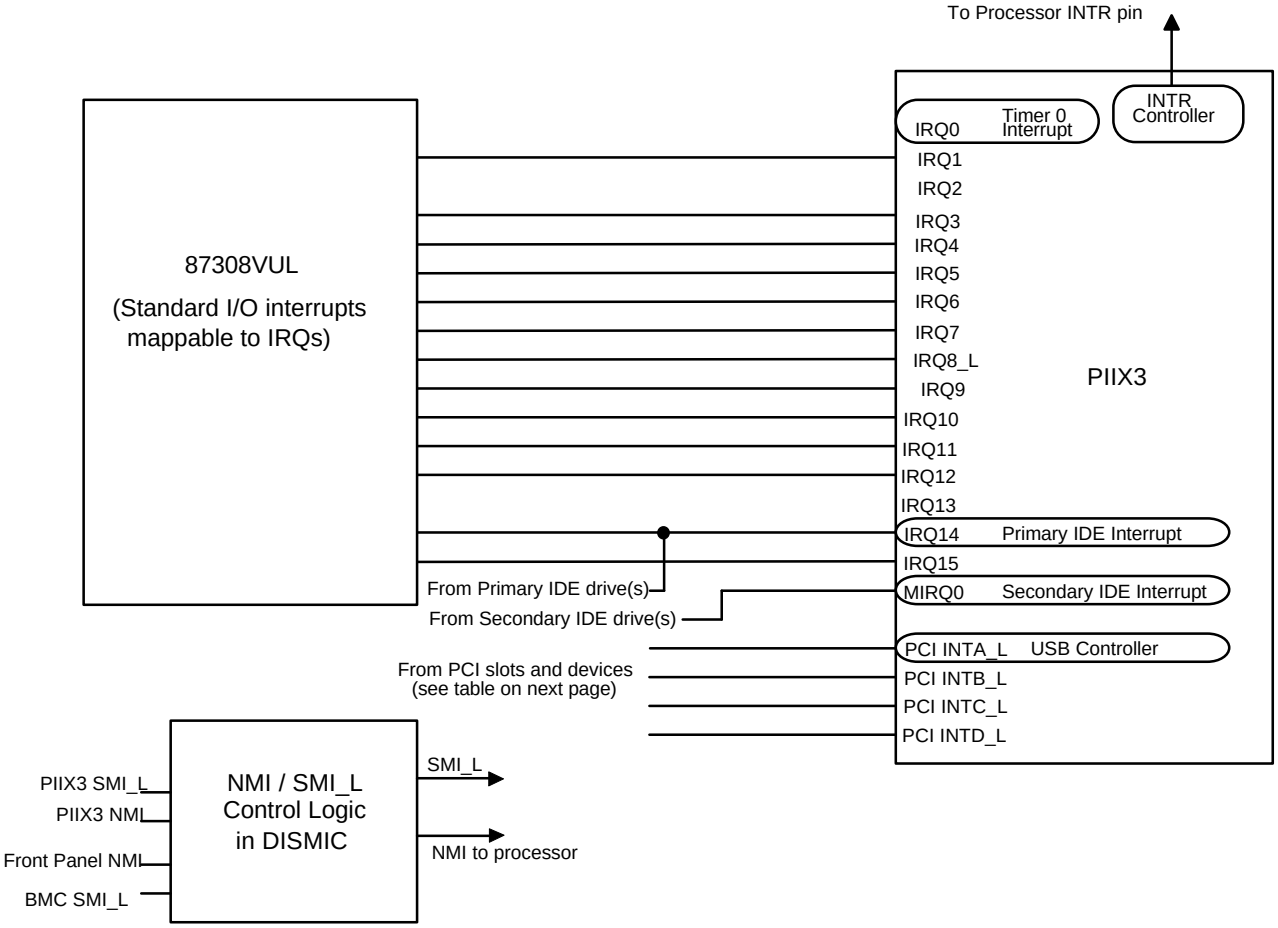

Figure1-4 Interrupt Connections

1.6.3.3 Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on the R440FX UP Server. The actual interrupt map is defined using configuration registers in the PIIX3 and 87308VUL.

The PCI interrupts are hard-wired into the PIIX3, where they must be steered to one of the ISA IRQ lines. Since there are more devices and slots than PCI interrupts, embedded devices must share interrupts with expansion slots. Assuming that most PCI add-in cards use the interrupt signal PCI_INTA on their connectors, this signal is wired to PCI_INTA in slot 1, PCI_INTD in slot 2, and PCI_INTC in slot 3. This makes it less likely that the onboard LAN controller, which is sensitive to interrupt latencies, would share PCI_INTB with an add-in card.

Table1-4 Interrupt Definitions

Interrupt	Description
INTR	Processor interrupt
NMI	NMI from DISMIC to processor
IRQ1	RTC
IRQ3	Serial port A or B interrupt from 87308VUL device, user-configurable.
IRQ4	Serial port A or B interrupt from 87308VUL device, user-configurable.
IRQ5	Parallel port
IRQ6	Floppy disk
IRQ7	Parallel port
IRQ8	
IRQ9	
IRQ10	
IRQ11	
IRQ12	Keyboard/mouse interrupt from 87308VUL
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	
MIRQ0	Additional IDE interrupt from secondary channel IDE devices 0 and 1
PCI_INTA	PCI Interrupt signal A to PIIX3. Wired to USB controller (internal to PIIX3), PCI slot 1 INTA, PCI slot 2 INTB, PCI slot 3 INTC
PCI_INTB	PCI Interrupt signal B to PIIX3. Wired to onboard LAN controller, PCI slot 1 INTB, PCI slot 2 INTC, PCI slot 3 INTD.
PCI_INTC	PCI Interrupt signal C to PIIX3. Wired to onboard SCSI controller, PCI slot 1 INTC, slot 2 INTD, PCI slot 3 INTA.
PCI_INTD	PCI Interrupt signal D to PIIX3. Wired to PCI slot 1 INTD, PCI slot 2 INTA, PCI slot 3 INTB
SMI	System Management Interrupt. General-purpose error indicator that provides an SMI from non-traditional error sources (PERR, SERR, and others).

Note: The onboard Cirrus Logic does not have an interrupt line connected.

1.6.4 SCSI Subsystem

The Adaptec AIC-7880 is the embedded SCSI host adapter provided by the R440FX UP Server. The AIC-7880 contains a Fast-20 SCSI controller and full-featured PCI bus master interface. The AIC-7880 supports either 8- or 16-bit Fast SCSI providing 10MB/s or 20MB/s throughput, or Fast-20 SCSI that can burst data at 20MB/s or 40MB/s. As a PCI 2.1 bus master, the AIC-7880 supports burst data transfers on PCI up to the maximum rate of 133MB/sec using the on-chip 256 byte FIFO.

1.6.4.1 Adaptec AIC-7880† PCI Signals

The Adaptec AIC-7880 supports all of the required 32-bit PCI signals, including the PERR and SERR functions. Full PCI parity is maintained on the entire data path through the chip. The device also takes advantage of PCI interrupt signaling capability, which is hardwired to PCI_INTC on the R440FX UP Server.

1.6.4.2 Supported PCI Commands

The extensions to memory commands (memory read multiple, memory read line, and memory write and invalidate) work with the cache line size register to give the cache controller advance knowledge of the minimum amount of data to expect. The decision to use either the memory read line or memory read multiple commands is determined by a bit in the configuration space command register for this device.

1.6.5 PCI Video

The R440FX UP Server uses the next generation of integrated video controller and support circuitry. It contains the Cirrus Logic CL-GD54M40† 32-bit VGA Graphics Accelerator chip with an SVGA video controller, Clock Generator, and 80 MHz RAMDAC. One 256K x 16 DRAM chip provides 512KB of 60ns video memory, with optional expansion to 1MB for improved performance and more video modes. The Cirrus Logic CL-GD54M40 supports a variety of modes: up to 1280 x 1024 resolution, and up to 64K colors.

This SVGA subsystem supports analog VGA monitors, single and multi-frequency, interlaced and non-interlaced, up to 87 Hz vertical retrace frequency. The connector is a standard 15 pin VGA connector.

1.6.5.1 Video Chip PCI Signals

The Cirrus Logic CL-GD54M40 supports a minimal set of 32-bit PCI signals since it never acts as a PCI master. As a PCI slave, the device requires no arbitration connections. Additionally, the PCI interrupt pin on the device is not connected on the R440FX UP Server.

1.6.5.2 Video Modes

The Cirrus Logic CL-GD54M40 provides all standard IBM™ VGA modes. With 1MB of video memory, the standard R440FX UP Server goes beyond standard VGA support.

Table1-5 Standard VGA Modes

Mode(s) in Hex	Colors (number /palette size)	Resolution	Pixel Freq. (MHz)	Horizontal. Freq. (kHz)	Vertical. Freq. (Hz)
0, 1	16/256K	360 X 400	14	31.5	70
2, 3	16/256K	720 X 400	28	31.5	70
4, 5	4/256K	320 X 200	12.5	31.5	70
6	2/256K	640 X 200	25	31.5	70
7	Mono	720 X 400	28	31.5	70
D	16/256K	320 X 200	12.5	31.5	70
E	16/256K	640 X 200	25	31.5	70
F	Mono	640 X 350	25	31.5	70
10	16/256K	640 X 350	25	31.5	70
11	2/256K	640 X 480	25	31.5	60
12	16/256K	640 X 480	25	31.5	60
12+	16/256K	640 X 480	31.5	37.5	75
13	256/256K	320 X 200	12.5	31.5	70

Table1-6 Extended VGA Modes

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horizontal. Freq. (kHz)	Vertical. Freq. (Hz)
14, 55	16/256K	1056 X 400	41.5	31.5	70
54	16/256K	1056 X 350	41.5	31.5	70
58, 6A	16/256K	800 X 600	40	37.8	60
58, 6A	16/256K	800 X 600	49.5	46.9	75
5C	256/256K	800 X 600	36	35.2	56
5C	256/256K	800 X 600	40	37.9	60
5C	256/256K	800 X 600	49.5	46.9	75
5D	16/256K (interlaced)	1024 X 768	44.9	35.5	87
5D	16/256K	1024 X 768	65	48.3	60
5D	16/256K	1024 X 768	75	56	70
5D	16/256K	1024 X 768	78.7	60	75
5F	256/256K	640 X 480	25	31.5	60
5F	256/256K	640 X 480	31.5	37.5	75
60*	256/256K (interlaced)	1024 X 768	44.9	35.5	87
60*	256/256K	1024 X 768	65	48.3	60
60*	256/256K	1024 X 768	75	56	70
60*	256/256K	1024 X 768	78.7	60	75
64*	64K	640 X 480	25	31.5	60
64*	64K	640 X 480	31.5	37.5	75
65*	64K	800 X 600	36	35.2	56
65*	64K	800 X 600	40	37.8	60
65*	64K	800 X 600	49.5	46.9	75
66*	32K Direct/256 Mixed	640 X 480	25	31.5	60
66*	32K Direct/256 Mixed	640 X 480	31.5	37.5	75
67*	32K Direct/256 Mixed	800 X 600	40	37.8	60
67*	32K Direct/256 Mixed	800 X 600	49.5	46.9	75
6C*	16/256K (interlaced)	1280 X 1024	75	48	87

* Requires 1MB video memory option.

For more information refer to the *Cirrus Logic CL-GD54M40 Advance Product Bulletin*

1.6.5.3 Video DRAM

Video DRAM memory can be upgraded using one 256K x 16, 60 ns, SOJ component. Unlike the system DRAM, we do not qualify video DRAM vendors. The examples below have been used and have no known issues with the R440FX UP Server baseboard.

Table 7-12 Video DRAM Vendors

Manufacturer	Part Number
Samsung	KM416C256AJ-6T
Micron Technology	MR4C1625DJ-6TR
Samsung	KM416C256BJ-6T
Siemens Corp.	HYB514171BJ-60
Hyundai	HY514260BJC-60
Oki Semiconductor	M514260BSL-60J

Contact your local sales office to obtain the latest specifications before placing your order.

1.7 Network Interface Controller (NIC)

The R440FX UP Server supports a 10Base-T/100Base-TX network subsystem that is based on the Intel 82557 Fast Ethernet PCI Bus Controller. The following diagram illustrates the architecture of the network controller subsystem:

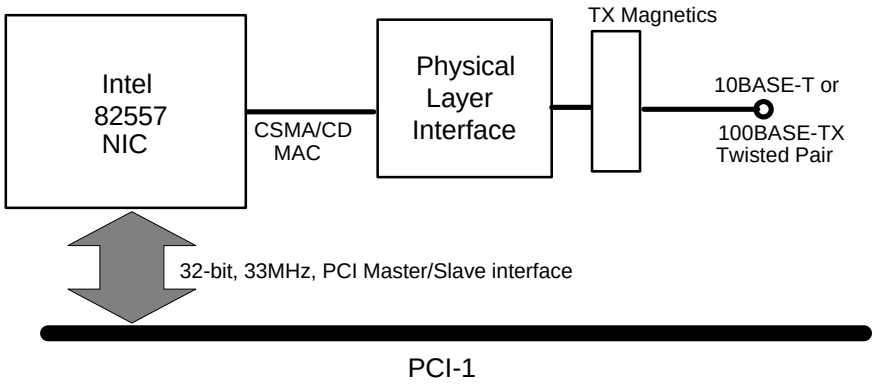

Figure1-5 Network Controller Subsystem

The Intel 82557 is a highly integrated PCI LAN controller for 10 or 100Mbps fast ethernet networks. As a PCI bus master, the Intel 82557 can burst data at up to 132MB/s. This high-performance bus master interface can eliminate the intermediate copy step in Receive and Transmit frame copies, which allows for faster frame processing. The network OS communicates with the Intel 82557 using a memory-mapped I/O interface, PCI_INTB, and two large receive and transmit FIFOs, which prevent data overruns or underruns while waiting for access to the PCI bus. They also enable back-to-back frame transmission within the minimum 960ns inter-frame spacing.

1.7.1.1 Supported Network Features

The Intel 82557 contains an IEEE MII compliant interface to the components needed for an IEEE 802.3 100Base-TX network connection. The R440FX UP Server supports the following features of the Intel 82557 controller:

- Glueless 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with PCI Bus Specification, revision 2.1
- Chained memory structure similar to Intel 82596 LAN controller, with improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- On-chip counters for network management
- Autodetect and autoswitching for a 10Mbps or 100Mbps network speed
- Support for both 10Mbps and 100Mbps networks, full or half duplex-capable, with back-to-back transmit at 100Mbps
- A magnetic component that terminates the 100Base-TX connector interface
- Support for the DP83840 to switch between 10Mbps and 100Mbps operation
- A Flash device that stores the network ID

DP83840 drives LEDs to indicate status as follows: transmit/receive activity on the LAN, valid link to the LAN, and 10/100Mbps operation. These LED's are visible from the back up the machine near the network connections.

1.8 ISA I/O Subsystem

The ISA bus interface on the PIIX3 device supports the following connectors and devices:

- Two ISA connector slots
- Flash memory for BIOS ROM and extensions
- Intel I/O APIC
- National 87308VUL Super I/O chip, in which the R440FX UP Server uses the following:
    - ⇒ Two PC-compatible serial ports
    - ⇒ Enhanced parallel port
    - ⇒ Floppy disk controller (FDC)
    - ⇒ Keyboard/mouse port
    - ⇒ Plug and Play features
    - ⇒ Real-time Clock (RTC)
    - ⇒ General Purpose I/O (GPIO) bits used in server management and miscellaneous functions

1.8.1 ISA Connectors

The R440FX UP Server provides two non-shared full length ISA expansion slots. For the *ISA connector signal pin-outs*, see Appendix B.

1.8.2 Flash ROM

An eight-bit flash memory (Intel 28F004BV) provides 512Kx8 of BIOS and non-volatile storage space, partitioned as shown in the figure below. The Flash device is directly addressed as eight-bit ISA memory.

1.8.3 Flash Memory Map

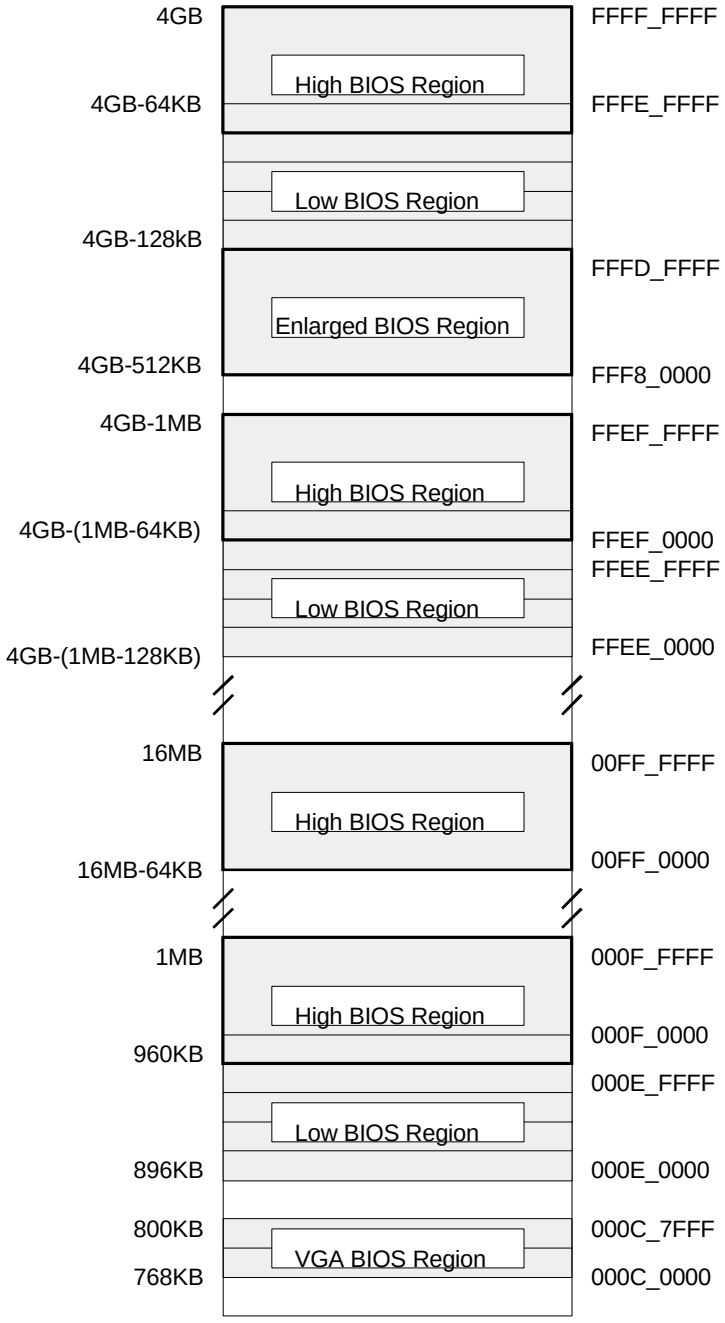

Figure1-6 Flash Memory Map

1.8.3.1 Flash Update Utility Requirements

Flash memory may be loaded from a floppy disk with a Flash update utility. Refer to the *R440FX UP Server BIOS EPS* for more information.

1.8.4 I/O Subsystem

The National Semiconductor 87308VUL Super I/O device contains all of the necessary circuitry to control two serial ports, one IEEE 1284-compatible parallel port, floppy disk, and PS/2-compatible keyboard and mouse. The R440FX UP Server provides connector interfaces for all. The R440FX UP Server uses Plug n Play (PnP) motherboard mode, which provides default values for all registers on power up at a base address that differs from full ISA PnP compliance. Hardware strapping of National 87308VUL signal pins, pulled high or low on the baseboard, determines the operating mode and base address of the device on power up. The National 87308VUL also provides general-purpose I/O (GPIO) bits that power up as inputs. Some of these bits are used by server management hardware and must be properly configured by the BIOS.

1.8.4.1 Serial Ports

One of the two serial port connectors is 9-pin D-Sub type (Serial port A). The other is provided as a 10-pin header (Serial port B).

Each serial port can be set to one of four different COMx ports that can be enabled separately. When enabled, each port can be programmed to generate edge or level sensitive interrupts. When disabled, serial port interrupts are available to add-in cards. For serial port pin-outs, see Appendix B.

1.8.4.2 Parallel Port

The National 87308VUL provides an IEEE 1284-compatible (ECP/EPP) 25-pin bidirectional parallel port. Hardware strapping enables the parallel port and sets the port address and interrupt. When disabled, the interrupt is available to add-in cards.

The 25/15 pin connector stacks the parallel port connector over the VGA and Serial A connectors. For the pin-out information, see Appendix B.

1.8.4.3 Floppy Disk Port

The Floppy Drive Controller (FDC) on the National 87308VUL is functionally compatible with 82077SL, 82077AA, and 8272A floppy disk controllers. All other FDC functions are integrated into the National 87308VUL, including PLL separator and 16-byte FIFO. The R440FX UP Server supports 720KB, 1.2MB, 1.44MB, or 2.88MB floppy drives.

1.9 Server Management

R440FX UP Server Management features are implemented using two microcontrollers and one ASIC:

- Baseboard Management Controller (BMC)
- Front Panel Controller (FPC)
- Distributed Integrated Server Management Interface Chip (DISMIC)

The following diagram illustrates R440FX UP Server management architecture.

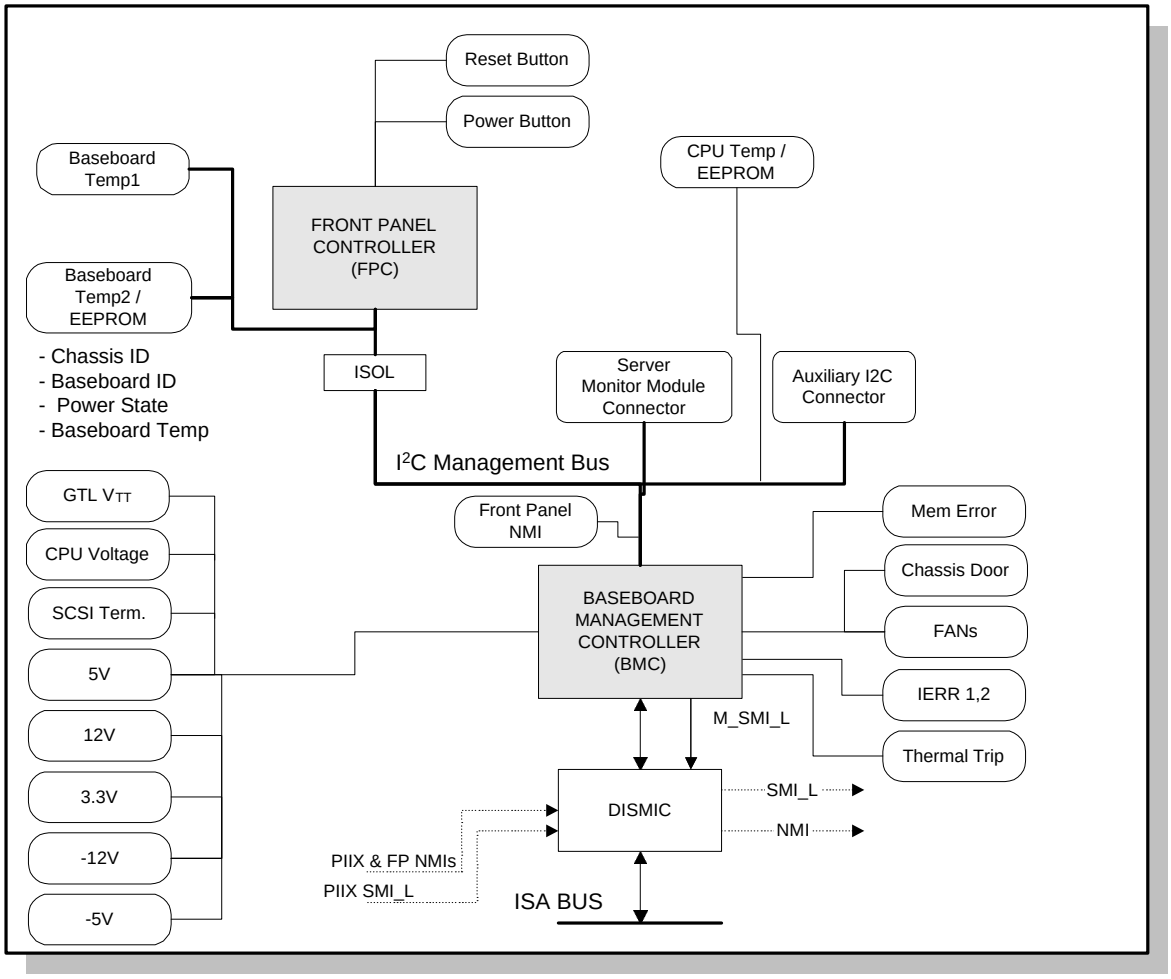

Figure1-7 R440FX UP Server Management Architecture

1.9.1 Baseboard Management Controller (BMC)

The BMC is an 8051-compatible microcontroller located on the baseboard. The BMC monitors baseboard power supply and SCSI termination voltages by using an onboard Analog to Digital Converter (ADC). It also checks the status of the fans, chassis intrusion indicators, and it monitors system temperature sensors using the I^2C management bus. When any monitored parameter is outside defined thresholds, the BMC generates an SMI. The BMC also provides general purpose I/O (GPIO) functions and acts as the primary communication gateway to the FPC, DISMIC, and other I^2C devices in the system chassis.

An EEPROM associated with the baseboard temperature sensor contains the Chassis ID, Baseboard ID, Power State, and Baseboard Temperature during power off conditions. These values are managed by the BMC via I^2C.

1.9.1.1 Processor-related Server Management Functions

The BMC also handles monitoring of processor voltage levels, processor thermal trip and internal error signals, handling of the I^2C thermal sensor located near the processor, and DIMM configuration.

1.9.2 Front Panel Controller (FPC)

The FPC, located on the baseboard, manages system power on/off control, system reset, the front panel NMI button, and an external I^2C interface. The device is powered from the +5V standby power supply to stay alive when system power is off. The FPC controls main power to the baseboard, and is responsible for monitoring all sources of power control both onboard and off board (including the front panel, Server Monitor Module, chassis intrusion, and RTC).

1.9.2.1 I^2C Isolation Buffers

Isolation buffers keep the I^2C bus alive even though the main +5V power supply is unavailable. This allows the FPC to read and write the EEPROM at all times.

1.9.2.2 Standby Power Allocation

The ATX-compatible power supply delivers 10 mA of standby +5V current. The FPC, which is powered by the standby current, is run at a frequency of 3.5 MHz in order to keep the current draw to 4mA or less. The Server Monitor Module can draw up to 1mA from the standby supply. The remaining 5mA of standby current is left for the isolation buffer (74HC4066), power and temperature monitoring, and related pull-up resistors.

When a non-ATX power supply is plugged into the baseboard, the isolation buffer connects a 510 ohm pull-up resistor from the +5V standby to the PS_ON (power supply on) signal. The non-ATX supply provides the additional 10 mA of current required by the 510 ohm pull-up resistor, plus additional current to allow for an LED to be driven from the standby power.

1.9.3 I^2C Management Bus

The I^2C bus facilitates communication between the management controllers by defining a standard protocol for sending and receiving bytes across this network. A byte-level protocol is defined by the *Intelligent Management Bus Communications Protocol Specification*, to which all devices operating on this network must conform.

1.9.4 Distributed Integrated Server Management Interface Chip (DISMIC)

The DISMIC is the mailbox between the BMC and the ISA bus. It facilitates communication between BMC software and SMI or SMS software running on the server. The DISMIC also gates and redirects SMI and NMI by acting as a bridge between the BMC and ISA bus.

1.10 System Reset Control

Reset circuitry is designed to accommodate a variety of ways to reset the system, which can be divided into the following categories:

- Power-up (system) reset
- Programmed (warm) reset
- Soft (keyboard) reset

1.10.1 Power-up Reset

The system power supply asserts POWERGOOD within 400-2000 msec after all voltages have been stabilized. Stable processor power from onboard Vccp occurs 30 to 40 msec after the main Vcc is stable. At this point, power is considered to be up, and power-up reset can proceed.

The FPC controls the P6_PWR_GOOD signal that verifies stable power-up reset conditions to the Pentium Pro processor. The processor is held in reset until P6_POWER_GOOD is asserted, which is when processor clocks are started. On power-up reset, the processor performs the internal BIST. Once the processor has been successfully initialized, the PMC is reset. The system starts once the reset propagates throughout the I/O system.

1.10.2 Programmed Reset

Software can initiate Programmed Reset. Registers in the PMC and PIIX3 provide reset control. Reset can also be initiated by the FPC and BMC, but this is not recommended. For the R440FX UP Server implementation, the 82440FX chipset documentation recommends that the PIIX3 Reset Control register be used for programmed resets.

1.10.3 Soft Reset

Soft resets may be generated by the keyboard controller in the Super I/O chip, PMC, and PIIX3 to DISMIC reset logic, which controls reset delivery to the system. Soft resets preserve all cache contents, but reset the processor bus.

1.11 System Board Jumpers

This section describes jumper options on the R440FX UP Server. A 28-pin single inline header provides 7 3-pin jumper blocks that control various configuration options, as shown in the figure below. The shaded areas show default jumper placement for each configurable option.

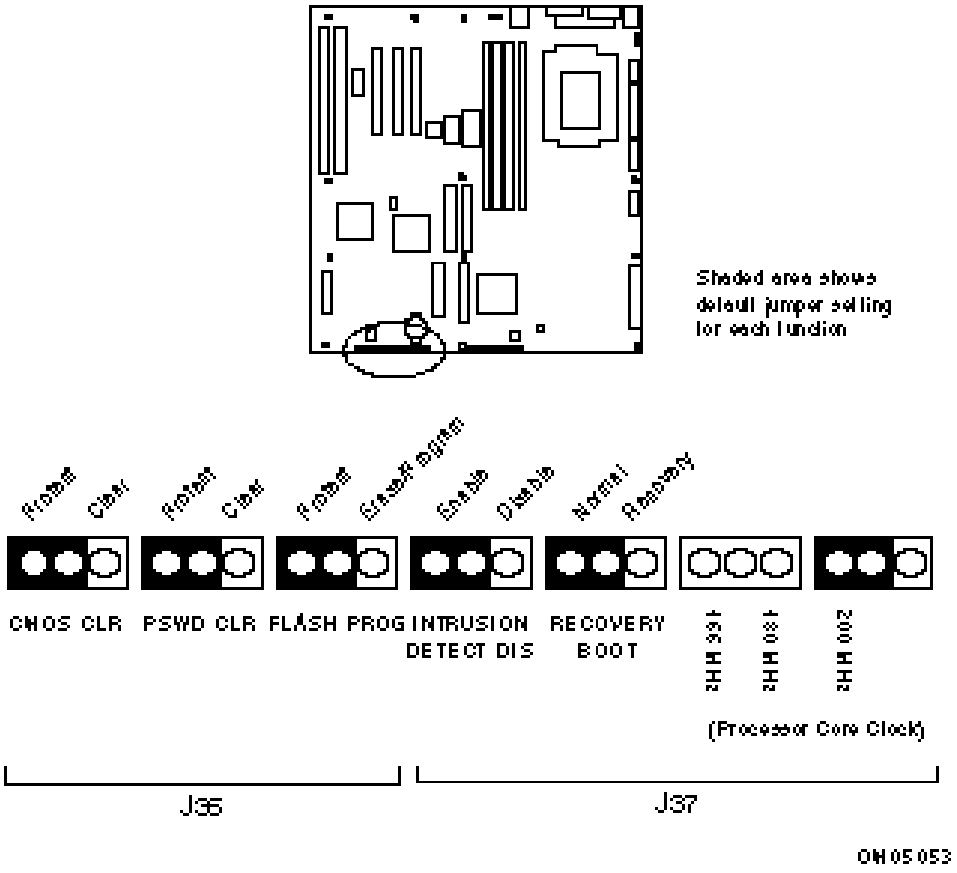

Figure1-8 Configuration Jumpers

Table1-7 Configuration Jumper Options

Function	Pins (default in bold)	What it does at system reset
CMOS clear, J36A	**1-2, Protect**	Preserves the contents of NVRAM.
	2-3, Erase	Replaces the contents of NVRAM with the manufacturing default settings.
Password clear, J36B	**1-2, Protect**	Maintains the current system password.
	2-3, Erase	Clears the password.
Flash program, J36C	**1-2, Protect**	Prevents writing to the BIOS boot block.
	2-3, Erase/Program	Permits boot block erasing and programming. ⚠ **CAUTION** Programming the boot block incorrectly will prevent the system from booting.
Intrusion detection disable, J37D	**1-2, Enable**	Activates intrusion alarm switch on the chassis; the switch then detects and signals when the chassis cover is removed.
	2-3, Disable	Deactivates the intrusion alarm switch.
Recovery boot, J37E	**1-2, Normal Boot**	Allows the system to boot from the normal BIOS.
	2-3, Recovery Boot	Allows the system to boot from the Recovery BIOS if the normal BIOS gets corrupted and you are unable to reload a fresh copy of the BIOS from diskette.
Processor Core Clock, J37F and J37G	J37F 1-2, 166 MHz 2-3, 180 MHz **J37G 1-2, 200 MHz**	Selects the processor core frequency, which in turn determines the operating frequencies of processor and PCI buses.

2. Memory and Other Resource Mappings

2.1 Extended Memory

Extended memory on the R440FX UP Server is defined as all address space greater than 1MB. The Extended Memory region covers 4GB from addresses 0100000h to FFFFFFFFh, as shown in the following figure.

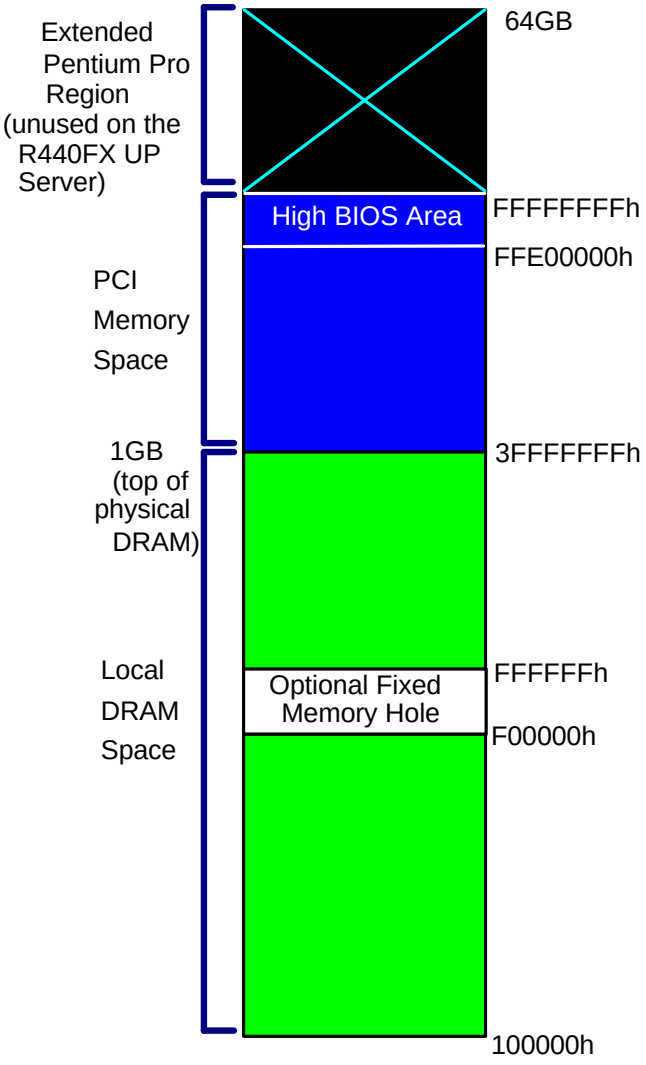

Figure2-1 Extended Memory Map

2.2 I/O Map

The PMC allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including the PIIX3, have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On the R440FX UP Server, the PIIX3 provides the bridge to ISA functions (compatibility bridge).

The I/O map in the following table shows the location in R440FX UP Server I/O space of all directly I/O accessible registers. PCI configuration space registers for each device control mapping in I/O and memory spaces, and other features that may affect the global I/O map. The Super I/O chip contains configuration registers that are accessed through an index and data port mechanism.

Table2-1 R440FX UP Server I/O Map

Address(es)	Resource	Notes
0000h - 000Fh	DMA Controller 1	PIIX3
0020h - 0021h	Interrupt Controller 1	PIIX3
002Eh - 002Fh	Super I/O Index and Data Ports	
0040h - 0043h	Programmable Timer	PIIX3
0060h, 0064h	Keyboard Controller	Keyboard chip select from 87308VUL
0061h	NMI Status & Control Register	PIIX3
0070h	NMI Mask (bit 7) & RTC Address (bits 6:0)	Write Only.
0071h	Real Time Clock (RTC)	RTC chip select from 87308VUL
0080h - 0081h	BIOS Timer	
0080h - 008Fh	DMA Low Page Register	PIIX3
0092h	System Control Port A (PC-AT control Port)	PIIX3 does not alias this port in DMA range.
0094h	Video Display Controller	
00A0h - 00BFh	Interrupt Controller 2	PIIX3
00C0h - 00DFh	DMA Controller 2	PIIX3
00F0h	Clear NPX error	Resets IRQ13
00F8h - 00FFh	x87 Numeric Coprocessor	
0102h	Video Display Controller	
0170h - 0177h	Secondary Fixed Disk Controller (IDE)	
01F0h - 01F7h	Primary Fixed Disk Controller (IDE)	
0200h - 0207h	Game I/O Port	Not used
0220h - 022Fh	Serial Port A	
0238h - 023Fh	Serial Port B	
0278h - 027Fh	Parallel Port 3	
02E8h - 02EFh	Serial Port B	
02F8h - 02FFh	Serial Port B	
0338h - 033Fh	Serial Port B	
0370h - 0375h	Secondary Floppy	
0378h - 037Fh	Parallel Port 2	
03B4h - 03BAh	Monochrome Display Port	
03BCh - 03BFh	Parallel Port 1 (Primary)	

Table2-2 R440FX UP Server I/O Map (cont.)

Address(es)	Resource	Notes
03C0h - 03CFh	Video Display Controller	
03D4h - 03DAh	Color Graphics Controller	
03E8h - 03EFh	Serial Port A	
03F0h - 03F5h	Floppy Disk Controller	
03F6h - 03F7h	Primary IDE	
03F8h - 03FFh	Serial Port A (Primary)	
0400h - 043Fh	DMA Controller 1, Extended Mode Registers.	PIIX3
0461h	Extended NMI / Reset Control	PIIX3
0462h	Software NMI	PIIX3
0480h - 048Fh	DMA High Page Register.	PIIX3
04C0h - 04CFh	DMA Controller 2, High Base Register.	
04D0h - 04D1h	Interrupt Controllers 1 and 2 Control Register.	
04D4h - 04D7h	DMA Controller 2, Extended Mode Register.	
04D8h - 04DFh	Reserved	
04E0h - 04FFh	DMA Channel Stop Registers	
0678h - 067Ah	Parallel Port (ECP)	
0778h - 077Ah	Parallel Port (ECP)	
07BCh - 07BEh	Parallel Port (ECP)	
0800h - 08FFh	NVRAM	
0CA9h	DISMIC Data Register	Server management mailbox registers.
0CAAh	DISMIC Control/Status Register	
0CABh	DISMIC Flags Register	
0C84h	Board Revision Register	
0C85h - 0C86h	BIOS Function Control	
0CF8h	PCI CONFIG_ADDRESS Register	Located in PMC
0CF9h	PMC Turbo and Reset control	PIIX3
0CFCh	PCI CONFIG_DATA Register	Located in PMC
46E8h	Video Display Controller	
xx00 - xx1F*	SCSI device space registers	Refer to SCSI chip document.
xx00 - xxFF*	I/O Mapped NIC registers	Refer to NIC chip document.

*SCSI and LAN I/O base addresses are set using configuration registers.

2.3 PCI Memory Space

Memory addresses from the 1 - 4GB range are mapped to PCI space. This region is divided into two sections; High BIOS and general purpose PCI Memory. The general purpose PCI memory area is typically used for memory mapped I/O to PCI devices. The memory address space for each device is set using PCI configuration registers.

2.4 DMA Channels

Table2-3 DMA Channels

DMA	Slot	Function
2	0	Onboard Floppy Controller
4	0	DMA Controller
7	0	ISA IDE DMA Transfers

2.5 Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on the R440FX UP Server. The actual interrupt map is defined using configuration registers in the PIIX3 and 87308VUL.

The PCI interrupts are hard-wired into the PIIX3 where they must be steered to one of the ISA IRQ lines. Since there are more devices and slots than PCI interrupts, embedded devices must share interrupts with expansion slots. Assuming that most PCI add-in cards use the interrupt signal PCI_INTA_L on their connectors, this signal is wired to PCI_INTA_L in slot 1, PCI_INTD_L in slot 2, and PCI_INTC_L in slot 3. This scheme makes it less likely that the onboard LAN controller, which is sensitive to interrupt latencies, would share PCI_INTB_L with an add-in card.

Table2-4 Interrupt Definitions

Interrupt	Description
INTR	Processor interrupt
NMI	NMI from DISMIC to processor
IRQ1	RTC
IRQ3	Serial port A or B interrupt from 87308VUL device, user-configurable.
IRQ4	Serial port A or B interrupt from 87308VUL device, user-configurable.
IRQ5	Parallel port
IRQ6	Floppy disk
IRQ7	Parallel port
IRQ8	
IRQ9	
IRQ10	
IRQ11	
IRQ12	Keyboard/mouse interrupt from 87308VUL
IRQ14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	
MIRQ0	Additional IDE interrupt from secondary channel IDE devices 0 and 1
PCI_INTA	PCI Interrupt signal A to PIIX3. Wired to PCI slot 1 INTA, PCI slot 2 INTB, PCI slot 3 INTC
PCI_INTB	PCI Interrupt signal B to PIIX3. Wired to onboard LAN controller, PCI slot 1 INTB, PCI slot 2 INTC, PCI slot 3 INTD.
PCI_INTC	PCI Interrupt signal C to PIIX3. Wired to onboard SCSI controller, PCI slot 1 INTC, PCI slot 2 INTD, PCI slot 3 INTA.
PCI_INTD	PCI Interrupt signal D to PIIX3. Wired to USB controller (internal to PIIX3), PCI slot 1 INTD, PCI slot 2 INTA, PCI slot 3 INTB
SMI_L	System Management Interrupt. General-purpose error indicator that provides an SMI_L from non-traditional error sources (PERR_L, SERR_L, and others).

3. BIOS, Setup, SCU and SCSISelect™ Utilities

3.1 Overview

The term “BIOS” refers to the following:

- System BIOS, which controls basic system functionality using stored configuration values.
- Configuration Utility (CU), which consists of a Flash ROM-resident setup utility and the system memory-resident System Configuration Utility (SCU) which provides user control of configuration values stored in NVRAM and battery-backed CMOS configuration RAM.
- Flash Memory Update utility (FMUP), which loads pre-defined areas of Flash ROM with Setup, BIOS, and other code/data.

The following figure shows the relationship between BIOS components and register spaces. Unshaded areas are loaded into Flash using FMUP.

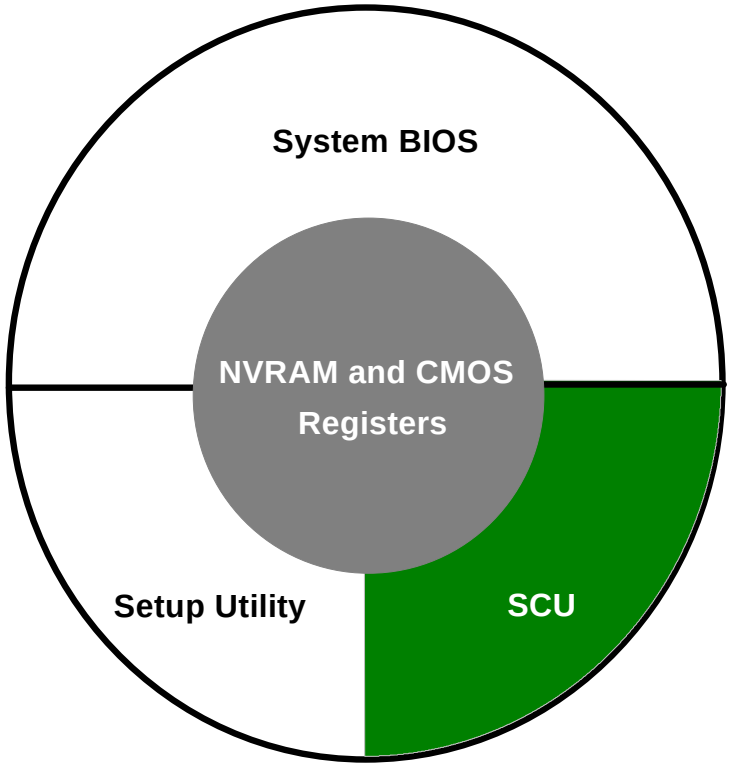

Figure3-1 R440FX UP Server BIOS Architecture

3.2 BIOS

The system BIOS is the core of the Flash ROM-resident portion of the BIOS. The system BIOS provides standard PC-BIOS services. In addition, the system BIOS provides support for these R440FX UP Server-specific features: security features, multiple-speed processor support, logging of critical events, server management features, I^2C support, CMOS configuration RAM defaults, multiple language support, defective DIMM detection and remapping, automatic detection of video adapters, greater than 16MB memory support, PCI BIOS interface, option ROM shadowing, cache state on boot, system information reporting, ECC support, SMI support, user-supplied BIOS support, L2 cache support, ISA support, memory sizing, boot drive sequencing, and resource allocation support.

3.2.1 Configuration Utility

The CU provides the means to configure onboard hardware devices and add-in cards. The CU consists of the following:

- Standard PC-AT Setup utility (a.k.a. Setup), embedded in Flash ROM, for configuration of onboard resources.
- SCU, for configuration of add-in cards, which must be run from a boot media shipped with the system.

3.3 System Configuration Utility (SCU)

The System Configuration Utility (SCU) is the main tool to configure the system or to check or change the configuration. Many system settings can be entered from either the SCU or Setup, but the SCU provides conflict resolution as well as access to information about ISA, ISA Plug and Play, and PCI adapters. The SCU is PCI aware, and it complies with the ISA Plug and Play specifications. The SCU works with any compliant configuration (.CFG) or overlay (.OVL) files supplied by a peripheral device manufacturer.

SYSTEM MUST HAVE A DISKETTE DRIVE *The system must have a diskette drive present and enabled to use the SCU. If a diskette drive is present but is disabled or misconfigured, use the BIOS Setup utility to enable or configure the drive.*

3.3.1 Where the SCU Gets Information

Source	Description
Configuration (.CFG) and overlay (.OVL) files	For the system board, we provide a .CFG file and an .OVL file with the SCU. These files describe the board's characteristics and the system resources required. Some ISA adapters come with a diskette that contains a .CFG file (and an optional .OVL file).
Configuration registers	Information and required resources for PCI and Plug and Play adapters are derived from the adapter's configuration registers.
User selected options	The SCU displays the exact system configuration and the user's current settings by reading ISA CMOS and system nonvolatile storage (NVRAM or flash memory).

Using information from the sources listed above, the SCU stores the system configuration in ISA CMOS and system nonvolatile storage (NVRAM or flash memory).

At Power-On or rebooting, the BIOS POST routines and the Plug and Play Auto Configuration Manager check and configure the hardware. If possible, POST will program the hardware according to the configuration stored by the SCU; if conflicts exist, an error message will be generated. You must then use the SCU to correct the conflict before the system boots.

3.3.2 When to Run the SCU

- When you first set up and configure the system
- If you get a configuration error message at power-on
- Whenever you add, remove, or move an ISA adapter that is not Plug and Play
- Whenever you add or remove memory
- In general, whenever you add hardware to or remove hardware from the system

Running the SCU is also recommended but optional for Plug and Play and PCI adapters.

3.4 SCSI*Select* Utility

The SCSI*Select* utility detects the number of AIC-7880 wide/fast20 SCSI III host adapters in the system. Use the utility to:

- Change default values
- Check or change SCSI device settings that may conflict with those of other devices in the system
- Perform a low-level format on SCSI devices installed in the system

3.4.1 To Start up SCSI*Select*

1. Turn on or reboot the system. During the boot-up process, the following prompt is displayed at the time the SCSI BIOS is loaded:, select from the SCU menu.

   <<< Press <CTRL><A> for SCSISelect™ Utility! >>>

   To enter the SCSI*Select* utility, press <Ctrl-A> when you see the prompt.

2. When the utility appears, choose the bus device that you want to configure.

3.5 Flash Update Utility

The system BIOS, setup utility, and configuration files are resident in partitioned Flash ROM. The device is in-circuit reprogrammable, except for the recovery boot block, which is electrically protected from erasure. A jumper on the baseboard can enable writing to this region.

To reload Flash memory from a floppy disk, a Flash update utility is required. The file to be loaded contains a new copy of BIOS code and a list of supported ISA IDs. The utility must match the ISA ID found at C80h - C83h with one in the load file, and check the baseboard ID. Baseboard revisions may share a common SCU but require different BIOS code.

3.5.1.1 System Flash ROM Layout

The Flash ROM contains system initialization routines, Setup utility, and runtime support routines. The exact layout is subject to change and is determined by Intel. 128KB is reserved for the SCU and associated files, and an 8KB User block is available for user ROM code or custom logos. The complete ROM is visible starting at physical address 4GB less 512KB. The Flash Memory Update utility loads BIOS components to blocks of specified length and location. For more information see the R440FX UP Server BIOS EPS.

3.6 Using Setup and Setup Menu Screens

This section describes the BIOS Setup options. Use Setup to change the system configuration defaults. You can run Setup with or without an operating system being present. Setup stores most of the configuration values in battery-backed CMOS ; the rest of the values are stored in flash memory. The values take effect when you boot the system. POST uses these values to configure the hardware; if the values and the actual hardware do not agree, POST generates an error message. You must then run Setup to specify the correct configuration.

Run Setup: you may run Setup to modify any standard PC AT† system board feature such as:

- Select diskette drive
- Select parallel port
- Select serial port
- Set time/date (to be stored in RTC)
- Configure IDE hard drive
- Specify boot device sequence
- Enable SCSI BIOS Run SCU, not Setup: you must run the SCU instead of Setup to do the following:
- Add or remove any ISA board (Plug and Play board, or ISA board that came out before Plug and Play)
- Enter or change information about a board
- Set system management threshold values
- Alter system resources (such as interrupts, memory addresses, I/O assignments) to user-selected choices instead of choices selected by the BIOS resource manager.

3.6.1 How to Enter and Start Setup

You can enter and start Setup under these conditions:

- When you turn on the system, after POST completes the memory test
- When you reset the system by pressing <Ctrl+Alt+Del> while at the MS-DOS operating system prompt
- After you have moved the CMOS jumper on the system board to the “Clear” position (enabled)
- After CMOS/NVRAM has been corrupted In each case, you will see this prompt:

  Press F1 key if you want to run SETUP

  If the <F1> prompt has been disabled

  If the <F1> prompt has been disabled, to enter Setup you must press <F1> as soon as the display comes up.

Setup has four major menus and several submenus:

⇒ Main Menu

⇒ Advanced Menu

Peripheral Configuration

Advanced Chipset Configuration

Plug and Play Configuration

⇒ Security Menu

Set User Password

Set Administrative Password

⇒ Exit Menu

To navigate the menus:	**Press**
Get help about an item	<F1>
Go back to a previous item	<Esc>
Select an item or display a submenu	<Enter>
Go to previous item	↑
Go to next Item	↓
Move between menus	← →
Reset to Setup defaults	<F5>
Return to previous values	<F6>
Save and exit Setup	<F10>

When you see this on the screen:	What it means
On screen, an option is shown but you cannot select it or move to that field.	You cannot change or configure the option in that menu screen. Either the option is autoconfigured or autodetected, or you must use a different Setup screen, or you must use the SCU.
On screen, the phrase Press Enter appears next to the option.	Press <Enter> to display a submenu that is either a separate full-screen menu or a small pop-up menu with one or more choices.

Keep track of your changes from the defaults. As you work through the Setup menus, keep track of the options you choose. You could circle them or write the values in the pages in this section. Then, if the default values ever need to be restored to CMOS (after a CMOS-clear, for example), you'll have your notes to make setup easier.

3.7 SCSI Interface

The AIC-7880 offers 8-bit or 16-bit SCSI operation at data transfer rates of up to 10, 20, or 40MB/s. The 7880 also offers active negation outputs, controls for external differential transceivers, a disk activity output, and a SCSI terminator power down control. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus, thereby avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48 mA single-ended SCSI bus with no additional drivers (the SCSI segment can handle up to 15 devices). SCSI termination power is always on, regardless of the register settings for 7880 SCSI termination power control features. The SCSI controller on the R440FX UP Server always sits at one end of the SCSI bus. This implementation was intended to keep the SCSI channel inside the system and not be exposed to the outside world.

3.7.1 SCSI Bus

The SCSI data bus is 8- or 16-bits wide with odd parity generated per byte. SCSI control signals are the same for either bus width. SCSI P-connector cabling connects easily. To accommodate 8-bit devices on a 16-bit Wide SCSI bus, the AIC-7880 assigns the highest arbitration priority to the low byte of the 16-bit word. This way, 16-bit targets can be mixed with 8-bit targets if the 8-bit devices are placed on the low data byte. For 8-bit mode, the unused high data byte is self-terminated and does not need to be connected. During chip power down, all inputs are disabled to reduce power consumption. In order to support 8-bit devices, a wide-to-narrow adapter is required. The adapter that is supplied in the country kit has load-equalizing circuitry in it so that the 8-bit device appears the same as a 16-bit device. If another adapter is supplied, it needs to be checked to make sure it is the proper device for the application.

For more information on the functional architecture of this device, refer to the *AIC-7880 PCI Bus Master Single-chip SCSI Host Adapter Data Book*

3.7.2 SCSI Termination

It is important that cabling and connections meet the SCSI bus specification. Otherwise, the bus could be unreadable and data corruption could occur or devices may not work at all. The SCSI bus needs to be terminated at the end of the cable, and this is usually provided by the last SCSI device on the cable.

If you are installing a SCSI drive: the system includes a standard 50-pin narrow (8-bit) SCSI ribbon cable that can support up to seven SCSI devices. The system also includes a wide-to-narrow adapter used to connect this cable to the 68-pin wide SCSI connector on the system board. An optional 68-wire wide SCSI cable is also available that will allow the use of up to eight Fast/Wide or Fast-20/Wide (16-bit) SCSI devices with the internal interface.

- **Unique SCSI ID:** A SCSI drive must be assigned a unique SCSI ID. Use the configuration jumpers on the back of the drive to change the ID of the drive. The SCSI microcontroller on the system board is always set to SCSI ID 7.
- **Active termination at end of SCSI bus cable:** Hard drives generally provide active termination; if a SCSI hard drive (presumably in the 3.5-inch internal bay) is the last device, it can terminate the bus.
- **CD-ROM plus other SCSI drives installed:** CD-ROM drives generally do not provide active termination. If a SCSI CD-ROM drive is the last device but other SCSI devices are also installed, a separate active terminator should be installed on the CD-ROM drive.
- **CD-ROM as only SCSI drive installed:** If a CD-ROM drive is the only SCSI device installed, an active terminator is not needed. Such drives usually have resistor packs installed to provide passive SCSI bus termination.

CAUTION

The internal SCSI interface in this system supports only single-ended SCSI devices. Connecting differential SCSI drive types to this interface can result in electrical damage to the system board and peripherals.

Bus termination is needed for SCSI drives

If you install a SCSI cable, you must provide active SCSI bus termination *at the end of the cable* Leaving the cable installed without active termination will violate the SCSI bus specification and will cause the SCSI bus to be unreliable. You must also ensure that termination is removed or disabled in all other drives on the bus.

You can meet the specification by installing, as the last SCSI device on the cable, a drive that includes active bus termination, or by attaching an active termination device onto the end of the cable.

To terminate the SCSI bus:

- If the drive is NOT the last device on the SCSI cable: remove the terminating resistor packs or disable the SCSI IC active terminators, whichever is present on the drive.
- If the drive IS the last device on the SCSI cable: **do not** remove the terminating resistor packs or disable the SCSI IC terminators on the drive. The terminating drive at the end of SCSI bus must be Fast-20 compliant..

4. Error Messages and Beep Codes

4.1 Error Messages and Error Codes

The system BIOS displays error messages on the video screen. Prior to video initialization, beep codes inform you of errors. POST error codes are logged in NVRAM, as well as the Extended BIOS Data area (EBDA).

The BIOS displays POST error codes on the video monitor. The error codes are defined by Intel and whenever possible are backward-compatible with error codes used in the previous platform.

Following are definitions of POST error codes, POST beep codes, and system error messages.

4.1.1 POST Codes and Countdown Codes

The BIOS indicates the current testing phase during POST after the video adapter has been successfully initialized by writing a 2-digit hex code to I/O location 80h. If a Port-80h card (POSTcard™) is installed, it displays this 2-digit code on a pair of hex display LEDs. The current countdown code indicates how far into POST the error occurred. The countdown ranges from 900 to 000 (boot OS).

Table4-1 Port-80h and Countdown Code Definition

Code	Meaning
CP	AMIBIOS check point (port-80) code
XX	Intel AMIBIOS BIOS countdown code

The following table contains the port-80 codes and the POST countdown codes displayed during the recovery boot process. Recovery boot is enabled by moving the jumper at J47 from pins 1 and 2, to pins 2 and 3, and cold-booting the system. The system will boot from the floppy disk in drive A using a recovery BIOS image that is automatically installed.

Table4-2 Recovery BIOS Port-80 and Countdown Codes

CP	XX	Reason
02h		Disable internal cache
08h		Disable DMA controller #1 and #2, disable interrupt controller #1 and #2, and reset video display.
13h		Initialize all chipset registers
15h	900	Initialize system timer
1Bh	800	Real-mode base 64KB memory test
20h	700	16KB base RAM test
23h	650	Setup interrupt vectors
40h	600	Test memory in virtual mode.
65h	500	Initialize 8237 DMA controller
67h	400	8259 interrupt controller test
80h	300	Unmask diskette, Keyboard, and timer interrupts
88h	200	Floppy unit initialization
A0h	100	Cache enable
00h	000	Boot OS.

The following table shows the port-80 codes and countdown codes displayed during POST.

Table4-3 Standard BIOS Port-80 Codes and Countdown Codes

CP	XX	Reason
D0h		Early MP Initialization, enter real big mode
D1h		Power On Initialization
D2h		Disable NMI
D3h		Reset video controller
D4h		Enter real mode
D5h		Checksum the 8KB loader BIOS
D6h		Loader BIOS checksum good
D7h	900	Check if Keyboard Controller (KBC) buffers are free..
D8h		Issue BAT (basic assurance test)command to KBC
D9h		Read BAT results
DAh		Check if KBC passed BAT
DBh	820	Keyboard Initialization Passed
DDh		Disable keyboard and auxiliary devices
DFh		Disable both DMA controllers
E0h	780	Preliminary initialization of PICs
E1h		Enter real big mode and initialize chipset, size memory
E2h		Initialize timer 2 for speaker
E3h	760	Initialize timer channel 0 for system timer.
E4h		Clear any pending parity errors.
E6h	740	Test RAM from 0 - 640KB
E7h		Test and initialize 2MB memory
E8h		RAM failure, remap memory partitions and test again
E9h		RAM test complete, passed. Clear parity errors
EAh	730	Set up stack at 30:100, enable cache and shadow BIOS
EBh		Initialize code dispatcher
ECh		Make F000h DRAM R/W Enabled
EDh		Dispatch POST
23h	700	Initializations before setting up vector table
24h		Setup interrupt vector table
0Dh		Check CMOS clear jumper
0Eh	690	Check validity of CMOS
0Fh		Force CMOS defaults if required
10h		CMOS initialization complete
25h		Nothing
28h		Set monochrome mode
29h		Set color display
2Ah		Clear parity status if any, initialize warm reset flag
2Bh		Video auto-configuration and initialization
F0h		EISA Slot Initialization
F1h		Enable extended NMI sources
F2h		Test extended NMI sources
2Ch	580	Conventional video option ROM search
2Dh		Scan User Binary
2Eh	570	Initialize monochrome display if no other video present
2Fh	560	Test buffer memory for monochrome
30h		Check vertical and horizontal retrace

Table4-4 Standard BIOS Port-80 Codes and Countdown Codes (cont.)

31h		Test for color display memory if no external video BIOS found
CP	**XX**	**Reason**
32h		Check vertical retrace
34h		Sign on message
36h		Initialize Messaging Services and clear screen
37h	500	Custom sign on display
80h	370	KB/mouse port check
81h		KBC initialization and testing
83h		Check if keyboard is locked
F5h	330	Initialize mouse
39h		Keyboard, mouse and other sign-ons
3Bh		Prepare for memory test
43h	290	Decide memory size from chipset
4Fh		Disable cache, test memory and display memory size on screen
52h		Initialize for the other processors in MP system, reset DMA controller
61h	250	DMA register tests
62h		DMA test OK
65h		Initialize 8237 DMA controller
66h		Clear DMA write request register and mask set/reset register
67h	220	8259 Interrupt controller test
F4h		Enable extended NMI sources
8Ch	140	Initialize remaining Plug-n-Play devices (i.e. other than video), initialize IPL, initialize IDE controller
8Fh	130	Floppy Initialization
92h		set printer, RS-232 time-out
96h		Option ROM scan and initialization above C800h
97h	080	Scan User Binary and conventional option ROM scan
98h		Scan User Binary area
9Ah		Clear soft reset flag, complete MP Table
9Dh	070	timer data area initialization
A0h		printer setup
A1h		RS-232 setup
A2h		Check for stuck key
ABh		Before NPX test and initialization
ACh	060	NPX test and initialization
ADh		update coprocessor inf. in CMOS and recalculate checksum
AEh		Set typematic rate
AFh	050	Keyboard read ID command
B0h		Wait for READ ID response
A3h		Display POST errors
A6h		Before Setup
A7h	030	Call Setup if required, prompt for password if enabled
B1h		Enable Cache for boot
B3h		Setup display mode set
B4H		Jump to pre-OS code
BBh	020	Initialize SMI code, prepare for boot
00h	000	Execute BOOT

4.1.2 POST Beep Codes

A beep code is a series of individual beeps on the PC speaker, each of equal length. The following table describes the error conditions associated with each beep code and the corresponding POST checkpoint code as seen by a 'port 80h' card.

Table4-5 BIOS Error Beep Codes

Count	CP	Error Condition
1	71h	Refresh failure
2	72h	Parity can't be reset
3	73h	First 4MB memory failure
4	74h	Timer not operational
5	75h	Processor failure
6	76h	Keyboard controller gate A20 is off (v_mode)
7	77h	Exception interrupt error
8	78h	Display memory R/W error
9	79h	ROM checksum error
10	7Ah	Shutdown register R/W error

4.1.3 POST Error Codes and Messages

The following table defines POST error codes and associated messages.

Table4-6 POST Error Messages and Codes

Code	Error message
0002	Primary Boot Device Not Found
0010	Cache Memory Failure, Do Not Enable Cache
0015	Primary Output Device Not Found
0016	Primary Input Device Not Found
0041	EISA ID Mismatch for Slot
0043	EISA Invalid Configuration for Slot
0044	EISA configuration NOT ASSURED!
0045	EISA Expansion Board Not Ready in Slot
0047	EISA CMOS Configuration Not Set
0048	EISA CMOS Checksum Failure
0049	EISA NVRAM Invalid
0060	Keyboard Is Locked ... Please Unlock It
0070	CMOS Time & Date Not Set
0080	Option ROM has bad checksum
0083	Shadow of PCI ROM Failed
0084	Shadow of EISA ROM Failed
0085	Shadow of ISA ROM Failed
0131	Floppy Drive A:
0132	Floppy Drive B:
0135	Floppy Disk Controller Failure
0140	Shadow of System BIOS Failed
0171	CPU Failure - Slot 1, CPU 1
0172	*N/A for R440FX UP Server* CPU Failure - Slot 1, CPU 2
0173	*N/A for R440FX UP Server* CPU Failure - Slot 2, CPU 1
0174	*N/A for R440FX UP Server* CPU Failure - Slot 2, CPU 2
0171	Previous CPU Failure - Slot 1, CPU 1
0172	*N/A for R440FX UP Server* Previous CPU Failure - Slot 1, CPU 2
0173	*N/A for R440FX UP Server* Previous CPU Failure - Slot 2, CPU 1
0174	*N/A for R440FX UP Server* Previous CPU Failure - Slot 2, CPU 2
0175	*N/A for R440FX UP Server* CPU modules are incompatible
0180	*N/A for R440FX UP Server* Attempting to boot with failed CPU
0191	CMOS Battery Failed
0195	CMOS System Options Not Set
0198	CMOS Checksum Invalid
0289	System Memory Size Mismatch
0295	Address Line Short Detected
0297	Memory Size Decreased
0299	ECC Error Correction failure
0301	ECC Single bit correction failed, Correction Disabled
0302	ECC Double bit Error
0310	ECC Address failure, Partition #
0370	Keyboard Controller Error
0373	Keyboard Stuck Key Detected
0375	Keyboard and Mouse Swapped

Table 4-7 POST Error Messages and Codes (cont.)

Code	Error message
0380	ECC SIMM failure, Board in slot 1 SIMM #
0392	*N/A for R440FX UP Server* ECC SIMM failure, Board in slot 2 SIMM #
0430	Timer Channel 2 Failure
0440	Gate-A20 Failure
0441	Unexpected Interrupt in Protected Mode
0445	Master Interrupt Controller Error
0446	Slave Interrupt Controller Error
0450	Master DMA Controller Error
0451	Slave DMA Controller Error
0452	DMA Controller Error
0460	Fail-safe Timer NMI Failure
0461	Software Port NMI Failure
0465	Bus Time-out NMI in Slot
0467	Expansion Board NMI in Slot
0501	PCI System Error
0510	PCI Parity Error
0710	System Board Device Resource Conflict
0711	Static Device Resource Conflict
0800	PCI I/O Port Conflict
0801	PCI Memory Conflict
0802	PCI IRQ Conflict
0803	PCI Error Log is Full.
0810	Floppy Disk Controller Resource Conflict
0811	Primary IDE Controller Resource Conflict
0812	Secondary IDE Controller Resource Conflict
0815	Parallel Port Resource Conflict
0816	Serial Port 1 Resource Conflict
0817	Serial Port 2 Resource Conflict
0818	USB 1...TBD
0819	USB 2...TBD
0820	Expansion Board Disabled in Slot
0900	NVRAM Checksum Error, NVRAM Cleared
0903	NVRAM Data Invalid, NVRAM Cleared
0905	NVRAM Cleared By Jumper
0982	I/O Expansion Board NMI in Slot
0984	Expansion Board Disabled in Slot
0985	Fail-safe Timer NMI
0986	System Reset caused by Watchdog Timer
0987	Bus Time-out NMI in Slot

5. Board Set Specifications

This chapter specifies the operational parameters and physical characteristics for the R440FX UP Server. This is a board-level specification only. System specifications are beyond the scope of this document.

5.1 Absolute Maximum Ratings

Operation of the R440FX UP Server at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table1-1. Absolute Maximum Ratings

Operating Temperature	0°C to +55°C *
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to VDD + 0.3V **
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V

* Chassis design must provide proper airflow to avoid exceeding Pentium Pro maximum case temperature.
** VDD means supply voltage for the device.

Further topics in this chapter specify normal operating conditions for the R440FX UP Server.

5.2 Electrical Specifications

DC specifications for the R440FX UP Server power connectors and module power budgets, are summarized here. Electrical characteristics for major connector interfaces (including DC and AC specifications), can be obtained from the following documents:

- PCI bus connector PCI Local Bus Specification Rev. 2.1
- ISA bus connector ISA Specification
- Power supply and system chassis ATX Specification

5.2.1 Power Connection

Power supply connection may be obtained using the 24-pin main and 14-pin auxiliary power connectors, or the 20-pin ATX-style connector (if the R440FX UP Server is installed in an ATX-compatible chassis . Each signal of the 24-pin main connector attaches to the power supply via 18 AWG wire of the color shown below. The 14-pin auxiliary power connector attaches using 24 AWG wire. Each signal of the 20-pin ATX connector attaches to the power supply via 18 AWG wire of the color shown below, with the exception of pin 11.

Table1-2. 24-pin Main Power Connector Pin-out

Pin	Signal	Color	Pin	Signal	Color
1	+5 Vdc	Red	13	+5 Vdc	Red
2	+5 Vdc	Red	14	+5 Vdc	Red
3	-5 Vdc	White	15	+5 Vdc	Red
4	-12Vdc	Blue	16	+5 Vdc	Red
5	COM	Black	17	COM	Black
6	COM	Black	18	COM	Black
7	COM	Black	19	COM	Black
8	COM	Black	20	COM	Black
9	COM	Black	21	COM	Black
10	+3.3Vdc	Orange	22	+3.3Vdc	Orange
11	+12Vdc	Yellow	23	+3.3Vdc	Orange
12	+12Vdc	Yellow	24	+12Vdc	Yellow

Table1-3. 14-pin Auxiliary Power Connector Pin-out (non-ATX)

Pin	Signal	Color	Pin	Signal	Color
1	Remote Sense return	Black	8	POWER_GOOD	Gray
2	5V Remote Sense	Red	9	PS_ON	Green
3	3.3V remote sense	Orange	10	NON_ATX_L *	Black
4	COM	Black	11	5VSB	Purple
5	N/C	None	12	KEY (Amp 87077-2)	None
6	N/C	None	13	24Vdc	Brown
7	COM	Black	14	24Vdc Return	Black

If grounded, indicates a non-ATX power supply is in use.

Table1-4. 20-pin Main Power Connector Pin-out (ATX)

Pin	Signal	Color	Pin	Signal	Color
1	+3.3 Vdc	Orange	11	+3.3 Vdc +3.3V sense	Orange(22AWG) Brown(22AWG)
2	+3.3 Vdc	Orange	12	-12Vdc	Blue
3	COM	Black	13	COM	Black
4	+5 Vdc	Red	14	PS_ON_L	Green
5	COM	Black	15	COM	Black
6	+5 Vdc	Red	16	COM	Black
7	COM	Black	17	COM	Black
8	PWR_OK	Gray	18	-5Vdc	White
9	+5V SB	Purple	19	+5 Vdc	Red
10	+12Vdc	Yellow	20	+5 Vdc	Red

5.2.2 Power Consumption

The following table shows the power consumed on each supply line for a typical R440FX UP Server with 1 processor, 4 DIMMs, 3 PCI slot loads (2 A @ 5V per slot), and 2 ISA slot loads (Server Monitor Module and terminal concentrator board).

NOTE: *The following numbers are provided as an example. Actual power consumption will vary depending on the exact R440FX UP Server configuration. Refer to the appropriate system chassis document for more information.*

Table1-5. R440FX UP Server Power Consumption

Device(s)	3.3V	+5V	+12V	-12V
Processor		10.3 A		
Memory	2.0 A			
Baseboard	4.5A	2.5 A	.5 A	.1 A
PCI slots		6 A		
ISA slots		1.9 A	2.0 A	.4 A
Total	**6.5 A**	**21.7 A**	**2.5 A**	**.5 A**

5.3 Mechanical Specifications

The following diagrams show the mechanical specifications of the R440FX UP Server motherboard. All dimensions are given in inches, as per ANSI Y15.4M. Unless otherwise noted, maximum component height is .550 inches. Connectors are dimensioned to pin 1. Refer to "Connector Specifications" after the diagrams for more information.

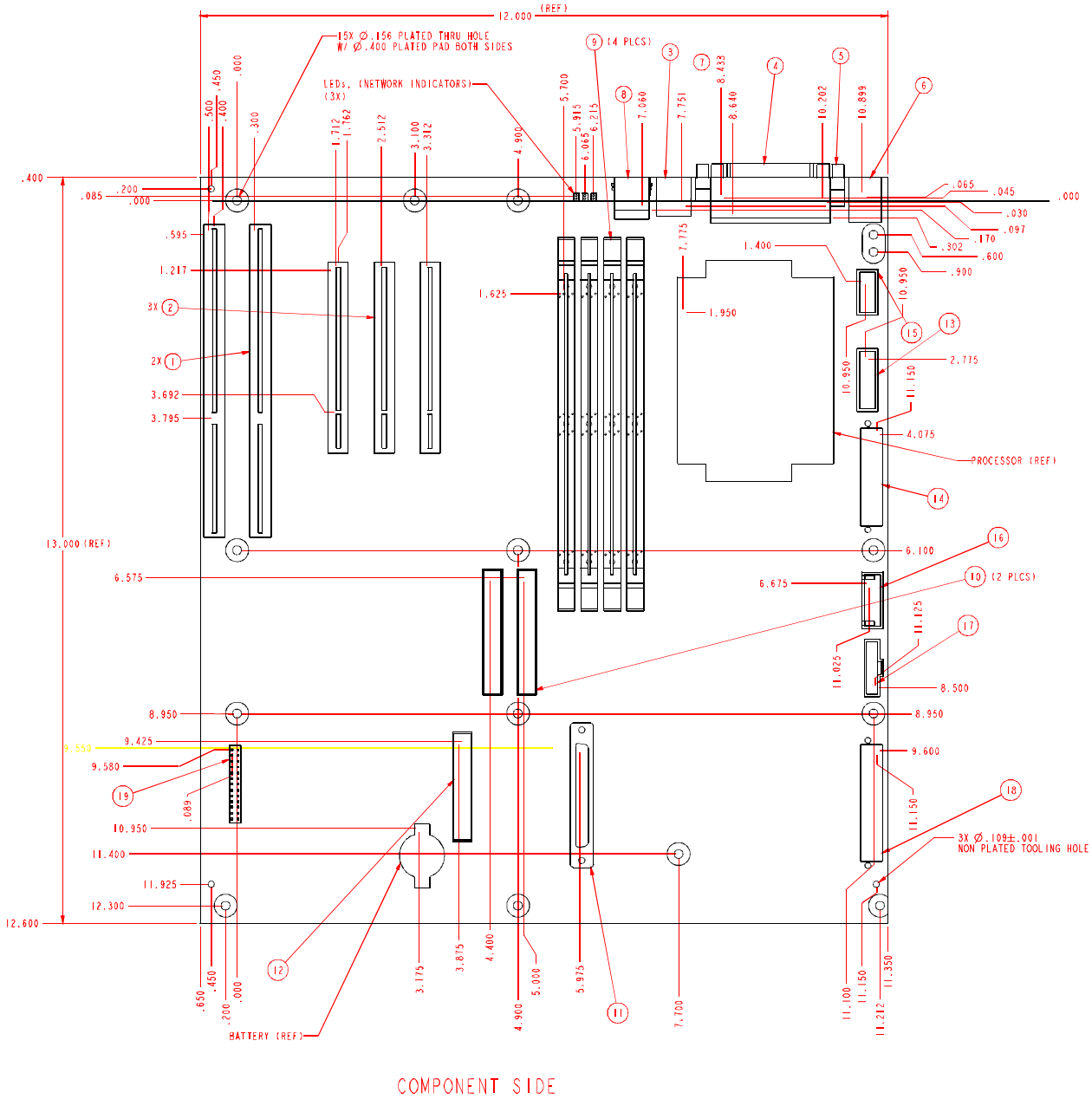

Figure5-1R440FX UP Server Mechanical Diagram (Rev 6)

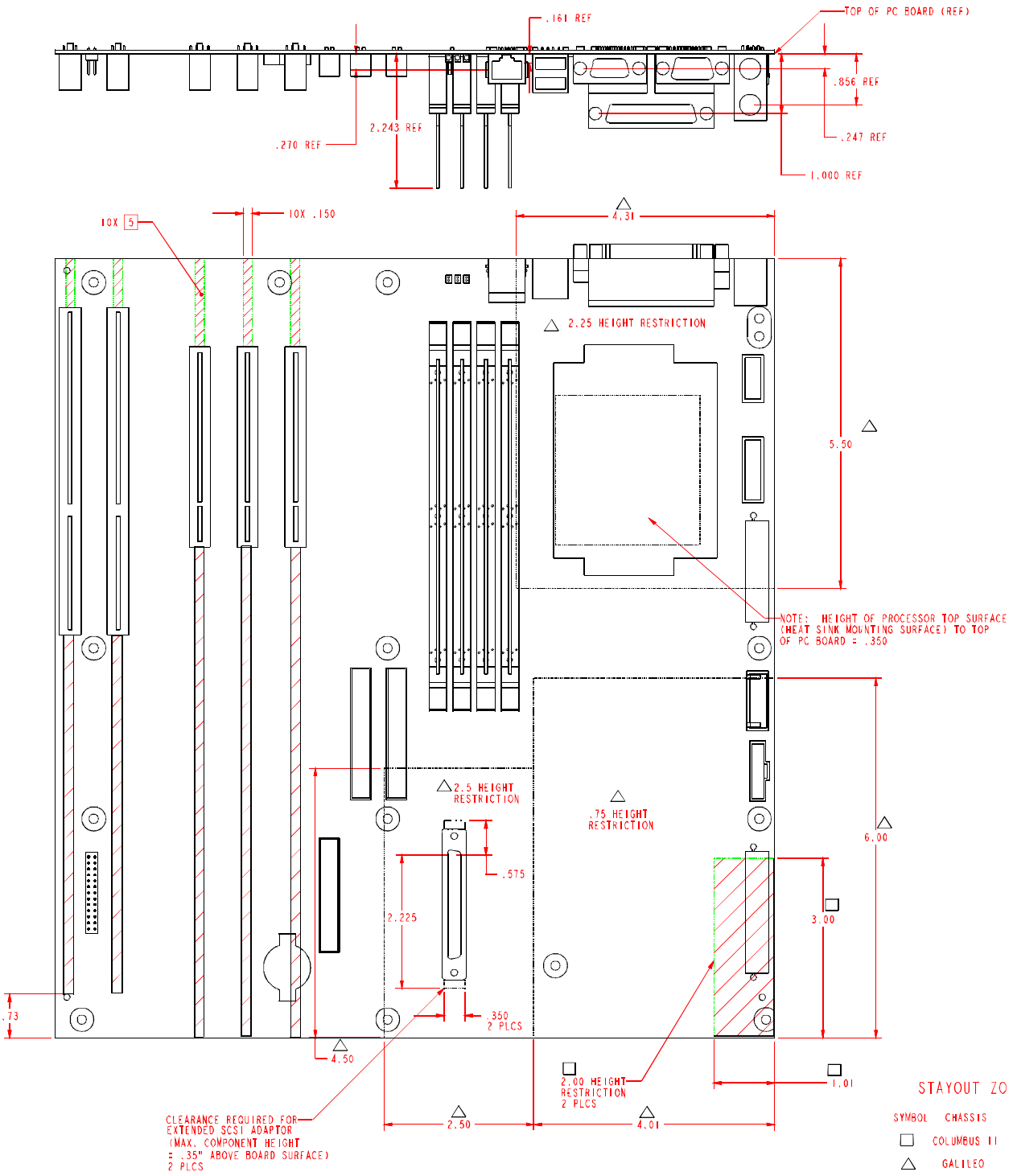

Figure5-2 Component Height Specifications (Rev 6)

Appendix A. Supported Environments

The R440FX UP Server has been validated with the leading network operating systems, adapter cards and DIMM combinations. Below is a summary of them. Not all configurations have been validated and there may be limitations to their interoperability. The list will change as more environments are validated. Contact your Intel technical representative for an updated list.

Validated Operating Systems

The table below lists which O/S each particular adapter was tested with.

- Level 1 - Heavy testing done in Intel's Server Validation Lab
- Level 2 - Minimal testing done in one of Intel's compatibility labs

Level	Operating System	Version	Certified
1	Windows NT	Versions 3.51 (Build 1057) Advanced Server (w/Service Pack 3)	OEM must certify w/Microsoft
1	Novell NetWare	4.1 SMP (patches 410pt3 & 410it6 installed on UP prior to installing MP)	Scheduled
1	IBM OS/2	IBM OS/2 2.11 SMP w/LANServer 4.0 (Fix Pack s.630), OS/2 WarpServer Advanced	Scheduled
2	Banyan	6.0	Scheduled
2	IBM OS/2	WARP 3.0	Scheduled
2	MS DOS	6.22	N/A
2	Novell NetWare	3.12, 4.10	Scheduled
2	SCO UNIX	ODT 5.0	OEM must certify W/SCO
2	Solaris	2.5	Scheduled

Appendix B. Product Codes

R440FX Baseboard Codes

Description	Product code
CPU 200 MHz/256K ; 8MB	BRO06APP
CPU 200 MHz/256K ; 16MB	BROS06A
CPU No processor/no memory	BROS14A

R440FX System Codes

Description	Product code
R440FX UP Server Accessory Kit (1 wide ultra cable, 9 connectors, & 1 wide-to-narrow device adapter)	ACOLROSWSCSIA
CPU 200 MHz/256K ; 16MB	SROSCOLSTD05PP
CPU 200 MHz/256K ; 32MB	SROSCOLSTD05A
CPU 200 MHz/256K ; 32MB PFC Power Supply	SROSCOLJPN17A

The Rosewood project consists of a baseboard product and one system product. The table below characterizes the specifics of the baseboard and system products.

PRODUCT CODE	TYPE	PROCESSOR	MEMORY	Other	EXTERNAL DRIVE	INTERNAL DRIVE
SROSCOLSTD05PP	SYSTEM	200 MHz /256KB Pentium Pro processor	2-16MB DIMMs		1-IDE CDROM	1 1GB IDE drive
SROSCOLSTD05A	SYSTEM	200 MHz /256KB Pentium Pro processor	1-32MB DIMM		1-IDE CDROM	None
SROSCOLJPN17A	SYSTEM	200 MHz /256KB Pentium Pro processor	1-32MB DIMM	PFC Power Supply	None	None
BROS06APP	BASEBOARD	200 MHz /256KB Pentium Pro processor	2-8MB DIMMs			
BROS06A	BASEBOARD	200 MHz /256KB Pentium Pro processor	1-32MB DIMMs			
BROS14A	BASEBOARD	no processor	no memory			

PP - Pre-Production, A - Production

Appendix C. Connector Pin-outs

PCI Connectors

The following table defines the pin-out for each PCI expansion connector on the R440FX UP Server. Signals which are unused are labeled as either “Reserved”, or by signal mnemonic with the R440FX UP Server implementation shown in parentheses.

PCI Connector Signal Pin-out

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	-12V	A32	AD17	B1	TRST_L (p/d)	B32	AD16
A2	TCK (p/d)	A33	C/BE2_L	B2	+12V	B33	+3.3V *
A3	GND	A34	GND	B3	TMS (p/u)	B34	FRAME_L
A4	TDO (n/c)	A35	IRDY_L	B4	TDI (p/u)	B35	GND
A5	+5V	A36	+3.3V *	B5	+5V	B36	TRDY_L
A6	+5V	A37	DEVSEL_L	B6	INTA_L	B37	GND
A7	INTB_L	A38	GND	B7	INTC_L	B38	STOP_L
A8	INTD_L	A39	LOCK_L	B8	+5V	B39	+3.3V *
A9	PRSNT1_L	A40	PERR_L	B9	Reserved	B40	SDONE (p/u)
A10	Reserved	A41	+3.3V *	B10	+5V	B41	SBO_L (p/u)
A11	PRSNT2_L	A42	SERR_L	B11	Reserved	B42	GND
A12	GND	A43	+3.3V *	B12	GND	B43	PAR
A13	GND	A44	C/BE1_L	B13	GND	B44	AD15
A14	Reserved	A45	AD14	B14	Reserved	B45	+3.3V *
A15	GND	A46	GND	B15	RST_L	B46	AD13
A16	CLK	A47	AD12	B16	+5V	B47	AD11
A17	GND	A48	AD10	B17	GNT_L	B48	GND
A18	REQ_L	A49	GND	B18	GND	B49	AD9
A19	+5V	A50	key	B19	Reserved	B50	key
A20	AD31	A51	key	B20	AD30	B51	key
A21	AD29	A52	AD8	B21	+3.3V *	B52	C/BE0_L
A22	GND	A53	AD7	B22	AD28	B53	+3.3V *
A23	AD27	A54	+3.3V *	B23	AD26	B54	AD6
A24	AD25	A55	AD5	B24	GND	B55	AD4
A25	+3.3V *	A56	AD3	B25	AD24	B56	GND
A26	C/BE3_L	A57	GND	B26	IDSEL	B57	AD2
A27	AD23	A58	AD1	B27	+3.3V *	B58	AD0
A28	GND	A59	+5V	B28	AD22	B59	+5V
A29	AD21	A60	ACK64_L (p/u)	B29	AD20	B60	REQ64_L (p/u)
A30	AD19	A61	+5V	B30	GND	B61	+5V
A31	+3.3V *	A62	+5V	B31	AD18	B62	+5V

* 3.3V system power is not present at this pin..

***NOTE**: The R440FX UP Server does not provide a PCI 3.3V power connector. Only the 5V PCI signaling environment is supported, and no power is available at the 3.3V signal pins in expansion slots.*

ISA Connectors

ISA Connector Signal Pin-out

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A01	IOCHK_L	A26	SA5	B01	GND	B26	DACK2_L
A02	SD7	A27	SA4	B02	RESDRV	B27	TC
A03	SD6	A28	SA3	B03	+5V	B28	BALE
A04	SD5	A29	SA2	B04	IRQ9	B29	+5V
A05	SD4	A30	SA1	B05	-5V	B30	OSC
A06	SD3	A31	SA0	B06	DRQ2	B31	GND
A07	SD2	C01	SBHE_L	B07	-12V	D01	MEMCS16_L
A08	SD1	C02	LA23	B08	NOWS_L	D02	IOCS16_L
A09	SD0	C03	LA22	B09	+12V	D03	IRQ10
A10	IOCHRDY	C04	LA21	B10	GND	D04	IRQ11
A11	AEN	C05	LA20	B11	SMWTC_L	D05	IRQ12
A12	SA19	C06	LA19	B12	SMRDC_L	D06	IRQ15
A13	SA18	C07	LA18	B13	IOWC_L	D07	IRQ14
A14	SA17	C08	LA17	B14	IORC_L	D08	DACK0_L
A15	SA16	C09	MRDC_L	B15	DACK3_L	D09	DRQ0
A16	SA15	C10	MWTC_L	B16	DRQ3	D10	DACK5_L
A17	SA14	C11	SD8	B17	DACK1_L	D11	DRQ5
A18	SA13	C12	SD9	B18	DRQ1	D12	DACK6_L
A19	SA12	C13	SD10	B19	REFRESH_L	D13	DRQ6
A20	SA11	C14	SD11	B20	BCLK	D14	DACK7_L
A21	SA10	C15	SD12	B21	IRQ7	D15	DRQ7
A22	SA9	C16	SD13	B22	IRQ6	D16	+5V
A23	SA8	C17	SD14	B23	IRQ5	D17	MASTER16_L
A24	SA7	C18	SD15	B24	IRQ4	D18	GND
A25	SA6	--	--	B25	IRQ3	--	--

5.4 Serial Port Connectors

Serial Port Connector Pin-out

Pin	Name	Description
1	DCD	Data Carrier Detected
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Return to Send
8	CTS	Clear to Send
9	RIA	Ring Indication Active

Serial Port B

The pin-out below shows pin-outs from serial port B from the board-level perspective. Note that the system uses a short cable to connect from the board to the serial port on the chassis, and that this cable makes serial port B have the same pin-out as serial port A.

Pin	Name	Pin	Name
1	DCD	6	CTS
2	DSR	7	DTR
3	RXD	8	RI
4	RTS	9	GND
5	TXD	10	key

Parallel Port Connector

Parallel Port Connector Pin-out

Pin	Name	Pin	Name
1	STROBE_L	14	AUFDXT_L
2	D0	15	ERROR_L
3	D1	16	INIT_L
4	D2	17	SLCTIN_L
5	D3	18	GND
6	D4	19	GND
7	D5	20	GND
8	D6	21	GND
9	D7	22	GND
10	ACK_L	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT		

Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single housing. Although functionally equivalent, the mouse connector is defined as the one above the keyboard connector.

Mouse Connector Pin-out

Pin	Signal	Description
7	MSEDAT	Mouse Data
8	(NC)	
9	GND	
10	FUSED_VCC	
11	MSECLK	Mouse Clock
12	(NC)	

Keyboard Connector Pin-out

Pin	Signal	Description
1	KEYDAT	Keyboard Data
2	(NC)	
3	GND	
4	FUSED_VCC	
5	KEYCLK	Keyboard Clock

6	(NC)	

Appendix D. Customer Support

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