R440LX DP Server Baseboard Specification Update

Release Date: January, 1999

Order Number: 243558-013

The R440LX DP Server board set may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

REVISION HISTORY

Date of Revision	Description
December 1997	Initial release of the Specification Update for the R440LX DP Server baseboard.
January 1998	Added errata 26, 27, 28, 29 and 30. Added General Information section and Identification table.
February 1998	Added errata 31, 32, and 33. Updated errata 5, 8, 12, 15, 16, 20, 21, 22, 25, 26, 27, 28, 29, and 30.
March 1998	Added errata 34 and 35. Updated errata 32 and 33.
April 1998	Moved previous errata 1-35 into the R440LX TPS Rev. 4. New errata 1-7. Updated Supported Processor Combinations Table and Supported BIOS/Processor Combinations Tables to include 333Mhz Processor information.
May 1998	Added errata 8 and 9. Updated errata 1-7.
June 1998	Added errata 10 – 14. Updated errata 1, 3, 6, and 8.
July 1998	Renumbered errata starting at 36 to correspond to numbering used in the R440LX TPS Rev. 4. Added errata 50. Updated errata 49.
August 1998	Added errata 51. Updated errata 41 and 38.
September 1998	Added errata 52, 53, and 54. Updated errata 36 and 38.
October 1998	No updates.
November 1998	No updates.
December 1998	No updates.
January 1999	No updates.

PREFACE

This document is an update to the specifications contained in the *R440LX DP Server Baseboard Technical Product Specification* (Order Number 282998). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Specification Clarifications, Errata, and Document Changes.

Refer to the *Pentium® II processor Specification Update* (Order Number 243337) for specification updates concerning the Pentium II processor. Items contained in the Pentium II Processor Specification Update that either do not apply to the R440LX DP Server Baseboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Refer to the *Intel 82443LX PAC AGPset Specification Update* (Order Number 297655) and the *Intel 82371AB (PIIX4) Specification Update* (Order Number 297738) for specification updates concerning the Intel 82440LX AGPset. Items contained in these Specification Updates that either do not apply to the R440LX DP Server Baseboard or have been worked around are noted in this document. Otherwise, it should be assumed that any AGPset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. These may cause the R440LX DP Server's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all erratum documented for that stepping are present on all devices.

GENERAL INFORMATION

Identification Information

Below are the specific boards, BIOS, and components covered by this update.

Board Fab #	Product Code	PBA #	MM #	BIOS	SCU	Processor Stepping Supported
2.0	B0RD0STD	674688-022	814969	REDWD0.86B.0015.P01.97	3.80 OVL 1.10R	C0/C1
2.0	B0XR440LX	674688-022	814969	REDWD0.86B.0015.P01.97	3.80 OVL 1.10R	C0/C1
3.0	B0RD0STD	674688-301	814709	REDWD0.86B.0027.P03.98	3.80 OVL 1.10R	C0/C1 dA-0/dA-1
3.0	B0RD0STD	674688-311	814709	REDWD0.86B.0036.P04.98	3.80 OVL 1.10R	C0/C1 dA-0/dA-1 B0

The following table indicates which steppings of the Pentium® II processor can be mixed within the same system. An “X” denotes which steppings can be mixed and a blank indicates the R440LX DP Server board set does not support the given stepping combination.

Supported Processor Combinations

Stepping (Core/L2)	C0	C0	C0	C1	C1	C1	dA-0	dA-1	B0
Frequency	233	266	300	233	266	300	333/66	333/66	300
Cache Size/ Cacheability	512MB 512MB	512MB 512MB	512MB 512MB	512MB 512MB	512MB 512MB	512MB 512MB	512MB 512MB	512MB 4GB	512MB 4GB
Stepping ID	0633	0633	0633	0634	0634	0634	0650	0651	0652
S-Spec	SL268	SL269	SL28R/ SL2MZ	SL2HF	SL2HE	SL2HA/ SL2QC	SL2KA/ SL2QF	SL2S5/ SL2QH	SL2W8
SL268	X			X					
SL269		X			X				
SL28R			X			X			
SL2HF	X			X					
SL2HE		X			X				
SL2HA			X			X			
SL2KA							X	X	
SL2S5							X	X	
SL2W8									X

NOTES:

1. The BIOS used must support each stepping installed in the system.
2. Although Intel recommends using the identical steppings of processor silicon in dual processor systems whenever possible (as this is the only configuration which receives full validation across all of Intel's testing), Intel supports mixing processor steppings and does not actively prevent various steppings of the Pentium® processor from working together in a dual processor (DP) systems. However, since Intel cannot validate every possible combination of devices, each new stepping of a device is fully validated only against the latest steppings of other processors and chipset components.
3. If processor steppings dA-0 and dA-1 are used together in a dual processing configuration, the processor cacheability will default to 512MB.
4. Intel does not recommend using non-ECC processors for Server applications.

The following table lists the production BIOS versions and processor steppings supported by the board set. The table also indicates which steppings of the Pentium®II processor are supported by each version of the BIOS. The "X" denotes which steppings are supported and a blank indicates the R440LX DP Server board set does not support the given BIOS/stepping combination.

Supported BIOS/Processor Combinations

	Stepping (Core/L2)	B0	C0	C0	C0	C1	C1	C1	dA-0	dA-1	B0
	Frequency	233	233	266	300	233	266	300	333/66	333/66	300
	Cache Size/ Cacheability	512MB 512MB	512MB 512MB	512MB 512MB	512MB 512MB	512MB 512MB	512MB 512MB	512MB 512MB	512MB 512MB	512MB 4GB	512MB 4GB
	Stepping ID	0632	0633	0633	0633	0634	0634	0634	0650	0651	0652
BIOS	S-Spec	Q102	SL268	SL269	SL28R/ SL2MZ	SL2HF	SL2HE	SL2HA/ SL2QC	SL2KA/ SL2QF	SL2S5/ SL2QH	SL2W8
REDWD0.86B. 0015.P01.97		X	X	X	X	X	X	X			
REDWD0.86B. 0022.P02.98			X	X	X	X	X	X			
REDWD0.86B. 0025.P02.98			X	X	X	X	X	X	X	X	
REDWD0.86B. 0027.P03.98			X	X	X	X	X	X	X	X	
REDWD0.86B. 0031.P03.98			X	X	X	X	X	X	X	X	
REDWD0.86B. 0036.P04.98			X	X	X	X	X	X	X	X	X

ERRATA

The following table indicates the Errata, Specification Changes, Specification Clarifications, and documentation changes which apply to the R440LX DP Server baseboard. Intel intends to fix some of the erratum in the future and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the hardware or software associated with the R440LX DP Server.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.

#	Status	Summary
36	Fixed	Hard Disk Drive LED is always on when SCSI BIOS is Disabled in Setup
37	Fixed **	LanDesk® reports High CPU Voltage Reading
38	Fixed	Phoenix Core BIOS Errata
39	Fix	R440LX eventlog.exe Utility will not clear the Event Log
40	Fixed	Keyboard Controller Conflict in Microsoft* Windows* 95 OEM Service Release 2 (OSR2)
41	Fix	IRQ 14 cannot be assigned to add-in cards
42	Fixed	SCU V. 3.80 OVL 1.10R indicates incorrect IRQ assignment
43	Fixed	PC9X Test Failure when running PC97 V.7.5 under Microsoft* Windows* 95 OEM Service Release 2 (OSR2)
44	NoFix	FRB error with FRB jumper set to position 6-7
45	Fix	PCI 2.1 (cards) Test Failure when running PC97 V.7.5 under Microsoft* Windows* 95 OEM Service Release 2 (OSR2)
46	Fixed	PCI Bridge not identified in Microsoft* Windows* 95 OEM Service Release 2 (OSR2)
47	Fixed	MTA V.3.48 PIIX4 ACPI_IO_REGISTERS Test Failure
48	NoFix	BIOS Logo Utility Displays Misleading Message
49	Fixed	No Boot, Port 80 = 69h
50	NoFix	SCU V. 3.80 OVL 1.10R does not recognize Pentium® II 333 Mhz processors
51	Fix	Cannot exit BIOS Virus Scan or System Backup Notification Screen
52	NoFix	Effect of conversion from 300 MHz Pentium® II processor core change to 0.25µ on R440LX DP Server
53	Fixed	MTA v. 3.49 PIIX4E.EXE Test Failure
54	Fix	MTA v. 3.50 SMP_PROCESSOR.APIC_INTERRUPT Test Hang

** This fix will be incorporated in the BORDOSTD product code (MM # 814709) only. This fix will not be incorporated in the BOXR440LX product code. In addition, errata # 20, 21, 26, 28, and 30 documented in the R440LX DP Server TPS Rev. 4 will not be fixed in the BOXR440LX product code.

36. Hard Disk Drive LED is always on when SCSI BIOS is Disabled in Setup

PROBLEM: When the SCSI BIOS is disabled in BIOS Setup on R440LX, the HDD LED is always on. When SCSI BIOS is enabled, the LED works as expected.

IMPLICATION: The HDD LED will always be on when SCSI BIOS is disabled.

WORKAROUND: None.

STATUS: Fixed in BIOS Release 4.0.

*37. LANDesk® Reports High CPU Voltage Reading ***

PROBLEM: LANDesk® reports the processor voltage sensor reading is too close to the Upper Critical Limit on R440LX. LANDesk® displays the Current value 3.000V, the Upper Critical 3.078V, and Lower Critical 2.509V. The voltage specification for the Pentium® II is 2.80V nominal, 2.90V maximum, and 2.74V minimum. This is due to the series pullup resistor connected to the PBC ADC pin having to large a value. The problem is eliminated if the pullup resistor is changed from 1K to 100 ohm.

IMPLICATION: LANDesk® reports a higher processor voltage reading than the actual processor voltage.

WORKAROUND: None.

STATUS: Fixed in R440LX FAB 3.0.

38. Phoenix Core BIOS Errata

PROBLEM: There are two errata present in the Phoenix Core BIOS:

1. After setting both the user and administrative password, and entering BIOS setup with the user password, many settings are locked from the operator but the operator can load the defaults by pressing the <F9> key. All of the parameters can be set back to default values including the ones that are locked.
2. If the user or administrator password is set in setup, BIOS shows a password screen before entering setup. This password screen states that the <ESC> key “Exits.” The text string has been corrected in BIOS Release 4.0 to state “Clear Text”.

IMPLICATION: The above errata may be encountered with any R440LX BIOS prior to and including Release 3.0. These errata will be fixed in BIOS Release 4.0.

WORKAROUND: None.

STATUS: Fixed BIOS Release 4.0.

39. R440LX eventlog.exe Utility will not clear the Event Log

PROBLEM: The R440LX eventlog.exe utility will not clear the event log area with the /c switch. There currently is no stand alone program for the utility to call to clear the event log area on R440LX.

IMPLICATION: The eventlog.exe utility cannot be used to clear the event log on R440LX.

WORKAROUND: BIOS Setup contains an option to clear the event log.

STATUS: Will be fixed in a future BIOS Release.

40. Keyboard controller conflict in Microsoft Windows* 95 OEM Service Release 2 (OSR2)*

PROBLEM: In Windows 95 OEM Service Release 2 (OSR2), the I/O address 0064, used by the keyboard controller, is listed as conflicting with a Motherboard resource. No operational problems were encountered.

IMPLICATION: The keyboard controller will be listed as conflicting with a Motherboard resource in Windows 95 OEM Service Release 2 (OSR2).

WORKAROUND: Use BIOS Release 2.1 or later versions.

STATUS: The keyboard I/O address conflict has been resolved in BIOS Release 2.1 and later versions.

41. IRQ 14 cannot be assigned to add-in cards

PROBLEM: IRQ 14 is not freed by BIOS to assign to add-in cards, even when the primary IDE channel which normally uses IRQ 14 is not in use.

IMPLICATION: IRQ 14 currently cannot be assigned to add-in cards.

WORKAROUND: None.

STATUS: Will be fixed in a future BIOS Release.

42. SCU V. 3.80 OVL 1.10R indicates incorrect IRQ assignment

PROBLEM: The System Configuration Utility (SCU) V. 3.80 OVL 1.10R Global Resource Map indicates incorrect IRQ assignment for IRQ 1 and IRQ 12. The actual IRQ assignment is:
IRQ 1: Keyboard Interrupt
IRQ 12: Mouse Interrupt

IMPLICATION: The IRQ assignment in the SCU Global Resource Map currently appears as IRQ 1: Chipset and IRQ 12: Keyboard & Mouse, which is incorrect.

WORKAROUND: Use the updated configuration file to correct IRQ1to indicate "Keyboard Interrupt".

STATUS: There is an updated configuration file that can be used correct IRQ 1 to indicate "Keyboard Interrupt". This configuration file is called SCU_IRQ1.cfg and is available at www.alder.com and support.intel.com. IRQ 12 will not be fixed to indicate Mouse Interrupt because it would require a new Overlay to be generated.

43. PC9X Test Failure when running PC97 V.7.5 under Microsoft Windows* 95 OEM Service Release 2 (OSR2)*

PROBLEM: Failure of the PC9X Resource test may be reported when running PC97 V.7.5 under Windows 95 OEM Service Release 2 (OSR2). The PC9X Resource error log will contain the entries noted below:

ERROR: ECP Printer Port (LPT1) only supports I/O: 0378-037F,0278-027F (2 options). 3 are required.

ERROR: ECP Printer Port (LPT1) only supports I/O: 0778-077F,0678-067F (2 options). 3 are required.

In addition, if Plug and Play is set to "YES" in BIOS setup, the PC9X error log will contain the entry noted below:

ERROR: PCI Universal Serial Bus (Code 29) – Device failed to start.

IMPLICATION: The customer will not be able to obtain PC97 certification without passing the PC9X Resource test under PC97 V.7.5.

WORKAROUND: Use BIOS Release 3.1 or later versions.

STATUS: The ECP Printer Port error has been fixed in BIOS Release 3.1, available at www.alder.com and support.intel.com. Microsoft has verbally agreed to waive the USB failure, since USB is not required for server products. Customers need to indicate that the product contains the R440LX motherboard when submitting systems to Windows Hardware Quality Lab* (WHQL).

44. FRB error with FRB jumper set to position 6-7

PROBLEM: By default the R440LX boxed boards come with both processors enabled in the BIOS. If a customer installs a processor in the primary slot and term card in secondary slot and moves the FRB Enable jumper to position 6-7 the system will not boot and hangs at POST = 93h. The primary processor (CPU SLOT1 in BIOS) is marked as disabled and therefore system does not boot.

IMPLICATION: The customer will see the system hang at POST = 93h in the configuration described above.

WORKAROUND: Workaround is to have customers put the FRB jumper back to position 5-6 and reboot the system.

STATUS: Will not fix.

45. PCI 2.1 (cards) Test Failure when running PC97 V.7.5 under Microsoft Windows* 95 OEM Service Release 2 (OSR2)*

PROBLEM: PCI 2.1 (cards) test failures may be reported when running PC97 V.7.5 under Windows 95 OEM Service Release 2 (OSR2). The PCI 2.1 (cards) error log will contain the entries noted below:

Testing Read-Only Bits in Power Management Control Block
Testing 0xFFFFFFFF bits at offset 0xD0 FAIL
ERROR: DWORD 34 changed to 7fd5d55f when written to, expected 00000000!
The test was able to WRITE to the following READ-ONLY bits: 7fd5d55f

Beginning test of device : Unknown Device
Bus: 0x000, Device: 0x010, Function: 0x000
Reading the PCI Card's Config Space...
Vendor ID: 0x8086, Device ID 0x1229
Class Code: 0x02, SubClassCode: 0x00, P/F 0x00
Verify that the Vendor ID is not zero or 0FFFFh (8086)...PASS
ERROR: PCI Subsystem Vendor 0x0000, expected a valid Subsystem Vendor ID!
ERROR: PCI Subsystem Device ID is 0x0000, expected a valid Subsystem Device ID!
ERROR: Extended Capabilities not supported on this device (Power Management)

Beginning test of device : Unknown Device
Bus: 0x000, Device: 0x012, Function: 0x000
Reading the PCI Card's Config Space...
Vendor ID: 0x1013, Device ID 0x00B8
Class Code: 0x03, SubClassCode: 0x00, P/F 0x00
Verify that the Vendor ID is not zero or 0FFFFh (1013)...PASS
ERROR: PCI Subsystem Vendor 0x0000, expected a valid Subsystem Vendor ID!
ERROR: PCI Subsystem Device ID is 0x0000, expected a valid Subsystem Device ID!
ERROR: Extended Capabilities not supported on this device (Power Management)

IMPLICATION: The customer will not be able to obtain PC97 certification without passing the PCI 2.1 (cards) test under PC97 V.7.5.

WORKAROUND: None.

STATUS: Microsoft has verbally agreed to waive the PC97 V.7.5 PCI 2.1 (cards) test failure for products released prior to January 1, 1998.

46. PCI Bridge not identified in Microsoft Windows* 95 OEM Service Release 2 (OSR2)*

PROBLEM: In Windows 95 OEM Service Release 2 (OSR2), the PCI Bridge is listed under Other Devices in Device Manager. No operational problems were encountered.

IMPLICATION: The PCI Bridge will be listed under Other Devices in Device Manager.

WORKAROUND: A driver for the PCI Bridge (PIIX4) on R440LX has been posted on www.alder.com. When this driver is installed, Windows 95 OEM Service Release 2 (OSR2) will recognize the PCI Bridge.

STATUS: Fixed.

47. MTA V.3.48 PIIX4 ACPI_IO_REGISTERS Test Failure

PROBLEM: The MTA Version 3.48 PIIX4 ACPI_IO_REGISTERS test will fail on R440LX DP Server baseboards with the PIIX4E component (baseboard P/N 674688-311 and later revisions). This is a known test issue. MTA Version 3.48 currently ships with the R440LX DP Server System CD. The PIIX4E component present on R440LX DP Server baseboards with P/N 674688-311 and later revisions requires a modification to the MTA Version 3.48 PIIX4 ACPI_IO_REGISTERS test.

IMPLICATION: The MTA Version 3.48 PIIX4 ACPI_IO_REGISTERS test will fail on R440LX DP Server baseboards with the PIIX4E component (baseboard P/N 674688-311 and later revisions).

WORKAROUND: MTA Version 3.49, currently posted on www.alder.com, includes a fix for the PIIX4 ACPI_IO_REGISTERS test that will allow the test to run on R440LX DP Server baseboards with the PIIX4E component (baseboard P/N 674688-311 and later revisions). If customers choose to use MTA Version 3.48, they are advised not to run the PIIX4 ACPI_IO_REGISTERS test by manually disabling this test in MTA Version 3.48.

STATUS: Fixed.

48. BIOS Logo Utility Displays Misleading Message

PROBLEM: When using the BIOS Logo Utility to convert a .BMP file to a .USR file to be flashed into BIOS, the .BMP file size must not exceed 8K. If the .BMP file size is greater than 8K, the message "IMAGE MUST NOT EXCEED 64K" is displayed.

IMPLICATION: If the user tries to convert a .BMP file greater than 8K in size to a .USR file to be flashed into the BIOS, the message"IMAGE MUST NOT EXCEED 64K" will be displayed. The message "IMAGE MUST NOT EXCEED 64K" is misleading, it should actually read "IMAGE MUST NOT EXCEED 8K".

WORKAROUND: None.

STATUS: Will not fix.

49. No Boot, Port 80 = 69h

PROBLEM: Incidences have been encountered in which R440LX DP Server systems have failed to complete POST. When a POST card is used, the POST display halts at Port 80 = 69h. Clearing CMOS or trying to perform a recovery boot with BIOS Release 3.0 and earlier versions has no affect on the system.
The root cause of the R440LX DP Server system halt during POST at Port 80 = 69h is corruption of the event log area in BIOS. At Port 80 = 69h, BIOS is checking the condition of the event log. When the event log has been corrupted, BIOS cannot identify the termination of the event log, and instead enters an infinite loop looking for the termination of the event log from which the BIOS cannot exit, causing a halt at Port 80 = 69h. BIOS Release 3.0 as well as all previous BIOS releases do not have the capability to terminate from this infinite loop in the case of event log corruption.
Intel® has identified two possible root causes of the R440LX DP Server system event log corruption:

1. System power down or reset when the event log is being cleared by the logchk.exe utility. It is recommended to wait at least 2 seconds after an event log clear with the logchk.exe utility before powering down or resetting the system to avoid event log corruption.
2. System power down or reset when the event log is being cleared by BIOS during POST after 'event log clear' has been set to 'yes' in BIOS setup. In the case of event log clear by BIOS setup, the event log clear operation occurs at Port 80 = 69h, however, it is recommended to allow the system to fully complete POST after selecting event log clear in BIOS setup before powering down or resetting the system to avoid risk of event log corruption.

Intel's testing indicates that event log corruption is not caused either by SMI occurrence, by SMI occurrence in combination with power down or reset, or by SMI occurrence in combination with event log clearing.

IMPLICATION: If this condition is encountered, the system will not complete POST and will halt at Port 80 = 69h.

WORKAROUND: Use BIOS Release 3.1 to do a recovery boot.

STATUS: Corrective action taken includes the following:

1. Board level and system level tests have been changed to include a check of the event log after clearing.
2. BIOS Release 3.1 has been created to provide BIOS a way out of the infinite loop encountered at Port 80 = 69h in the case of event log corruption.

BIOS Release 3.1 is the same as BIOS Release 3.0 with the addition of the PC9X Resource test fix (a PC97 test requirement) and the Port 80 = 69h fix. BIOS Release 3.1 will allow customers to do a recovery boot on a system experiencing a halt at Port 80 = 69h, whereas this was not possible with previous BIOS Releases. BIOS Release 3.1 is available to customers on our Intel's web site, www.alder.com and support.intel.com.
Below are the recovery instructions:

1. Copy BIOS 3.1 to a bootable floppy.
2. Insert BIOS 3.1 floppy in the floppy disk drive and move the baseboard Recovery Boot jumper to the 'enable' position.
3. Power on the system and perform the recovery boot. This will take approximately 3 to 5 minutes. A high-pitched beep will sound and the floppy light will go off when the recovery boot is complete.
4. When finished with the recovery boot, power down the system, put the Recovery Boot jumper back to the 'default' position, and power on the system.
5. Go into BIOS setup --> Server --> System Management --> Clear Event Log --> Save changes and exit

50. SCU V. 3.80 OVL 1.10R does not recognize Pentium® II 333 MHz processors

PROBLEM: The R440LX DP Server System Configuration Utility (SCU) Release 3.80 R/OLV 1.10R code does not recognize Pentium®II 333 MHz processors, even though the R440LX BIOS properly recognizes Pentium®II 333 MHz processors and reports that they are installed in the system during POST.

IMPLICATION: The SCU reports "processor not present" when Pentium®II 333 MHz processors (S-Spec Numbers SL2KA/SL2QF or SL2S5/SL2QH) are installed.

WORKAROUND: None.

STATUS: No Fix. This issue will not cause any functional hardware issues, or issues using the SCU, as the processor type is presented in the SCU for the user's benefit only. Intel does not plan to update the R440LX DP Server SCU to fix this issue.

51. Cannot Exit BIOS Virus Scan or System Backup Notification Screens

PROBLEM: When using BIOS Release 3.1 or earlier versions, when Virus Scan Reminder and/or System Backup Reminder are set to any option besides DISABLED under the Security menu in BIOS setup, during POST a Virus Scan Reminder or System Backup Reminder screen appears. There are two options at this screen: Yes and No. The user can toggle between Yes and No, but there is no way to exit these screens; selecting either Yes or No does nothing. The only way to exit the screens is to power down or reset the system.

IMPLICATION: The user cannot exit the Virus Scan Reminder or System Backup Reminder screens that appear during POST when Virus Scan Reminder and/or System Backup Reminder are set to any option besides DISABLED.

WORKAROUND: None.

STATUS: Will be fixed in a future BIOS Release.

52. Effect of conversion from 300 MHz Pentium® II processor core change on R440LX DP Server

PROBLEM: To improve product availability and optimize production efficiencies via our newest 0.25µ process, Intel® will replace the 300 MHz Pentium® II processor core. The following table shows the details of the processor products affected by the 300 MHz Pentium® II processor core change:

	Core Step	Affected Product Code	S-Spec/QDF	MM#	CPU ID	Microcode Update #
Pre-Change	C1	80522PX300512EC	SL2HA	814593	0634	mu33
Qualification Sample	B0	80523PX300512PE	Q439	818531	0652	mu165214
Post-Change	B0	80523PX300512PE	SL2W8	818742	0652	mu165214

The Entry/Mid-range Server Division does not recommend mixing of different 300 MHz Pentium® II processor cores in a dual-processing R440LX DP Server System. The Entry/Mid-range Server Division recommends using identical steppings of processor silicon in dual processing R440LX DP Server Systems whenever possible, as this is the only configuration which receives full validation across all of Intel's testing. In particular, mixing processors of different core families in a dual processing R440LX DP Server System is not recommended.

IMPLICATION: Since Intel cannot validate every possible combination of devices, each new stepping of a processor is fully validated only against the latest steppings of other processors. Therefore, unpredictable behavior may be encountered with a dual processing R440LX DP Server System utilizing processors of mixed core processor families when running various operating systems and drivers.

WORKAROUND: The Entry/Mid-range Server Division recommends using two 300 MHz Pentium® II processors of the same core family in a dual-processing R440LX DP Server System.

STATUS: The Entry/Mid-range Server Division recommends using either two 300 MHz Pentium® II processors of the same core family in a dual-processing R440LX DP Server System.

53. MTA v. 3.49 PIIX4E.EXE Test Failure

PROBLEM: When utilizing MTA (Intel® PC Diagnostics) v. 3.49 and previous versions, if the PIIX4E.EXE test is selected and run on an R440LX DP Server, it is possible that the test will fail. The PIIX4E.EXE failure is exhibited as a "Reserved Register" failure as follows:

```
*** ERROR PIIX4.ISA_FUNCTION_REGISTERS 4.11
Miscompare at register 0x00f8: expected 0x0f28, found 0x0f30
Standard Error Code = 07902007
(Error logged at 06-22-98 09:29:39)
PIIX4.ISA_FUNCTION_REGISTERS FAILED

*** ERROR PIIX4.IDE_FUNCTION_REGISTERS 4.11
Miscompare at register 0x00f8: expected 0x0f28, found 0x0f30
Standard Error Code = 07903007
(Error logged at 06-22-98 09:29:41)
PIIX4.IDE_FUNCTION_REGISTERS FAILED

*** ERROR PIIX4.USB_FUNCTION_REGISTERS 4.11
Miscompare at register 0x00f8: expected 0x0f28, found 0x0f30
Standard Error Code = 07904007
(Error logged at 06-22-98 09:29:43)
PIIX4.USB_FUNCTION_REGISTERS FAILED
```

During a routine update to Testview (Intel PC Diagnostics), it was discovered that the PIIX4E.EXE test read a "reserved register" and compared it to a known value of the PIIX4E component. This is not a valid test since the register is "reserved" and could change without notice, causing the PIIX4E.EXE test to erroneously fail. In Testview v. 3.50 and later versions, the PIIX4E.EXE test code has been corrected to not read the data from this "reserved register".

IMPLICATION: The user may see the failure record above if MTA v. 3.49 and previous versions PIIX4E.EXE test is selected and run on a R440LX DP Server.

WORKAROUND: In Testview v. 3.50 and later versions, the PIIX4E.EXE test code has been corrected to not read data from the "reserved register". When using Testview v. 3.49 or previous versions, it is possible that PIIX4E.EXE test failures with the signature listed above will be encountered. It is recommended that customers upgrade to Testview v. 3.50 or later versions, or avoid running the PIIX4E.EXE test if Testview v. 3.49 or previous versions are used. Testview v. 3.50 is available at www.alder.com. This is a Testview issue only. No other failures of the PIIX4E component will be exhibited.

STATUS: Fixed in MTA v. 3.50.

54. MTA v. 3.50 SMP_PROCESSOR.APIC_INTERRUPT Test Hang

PROBLEM: When utilizing MTA (Intel® PC Diagnostics) v. 3.50, if the SMP_PROCESSOR_0.APIC_INTERRUPT or the SMP_PROCESSOR_1.APIC_INTERRUPT test is selected and run on an R440LX DP Server, it is possible that the test will hang. During the update to MTA (Intel PC Diagnostics) v. 3.50, the incorrect version of the DUALPENT.EXE file was included.

IMPLICATION: The user may encounter a test hang if the SMP_PROCESSOR_0.APIC_INTERRUPT or the SMP_PROCESSOR_1.APIC_INTERRUPT test is selected and run on an R440LX DP Server.

WORKAROUND: The correct version the DUALPENT.EXE file that should have been included with MTA v. 3.50 is posted at www.alder.com, in the same location as MTA v. 3.50. Customers can replace the DUALPENT.EXE file included in MTA v. 3.50 with the DUALPENT.EXE file posted atwww.alder.com. Otherwise customers should disable the MTA v. 3.50 SMP_PROCESSOR_0.APIC_INTERRUPT and SMP_PROCESSOR_1.APIC_INTERRUPT tests when running MTA v. 3.50 on an R440LX DP Server, as test hangs may occur if the tests are not disabled. This issue will be fixed in a future release of MTA.

STATUS: This issue will be fixed in a future release of MTA.

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