Intel Balboa Chassis

Technical Product Specification

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The Balboa chassis may contain design defects or errors known as errata. Characterized errata that may cause the Balboa chassis's behavior to deviate from published specifications are documented in the B440FX DP Server Specification Update.

Revision History

Revision	Revision History	Date
.001	Preliminary release of the Balboa Chassis Technical Product Specification.	7/96
1.0	Final release of the Balboa Chassis Technical Product Specification.	10/96

This product specification applies only to standard Balboa

Changes to this specification will be published in the B440FX DP Server Specification Update before being incorporated into a revision of this document.

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1. INTRODUCTION

This document details the features of the Balboa mid-size desk side chassis, detailing the chassis, power system, chassis cooling, peripheral bays, baseboards, I/O and interconnects, system configuration, system certifications, environmental limits, reliability, serviceability, and availability. Price, time to market, ability to support multiple platforms and configurations, user friendly features, accessibility, serviceability, and ability to be customized for an OEM's unique look were the primary considerations in the design of this chassis. The chassis has features for high availability servers, including power and cooling systems with optional redundancy and a mass storage system with hot-swap capable hard drives. Typically, fans and the power supplies have the lowest MTBF specifications, so the optional redundancy in these components permit the system to continue to operate with a failed fan or power supply. With the use of RAID technology, the system can also continue to operate with a hard drive failure by using hot-swap technology to replace the hard drive while the system continues to operate.

The chassis is designed for a modular processing system. This includes a baseboard containing the I/O system and a processor/memory board with multiple processors.

1.1 Related Documentation

B440FX DP Server Technical Product Specification

Columbus II Chassis TPS

B440FX DP Server Performance Report

B440FX DP Server Product Guide

Adaptec AIC-7870† SCSI Software Guide

BB440FX DP Server system Data Sheet

MTA TestView User's Guide

2. CHASSIS

The chassis is approximately 17" wide, 20" high and 20" deep. Divided by a vertical bulkhead, the baseboard and processor/memory module reside on the left side of the chassis and the power system and peripheral systems are housed on the right side. The two sides of the chassis are accessed with two removable covers which are interchangeable. There are nine I/O filler panels on the rear of the chassis for eight full length expansion cards and three bays in the back of the chassis for power supplies or fans. The first power supply is installed in the upper bay, and additional power supplies, fans, or a blank filler panel are installed in the other bays.

2.1 Color

The primary exterior system color matches Intel Color Standard 513505. The color of the chassis is “Intel Pearl White.”

- Plastic: Standard Intel Pearl White, GE Plastics C2800 - #H86204
- Paint: Standard Intel Pearl White, Sherwin William’s - Polane T #F99WX119

The bottom and back of the chassis are not painted.

OEM color matching is available for all painted exterior sheet metal components.

2.2 Front Bezel Features

The front bezel is made of three pieces of molded plastic. The main portion of the bezel covers the left front half of the chassis and provides support in order to hold the bezel for the upper drive bay area on the right side. The lower right side, with the hard drive area, is covered by an EMI shield and a plastic door.

Customized bezels for OEM customers can be designed from the standard bezel design.

2.3 Security

A variety of security options are provided. Padlock loops on the system side cover and a lock on the hard drive inner cover can prevent access to add-in cards and peripherals. Optional cover alarm switches are provided for the side covers and hot-swap bay door. The alarm is transmitted to the baseboard where the user software can process it as desired. Software and BIOS security features are described in the baseboard Technical Product Specification.

2.4 I/O panel

All input/output connectors are located on the back of the chassis. The built-in interfaces on the baseboard are mapped in the figure below.

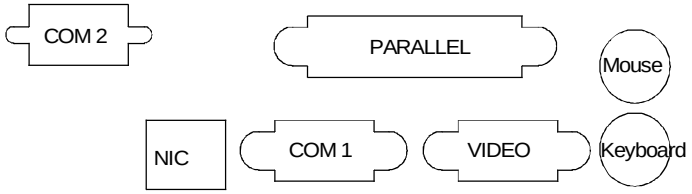

Figure 2-1 I/O Connector Map

2.5 Chassis Views

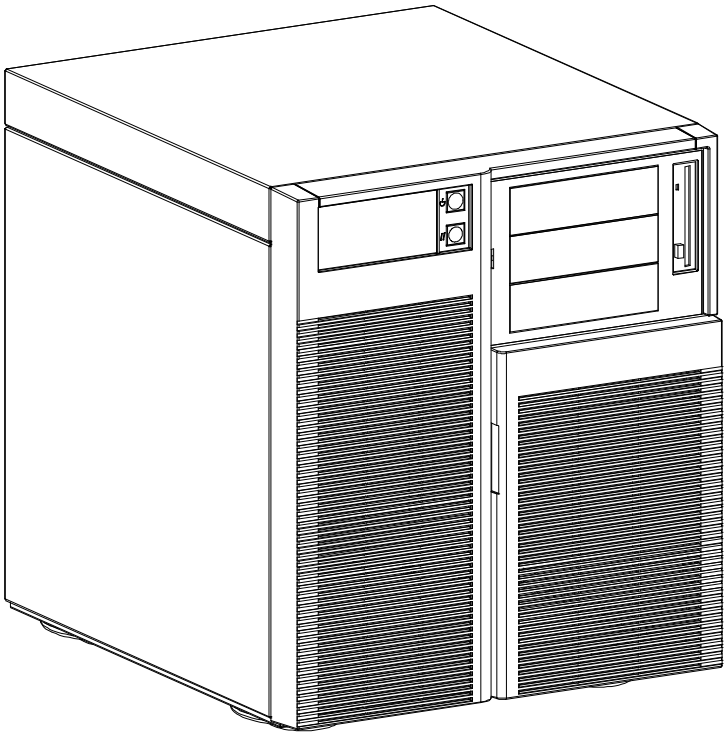

Figure 2-2 Balboa Front Bezel View

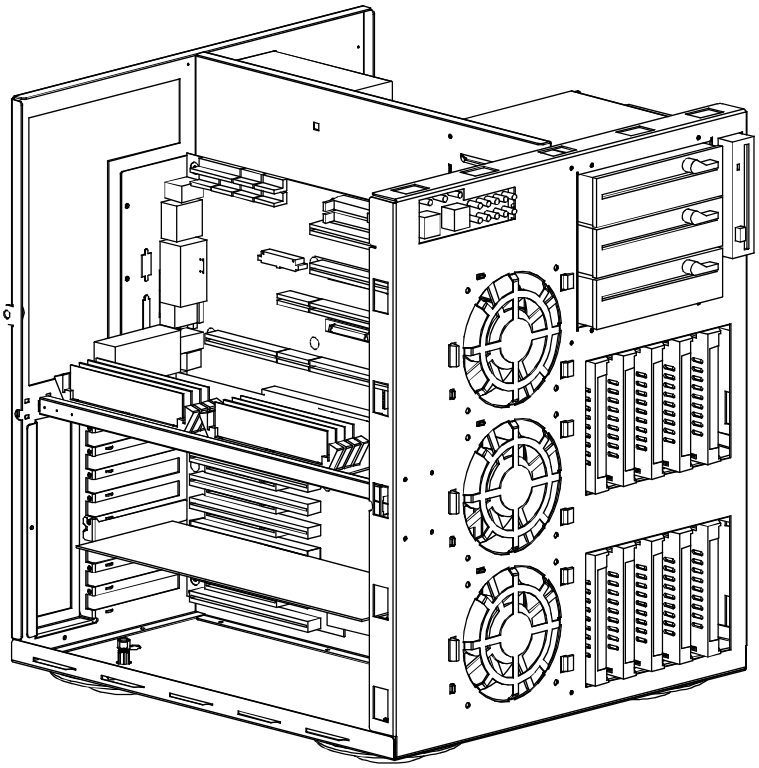

Figure 2-3 Balboa Open Side View

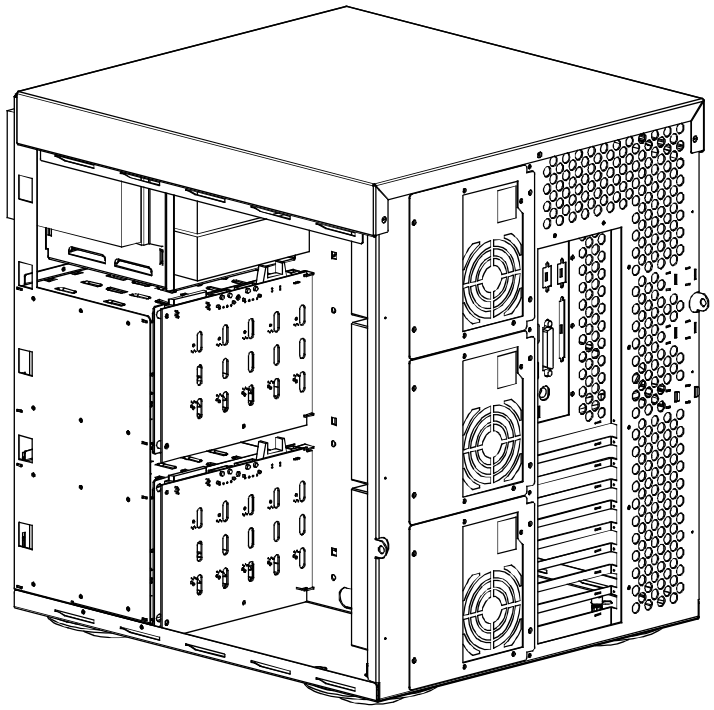

Figure 2-4 Balboa Rear View

2.6 Chassis Dimensions

Table 2-1 Chassis Dimensions

Height	20.25”
Width	17.15”
Depth	19.9”
Clearance Front	8.5”
Clearance Rear	5”
Clearance Side	0” (additional side clearance required for service)
Weight	67 Lb.

3. SYSTEM BASEBOARDS

3.1 B440FX DP Server

The B440FX DP Server supports one or two identical Pentium® Pro processors. The system is fully MPS 1.1 and 1.4 compliant with appropriate Pentium Pro processor extensions, and the memory subsystem supports up to 1GB of system memory using commodity DRAM DIMMs on the processor module. The baseboard provides a connector slot for the processor/memory module. Features of the B440FX DP Server include:

- Pentium Pro processor support 166 MHz/256KB & 512KB, 180 MHz/256KB, 200 MHz/256KB & 512KB
- Dual PCI high-performance I/O segments - PCI-0 (via host bridge) and PCI-1 (via PCI-to-PCI bridge).
- Six PCI and three ISA add-in card slots - one shared slot
- PC-compatible I/O control (serial, parallel, keyboard, mouse)
- Intel 82440FX™ PCIset
- Onboard PCI bus master network, SCSI, and IDE subsystems
- Onboard Cirrus CL-GD54M40† VGA adapter (512KB memory expandable to 1MB)
- Onboard Server Management features

4. SYSTEM POWER

The power system can be configured with one, two, or three power supplies. Each power supply has its own power cord. For redundant level powered systems, the loss of a single power supply will not affect the operation of the system, although care must be taken not to overload a branch circuit of the AC mains by plugging too many supply cords into a single AC circuit. To avoid this, the power supply should be plugged into separate circuits or phases. When multiple power supplies are used, a power share board distributes power.

Current sensing is the power system's other significant feature. Current sensing shuts down the entire power system if any single output from the power distribution backplane exceeds 240VA. This feature enables the system to meet CSA Level 3 operator accessibility without interlocks.

If a single power supply fails in a redundant system, a power supply Failure LED on the front panel will turn on. When the system can safely be shut down, the power supply can be replaced, easily accessible by the right side cover for the cabling. The power supply is inserted into the chassis through the back of the chassis and held in place with a power supply plate.

Table 4-1 330 Watt Power Supply Output Summary (per supply)

DC Power	3.3VDC at 11A Max.
	+5 VDC at 32A Max.
	+12 VDC at 12 A with 16A/12 sec peak current
	-12 VDC at 0.5A
	-5 VDC at 0.5A.
	5V Standby 100 mA,
	Total combined output power of 3.3v and +5v shall not exceed 178W
AC Line voltage	100-120 VAC, 200-240 VAC, switch selectable
AC Line Frequency	50 / 60 Hz
AC Input Current	7A@ 110 VAC /3.5A@ 210 VAC

4.1 330W Power Supply Mechanical Outline

The mechanical outline and dimensions are a custom form factor. The approximate dimensions are 150mm by 150mm by 150mm.

4.2 AC Power Line

The system operates at 50 or 60 Hz, from 100-120VAC, 200-240VAC. The power supply is switch selectable. The system meets these line voltages, and has been tested (but not specified) at +10% and -10% of the voltage ranges, and similarly ±3 Hz on the line input frequency.

The computer operates without error with line source interruptions that do not exceed 20 milliseconds (at nominal line conditions), and at full power supply output load.

The system is not damaged by AC surge ring waves to 3.0kV/500A. This ring wave is a 100kHz damped oscillatory wave with a specified rise time for the linear portion of the initial half-cycle of 0.5µsec. Additionally, the system will not be damaged by a unidirectional surge wave form of 1.5kV /3000A, with a 1.2µsec rise time and 50µsec duration. Further details on these wave forms can be obtained in *ANSI/IEEE STD 28-1974*.

4.3 Power Supply/System Configuration

The system can be configured with a single power supply (entry level power). With a single supply, it will be limited to a dual processor, 512MB memory, five hard drives, and a restricted number of add-in cards. Nevertheless, this entry level configuration allows a wide class of server installations. Power budgets for specific configurations will determine required power configurations.

When configured with two power supplies, the system allows fully configurable systems. The current share uses a proprietary forced current sharing technique that ensures that the current share is less than 5% and has exceptional voltage regulation specifications.

*Table 4-2 System Power Supply Output Summary**

	+3.3V	**+5V**	**+12V**	**-5V**	**-12V**
Entry Level Power - Total combined output power of 3.3v and +5v shall not exceed 178W	11 A	32 A	12 A	0.5 A	0.5 A
Maximum Level Power 2 Power Supplies	20 A	60 A	23 A	1.0 A	1.0 A
Redundant Level Power 2 Power Supplies	10 A	30 A	11 A	0.5 A	0.5 A
Redundant Level Power 3 Power Supplies	20 A	60 A	23 A	1.0 A	1.0 A

*Above specifications are preliminary and subject to change.

The processor module can implement one or two Pentium Pro processors, using onboard DC-DC voltage converters for the CPU core power requirements. These DC-DC voltage converters utilize +12V for the primary processor and +5V for the secondary processor.

4.3.1 Sample Fully Loaded Configuration

Table 4-3 BB440FX DP Server Power

FEATURE	DESCRIPTION	+3.3V	+5V	+12V	+12VPK	-12V	-5V
Processor #2	200/256 3.3V 10.6A 35W		8.23				
Processor #1	200/256 3.3V 10.6A 35W			3.43			
Memory DIMM	8*32MByte 3.3V 1.8A	1.80					
82440FX	DBX+PMC 3.3V 1.2A	0.96					
Processor Bus	Terminator 1.5V 5.42A	3.39					
Logic	Misc.	0.02	0.06	0.03			
Sub Total Module	1 Processor	**6.17**	**0.00**	**3.46**		**0.00**	**0**
Sub Total Module	2 Processor	**6.17**	**8.29**	**3.46**		**0.00**	**0**
Baseboard	Misc.		2.50	0.10		0.05	
Fan	110mm			0.50			
Keybd	K/board-Mouse		0.50				
Sub Total Baseboard			**3.00**	**0.60**		**0.05**	**0.00**
ISA Slot 1	Server Monitor Module		0.10	1.50			
ISA Slot 2	Term Concentrator		1.75	0.50		0.40	
PCI#0 Slot 4	PCI Board 10W		2.00				
PCI#0 Slot 3	PCI Board		2.00				
PCI#0 Slot 2	PCI Board		2.00				
PCI#0 Slot 1	PCI Board		2.00				
PCI#1 Slot 2	PCI Board		2.00				
PCI#1 Slot 1	PCI Board		2.00				
Subtotal I/O, for 8 slots			**13.85**	**2.00**		**0.40**	**0.00**
Total Electronics	1 Processor	**6.17**	**16.85**	**6.06**		**0.45**	**0.00**
Total Electronics	2 Processor	**6.17**	**25.14**	**6.06**		**0.45**	**0.00**
BAY 1	Seagate ST12551N (13W)	0.00	0.90	0.70	2.50		
BAY 2	Seagate ST12551N	0.00	0.90	0.70			
BAY 3	Seagate ST12551N	0.00	0.90	0.70			
BAY 4	Seagate ST12551N	0.00	0.90	0.70			
BAY 5	Seagate ST12551N	0.00	0.90	0.70			
Ext Bay 1	CD-ROM drive	0.00	0.55	1.00	1.80		
Ext Bay 2	Tape Drive	0.00	0.80	1.40	1.80		
Floppy	3.5" drive	0.00	0.25	0.00			
Total Peripheral			**6.10**	**5.90**	**101.30**	**0.00**	**0.00**
Total system 5V PCI, 1 Processor		**6.17**	**22.95**	**11.96**	**14.46**	**0.45**	**0.00**
Total system 5V PCI, 2 Processor		**6.17**	**31.24**	**11.96**	**14.46**	**0.45**	**0.00**
330W P/S	Load profile	11	32	12	16	0.5	0.5
Total Watts 5V PCI, 1 Processor		**20.36**	**114.75**	**143.51**	**0.00**	**6.00**	**2.50**
Total Watts 5V PCI, 2 Processor		**20.36**	**156.20**	**143.51**	**0.00**	**6.00**	**2.50**
Total Supply Watts 1 Processor		**287.13**					
Total Supply Watts 2 Processor		**328.58**					

5. SYSTEM COOLING

Two fans cool the processor and add-in cards in the card cage area, and up to two additional fans can be installed in that area. The power supply fan and an additional fan cool the hard drives. Multiple power supply fans cool the peripheral side**.** If a fan fails, a fault signal is sensed by the baseboard and the fan failure LED on the front panel is turned on. This signal will also be available for server management software functions.

The fans are located behind the side covers. Failed fans can be changed after the system has been shut down.

6. SYSTEM PERIPHERAL BAYS

6.1 Drive Bays

6.1.1 3.5" Floppy Drive Bay

The system ships from the factory with a 3.5" floppy drive installed in the upper right bay. This drive can be accessed by removing the right side cover.

6.1.2 5.25" Drive Bays

The chassis has three 5.25" half height peripheral bays. These bays are designed for peripherals with removable media (floppy disk, CD-ROM or tape drive), and they have removal filler panels when no peripherals are installed.

A single full height bay can be created using any two of the 5.25" bays. The cable from the onboard SCSI controller allows for two 5.25” SCSI devices to be installed in these bays. The SCSI wide cable uses a wide-to-narrow converter for the 5.25” devices, and an IDE CD-ROM can be installed. The 5.25" peripherals can be removed from the front of the chassis, and cosmetic cover panels are installed for all of the unused 5.25" bays by the factory.

Note: These bays are not recommended for a hard disk drive because of hard disk drive generated EMI and increased ESD susceptibility (i.e. less hardened to ESD). These factors are also affected by the manufacturer/drive model that a customer would select. A hard drive will not be integrated into these bays at the Intel factory.

6.1.3 Internal 3.5” Hard Drive Bays with SCSI Hot Swap Backplane

The product contains a bay for five 3.5" hard drives which are accessible from the lower front bezel. A hot-swap capable backplane is part of the 3.5” drive bay assembly. The backplane is designed for Fast-20 SCSI III devices using the industry standard 80-pin SCA II connector.

An optional hot-swap backplane can be installed for a second bay of five drives. An add-in SCSI host adapter, power supply, and power share backplane have to be utilized for the lower hot-swap backplane.

A drive carrier is required as part of the hot-swap implementation. The 3.5" peripherals that are 1.0" high can be accommodated in the carrier. Four fasteners are used to mount the drives in the carrier, and a locking handle retains the carrier in the chassis.

The peripheral bays accept peripherals that consume up to 11 watts of power and are specified with a maximum ambient temperature of 50^{o}C.

A single metal EMI door and a plastic door covers the drive bays.

7. SYSTEM INTERCONNECTION

7.1 Signal Definitions

The pinout on the connectors referred to in this section are defined in the server system user's guide or listed here.

7.2 System Internal Cables

- **Baseboard to Front Panel**

2X8 connectors with 16 wire cable

- **Baseboard to I/O Panel - COM 2**

2X5 connector with 9 wire cable to 9 pin Sub-D serial connector

- **Baseboard to SCSI devices**

68 pin Wide SCSI cable to two wide connectors for 5.25" SCSI devices and to the hot-swap backplane.

- **Baseboard to IDE devices - Optional Cables**

2X20 connectors for 18 inch IDE cable for either an optional hard drive and an optional 5.25" IDE CD-ROM

- **Baseboard to Power Share Board**

2X5 connector with 10 wire cable

- **Front Panel to Hot Swap SCSI Backplane**

2X5 connectors for cabling front panel to hot-swap SCSI backplane.

Second cable is used with optional hot-swap backplane

- **Front Panel Chassis Intrusion Cables**

Three 2-wire cables from chassis intrusion micro-switches to front panel

- **Fan Connectors**

Four 3-pin connectors on baseboard and one 3-pin connector on hot-swap backplanes.

The fan connectors are:

⇒ Pin 1 - ground

⇒ Pin 2 - fault signal

⇒ Pin 3 - +12V.

This pinout is different than the pinouts of previous chassis. The connector is a shrouded keyed connector so that fans cannot be installed incorrectly.

7.3 I/O Panel Connectors

- PS/2 keyboard connector
- PS/2 mouse connector
- Two 9-pin serial ports - one is cabled to the baseboard
- 25-pin parallel port
- 15-pin video port
- RJ-45 Ethernet connector

8. CHASSIS ELECTRONICS

8.1 Power Share Backplane

This chapter discusses the physical size and general requirements for the design and manufacture of the power share PBA for the power share of two or three power supplies. Main features of the power share backplane include:

- I^2C bus
- Report power supply failure
- Max Current Report
- Current usage report
- Number of supplies installed
- Redundant mode report
- 240 VA Limit, meets CSA Level III requirements
- Visual Power Supply subsystem Fail indictors(s)

8.1.1 Power Share Board Description

The board's dimensions are 15.45" x 4.15". To limit access to circuits capable of delivering over 240VA, the board is entirely covered except for the area of the shown below.

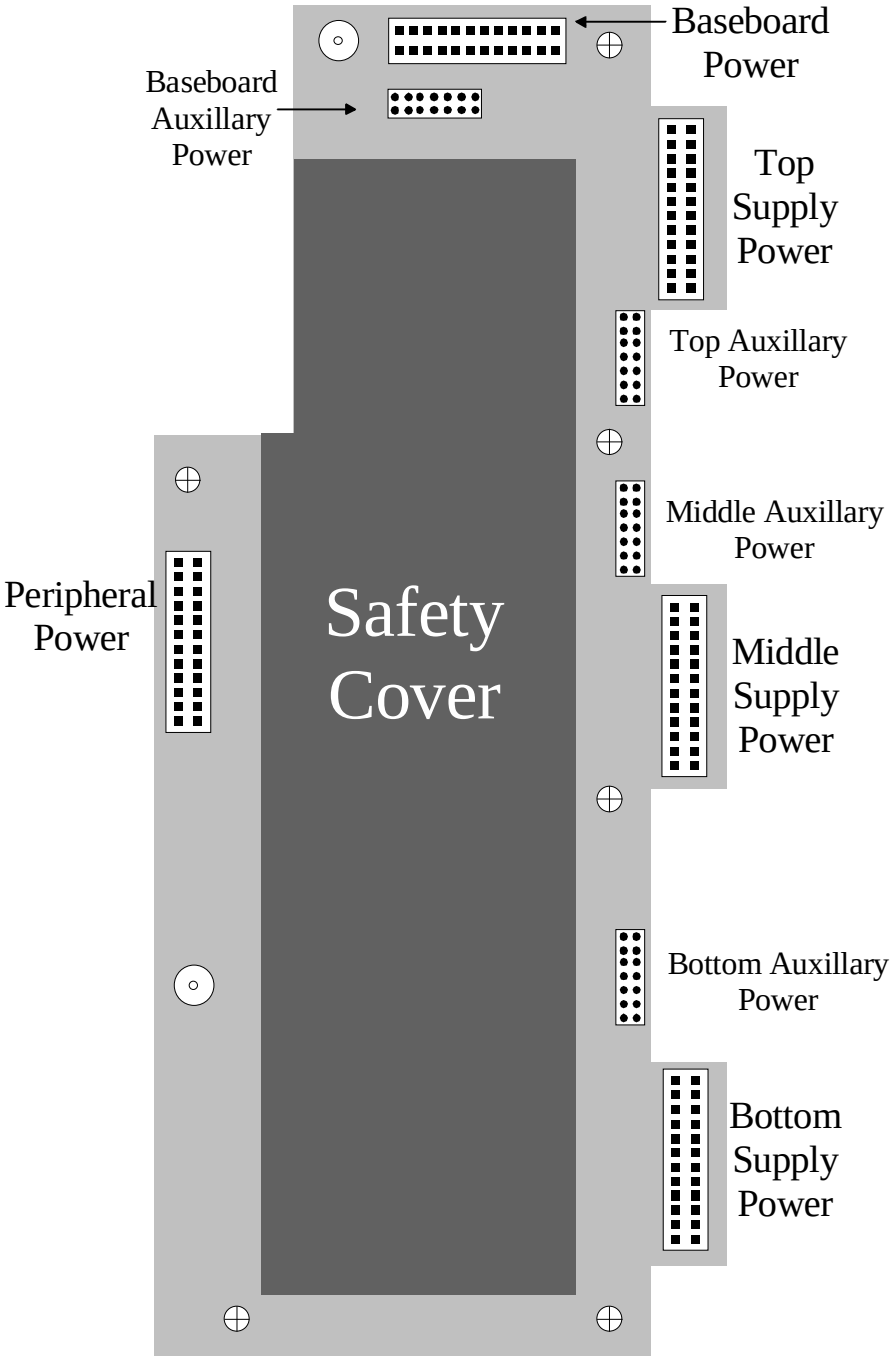

Figure 8-1 Power Share Board Layout

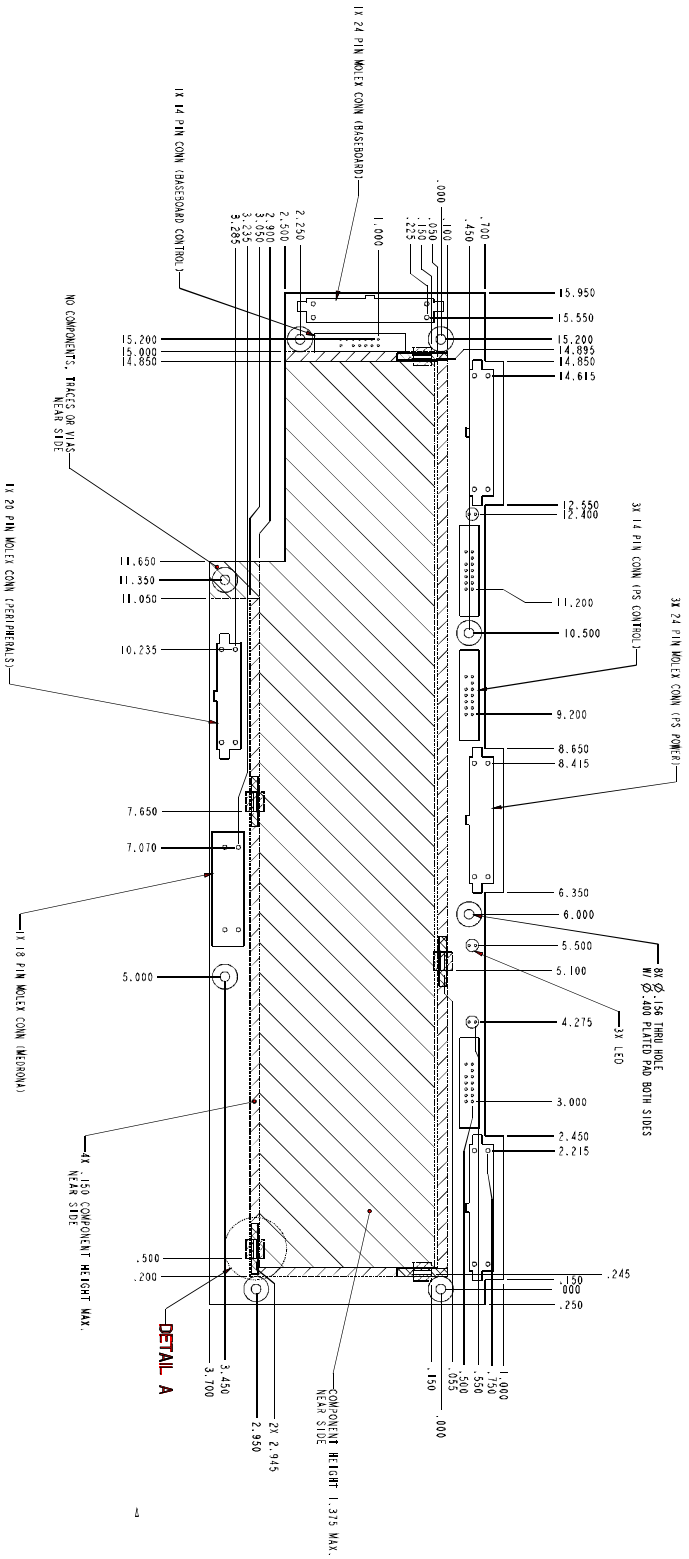

Figure 8-2 Power Share Mechanical Diagram

8.1.2 Power Share Functions

- Power Enable/Disable (PON)

The PON signal is a control signal that originates on the baseboard and is routed through the power share backplane microcontroller. The Backplane Microcontroller monitors the 240VA limit in two zones. If the +5 and +12 power going to the baseboard or the peripherals exceeds 240VA, the backplane microcontroller will de-assert the PON control going to each power supply (J3, J4, J5). This signal is used to enable/disable the power supplies.

- Remote Sense Connections

Remote voltage sense for +5VDC and +3.3VDC is actually done on the baseboard. The +5.0VDC and +3.3VDC remote sense lines are routed through the backplane and connect to the current sense circuitry. The remote sense signals are conditioned by the current sense circuit. Individual remote sense outputs are provided to each of the +5.0VDC and +3.3VDC power supply sections.

The +12V is not sensed remotely - it is sensed on the power share backplane. The load share pass transistors regulate the process.

- Load Share Connection

The power share backplane is installed in systems with two or three power supplies. Each of the +5.0VDC, +3.3VDC and +12VDC outputs from each of the supplies is routed through the power share backplane. The loading of each power supply is controlled by a series FET.

The current from each power supply output is monitored with a zero-drop saturable reactor current monitoring circuit. The primary of the saturable reactor consists of a single large conductor passing through the reactor's toroidal core. Normal load current through the primary is sufficient to cause the reactor to saturate. A ramp-generator connected to the multi-turn secondary of each reactor creates a counter-magnetic field in the reactor. The point on the ramp at which each reactor comes out of saturation provides an indication of the current in its primary. The value of this current is then used to adjust the gate voltage on the series FET and thereby adjust the load share of each power supply output.

- Output Power Connections

Following the load share circuit, +12VDC, +5.0VDC, and 3.3VDC power is routed to the baseboard power connector, J7 and the power connector, J10. Following the peripheral 240VA limit circuit, +12VDC and +5.0VDC are routed to the peripheral power connector, J9.

The -12VDC, -5VDC, and +5V standby outputs are joined together through a diode isolation circuit and connected to the baseboard through connector J7.

- Power Good Circuit

The power good circuit looks at the levels of the power supply good, PGOOD, signals. When a power supply PGOOD, is sensed by the backplane PGOOD circuit, a system PGOOD is asserted after an approximately 550mS delay. Only a single Power Supply PGOOD signal assertion is required to cause the assertion of the System PGOOD.

The following table shows the logic levels for the System PGOOD signal.

- 240VA Monitor Circuit

+5VDC and +12VDC are monitored at two points - the total supply currents and current to the peripherals. Total supply currents form part of the load sharing circuit and monitor the +3.3VDC and the +5VDC and +12VDC. Analog voltages, which represent the total supply currents, are fed to the analog-to-digital converter portion of the backplane microcontroller. The digitized form of these supply currents is used to report the system current usage. Current to the peripherals, which is also monitored, can be determined by the microcontroller by subtracting the peripheral current from the total. If either the baseboard power or peripheral power exceeds 240VA, the backplane microcontroller disables the supply outputs by de-asserting PON. An OFF/ON cycling of the AC line is required to reset the circuit.

- I^2C Communication Circuit

The power share backplane has a microcontroller that uses an I^2C data link to communicate with a similar device on the baseboard. The I^2C link reports the number of power supplies present in the system, current, power to the baseboard and peripherals, and power supply status. I^2C signals are routed through J8 to the system baseboard.

- Power Supply FAULT

Each power supply provides a Power Good, PGOOD, signal which is asserted High. In the event of a power supply failure, the PGOOD signal goes Low. The PON signal asserts the power supply outputs. If PGOOD goes Low, indicating a Power Bad condition, while PON is asserted, a FAULT is generated and applied to one of the FAULT inputs of the backplane microcontroller.

- Power Supply Presence Detect

The DETECT signal senses the number of power supplies (operational or not) in the system. Each power supply presents a grounding connection to one of the backplane microcontroller input pins to show that a power supply is present. If a power supply is not present, the backplane microcontroller input pin will be pulled High though a pull-up resistor to +5V standby.

- FAULT and DETECT Connections to Microcontroller

FAULT and presence DETECT inputs connect to the Port 3 pins of the 83C752 microcontroller (PSBC) .

8.1.3 Backplane Interconnections

- DC Power Circuits (Power Supply-to-Backplane Interface)

A Molex 24 position straight-up Mini-Fit Jr. header (Molex# 39-29-9242) on the power share backplane, Intel part no. 650520-012, is used to connect the +12VDC, +5.0VDC, +3.3VDC, -12VDC, -5VDC, +5V Standby and Ground to the power supply by using a 6 amps/circuit rating on the contacts. Connection is made to the backplane through J1, J2 and J3.

- Signal and Low Current Circuits (Power Supply-to-Backplane Interface)

A 2X5 connector (Intel part no. 109717-010) makes the connection with remote sense and the other control/alarm connections. Control signals connect to the backplane through J4, J5, and J6.

- Backplane-to-Baseboard Power Interface

The power share backplane uses the J7 connector to power the baseboard. The connector on the backplane is a 24-position Molex Mini-Fit Jr. header (Molex# 39-29-9242).

- Backplane-to-Peripheral Interface

J9 supplies +5.0VDC and +12VDC power to the system peripherals. The connector on the backplane is a Molex MiniFit Jr. straight-up header (Molex part no. 39-29-9202) Intel part no. 650520-001.

- Backplane-to-Baseboard Control Connections

J8 connects the I²C, remote sense, and power supply control of the Backplane to the system.

8.1.4 Server Management Architecture - Power Share Subsystem

- Microcontroller Circuit - PSBC

The microcontroller circuit is used to:

1. Provide control for an orderly turn-on of system power.
2. Monitor the power share circuitry and power supplies, reporting status back to the system baseboard.
3. Shut down power supplies if the 240VA limit is exceeded on +5V or +12V loads.

- Power-On

  The Power Share Microcontroller (PSM) circuit includes a special voltage monitor device which keeps the microcontroller chip reset until the +5V standby power has stabilized to greater than 4.5 Volts (the micro's V_{CC} tolerance specification) and keeps the reset active for at least 250 msec to allow the micro to stabilize. During this reset interval 1s are written to all port latches by the PSBC's internal reset function. The power supply power-on (PS_PON) output from the PSM is inverted so that the logic 1 from the port bit represents the power-off state.

- System Current Monitor

The power share board uses the I^2C communications bus to provide a power usage report to the system. The PSM contains five built-in analog-to-digital converters. These converters monitor DC voltage levels supplied by the current sense circuits. The current sense circuits act as a representation of the +3.3V and +5V loads at the baseboard, and +12V load at both the baseboard and the peripheral bays.

If either the +5V or +12V load from the baseboard or the peripherals go beyond the CSA Level III requirement of 240VA, the power will be shut off immediately by de-asserting PS_PON. It is not possible to draw 240 VA from the 3.3 Volt power supply even when three supplies are installed.

A voltage level between 0 to 5 Volts is supplied by the current sense circuits on the power share baseboard. For Balboa, the limit threshold is set to 44 + 4 Amps for each +5 Volt channel and 16 Amps +4 Amps for each +12 Volt channel.

8.2 SCSI Hot-Swap Backplane

This section describes the architecture of the Balboa SCSI backplane: a SCSI backplane board which supports hot-swapping SCSI drives and enclosure management and monitoring functions conforming to the SCSI-Accessed Fault-Tolerant Enclosures specification (SAF-TE).

The Balboa hot-swap SCSI backplane is an embedded application subsystem. During normal operations, the following operations are taking place:

1. Responds to SAF-TE messages (transmitted to the backplane via the SCSI bus)
2. Monitors the state of the power supply sharing board and uses a SAF-TE message to inform the system of any changes in the state of the board.
3. Monitors the temperature on the backplane and reports a warning or critical error if the warning or critical error threshold is exceeded.
4. Monitors the speed of the fan (if present) and reports a warning or critical error if the warning or critical error threshold is exceeded.

The Balboa Hot-Swap SCSI Backplane is made up of the following functional blocks:

- SCSI Bus with SCA (Single Connector Attach) drive connectors, and active terminators
- Microcontroller
- I^2C interface
- SCSI drive power control
- Fault indicator LEDs
- The Hot-Swap SCSI Backplane resides in the hot-swap drive bay of a server. During normal operation, it periodically polls the power-supply sharing board (if it is present in the server) for status information.
- The Hot-Swap SCSI Backplane performs the tasks associated with hot-swapable SCSI drives and enclosure (chassis) monitoring and management, as specified in the SCSI-Accessed Fault-Tolerant Enclosures specification, rev 1.0. These tasks include, but are not limited to, the following:
- Monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages include:
    - Activate a drive fault indicator.
    - Power down a drive which has failed.
    - Report backplane temperature
- Acting as a proxy for “dumb” I^2C devices during inter-chassis communication
- Monitoring the state of the power-supply-sharing board, if it exists.
- Monitoring the state of other hot-swap SCSI backplanes, if there are others in the same chassis.
- All revisions of the firmware will need to be able to perform software upgrades

8.2.1 Board Layout

The following diagram shows the layout of components and connectors on the SCSI backplane printed circuit board.

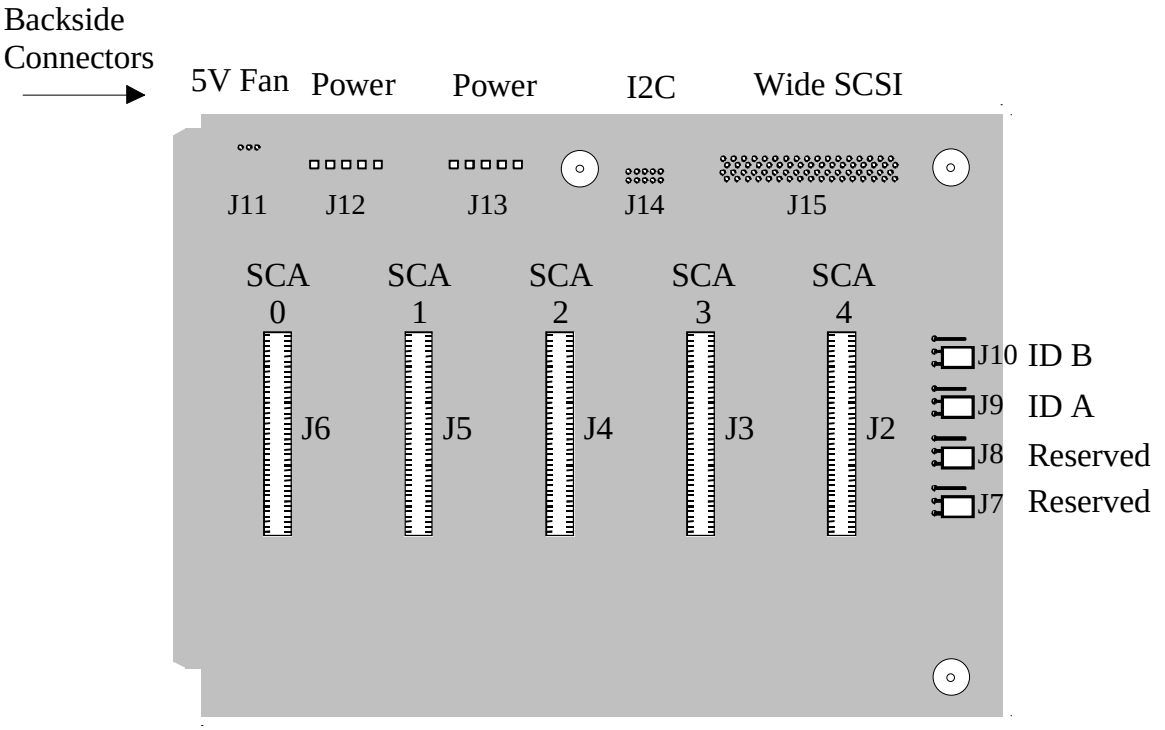

Figure 8-3 Hot-swap SCSI Backplane Component and Connector Layout

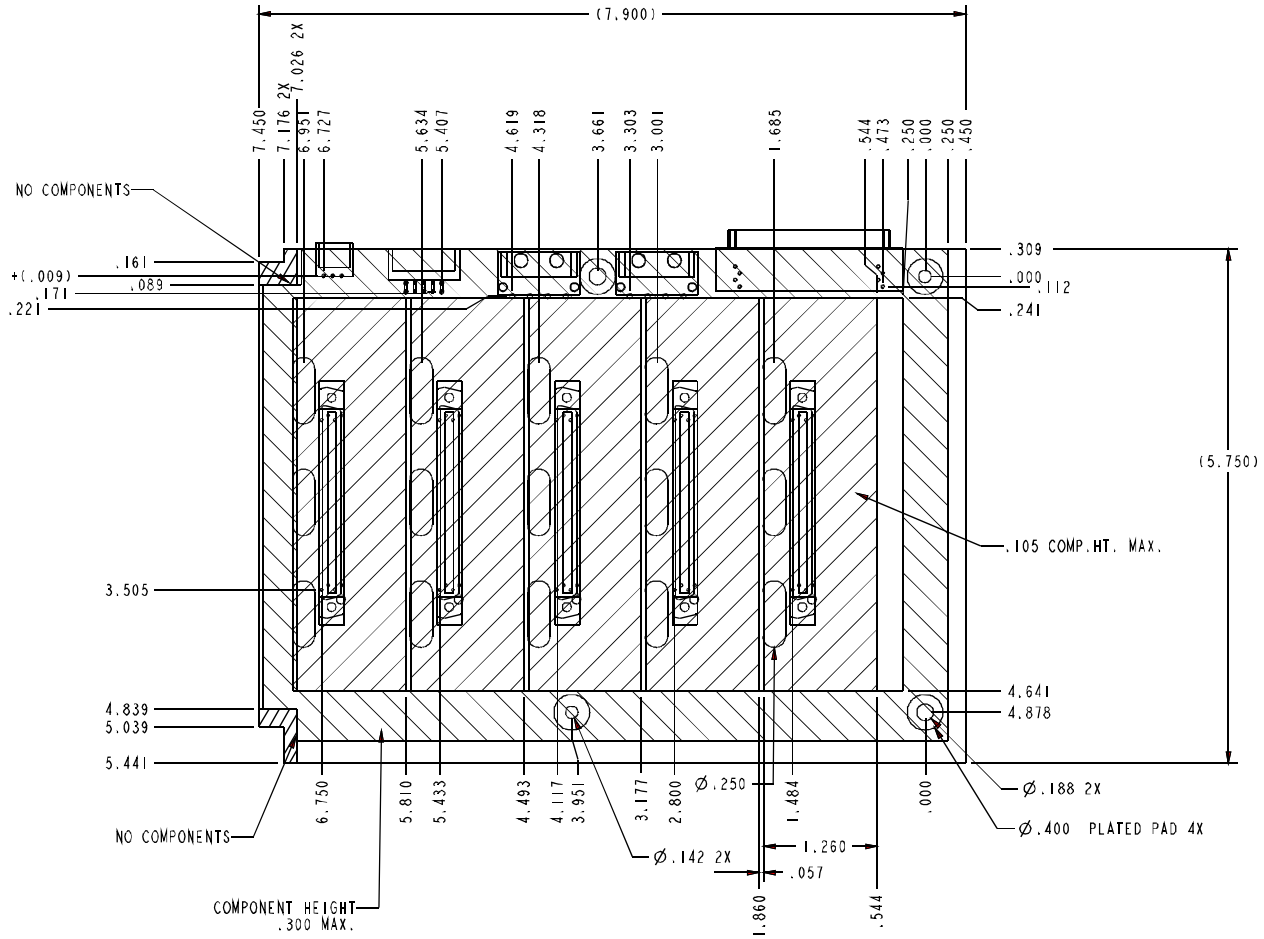

Figure 8-4 Hot-swap SCSI Backplane Component and Connector Layout

8.2.2 Configuration Options

The following table describes the various configuration jumpers on the Balboa Hot-Swap SCSI Backplane along with their function and intended usage.

Table 8-1 Hot-Swap Backplane Jumpers

J9 ID-B	J8 ID-A	Drive 0 (J6)	Drive 1 (J5)	Drive 2 (J4)	Drive 3 (J3)	Drive 4 (J2)
2-3	2-3	ID8	ID9	ID2	ID11	ID12
1-2	2-3	ID0	ID1	ID2	ID3	ID4
2-3	1-2	ID8	ID9	ID10	ID11	ID12
1-2*	1-2*	ID0	ID1	ID10	ID3	ID4

*Jumper Default Setting

8.2.3 Design Constraints and Assumptions

- SCSI bus

The SCSI bus, based on the SCSI-3 specification, allows any SCSI device to communicate with any other SCSI device. The SCSI specification requires that all SCSI devices be at least 0.3m (11.81in) apart (draft-Proposed SCSI-3, section 6.4). Since this hot-swap backplane will violate this specification (drives will be 1.3 in apart), certain constraints must be placed on the backplane in order for the product to operate correctly. Only one initiator is allowed on the hot-swap SCSI bus, and that initiator is the SCSI controller located on the system baseboard. All SCSI devices on the backplane are targets. This arrangement allows communication over the SCSI bus to occur only between the two ends of the bus, significantly reducing the signal reflections, and thereby increasing the signal quality at the receiver.

- Deviations from SAF-TE Specification

The SAF-TE specification, rev 1.00, requires the use of a “PAIR” signal. The intended use of this signal is to allow inter-backplane processor communication. However, this signal has not been used in the designs prior to this one and is not implemented in this design, either.

- Miscellaneous

Per-drive power and activity indicators are somewhat common for a design such as this. To save money, these indicators are not be supported or implemented.

8.2.4 Server Management Architecture - SCSI Subsystem

This section details the architecture of the server management subsystem, including descriptions of functional blocks and how they operate. The following figure shows the functional blocks of the server manager subsystem. An overview of each block follows.

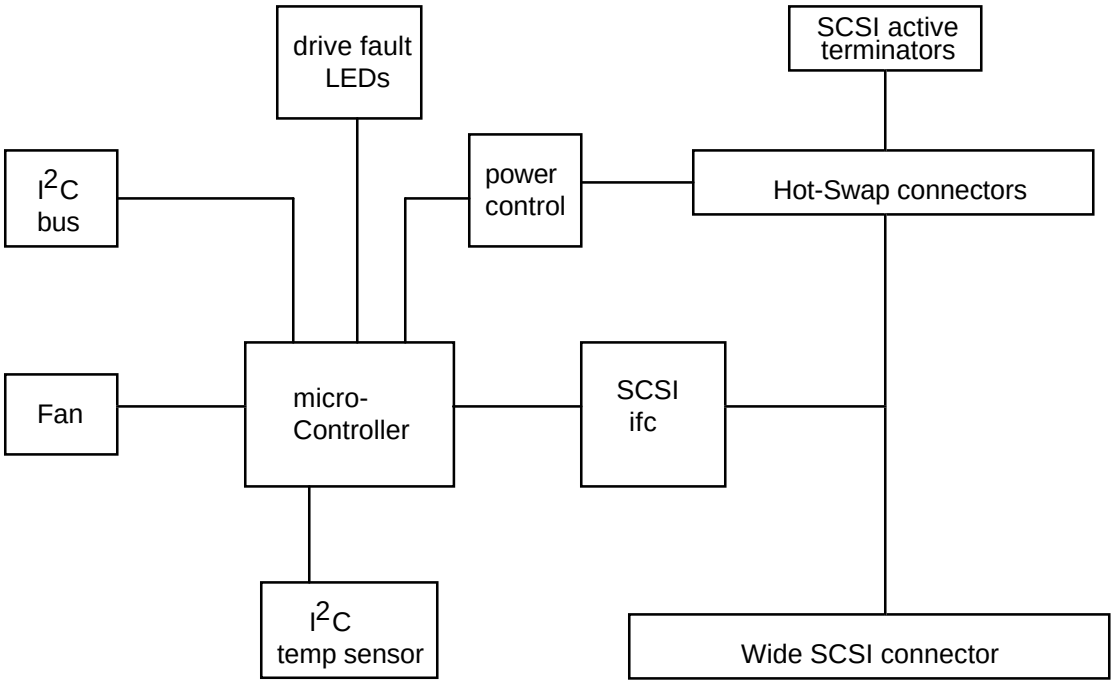

Figure 8-5 Functional Block Diagram

- Hot-Swap Connectors

The hot-swap connectors are SCA (Single Connector Attachment) connectors. Each of the five SCSI drives attaches to the backplane at this point. The SCA provides connection to both the SCSI bus and power.

- SCSI Interface

The SCSI interface controller on the hot-swap backplane provides the interface between the SCSI bus and the microcontroller, which contains all the “intelligence” on the board. Because the SCSI interface only interfaces to an 8-bit microcontroller and does not need high performance functions, it is a very simple, 8-bit wide interface.

- SCSI Active Terminators

The SCSI active terminators provide termination for the hot-swap backplane end of the SCSI bus. The initiator-end of the SCSI bus is also terminated.

- Power Control

Power control is provided to power-down the drive when a failure is detected and reported (via enclosure services messages) to the SCSI bus. This decreases the likelihood that the drive, which may be under warranty, will be damaged during removal from the hot-swap drive bay. When a new drive is inserted, the power control waits a small amount of time for the drive to be fully seated, and then applies power to the drive in preparation for operation.

The hardware will turn off power to a drive slot when it detects that a drive has been removed. This prevents the unwanted condition where a drive is partially removed and re-inserted while full power is available. If this happened, the resultant sags in supply voltages could disrupt the entire SCSI array.

Power control also allows for hot-spare drives. Spare drives are kept in the hot-swap bay, but are left powered down. When a drive fails, the hot-spare can be powered up and put into service without requiring immediate operator intervention to replace the drive.

- Microcontroller

The microcontroller provides all intelligence on the backplane. It is an 80C51-based microcontroller, with a built-in I^2C bus. The microcontroller block includes the ROM or EPROM (built-in or external), and the RAM that the microcontroller needs to operate. The development phase of the backplane will use external RAM and ROM; when the code is stable and sufficiently optimized, mask-ROM parts can be substituted for cost savings.

- Fault LEDs

The drive fault LEDs, which indicate failure status for each drive, are driven by the microcontroller. The LEDs are not physically located on the Hot-Swap SCSI backplane; they are only driven from the backplane. For more information, see the *SAF-TE Specification*.

- I^2C Bus

The I^2C bus is a system-wide management bus. The I^2C bus controller is integrated into the microcontroller. Further information can be found in the *SAF-TE Specification*, and the *I^2C bus Specification.*

- Fan

The hot-swap backplane supports a fan with a digital-output tachometer for speed monitoring. The fan's digital output is connected to an input on the microcontroller. Software monitors fan speed and reports its status.

- Temperature Sensor

The temperature sensor is an I^2C-bus temperature sensor that resides on a private (hot-swap backplane-only) I^2C bus. The temperature information is available to other devices in the chassis through enclosure services messages. The private I^2C bus is a "bit-banged" bus with only one master (the microcontroller) and one slave, the temperature sensor. The firmware must implement the private I^2C bus "manually" by explicitly setting and clearing the clock and data signals, because there is no hardware that directly supports this private bus.

8.2.5 Connectors

- Wide SCSI Connector

The wide SCSI connector is a 0.050” spacing 68-pin, unshielded connector. Signals are described in the board TPS.

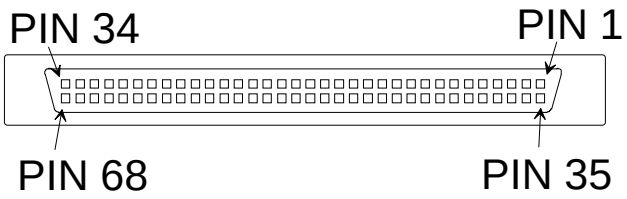

Figure 8-6 Wide SCSI Connector

- SCA Connectors

The five SCSI SCA I connectors are Molex 15-92-10800, .050” spacing, 80-pin, unshielded connectors.

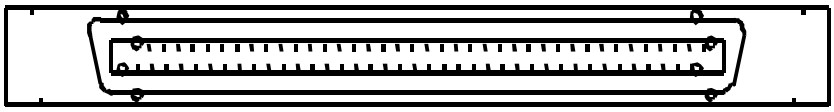

Figure 8-7 SCA Connector

- Front Panel Connector

The front panel 10-pin connector attaches to the system front panel which passes drive management information to the baseboard. Signals are described in the front panel section of this document, in the *Hot-Swap Backplane Connector Pinout* table.

- Fan Connector

The fan connector supports a 3-pin 12V fan. Signals are described in the board TPS.

- Power Connectors

The power connectors are identical to those used on standard peripherals: a 4-pin shrouded plastic connector with mechanical keying.

8.3 Front Panel

8.3.1 Front Panel Overview

The front panel allows mounting and electrical connection for switches and indicators accessible from the front of the chassis, like the power-on/off and system reset. Power-on and disk activity are examples of indicators mounted on the front panel board which are viewable at the front of the chassis.

The front panel contains three switches and 14 LEDs. It also contains a 16-pin baseboard connector, three 3-pin chassis intrusion connectors, and two 10-pin connectors which are used to connect to the two potential hot-swap drive backplanes in a system. The hot-swap drive backplane connectors contain the I^2C bus passed from the baseboard and the signals to drive the five error LEDs for the respective hard drive backplane. Of the remaining four LEDs, one indicates power is on, two are used to indicate fan and power faults, and one indicates hard drive activity. The three switches control power-on, reset, and NMI.

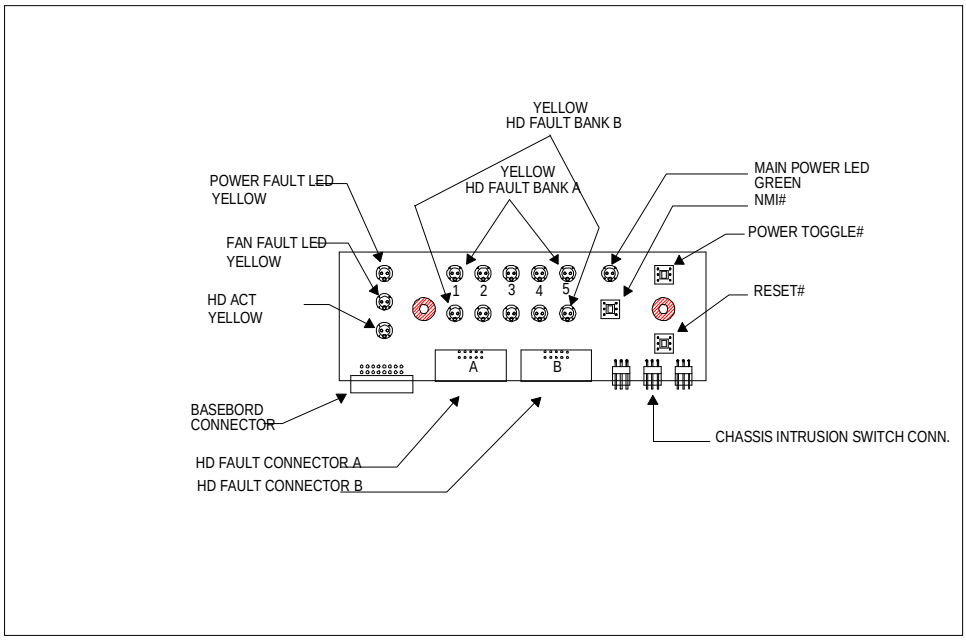

Figure 8-8 Balboa Front Panel Layout

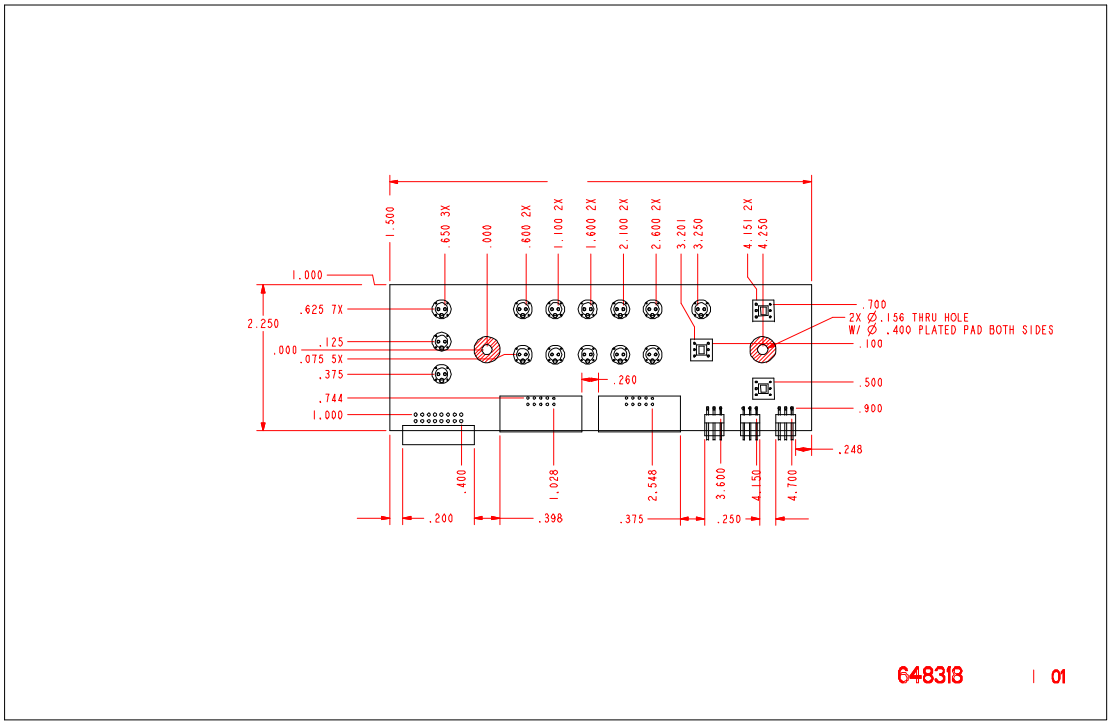

Figure 8-9 Front Panel Mechanical Diagram

- Front Panel Connectors

Table 8-2 Front Panel Connector Pinout

Name	Description
GND	0V
Hard Drive-Activity	TTL Low true = hard disk activity, requires series R for LED
Reset	TTL Low True = reset system
Power-Control	TTL Low True = toggle system power
VCC	+5V
N/C	Spare
NMI	TTL Low True = NMI to CPU
VCC	+5V
Fan-Failed	TTL Low True = fan failed, requires series R for LED
Chassis - Intrusion	TTL High True = chassis intrusion, This signal comes from the chassis
Power-Fault	TTL Low True = power fault condition, requires series R for LED
+5V-STBY	+5V-Standby
I^2C-SDA	I^2C - SDA (Serial Data)
GND	0V
I^2C-SCL	I^2C - SCL (Serial Clock)
GND	0V

Table 8-3 Balboa Chassis Intrusion Switch Connector Pinout

Pin #	I/O	Description
1	O	TTL High True = Chassis switch
2		Chassis switch return (GND or output of next chassis switch connector)
3	O	TTL High True = Chassis switch

Table 8-4 Hot-Swap Backplane Connector Pinout

Name	Description
GND	Electrical ground (0V)
I2C_SDA	I^2C SDA (Serial Data)
GND	Electrical ground (0V)
I2C_SCL	I^2C SCL (Serial Clock)
RFU	Reserved for future use. No connections to this signal or pin are allowed.
FAULT1#	Fault signal for drive 1 (logical drive 0). Active low signal
FAULT2#	Fault signal for drive 2 (logical drive 1) . Active low signal
FAULT3#	Fault signal for drive 3 (logical drive 2) . Active low signal
FAULT4#	Fault signal for drive 4 (logical drive 3) . Active low signal
FAULT5#	Fault signal for drive 5 (logical drive 4) . Active low signal

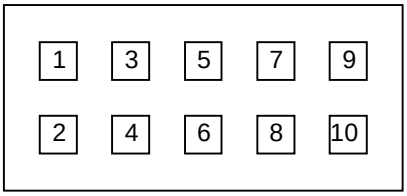

Figure 8-10 HD Backplane Connector Diagram

Table 8-5 Balboa Front Panel LED Current

SIGNAL NAME	RECOMMENDED SERIES R VALUE	MAX CURRENT	LED COLOR
PWR_GOOD	150 ohms	20 mA	GREEN
HD_FAULT_1..4#	100 ohms	35 mA	YELLOW
HD_ACTIVITY#	100 ohms	35 mA	YELLOW
FAN_FAIL#	100 ohms	35 mA	YELLOW
POWER_FAULT#	300 ohms	10 mA	YELLOW

- I^2C Diagnostic Bus

The baseboard connects the I^2C interface to the front panel. This bus is not used on the front panel, but is passed through the front panel to the connectors for the hard drive backplanes. The I^2C bus is then utilized by the hard drive backplanes to pass error information back to the baseboard.

9. CERTIFICATION

9.1 Safety

9.1.1 USA

The system is UL listed to UL 1950, 3rd Edition.

9.1.2 Canada

The system is certified by UL (cUL) to meet the requirements of CSA C22.2 No. 950-M93. The product bears the cUL mark.

9.1.3 Europe

The system is certified to meet the requirements of EN 60 950 with amendments by TUV (GS License).

9.1.4 International

The system is certified by NEMKO to meet the requirements of EN 60 950 with amendments and Nordic deviations, and IEC 950 with amendments.

9.2 Electromagnetic Compatibility

9.2.1 USA

The system is certified to FCC CFR 47 Part 15, Class B

9.2.2 Canada

The system complies with the limits for radio noise emissions from Class B digital apparatus as required by Industry Canada (IC).

9.2.3 Europe

The system complies with the EU EMC directive (89/336/EEC) via EN 55022, Class B and EN 50082-1. The product carries the CE mark. The system is tested to the following immunity standards and maintains normal performance within these specification limits:

IEC 801-2	ESD Susceptibility (level 2 contact discharge, level 3 air discharge)
IEC 801-3	Radiated Immunity (level 2)
IEC 801-4	Electrical fast transient (level 2)

9.2.4 International

The system is compliant with CISPR 22 class B

9.2.5 Japan

The system is registered with VCCI and complies with VCCI Class 2 limits (CISPR 22 B Limit).

10. RELIABILITY, SERVICEABILITY, AND AVAILABILITY

10.1 Mean Time Between Failure - MTBF

The Mean-Time-Between-Failures (MTBF) data is calculated from predicted data.

Table 10-1 System MTBF

Sub Assembly Description	Calculated MTBF (in hours)
Sample Baseboard (B440FX)	62,065
Sample Processor / Memory board (B440FX)	152,088
SCSI Hot plug BP	109,373
Front panel board	1,491,808
VRM linf 12V/5V	186,315
Power backplane	67,411
Power supply	100,636
1.44MB 3.5" FDU	405,000
Complete System	**15,359**

10.2 Serviceability

The system should only be serviced by qualified technical personnel.

The desired MTTR of the system is 30 minutes, including diagnosis of the system problem. To meet this goal, the system enclosure and hardware have been designed to minimize the MTTR.

Following are the maximum times that a trained field service technician should take to perform the listed system maintenance procedures, after diagnosis of the system.

Table 10-2 Maximum Time for Maintenance Procedures

Procedure	Time
Remove cover	1 minute
Remove and replace disk drive	1 minute
Remove and replace power supply	5 minutes
Remove and replace fan	5 minutes
Remove and replace expansion board	5 minutes
Remove and replace front panel board	5 minutes
Remove and replace baseboard (with no expansion boards)	10 minutes
Remove and replace power backplane	15 minutes
Remove and replace SCSI backplane	15 minutes
Overall MTTR	20 minutes

11. ENVIRONMENTAL LIMITS

11.1 System Office Environment

Table 11-1 System Office Environment Summary

Operating Temperature	+5^{O}C to +35^{O}C Maximum rate of change of 10^{O}C per hour.
Non-Operating Temperature	-40^{O}C to +70^{O}C
Non-operating Humidity	95%, non-condensing @ 30^{O}C
Acoustic noise	< 45 dBA at typical office ambient temperature (65-75F)
Operating Shock	No errors with a half sine wave shock of 2G (with 11 millisecond duration).
Package Shock	operational after a 24 inch free fall, although cosmetic damage may be present
ESD	20kV per Intel Environmental test specification

12. DIAGNOSTICS

12.1 MTA TestView

Standard Intel server systems ship with a floppy-based diagnostic capability. This diagnostic is called PCDIAGS, or TestView. TestView is the menu interface for MTA (Modular Test Architecture) test programs and support files. Two interfaces exist for the MTA tests. The first is TestView, which is a menu interface for Windows. The other program is T (T.exe), which is the command line interface, meaning that it can be accessed at the command line prompt without having a hard drive installed. Both interfaces allow users to run test sequences through a numerical mapping. In both cases, a PKG file is used to map names and numbers to a test invocation line.

12.2 Main Menus

TestView displays a horizontal bar across the top of the screen displaying the main menus that are available. The menu list and its functions are as follows:

TEST	Access to test modules and subtests.
ERRORS	View history of error messages.
SUMMARY	View summary of test run.
CONFIGURATION	Menu and system configuration tools.
OPTIONS	Changes the way tests are run.
HELP	On-line help for using TestView menus.
QUIT	Exits TestView and returns to DOS.

12.3 Starting Tests

There are several ways to start tests. The following table summarizes the possibilities.

Table 12-1 TestView Startup Options

	TEST menu	**SUBTEST menu**
All modules	ALT-F2	---
One module	F2	ALT-F2
One test	---	F2 or ENTER

When F2 or ALT-F2 is used, the operator is prompted for the number of loops desired. If ENTER is used in the SUBTEST menu, the test will be run once, no questions asked.

12.3.1 Execution Sequence

The tests will execute in the same order as they appear in the menus. The order may be changed by using CTL+D and CTL+A or editing the PKG file. The subset of tests run may be changed by using F3 and F4 to enable and disable subtests or modules.

12.3.1.1 Test Window

Each time a test is run, its output appears on a window. Some tests, like the video test, will use the whole screen for a window. When the test has completed, the message “press any key to continue” is displayed. If the desired message scrolls off the screen, use F7 or the ERROR menu to review the output.

12.3.2 Error Messages

The error messages from a test are directed to the console or test window. It is possible to change the destination of the error message by changing the /Rx run-time flag (where x can be R,E,A or S). This can be done using the “Options” menu or the function key F5. Any messages redirected to a file can be viewed using the “Errors” menu or the function key F7. The error message buffer file is normally set to record only error messages. If “status” or “advisory” messages are desired, use F5 to change the global run-time flag “/RE test.out” to “/RR test.out”.

12.4 Run Time Environment

When booted from diskette, TestView runs from the RAM drive. The AUTOEXEC.BAT file on the boot diskette sets up a RAM drive before invoking TestView. TestView uses the RAM drive as a virtual cache by copying those tests selected for execution to the RAM drive and then running them. Once a test EXE file is loaded, it remains on the RAM drive. If the RAM drive becomes full, TestView removes it from the RAM drive before copying the next test to the RAM drive. TestView and all of its test module files can be copied to a hard drive or another floppy and executed from there. It will run exclusively out of the directory in which it was placed, either hard disk or floppy.

Using the RAM drive is faster, but modified files will disappear when the power goes off. This can be avoided by specifying a path name on non-volatile media when possible or using DOS to copy files.

12.4.1 Stopping Tests

Control-C or Control-break will stop tests. Control-C will not be seen if the input buffer already has something in it. Control-break is more responsive, but could interrupt a critical DOS function. The amount of time a test takes to respond to Control-C will vary, depending on the type of loop that is running and the amount of clean-up that must be done.

12.4.2 CFG parameters

Each MTA test is designed to handle a range of device and/or peripheral implementations by using hardware configuration parameters instead of hard-coding. The specific parameters vary among the test modules, but each is described by its label and assigned a value.

The parameters may be found in one of two places: the PKG file or the CFG file. The ts_getcfg_xxx calls access the parameters in both locations. Any parameter found in the PKG file takes precedence over ones found in the CFG file. The default CFG file has the same base name as the load file. It has a “.CFG” suffix instead of “.EXE”. If the filename is different from the load file, it must be declared on the test invocation line using /CF <file name>. The file contains one line for each parameter, and may also contain comments. The format of a line specifying a parameter is:

<module name>.<parameter name> = <value>

The value can be a number or a string. Quotation marks are used to force a number to be interpreted as a string or to force spaces to be imbedded in the string. The maximum length of a value string is 256 characters. CFG parameters may occur in the PKG file as well as the CFG file. Parameters which occur in the PKG file override the values found in the CFG file. The F6 function key edits the parameters. Parameters which occur in the PKG file are listed after those found in the CFG file. They are set apart by the fact that the module name is in brackets. Even in the case of name conflicts all parameters from both sources will be listed. If the changes are saved, a file of the same name is written to the RAM drive. This means that the changes will only be in effect for the current session. To save changes to the CFG file it is necessary to exit to DOS and copy the new file to the floppy.

12.4.3 PKG File

The PKG file is an ASCII (readable) file containing a description of each module and subtest in the package. The PKG file is separated into groups of subtests belonging to modules. In addition to subtests, module groups may contain CFG parameters. The file may also contain one or more product-code sections. This file creates the logical mapping between test names and their corresponding EXE files and parameters. The order of the subtests and modules in the file determines the numerical labeling. This numerical labeling may be used to reference the tests when invoking them from the command line using T.EXE. The PKG file is case insensitive (upper and lower case letters considered the same) and may contain comments. The comments are placed between /* and */ symbols and may not be placed on lines with subtests or parameters.

12.4.4 TestView Command Line Flags

The TestView command line may contain any of TestView flags and/or any run time flags. The TestView flags are described below.

- /AUTO [<filename>]

Auto integrate. This parameter causes TestView to perform a self configuration, display the hardware detected in the system, append the selfsens.cfg file to the PKG with a product code heading and invoke any tests found in the PACKAGE.INTEGRATION_LIST parameter. If <filename> is present, the contents of the file specified are appended to the selfsens.cfg file.

- /EXIT Exit

When finished with TestView, this runs all tests from the run-list, when used with /RUNALL. Then it exits without operator intervention.

- /HOURS <nn.n>

Sets the duration of testing. After <nn.n> hours has elapsed, testing will halt. This is used in combination with other flags, like /RUNALL or /SHUFFLE, and <nn.n> becomes an upper limit, not a guaranteed duration.

- /RUNALL [<nn>]

Runs all enabled tests automatically. After tests are run, the menus are up and ready for input. The <nn> argument indicates the number of passes to be taken through the run-list. Zero (0) or omitting <nn> indicates that it will run forever.

- /PC <product-code>

Product code selection. This flag causes TestView to search the PKG file for a section labeled <product-code>. This section is then processed. All processed parameter definitions and test exclusions will override previous settings from the PKG file.

- /PKG <filename>

Causes TestView to use <filename> instead of T.PKG

- /SELF [<filename>]

Self sense. Probes the system hardware and sets CFG parameters appropriately. The “sensed” hardware is presented to the operator for approval. The optional <filename> specifies a default PKG file when the BIOS ID matching fails.

- /SHUFFLE [<nn>]

Shuffle test order. This flag causes all enabled subtests to be shuffled and run before the menus begin accepting input. The optional <nn> argument determines the number of times through the list. Omitting <nn> will cause the subtests to run forever, assuming no /RUNALL flag.

- /TITLE text

Over-rides the default banner at the top of the TestView screen.

12.4.4.1 T Tests

Here are some examples of running tests with T.

Table 12-2 Running Tests with T

T	Run all enabled subtests in all modules in the PKG files.
T FLOPPY	Run all enabled subtests in the floppy module.
T 1.1	Run the first subtest of the first module in the PKG file, if enabled.
T FLOPPY.1	Run the first subtest of the FLOPPY module, if enabled.
T 1 - 5	Run all enabled subtests of the first 5 modules in the PKG file.
T 1.3 - 1.7	Run all enabled subtests in the range 3 through 7 of the first module in the PKG file.
T {1,5,7}	Run all enabled subtests in modules 1, 5 and 7.

The <flags> parameter can be any number of valid flags which are either handled by T or passed on to the test.

The <tests> parameter has a rich syntax, to allow for flexibility. The terse definition is as follows.

(note: |[] and <...> are meta symbols)

(note: no spaces allowed)

<tests> = <runlist>|<range>|<logical>[*<count>]<runlist> = {<tests>[,<tests>]}<range>=<logical>[-<logical>]<logical> = <label>[.<label>]<label> = string|number

When the hyphen (-) is used, all the enabled tests listed in the PKG file between (and including) the two specified tests are run. When specifying a single subtest it is necessary to separate the module name and the subtest name with a dot (.). Both the module name and the subtest name may be specified as either a number or a string. Both of these mappings are determined by the t.pkg file. An empty runlist may be specified as {}.

APPENDIX A - SPARE PARTS

Table 13-1 Spare Parts

	Item Number	Description	Comments
1	651031	CHASSIS ASSY,BALBOA	Main Chassis Assembly
2	651399	COVER,SIDE	Chassis Side cover
3	651351	KIT, BUCKEYE MOUNTING HW	I/O plate EMI Gasket, baseboard mounting clips, bumpers
4	657372	ASSY., MODULE RAIL	Processor card mounting rail
5	651009	CA,FLOPPY,BALBOA	Floppy Cable for one floppy device
6	651010	CA,WIDE SCSI,BALBOA	Cable - 68 pin wide SCSI cable, 2 connectors (One device & controller)
7	651011	CA,PSB_PER BAY, BALBOA	Cable - Power share board to peripheral bays
8	651012	CA,INTRUSION,BALBOA,FRNT	Item 641476 + mounting bracket Hot Swap intrusion switch assembly.
9	651013	CA,FRNTPNL_BB,BALBOA	Cable - Front panel to baseboard
10	651015	CA,FRNTPNL_HSBP2,BALBOA	Cable - Front panel to SCSI Hot swap backplane
11	651016	CA,PSB_24,BALBOA	Cable - Power share board main baseboard 24 pin connector
12	651017	CA,PSB_CONTROL, BALBOA	Cable - Power share board baseboard auxiliary power connector
13	651018	CA,COM2,BALBOA	Cable for Serial COM2
14	651019	CA,EXT,SINGLE PS,BALBOA	Cable - Power harness for single supply system (both main & auxiliary)
15	641476	CA,ALARM,PK	Cable and Chassis Intrusion Switch
16	653973	ADAPTER,SCSI,50P/68P,F/F	Adapter for 68 pin cable to 50 pin SCSI device
17	651040	FAN,ASSY,12V,92MM,45CFM	Fan
18	652012	KIT,FAN ASSEMBLY,BALBOA	Fan and mounting hardware
19	648331	CARDGUIDE	Adapter card guide
20	659250	RAIL,ASSY,PERIPHERAL	Rails for mounting peripherals in 5.25" drive bays (+EMI clips)
21	648319	CARRIER,HDU,3.5"	Hot swap drive carrier - plastic
22	651653	BEZEL ASSY,BALBOA I	System plastic front bezel
23	651034	PBA,FRNT PNL,BALBOA,PROD	Front panel circuit board
24	654315	TA,CNTRY KIT,BALBOA,US	Country kit includes: - Power cord - 2 drive rail sets - System User's Guide - SCSI S/W Guide - LANDesk Guide - System Software - * Video Drivers * SCSI Drivers * Network Drivers * SCU * Diags * LANDesk Server Manager

APPENDIX B ACCESSORY LIST

KIT DESCRIPTION	CONTENTS	ORDER CODE	NOTE	TARGET PLATFORM
2nd CPU kit	No CPU, directions, heat sink, VRM, Clips, Grease	ABUC2NDCPUA	Must purchase CPU separately	Board B440FX / Col-2 B440FX / Balboa NR (non redundant) B440FX / Balboa R (redundant)
Wide SCSI cable	SCSI cable 2x wide to narrow converters	ACOLBUCWSCSIA		B440FX / Col-2
Fan Kit	2 x fans 1 x housing 2 x adapters instructions	ABALBUCRCOOLA		B440FX / Balboa NR
Power supply upgrade kit	No Power supply, 1 x PS share board, 1 x cover, cables, manual, AC cord (US), AC warning label	ABALBUCRPWRA	Must purchase 330 watt power supply (PFC or Standard) separately - See below	B440FX / Balboa NR
Balboa Power supply standard	1 Balboa power supply, instructions	ABALBUCPS1A	Must have existing PS share board or purchase kit: ABALBUCRPWRA	Balboa
Balboa Power supply PFC	1 Balboa power PFC supply, instructions	ABALBUCPS2A	Must have existing PS share board or purchase kit: ABALBUCRPWRA	Balboa
2nd Drive Array	5 x drive trays, EMI clips, wide SCSI cable, instructions, SCSI backplane	ABALBUC2NDHDA		B440FX / Balboa NR