# Intel AP450GX MP Server Board Set

*Technical Product Specification*

## Revision History

| Revision | Revision History | Date |
|---|---|---|
| -001 | Preliminary release of the AP450GX MP Server Board Set Technical Product Specification | 7/96 |
| -002 | Second release of the AP450GX MP Server Board Set Technical Product Specification with additions and corrections. | 3/97 |

This product specification applies only to the standard AP450GX MP Server Board Set with BIOS identifier CD0.

Changes to this specification will be published in the AP450GX MP Server Board Set Specification Update before being incorporated as a revision to this document.

The AP450GX MP Server Board Set may contain design defects or errors known as errata which may cause the product to deviate from published specifications

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# 1 Board Set Description

## 1.1 Overview

The AP450GX MP Server Board Set is a modular, high performance server system capable of supporting up to four Pentium® Pro processors. The board set includes the system baseboard, one or two processor modules, a memory module, and an optional bus terminator module.

| Board Set Feature | Description |
|---|---|
| Multi-processing support | Two expansion slots for processor modules; up to four Pentium® Pro microprocessors (two on each module). The system may include one processor module and one terminator module, or two processor modules. |
| Upgradable memory | One expansion slot for a memory module, supporting up to 1GB of memory using 64 MB SIMMs. The module will support up to 2GB of memory using 128MB SIMMs. An alternate memory module is available to support up to 4GB of memory using 128MB DIMMs. |
| Bus Termination Module | Required per the GTL+ processor bus specification if only one processor module is installed in the system. |
| PCI bus support | Two PCI "peer" buses, each with three 32-bit PCI slots on the system base baseboard. |
| EISA bus support | Four dedicated EISA bus master slots on the system baseboard. |
| SCSI controller | Two PCI based, integrated AIC-7880 controllers; fast and wide, Fast 20/Ultra SCSI-2 support. |
| Integrated Drive Electronics (IDE) interface | Provides access to two IDE hard drives; ISA-based controller. |
| BIOS | Basic Input/Output System (BIOS) stored in enhanced 512 KB (4Mbit) Paged flash memory device. |
| Video controller | Integrated ISA based CL-GD5424 super VGA controller shipped with 512 KB of video memory (expandable to 1 MB). |
| External device connectors | Onboard connectors for 2 serial ports, parallel port, PS/2-compatible keyboard and mouse, and VGA monitor. |
| Clock | Real-time clock/calendar (RTC) chip with 8 KB of NVRAM. |
| Flash memory | Contains Power-on Self Test (POST), BIOS core and Setup utilities. |
| System hardware monitoring | Detects chassis intrusion and contains sensors for temperature, voltage, power supply and fan failure. |
| $I^2C$ Bus Support | $I^2C$ bus connects all major system components together for diagnostic information |
| Configuration utilities | System Configuration Utility (SCU) and SCSISelect Utility |

The following diagram shows the functional blocks and system architecture.
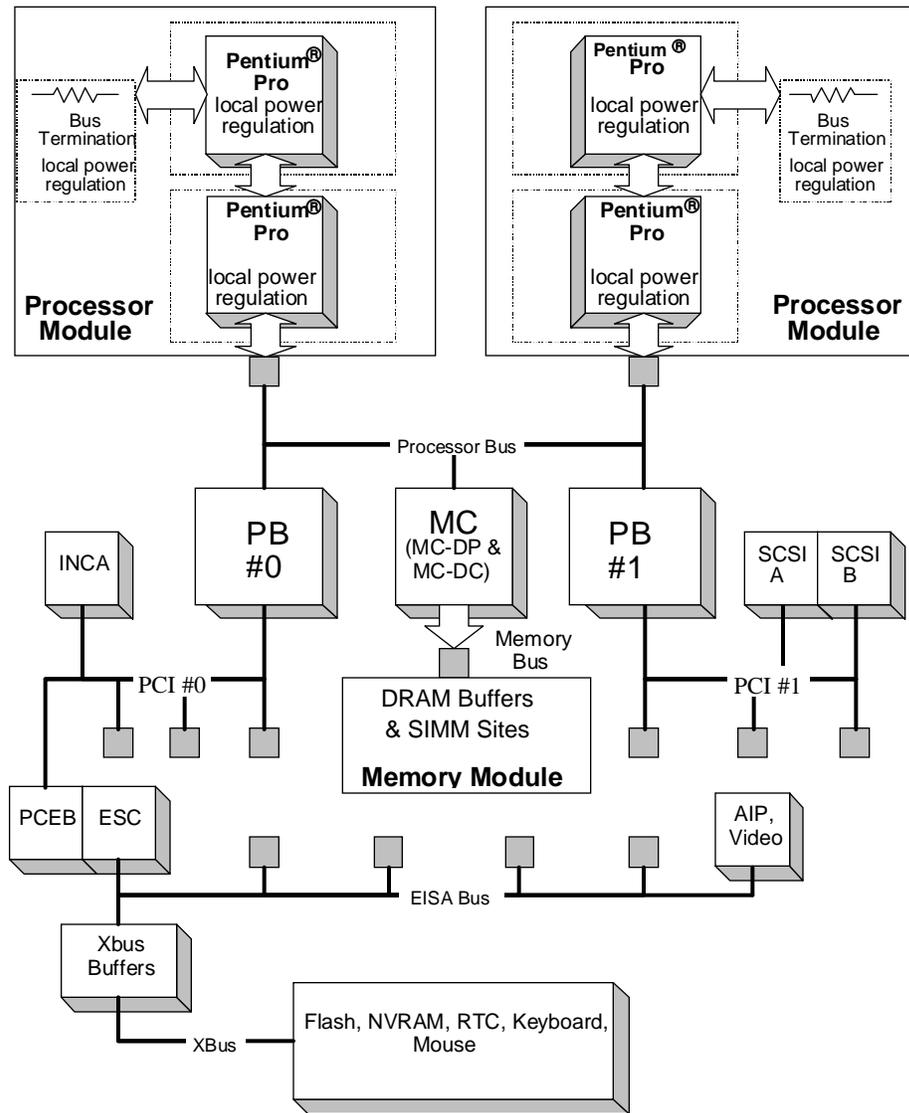


**Figure 1.1 System Block Diagram**

## 1.2 Board Set Options

The server design allows expanded processor and memory capacity.

- Baseboard has two slots for processor modules and one slot for the memory module.

- Each processor module may contain one or two processors, for a configurable range from one to a maximum of four processors.

- A bus termination module is available to terminate the processor bus if only one processor module is installed in the system. Both processor slots must be filled to correctly terminate the processor bus.

- The standard memory module will support up to 2GB of memory using 128MB SIMMs.

- An optional memory module with 32 DIMM connectors is available which will support up to 4GB of memory using 128MB DIMMs.

- The video memory is expandable up to 1MB with a 512KB memory component.

## 1.3 Form Factor

The board set is designed to fit into a custom form factor chassis. Currently Intel's chassis, identified as the AP450GX Chassis, is the only Intel designed chassis qualified for the AP450GX Board Set.

# 1.4  Placement Diagrams

The following diagram shows the placement of major components and connector interfaces on the system baseboard, and the modules.  See Chapter 5 for complete mechanical drawings.
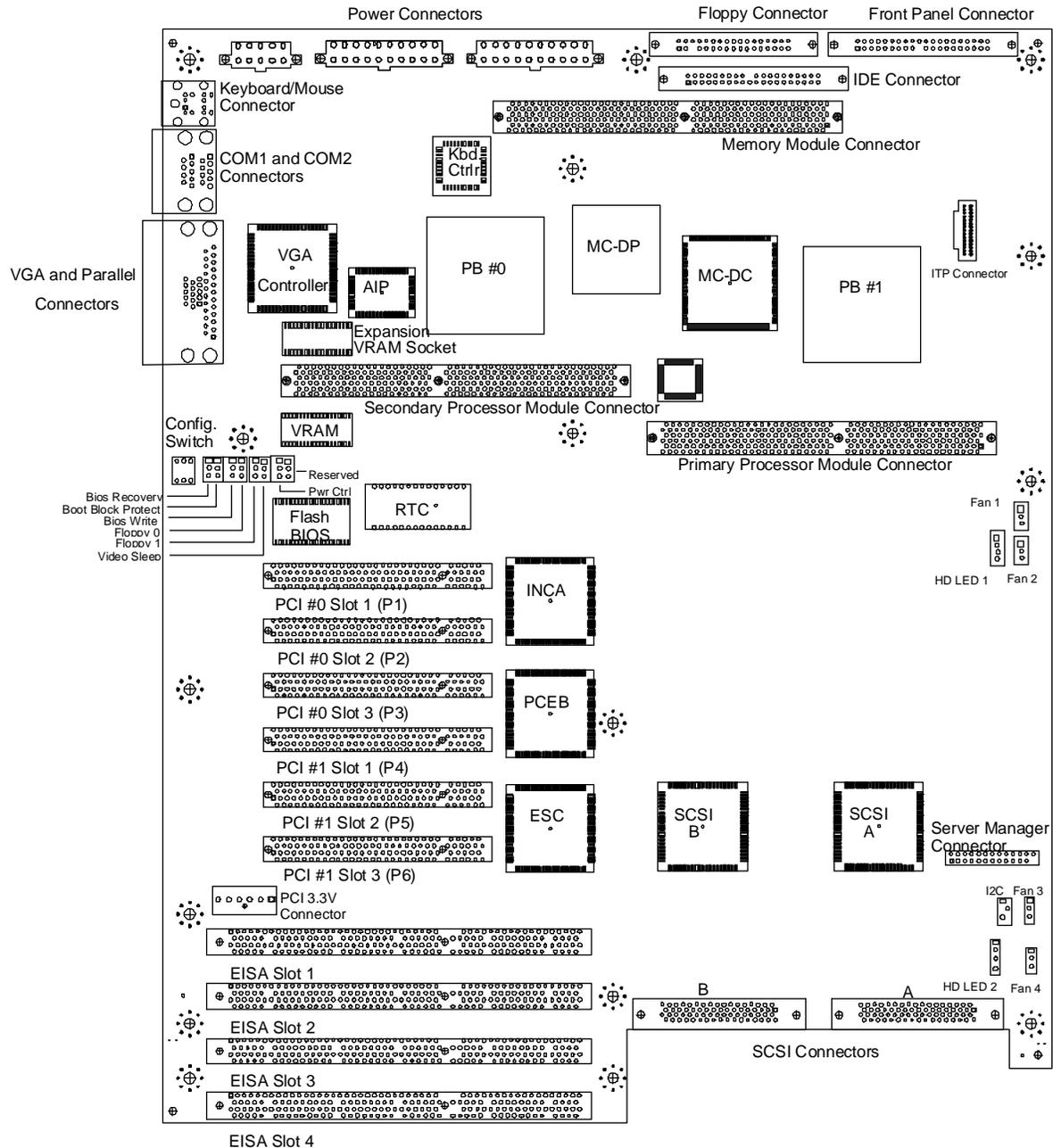
**Figure 1.2 Baseboard Layout**
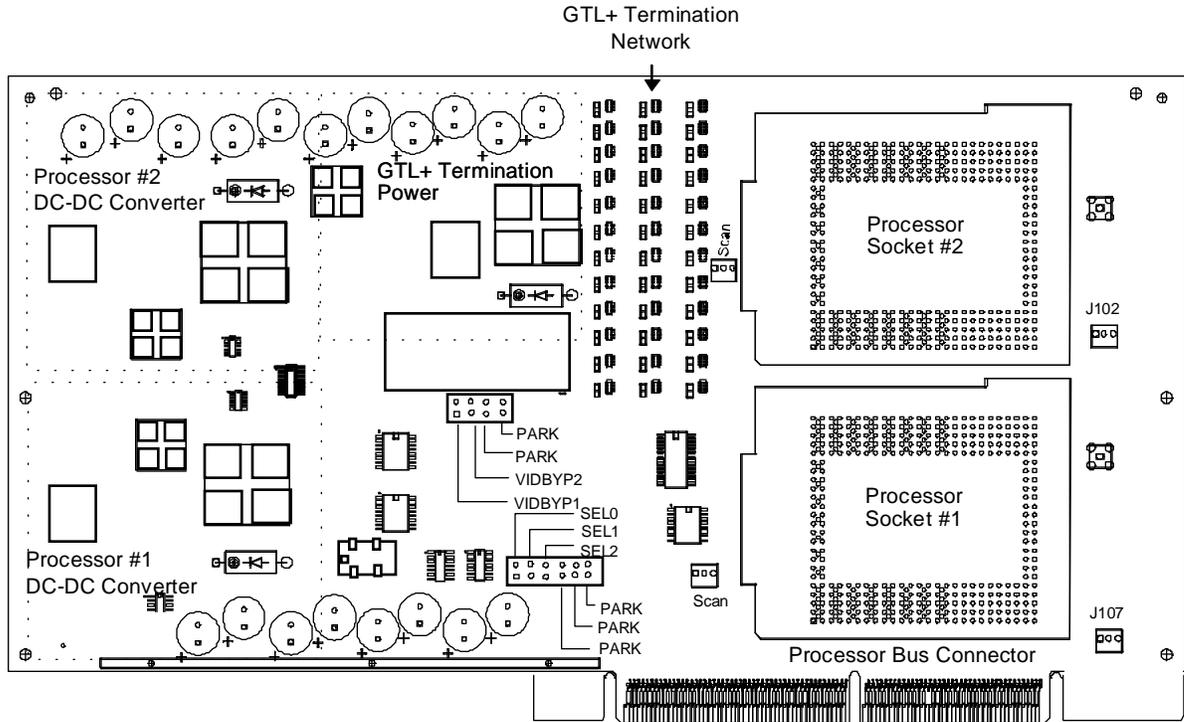
**Figure 1.3 Fab 3.x Processor Module Layout (supports 166MHz/512KB processors only)**
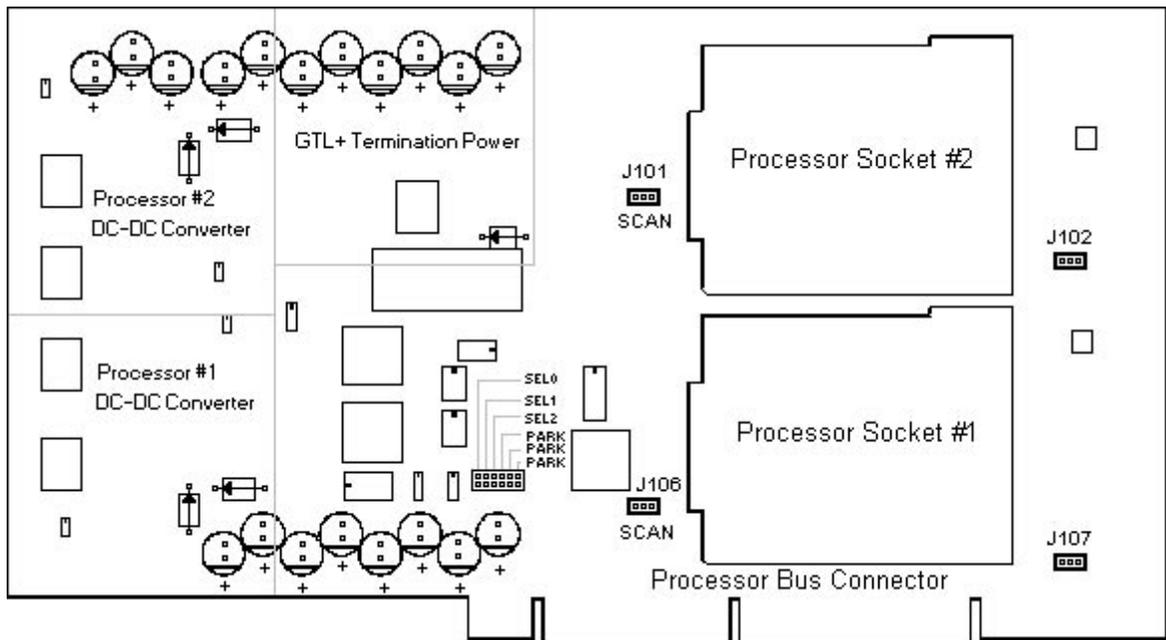


**Figure 1.4 Fab 4.x Processor Module Layout (supports both 166MHz/512KB & 200MHz/512KB processors)**
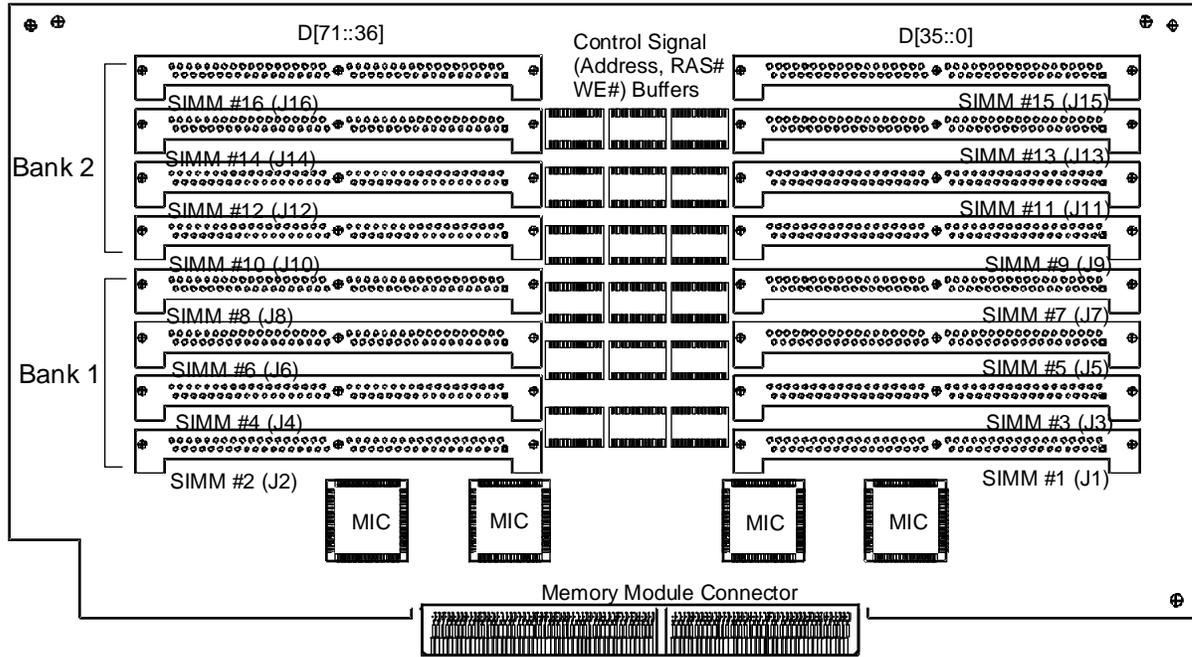
**Figure 1.5 1GB Memory Module Layout**

| | |
|---|---|
| Bank 0 Interleave 1 Row 0 J3 | Bank 0 Interleave 2 Row 0 J4 |
| Bank 0 Interleave 1 Row 1 J7 | Bank 0 Interleave 2 Row 1 J8 |
| Bank 1 Interleave 1 Row 2 J11 | Bank 1 Interleave 2 Row 2 J12 |
| Bank 1 Interleave 1 Row 3 J15 | Bank 1 Interleave 2 Row 3 J16 |
| Bank 2 Interleave 1 Row 4 J19 | Bank 2 Interleave 2 Row 4 J20 |
| Bank 2 Interleave 1 Row 5 J23 | Bank 2 Interleave 2 Row 5 J24 |
| Bank 3 Interleave 1 Row 6 J27 | Bank 3 Interleave 2 Row 6 J28 |
| Bank 3 Interleave 1 Row 7 J31 | Bank 3 Interleave 2 Row 7 J32 |
| Bank 0 Interleave 0 Row 0 J2 | Bank 0 Interleave 3 Row 0 J5 |
| Bank 0 Interleave 0 Row 1 J6 | Bank 0 Interleave 3 Row 1 J9 |
| Bank 1 Interleave 0 Row 2 J10 | Bank 1 Interleave 3 Row 2 J13 |
| Bank 1 Interleave 0 Row 3 J14 | Bank 1 Interleave 3 Row 3 J17 |
| Bank 2 Interleave 0 Row 4 J18 | Bank 2 Interleave 3 Row 4 J21 |
| Bank 2 Interleave 0 Row 5 J22 | Bank 2 Interleave 3 Row 5 J25 |
| Bank 3 Interleave 0 Row 6 J26 | Bank 3 Interleave 3 Row 6 J29 |
| Bank 3 Interleave 0 Row 7 J30 | Bank 3 Interleave 3 Row 7 J33 |

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**Figure 1.6 4GB Memory Module Layout**

## 1.5  Connector Locations

Baseboard connector locations are shown in the figure below.  See Appendix C for the connector pinouts.
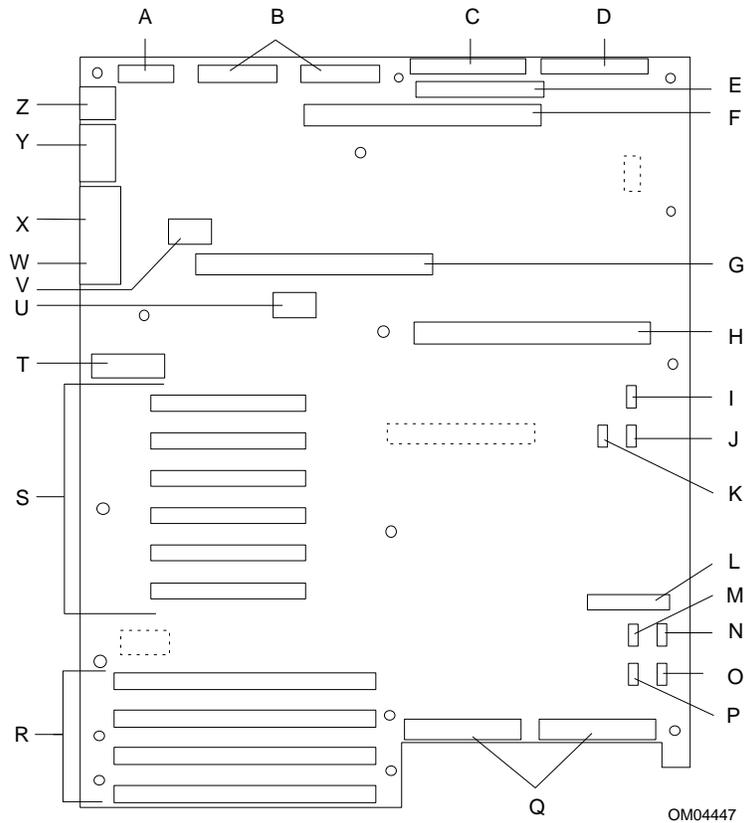


**Figure 1.7 AP450GX Board Set Connectors**

*\*\*        Comments in italics are applicable when the board set is installed into Intel's  AP450GX chassis.*

A        Power control and status connector (PS3)

B        +5V, +12V, and 3.3V power connectors (PS1 and PS2) (identical)

C        Diskette drive connector

D        Front panel connector

E        IDE drive connector

F        Memory module connector

G        Secondary processor module (or termination module) connector

H        Primary processor module connector

I        Fan 1 connector (*not used*, *fan sense jumper should be installed)*

J        Fan 2 connector *(inner chassis fan)*

K        Hard drive LED 1 connector (*not used*)

L        Connector for optional Server Management Module (SMM)

M        I$^2$C connector (*not used*)

| N | Fan 3 connector (*upper outer chassis fan*) |
|---|---|
| O | Fan 4 connector (*lower outer chassis fan*) |
| P | Hard drive LED 2 connector (*not used*) |
| Q | SCSI bus connectors:  Channel A to the right, Channel B to the left |
| R | EISA slots 1 - 4 for add-in boards (slot 1 toward top, 4 toward bottom) |
| S | PCI slots 1 - 6 for add-in boards (slot 1 toward top, 6 toward bottom: PCI Bus 0 = slots 1 - 3; PCI Bus 1 = slots 4 - 6) |
| T | Configuration switches and jumpers |
| U | Real-time clock |
| V | Video DRAM expansion socket |
| W | VGA monitor connector (bottom) |
| X | Parallel port connector (top) |
| Y | Serial port connectors -- Port 1 (top), Port 2 (bottom) |
| Z | PS/2-compatible keyboard and mouse connectors (interchangeable) |

Three connectors are shown in the board drawing as dotted-line boxes.  They are not used in this system configuration.  Their functions are as follows:

- ITP (In-target Probe) :  Located near the upper right corner of the baseboard for low level system debug.

- PCI test connector:  Blue connector near middle of board (not used)

- 3.3V PCI power connector:    Located near the lower left corner,  below the PCI slots.

## 1.6  Microprocessor

The Pentium Pro processor utilizes a 387-pin dual-cavity PGA package.  The package contains two devices:  a 5.5 million transistor processing core with 8 KByte primary cache, and 32 million transistor 512 KB secondary cache (L2 cache).

The AP450GX Board Set operates with Pentium Pro processors whose voltage may range from 2.1V to 3.5V and are Voltage ID (VID) enabled (i.e. the processors have the ability to ask for a certain voltage). A voltage regulator circuit on the processor module makes use of the VID capabilities to automatically adjust its voltage output to match that of the installed processor.  The board set also has jumpers allowing processors ranging from 133 to 266 MHz to be installed.  It should be noted, however, that there will be limitations on which processors will be supported.

The following table indicates which steppings of the Pentium Pro processor can be mixed within the same system. An "X" denotes which steppings can be mixed and a blank indicates the AP450GX MP Server Board Set does not support the given stepping combination.

**Table 1.1  Supported Processor Combinations**

| Stepping (Proc/Cache) | sA1/α | sA1/β | sA1/β | sB1/β | sB1/β |
|---|---|---|---|---|---|
| Frequency | 166 | 166 | 200 | 166 | 200 |
| Cache Size | 512 | 512 | 512 | 512 | 512 |
| Stepping ID | 0617 | 0617 | 0617 | 0619 | 0619 |
| QDF # | SY034 | SY047 | SY048 | SL22X | SL22Z |
| SY034 | X | X | | X | |
| SY047 | X | X | | X | |
| SY048 | | | X | | X |
| SL22X | X | X | | X | |
| SL22Z | | | X | | X |

**NOTES:**

1. The BIOS used must support each stepping installed in the system.

2. If the sB1 stepping of the Pentium® Pro processor is installed, BIOS revision 1.00.08.CD0 or later is required.

3. Refer to erratum 34 in the Pentium Pro Processor Specification Update for issues related to the sB1 stepping of the Pentium Pro processor.

4. Though Intel recommends using identical steppings of processor silicon in multiprocessor systems whenever possible (as this is the only configuration which receives full validation across all of Intel's testing), Intel supports mixing processor steppings, and does not actively prevent various steppings of the Pentium Pro processor from working together in multiple processor (MP) systems. However, since Intel cannot validate every possible combination of devices, each new stepping of a device is fully validated only against the latest steppings of other processors and chipset components. Refer to Specification Change 1 of the *Pentium Pro Processor Specification Update* for further details on issues related to mixed processor steppings in an MP system.

An approved Pentium Pro processor heatsink (Intel part #644591-002) is necessary for proper thermal dissipation.  The processor/heatsink assembly must be securely fastened to the socket by two clips (Intel part #637885-002).  These clips fit over the heatsink assembly and attach to the outer wide tabs of the socket assembly. The heat sink must use thermal grease for proper heat dissipation for any processor greater than 35W (i.e. the 200MHz/512KB).  "Foil pads" with grease on them will not properly cool a >35W processor.  A heat sink kit is available that contains the proper heatsink, two clips and thermal grease.  The current Intel order code is ALHSINKKIT.

The Pentium Pro processor maintains full backward compatibility with the 8086, 80286, Intel386™, Intel486™ and Pentium® processors.  It  also has a numeric coprocessor that significantly increases the speed of floating point operations, while maintaining backward compatibility with the i486DX math coprocessor and complying with ANSI/IEEE standard 754-1985.

⚠  CAUTION

*Do not use the older style of bail-wire clips for securing the heatsink assembly.  These clips have been found to cause damage when installed or removed incorrectly.*

### 1.6.1    Processors and Processor Modules

The processor module will support up to two Pentium® Pro processors.  The two processor sites are ZIF socketed, so that only one might be installed at the time of shipment with upgrades to be added later.  Each processor module contains termination circuitry required by the GTL+ signaling environment, DC to DC converters for proper power to each processor, an $I^2C$ controller, and logic for $I^2C$ support and clock ratio programming.  Each processor module has three DC-DC converters: one for the 1.5V GTL+ termination voltage, and two identical converters for the processors.  The processor converters are supplied from the +12V supply.  The GTL+ converter is supplied from the +12V supply on Fab 3.x processor modules (identified as 647428-xxx), or from the 3.3V supply on Fab 4.x processor modules (identified as 659506-xxx).  The Fab 4.x processor modules will support up to a 40W processor (i.e. the 200MHz/512KB).  The Fab 3.x processor modules will only supply enough current for up to a 35W processor (i.e. the 166MHz/512KB).

## 1.7  Bus Termination Module

This module is required when only one processor module is installed in the system.  The terminator module provides GTL+ signal termination and voltage regulation.  When used, this module must be installed in the secondary processor module slot on the system.  The terminator module contains a single DC-DC converter which provides the 1.5V termination voltage.  This converter is driven from the +12V supply.

## 1.8  Processor Population Order

The system baseboard has a primary processor module connector and a secondary processor module connector.  A processor module can have one or two Pentium Pro processors installed. The figures that follow show the different supported population orders for 1, 2, 3 or 4 processors. Other processor configurations are not supported.

**Processor board connectors on system baseboard**

A    System baseboard

B    Connector for secondary processor module or bus termination module

C    Connector for primary processor module

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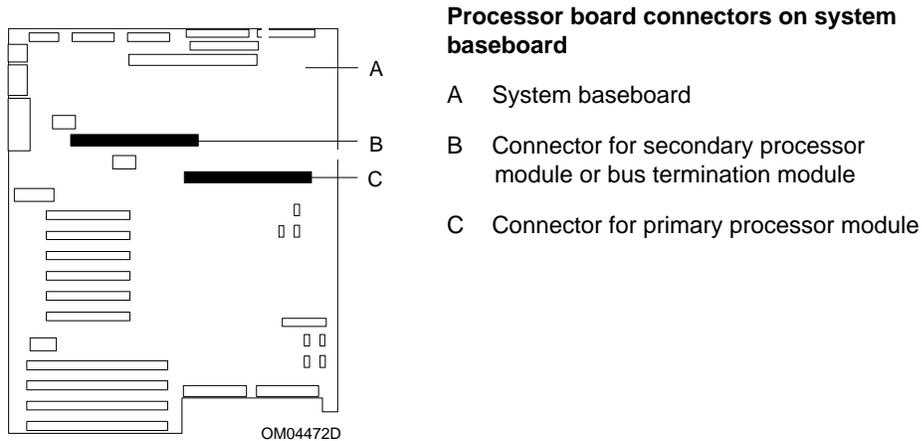
**Figure 1.8 Processor Module Connector Locations**
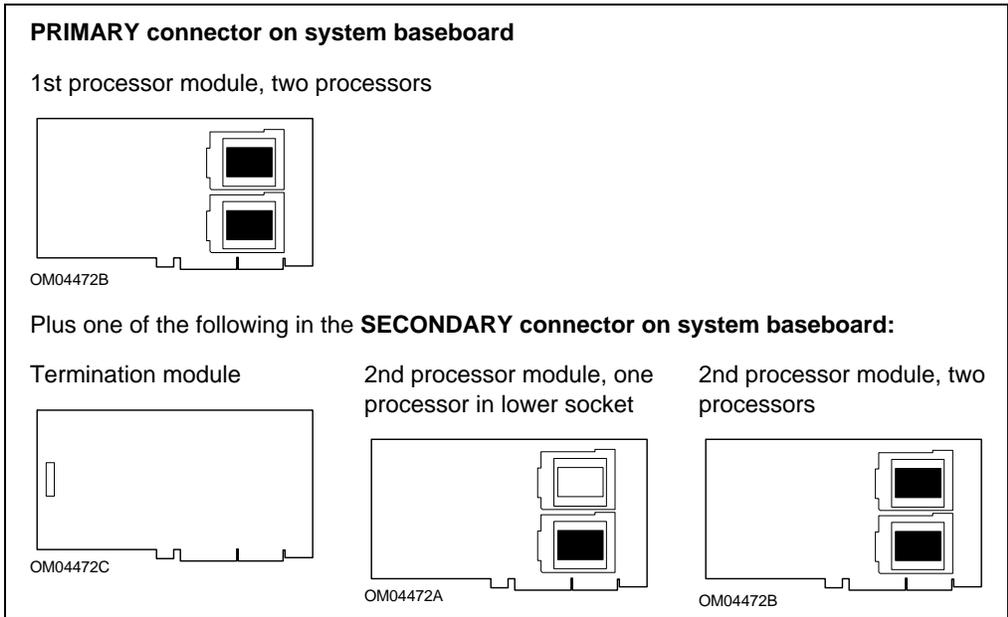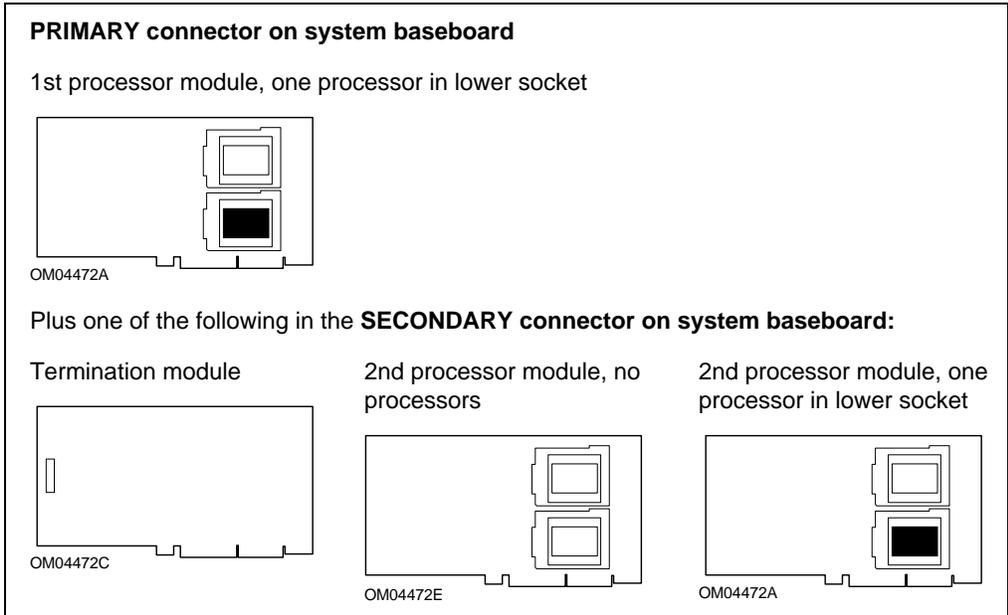
**Figure 1.9 Processor Configuration Models**

Refer to section 1.21 for the processor module jumper configurations.

## 1.9  Memory

### 1.9.1   System Memory

The memory subsystem consists of the memory chip set, the memory module connector on the system baseboard, and the memory module itself.  The system baseboard contains the data path and data control portions of the chip set.  The memory module contains the buffer devices from the chip set and 16 SIMM sites for up to 1 GB of system memory (using 64MB SIMMs) and 2 GB of system memory (using 128MB SIMMs).  DRAM SIMMs on the module are organized as two 72-bit wide, 2-, or 4-way interleaves and 1 or 2 banks.  SIMM sites accept 72-pin single- or double-sided SIMMs (60 or 70ns SIMMs only).  All SIMMs in a bank must be identical (same size and speed).

Memory error checking and correction is supported via ECC logic in the chip set while using standard parity SIMM/DIMMs. The chip set will detect double bit errors and correct single bit errors.  Errors may be generated by a defective memory module or soft errors.  When a bad SIMM/DIMM is detected (i.e. a double bit error), during booting the BIOS will automatically downsize memory to eliminate the bad SIMM/DIMM location.

The 1GB memory module is available in two versions.  Both are functionally identical except for the type of metal used in the SIMM connector and the type of capacitors used.  One version has tin lead SIMM connectors and must be used with tin lead SIMMs.  The other version is available with gold lead SIMM connectors and must be used with gold lead SIMMs.  The gold lead module also has fused tantalum capacitors.  The tin lead version simply has non-fused tantalum capacitors. There are separate order codes for each version.  See Appendix B for the specific order codes.

⟹ **NOTE**

*Only use SIMMs approved for use in this system.  Contact your Intel representative for an updated list of qualified SIMMs and DIMMs.*

## 1.9.2 Memory Installation Options (1GB Memory Module)

The following SIMM interleaving options are supported:

- Two-way interleave, J1 through J4;

- Four-way interleave, single bank, J1 through J8

- Four-way interleave, dual bank, J1 through J16.
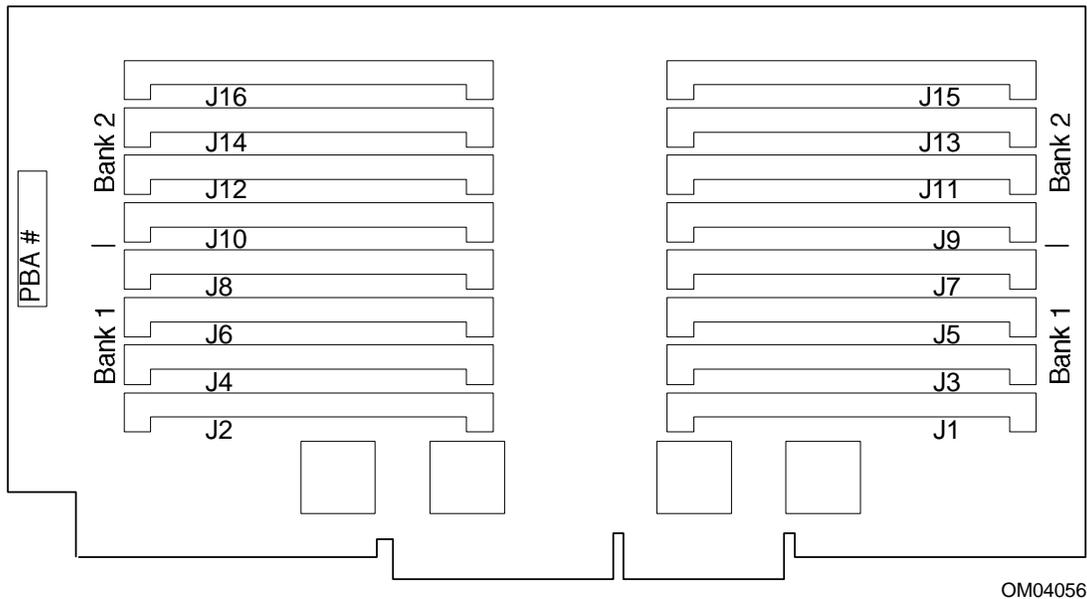


**Figure 1.10 Memory Configurations**

The 1GB memory module has 16 SIMM sockets, arranged in two banks. The system automatically detects system memory installed, so jumpers do not need to be set to specify memory size although the SCU must be run after you change the memory configuration. See Chapter 3 for details.

**Table 1.2  Supported Memory Options**

| Memory Size | Bank Installation | SIMM Type |
|---|---|---|
| Minimum memory configuration is 64 MB of DRAM (with four 16 MB SIMMs installed in J1, J2, J3, and J4).<br><br>Maximum memory configuration is 1GB of DRAM (with 64 MB SIMMs installed in each socket, J1 through J16). Maximum memory configuration is 2GB with 128MB SIMMs. | Always begin with the bottom SIMM sites (lowest number is J1) as you fill the board sockets.<br><br>All SIMMs in a bank must be identical (same size and speed).<br><br>SIMMs in bank 1 may differ in size from the SIMMs in bank 2, but may not differ in speed.<br><br>Number of SIMMs supported: 4, 8, or 16 only. | Use 16 MB, 64MB or 128 MB single-sided SIMMs or 32 MB double-sided SIMMs.<br><br>Use only 36-bit, 72-pin, 60 or 70ns fast page mode SIMMs, single- or double-sided.  (Single-sided refers to the addressing method, not to the physical layout of the SIMM.)<br><br>Use the 1 GB memory module with tin lead SIMM connectors when using  tin lead SIMMs.  Use the 1 GB memory module with gold lead SIMM connectors when using gold lead SIMMs.<br><br>Use JEDEC-compatible SIMMs.  Contact your Intel representative for a list of approved SIMMs. |

## 1.9.3   Memory Performance Hints

Memory performance, and thus system performance, can be increased by changing the number of interleaves, number of banks and the speed of memory installed.  For more information about system performance, refer to the *AP450GX MP Server System Performance Brief*.

## 1.9.4   4GB Memory Module

An optional 4GB memory module is available and will support up to 4GB of memory using 128MB DIMMs.  This module fits into the same memory module connector the 1GB module fits into and has the same mechanical form factor.  The additional memory capacity is accomplished with the use of TOSP DRAM's packaged in JEDEC standard 16Mx72 60ns DIMMs only.  Note these are 3.3V DIMMs, while the 1GB module uses 5V SIMMs.  The DIMMs are also installed at a 90° angle to the memory module (vs. 45° for the 1GB memory module) and are 1.25" high.  The 4GB module contains 32 DIMM sockets, which when populated in groups of 4 DIMMs, offers memory capacity options of 0.5GB through 4GB in 0.5GB increments. Memory on the module is organized in 8 banks and 4-way interleaves.

## 1.9.4.1   DIMM Requirements

The 4GB memory module will only support a 128MB DIMM which meet JEDEC Standard No. 21-C, Release 4.  In addition the DIMM must utilize TSOP DRAMs and must not exceed 0.157" in width.  Two JDEC standard options with identical mechanical pinouts are listed below.

1.        16Mx72 Fast Page Mode DRAM DIMM with ECC, 8K refresh, 3.3 V, 16Mx4 DRAM based, 13 row addresses, 11 column addresses internally.

2.        16Mx72 Fast Page Mode DRAM DIMM with ECC, 4K refresh, 3.3 V, 8Mx8/9 DRAM based, 12 row addresses, 11 column addresses internally.

⇒ **NOTE**

*Only use DIMMs approved for use in this system.  Contact your Intel representative for an updated list of qualified SIMMs and DIMMs.*

### 1.9.4.2    Memory Installation Options (4GB Memory Module)

For the 4GB memory module the following DIMM population procedure must be used.  The DIMMs are to be populated from J2 through J33 consecutively in groups of 4.  All configurations result in a four-way memory interleave.  Refer to Figure 1.6.

**Table 1.3  Supported 4GB Memory Module Options**

| Memory Capacity | DIMM population instructions |
|---|---|
| 0.5 GB | populate J2, J3, J4, J5 |
| 1.0 GB | add J6, J7, J8, J9 |
| 1.5 GB | add J10, J11, J12, J13 |
| 2.0 GB | add J14, J15, J16, J17 |
| 2.5 GB | add J18, J19, J20, J21 |
| 3.0 GB | add J22, J23, J24, J25 |
| 3.5 GB | add J26, J27, J28, J29 |
| 4.0 GB | add J30, J31, J32, J33 |

### 1.9.5    Memory Configuration Options

Error correction and detection, memory downsizing and address bit permuting are capabilities supported by both the 1GB and 4GB memory modules.  Some options work slightly differently depending on the module and are described in the following sections.

### 1.9.5.1    Error Detection and Correction

The memory controller of the Intel 450GX PCIset performs run-time correction of single bit errors and detects double bit errors.  Because a double bit error is not correctable, system operation once a double bit error has been detected is unpredictable and dependent on the operating system's ability to recover from it.  Both single and double bit errors are recorded in the system error log if error reporting is enabled.

### 1.9.5.2    Memory Downsizing

During POST the BIOS performs a check of memory to insure all SIMMs/DIMMs are fully functional.  Should a bad memory location be detected during POST, the BIOS will resize memory to eliminate the bad memory location.  Unlike some memory resizing algorithms which will eliminate an entire SIMM/DIMM module from the system if a bad memory location is detected, the memory resizing algorithm used in the AP450GX system maintains the current memory configuration (i.e. same number of SIMM/DIMMs, same number of banks, same number of interleaves) and eliminates only the bad memory location.  This is done by reducing the amount of memory used by each SIMM/DIMM until the bad memory location is no longer allocated.

When an error is detected, the BIOS first determines which bank is affected by the error.  The memory allocation for the affected bank is then decreased by a power of two (i.e. only half the memory of each SIMM/DIMM will be allocated).  The BIOS will continue decreasing the affected banks memory size by a power of two until the bad memory location is no longer allocated. A BIOS error will also be displayed indicating memory has been resized.  If memory for the affected bank is decreased to 4MB and the bad memory location cannot be eliminated, the BIOS will display an error message and will not boot.

The above algorithm is identical for both the 1GB and 4GB memory modules.

**⇒ NOTE**

*If double-sided (also called double-banked) SIMMs are used on the 1GB Memory Module, ECC memory errors may be reported on banks 1-4, even though the Memory Module only contains two physical memory banks.  In this case, ECC errors on bank #1 would indicate a bad SIMM location in sockets J1-J8 and the error is on the front side of the SIMM.  ECC errors on bank #2 would indicate a bad SIMM location in sockets J1-J8 and the error is on the back side of the SIMM.  ECC errors on bank #3 would indicate a bad SIMM location in sockets J9-J16 and the error is on the front side of the SIMM.  ECC errors on bank #4 would indicate a bad SIMM location in sockets J9-J16 and the error is on the back side of the SIMM.*

## 1.9.5.3   Address Bit Permuting

The 450GX PCIset has a performance enhancing feature called Address Bit Permuting (ABP).  ABP, if enabled, swaps memory row selection bits with the lower order bits in the address.  In some applications this can improve system performance by increasing the number of row misses and thus decreasing the number of precharge penalties.  ABP can be enabled under certain memory configurations.  These configurations are listed below for each memory module.  The ABP option in the BIOS setup (Advanced Chip Set Menu) must also be enabled.

**1GB Memory Module**

ABP can be enabled by the BIOS if all of the following are true:

- ABP BIOS option set to enabled

- Same speed SIMMs in both banks

- Same sized SIMMs in both banks

*Note:  The ABP bit in the $I^2C$ register is used to allow ABP with single sided SIMMs and will only be set if all of the above are true and the SIMMs installed in the system are single-sided.  ABP will still be enabled if all of the above are true and double sided SIMMs are installed, but the $I^2C$ register bit will not be set.*

**4GB Memory Module**

ABP can be enabled by the BIOS if all of the following are true:

- ABP BIOS option set to enabled

- Same speed DIMMs in all banks

- The module is populated in a two (1GB), four (2GB) or eight (4GB) bank configuration.

*Note:  ABP will not be enable if populated in a one, three, five, six or seven bank configuration.*

## 1.10  Intel 450GX PCIset

The Intel 450GX PCIset (B0 stepping & C0 stepping) consists of two functional groups, the PCI controller and the memory controller.  The PCI controller consists of a single 82454GX PCI Bridge (PB) component, which supports PCI Bus mastering.  Two of 82454GX components are on the system baseboard, each supporting a single PCI (peer) bus.  The memory controller consists of six components; the 82452GX (DP) Data Path component, 82453GX (DC) Data path Controller, and the 82451GX (MIC) Memory Interface Controller.  The DP and DC each reside on the system baseboard.  Four of the MIC components are located on the memory module.

## 1.11  Onboard SCSI Controllers

The baseboard includes two embedded wide SCSI-2 controllers (Adaptec AIC-7880, channels A and B) integrated as PCI bus masters.  The controllers support data path widths of 8-bit (narrow SCSI) at a data transfer rate of 10 MB/sec, 16-bit (wide fast SCSI) at a data transfer rate of 20 MB/sec and 16-bit (Fast-20/Ultra) at a data trasfer rate of 40MB/sec.  As PCI bus masters, these controllers support data transfer rates of 133 MB/sec.

You can connect up to seven 8-bit narrow SCSI devices or up to fifteen 8-bit narrow and/or 16-bit wide SCSI devices and one controller (maximum of seven 8-bit narrow devices) to each channel. Devices can be tape drives, printers, optical media drives, and other devices.  Narrow SCSI devices are not supported in Fast-20/Ultra mode.

Active termination must be provided on the far end of the SCSI bus to ensure proper termination of the bus.  The baseboard provides active termination at the near end.

Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus and avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48 mA, single-ended SCSI bus with no additional drivers.

## 1.12  EISA Expansion Slots

The baseboard has four EISA bus slots.  The EISA bus is an extension of the Industry Standard Architecture (ISA) bus. Because EISA is fully backward-compatible with ISA, you can install EISA or ISA add-in boards and software in your server.  This compatibility is handled by the PCEB and ESC chip set components on the system baseboard.

The EISA bus provides:
- 32-bit memory addressing
- Type A transfers at 5.33 MB per second
- Type B transfers at 8 MB per second
- Burst transfers at 33 MB per second

- 8-, 16-, or 32-bit data transfers
- Automatic translation of bus cycles between EISA and ISA masters
- Interrupt sharing

All four slots have the capability of being bus masters.  When EISA masters arbitrate for the bus, the following pairs of slots share arbitration requests:  1 and 2, 3 and 4.  Therefore, in the round-robin scheme of letting EISA masters take over the bus, ownership of it occurs in the following sequence:  1, 2, 3, 4, 1, 2, 3, 4, etc.

## 1.13  PCI Expansion Slots

The system baseboard has six, 32 bit, PCI 2.0 compliant bus slots.  The PCI subsystem consists of two I/O bus segments.  PCI #0 is the primary or compatibility bus segment, running always at 33 MHz.  PCI #0 connects the processor bus to the INCA (Intel's Interrupt Controller ASIC), a PCI/EISA bridge, and three PCI connectors.  PCI #1 connects the processor bus to two embedded wide SCSI controllers and three PCI connectors.  PCI #1 also always runs at 33MHz.  The architecture supports Host-to-PCI, PCI-to-Memory, PCI-to-EISA, EISA-to-Memory, and PCI-to-PCI transfers.  The PCI bus provides:

- 32 and 64-bit memory addressing
- +5 V and + 3 V signaling environments
- Burst transfers at 133 MB per second
- 8-, 16-, or 32-bit data transfers
- Plug-and-play configuration
- PeerBus to maximize throughput

The INCA device provides these features:

- PCI clock generation:  14 PCI clocks (7 per PCI segment)
- Three buffered clocks
- Interrupt control
- Arbitration support for six PCI masters on PCI #1
- General purpose I/O ports:  two 8-bit I/O ports for control or status
- 3-mode diskette control support
- DMA steering for IDE and parallel port to 1 of 4 DRQs/DACKs
- Keyboard emulation
- Support for front panel interface and LCD
- Security features:  watchdog timer (software start/reset) resets system if it expires; monitors keyboard/mouse; monitors system baseboard voltage (+12V, -12V, +5V, -5V, +3.3V); monitors baseboard temperature and chassis door switch

## 1.14  Boot Order

When the system boots, it will look for a bootable device in a certain order.  The system will then boot off the first bootable device it finds.  Below is the order in which the system will look for bootable devices.

1. Floppy Drive
2. IDE Drive
3. E1            (EISA bus slot #1)
4. E2            (EISA bus slot #2)

| | | |
|---|---|---|
| 5. | E3 | (EISA bus slot #3) |
| 6. | E4 | (EISA bus slot #4) |
| 7. | P1 | (PCI Bus#0, slot 1) |
| 8. | P2 | (PCI Bus#0, slot 2) |
| 9. | P3 | (PCI Bus#0, slot 3) |
| 10. | P4 | (PCI Bus#1, slot 1) |
| 11. | SCSI A | (On-board AIC-7880 SCSI controller) |
| 12. | SCSI B | (On-board AIC-7880 SCSI controller) |
| 13. | P5 | (PCI Bus#1, slot 2) |
| 14. | P6 | (PCI Bus#1, slot 3) |

**Notes:**

- The actual boot order on the EISA bus may change depending on how the devices installed on the EISA bus are configured, but the EISA bus will always be scanned for bootable devices before the PCI buses.

- If a PCI-to-PCI bridge device (P2P) is installed in the system, the boot order will change and may vary depending on the configuration. Typically, if a P2P is installed in P2, for example, the boot order will likely look for a bootable device on the P2P before looking at P3. However under some circumstance, the system may actually go to P3 before looking for a bootable device on the P2P.

## 1.15 Super VGA Controller

The onboard, integrated Cirrus Logic CL-GD5424 super VGA controller (ISA based) is fully compatible with these video standards: CGA, EGA, Hercules Graphics, MDA, and VGA. The standard system configuration comes with 512 KB of onboard 70ns video memory. You can optionally expand the onboard video memory buffer size to 1 MB by adding one 40-pin 256 K x 16, 70 ns fast-page DRAM. Contact your Intel representative for an updated list of qualified video memory. The SVGA controller supports only analog monitors (single and multiple frequency, interlaced and noninterlaced) with a maximum vertical retrace interlaced frequency of 87 Hz.

The BIOS will automatically disable the onboard video if another add-in video adapter is installed into the system baseboard. Note, however, the BIOS will only support add-in video adapters in the first PCI bus (slots P1-P3). Video adapters placed in the second PCI bus (slots P4-P6 will not be recognized).

- Supported with 512 KB memory: Pixel resolutions of 640 x 480 x 256 colors, and 800 x 600 and 1024 x 768 in 16 colors.

- Supported with 1 MB memory (optional): 132-column text modes and high resolution graphics with 1280 x 1024 x 16 colors. Depending on the environment, the controller displays up to 64,000 colors in some video resolutions.

**Table 1.4  Standard VGA Modes**

| Mode(s) in Hex | Colors (number /palette size) | Resolution | Pixel Freq. (MHz) | Horiz. Freq. (KHz) | Vert. Freq. (Hz) |
|---|---|---|---|---|---|
| 0, 1 | 16/256K | 360 X 400 | 14 | 31.5 | 70 |
| 2, 3 | 16/256K | 720 X 400 | 28 | 31.5 | 70 |
| 4, 5 | 4/256K | 320 X 200 | 12.5 | 31.5 | 70 |
| 6 | 2/256K | 640 X 200 | 25 | 31.5 | 70 |
| 7 | Mono | 720 X 400 | 28 | 31.5 | 70 |
| D | 16/256K | 320 X 200 | 12.5 | 31.5 | 70 |
| E | 16/256K | 640 X 200 | 25 | 31.5 | 70 |
| F | Mono | 640 X 350 | 25 | 31.5 | 70 |
| 10 | 16/256K | 640 X 350 | 25 | 31.5 | 70 |
| 11 | 2/256K | 640 X 480 | 25 | 31.5 | 60 |
| 12 | 16/256K | 640 X 480 | 25 | 31.5 | 60 |
| 12+ | 16/256K | 640 X 480 | 31.5 | 37.5 | 75 |
| 13 | 256/256K | 320 X 200 | 12.5 | 31.5 | 70 |

**Table 1.5  Extended VGA Modes**

| Mode(s) in Hex | Colors (number /palette size | Resolution | Pixel Freq. (MHz) | Horiz. Freq. (KHz) | Vert. Freq. (Hz) |
|---|---|---|---|---|---|
| 14, 55 | 16/256K | 1056 X 400 | 41.5 | 31.5 | 70 |
| 54 | 16/256K | 1056 X 350 | 41.5 | 31.5 | 70 |
| 58, 6A | 16/256K | 800 X 600 | 40 | 37.8 | 60 |
| 58, 6A | 16/256K | 800 X 600 | 49.5 | 46.9 | 75 |
| 5C* | 256/256K | 800 X 600 | 36 | 35.2 | 56 |
| 5C* | 256/256K | 800 X 600 | 40 | 37.9 | 60 |
| 5C* | 256/256K | 800 X 600 | 49.5 | 46.9 | 75 |
| 5D | 16/256K (interlaced) | 1024 X 768 | 44.9 | 35.5 | 87 |
| 5D | 16/256K | 1024 X 768 | 65 | 48.3 | 60 |
| 5D | 16/256K | 1024 X 768 | 75 | 56 | 70 |
| 5D | 16/256K | 1024 X 768 | 78.7 | 60 | 75 |
| 5F | 256/256K | 640 X 480 | 25 | 31.5 | 60 |
| 5F | 256/256K | 640 X 480 | 31.5 | 37.5 | 75 |
| 60* | 256/256K (interlaced) | 1024 X 768 | 44.9 | 35.5 | 87 |
| 60* | 256/256K | 1024 X 768 | 65 | 48.3 | 60 |
| 60* | 256/256K | 1024 X 768 | 75 | 56 | 70 |
| 60* | 256/256K | 1024 X 768 | 78.7 | 60 | 75 |
| 64* | 64K | 640 X 480 | 25 | 31.5 | 60 |
| 64* | 64K | 640 X 480 | 31.5 | 37.5 | 75 |
| 65* | 64K | 800 X 600 | 36 | 35.2 | 56 |
| 65* | 64K | 800 X 600 | 40 | 37.8 | 60 |
| 65* | 64K | 800 X 600 | 49.5 | 46.9 | 75 |
| 66* | 32K Direct/256 Mixed | 640 X 480 | 25 | 31.5 | 60 |
| 66* | 32K Direct/256 Mixed | 640 X 480 | 31.5 | 37.5 | 75 |
| 67* | 32K Direct/256 Mixed | 800 X 600 | 40 | 37.8 | 60 |
| 67* | 32K Direct/256 Mixed | 800 X 600 | 49.5 | 46.9 | 75 |
| 6C* | 16/256K (interlaced) | 1280 X 1024 | 75 | 48 | 87 |
| 6C* | 16/256K | 1280 X 1024 | 108 | 65 | 60 |
| 6D* | 256/256K (interlaced) | 1280 X 1024 | 75 | 48 | 87 |
| 6D* | 256/256K | 1280 X 1024 | 108 | 65 | 60 |
| 71* | 16M | 640 X 480 | 25 | 31.5 | 60 |
| 72* | 16M 32-bit/pixel | 800 X 600 | 40 | 37.8 | 60 |
| 73* | 16M 32-bit/pixel (interlaced) | 1024 X 768 | 44.9 | 35.5 | 87 |
| 74* | 64K (interlaced) | 1024 X 768 | 44.9 | 35.5 | 87 |
| 74* | 64K | 1024 X 768 | 65 | 48.3 | 60 |
| 74* | 64K | 1024 X 768 | 75 | 56 | 70 |
| 74* | 64K | 1024 X 768 | 78.7 | 60 | 75 |
| 75* | 64K (interlaced) | 1280 X 1024 | 75 | 48 | 87 |
| 76* | 16M 32-bit/pixel | 640 X 480 | 25 | 31.5 | 60 |
| 76* | 16M 32-bit/pixel | 640 X 480 | 31.5 | 37.5 | 75 |

* Requires 1MB video memory option.

## 1.16  Keyboard and Mouse

The 8742 keyboard controller is PS/2-compatible.  The system may be locked automatically if there is no keyboard or mouse activity for a predefined length of time, as specified through the Setup utility.  The default keystroke combination to enable this feature is <Ctrl + Alt + Backspace>.  Once the inactivity timer has expired, the keyboard or mouse does not respond until the previously stored password in the keyboard controller is entered.  The keyboard LED will blink until the password is entered.

The mouse is disabled on power-up; in this state, interrupt IRQ12 is available for use by add-in boards, and the mouse clock input to the keyboard controller is connected to the mouse clock output, with no connection to the external mouse.

## 1.17  Advanced Integrated Peripheral (AIP)

The AIP resides on the EISA bus and contains a floppy disk controller (FDC), 2 serial ports, a multi-function parallel port and an IDE interface.

### 1.17.1  Floppy Drive Support

The FDC on the AIP is functionally compatible with the 82077SL, 82077AA and 8272A floppy disk controllers and can provide a data rate up to 2MB/s.  The FDC will support up to two floppy disk drives.

### 1.17.2  Serial Ports

Two 9-pin serial ports are provide in a single stacked housing (ports 1 and 2).  Port 1 is located on the top, port 2 on the bottom.  Both serial ports are 16550 compatible with 16-byte FIFO's.  Each serial port can be set to 1 of 4 different COM ports (via the BIOS setup), and can be enabled separately.  When enabled, each port can be programmed to generate edge or level sensitive interrupts.  When disabled, serial port interrupts are available to adapter cards.

### 1.17.3  Parallel Port

A single PS/2 compatible 25-pin bi-directional parallel port is provided.  The parallel port supports Extended Capabilities Port (ECP) protocol with DMA, EPP protocol and IEEE 1284 protocol for PS/2 bi-directional compatibility.  The parallel port can be enabled or disabled via the BIOS setup.  When disabled, the interrupt is available to adapter cards.

### 1.17.4  IDE Support

IDE is an 8-bit or 16-bit interface for intelligent disk drives with AT disk controller electronics onboard.  AC timing constraints allow only Type 2 IDE drives in the CAM specification (or faster) to be supported.  The processor can transfer data from the IDE interface at a maximum transfer rate of 2.4Mbytes per second.  This IDE implementation will also support DMA to the IDE device, which has a maximum transfer rate of 4.2Mbytes per second.  Typical IDE devices can access data a peak rate of 1.2Mbytes per second.  Therefore, the usage of DMA will significantly reduce the bus utilization (with respect to IDE device access), and will significantly improve system performance.

The IDE interface can be disabled. It is disabled on reset; in this state, the I/O address space and interrupt IRQ14 are available for add-in modules. The system BIOS may disable the interface when it finds the registers of another hard disk controller.

## 1.18  Miscellaneous Functions

The board set provides the additional miscellaneous functions listed below:

- $I^2C$ Diagnostic Bus

- Server Management Connector

- System Fan Interface

- Hard Drive LED Interface

## 1.18.1  $I^2C$ Diagnostic Bus

The baseboard has an integral $I^2C$ (Inter-Integrated Circuit) bus which can be used for general purpose system management such as providing module revision or status information from anywhere in the system. This bus is routed to processor and memory modules, the front panel and power supply connectors, the Server Management Connector and a single user connector on the baseboard.

A Philips PCF8584 $I^2C$ controller is mapped into EISA I/O space and can be used by system software to access the $I^2C$ bus. The 8584 appears at addresses CA0h and CA1h. The interrupt from the 8584 is routed to input PCI8 on the INCA component.

The baseboard, processor, memory and terminator modules have PCF8574 and PCF8474A I/O devices on them. These are 8-bit devices that connect the $I^2C$ bus and provide system information from each module. Below is the $I^2C$ base address for each component.

| Component | $I^2C$ Base Address |
|---|---|
| Baseboard | 0x40 |
| Primary Processor Module Slot | 0x70 |
| Secondary Processor Module Slot | 0x72 |
| Primary Processor Module Slot, Reserved | 0x90 |
| Secondary Processor Module Slot, Reserved | 0x92 |
| Memory Module | 0x42 |

The information available from each module when accessed via the $I^2C$ bus is shown in the following table along with the bit definitions.

**Table 1.6  Baseboard I$^2$C Bit Map**

| Bit | Bit Name | Description |
|---|---|---|
| 2:0 | BRDREV(2:0) | Baseboard board revision ID |
|  |  | 001 = Fab 1 |
|  |  | 010 = Fab 2 |
|  |  | 011 = Fab 3 |
| 6:3 | RESERVED | Reserved |
| 6:3 | FANFAIL(3:0) | A zero (0) indicates a failed fan. Bits 6:3 are valid as FANFAIL when bit 7 = "1". |
|  |  | bit 3 = fan 4  (Outer chassis fan, lower) |
|  |  | bit 4 = fan 3  (Outer chassis fan, upper) |
|  |  | bit 5 = fan 2  (Inner chassis fan) |
|  |  | bit 6 = fan 1  (Not used in AP450GX MP Server chassis) |
|  |  | (not a supported feature) |
| 7 | FANFAILSEL | When "1", bits 6:3 are fan fail |
|  |  | When "0", bits 6:3 are Reserved |
|  |  | (not a supported feature) |

**Table 1.7  Processor Module I$^2$C Bit Map**

| Bit | Bit Name | Description |
|---|---|---|
| 2:0 | P6ID(2:0) | Pentium® Pro processor core/bus frequency ID |
|  |  | 000 = 150/60 MHz |
|  |  | 001 = 180/60 MHz |
|  |  | 010 = 210/60 MHz |
|  |  | 011 = 240/60 MHz |
|  |  | 100 = 166/66 MHz |
|  |  | 101 = 200/66 MHz |
|  |  | 110 = 233/66 MHz |
|  |  | 111 = 266/66 MHz |
| 4:3 | Reserved |  |
| 5:3 | BRDREV(0:2) | Processor Module Board Revision ID |
|  |  | 000 = Fab 3 |
|  |  | 001 = Fab 4 |
|  |  | 100 = Fab 3 modified for the sB1 processor |
|  |  | 101 = Fab 4 modified for the sB1 processor |
|  |  | Bits 5:3 are valid as BRDREV when bit 7 = "1". |
|  |  | All previous processor module revisions are not compatible with Fab 3 which is why the numbering starts with 000. |
| 6:5 | Reserved |  |
| 7 | BRDREVSEL | When "1", bits 5:3 indicate the board revision, bit 6 is reserved |
|  |  | When "0", bit 6:3 are reserved. |

**Table 1.8  1GB Memory Module I²C Bit Map**

| Bit | Bit Name | Description |
|-----|----------|-------------|
| 1:0 | | Board Revision ID |
| | | 00 = 1GB Module (Fab1 or Fab2) |
| | | 01 = 1GB Module (Fab3) |
| | | 10 = 4GB Module |
| | | 11 = Reserved |
| 3:2 | | Bank 0 SIMM Speed |
| | | 00 = 50ns (bank 0) |
| | | 01 = 80ns (bank 0) |
| | | 10 = 70ns (bank 0) |
| | | 11 = 60ns (bank 0) |
| 5:4 | | Bank 1 SIMM Speed |
| | | 00 = 50ns (bank 1) |
| | | 01 = 80ns (bank 1) |
| | | 10 = 70ns (bank 1) |
| | | 11 = 60ns (bank 1) |
| 6 | | Reserved |
| 7 | | RAS/CAS Multiplexing for Address Bit permuting |
| | | 0 = Enabled |
| | | 1 = Disabled |

**Table 1.9  4GB Memory Module I²C Bit Map**

| Bit | Bit Name | Description |
|-----|----------|-------------|
| 1:0 | BRDREV(1:0) | Board Revision ID |
| | | 00 = 1GB Module (Fab1 or Fab2) |
| | | 01 = 1GB Module (Fab3) |
| | | 10 = 4GB Module |
| | | 11 = Reserved |
| 5:2 | REFRESH(3:0) | Refresh |
| | | 1110 = 8Mx8/9 DRAM based 4K refresh |
| | | 1111 = 16Mx4 DRAM based 8K refresh |
| | | All others are reserved. |
| 7:6 | DIMMSPD(1:0) | DIMM Speed (All Banks) |
| | | 00 = 50ns |
| | | 01 = 80ns |
| | | 10 = 70ns |
| | | 11 = 60ns |

**Table 1.10  Termination Module I$^2$C Bit Map**

| Bit | Bit Name | Description |
| --- | --- | --- |
| 2:0 | BRDREV(2:0) | AP450GX Terminator Module revision ID |
| | | 000 = Fab 3 |
| | | All previous terminator module revisions are not compatible with Fab 3 which is why the numbering starts with 000. |
| 6:3 | N/C | These signals are not used. |
| 7 | GROUND | Hard wired to ground. |
| | | To differentiate between a terminator module and a processor module, write a one "1" to bit 7 then do a read of bit 7.  If a one "1" is read back, the board is a processor module.  If a zero "0" is read back, the board is a terminator module. |

### 1.18.2 Server Management Connector

A 26-pin connector is provided to interface with an emergency management adapter card.  It is designed for Intel's Server Monitor Module which allows the user to manage (monitor and control) the server from a remote console, but could be used by other similar implementations.  The connector provides access to the I$^2$C bus, power on/off signals, power good from the power supply and a host of other signals.  Refer to the connector pin-out in Appendix C for a list of all signals.

### 1.18.3 System Fan Interface

There are four fan connectors on the system baseboard.  The connector pin-out is listed in Appendix C.  These connectors provide a ground, 12V power to the fan and a fan-fail input from the fan.  The system will be able to detect the failure and will report it via Intel's LANDesk® Server Control Software.  These fan failures are also logged in the BIOS event log, and are denoted by the fan fail light on the system front panel.  All four fan-fail inputs are tied to A/D channel 8 for monitoring by the INCA component.  The current LANDesk software does have the ability to distinguish between the four fans.  It simply knows if one fan has failed.  If one or more of the fan connectors is not used in a particular application, pins 1 (GND) and 3 (Fan Fail) on the connector must be connected together.  This connection is required to prevent an erroneous failed fan indication.

### 1.18.4 Hard Drive LED Interface

There are two Hard Drive LED interface connectors on the baseboard (locking polarized, 4 position, single in-line, .025 in square pin).  See Appendix C for the pinout.  Pin 2 of both connectors is tied together as well as to the IDE connector (pin 39), the SCSI A LED signal and the front panel signal HD1_LED_ACT# (pin 10). They are tied together so that any of these sources can activate a light on the front panel to indicate hard drive access.

Likewise pin 3 of both connectors is tied together as well as to the SCSI B LED signal and the front panel signal HD2_LED_ACT# (pin 11).

The purpose of the connectors themselves is to provide a way for a front panel LED to be driven from an add-in disk controller.   Note Intel's AP450GX MP Server chassis does provide LED's on its front panel that can be driven by either of these signals.

## 1.19  Control Signals

### 1.19.1  Remote Sensing

Remote sensing exists on the +5.1 Vdc, +12 Vdc, and +3.3 Vdc outputs.  The -12 Vdc, -5 Vdc, and +5 V standby outputs are referenced to the negative (-) remote sense point.  Only voltage drops exterior to the power supply are included.  The loss of a remote sense connection will not cause the power supply to go into a high output voltage condition.  Intel strongly recommends using the signals for remote sense.  Without remote sense capabilities, it will be difficult to keep the power rails within the board set specifications.

**Table 1.11 Amount of Drop to Regulate**

| Output voltage | Maximum voltage drop |
| --- | --- |
| +5.1 Vdc | 0.3V |
| +12 Vdc | 0.2V |
| +3.3 Vdc | 0.2V |
| Ground | 0.2V |

### 1.19.2  Power Good (PGOOD & PWRGOOD) signals

Each power supply provides a power good signal to the power distribution backplane.  This signal indicates that all outputs have reached operating state. The PGOOD signal is deasserted for a minimum of 250uS before any of the output voltages fall below the regulation limit.  During normal power on, PGOOD will be asserted between 100mS and 1500mS after the 5.1V output reaches a minimum of 4.75V.

To indicate that all power supplies are within regulation, the PGOOD signals from each supply are OR'd together on the power distribution backplane to create a single PWRGOOD signal which is passed on to the baseboard.  The PWRGOOD signal has the same timing parameters as the individual PGOOD signals described above.

## 1.20  Baseboard Jumper Settings

**Table 1.12 Jumper Configuration, Baseboard**

| Baseboard configuration jumper summary (listed by block number on board) | Pins | Description |
|---|---|---|
| J6A1, BIOS Recovery | 1-2* | Normal BIOS boot block |
| | 2-3 | Recovery BIOS boot block |
| | | *If the normal BIOS gets corrupted, and you are unable to reload a new BIOS from floppy disk, install the jumper into recovery mode which will allow the system to boot from the recovery BIOS.* |
| J6A1, Boot Block Protect | 1-2* | BIOS boot block is write-protected |
| | 2-3 | BIOS boot block is programmable |
| | | *The programmable mode should only be enabled under carefully controlled circumstances.  Incorrect programming of the boot block will render the system unbootable.* |
| J6A4, BIOS write | 1-2 | Disables BIOS update of flash memory |
| | 2-3* | Enables BIOS update of flash memory with special utility |
| | | *Install the jumper in the enable mode when updating the system BIOS.  This jumper should always be set to enable.  Some operating systems will not boot without this jumper enabled.* |
| J6A4, Floppy 0 | 1-2 | For 1.44 MB diskette drive size or autodetection.  Disables 2.88 MB size detection |
| | 2-3* | For forced 2.88 MB diskette drive size |
| J6A2, Floppy 1 | 1-2 | For 1.44 MB diskette drive size or autodetection.  Disables 2.88 MB size detection |
| | 2-3* | For forced 2.88 MB diskette drive size |
| J6A2, Video Sleep | 1-2 | Video Sleep Register resides at 03C3H |
| | 2-3* | Video Sleep Register resides at 46E8H |
| J6A3, Power Control | 1-2 | Disables RTC power supply control |
| | 2-3* | Enables power supply control using RTC |
| | | *Under certain conditions the RTC can be programmed via the BIOS setup to turn off the system.  Installing the jumper in the enable mode allows the RTC to use this feature.* |

\* Factory default setting

## 1.20.1    BIOS Recovery Jumper, J6A1



**1-2    Normal BIOS boot block, factory default**

2-3    Recovery BIOS boot block
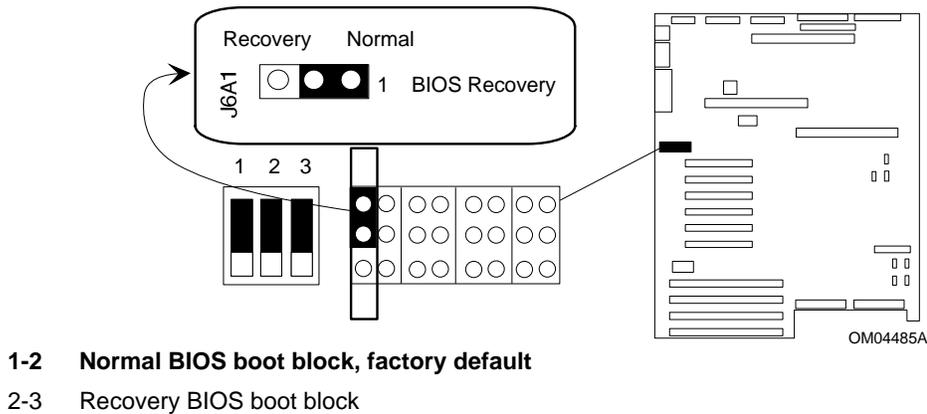
**Figure 1.11 BIOS Recovery Jumper**

This jumper enables the recovery mode for the BIOS flash memory.  This mode is important because the system BIOS can be corrupted—for example, when the update procedure is aborted due to a power outage.  The flash memory contains a protected area that cannot be corrupted. Code in this area is used to boot the computer from a diskette in drive A when the BIOS has been corrupted.  After booting, the flash Memory Update utility is used to automatically recover the system BIOS from the BIOS recovery files on the diskette.  (For normal operation, it is important to keep the jumper on pins 1 and 2.)   When the recovery procedure is run, another jumper, BIOS Write at J6A4, must also be in its default position (pins 2 and 3 jumpered).

## 1.20.1.1    System BIOS, Recovery Procedure

**Requirements:**

· At least 4 MB of RAM installed.

· Drive A: must be a 3.5-inch 1.44 MB diskette drive.

· On the system board, the configuration jumper at J6A4 must be in the default position (pins 2 and 3, BIOS Write enabled).

The recovery operation automatically updates only the main system BIOS. Video is not initialized, and the keyboard is disabled. Because there is no screen display, you will need to listen for these audible status signals:

**Audible Beeps Description**

1:   Signals beginning of recovery process; process takes 2 to 4 minutes.

2:   Signals successful completion, no errors.

4:   System could not boot from the diskette. Diskette may not be bootable.

Continuous series of low beeps (like a buzz):  Any or all of these causes:

- The wrong BIOS recovery files are being used.

- Configuration switch allowing BIOS Recovery mode is in wrong position.

- Configuration switch allowing BIOS Write to flash memory is in wrong position.

- One or more system BIOS FMUP files is corrupt or missing.

**WARNING:** If the system has been running, any processor and heat sink installed on the processor board will be hot. The system board configuration switches are immediately adjacent to a processor board connector. To avoid the possibility of a burn while accessing a configuration switch, let the components cool for 10 minutes before continuing with the procedures described here.

Before beginning recovery procedure If you have mapped the BIOS of an add-in board to any part of the E0000H address range, you must either map it to another area before beginning a recovery procedure or physically remove the board from the system.

1. Observe safety and ESD precautions.

2. If you have not already done so, create a bootable MS-DOS diskette, and copy the BIOS update to the diskette.

3. Turn off the system, and unplug the power cord(s).

4. Open the system. On the system board, move the BIOS Recovery jumper from pins 1 and 2 to pins 2 and 3.

5. Insert the Flash Memory Update diskette in drive A. Turn the system on. You will hear a single initial beep that is part of the typical system boot-up process.

6. Then you will hear another single beep that indicates the recovery process is beginning. The process takes two to four minutes. While in the recovery mode, there is no screen display on the monitor, and the keyboard is disabled as the system automatically recovers the BIOS.

7. You will hear two beeps when the process is successfully completed.

8. Make sure the diskette drive activity light is OFF. Turn off the system.

9. At J6A1, remove the BIOS Recovery jumper from pins 2 and 3, and place it back on pins 1 and 2.

10. Remove the FMUP diskette from drive A.

11. Close the system, plug in the power cord(s), and turn on the system. Check the BIOS version number against what you intended to flash in.

CMOS is not cleared when you update the BIOS. After doing the recovery procedure, clear CMOS. Also, you will need to flash in again any additional languages that were present before updating.

## 1.20.2   Boot Block Jumper, J6A1
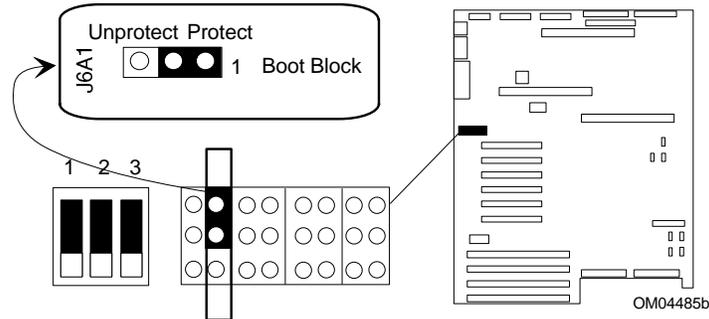


**1-2   BIOS boot block is write-protected, factory default**

**Figure 1.12 Boot Block Jumper**

⚠   **CAUTION, leave at factory-default setting, pins 1 and 2**

Always leave the Boot Block jumper installed in the factory-default position, on pins 1 and 2, to protect the BIOS boot block from being overwritten.

## 1.20.3   BIOS Write Jumper, J6A4
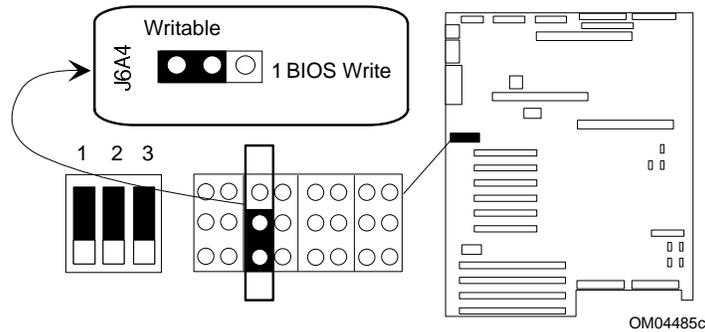


**2-3   Enables BIOS update of flash memory with special utility, factory default**

1-2   Disables BIOS update of flash memory (cannot overwrite the BIOS)

**Figure 1.13 BIOS Write Jumper**

⚠   **CAUTION, updating the BIOS requires special utility**

Changing this jumper should be done only by a qualified technical person, because updating the BIOS requires a special utility.

This jumper enables updating the BIOS in flash memory with a special utility.  The factory default is to leave this function enabled so that you can update the BIOS from a bootable diskette without needing to open the system and change the jumper.  For a copy of the utility to update the BIOS, contact your Intel representative.

## 1.20.4 Floppy 0 Jumper at J6A4; Floppy 1 Jumper at J6A2
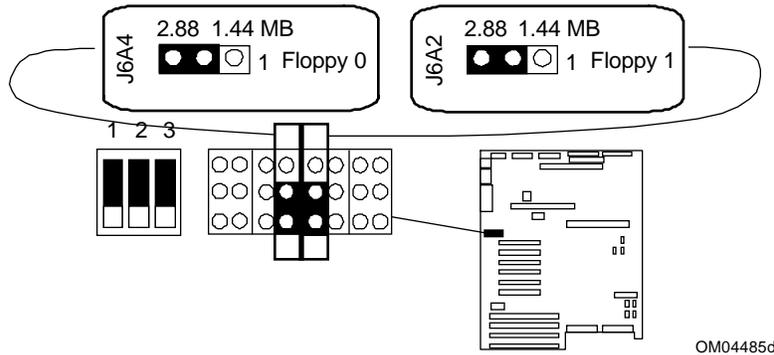


OM04485d

**2-3** **For forced 2.88 MB diskette drive size, factory default**

1-2 For 1.44 MB drive size or autodetection; disables 2.88 MB size detection

**Figure 1.14 Floppy Jumpers**

The Floppy 0 and Floppy 1 functions are set at separate jumper blocks, but the descriptions are identical. These jumpers configure the floppy drive port to force 2.88 MB drive size or to support automatic size detection.

## 1.20.5   Video Sleep Jumper, J6A2
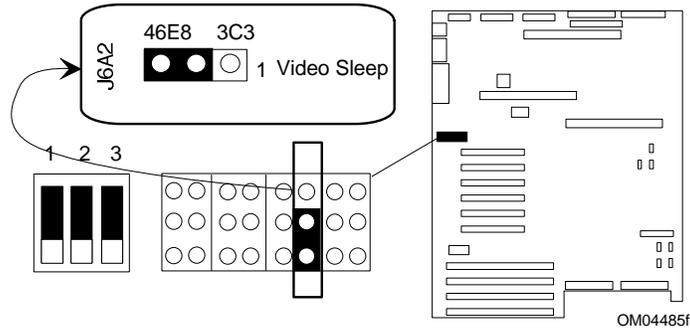


**2-3     Video Sleep register resides at 46E8H, factory default**

1-2     Video Sleep register resides at 03C3H

**Figure 1.15 Video Sleep Jumper**

The video address jumper determines which I/O port the onboard Cirrus Logic CL-GD5424 super VGA controller uses for its internal AT mode setup port.  The starting address of the default port is 046E8H.

If there is no keyboard activity after a specified time-out period (1 to 128 minutes as specified by using the SCU), the video sleep register blanks out the monitor screen.  When this happens, you must enter a password to reactivate the monitor and the keyboard.

## 1.20.6   Power Control Jumper, J6A3
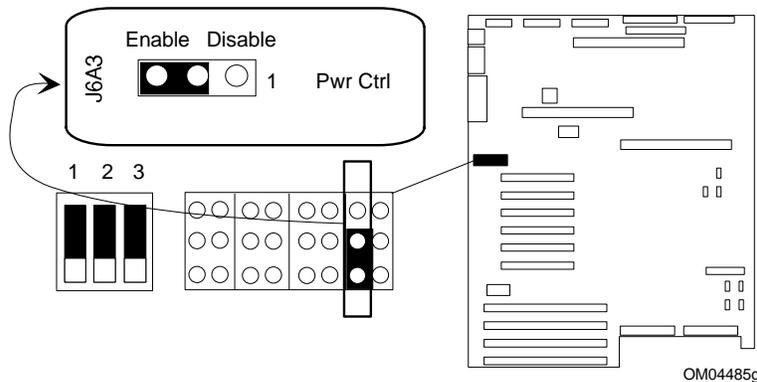


**2-3     Enables power supply control using the RTC, factory default**

1-2     Disables RTC power supply control

**Figure 1.16 Power Control Jumper**

This jumper (PWR CTRL) enables power supply control using the real-time clock.  Power control from the RTC is typically used for Automatic Server Recovery.  An alarm is set in the RTC by the BIOS or a utility program to power the system on or off at a predetermined time.

## 1.20.7  Configuration Switches
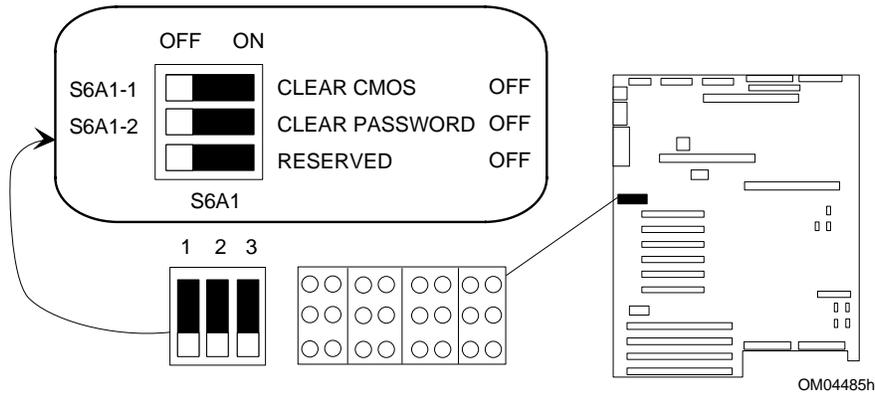


**Figure 1.17 Clear CMOS/Password Switch**

**Table 1.13 Switch Configuration, Baseboard**

| Switch | Position | Function |
| --- | --- | --- |
| S6A1-1 | On | Clear CMOS |
| | Off* | Normal operation |
| S6A1-2 | On | Clear password |
| | Off* | Normal operation |
| S6A1-3 | Off* | Reserved |

**To change setting, slide switch to desired position.**

*Factory default setting

### CMOS Switch, S6A1-1

Switch S6A1-1 controls whether settings stored in CMOS nonvolatile memory (NVRAM) are retained during a system reset:

- Switch OFF:  settings in CMOS and real-time clock are preserved during system reset.

- Switch ON:  settings in CMOS and real-time clock are reset to factory defaults during system reset.

To clear CMOS (restore to factory default values), do these steps:

1. Observe the safety and ESD precautions.  See Chapter 3 of the AP450GX MP Server System Installation Guide for this information.

2. Turn off system power and disconnect the AC power cord(s).

3. Remove the card cage side panel.  You do not need to remove the system board, and you probably do not need to remove any add-in boards.

4. On the system board, at switch S6A1-1, CLEAR CMOS, slide switch to ON.

5. Install side panel for your safety.  Connect the power cord(s), and turn on the system.

6. Wait for POST to complete and the message "NVRAM cleared by jumper" to appear.

7. Turn off system power and disconnect the AC power cord(s).

8. Remove the side panel again.

9. At switch S6A1-1, slide switch to OFF (the original position). Setting it to OFF preserves the settings during system reset.

10. Install side panel, connect the power cord(s), and turn on the system.

11. Run BIOS Setup to verify the correct settings.


## Password Switch, S6A1-2

This switch controls whether a stored password is retained or cleared during a system reset:

- Switch OFF: lets you enter a password that is preserved even during system reset.

- Switch ON: clears the password during system reset.

To clear and enter a password, do these steps:

1. Observe the safety and ESD precautions. See Chapter 3 of the AP450GX MP Server System Installation Guide for this information.

2. On the system board, slide switch to ON (to clear old password).

3. Turn system on and wait for POST to complete. The password will have been cleared automatically.

4. Turn system off.

5. Slide switch to OFF to resume normal operation (your settings are retained during system reset).

6. Run Setup to specify a new password. When you reboot the system, the new password will have been retained.

## 1.21  Processor Module Jumper Settings

**Table 1.14 Jumper Configuration, Processor Module**

| Processor board jumper summary | Pins | Description |
| --- | --- | --- |
| J101 and J106, scan for processor (SCAN) | 1-2* | Processor not installed in adjacent socket** |
| | 2-3 | Processor installed in adjacent socket |
| J103, voltage identification (VID)*** | 1-2 | If jumper is installed, VID is disabled, processor 2.  If not installed, VID is enabled, processor 2. |
| | 3-4 | If jumper is installed, VID is disabled, processor 1.  If not installed, VID is enabled, processor 1. |
| | 5-6* | Park - not connected |
| | 7-8* | Park - not connected |
| J105, processor frequency select (SEL)<br><br>(see Table 1.15) | 1-2* | SEL0 |
| | 3-4 | SEL1 |
| | 5-6 | SEL2 |
| | 7-8 | Park - not connected |
| | 9-10 | Park - not connected |
| | 11-12 | Park - not connected |

\*    Factory default setting.
\*\*   The pins at J101 and J106 are only useful when using the ITP.  During normal operation they have no
     effect on the system.
\*\*\*  J103 block may not be present on all versions of the processor module.  If not present, then VID is
     enabled and is not selectable.

## 1.21.1   SCAN Jumpers, J101 and J106



OM04282
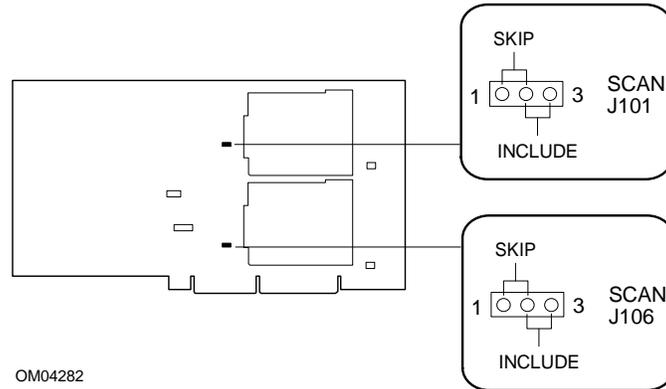
**1-2  Processor not installed in adjacent socket (SKIP position), factory default**

2-3  Processor installed in adjacent socket (INCLUDE position)

**Figure 1.18 SCAN Jumpers**

There are two SCAN jumper blocks, one for each processor socket.  These are used to determine if a processor is installed in the socket adjacent to a given jumper block.  In normal operation, these jumpers have no function and are useful only during low-level processor ITP bus debugging.

## 1.21.2   VID Jumpers, J103



OM04285
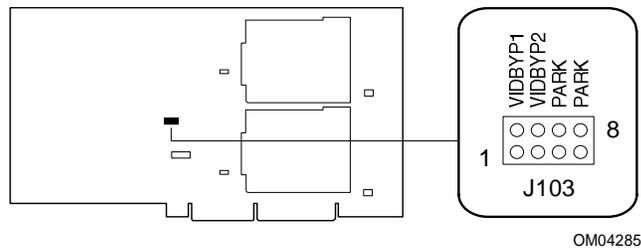
1-2 VID bypass 1; 3-4 VID bypass 2

**5-6 Park, factory default; 7-8 Park, factory default**

**Figure 1.19 VID Jumpers**

The settings at J103 depend on whether processors are voltage-ID-ready or not.  In general, voltage identification (VID) is default-enabled; that is, the unused jumpers are placed in the Park locations.  The J103 block is present only on early versions of the processor board; later versions have VID enabled at all times.

To disable VID for processor 2, move a jumper to pins 1 and 2 (VIDBYP1).

To disable VID for processor 1, move a jumper to pins 3 and 4 (VIDBYP2).  (This is the correct description:  VIDBYP1 refers to processor 2, and VIDBYP2 to processor 1.)

*Note:       J103 block may not be present on all versions of the processor module.  If not present, then VID is enabled and is not selectable.*

## 1.21.3    Processor Frequency Select Jumpers, J105



OM04284
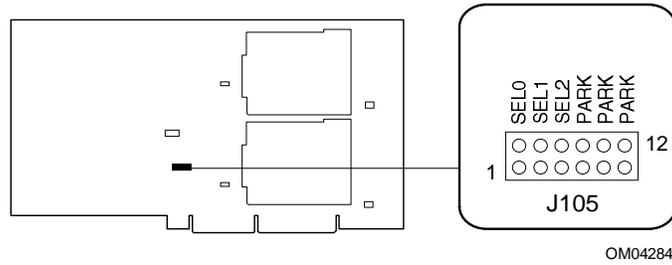
**Figure 1.20 Processor Frequency Jumpers**

⚠    **CAUTION, select the actual frequency setting**

Damage to the processor may occur if you select a jumper setting frequency that is greater than the actual frequency of the processor.

Use this jumper block to select the processor core/bus frequency.  The selection must match the frequency of the processor being installed in the system.  Be sure that both boards are programmed to the same frequency.  Install jumpers for the desired frequency as shown in the following table.  Place any unused jumpers in the Park locations (pins 7-8; 9-10; 11-12).

**Table 1.15 Frequency Jumper Configurations**

| Frequency | SEL0 Pins 1-2 | SEL1 Pins 3-4 | SEL2 Pins 5-6 |
|---|---|---|---|
| 150/60 MHz | No jumper | No jumper | No jumper |
| 180/60 MHz | Jumper | No jumper | No jumper |
| 210/60 MHz | No jumper | Jumper | No jumper |
| 240/60 MHz | Jumper | Jumper | No jumper |
| 166/66 MHz | No jumper | No jumper | Jumper |
| 200/66 MHz | Jumper | No jumper | Jumper |
| 233/66 MHz | No jumper | Jumper | Jumper |
| 266/66 MHz | Jumper | Jumper | Jumper |

**Example, jumpering for 150/60 MHz**     **Example, jumpering for 200/66 MHz**
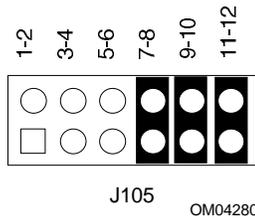


J105     OM04280          J105     OM04283
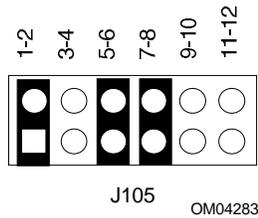
## 1.21.4   Processor Board Fan Sink Connectors, J102 and J107
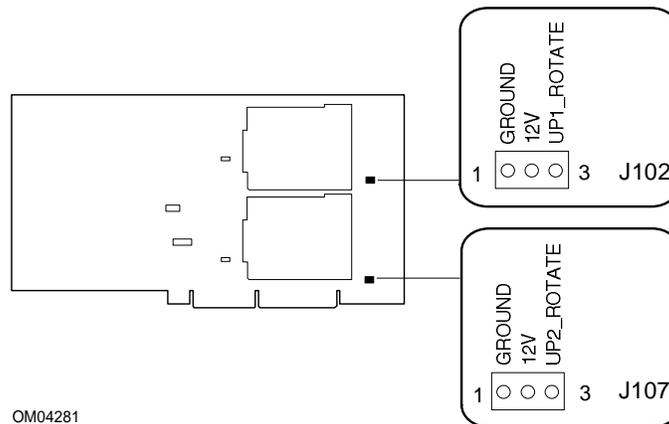


**Figure 1.21 Fan Sink Connectors**

J102 and J107 are connectors to provide power for optional fan sinks to cool the processors while the board set is being tested outside of the chassis on a test bench.  Each fan sink comes with a 3-pin connector wire.  The connectors are not used in normal system operation.

### 1.21.5   Power Supply Considerations

The AP450GX MP Server Board Set is designed to operate with 2 or 3 420W custom power supplies when installed in Intel's AP450GX MP Server chassis.  Refer to Chapter 5 for the actual power requirements. Intel strongly recommends using the signals provided for remote sense. Without remote sense capabilities, it will be difficult to keep the power rails within the board set's specifications.

## 1.22   Regulatory Compliance

**Table 1.16 Regulatory Specifications**

| Board | Specification |
| --- | --- |
| Safety | UL 1950<br>CSA 22.2 No. 950 -M93 by cUL<br>EN 60950 by TÜV<br>IEC 950 by TÜV<br>EN 60950 and Nordic deviations by NEMKO |
| Electromagnetic Emissions | Certified to FCC 47 Class B<br>Tested, CISPR 22/85 Class B, EN 55022 Registered with VCCI<br><br>Declaration of the Manufacturer or Importer:  We hereby certify that this product is in compliance with EU Directive 89/336/EEC, using the EMC standards EN55022, EN61000-3-2 and EN50082-2. |
| Electromagnetic Immunity | Verified to comply with EN 50082-2 |

## 1.23   Product Certification Markings

## 1.23.1   European CE Marking

Marking on the board or shipping container.

## 1.23.2   UL Recognition

UL Recognized Marking consists of UL File No. E139761 on component side of board PB No. on solder side of board.  Board material flammability is 94V-1 or -0.

## 1.23.3   Canadian Compliance

Marking consists of small c followed by a stylized backward UR on component side of board.

## 1.23.4 Installation Requirements

### ⚠ CAUTION

*To avoid an adverse impact on the compliance with safety or regulatory requirements due to installation of this board assembly, the following guidelines must be followed.*

### 1.23.4.1 Follow Installation Instructions

Be sure to read and adhere to all of these instructions, and the instructions supplied with the host system and associated modules. If the instructions of the host system appear to be incompatible with these instructions or the instructions of any associated modules, contact the suppliers' technical support organization for the products involved to determine the appropriate action for continued safety and regulatory compliance of the resultant system. Failure to read and follow instructions provided by host system and module suppliers may result in increased safety risk and non-compliance with regional laws and regulations.

### 1.23.4.2 Assure Host System Compatibility

For electromagnetic compatibility, the host system enclosure and power supply should have passed electromagnetic compatibility testing using a board with a processor from the same family as the processor on this board, operating at the same or higher processor speed. Also, only peripherals (computer input/output devices, terminals, printers, etc.) that are CE Marked and certified by the FCC to comply with Class B limits may be attached to this board. Pay particular attention to the installation instructions of the host system and other modules, particularly concerning certifications, external I/O cable shielding and filtering, mounting, grounding and bonding requirements to assure appropriate shielding effectiveness. Otherwise electromagnetic compatibility testing must be repeated on a representative sample of the complete system.

For safety, if mis-mating of connectors could result in a hazard, assure that all connectors are sufficiently keyed to prevent mis-mating.

### 1.23.4.3 Use Only In Intended Applications

This product was evaluated for use in systems installed in offices, homes, schools, computer rooms or similar applications. Other applications, such as medical, industrial, alarm systems and test equipment may necessitate a re-evaluation of the product suitability.

### 1.23.4.4 Assure Host System & Accessory Certifications

Assure that the host system, any other subassemblies such as board and drive assemblies being added in, and internal or external wiring, are properly certified for the region(s) the end-product will be used in. Proof of certification can be determined by the marks on the product. For example:

#### 1.23.4.4.1 Europe

The CE Marking signifies compliance with all relevant EU requirements. If the host system does not bear the CE Marking, obtain a supplier's Declaration of Conformity to the appropriate standards required by the European EMC Directive and Low Voltage Directive. Other directives,

such as the Machinery and Telecommunications Directives, may also apply depending on the type of product. No regulatory assessment is necessary for low voltage DC wiring used internally, or wiring used externally when provided with appropriate overcurrent protection. Appropriate protection is achieved by a maximum 8 Amp current limiting circuit or a maximum 5 Amp fuse or Positive Temperature Coefficient Resistor (PTC). All Intel baseboards presently have PTC's on all external ports which provide DC power externally.

### 1.23.4.4.2  U.S.

For safety, a certification mark by a Nationally Recognized Testing Laboratory (NRTL) such as UL, CSA or ETL. External wiring must be UL Listed and suitable for the use. Internal wiring must be UL Listed or Recognized and rated appropriately for the voltages and temperatures involved. For electromagnetic interference, the FCC mark: Class A for commercial or industrial only; or Class B for all applications other than described above.

### 1.23.4.4.3  Canada

For safety, a nationally recognized certification mark such as CSA or cUL. No regulatory assessment is necessary for low voltage DC wiring used internally, or wiring used externally when provided with appropriate overcurrent protection. Appropriate protection is achieved by maximum 8 Amp current limiting circuit or a maximum 5 Amp fuse or Positive Temperature Coefficient Resistor (PTC). All Intel baseboards presently have PTC's on all external ports which provide DC power externally.

## 1.23.5  Installation Precautions

During installation and initial test, use caution to avoid personal injury and damage to wiring due to sharp pins on connectors and printed circuit assemblies, rough chassis edges and corners, and hot components. Adhere to warnings and limitations regarding accessibility into areas designated only for authorized technical personnel.

## 1.23.6  Battery Marking

There is insufficient space on this board product to provide the required replacement and disposal instructions for the battery. The following marking must be placed permanently and legibly on the host system as near as possible to the battery:

## ⚠ CAUTION

*Danger of explosion if battery is incorrectly replaced.*

*Replace with only the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.*

## 1.23.7  Overload Protection

Unless the power supply is provided with inherent overcurrent protection, use caution to avoid overloading the power supply output. This can be accomplished by assuring that the calculated total current load of all the modules within the system is less than the output current rating of the power supply. Failure to accomplish this could result in overheating in the power supply, which

could result in a fire or could cause damage to insulation separating hazardous AC line circuitry from low-voltage user accessible circuitry.  If the load drawn by a particular module cannot be determined by the markings and instructions supplied with the module, contact the module supplier's technical support organization.

# 2  System Resources

## 2.1  Memory Map

**Table 2.1 Memory Addressing**

| Address Range (hex) | Amount | Function |
|---|---|---|
| 0000_0000H – 0007_FFFFH | 512 KB | Base system memory (fixed) |
| 0008_0000H – 0009_FFFFH | 128 KB | Base system memory or ISA memory enabled in Setup |
| 000A_0000H – 000B_FFFFH | 128 KB | ISA video buffer |
| 000C_0000H – 000E_7FFFH | 160 KB | Video BIOS, AIC-7880 SCSI BIOS, other option ROMs. All these can be shadowed |
| 000E_8000H – 000F_FFFFH | 96 KB | System BIOS and data areas (fixed) |
| 0010_0000H – 00EF_FFFFH | 14 MB | System memory or unused |
| 00F0_0000H – 00FF_FFFFH | 1 MB | System memory or EISA memory |
| 0100_0000H – FEBF_FFFFH | 4060 MB | System memory or add-in cards or unused |
| FEC0_0000H – FEC0_0FFFH | 4 KB | I/O APIC #1 |
| FEC0_1000H – FEC0_1FFFH | 4 KB | I/O APIC #2 |
| FEC0_2000H – FEC0_7FFFH | 24 KB | Unused |
| FEC0_8000H – FEC0_8FFFH | 4 KB | Local APIC |
| FEC0_9000H – FFF7_FFFFH | 4939 KB | Add-in card or unused |
| FFF8_0000H – FFFF_FFFFH | 512 KB | System BIOS (fixed) |

## 2.2  I/O Map

**Table 2.2 I/O Addressing**

| I/O address | Resource |
|---|---|
| 0000 – 001F | DMA controller 1 |
| 0020 – 0021 | Interrupt controller 1 |
| 0022 – 0023 | EISA bridge configuration space access ports |
| 0040 – 005F | Programmable Timer |
| 0060 – 0064 | Keyboard Controller |
| 0061 | NMI Status & Control Register |
| 0070 | NMI Mask (bit 7) & RTC Address (bits 6:0) |
| 0071 | Real-time Clock (RTC) |
| 0080 – 0081 | PCEB BIOS Timer |
| 0080 – 008F | DMA Low Page Register |
| 0092 | System Control Port A ( PC-AT control Port) |
| 00A0 – 00BF | Interrupt Controller 2 |
| 00C0 – 00DF | DMA Controller 2 |
| 00F0 | Clear NPX error |
| 00F8 – 00FF | x87 Numeric Coprocessor |
| 0102 | Video Display Controller |
| 0170 – 0177 | Secondary Fixed Disk Controller (IDE) |
| 01F0 – 01F7 | Primary Fixed Disk Controller (IDE) |
| 0278 – 027F | Parallel Port 2 (relocatable) |
| 02E8 – 02EF | Serial Port 4 (relocatable) |
| 02F8 – 02FF | Serial Port 2 (relocatable) |
| 0370 – 0377 | Secondary Floppy |
| 0378 – 037F | Parallel Port 1 (relocatable) |
| 03B4 – 03BA | Monochrome Display Port |
| 03BC – 03BF | Parallel Port 3 |
| 03C0 – 03CF | Enhanced Graphics Adapter |
| 03D4 – 03DA | Color Graphics Controller |

**System I/O Map, continued**

| I/O address | Resource |
| --- | --- |
| 03E8 – 03EF | Serial Port (relocatable) |
| 03F0 – 03F7 | Floppy Disk Controller |
| 03F8 – 03FF | Serial Port 1 (relocatable) |
| 0400 – 043F | DMA Controller 1, Extended Mode Registers |
| 0461 | Extended NMI / Reset Control |
| 0462 | Software NMI |
| 0464 | Last EISA Bus master granted |
| 0480 – 048F | DMA High Page Register |
| 04C0 – 04CF | DMA Controller 2, High Base Register |
| 04D0 – 04D1 | Interrupt Controllers 1 and 2 Control Register |
| 04D4 – 04D7 | DMA Controller 2, Extended Mode Register |
| 04D8 – 04DF | Reserved |
| 04E0 – 04FF | DMA Channel Stop Registers |
| 0C80 – 0C83 | EISA System Identifier Registers |
| 0C84 | Board Revision Register |
| 0CA0-0CA1 | $I^2C$ Interface Base Address |
| 0CF8 | PCI CONFIG_ADDRESS Register |
| 0CFC | PCI CONFIG_DATA Register |
| n000 –n0FF | EISA Slot n I/O Space (n = 1 to 4) |
| x100 – x3FF | ISA I/O slot alias address |
| n400 – n4FF | EISA Slot n I/O Space (n = 1 to 4) |
| x500 – x7FF | ISA I/O slot alias address |
| n800 – n8FF | EISA Slot n I/O Space (n = 1 to 4) |
| x900 – xBFF | ISA I/O slot alias address |
| nC00 – nCFF | EISA Slot n I/O Space (n = 1 to 4) |
| xD00 – xFFF | ISA I/O slot alias address |

## 2.3 PCI Configuration Space Map

**Table 2.3 PCI Configuration Space Map**

| Bus Number (hex) | Dev Number (hex) | Function Number (hex) | Description |
|---|---|---|---|
| 00 | C8 | 00 | Intel 82454GX (PB) PCI Bridge - Bus 0 (Compatibility) |
| 00 | D0 | 00 | Intel 82454GX (PB) PCI Bridge - Bus 1 |
| 00 | A0 | 00 | Intel 82453GX (DC) Memory Controller |
| 00 | 78 | 00 | INCA |
| 00 | 70 | 00 | PCEB |
| 00 | 58 | 00 | P1 (PCI Bus 0, slot 1) |
| 00 | 60 | 00 | P2 (PCI Bus 0, slot 2) |
| 00 | 68 | 00 | P3 (PCI Bus 0, slot 3) |
| 01 | 60 | 00 | On-board SCSI controller, Channel B |
| 01 | 58 | 00 | On-board SCSI controller, Channel A |
| 01 | 50 | 00 | P4 (PCI Bus 1, slot 1) |
| 01 | 68 | 00 | P5 (PCI Bus 1, slot 2) |
| 01 | 70 | 00 | P6 (PCI Bus 1, slot 3) |

## 2.4 DMA Channels

**Table 2.4 DMA Channel Mapping**

| Channel | Device |
|---|---|
| 0 | (add-in board) |
| 1 | (add-in board) |
| 2 | Diskette drive |
| 3 | IDE hard disk drive |
| 4 | Reserved |
| 5 | (add-in board) |
| 6 | (add-in board) |
| 7 | (add-in board) |

## 2.5  Interrupts

**Table 2.5 Interrupt Mapping**

| IRQ | Device |
|-----|--------|
| NMI | Parity error |
| 0 | Interval timer |
| 1 | Keyboard buffer full |
| 2 | Reserved, cascade interrupt from slave PIC |
| 3 | Onboard serial port B (COM2) or add-in board |
| 4 | Onboard serial port A (COM1) or add-in board |
| 5 | Parallel port LPT2 or add-in board |
| 6 | Onboard diskette (floppy) controller, if enabled |
| 7 | Parallel port LPT1 or add-in board |
| 8 | Real-time clock (RTC) |
| 9 | (add-in board) |
| 10 | (add-in board) |
| 11 | (add-in board) |
| 12 | Onboard PS/2 mouse port or add-in board |
| 13 | Math coprocessor error |
| 14 | IDE hard drive controller, if enabled |
| 15 | (add-in board) |

# 3   BIOS, Setup, SCU and SCSISelect Utilities

## 3.1   Introduction

The AP450GX MP Server Board Set uses an Intel BIOS, which is stored in flash memory and easily upgraded using a floppy disk-based program.  In addition to the Intel BIOS, the flash memory also contains the Setup utility, Power-On Self Tests (POST), the PCI auto-configuration utility, and Windows 95 ready Plug-N-Play 1.0a. This board set also supports system BIOS shadowing, allowing the BIOS to execute from 64-bit on-board write-protected DRAM.  The Setup and SCU utilities are used to change configuration values in flash memory.  In addition, the SCSISelect utility is provided to configure the on-board AIC-7880 SCSI controllers. All three utilities are briefly described in this chapter.  Refer to the AP450GX MP Server Installation Guide, Intel Part #642976, for more detail on each utility.

## 3.2   BIOS

The BIOS displays a sign-on message during POST identifying the type of BIOS and a five-digit revision code. The initial production BIOS in the baseboard is identified as 1.00.04.CD0

### 3.2.1   BIOS Flash Memory Organization

The Intel  4Mb flash component is organized as 512K x 8 (512 KB).  The flash device is divided into eight areas, as described in Table 3.1.

**Table 3.1 Flash Memory Organization**

| System Address | | FLASH Memory Area |
|---|---|---|
| FFFF0000H | FFFFFFFFH | 64 KB Main BIOS |
| FFFEC000H | FFFEFFFFH | 16 KB Boot block (Not FLASH erasable) |
| FFFEA000H | FFFEBFFFH | 8 KB ESCD Area (Plug-N-Play data storage area) |
| FFFE9000H | FFFE9FFFH | 4 KB Reserved for BIOS |
| FFFE8000H | FFFE8FFFH | 4 KB OEM Logo Area |
| FFFE0000H | FFFE7FFFH | 32 KB Reserved for BIOS |
| FFFD0000H | FFFDFFFFH | 64 KB Reserved for BIOS |
| FFFC0000H | FFFCFFFFH | 64 KB Reserved for BIOS |

### 3.2.2   BIOS Upgrades

Flash memory makes distributing BIOS upgrades easy.  A new version of the BIOS can be installed from a diskette.  BIOS upgrades are available from your Intel representative.

The disk-based flash upgrade utility, FMUP.EXE, has three options for BIOS upgrades:

- The flash BIOS can be updated from a file on a disk;
- The current BIOS code can be copied from the flash memory to a disk file as a backup in the event that an upgrade cannot be successfully completed; or

- The BIOS in the flash device can be compared with a file to ensure the system has the correct version.

The upgrade utility ensures the upgrade BIOS extension matches the target system to prevent accidentally installing a BIOS for a different type of system.

### 3.2.3  ISA IDE Support

The ISA based IDE connector with independent I/O channel support are setup up automatically by the BIOS if the user selects "Autoconfiguration" in setup.  The IDE interface supports PIO Mode 3, and  Mode 4 hard drives and recognition of ATAPI CD-ROMs, tape drives, and any other ATAPI devices.  The BIOS will determine the capabilities of each drive and configure them to optimize capacity and performance.  For the high capacity hard drives typically available today, the drive will be automatically configured for Logical Block Addressing (LBA) for maximum capacity and to PIO Mode 3 or 4 depending on the capability of the drive.  The user is able to override the auto-configuration options by using the manual mode setting.  The ATAPI Specification Revision 2.5 recommends that an ATAPI device be configured as shown in the table below.

**Table 3.2 Recommendations for Configuring an ATAPI Device**

| Primary Cable | | Secondary Cable | | |
| --- | --- | --- | --- | --- |
| Drive 0 | Drive 1 | Drive 0 | Drive 1 | |
| ATA | | | | Normal, no ATAPI |
| ATA | | ATAPI | | Disk and CD-ROM for enhanced IDE systems |
| ATA | ATAPI | | | Legacy IDE System with only one cable |
| ATA | | ATAPI | ATAPI | Enhanced IDE with CD-ROM and a tape or two CD-ROMs |

### 3.2.4  PCI Auto-Configuration

The PCI auto-configuration utility operates in conjunction with the system Setup utility to allow the insertion and removal of PCI cards to the system without user intervention (Plug-N-Play).  When the system is turned on after adding a PCI add-in card, the BIOS automatically configures interrupts, I/O space, and other parameters.  PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card, or system resources.

The PCI Auto-Configuration function complies with version 2.0 of the PCI BIOS specification.  System configuration information is stored in ESCD format.  The ESCD data may be cleared by setting the CMOS clear jumper to the ON position.

PCI specification 2.0 for add-in card auto-configuration is also a part of the Plug-N-Play BIOS.  Peer-to-peer hierarchical PCI Bridge 1.0  is supported, and by using an OEM supplied option ROM or TSR, a PCI-to-PCMCIA bridge capability is possible as well.

### 3.2.5  ISA Plug-N-Play

The BIOS incorporates ISA Plug-N-Play capabilities as delivered by Plug-N-Play Release 1.0A (Plug-N-Play BIOS version 1.0A, ESCD version 1.03).  When used in conjunction with the System  Configuration Utility (SCU) for DOS, the system allows auto-configuration of Plug-N-

Play ISA cards, PCI cards, and resource management for legacy ISA and EISA cards. System configuration information is stored in ESCD format. The ESCD data may be cleared by setting the CMOS clear jumper to the ON position.

The BIOS also has a setup option to support the Windows 95 run time Plug-N-Play utilities. When this option is selected, only devices critical to booting are assigned resources by the BIOS. Device node information is available for all devices to ensure compatibility with Windows 95.

Note:  copies of the Intel Plug-N-Play specification may be obtained via the Intel BBS , via CompuServe by typing "Go PlugPlay", or on the Intel corporate web site at www.intel.com.

## 3.2.6   Language Support

The BIOS setup screen and help messages are supported in 32 languages.  There are five languages available at this time:  American English, German, Italian, French, and Spanish. Translation to other languages may become available at a later date.

## 3.2.7   Boot Options

Booting from CD-ROM is supported in adherence to the "El Torito" v. 1.0 bootable CD-ROM format specification developed by Phoenix Technologies and IBM.  Under the *Boot Options* field in setup, *CD-ROM* is one of four possible boot devices which are defined in priority order.  The default setting is for floppy to be the primary boot device and hard drive to be the secondary boot device.  If CD-ROM is selected, it must be the first device.  The third and fourth devices are set to *disabled* in the default configuration.  The user can add also select *network* as a boot device.  The network option allows booting from a  network add-in card with a remote boot ROM installed.

⟹ **NOTE**

*A copy of "El Torito CD-ROM Boot  v1.0"  is available on the Phoenix Web page (http://www.ptltd.com/techs/specs.html).*

## 3.2.8   Console Redirection

The BIOS supports redirection of both the video and keyboard via a serial port (COM 1 or COM 2).  When console redirection is enabled, keyboard input and video output is transferred not only through the normal keyboard and video connections, but also via the serial port (i.e. keyboard inputs from both sources are considered valid and video is displayed to both sources).  If you choose, the system can be operated without a keyboard or monitor attached to the system and run entirely via the remote console.  Both Setup and the SCU can be used while console redirection is enabled.

When connecting a modem up to the COM port, it should be configured in both auto-answer and the modems reaction to DTR must be to switch to command state.

## 3.2.8.1   Keystroke Mappings

During console redirection, the **remote** terminal (which may be a dumb terminal or a system with a modem running a package such as ProComm) sends keystrokes to the **local** server, which then passes video back.  For keys which have an ASCII mapping (such as A and Ctrl-A), the ASCII

character is sent.  For keys which do not have an ASCII mapping (such as F1 and Alt-A), a string of characters as defined in the tables below is sent.

The strings are based on the ANSI BBS and vt100 terminal standards.  Since these terminals do not support all the keys on the standard 101 key U.S. keyboard, some additional characters were added (such as F5 - F12, Page Up, and Page Down.)  Alt key combinations were created by adding the prefix  **^[}** to the character (both ^[}a and ^[}A will be interpreted at the local server as alt-a.).  In addition, ^[{ will be interpreted as a screen refresh.

Since the mappings for non-ASCII keys are done via table lookup, the decision was made not to support unusual combinations such as Ctrl-F1.  This saves space in BIOS, as well as a good deal of coding to interpret these sequences.

**Table 3.3 Non-ASCII Key Mappings**

| Key | Normal | Shift | Ctrl | Alt |
|---|---|---|---|---|
| ESC | ^[ | NS | NS | NS |
| F1 | ^[OP | NS | NS | NS |
| F2 | ^[OQ | NS | NS | NS |
| F3 | ^[OR | NS | NS | NS |
| F4 | ^[OS | NS | NS | NS |
| F5 | ^[OT | NS | NS | NS |
| F6 | ^[OU | NS | NS | NS |
| F7 | ^[OV | NS | NS | NS |
| F8 | ^[OW | NS | NS | NS |
| F9 | ^[OX | NS | NS | NS |
| F10 | ^[OY | NS | NS | NS |
| F11 | ^[OZ | NS | NS | NS |
| F12 | ^[O1 | NS | NS | NS |
| Print Screen | NS | NS | NS | NS |
| Scroll Lock | NS | NS | NS | NS |
| Pause | NS | NS | NS | NS |
| Insert | ^[[L | NS | NS | NS |
| Delete | (7Fh) | NS | NS | NS |
| Home | ^[[H | NS | NS | NS |
| End | ^[[K | NS | NS | NS |
| Pg Up | ^[[M | NS | NS | NS |
| Pg Down | ^[[2J | NS | NS | NS |
| Up Arrow | ^[[A | NS | NS | NS |
| Down Arrow | ^[[B | NS | NS | NS |
| Right Arrow | ^[[C | NS | NS | NS |
| Left Arrow | ^[[D | NS | NS | NS |
| tab | (09h) | NS | NS | NS |

NS = Not supported, (xxh) = ASCII character xx

**Table 3.4 ASCII Key Mappings**

| Key | Normal | Shift | Ctrl | Alt |
|---|---|---|---|---|
| backspace | (08h) | (08h) | (7Fh) | ^[}(08h) |
| (accent) ` | ` | (tilda) ~ | NS | ^[}` |
| 1 | 1 | ! | NS | ^[}1 |
| 2 | 2 | @ | NS | ^[}2 |
| 3 | 3 | # | NS | ^[}3 |
| 4 | 4 | $ | NS | ^[}4 |
| 5 | 5 | % | NS | ^[}5 |
| 6 | 6 | ^ | NS | ^[}6 |
| 7 | 7 | & | NS | ^[}7 |
| 8 | 8 | * | NS | ^[}8 |
| 9 | 9 | ( | NS | ^[}9 |
| 0 | 0 | ) | NS | ^[}0 |
| (dash) - | - | (under) _ | (1Fh) | ^[}- |
| = | = | + | NS | ^[}= |
| a to z | a to z | A to Z | (01h) to (1Ah) | ^[}a to ^[}z |
| [ | [ | { | (1Bh) | ^[}[ |
| ] | ] | } | (1Dh) | ^[}] |
| \ | \ | \| | (1Ch) | ^[}\ |
| (semi-colon) ; | ; | (colon) : | NS | ^[}; |
| (apostrophe) ' | ' | (quote) " | NS | ^[}' |
| (comma) , | , | < | NS | ^[}, |
| (period) . | . | > | NS | ^[}. |
| / | / | ? | NS | ^[}/ |
| (space) | (20h) | (20h) | (20h) | ^[}(20h) |

NS = not supported, (xxh) = ASCII character xx

## 3.2.8.2   Limitations

Console redirection can only be used in "Real Mode".  It will not work in "Protected Mode".
Console redirection only works with text based video, and will not work with graphics based
video applications.  For keyboard redirection to work, the application on the local server must use
the INT 16 keyboard services normally to receive keystrokes.  If the program uses INT 9 and INT
15 services instead, the redirection will not work. For example, the DOS edit program cannot be
used remotely due to the way it gets keys in the menu code and WordPerfect will not work due to
its extensive use of Shift-F1, Ctrl-F1 and other "special" keystrokes.

## 3.3  BIOS Setup

The Setup utility stores configuration values in flash memory and in the battery-backed memory of the real-time clock (RTC).  Values you enter in Setup are overwritten if you change these values in the SCU and save them.

For a number of options, the settings are made by using the SCU, not Setup.  The values are simply displayed in the Setup screens.  To see the descriptions of such options, refer to the SCU section later in this chapter.

Setup has four major menus and several sub-menus.  To move between the major menus, use the $\leftarrow \rightarrow$ keys.  To display the sub-menus, press <Enter> when the prompt is displayed beside an option name.

| When you see this on the screen: | What it means |
|---|---|
| On screen, an option is grayed out. In the tables in this chapter, the phrase "Display only" appears in the "Choice" column. | You cannot change or configure the option through Setup.  You must use (1) a different Setup screen or (2) the SCU.  In some cases, the option may be auto-configured or auto-detected. |
| On screen, the phrase <Press Enter> appears next to the option, and, in the tables here, in the "Default/next menu" column. | Press <Enter> to display a sub-menu (either a separate full-screen menu or a small pop-up menu with one or several choices). |
| "Default/next menu" appears as a column header in the tables here. | The column shows either the default option setting, a grayed-out "display only" setting, or a "Press Enter" prompt that leads to a separate menu. |

### 3.3.1  When to Run Setup

... if you get a boot-time prompt that says to do so.

... if you need to enable or properly configure your diskette drive.

... if you do not have access to a diskette drive.

Much of the system configuration is done through the SCU, not Setup.  Because the SCU is provided on diskette, a diskette drive needs to be connected and enabled.  After configuring the system, you may prefer to secure it against casual or unauthorized access by someone using diskettes.  Therefore, you can

- run Setup to enable the diskette drive

- then use Setup or the SCU to configure the system

- run Setup again to disable the diskette drive for security

Refer to the AP450GX MP Server System Installation Guide, Intel Part #642976, for more details on the BIOS Setup utility.

## 3.4  System Configuration Utility (SCU)

The System Configuration Utility (SCU) is the main tool to configure the system or to check or change the configuration.  Most system settings can be entered from either the SCU or BIOS Setup, but the SCU provides conflict resolution as well as access to information about ISA, EISA, and PCI adapters.

⇒　　　**System must have a diskette drive**

Your system must have a diskette drive present and enabled to use the SCU, because it is provided on a diskette.  If a drive is present but is disabled or improperly configured, use the BIOS Setup utility to enable or configure the diskette drive.  Then make a bootable SCU diskette and use the SCU to configure the system.

### 3.4.1  When to Run the SCU

...when you first set up and configure your system

...if you get a configuration error message at power-on

...each time you add, remove, or move an EISA or ISA add-in board

...each time you add or remove a Plug-N-Play or PCI add-in board

...each time you add or remove memory

### 3.4.2  Where the SCU Gets Information

| Information comes from | Description |
| --- | --- |
| Configuration (.CFG) or overlay (.OVL) files | For the baseboard, we provide these files.  For EISA and some ISA add-in boards, each comes with a diskette that contains a .CFG file (and an optional .OVL file) supplied by the device manufacturer.  The file describes the board's characteristics and the system resources it requires. |
| Configuration registers | The configuration registers on PCI boards contain the same type of information that an EISA .CFG file does.  The SCU is PCI aware, and it complies with the EISA Specification (version 3.12). |
| Your option selections | The SCU stores your information by modifying ISA CMOS and EISA nonvolatile RAM (NVRAM).  It stores most of the values in the battery-maintained memory of the real-time clock (RTC); it stores the rest of the values in flash memory. |

### 3.4.3  Checking the Configuration at Power-on

At power-on or rebooting, the BIOS POST routines and the Plug-N-Play Auto Configuration Manager check and configure the hardware.  POST checks the values that have been stored against the actual hardware configuration; if the values do not agree, you will get an error message.  You must then run the SCU to correct the configuration before the system boots.

### 3.4.4  How to Use the SCU

First make a bootable diskette, and copy the file HIMEM.SYS onto it.

1. Turn on your video display monitor and system.

2. There are three ways to start and run the SCU:

   - From diskette:  insert the System Configuration Disk in drive A, and then press the reset button or type <Ctrl+Alt+Del> to reboot the system.

   - From a DOS directory that you have copied onto your hard drive, type SCU.  Press <Enter>.  If you use this method, you need to load HIMEM.SYS into the AUTOEXEC.BAT and CONFIG.SYS files.

   - From diskette in drive A:  change to drive A and type SCU at the MS-DOS prompt. Press <Enter>.

   Whether or not you can use the second and third methods depends upon how much conventional memory is available in the system when the SCU is run.  The amount of conventional memory available depends on the device drivers that are loaded on the system.

The SCU has four major configuration menus and several sub-menus.   From the main menu, select "Step 1:  About System Configuration" for information about setting up your computer.

| To navigate the screens | Press key | or use mouse |
|---|---|---|
| Change between major menus | ← or → | |
| From main menu, press up or down arrow to highlight an item | ↑ or ↓ | Point to item |
| Select an item | <Enter> | Double-click left button |
| Get help | <F1> | Point to help on toolbar |
| Enter numbers and symbols | numeric keypad keys | |
| To change options | Enter Administrator password if this is enabled | |

⟹ **To run the SCU faster on a DOS-based system**

To run the SCU faster on a DOS-based system, copy to a directory on your hard drive, and run it from there. The SCU may not run properly unless HIMEM.SYS is loaded and there is approximately 600 KB of conventional system memory available.

### 3.4.5   Configuring the System

There are six steps to configure your system. These steps are accessed from the main menu:

- Step 1: About System Configuration
- Step 2: Add and Remove Boards
- Step 3: Change Configuration Settings
- Step 4: Save Configuration
- Step 5: View Switch/Jumper Settings
- Step 6: Exit

The SCU has three major menus and multiple sub-menus. Follow the screen prompts to move between the major menus, display sub-menus, and make selections.

### 3.4.5.1   About System Configuration

This step provides basic information for configuring expansion devices. More experienced users can skip this step.

### 3.4.5.2 Add and Remove Boards

Use this step to add, delete, or move boards.  Most boards are automatically detected and added by the SCU once you enter this step.  However, if the SCU did not detect a board, you can add a board manually.

```
┌───────────────────  Add and Remove Boards  ───────────────────┐
│                                                               │
│   ┌───────────────────────────────────────────────────────┐  │
│   │  System Board                          System Board    │  │
│   │  PCI Undefined Device                  Bus 0  Dev F    │  │
│   │  PCI SCSI Device                       Bus 1  Dev C    │  │
│   │  PCI SCSI Device                       Bus 1  Dev B    │  │
│   └───────────────────────────────────────────────────────┘  │
│                                                               │
│    - Press INSERT to add a board that was not detected        │
│      or has not been installed yet.                           │
│                                                               │
│    - Press DEL to remove the selected board.                  │
│                                                               │
│    - Press F7 to move the selected board to a different slot. │
│                                                               │
│    - Press ESC when finished with this setup.                 │
│                                                               │
├───────────────────────────────────────────────────────────────┤
│      [Add = INSERT]   [Remove = DEL]   [Move = F7]   [Done = ESC] │
│              [Help = F1]          [Define ISA = F6]           │
└───────────────────────────────────────────────────────────────┘
```

OM04253

**To add a board:**

1. Press Insert.

2. From the Select the Board to Add dialog box, select the board's .CFG file and press Enter.

**To delete an existing board:**

1. Use the arrow keys to select the board that you want to delete.

2. Press Delete.

3. Confirm that you want to delete the board.

**To move a board from one slot to another:**

1. Use the arrow keys to select the board that you want to move.

2. Press F7.

⇒ **If you add, move, or remove boards**

Manually verify the resource settings of these adapters, and any other adapters that are not locked, before saving your configuration.

**To define an ISA board:**

Press F6 to display the ISA Board Definition dialog box.  Refer to the section below for details.

### 3.4.5.3   Define an ISA Board

To define an ISA board that has no .CFG file, press F6 while viewing the Add and Remove Boards screen.  The ISA Board Definition dialog box will appear.  It is necessary to define a board to prevent other boards in the system from using the same IRQ levels, DMA channels, I/O addresses, or memory addresses as that of the ISA board.

```
                          Add and Remove Boards

     System Board                           System Board
     PCI Undefined Device                   Bus 0  Dev F
     PCI SCSI Device                        Bus 1  Dev C
     PCI SCSI Device                        Bus 1  Dev B

     - Press INSERT to add a board that was not detected
       or has not been installed yet.

     - Press DEL to remove the selected board.

     - Press F7 to move the selected board to a different slot.

     - Press ESC when finished with this setup.

       [Add = INSERT]  [Remove = DEL]  [Move = F7]  [Done = ESC]
                [Help = F1]      [Define ISA = F6]
```

```
                          ISA Board Definition

     Board Name      [                              ]

     Manufacturer    [                              ]

      Board Type                  Board Slot
     ( • ) Video Board           ( • ) 16-Bit
     (   ) Multifunction Board   (   ) 8-Bit
     (   ) Mass Storage Device   (   ) 8 or 16-Bit


      DMA        IRQ        Ports       Memory
       –          –           –           –
       –          –           –           –
       –          –           –           –
       –          –           –           –
       –          –           –           –


     [Save = F10]   [Load = F9]   [New = F2]   [Delete = F4]
                        [Quit = ESC]
```

OM04254

**To define an ISA board:**

1.   In the Board Name box, type a description of the board.

2.   In the Manufacturer box, type the name of the board manufacturer.

3.   From the Board Type box, choose the type of board.

4.   From the Board Slot box, choose the type of slot.

5.   In the DMA box, define up to four DMA channels.

6.   In the IRQ box, define up to seven IRQ levels.

7.   In the Ports box, define up to eight ranges of I/O ports.

8.   In the Memory box, define up to eight memory address ranges.

9.   Press F10 to save the ISA board definition.

You can load an existing ISA board in order to modify the board definition.

**To load an existing ISA board:** Press F9.

**To delete an ISA board:** Press F9, and confirm that you intend to delete the ISA definition.

### 3.4.5.4  Change Configuration Settings

Use this step to view or change the configuration settings for any board in the system. You can verify that the baseboard and adapter board resources are set properly.

```
┌─────────── Change Configuration Settings ───────────┐
│                                                      │
│  ┌────────────────────────────────────────────────┐ │
│  │  System Board                    System Board   │ │
│  │  PCI Undefined Device            Bus 0  Dev F   │ │
│  │  PCI SCSI Device                 Bus 1  Dev C   │ │
│  │  PCI SCSI Device                 Bus 1  Dev B   │ │
│  └────────────────────────────────────────────────┘ │
│                                                      │
│   - This step is optional, you may skip it by        │
│     pressing ESC and all configuration settings      │
│     will remain unchanged.                           │
│                                                      │
│   - Press ENTER to view or change a board's          │
│     configuration settings.                          │
│                                                      │
│   - Press ESC when you are satisfied with the        │
│     current settings.                                │
│                                                      │
├──────────────────────────────────────────────────────┤
│    [Select = ENTER]   [Done = ESC]   [Advanced Options = F9] │
│              [Help = F1]          [Lock Toggle = F8] │
└──────────────────────────────────────────────────────┘
```

OM04256

**To view or change the settings for a board:**

1. Use the arrow keys to select the board.

2. Press Enter.

3. When you are satisfied with the current settings, press ESC to return to the Main Menu.

### 3.4.5.5  Advanced Options

The Advanced Options menu is intended for advanced users.  These are the options available:

| Use this option | To see this |
|---|---|
| Global resource map | A list of allocated resources (DMA, IRQ, ports, and memory) |
| Board details | Detailed information for individual boards |
| System details | Information on the entire system and the current configuration |
| Physical board ID map | IDs of  boards present in the system |

**To view the Advanced Options menu:** from the Change Configuration Settings dialog box, press F9.

### 3.4.5.6 Save Configuration

This step saves the configuration settings to nonvolatile RAM as well as to a backup file (.CMS file). You must save your settings once they have been configured.

### 3.4.5.7 View Switch/Jumper Settings

Use this step to view manufacturer's instructions about setting dip switches and jumpers, and how to run utilities to ensure correct configuration of each adapter.

```
┌────────────── View Switch/Jumper Settings ──────────────┐
│                                                         │
│     After saving the configuration, it is important that you do │
│     the following steps before using the system:        │
│                                                         │
│     1.  Note the switch and jumper settings and verify that all │
│         switches and jumpers on boards in your system are │
│         set correctly.  Some boards have switches and jumpers │
│         that need to be set manually.                   │
│                                                         │
│     2.  Note the software statements to see if any of the boards │
│         in your configuration need special drivers to be loaded. │
│                                                         │
├─────────────────────────────────────────────────────────┤
│                     [OK = ENTER]                        │
└─────────────────────────────────────────────────────────┘
```

OM04255

This feature is not supported for the AP450GX MP Server baseboard.

### 3.4.5.8 Exit

This step exits to the operating system. If any configuration settings were changed, you will be prompted to restart your system to see the changes.

### 3.4.6 About the Options

Refer to the AP450GX MP Server Installation Guide, Intel Part #642976, for a list of SCU groups as they are displayed on screen after you select System Board from the Change Configuration Settings screen. These are the groups: Systems Group, Peripheral Configuration Group, LCD Display, Management Subsystem, and System Management.

After each group, some of the option choices are described in the AP450GX MP Server Installation Guide. Not all of them are described because (a) a few are not user-selectable but are displayed for your information, and (b) many of the option choices are relatively self-explanatory.

## 3.5 SCSI*Select* Utility

The SCSI*Select* utility detects the number of SCSI AIC-78xx host adapters in your system. Use the utility to start, format, and verify SCSI drives or to explicitly configure the SCSI host adapter to settings other than defaults.

The utility is menu-driven.  Follow the screen prompts and information about moving around through the menus and selecting options. Refer to the AP450GX MP Server Installation Guide, Intel Part #642976, for more details on the SCSI*Select* utility.

# 4  Error Messages and Beep Codes

## 4.1  BIOS Beep Codes

**Table 4.1 Beep Codes**

| Beep Count | Port 80 Codes | Error Condition |
|---|---|---|
| 1 | 71h | Refresh failure |
| 2 | 72h | Parity cannot be reset |
| 3 | 73h | First 64 KB memory failure |
| 4 | 74h | Timer not operational |
| 5 | 75h | Processor failure |
| 6 | 76h | 8042 Gate A20 is off (v_mode) |
| 7 | 77h | Exception interrupt error |
| 8 | 78h | Display memory R/W error |
| 9 | 79h | ROM checksum error |
| 10 | 7Ah | Shutdown reg. R/W error |
| 11 | 7Bh | $I^2C$ Error |

## 4.2  POST Codes and Countdown Codes

At power-on, after the video adapter has been initialized, the BIOS indicates the current testing phase by sending a 2-digit hex code to I/O location 80h. The current countdown code will be displayed on the LCD panel, once the panel is initialized.

## 4.2.1   Recovery Port-80 Codes and Countdown Codes Displayed

During BIOS recovery, the diskette in drive A is booted, and a BIOS image is automatically installed.

**Table 4.2 Recovery Port-80 Codes**

| Port 80 Code | Countdown Code | Reason |
|---|---|---|
| 02h | | Disable internal cache |
| 08h | | Disable DMA controller #1, #2, disable interrupt controller #1, #2, reset video display |
| 13h | | Initialize all chip set registers (Enable LCD display here) |
| 15h | 900 | Initialize system timer |
| 1Bh | 800 | Real mode base 64 KB test |
| 20h | 700 | 16 KB base RAM test |
| 23h | 650 | Setup interrupt vectors |
| 40h | 600 | Test memory in virtual mode |
| 65h | 500 | Initialize 8237 DMA controller |
| 67h | 400 | 8259 interrupt controller test |
| 80h | 300 | Unmask diskette, keyboard and timer interrupts |
| 88h | 200 | Floppy unit initialization |
| A0h | 100 | Cache enable |
| 00h | 000 | Boot OS |

## 4.2.2   Standard Port-80 Codes and Countdown Codes Displayed

**Table 4.3 Standard Port-80 Codes**

| Port 80 Code | Countdown Code | Reason |
| --- | --- | --- |
| D0h | | Early MP Initialization |
| D1h | | Power On Initialization |
| D2h | | Disable NMI |
| D3h | | Reset video controller |
| D4h | | Enter real mode |
| D5h | | Checksum the 8 KB loader BIOS |
| D6h | | Loader BIOS checksum good |
| D7h | 900 | Check if Keyboard Controller (KBC) buffers are free |
| D8h | | Issue BAT (basic assurance test) command to KBC |
| D9h | | Read BAT results |
| DAh | | Check if keyboard controller passed BAT |
| DBh | 820 | Keyboard Initialization Passed |
| DDh | | Disable keyboard and auxiliary devices |
| DFh | | Disable both DMA controllers |
| E0h | 780 | Preliminary initialization of PICs |
| E1h | | Enter real big mode and initialize chip set, size memory |
| E2h | | Initialize timer 2 for speaker |
| E3h | 760 | Initialize timer channel 0 for system timer |
| E4h | | Clear any pending parity errors |
| E6h | 740 | Test RAM from 0-640 KB |
| E7h | | Test and initialize 2 MB memory |
| E8h | | RAM failure, remap memory partitions and test again |

| Port 80 Code | Countdown Code | Reason |
| --- | --- | --- |
| E9h | | RAM test complete, passed.  Clear parity errors |
| EAh | 730 | Set up stack at 30:100, enable cache and shadow BIOS |
| EBh | | Initialize code dispatcher |
| ECh | | Make F000h DRAM R/W Enabled |
| EDh | | Dispatch POST |
| 23h | 700 | Initializations before setting up vector table |
| 24h | | Setup interrupt vector table |
| 0Dh | | Check CMOS clear jumper |
| 0Eh | 690 | Check validity of CMOS |
| 0Fh | | Force CMOS defaults if required |
| 10h | | CMOS initialization complete |
| 25h | | Nothing |
| 28h | | Set monochrome mode |
| 29h | | Set color display |
| 2ah | | Clear parity status if any, initialize warm reset flag |
| 2bh | | Video autoconfiguration and initialization |
| F0h | | EISA Slot Initialization |
| F1h | | Enable extended NMI sources |
| F2h | | Test extended NMI sources |
| 2ch | 580 | Conventional video option ROM search |
| 2dh | | Scan user flash |
| 2eh | 570 | Initialize monochrome display if no other video present |
| 2fh | 560 | Test buffer memory for monochrome |
| 30h | | Check vertical and horizontal retrace |

| Port 80 Code | Countdown Code | Reason |
|---|---|---|
| 31h | | Test for color display memory if no external video BIOS found |
| 32h | | Check vertical retrace |
| 34h | | Sign on message |
| 36h | | Initialize Messaging Services and clear screen |
| 37h | 500 | Custom sign on display |
| 80h | 370 | Keyboard/mouse port check |
| 81h | | Keyboard controller initialization and testing |
| 83h | | Check if keyboard is locked |
| F5h | 330 | Initialize mouse |
| 39h | | Keyboard, mouse and other signons |
| 3bh | | Prepare for memory test |
| 43h | 290 | Decide memory size from chip set |
| 4Fh | | Disable cache, test memory and display memory size on screen |
| 52h | | Initialize for the other processors in MP system, reset DMA controller |
| 61h | 250 | DMA register tests |
| 62h | | DMA test OK |
| 65h | | Initialize 8237 DMA controller |
| 66h | | Clear DMA write request register and mask set/reset register |
| 67h | 220 | 8259 Interrupt controller test |
| F4h | | Enable extended NMI sources |
| 8Ch | 140 | Initialize remaining Plug-N-Play devices (i.e., other than video), initialize IPL, initialize IDE controller |

Continued

| Port 80 Code | Countdown Code | Reason |
|---|---|---|
| 8Fh | 130 | Floppy Initialization |
| 92h | | Set printer, RS-232 time-out |
| 96h | | Optional ROM scan and initialize above C800h |
| 97h | 080 | Scan User flash and conventional option ROM scan |
| 98h | | Scan User flash area |
| 9Ah | | Clear soft reset flag, complete MP Table |
| 9Dh | 070 | Timer data area initialization |
| A0h | | Printer setup |
| A1h | | RS-232 setup |
| A2h | | Check for stuck key |
| ABh | | Before NPX test and initialization |
| ACh | 060 | NPX test and initialization |
| ADh | | Update coprocessor information in CMOS and recalculate checksum |
| Aeh | | Set typematic rate |
| AFh | 050 | Keyboard read ID command |
| B0h | | Wait for READ ID response |
| A3h | | Display POST errors |
| A6h | | Before Setup |
| A7h | 030 | Call Setup if required, prompt for password if enabled |
| B1h | | Enable Cache for boot |
| B3h | | Setup display mode set |
| B4H | | Jump to pre-OS code |
| BBh | 020 | Initialize SMI code, prepare for boot |
| 00h | 000 | Execute BOOT |

## 4.3  POST Error Codes and Messages

The BIOS indicates errors as follows:

- By writing an error code to the PS/2-standard logging area in the Extended BIOS Data Area.

- By displaying a POST Error Code and message on the screen.

**Table 4.4 POST Error Codes**

| Number | Error message |
|--------|---------------|
| 0002 | Primary Boot Device Not Found |
| 0010 | Cache Memory Failure, Do Not Enable Cache |
| 0015 | Primary Output Device Not Found |
| 0016 | Primary Input Device Not Found |
| 0041 | EISA ID Mismatch for Slot |
| 0042 | ISA Config contains invalid info |
| 0043 | EISA Invalid Configuration for Slot |
| 0044 | EISA config NOT ASSURED! |
| 0045 | EISA Expansion Board Not Ready in Slot |
| 0047 | EISA CMOS Configuration Not Set |
| 0048 | EISA CMOS Checksum Failure |
| 0049 | EISA NVRAM Invalid |
| 0050 | PnP Memory Conflict |
| 0051 | PnP 32 bit Memory Conflict |
| 0052 | PnP IRQ Conflict |
| 0053 | PnP DMA Conflict |
| 0054 | PnP Error Log is Full |
| 0055 | Bad PnP Serial ID Checksum |
| 0056 | Bad PnP Resource Data Checksum |
| 0060 | Keyboard Is Locked ... Please Unlock It |
| 0070 | CMOS Time & Date Not Set |
| 0080 | Option ROM has bad checksum |
| 0081 | Custom Binary Checksum Failure |
| 0083 | Shadow of PCI ROM Failed |
| 0084 | Shadow of EISA ROM Failed |

| Number | Error message | (continued) |
|--------|---------------|-------------|
| 0085 | Shadow of ISA ROM Failed | |
| 0131 | Floppy Drive A: | |
| 0132 | Floppy Drive B: | |
| 0135 | Floppy Disk Controller Failure | |
| 0140 | Shadow of System BIOS Failed | |
| 0162 | Unable to apply BIOS Update for Slot 1 Processor #1 | |
| 0163 | Unable to apply BIOS Update for Slot 1 Processor #2 | |
| 0164 | Unable to apply BIOS Update for Slot 2 Processor #1 | |
| 0165 | Unable to apply BIOS Update for Slot 2 Processor #2 | |
| 0166 | BIOS does not support current stepping of Slot 1 Processor #1 | |
| 0167 | BIOS does not support current stepping of Slot 1 Processor #2 | |
| 0168 | BIOS does not support current stepping of Slot 2 Processor #1 | |
| 0169 | BIOS does not support current stepping of Slot 2 Processor #2 | |
| 0170 | Disable CPU slot # | |
| 0171 | CPU Failure - Slot 1, CPU #  1 | |
| 0172 | CPU Failure - Slot 1, CPU #  2 | |
| 0173 | CPU Failure - Slot 2, CPU #  1 | |
| 0174 | CPU Failure - Slot 2, CPU #  2 | |
| 0175 | CPU modules are incompatible | |
| 0176 | Previous CPU Failure - Slot 1, CPU #  1 | |
| 0177 | Previous CPU Failure - Slot 1, CPU #  2 | |
| 0178 | Previous CPU Failure - Slot 2, CPU #  1 | |
| 0179 | Previous CPU Failure - Slot 2, CPU #  2 | |
| 0180 | Attempting to boot with failed CPU | |
| 0181 | BSP switched, system may not be in uniprocessor mode | |
| 0191 | CMOS Battery Failed | |
| 0195 | CMOS System Options Not Set | |
| 0198 | CMOS Checksum Invalid | |
| 0200 | Invalid voltage jumper for processor in Slot 1 Processor #1 | |
| 0201 | Invalid voltage jumper for processor in Slot 1 Processor #2 | |
| 0202 | Invalid voltage jumper for processor in Slot 2 Processor #1 | |
| **Number** | **Error message** | **(continued)** |

| 0203 | Invalid voltage jumper for processor in Slot 2 Processor #2 |
| 0204 | CPU Removed - Slot 1, CPU #1 |
| 0205 | CPU Removed - Slot 1, CPU #2 |
| 0206 | CPU Removed - Slot 2, CPU #1 |
| 0207 | CPU Removed - Slot 2, CPU #2 |
| 0208 | CPU not responding - Slot Slot 1, CPU #1 |
| 0209 | CPU not responding - Slot Slot 1, CPU #2 |
| 0210 | CPU not responding - Slot Slot 2, CPU #1 |
| 0211 | CPU not responding - Slot Slot 2, CPU #2 |
| 0220 | Fan Failure Slot 1 Processor #1 |
| 0221 | Fan Failure Slot 1 Processor #2 |
| 0222 | Fan Failure Slot 2 Processor #1 |
| 0223 | Fan Failure Slot 2 Processor #2 |
| 0230 | Invalid processor for module in Slot 1 Processor #1 |
| 0231 | Invalid processor for module in Slot 1 Processor #2 |
| 0232 | Invalid processor for module in Slot 2 Processor #1 |
| 0233 | Invalid processor for module in Slot 2 Processor #2 |
| 0289 | System Memory Size Mismatch |
| 0295 | Address Line Short Detected |
| 0297 | Memory Size Decreased |
| 0299 | ECC Error Correction failure |
| 0301 | ECC Single bit correction failed, Correction Disabled |
| 0302 | ECC Double bit Error |
| 0303 | ECC SIMMs incompatible |
| 0304 | Invalid memory configuration.  Caused by either memory failures during POST or invalid combination of SIMM sizes. |
| 0305 | PCI-to-PCI bridge found, IO Queue Depth set to 1, setup value overriden |
| 0309 | ECC Memory Failure |
| 0310 | ECC Memory Size Changed, Bank #1  (2GB memory module) |
| 0311 | ECC Memory Size Changed, Bank #2  (2GB memory module) |
| 0312 | ECC Memory Size Changed, Bank #3  (2GB memory module) |
| **Number** | **Error message**                             **(continued)** |

| 0313 | ECC Memory Size Changed, Bank #4  (2GB memory module) |
| 0314 | ECC Memory Size Changed, Bank #0  (4GB memory module) |
| 0315 | ECC Memory Size Changed, Bank #1  (4GB memory module) |
| 0316 | ECC Memory Size Changed, Bank #2  (4GB memory module) |
| 0317 | ECC Memory Size Changed, Bank #3  (4GB memory module) |
| 0320 | Adding/removing PCI adapters has changed available memory. |
| 0322 | An error has caused the memory resizing to fail, insufficient memory to continue. |
| 0370 | Keyboard Controller Error |
| 0373 | Keyboard Stuck Key Detected |
| 0375 | Keyboard and Mouse Swapped |
| 0380 | ECC SIMM failure, Board in slot 1 SIMM # |
| 0392 | ECC SIMM failure, Board in slot 2 SIMM # |
| 0430 | Timer Channel 2 Failure |
| 0440 | Gate-A20 Failure |
| 0441 | Unexpected Interrupt in Protected Mode |
| 0445 | Master Interrupt Controller Error |
| 0446 | Slave Interrupt Controller Error |
| 0450 | Master DMA Controller Error |
| 0451 | Slave DMA Controller Error |
| 0452 | DMA Controller Error |
| 0460 | Fail-safe Timer NMI Failure |
| 0461 | Software Port NMI Failure |
| 0465 | Bus Time-out NMI in Slot |
| 0467 | Expansion Board NMI in Slot |
| 0510 | PCI Parity Error |
| 0511 | PCI System Error |
| 0710 | System Board Device Resource Conflict |
| 0711 | Static Device Resource Conflict |
| 0780 | PCI Segment 1 memory request exceeds 998Mb |
| 0781 | PCI Segment 1 I/O requests exceeds 12K |
| 0782 | PCI I/O request exceeds amount available |
| **Number** | **Error message**                    **(continued)** |

| 0783 | PCI memory request exceeds amount available |
| 0784 | Illegal bus for memory request below 1Mb |
| 0785 | Memory request below 1Mb exceeds 1Mb |
| 0800 | PCI I/O Port Conflict |
| 0801 | PCI Memory Conflict |
| 0802 | PCI IRQ Conflict |
| 0803 | PCI Error Log is Full |
| 0804 | PCI ROM not found, May Be OK For This Card |
| 0805 | Insufficient Memory to Shadow PCI ROM |
| 0806 | Memory Allocation Failure for Second PCI Segment |
| 0809 | PCI Error Log is Full |
| 0810 | Floppy Disk Controller Resource Conflict |
| 0811 | Primary IDE Controller Resource Conflict |
| 0812 | Secondary IDE Controller Resource Conflict |
| 0815 | Parallel Port Resource Conflict |
| 0816 | Serial Port 1 Resource Conflict |
| 0817 | Serial Port 2 Resource Conflict |
| 0900 | NVRAM Checksum Error, NVRAM Cleared |
| 0903 | NVRAM Data Invalid, NVRAM Cleared |
| 0905 | NVRAM Cleared By Jumper |
| 0906 | Password Cleared By Jumper |
| 0982 | I/O Expansion Board NMI in Slot |
| 0984 | Expansion Board Disabled in Slot |
| 0985 | Fail-safe Timer NMI |
| 0986 | System Reset caused by Watchdog Timer |
| 0987 | Bus Time-out NMI in Slot |

# 5  Electrical, Environmental and Mechanical Specifications

This chapter specifies the operational parameters and physical characteristics for the processor, memory, and termination modules and the baseboard.  This is a board-level specification only.  System specifications are beyond the scope of this document.

## 5.1  Absolute Maximum Ratings

Operation at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only).  Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

**Table 5.1 Absolute Maximum Board Level Ratings**

| | |
|---|---|
| Operating temperature for board set | 0°C to +55°C |
| | Note:  Chassis design must meet the Pentium® Pro processor maximum case temperature as specified in the *Pentium Pro Electrical Mechanical and Thermal Specification.* |
| Storage temperature | -55°C to +150°C |
| Voltage on any signal with respect to VSS | -0.3 to supply voltage + 0.3 V |
| Supply voltage with respect to VSS | -0.3 to +5.5 V (VCC only) |

Further topics in this chapter specify normal operating conditions.

## 5.2  Electrical Specifications

Below is a summary of the power requirements for the AP450GX MP Server Board Set.

**Table 5.2 Voltage and Current Specifications**

| Voltage | Specification | Min Current | Max Current | Max di/dt | Suggested Bulk Capacitance (in power supply) | Notes |
|---|---|---|---|---|---|---|
| +3.3V | 3.3V ± 5% | --- | 28A | 14A/300uS | 80,000uF | 1,2,3,4,5 |
| +5V | 5.0V ± 5% | --- | 40A | 14A/300uS | 80,000uF | 1,2,3,5 |
| +12V | 12.0V ± 5% | --- | 18.5A | 0.2A/uS | 10,000uF | 1,2,5 |
| -5V | -5.0V ± 5% | --- | 0.25A | --- | --- | 1,2 |
| -12V | -12.0V ± 10% | --- | 1A | --- | --- | 1,2 |

**Notes:**

1. All values are specified at the power supply connector on the baseboard.
2. di/dt is the maximum rate of change of current the power supply must be able to supply to the board set while keeping the voltage within tolerance.
3. Bulk Capacitance is a suggestion only.  The system integrator is looked upon to make the appropriate determination.
4. Max values for +3.3V will  only be achieve if the 4GB Memory Module is installed, which uses 3.3V DIMMs.
5. Remote sense capabilities should be used to ensure proper regulation

**Table 5.3 Voltage Sequencing Specifications**

| Parameter | Description | Specification | Notes |
|---|---|---|---|
| $T_{rise}$ | Voltage Rise Time | 100 mS | 1 |
| $T_{fall}$ | Voltage Fall Time | None | 2 |
| $T_{sequence-on}$ | Voltage Sequencing During Power On | None | 3 |
| $T_{sequence-off}$ | Voltage Sequencing | None | 3 |

| | | | |
|---|---|---|---|
| | During Power Off | | |
| PwrGood | PowerGood Assertion | Min = 100mS | 4 |
| | | Max = 1500mS | |
| $T_{powerGood Rise}$ | PowerGood Rise Time | 0.5V/ns | Typical value |

**Notes:**
1. Voltage rise time is the time it takes for all voltages input to the baseboard (+3.3V, +5V, +12V, -5V, -12V) to be within their specified value as noted in Table 5.2. This time is measured from the time the voltages begin their rise from ground (0 Volts).
2. Voltage fall time is the time it takes for all voltages input to the baseboard to drop to 0V from the time the power supply is turned off.
3. There are no voltage sequencing requirements during power on or power off. All voltages can come up in any order, but they all must be within their specified value within 50mS as defined by $T_{rise}$.
4. PwrGood must be asserted no sooner that 100mS, but not longer than 1500mS after all voltages are within their specified values as defined by $T_{rise}$ (the rise time of Power Good).

# 5.3 Environmental

**Table 5.4 Board Set Environmental Specifications**

| Environmental Condition | | Specification |
|---|---|---|
| Temperature | nonoperating | -40° to 70°C (-40° to 158°F) |
| | operating | 0° to 55°C ( to 131°F) |
| Temperature, thermal map | | Must not exceed maximum IC junction temperature as specified in the component data sheets. |
| Thermal shock | nonoperating | -40° to 70°C (-40° to 158°F) |
| Humidity | nonoperating | 92% relative humidity (noncondensing) at 55°C (131°F) |
| | operating | 85% relative humidity (noncondensing) at 55°C (131°F) |
| Vibration | nonoperating | Random input, 0.01 g2/Hz at 5 Hz, sloping to 0.02 g2/Hz at 20 Hz, and maintaining 0.02 g2/Hz from 20 Hz to 500 Hz. |
| Shock | nonoperating | 50 g, 11 ms, 1/2 sine |
| | operating | Not applicable |
| Altitude | nonoperating | To 50,000 ft (15,240 m) |
| | operating | To 10,000 ft (3,048 m) |
| Electrostatic discharge (ESD) | operating | Tested to 25 kV; no component damage |
| EMI | operating | Tested as part of system; required to meet EMI emission requirements |

# 5.4 Cooling Requirements

Below are the cooling requirements for the board set, specifically the processors. The first table specifies cooling requirements for the primary processor module. The second table is for the secondary processor module. Both tables assume both processor sockets on each module are populated. Ambient temperature is measured just before it passes over the processor module.

**Table 5.5 Primary Processor Module Cooling Requirements**

| 30W Processor | | 35W Processor | | 40W Processor | |
|---|---|---|---|---|---|
| Air Flow (LFM) | Max Ambient Temp (°C) | Air Flow (LFM) | Max Ambient Temp (°C) | Air Flow (LFM) | Max Ambient Temp (°C) |
| 100 | 30.7 | 100 | 20.3 | 100 | 16.3 |
| 200 | 42.9 | 200 | 33.7 | 200 | 29.9 |
| 300 | 51.2 | 300 | 44.2 | 300 | 39.6 |
| 400 | 56.2 | 400 | 50.8 | 400 | 46.7 |
| 500 | 59.6 | 500 | 55 | 500 | 50.4 |

**Table 5.6 Secondary Processor Module Cooling Requirements**

| 30W Processor | | 35W Processor | | 40W Processor | |
|---|---|---|---|---|---|
| Air Flow (LFM) | Max Ambient Temp (°C) | Air Flow (LFM) | Max Ambient Temp (°C) | Air Flow (LFM) | Max Ambient Temp (°C) |
| 100 | 28.3 | 100 | 24.3 | 100 | 17.3 |
| 200 | 41.5 | 200 | 37.5 | 200 | 29.9 |
| 300 | 49.3 | 300 | 46.1 | 300 | 40.6 |
| 400 | 55.6 | 400 | 51.6 | 400 | 46.8 |
| 500 | 59.2 | 500 | 55.2 | 500 | 50.9 |

## 5.5  Power Budget

All power for the Pentium Pro processors on the processor module is provided by DC-DC converters powered from the +12V supply.  There is also a DC-DC converter used for the GTL+ termination voltage reference.  The efficiency of the converters is 80%.

$I^2C$ components are powered from +5 volts.

All power numbers are given for worst case conditions, not nominal.  See the *Pentium Pro Processor Data Sheet* for details of Pentium Pro processor power requirements.

Voltage tolerance is $\pm$ 5%.

The numbers below are for the baseboard, processor, and memory modules.  The system integrator is looked upon to make cost / performance / market tradeoffs to determine how much power to dedicate for add-in slots.

**Table 5.7 Example Power Budget in Watts (Maximum Values)**

|  | -12V | +12V | +3.3V | +5V |
|---|---|---|---|---|
| **Processor Module** | 0 | 99.2 | 0.2* | 1.4 |
| **Termination Module** | 0 | 10.9 | 0 | 0.9 |
| **Memory Module (1GB)** | 0 | 0 | 3.9 | 75.3 |
| **Baseboard (no add-in cards)** | 1.2 | 1.2 | 7.0 | 10.0 |
| **Total Watts** | | 300.2 | | |

**Assumptions:**

**two processor modules, four 35W processors (166/512KB), 1GB of memory,  no add-in cards**

\* The Pentium® Pro processor pinout also specifies power at +3.3V.  These numbers assume the Pentium Pro processor does not use that voltage.  Refer to the *Pentium Pro Processor Data Sheet* for details.

## 5.6  Mechanical Drawings

The following diagrams show the mechanical specifications of the baseboard, processor module, termination module, and memory module.  All dimensions are given in inches, as per ANSI Y15.4M.  Maximum primary-side component height is .550" unless otherwise noted.  Connectors are dimensioned to pin 1.  Refer to "Connector Specifications" after the diagrams for more information.

### 5.6.1  Processor and Terminator Module Mechanical Specifications
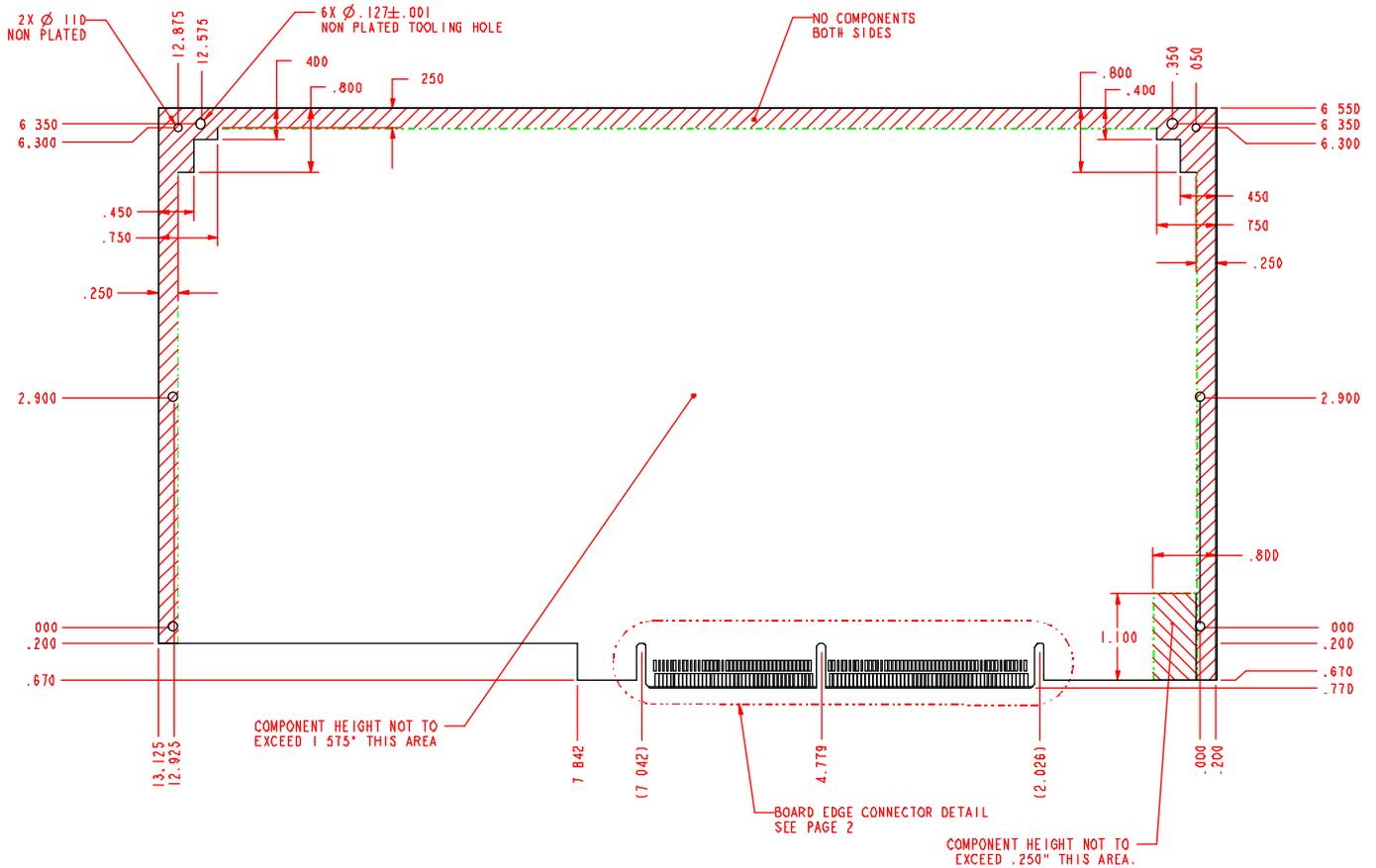


**Figure 5.1 Processor and Terminator Module Mechanical Specifications**

## 5.6.2    Memory Module Mechanical Specifications

**Figure 5.2 Memory Module Mechanical Specifications**

## 5.6.3 Baseboard Mechanical Specifications
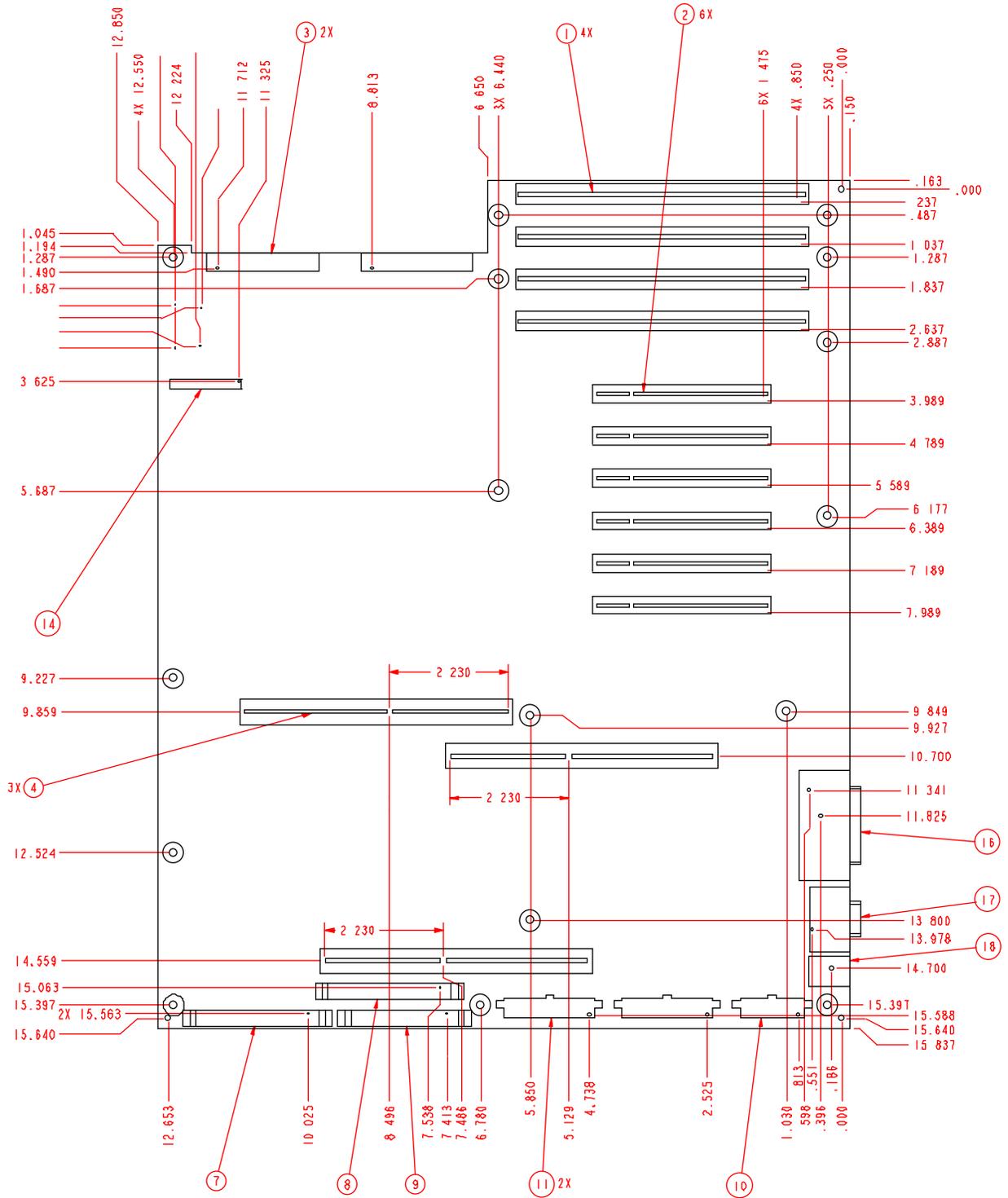


**Figure 5.3 Baseboard Mechanical Specifications**

## 5.6.4   Module Insertion/Extractor Handle Specifications

The card ejection lever shown below is a requirement for the processor and memory modules in the Pentium Pro processor server system.  The cards must be seated into the baseboard connector at no more than a 5° deviation from perpendicular to avoid damage to the baseboard.  Using the ejection lever ensures that  these modules are completely seated, and eases the insertion /extraction force needed to correctly remove and install the modules.

In addition to the ejection levers, card guides and a hold down rail are required to keep the cards from moving around and becoming displaced during shipping or handling.
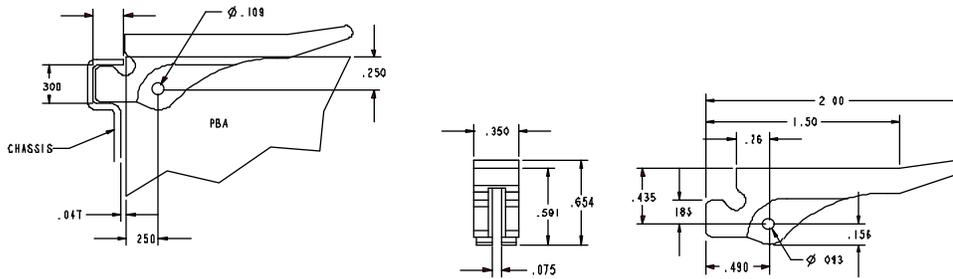
**Figure 5.4 Module Insertion/Extractor Handle**

## 5.7  Connector Specifications

The following table shows reference designators, quantity, and the manufacturer's part numbers for connectors on the baseboard and processor module.  Item numbers reference the circled numbers on the baseboard mechanical drawing.  Refer to manufacturers' documentation for more information.

**Table 5.8  Connector Specifications**

| Item | Ref. Designator(s) | Qty | Mfr(s) and Part # | Description |
|------|--------------------|-----|-------------------|-------------|
| 1 | J1A1, J1A2, J2A1, J2A2 | 4 | Burndy CB2E188SC-13Z14 | EISA bus add-in card connector |
| 2 | J5A2, J5A3, J4A2, J4A1, J3A2, J3A1 | 6 | AMP 646255-1 | PCI add-in card connector |
| 3 | J1F1, J1G1 | 2 | AMP 74931-7 | 68-pin SCSI connector |
| 4 | J6D1, J7D1, J9C1 | 3 | AMP 145264-1 | Processor and memory bus connectors |
| 7 | J9F1 | 1 | 3M 3432-Z00044 | LCD front panel display connector |
| 8 | J9E1 | 1 | 3M 2450-60Y2UB or G | IDE connector |
| 9 | J9E2 | 1 | 3M 2534-60V2UG | Floppy connector |
| 10 | J9A2 | 1 | Molex 39-29-9144 | Power control connector (PS3) |
| 11 | J9D1, J9B1 | 2 | Molex 39-29-9202 | 20-pin power connector (PS1 & PS2) |
| 14 | J3G1 | 1 | Fox Conn/Hon Haj HC11131-KD6 | Server Management feature connector |
| 16 | J7A1 | 1 | AMP 750433-2 | VGA and Parallel port connector |
| 17 | J8A1 | 1 | Fox Conn/Hon Haj DM10156-73 | Dual serial port connector |
| 18 | J9A1 | 1 | Fox Conn/Hon Haj MH11063-D0 | Keyboard and mouse connector |
|  | J5G3, J2G4, J2G3, J5G2, J107, J102 | 6 | AMP640456-3 | System & CPU Fan Connector (3 pin) (J107 & J102 on processor module) |
|  | J2G1, J5G1 | 2 | AMP 640456-4 | Hard Disk LED Connector (4 pin) |

# Appendix A  --  Supported Environments

The AP450GX MP Server has been validated with the leading network operating systems, adapter cards, video DRAM and SIMM/DIMM combinations.  Not all configurations have been validated and there may be limitations to their interoperability.  Contact your Intel representative for the latest interoperability information.

## A.1  Certified Operating Systems

The table below lists the operating system certifications for the AP450GX MP Server System.
- Level 1 - Heavy testing done in Intel's Server Validation Lab
- Level 2 - Minimal testing done in Intel's Compatibility Engineering Lab

| Level | Operating System | Version | Certification Status |
|---|---|---|---|
| 1 | Windows NT | 3.51 & 4.0 | OEM must certify with Microsoft |
| 1 | Novell NetWare | 3.12 & 4.11 | Completed at Novell facility |
| 1 | IBM OS/2 | LANServer 4.0 Advanced | Completed at IBM facility |
| 1 | SCO UnixWare | 2.1 | OEM must certify with SCO |
| 2 | Banyan | 6.0 | Completed at Banyan facility |
| 2 | IBM OS/2 | 3.0 WARP | Completed in Intel's Compatibility Engineering  Lab |
| 2 | SCO UNIX | OpenServer 5.0 & 5.0MPX | OEM must certify W/SCO |
| 2 | Solaris | 2.5 | Completed in Intel's Compatibility Engineering Lab |

## A.2  Tested Adapter Cards

Contact your Intel representative for an updated list of adapter cards that have been tested with the AP450GX MP Server System.

## A.3  Qualified SIMM/DIMMs

Only use SIMMs and DIMMs approved for use in this system. Contact your Intel representative for an updated list of qualified SIMMs and DIMMs.

## A.4  Qualified Video DRAM

Only use video DRAM approved for use in this system. Contact your Intel representative for an updated list of qualified Video DRAM.

# Appendix B  --  Product Codes

Contact your Intel representative for the current product codes, availability, and pricing.

# Appendix C -- Connector Pinouts

Below is the pinout for each connector on the AP450GX MP Server Board Set.

## C.1 Power Connectors PS1 and PS2, Baseboard

The baseboard receives power at PS1 and PS2 from connectors J6 and J7 on the power distribution board.  PS1 and PS2 are identical; J6 and J7 are identical.

Table C.1 Power Connectors

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | +5 VDC | 11 | +12 VDC |
| 2 | GND | 12 | GND |
| 3 | +5 VDC | 13 | +12 VDC |
| 4 | GND | 14 | GND |
| 5 | +5 VDC | 15 | +3.3 VDC |
| 6 | GND | 16 | GND |
| 7 | +5 VDC | 17 | +3.3 VDC |
| 8 | GND | 18 | GND |
| 9 | +5 VDC | 19 | +3.3 VDC |
| 10 | GND | 20 | GND |

## C.2 Power Status/Control Signal Connector PS3, Baseboard

The baseboard receives power status and control signals at PS3 from connector J11 on the power distribution board.

**Table C.2 Power Status/Control Signal Connector**

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | -12 VDC | 8 | +5 V standby |
| 2 | -5 VDC | 9 | GND |
| 3 | PWR_ON | 10 | PWRGOOD |
| 4 | I$^2$C-SDA (Data) | 11 | GND |
| 5 | I$^2$C-SCL (Clock) | 12 | I$^2$C_PRESENT |
| 6 | +5V remote sense (+) | 13 | +3.3V remote sense (+) |
| 7 | +12V remote sense (+) | 14 | Ground remote sense (-) |

## C.3  Diskette Drive Connector, Baseboard

**Table C.3 Diskette Drive Connector**

| Pin | Signal | Pin | Signal |
| --- | --- | --- | --- |
| 1 | GND | 18 | Head direction |
| 2 | Density select | 19 | GND |
| 3 | GND | 20 | Step |
| 4 | Not connected | 21 | GND |
| 5 | Key (pin missing) | 22 | Write data |
| 6 | Extended density in | 23 | GND |
| 7 | GND | 24 | Write enable |
| 8 | Index | 25 | GND |
| 9 | GND | 26 | Track 0 |
| 10 | Motor A on | 27 | GND |
| 11 | GND | 28 | Write protect |
| 12 | Drive B select | 29 | Extended density out |
| 13 | GND | 30 | Read data |
| 14 | Drive A select | 31 | GND |
| 15 | GND | 32 | Head select side 1 |
| 16 | Motor B on | 33 | High density out |
| 17 | GND | 34 | Disk change |

# C.4 Front Panel Connector, Baseboard

**Table C.4 Front Panel Connector**

| Pin | Signal name | Type | Function |
|-----|-------------|------|----------|
| 1 | SPKRDAT | Out | Drives standard PC-AT speaker |
| 2 | VCC5 | Out | 5 V power supply |
| 3 | 5VSTANDBY | Out | 5 V power supply standby |
| 4 | PS_ON | I/O | Power supply on/off switch connection |
| 5 | FP_RESET # | In | Active-low front panel reset switch connection |
| 6 | GND | | Ground |
| 7 | FP_NMI # | In | Connects to FP_NMI driver |
| 8 | GND | | Ground |
| 9 | HD1_LED_VCC | | Hard Drive #1 LED Activity indicator return |
| 10 | HD1_LED_ACT# | | Hard Drive #1 LED Activity indicator |
| 11 | HD2_LED_ACT# | | Hard Drive #2 LED Activity indicator |
| 12 | HD2_LED_VCC | | Hard Drive #2 LED Activity indicator return |
| 13 | KEYLOCK# | | Keyboard lock signal |
| 14 | GND | | Ground |
| 15 | SECURE | Out | Secure mode indicator |
| 16 | VCC5 | Out | LCD Display controller power |
| 17 | KEY | | Not connected |
| 18 | VCC5 | Out | 5 V power supply |
| 19 | $I^2$C-SDA | I/O | $I^2$C interface data signal |
| 20 | CHASIS_SWT_RET | In | Chassis intrusion detection switch return |
| 21 | LCD_SD | I/O | Serial I/O data to LCD controller |
| 22 | H_PWROFF# | Out | Host power control (from Server Management board) |

Continued

**Front Panel Connector, Baseboard, continued**

| Pin | Signal name | Type | Function |
|-----|-------------|------|----------|
| 23 | LCD_SCLK | Out | Clock for LCD serial I/O |
| 24 | I2C_SCL | I/O | I$^2$C interface clock signal |
| 25 | LCD_PCLK | Out | LCD controller processor clock |
| 26 | GND | | Ground |
| 27 | EN | Out | LCD enable |
| 28 | GND | | Ground |
| 29 | RW | Out | LCD Read/Write strobe |
| 30 | VCC3 | | 3.3 V power supply |
| 31 | RS | Out | LCD reset |
| 32 | PWR# | Out | RTC power control indication |
| 33 | LCD_GND | Out | LCD display ground connection |
| 34 | GND | | Ground |
| 35 | FAN_FAIL# | Out | Indicates failure of at least one cooling fan |
| 36 | GND | | Ground |
| 37 | I2C_PRES | | I$^2$C control signal |
| 38 | RESERVED | | Reserved |
| 39 | Vcc | | Vcc |
| 40 | RESERVED | | Reserved |

- Out: driven by system baseboard. In: driven by front panel.
- # at the end of a signal name indicates an active low signal

## C.5  IDE Drive Connector, Baseboard

**Table C.5 IDE Drive Connector**

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | IDERST# | 2 | GND |
| 3 | ID7 (data bit 7) | 4 | ID8 (data bit 8) |
| 5 | ID6 (data bit 6) | 6 | ID9 (data bit 9) |
| 7 | ID5 (data bit 5) | 8 | ID10 (data bit 10) |
| 9 | ID4 (data bit 4) | 10 | ID11 (data bit 11) |
| 11 | ID3 (data bit 3) | 12 | ID12 (data bit 12) |
| 13 | ID2 (data bit 2) | 14 | ID13 (data bit 13) |
| 15 | ID1 (data bit 1) | 16 | ID14 (data bit 14) |
| 17 | ID0 (data bit 0) | 18 | ID15 (data bit 15) |
| 19 | GND | 20 | Keyed (pin missing) |
| 21 | IDEDRQ (DMA request 3) | 22 | GND |
| 23 | IDEIOW# (I/O write) | 24 | GND |
| 25 | IDEIOR# (I/O read) | 26 | GND |
| 27 | CHRDY (I/O channel ready) | 28 | SPSYNC (address latch enable) |
| 29 | IDEDAK# (DMA acknowledge 3) | 30 | GND |
| 31 | IDEIRQ14 (interrupt request 14) | 32 | IDEIO16 # (I/O channel size 16) |
| 33 | IDESA1 (address bit 1) | 34 | PDIAG # |
| 35 | IDESA0 (address bit 0) | 36 | IDESA2 (address bit 2) |
| 37 | IDECS0# (host chip select 0) | 38 | IDECS1# (host chip select 1) |
| 39 | IDEHDACT#/DRVPRES# disk activity/drive present) | 40 | GND |

## C.6  Fan Connector, Baseboard & Processor Module

**Table C.6 Fan Connectors**

| Pin | Function |
|-----|----------|
| 1 | GND |
| 2 | +12V |
| 3 | Fan fail sensor |

## C.7  Hard Drive LED Connectors, Baseboard

**Table C.7 Hard Drive LED Connectors**

| Pin | Function |
| --- | --- |
| 1 | not connected |
| 2 | HD1_ACTIVE# |
| 3 | HD2_ACTIVE# |
| 4 | not connected |

## C.8  I2C Connector, Baseboard

**Table C.8 I2C Connector**

| Pin | Function |
| --- | --- |
| 1 | I2C_SDA (Data) |
| 2 | GND |
| 3 | I2C_SCL (Clock) |

## C.9  3.3V PCI Power Connector, Baseboard

**Table C.9 +3.3 Volt PCI Power Connector**

| Pin | Function |
| --- | --- |
| 1 | GND |
| 2 | GND |
| 3 | GND |
| 4 | +3.3V PCI |
| 5 | +3.3V PCI |
| 6 | +3.3V PCI |

# C.10 Server Monitor Module Connector, Baseboard

**Table C.10 Server Monitor Module Connector**

| Pin | Signal | Type | Description |
|-----|--------|------|-------------|
| 1 | SMI# | Input | System management interrupt |
| 2 | I2C_CLK | Output | I$^2$C clock (8 MHz) |
| 3 | GND | Power | Ground |
| 4 | Reserved | | No connection |
| 5 | PWROFF# | Output | Power supply off (active low) |
| 6 | I2CDATA | I/O | I$^2$C data signal |
| 7 | LPOK | Input | Host line power okay |
| 8 | KEYUNLK# | Input | Keyboard unlock |
| 9 | NMI | Input | Nonmaskable interrupt |
| 10 | 3.3 V | Input | 3.3 V power |
| 11 | RESET# | Output | Reset system board |
| 12 | GND | Power | Ground |
| 13 | GND | Power | Ground |
| 14 | Reserved | | No connection |
| 15 | SECURE | Input | Host in secure mode |
| 16 | GND | Power | Ground |
| 17 | INTRUD | Input | Chassis is open |
| 18 | Reserved | | No connection (reserved for future use) |
| 19 | Reserved | | No connection |
| 20 | GND | Power | Ground |
| 21 | Reserved | | No connection |
| 22 | Reserved | | No connection |
| 23 | POWERGD | | Power to system is within specification |
| 24 | Reserved | | No connection |
| 25 | Reserved | | No connection, pin missing |
| 26 | Reserved | | No connection |

## C.11  SCSI Channel A and B Connectors, Baseboard
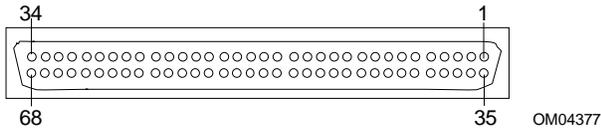


**Table C.11 68-pin Wide SCSI Connector**

| Signal name | Connector contact | SCSI bus conductor | SCSI bus conductor | Connector contact | Signal name |
|---|---|---|---|---|---|
| GND | 1 | 1 | 2 | 35 | DB(12) # |
| GND | 2 | 3 | 4 | 36 | DB(13) # |
| GND | 3 | 5 | 6 | 37 | DB(14) # |
| GND | 4 | 7 | 8 | 38 | DB(15) # |
| GND | 5 | 9 | 10 | 39 | DB(P1) # |
| GND | 6 | 11 | 12 | 40 | DB(0) # |
| GND | 7 | 13 | 14 | 41 | DB(1) # |
| GND | 8 | 15 | 16 | 42 | DB(2) # |
| GND | 9 | 17 | 18 | 43 | DB(3) # |
| GND | 10 | 19 | 20 | 44 | DB(4) # |
| GND | 11 | 21 | 22 | 45 | DB(5) # |
| GND | 12 | 23 | 24 | 46 | DB(6) # |
| GND | 13 | 25 | 26 | 47 | DB(7) # |
| GND | 14 | 27 | 28 | 48 | DB(P) # |
| GND | 15 | 29 | 30 | 49 | GND |
| GND | 16 | 31 | 32 | 50 | GND |
| TERMPWR | 17 | 33 | 34 | 51 | TERMPWR |
| TERMPWR | 18 | 35 | 36 | 52 | TERMPWR |
| Reserved | 19 | 37 | 38 | 53 | Reserved |
| GND | 20 | 39 | 40 | 54 | GND |
| GND | 21 | 41 | 42 | 55 | ATN # |
| GND | 22 | 43 | 44 | 56 | GND |
| GND | 23 | 45 | 46 | 57 | BSY # |
| GND | 24 | 47 | 48 | 58 | ACK # |
| GND | 25 | 49 | 50 | 59 | RST # |
| GND | 26 | 51 | 52 | 60 | MSG # |
| GND | 27 | 53 | 54 | 61 | SEL # |
| GND | 28 | 55 | 56 | 62 | CD # |
| GND | 29 | 57 | 58 | 63 | REQ # |
| GND | 30 | 59 | 60 | 64 | I/O # |
| GND | 31 | 61 | 62 | 65 | DB(8) # |
| GND | 32 | 63 | 64 | 66 | DB(9) # |
| GND | 33 | 65 | 66 | 67 | DB(10) # |
| GND | 34 | 67 | 68 | 68 | DB(11) # |

## C.12  PCI  Connectors, Baseboard

The baseboard PCI connectors adhere to the requirements in the PCI Specification 2.0.

## C.13  VGA Video Port, Baseboard
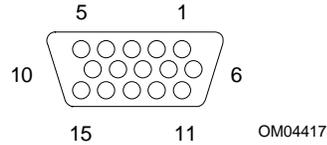


**Table C.12 VGA Video Port**

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | Red | 9 | Not connected |
| 2 | Green | 10 | GND |
| 3 | Blue | 11 | Not connected |
| 4 | Not connected | 12 | Not connected |
| 5 | GND | 13 | HSYNC (horizontal sync) |
| 6 | GND | 14 | VSYNC (vertical sync) |
| 7 | GND | 15 | Not connected |
| 8 | GND | | |

## C.14  Parallel Port Connector, Baseboard
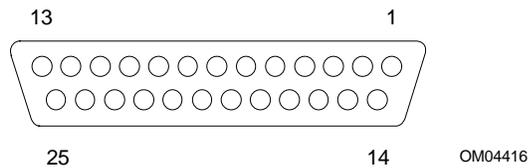


**Table C.13 Parallel Port Connector**

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | Strobe # | 10 | ACK (acknowledge) # |
| 2 | Data bit 0 | 11 | Busy |
| 3 | Data bit 1 | 12 | PE (paper end) |
| 4 | Data bit 2 | 13 | SLCT (select) |
| 5 | Data bit 3 | 14 | AUFDXT (auto feed) # |
| 6 | Data bit 4 | 15 | Error # |
| 7 | Data bit 5 | 16 | INIT (initialize printer) |
| 8 | Data bit 6 | 17 | SLCTIN (select input) # |
| 9 | Data bit 7 | 18–25 | GND |

## C.15  Serial Port Connectors 1 and 2, Baseboard

1    5

6    9    OM04415
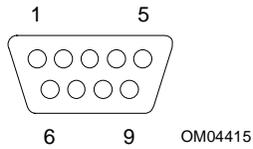
**Table C.14 Serial Port Connectors**

| Pin | Signal |
|-----|--------|
| 1 | DCD (data carrier detect) |
| 2 | RXD (receive data) |
| 3 | TXD (transmit data) |
| 4 | DTR (data terminal ready) |
| 5 | GND |
| 6 | DSR (data set ready) |
| 7 | RTS (request to send) |
| 8 | CTS (clear to send) |
| 9 | RI (ring indicator) |

## C.16  Keyboard and Mouse Connectors, Baseboard

6    5

4    3
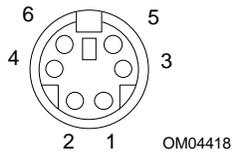
2    1    OM04418    These identical PS/2-compatible connectors share a common housing.

**Table C.15 Keyboard and Mouse Connectors**

| Pin | Keyboard signal | Pin | Mouse signal |
|-----|-----------------|-----|--------------|
| 1 | KEYDAT (keyboard data) | 1 | MSEDAT (mouse data) |
| 2 | Not connected | 2 | Not connected |
| 3 | GND | 3 | GND |
| 4 | FUSED_VCC (+5 V) | 4 | FUSED_VCC (+5 V) |
| 5 | KEYCLK (keyboard clock) | 5 | MSECLK (mouse clock) |
| 6 | Not connected | 6 | Not connected |

# Appendix D - 450GX PCIset Register Changes

**The following register changes have occurred in the 450GX PCIset as a result of going from the B0 stepping to the C0 stepping of the chipset. For a more detailed description of each register change, please refer to the Specification Update for the Intel 450GX PCIset.**

♦ Register 48h, bit 3 - Alias GAT mode sideband request to non-GAT mode

This bit allows the PCEB to be operated in GAT mode (so that EISA tenure is limited) while the OPB operates in nonGAT mode (so that BPRI is deasserted between requests).

♦ Register 48h, bit 4 - Use slow BPRI deassertion

This bit forces serialization of inbound requests. This is necessary in systems where inbound read prefetching can occur to a device that can issue a hard fail response.

♦ Register 48h, bit 5 - Disable Livelock Workaround

If this bit is zero (default), then nonGAT mode is entered for 64 clocks after an outbound request is retried. Setting bit 5 to one disables this new feature.

♦ Register 48h, bit 6 - Disable Outbound Traffic Priority

This bit can be asserted to effectively override the priority normally given to outbound requests. If this bit is zero (default), then nonGAT mode is entered for 64 clocks after an inbound request is retried eight times. Setting bit 6 to one disables this new feature.

♦ Register B0[8] is now reserved

This bit was the AERR input enable bit for the Driven on Reset register. The AERR input is now always on. Register B0[8] must be set to 0 so that no other Pentium Pro processor devices will observe AERR.

♦ Register C0[1] - AERR# to BERR#

This bit was added as another method of reporting AERRs. BERR# can optionally be elevated to BINIT#.

♦ Register C8[31:16] - Pentium Pro processor Retry Counter

This is not a new register, but its optimum value has changed since the B0 stepping. For optimum performance this counter should be left at its default value of 0 (in B0 systems the recommendation was to set it to a small, non-zero value).

♦ Register CC[15:0] - Unused Agent ID

These bits represent the Pentium Pro processor agent IDs that are not in use on the Pentium Pro processor bus. Bits 15 to 0 translate to agent IDs 31 to 16 respectively. A "1" in a bit location means the ID is not used by a Pentium Pro processor bus agent.

# Appendix E -- Errata

This appendix lists the errata which apply to the AP450GX MP Server Board Set. Intel intends to fix some of the errata in the future, and to account for the other outstanding issues through documentation or specification changes as noted. Refer to the *AP450GX MP Server Board Set Specification Update* (Order Number 282963) for additional specification updates concerning the AP450GX MP Server Board Set.

Refer to the *Pentium Pro Processor Specification Update* (Order Number 242689) for specification updates concerning the Pentium Pro processor. Items contained in the *Pentium Pro Processor Specification Update* that either do not apply to the AP450GX MP Server Board Set or have been worked around are noted. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Refer to the *Intel 450KX/GX PCIset Specification Update* (Order Number 243109) for specification updates concerning the Intel 450GX PCIset. Items contained in the *Intel 450KX/GX PCIset Specification Update* that either do not apply to the AP450GX MP Server Board Set or have been worked around are noted. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Certain Pentium Pro processor and Intel 450GX PCIset errata are also included as board set errata. These errata are included here because of their implications and/or significance to the operation of the AP450GX MP Server Board Set. Errata #10, 11, 20, 32, and 33 fall into this category.

## E.1  Summary Table of Changes

The following table indicates the errata which apply to the AP450GX MP Server Board Set. Intel intends to fix some of the errata in the future, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

**Codes Used in Summary Table**

| | |
|---|---|
| Fix: | This erratum is intended to be fixed in a future revision of the hardware or software associated with the AP450GX MP Server Board Set. |
| Fixed: | This erratum has been previously fixed. |
| No Fix: | There are no plans to fix this erratum. |

*Table E-1.  Summary Table of Changes*

| NO. | PLANS | ERRATA |
|---|---|---|
| 1 | Fixed | Board level shock and vibration testing may cause processor module capacitor fatigue |
| 2 | Fixed | IDE CD-ROM as master may cause server hang |
| 3 | NoFix | Flash boot block protect jumper in unprotected mode may cause flash corruption during a warm reset |
| 4 | Fixed | Power distribution board scan via the I²C bus may cause possible incorrect chip set register settings |
| 5 | Fixed | BIOS does not remap bad SIMMs correctly during a system reset |
| 6 | Fixed | The Fab 3.x processor module does not support the 200-MHz Pentium® Pro Processor with 512-Kbyte L2 cache |
| 7 | Fixed | EISA read performance is below expectations |
| 8 | NoFix | Incorrectly inserted memory module may cause baseboard damage |
| 9 | NoFix | If address bit permuting is enabled memory resizing can not be performed |
| 10 | Fixed | BIOS setting IOQ=8 may cause SMM handler to hang the operating system |
| 11 | Fixed | If incompatible SIMMs are installed the system may hang during reset |
| 12 | Fixed | Fan failure causes intrusion switch detection to be disabled |
| 13 | Fixed | BIOS record type 13H indicates incorrect hard drive information |
| 14 | Fixed | Memory resizing error causes BIOS to report wrong memory bank |
| 15 | Fixed | Pentium® Pro processor data bus single bit ECC errors may cause excessive SMI generation |
| 16 | Fixed | Incorrectly entering administrator password may hang SCU 3.40/OVL 1.31 |
| 17 | Fixed | Entering a valid password to exit BIOS "secure mode" leaves keyboard lights enabled |
| 18 | Fixed | Greater than 1.5 GB of memory installed may cause system hang |
| 19 | Fixed | BIOS does not log bad SIMM location during POST memory testing |
| 20 | Fixed | Spurious interrupts may cause virtual wire mode APIC operation to fail |
| 21 | Fixed | The SCU cannot change the state of the PCI system error option |
| 22 | Fixed | The SCU incorrectly sets the baud rates for serial redirection |
| 23 | Fixed | Power and reset security switches in the BIOS setup are not available in the SCU |
| 24 | Fixed | Incorrectly initialized real time clock registers may hang operating system on the tenth of each month |
| 25 | Fixed | BIOS setting IOQ=Autodetect causes BIOS to set IOQ=8 |
| 26 | Fixed | If the system temperature reaches a warning threshold temperature monitoring is disabled |
| 27 | Fixed | Using 60ns 64MB SIMMs and 2-way memory interleave may cause system hang during reset |
| 28 | Fixed | Location of password prompts in POST sequence may cause system security violation |
| 29 | Fixed | Clearing NVRAM (CMOS) and installing an operating system may cause a system hang |
| 30 | Fix | Excessive single-bit ECC errors incorrectly disables single-bit error logging for memory bus and processor data bus |
| 31 | Fixed | Saving BIOS configuration after date change may cause date to be set incorrectly |
| 32 | Fixed | BIOS setting IOQ = 8 may corrupt PCI configuration cycles |
| 33 | Fixed | PCI-to-PCI bridges may cause the system to hang |
| 34 | Fixed | Board set TAP reset circuit may cause incorrect system power on |
| 35 | Fixed | INCA anomaly at power up may cause PCI bus clocks to run at 66MHz on baseboards with the C0 stepping of Intel 450GX PCIset |

### E.2  Errata

### 1.    Board Level Shock and Vibration Testing May Cause Processor Module Capacitor Fatigue

**PROBLEM:** Fatigues and broken leads have occurred on the capacitors of the processor module during board level shock and vibration testing.

**IMPLICATION:** Fatigues and broken leads can occur on the processor module in certain chassis configurations.

**WORKAROUND:** None Identified.

**STATUS:** This erratum was fixed with the Fab 4.2 processor module (PBA# 659506-213).

### 2.    IDE CD-ROM as Master May Cause Server Hang

**PROBLEM:** During a system reboot, if an AP450GX MP Server is configured with an IDE CD-ROM as a master boot device in boot floppy emulation mode, the power on self test (POST) completes but the server will hang if a bootable CD-ROM is in the drive.

**IMPLICATION:** The server may hang while booting from a CD-ROM.

**WORKAROUND:** None Identified.

**STATUS:** This erratum was fixed in BIOS 1.00.07 CD0.

### 3.    Flash Boot Block Protect Jumper in Unprotected Mode May Cause Flash Corruption During a Warm Reset

**PROBLEM:** If the boot block protect jumper is moved from its default location, the flash boot area may be corrupted by a warm reset. If the flash boot block protect jumper is left in the unprotected mode and a warm reset occurs then the data in the flash can be corrupted, including the boot block.

**IMPLICATION:** If the boot block protect jumper is moved from its default location, the flash boot area may be corrupted by a warm reset. Once corrupted, the baseboard would require reprogramming at the factory and thus need to be replaced.

**WORKAROUND:** The boot block protect jumper should only be placed in the unprotected position by Intel BIOS developers (i.e., it is for Intel use only). Do not move this jumper from its default location.

**STATUS:** There are no plans to fix this erratum.

### 4.    Power Distribution Board Scan via the I²C Bus May Cause Possible Incorrect Chip Set Register Settings

**PROBLEM:** The AP450GX MP Server chassis SCSI Backplane periodically scans the power distribution board via the I²C bus. If the BIOS is reading the baseboard ID at the same time this

scan is occurring, then the chip set registers may be set incorrectly by the BIOS as a result of this scan.

**IMPLICATION:** There are a variety of implications for this erratum. The processor speeds may be reported incorrectly. If more than one processor is in the system, the BIOS will write a warning message to the console indicating the CPUs are incompatible. The system will function correctly under these conditions. The memory SIMM speed may be reported incorrectly. 60ns and 70ns SIMM timings are supported. If 60ns SIMMs are given 70ns timings, then silent system performance degradation will result. If 70ns SIMMs are given 60ns timings, then ECC errors may occur and silent data corruption is possible if the user does not monitor the ECC errors with appropriate software alarms or server management software.

**WORKAROUND:** Reboot the server.

**STATUS:** This erratum was fixed in BIOS 1.00.05 CD0.

## 5.    BIOS Does Not Remap Bad SIMMs Correctly During a System Reset

**PROBLEM:** When bad SIMMs are detected in the system, the BIOS may not remap the bad SIMMs correctly during a system reset.

**IMPLICATION:** Memory may be mapped to an incompatible memory range causing an error message to be displayed and the server to immediately halt or too much memory may be mapped out and the server will run with less memory.

**WORKAROUND:** The user must find and replace the bad SIMM(s) by trial and error until the problem ceases to exist.

**STATUS:** This erratum was fixed in BIOS 1.00.05 CD0.

## 6.    The Fab 3.x Processor Module Does Not Support the 200-MHz Pentium Pro Processor with 512-Kbyte L2 Cache

**PROBLEM:** The upper bound of the current requirements for the 200-MHz Pentium Pro processor with 512-Kbyte L2 cache is greater than the current provided by the DC-DC converters on the Fab 3.x processor module. The processor module currently supports the 166-MHz version of the Pentium Pro processor with 512-Kbyte L2 cache. This applies to all processor modules up through and including the Fab 3.2.

**IMPLICATION:** If the 200-MHz Pentium Pro processor with 512-Kbyte L2 cache is installed on a Fab 3.x processor module, intermittent errors may arise because of the DC-DC converter limitations and unpredictable system failures may result.

**WORKAROUND:** None Identified.

**STATUS:** This erratum was fixed with the Fab 4.2 processor module (PBA# 659506-212).

## 7.    EISA Read Performance is Below Expectations

**PROBLEM:** The B0 stepping of the Intel 450GX PCIset will not perform greater than Dword transfers if the read transfer requested by the PCI master is not 32 byte (cache line) aligned. This

causes EISA read performance to be lower than expected. Because the PCEB always performs a 16 byte read when beginning a transfer, the first read has a dword transfer rate of 4-1-1-1-1..., where the count indicates the dwords transferred per PCI transaction. The Intel 450GX PCIset has a long initial latency for reads (approximately 24 PCI clocks from FRAME# asserted to the first TRDY#), therefore, by the time the EISA master reads the first cache line, it must surrender the EISA bus.

**IMPLICATION:** The EISA master read rate never exceeds approximately 6.5 MB per second in the best case. This causes EISA read performance to be lower than expected.

**WORKAROUND:** None identified.

**STATUS:** This erratum was fixed with the Fab 3.5 baseboard module (PBA# 666107-001).

## 8. Incorrectly Inserted Memory Module May Cause Baseboard Damage

**PROBLEM:** If the memory module is inserted at an angle or is not fully inserted, and power is applied to the baseboard, the baseboard may be damaged. When the memory module is incorrectly inserted, the 3.3V power rail is shorted to the memory interface signal lines of the Intel 450GX PCIset. If the system is powered on in this condition, the chip set may be damaged within 10-30 seconds. This is not an issue with the processor or terminator modules.

**IMPLICATION:** The baseboard may be damaged if the memory module is not correctly inserted.

**WORKAROUND:** Insure the memory module is fully seated and straight before applying power to the baseboard. If the board set is installed in an AP450GX MP Server Chassis, make sure the module cover plate is installed before powering on the system. Correctly installing the cover plate will insure the memory module is fully inserted.

**STATUS:** There are no plans to fix this erratum.

## 9. If Address Bit Permuting is Enabled Memory Resizing Can Not Be Performed

**PROBLEM:** If address bit permuting is enabled on an AP450GX MP Server and a single bit or double bit memory error occurs which requires a reduction in memory size, the system may hang. It is not possible for memory downsizing to occur if address bit permuting is enabled. Furthermore, the error log will not correctly identify the SIMM where the memory error has occurred.

**IMPLICATION:** If a bad SIMM exists in the system and address bit permuting is enabled, then the system may hang, and the error log will not correctly identify the SIMM where the memory error has occurred.

**WORKAROUND:** Disable address bit permuting in the BIOS setup, clear the error log after address bit permuting has been disabled, and then find and replace the bad SIMM(s).

**STATUS:** There are no plans to fix this erratum.

## 10.  BIOS Setting IOQ=8 May Cause SMM Handler to Hang the Operating System

**PROBLEM:** An AP450GX MP Server system with two or more processors is configured with BIOS setting IOQ=8. If the stress test, iSTRESS, is run for approximately 8 hours, and if the SMI rate is greater than two interrupts per second, then the SMM handler may hang the operating system. Data corruption is also a possibility when using this configuration. (see Intel 450GX PCIset erratum number 1 for further details.)

**IMPLICATION:** Setting IOQ=8 may cause silent data corruption and server hangs. This problem was seen using Microsoft Windows NT 3.51.

**WORKAROUND:** The BIOS sets IOQ=1 if the default settings are selected in the BIOS setup. Manually set IOQ=1 in the BIOS setup if the default IOQ setting has been changed. Intel recommends only running with the default BIOS settings.

**STATUS:** This erratum was fixed with the Fab 3.5 baseboard module (PBA# 666107-001).

## 11.  If Incompatible SIMMs are Installed the System May Hang During Reset

**PROBLEM:** Due to an anomaly in the B0 stepping of the Intel 450GX PCIset memory controller there are limitations on which sizes of SIMMs can be mixed within a system using the 1GB Memory Module. (see Intel 450GX PCIset erratum number 4 for further details.)

**IMPLICATION:** Use of any unsupported SIMM combinations may result in server hangs. The BIOS will detect an unsupported SIMM configuration, display an error message and prevent the system from booting.

**WORKAROUND:** Only use supported SIMM combinations. Not all combinations of SIMMs can be mixed. Below is a matrix of supported SIMM combinations for the 1GB memory module.

| | | BANK 1 | | | | |
|---|---|---|---|---|---|---|
| | | 16 MB | 32 MB | 64 MB | 128 MB | Notes |
| **BANK 0** | **16 MB** | Yes | Yes | No | No | 1 |
| | **32 MB** | Yes | Yes | No | No | 2, 3 |
| | **64 MB** | No | No | Yes | Yes | |
| | **128 MB** | No | No | Yes | Yes | |

Notes:

16MB single sided SIMMs only

32MB double sided SIMMs only.

32MB single sided SIMMs may be used but may not be mixed with any other type of SIMM.

**STATUS:** This erratum was fixed with the Fab 3.5 baseboard module (PBA# 666107-001).

## 12.  Fan Failure Causes Intrusion Switch Detection to be Disabled

**PROBLEM:** The intrusion switch and the fan fail alert share the same A/D channel for reporting chassis intrusions and system fan failures. If a fan failure occurs, the BIOS disables the A/D channel.

**IMPLICATION:** A chassis intrusion will not be detected and logged if the intrusion switch is opened after a fan failure occurs.

**WORKAROUND:** None Identified.

**STATUS:** This erratum was fixed in BIOS 1.00.05 CD0.

### 13. BIOS Record Type 13H Indicates Incorrect Hard Drive Information

**PROBLEM:** The BIOS does not record the hard drive information into the flash Memory Device under record type 13H. This field is an information only field that contains data related to the first four hard drives in the system. The record type 13H exists but no data exists in the record fields.

**IMPLICATION:** Applications referencing this record may display incorrect information for the first four hard drives in the system.

**WORKAROUND:** None Identified.

**STATUS:** This erratum was fixed in BIOS 1.00.05 CD0.

### 14. Memory Resizing Error Causes BIOS to Report Wrong Memory Bank

**PROBLEM:** If a bad memory location is detected during the memory test at boot time, the BIOS correctly resizes the memory and incorrectly reports to the user the bank number that was just resized.

**IMPLICATION:** An incorrect location of the bad SIMM is reported. The user must find and replace the bad SIMM(s) by trial and error until the problem ceases to exist.

**WORKAROUND:** None Identified.

**STATUS:** This erratum was fixed in BIOS 1.00.05 CD0.

### 15. Pentium Pro Processor Data Bus Single Bit ECC Errors May Cause Excessive SMI Generation

**PROBLEM:** The BIOS SMI handler currently does not check and log single bit ECC errors for the Pentium Pro Processor data bus. The BIOS does not disable the bit that caused the error which results in the continual generation of the SMI for the error.

**IMPLICATION:** If a system continuously encounters single bit ECC errors, system performance may decrease due to an increase in the number of times the SMI handler needs to be executed.

**WORKAROUND:** Disable SMM mode in the BIOS setup.

**STATUS:** This erratum was fixed in BIOS 1.00.05 CD0.

### 16. Incorrectly Entering Administrator Password May Hang SCU 3.40/OVL 1.31

**PROBLEM:** With the administrator password enabled and set, the SCU will hang after an incorrect password is entered three consecutive times and then a correct password is entered.

**IMPLICATION:** The SCU and the system will hang as soon as it starts to process the CFG files. A reset is required.

**WORKAROUND:** None Identified.

**STATUS:** This erratum was fixed in SCU 3.50/OVL 1.40.

## 17. Entering a Valid Password to Exit BIOS "Secure Mode" Leaves Keyboard Lights Enabled

PROBLEM: When exiting BIOS secure mode by entering the appropriate user or administrator password both the caps lock and scroll lock keyboard lights are enabled. This only happens when pressing the caps lock key two times before putting the system into secure mode (characterized by the keyboard lights flashing in sequence) and not when it is waiting at a password prompt. The lights left enabled are always the same and are not dependent upon where the "pulsing" light was when the password was entered.

IMPLICATION: The keyboard lights display the incorrect state for the caps lock key and the scroll lock key, and the caps lock and scroll lock are not really enabled.

WORKAROUND: Pressing the caps lock key twice and the scroll lock key twice will reset the lights properly.

STATUS: This erratum was fixed in BIOS 1.00.05 CD0.

## 18. Greater Than 1.5 GB of Memory Installed May Cause System Hang

PROBLEM: If a Writeback Invalidate to page 0x7000000 - 0x7003ffff is performed, the system will hang. This is a valid address when greater than 1.5GB of memory is installed. System hangs have only been seen while executing focused tests during problem isolation. (see Pentium® Pro processor erratum numbers 29 and 50 for further details.)

IMPLICATION: If the memory module uses greater than 1.5 GB of memory, then the server may hang.

WORKAROUND: Use less than 1.5 GB of memory.

STATUS: This erratum was fixed in BIOS 1.00.05 CD0.

## 19. BIOS Does Not Log Bad SIMM Location During POST Memory Testing

PROBLEM: If there is a memory downsizing during POST memory testing, the BIOS does not log the bad SIMM(s) location into the event log; and the bad SIMM(s) can not be easily located.

IMPLICATION: Memory downsizing occurs as a result of one or more bad SIMMs. It will be difficult to find the bad SIMM(s). The user must find and replace the bad SIMM(s) by trial and error until the problem ceases to exist.

WORKAROUND: None Identified.

STATUS: This erratum was fixed in BIOS 1.00.05 CD0.

## 20. Spurious Interrupts May Cause Virtual Wire Mode APIC Operation to Fail

PROBLEM: In the local APIC design in the Pentium Pro Processor, if interrupts are configured for "virtual wire operation" with interrupt delivery via the INTR signal, then certain spurious interrupts can cause the spurious interrupt vector to be supplied by the local APIC and not the 8259 in the ESC.

IMPLICATION: An operating system can crash if no interrupt handler is available for the spurious interrupt vector supplied by the local APIC (see Pentium Pro processor erratum number 5AP for further details). In addition, the spurious interrupt is sometimes seen as a division by zero error by the Pentium Pro processor (see Pentium Pro processor erratum number 6AP for further details).

WORKAROUND: Use Virtual Wire Mode B option with BIOS 1.00.05 CD0.

STATUS: This erratum was fixed in BIOS 1.00.06 CD0.

## 21. The SCU Cannot Change the State of the PCI System Error Option

PROBLEM: The PCI System Error option is available in the SCU but is not functional. Choosing enable or disable within the SCU has no effect on the actual state of this option.

IMPLICATION: Depending on the initial state of the PCI System Error option, either the error logging associated with this option will not occur, or the error logging associated with this option will not be disabled.

WORKAROUND: The PCI System Error option can be properly set via BIOS Setup.

STATUS: This erratum was fixed in SCU 3.50/OVL 1.40.

## 22. The SCU Incorrectly Sets the Baud Rates For Serial Redirection

PROBLEM: The baud rates shown in the SCU are different from the actual baud rate set by the SCU. Currently, the SCU will display and set the baud rates as follows:

| Baud Rate Shown in SCU | Actual Baud Rate Set |
| --- | --- |
| 9600 | 2400 |
| 19200 | 9600 |
| 38400 | 19200 |
| 115200 | 115200 |

IMPLICATION: If the baud rate is set using the SCU, a slower than expected serial redirection baud rate will be realized.

WORKAROUND: The BIOS setup displays and sets the serial redirection baud rates properly.

STATUS: This erratum was fixed in SCU 3.50/OVL 1.40.

## 23. Power and Reset Security Switches In The BIOS Setup Are Not Available In The SCU

PROBLEM: The option to enable or disable the power and reset switches is accessible in the BIOS setup security section, but is not available in the security section of the SCU.

IMPLICATION: The power and reset security switches cannot be enabled or disabled using the SCU.

WORKAROUND: Use the BIOS setup to enable or disable these options.

STATUS: This erratum was fixed in SCU 3.50/OVL 1.40.

## 24. Incorrectly Initialized Real Time Clock Registers May Hang Operating System On The Tenth Of Each Month

PROBLEM: Incorrectly initialized registers in the Dallas 1587 real time clock may hang the operating system on Intel server products. The operating system may fail to boot, or a currently running system may hang. This symptom will only happen on the tenth of the month. After rebooting the system it will work properly until the tenth of the next month. The root cause is Testview, Intel's manufacturing test and diagnostic software. Testview improperly initializes the alarm registers in the Dallas Real Time Clock which results in an alarm interrupt.

IMPLICATION: All systems manufactured between November 1995 and April 1996, or systems that have had Testview (PCDIAGS) versions 3.31 through 3.36 run on them may hang on the tenth of the month. This issue was seen initially on servers running Microsoft Windows NT 3.51.

WORKAROUND: A special utility has been developed to properly initialize the real time clock registers. This utility is called RTC.EXE and is available from the Intel Applications support BBS, or by contacting an Intel Field representative.

STATUS: This erratum was fixed in Testview (PCDIAGS) version 3.37a.

## 25. BIOS Setting IOQ=Autodetect Causes BIOS To Set IOQ=8

PROBLEM: If the Autodetect option for the bus performance setting in the BIOS setup is selected, the IOQ depth will be set to IOQ=8 on an AP450GX MP server containing the B0 stepping of the Intel 450GX PCIset. (see Intel 450GX PCIset erratum numbers 1, 6, and 19 for further details.)

IMPLICATION: Setting IOQ=8 may cause silent data corruption and server hangs.

WORKAROUND: The BIOS sets IOQ=1 if the default settings are selected in the BIOS setup. Manually set IOQ=1 in the BIOS setup if the default IOQ setting has been changed. Intel recommends only running with the default BIOS settings.

STATUS: This erratum was fixed in BIOS 1.00.05 CD0.

## 26. If The System Temperature Reaches A Warning Threshold Temperature Monitoring Is Disabled

PROBLEM: The system temperature monitoring is disabled after the system either reaches the upper or the lower warning threshold temperature.

IMPLICATION: After temperature monitoring is disabled, all temperature events will not be logged.

WORKAROUND: None Identified.

STATUS: This erratum was fixed in BIOS 1.00.05 CD0.

## 27. Using 60ns 64MB SIMMs and 2-Way Memory Interleave May Cause System Hang During Reset

**PROBLEM:** If 60ns 64MB SIMMs are installed and the system is configured as 2-way interleave (i.e. 4 SIMMs are installed) , the system will hang after finishing the memory test during a reset.

**IMPLICATION:** The system will hang after finishing the memory test during a reset.

**WORKAROUND:** Do not install 60ns SIMMs in a 2-way interleave configuration.

**STATUS:** This erratum was fixed in BIOS 1.00.05 CD0.

## 28. Location of Password Prompts in POST Sequence May Cause System Security Violation

**PROBLEM:** The BIOS system administrator and user passwords must be verified before the option ROMs from adapter cards are scanned, otherwise the SCSI option ROMs would allow the user to reformat the hard drives, and do other actions which violate security.

**IMPLICATION:** The SCSI option ROM utilities are executed early in the system boot sequence, before the password prompt, and hence are available to anyone with access to the system. Access to the SCSI option ROM utilities allow the ability to format hard drives and could be a serious security violation if accessed by unauthorized users.

**WORKAROUND:** None Identified.

**STATUS:** This erratum was fixed in BIOS 1.00.05 CD0.

## 29. Clearing NVRAM (CMOS) and Installing an Operating System May Cause a System Hang

**PROBLEM:** NVRAM (CMOS) was cleared on an AP450GX MP Server and the system was reset. During the final stages of an operating system installation, when the system was restarted for the second time, the BIOS string was displayed on the LED display of the system for about a second and then the system failed to startup. The video never came up and the LED display went blank.

**IMPLICATION:** The server may hang during the final stages of an operating system installation. This issue was seen during a Microsoft Windows95 installation.

**WORKAROUND:** Clear the NVRAM (CMOS) and reset the system.

**STATUS:** This erratum was fixed in BIOS 1.00.05 CD0.

## 30. Excessive Single-Bit ECC Errors Incorrectly Disables Single-Bit Error Logging for Memory Bus and Processor Data Bus

**PROBLEM:** The BIOS will disable single bit error logging after ten single-bit errors occur on the Pentium Pro processor data bus or on the memory bus. This is done to avoid filling the error logs with repeated errors of the same type (i.e. a SIMM is bad and always has the same single bit error). However, if the errors were on the memory bus, the BIOS simultaneously disables error

logging  for both the memory bus and the processor data bus. The same is true if the errors occur on the processor data bus.

IMPLICATION: If single bit error logging is disabled due to errors on the memory bus, single bit errors on the processor data bus will not be logged. Conversely, if single bit error logging is disabled due to errors on the processor data bus, single bit errors on the memory bus will not be logged.

WORKAROUND: None Identified.

STATUS: This erratum is targeted to be fixed in a future release of the BIOS.

## 31.    Saving BIOS Configuration After Date Change May Cause Date to be Set Incorrectly

PROBLEM: If a user opens the BIOS setup menu a few minutes before 24:00, makes some BIOS changes, allows time to elapse such that a new day begins (i.e. 00:01), saves the configuration and resets the system, the BIOS setup will then record the previous date as the current date.

IMPLICATION: Saving BIOS setup configurations across date changes will cause the server to incorrectly set the date.

WORKAROUND: Do not execute and save BIOS setup configurations across date changes.

STATUS: This erratum was fixed in BIOS 1.00.06 CD0.

## 32.    BIOS Setting IOQ = 8 May Corrupt PCI Configuration Cycles

PROBLEM: When PCI configuration cycles interact with an inbound posted write in the non-compatibility PCI bridge, the system may hang or the configuration cycle data may become corrupted. (See Intel 450GX PCIset erratum number 6 for more details).

IMPLICATION:. The configuration space of bridges or PCI devices may be corrupted. PCI configuration cycles can occur any time an O/S boots or loads a driver. This erratum could occur under any O/S and any driver.

WORKAROUND: The BIOS sets IOQ=1 if the default settings are selected in the BIOS setup. Manually set IOQ=1 in the BIOS setup if the default IOQ setting has been changed. Intel recommends only running with the default BIOS settings.

STATUS: This erratum was fixed with the Fab 3.5 baseboard module (PBA# 666107-001).

## 33.    PCI-to-PCI Bridges May Cause The System To Hang

PROBLEM: A livelock condition may result if adapter cards with a PCI-to-PCI bridge are installed in the system. (See Intel 450GX PCIset erratum number 7 for more details).

IMPLICATION: The system may hang if a PCI-to-PCI bridge is installed in the system.

WORKAROUND: Do not install PCI-to-PCI bridges in the system.

STATUS: This erratum was fixed with the Fab 3.5 baseboard module (PBA# 666107-001).

## 34. Board Set TAP Reset Circuit May Cause Incorrect System Power On

PROBLEM: The AP450GX MP Server Board Set asserts the "pwrgood" signal which resets the processors Test Access Port (TAP) during a power on. The sB1 stepping of the Pentium Pro processor implemented a change to the TAP reset circuitry (See Pentium® Pro erratum number 27 for more details). This change does not allow "pwrgood" to reset the TAP circuitry, but does allow other reset methods. If an sB1 stepping of the Pentium Pro processor is installed, the system may not power on correctly. Note that while this could occur on any given system power cycle, Intel has only seen this occur on systems during rapid (less than 25 seconds) power cycle stress tests.

IMPLICATION: If an sB1 stepping of the Pentium Pro processor is installed, the system may not power on correctly, one or more installed processors may not come online, and the system may hang. Once the system has powered on correctly, no other side effects occur as a result of this eratum. Note that while this could occur on any given system power cycle, Intel has only seen this occur on systems during rapid (less than 25 seconds) power cycle stress tests.

WORKAROUND: There are three workarounds possible:

Add a Power Up TAP Reset (PUTR) module to the baseboard. A PUTR is a ~2" x 2" printed circuit board that plugs into the ITP connector on the baseboard. Installing the PUTR insures the system will power on correctly with the sA1 and/or sB1 stepping of the Pentium Pro processor installed. The PUTR is a field upgrade item only and should not be installed prior to product shipment because it may unseat from the ITP connector during shipment. The PUTR is available from Intel at no cost. Please contact your Intel representative for ordering information.

Perform rework to the processor module. (For rework details see the Intel Action Alert *AP450GX Power UP Issue with the sB1 Stepping of the Pentium Pro processor*, Serial Number: AA-0001, released 12/31/96.)

Wait at least 60 seconds after the system has been powered off before powering up the system. This option is not guaranteed to work all the time and should only be considered a temporary workaround.

STATUS: This erratum was fixed with the Fab 4.3 processor module (PBA# 659506-316).

## 35. INCA Anomaly at Power Up May Cause PCI Bus Clocks to Run at 66MHz on Baseboards with the C0 Stepping of Intel 450GX PCIset

PROBLEM: The AP450GX MP Server Board Set containing the C0 stepping of the Intel 450GX PCIset may power up with the PCI bus clocks incorrectly running at 66 MHz rather than at 33 MHz. Upon power up, the clock detection circuit in the INCA component samples the PCLK outputs (OPB1_PCLK, OPB2_PCLK) from OPB1 and OPB2 to determine if Source B or Source C clock inputs to the INCA are to be used for the PCI clocks. A timing change to the reset logic in the C0 stepping of OPB has resulted in a possibility that the INCA component selects the wrong clock(s) for the PCI bus(es). INCA clock selection occurs only at power-up. The INCA component samples the OPB PCLK (OPB1_PCLK, OPB2_PCLK) signals after the rising edge of the PS_PWR_GOOD signal (power supply good indicator) and with the qualifying assertion of the IRST_L signal (derived from the OPB PCIRST_L signals). The clock source detection circuitry within the INCA component requires that the sampled clock source information remain

stable during the first 45nS following the rising edge of the PS_PWR_GOOD signal, when the IRST_L signal is asserted. Source B or Source C clock inputs to INCA must not transition low to high during this time, or a possibility of incorrect PCI clock frequency selection exists. Specifically the Source B and Source C clock inputs to INCA are PCLK outputs from OPB1 (OPB1_PCLK) and OPB2 (OPB2_PCLK). The C0 stepping of the OPB issues the PCIRST_L signal significantly earlier than the B0 stepping and the new timing results in the assertion of IRST_L to the INCA chip during the first 45nS following the rising edge of the PS_PWR_GOOD signal. The OPB PCLK output signals (OPB1_PCLK, OPB2_PCLK) may generate low to high pulses during the sampling window opened up by the earlier IRST_L timing. The PCLK output signal (OPB1_PCLK, OPB2_PCLK) glitching is believed to be caused by internal OPB flip-flop state changes during the system 3.3 volt power supply initial power ramp, and is of a very short duration.

IMPLICATION: This anomaly is believed to be limited to the unique implementation and interaction between the (C0 stepping) 82454GX PB (OPB component) of the Intel 450GX PCIset and the INCA component of the AP450GX MP Server Board Set. This anomaly has not been observed on systems with baseboards containing the B0 stepping of the Intel 450GX PCIset and Intel has not been able to reproduce this anomaly on systems with baseboards containing the B0 stepping of the Intel 450GX PCIset. The system may exhibit various symptoms when the PCI bus clocks are running at the incorrect speed. Should the failure occur, the symptoms are believed to be highly visible and immediate, as indicated in observed scenarios 1 through 3 below. Scenario 4 results in the system running without any apparent failures. However, prolonged operation at 66MHz may damage the onboard SCSI controllers, and/or INCA component.

OPB1 PCI bus clock running at 66 MHz - System hangs with no post code (blank LCD).

OPB2 PCI bus clock running at 66 MHz - Device failures on PCI bus 2, various post codes, or MTA diagnostic failures.

OPB1, OPB2 PCI bus clocks running at 66 MHz - System hangs during POST with a NMI error.

OPB2 PCI bus clock running at 66 MHz - No adapters installed in PCI bus 2 and system appears to run correctly without the onboard SCSI controllers active.

WORKAROUND: None identified for Fab 3.5 baseboard modules with PBA# 666107-001 or PBA# 666107-002. See fix information in status section below.

STATUS: Intel has implemented a programming change to a PLD (Programmable Logic Device) on the AP450GX MP Server baseboard. This PLD change ensures that IRST_L remains inactive during the first 45nS following the rising edge of the PS_PWR_GOOD signal. This erratum was fixed with the Fab 3.5 baseboard module (PBA# 666107-004, PBA# 666107-005, or PBA# 666107-006).