TE430VX Technical Product Specification

Order Number 281817-004
November 1996

The TE430VX motherboard may contain design defects or errors known as errata. Characterized errata that may cause the TE430VX motherboard's behavior to deviate from published specifications are documented in the TE430VX Motherboard Specfication Update.

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Revision History

Revision	Revision History	Date
-004	Added serial port2, fan, and VESA connectors to art; Added Back Panel I/O Shield; Added Port 79 codes; Added Port 80 Codes; corrected inaccuracies; reworded sections for clarity	11/96
-003	Fixed drawing designators, added USB module, removed reference to Creative Labs Vibra16S with Yamaha FM Synthesis	5/96
-002	Changed Name of product from Advanced/TE to TE430VX throughout	4/96
-001	Preliminary release of the TE430VX Technical Product Specification	3/96

This product specification applies only to standard TE430VX motherboards with BIOS identifier 1.00.0x.CY0.

Changes to this specification will be published in the TE430VX Motherboard Specification Update before being incorporated into a revision of this document.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777, Germany 44-0-1793-421-333, other Countries 708-296-9333.

Table of Contents

1 Motherboard Description

1.1 Overview

The TE430VX motherboard supports Pentium® microprocessors operating at 75, 90, 100, 120, 133, 150, 166, and 200 MHz. The motherboard features:

- ATX form factor
- Socket 7 Pentium OverDrive® processor socket

Main Memory

- Two 168-pin DIMM sockets
- Support for up to 128 MB of Extended Data Out (EDO) or fast page DRAM, or 64 MB of synchronous DRAM (SDRAM)

Second Level Cache Memory

- 256 KB Pipeline Burst SRAM soldered to the motherboard, or
- CELP socket for COASt modules

Chipset and PCI/IDE Interface

- Intel 82430VX PCIset
- Integrated PCI bus mastering controller
- Two fast IDE interfaces
- Support for up to four IDE drives or devices

I/O Features

- SMC FDC37C932FR Ultra I/O controller
- Integrates standard I/O functions: floppy drive interface, one multi-mode parallel port, two FIFO serial ports, real-time clock, keyboard and mouse controller, IrDA†-compatible interface
- Support for two Universal Serial Bus (USB) interfaces

Expansion Slots

- 2 ISA
- 3 PCI
- 1 shared PCI/ISA

Audio Subsystem

- Creative Labs Vibra16C audio codec
- Wavetable upgrade header
- ModemBlaster upgrade header

Graphics Subsystem

- S3† Trio64† V+ graphics controller
- VESA† feature connector

Other Features

- Plug and Play compatible
- Support for Advanced Power Management

Software drivers and utilities are available from Intel.

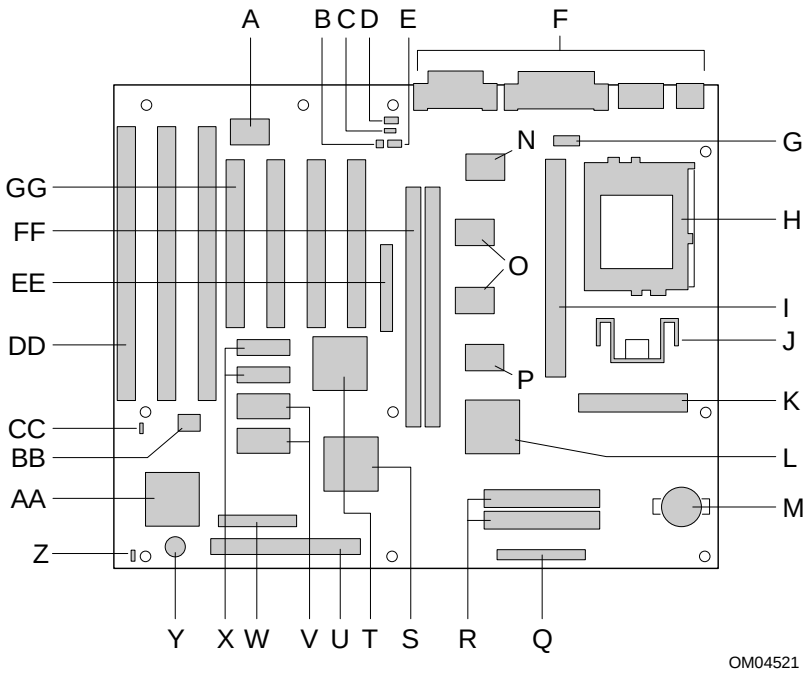


Figure 1. Motherboard Components

A	Optional Creative Labs audio device	R	IDE connectors
B	Optional telephony connector	S	PIIX3 PCI/ISA IDE Xcelerator
C	Optional CD-ROM audio connector	T	Optional S3 Trio64 V+ graphics controller
D	Optional ModemBlaster connector	U	Front panel header
E	Optional wavetable connector	V	Optional video memory sockets
F	Back panel I/O connectors	W	Configuration jumper block
G	Serial port 2 connector	X	Optional video memory
H	Socket 7 Pentium processor socket	Y	Onboard Speaker
I	Optional CELP socket	Z	Fan connector
J	Linear voltage regulator	AA	SMC FDC37C932FR Ultra I/O controller
K	Primary power connector	BB	2 Mbit TSOP FLASH
L	82437VX TVX	CC	BIOS recovery jumper
M	Battery	DD	ISA connectors
N	82438VX TDX	EE	Optional VESA video feature connector
O	Optional PB SRAM	FF	DIMM sockets
P	82438VX TDX	GG	PCI connectors
Q	Floppy drive connector		

1.2 Motherboard Manufacturing Options

- Second level cache (L2)
  - — 256KB Pipeline Burst SRAM soldered onto the motherboard, or
  - — CELP socket for COASt modules
- Support for Universal Serial Bus (USB)
- Creative Labs Vibra16C audio codec
- S3 Trio64 V+ graphics controller
- Split plane voltage support for Socket 7

1.3 Form Factor

The motherboard is designed to fit into a standard ATX form factor chassis. Figure 2 illustrates the mechanical form factor for the motherboard. The TE430VX form factor adheres to the standard ATX guidelines in that the outer dimensions are 12” x 9.6”. Location of the I/O connectors and mounting holes are in strict compliance with the ATX specification (see Section 5.2).

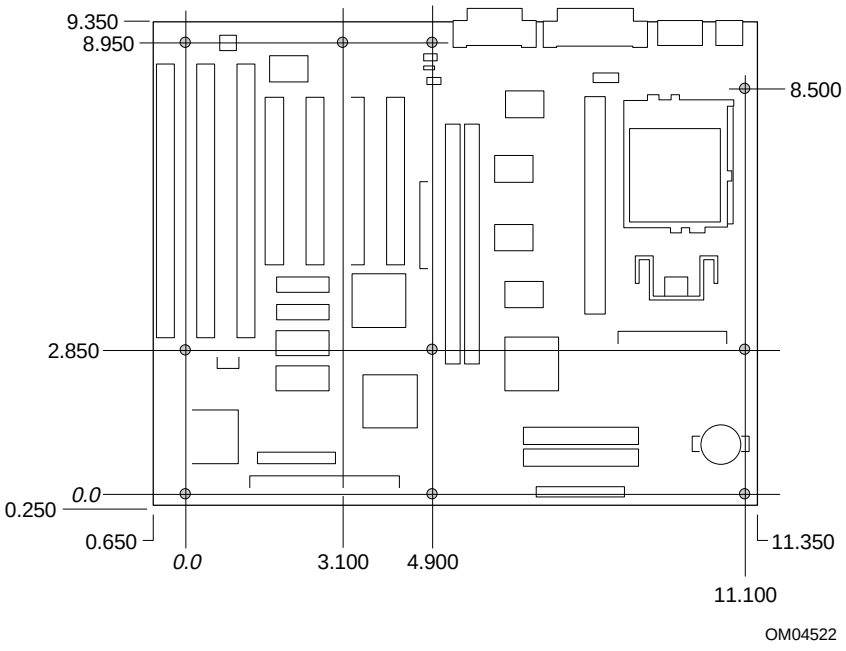


Figure 2. Motherboard Dimensions

1.4 I/O Shield

The back panel I/O shield for the TE430VX motherboard must meet specific dimensional and material requirements. Systems based on this motherboard need the back panel I/O shield in order to pass certification testing. Figure 3 shows the critical dimensions for both options of the I/O shield, and indicates the position of each cutout.

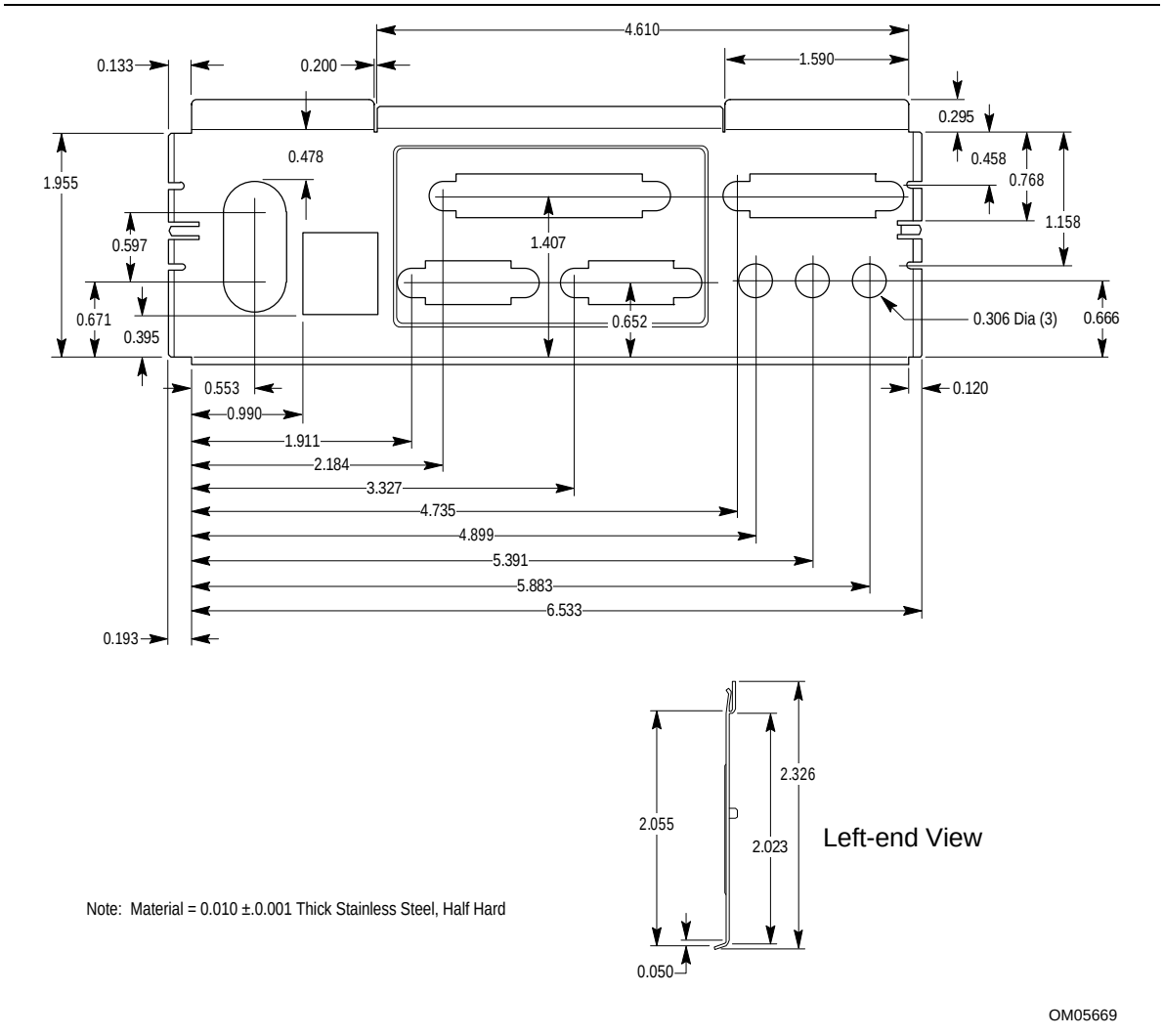


Figure 3. Back Panel I/O Shield Dimensions

1.5 Microprocessor

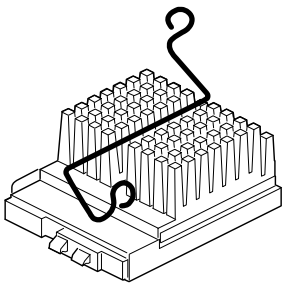
The motherboard supports 3.3 V Pentium processors running internally at 75, 90, 100, 120, 133, 150, 166, and 200 MHz. An onboard voltage regulator derives the necessary voltage from the system power supply. The motherboard supports standard, VR-, or VRE-specified processors.

The Pentium processor maintains full backward compatibility with the 8086, 80286, Intel386™ and Intel486™ processors. The processor supports both read and write burst mode bus cycles. It also features separate 8 KB on-chip code and data caches that employ a write-back policy.

The microprocessor contains an advanced numeric coprocessor that maintains full backward compatibility with math coprocessors that comply with ANSI/IEEE standard 754-1985.

CAUTION

If you use clips to secure a heat sink to the processor, do not use bail-wire style heat sink clips. These clips have been known to damage the motherboard when installed or removed incorrectly. The figure to the right shows an example of the bail-wire style heat sink clip.



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1.5.1 Microprocessor Upgrade

The motherboard has a 321-pin Socket 7 zero insertion force (ZIF) microprocessor socket. Socket 7 supports upgrades to higher performance Pentium OverDrive processors not supported by Socket 5.

1.6 Memory

1.6.1 Main Memory

The motherboard has two DIMM sockets. Memory can be installed in one or two sockets. Minimum memory size is 8 MB. Maximum memory size is 64 MB for SDRAM and 128 MB for EDO DRAM. The BIOS automatically detects memory type, size, and speed so no jumper settings are required.

The motherboard supports the following:

- 168-pin DIMMs with gold-plated contacts
- 66 MHz SDRAM and 60 ns EDO DRAM
- 64-bit data path
- Single- or double-sided DIMMs in the following sizes.

DIMM Size	Non-parity Configuration
8 MB (SDRAM/EDO)	1 x 64
16 MB (SDRAM/EDO)	2 x 64
32 MB (SDRAM/EDO)	4 x 64
64 MB (EDO only)	8 x 64

Memory type, size, and speed can vary between sockets so EDO and SDRAM can be installed on the same motherboard.

1.6.1.1 EDO DRAM

EDO DRAM improves memory read performance by holding the memory data valid until the next CAS# falling edge unlike fast page mode DRAM, which tri-states the memory data when CAS# negates to precharge for the next memory cycle. With EDO DRAM, the CAS# precharge overlaps the data-valid time, which allows CAS# to negate earlier while still satisfying the memory data-valid window.

1.6.1.2 SDRAM

Synchronous DRAM (SDRAM) is designed to improve main memory performance. Unlike fast page or EDO DRAM, SDRAM is synchronous with the memory clock. This simplifies the timing design and increases memory speed because all timing is dependent on the number of memory clock cycles. Discrete SDRAM components must meet the 66 MHz PC SDRAM Specification version 1.1 to function correctly.

1.6.2 Second Level Cache

The motherboard has two manufacturing options for second level (L2) cache memory:

- 256 KB direct-mapped write-back cache contained in two global write enable (GWE) Pipeline Burst SRAM (PBSRAM) devices soldered to the motherboard. An 8 KB x 8 external Tag SRAM provides caching support for up to 64 MB of main memory.
- Type 4 Card Edge Low Profile (CELP) socket conforming to Intel's COASt Module Specification. The CELP socket can accept 256 KB or 512 KB cache memory modules.

1.7 Chipset

The Intel 82430VX PCIset consists of the 82437VX Xcelerated Controller (TVX), two 82438VX data path (TDX) components, and one 82371SB PCI/ISA IDE Xcelerator (PIIX3) bridge chip.

1.7.1 82437VX Xcelerated Controller (TVX)

The TVX provides all control signals necessary to drive second level cache and main memory including multiplexed address signals. It also controls system access to memory and generates snoop controls to maintain cache coherency. The TVX comes in a 208-pin QFP package that features:

- Microprocessor interface control
- Integrated L2 write-back cache controller
  - — Pipeline Burst SRAM
  - — 256 KB direct-mapped
- Integrated DRAM controller
  - — 64-bit path to memory
  - — EDO and Synchronous DRAM support
  - — Non-parity support only
- Fully synchronous PCI bus interface
  - — 25, 30, and 33 MHz bus speeds
  - — PCI to DRAM data throughput at greater than 100 MB per second
  - — Up to four PCI masters in addition to the PIIX3 and IDE

1.7.2 82438VX Data Path (TDX) Components

Two TDX data path components provide a 64-bit processor-to-memory data path. The TDX components are controlled by the TVX. The TDX components add one load to the PCI bus and perform all of the required byte and word swapping. The TDX devices come in a 100-pin QFP package.

1.7.3 82371SB PCI/ISA IDE Xcelerator

The 82371SB PCI/ISA IDE Xcelerator (PIIX3) is the interface between the PCI and ISA buses. It features an integrated dual-channel enhanced IDE interface that supports up to four IDE devices. The PIIX3 comes in a 208-pin QFP package that features:

- PCI and ISA bus interface
- Universal Serial Bus (USB) controller
  - — Host/hub controller
- Integrated dual-channel enhanced IDE interface
  - — Support for up to four IDE devices
  - — PIO Mode 4 transfers at up to 16 MB per second
  - — Integrated 8 x 32-bit buffer for bus master PCI IDE burst transfers
  - — Bus master mode
- PCI compliance (see Section 5.2)
- Enhanced DMA controller supporting up to seven DMA channels
- Interrupt controller with PCI-to-ISA interrupt mapping circuitry
- 16-bit counters/timers
- SMI interrupt logic and timer with fast on/off mode
- NMI circuitry

1.7.4 Universal Serial Bus (USB) Support

The motherboard features two USB ports as a factory installed option. The ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports. The motherboard fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible. Features of the USB include:

- Self-identifying, hot pluggable peripherals
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error handling and fault recovery mechanisms built into protocol

1.7.5 IDE Support

The motherboard has two independent bus mastering PCI IDE interfaces that support PIO Mode 3, PIO Mode 4, and ATAPI (e.g., CD-ROM) devices. The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. IDE device transfer rate and translation mode are automatically detected by the BIOS.

Normally, programmed I/O operations require a substantial amount of processor bandwidth; however, in true multi-tasking operating systems like Windows† 95, the bandwidth freed by bus mastering IDE can be devoted to other tasks while disk transfers are occurring.

1.8 I/O Controller

The FDC37C932FR Ultra I/O Controller from Standard Microsystems Corporation features:

- Two serial ports: NS16C550-compatible UARTs with send/receive 16-byte FIFO
- Multimode bidirectional parallel port
  - — Standard mode, IBM† and Centronics† compatible
  - — Enhanced Parallel Port (EPP) mode with BIOS and driver support
  - — High-speed Extended Capabilities Port (ECP) mode
- Industry standard floppy controller with 16-byte FIFO and 2.88 MB floppy drive support
- 8042-compatible keyboard controller
- Real-time clock with 12- and 24-hour time format
- Intelligent Auto Power Management
- 16-bit address qualification
- Soft power management, system management interrupt (SMI) support
- ISA Plug and Play compatible register set (version 1.0a)
- Support for an IrDA-compliant infrared interface

By default, the I/O controller interfaces are automatically configured during boot up. The I/O controller can also be manually configured in the Setup program.

1.8.1 Serial Ports

The motherboard has one 9-pin D-Sub serial port connector located on the back panel. The NS16C550-compatible UARTs support data transfers at speeds up to 460 Kbits/second.

1.8.2 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel of the motherboard. In the Setup program, there are four options for parallel port operation:

- Compatible (standard mode)
- Bidirectional (PS/2† compatible)
- Bidirectional Enhanced Parallel Port (EPP). A driver from the peripheral manufacturer is required for operation. See Section 5.1 for EPP compatibility.
- Bidirectional high-speed Extended Capabilities Port (ECP)

1.8.3 Floppy Controller

The I/O controller is software compatible with the DP8473 and 82077 floppy drive controllers. In the Setup program, the floppy interface can be configured for the following floppy drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch (3-mode floppy support, driver required)
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

1.8.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel of the motherboard. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an over-current condition is removed. While this device eliminates the possibility of having to replace a fuse, power to the computer should be turned off before connecting or disconnecting a keyboard or mouse.

NOTE

You can plug the mouse and keyboard into either connector.

The keyboard controller contains the AMI Megakey keyboard and mouse controller code, which provides the traditional keyboard and mouse control functions, and also supports Power On/Reset password protection. A Power On/Reset password can be specified in the Setup program.

The keyboard controller also supports the following hot-key sequences:

- <CTRL><ALT><DEL> Software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power-On Self Test (POST).
- <CTRL><ALT><+> and <CTRL><ALT><-> Turbo mode. Note that Turbo mode could be affected by the operating system, or whether the processor is in protected mode or virtual x86 mode.
  - <CTRL><ALT><-> For Deturbo mode
  - <CTRL><ALT><+> For Turbo mode
- <CTRL><ALT><defined in Setup>: Power management. This key sequence invokes power managed mode, which reduces the computer's power consumption while maintaining its ability to service external interrupts.
- <CTRL><ALT><defined in Setup>: Keyboard lock. This key sequence is a security feature that locks the keyboard until the User password is entered. When keyboard lock is invoked, the keyboard LEDs flash. To enable the keyboard lock feature, a User password must be specified in the Setup program.

1.8.5 Real-Time Clock, CMOS RAM and Battery

The real-time clock is compatible with DS1287 and MC146818 components. It provides a time-of-day clock and a 100-year calendar with alarm features and century rollover. The clock is accurate to ±13 minutes/year at 25ºC and 5 V. The real-time clock also supports 242-bytes of battery-backed CMOS RAM in two banks, which are reserved for BIOS use.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program or by setting a configuration jumper on the motherboard.

An external coin-cell battery powers the real-time clock and CMOS memory. If the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 5 V standby current from the motherboard's power supply extends the life of the battery.

1.8.6 Infrared Support

The motherboard has a 5-pin header that supports Hewlett Packard† HSDL-1000 compatible infrared (IR) transmitters/receivers. In the Setup program, Serial Port 2 can be directed to a connected IR device. The connection can be used to transfer files to or from portable devices like laptops, PDAs and printers. The Infrared Data Association (IrDA) specification supports data transfers of 115 Kbits/second at a distance of 1 meter.

1.8.7 Consumer Infrared Support

The motherboard has a signal pin that supports Consumer Infrared (IR) devices (remote controls). The signal pin supports receive only. Consumer IR devices can be used to control telephony functions and multimedia operations like volume and CD track changes. A software and hardware interface is needed to use this feature.

1.9 Graphics Subsystem

The optional onboard graphics subsystem uses the S3 Trio64 V+ graphics controller, with the following features:

- 64-bit graphics engine with accelerator core
- 24-bit RAMDAC/clock synthesizer
- Dual programmable clock generators
- DCI-based linear addressing scheme
- S3 Streams Processor (enables the conversion of video data from YUV format to RGB format; accelerates display scaling while maintaining picture quality and frame rate)
- S3 Scenic Highway support for hardware MPEG

1.9.1 Memory Type and Size

The controller is supported by 1 MB of DRAM soldered to the motherboard. Graphics memory can be upgraded to 2 MB by installing 256 KB x 16, 60 ns SOJ DRAM chips in two sockets on the motherboard.

1.9.2 Resolutions and Refresh Rates

Table 1. S3 Trio64 V+ Resolutions and Refresh Rates

1 MB Memory	Refresh Rate (Hz) At:				
Resolution	**4-bit Color (16 Colors)**	**8-bit Color (256 Colors)**	**15/16-bit Color (32K/64K Colors)**	**24-bit Color (16M Colors)**	**32-bit Color (16M Colors)**
640 x 480	60	60, 72, 75, 85	60, 72, 75	60, 72, 75 *	not supported
800 x 600	not supported	56, 60, 72, 75, 85	60, 72, 75	60, 72, 75 *	not supported
1024 x 768	not supported	43(IL), 60 ,70, 75, 85	not supported	not supported	not supported
1152 x 864	not supported	60	not supported	not supported	not supported
1280 x 1024	43(IL), 45(IL), 60, 72, 75*	not supported	not supported	not supported	not supported
1600 x 1200	not supported	not supported	not supported	not supported	not supported
2 MB Memory	**Refresh Rate (Hz) At:**				
Resolution	**4-bit Color (16 Colors)**	**8-bit Color (256 Colors)**	**15/16-bit Color (32K/64K Colors)**	**24-bit Color (16M Colors)**	**32-bit Color (16M Colors)**
640 x 480	60	60, 72, 75, 85	60, 72, 75	60, 72, 75 *	60, 72, 75
800 x 600	not supported	56, 60, 72, 75, 85	60, 72, 75	60, 72, 75 *	60, 72, 75
1024 x 768	not supported	43(IL), 60 ,70, 75, 85	43(IL), 60, 70, 75	43(IL), 60, 70, 75 *	not supported
1152 x 864	not supported	60	not supported	not supported	not supported
1280 x 1024	43(IL), 45(IL), 60, 72, 75*	45(IL), 60, 72, 75	not supported	not supported	not supported
1600 x 1200	not supported	48.5(IL)	not supported	not supported	not supported

* Non-accelerated mode only

IL Interlaced

1.9.3 VESA/S3 Scenic Highway Interface Connector

The motherboard has an optional 34-pin multimedia feature connector that uses 26 pins for the VESA standard bus and 6 pins for the S3 Scenic Highway bus. The connector features a shared frame buffer interface and a local peripheral bus with a bidirectional interface that supports video companion devices such as MPEG/live video decoders.

1.9.4 Graphics Drivers and Utilities

Graphics drivers and common graphics utilities are available for Windows† 3.x, Windows 95, and Windows NT†. Drivers and utilities are available from Intel's World Wide Web site (see Section 5.1).

1.10 Audio Subsystem

The optional onboard audio subsystem features the Creative Labs Vibra16C multimedia codec. This component provides all the digital audio and analog mixing functions needed for recording and playing sound on personal computers. The Vibra16C features the following:

- Analog mixing of 6 audio sources
  - — Digital audio (stereo)
  - — CD audio (stereo)
  - — Synthesized music (stereo)
  - — Line level audio (stereo)
  - — Microphone level audio (mono)
  - — Mono audio
- Individual software programmable volume controls
- Mixer controlled recording and source selection
- Automatic gain control with amplifier or fixed gain amplifier for microphone level audio
- Dynamic filtering for digital audio recording and playback
- 8- or 16-bit stereo/mono digital audio playback and recording
- FIFOs for digital audio playback and recording
- Variable sampling rates from 5 KHz to 44.1 KHz
- Built-in analog joystick quad timer
- 8-level volume control mixer
- Integrated FM synthesizer
- Adlib†, Sound Blaster† 16, Sound Blaster Pro, and MPU-401 compatibility
- MPC and MPCII compliance
- Full-duplex operation
- Plug and Play support
- Power management mode

The audio subsystem requires one IRQ and up to two DMA channels. For full duplex operation, the audio subsystem requires two DMA channels (one 16-bit channel and one 8-bit channel). The following table shows the IRQ, DMA channel, and base I/O address options.

Device	IRQ (Options)	DMA Channel (Options)	I/O Address (Options)
Creative Labs 16C Base	5 (default) 7 10	1 (8 bit, default) 3 (8 bit) 5 (16 bit, default) 7 (16 bit)	220h-233h (default) 240h-253h 260h-273h 280h-293h
FM Synthesis			388h-38Bh
Joystick (MIDI port)			200h-207h
MPU-401			300h-301h 330h-331h

1.10.1 Audio Drivers and Utilities

Audio software and utilities are available from Intel's World Wide Web site (see Section 5.1).

1.11 Audio Manufacturing Options

Audio manufacturing options include the following:

- Back panel audio jacks (Line In, Line Out, Mic In)
- CD-ROM audio connector
- Telephony connector
- Wavetable connector
- ModemBlaster connector

1.11.1 CD-ROM Audio Connector

A 1 x 4-pin connector is available for connecting an internal CD-ROM reader to the audio subsystem's mixer. The connector is compatible with most cables supplied with ATAPI CD-ROM readers designed to connect to audio add-in cards.

1.11.2 Telephony Connector

A 2 x 2-pin connector is available for connecting the monaural audio signals of an internal telephony device such as a fax/modem to the motherboard's audio subsection. The mono-in and mono-out signal interface is necessary for telephony applications such as speakerphones and answering machines.

1.11.3 Wavetable Connector

An 8-pin header supports wavetable add-in cards. Most wavetable add-in cards are installed in a standard ISA slot; a cable is then routed from the card to the connector.

Compatible wavetable cards are available from several vendors. The ICS WaveFront and the CrystaLake Series 2000 wavetable product families offer general MIDI-compatible audio operation.

1.12 Motherboard Connectors

The following figure shows the connectors on the motherboard.

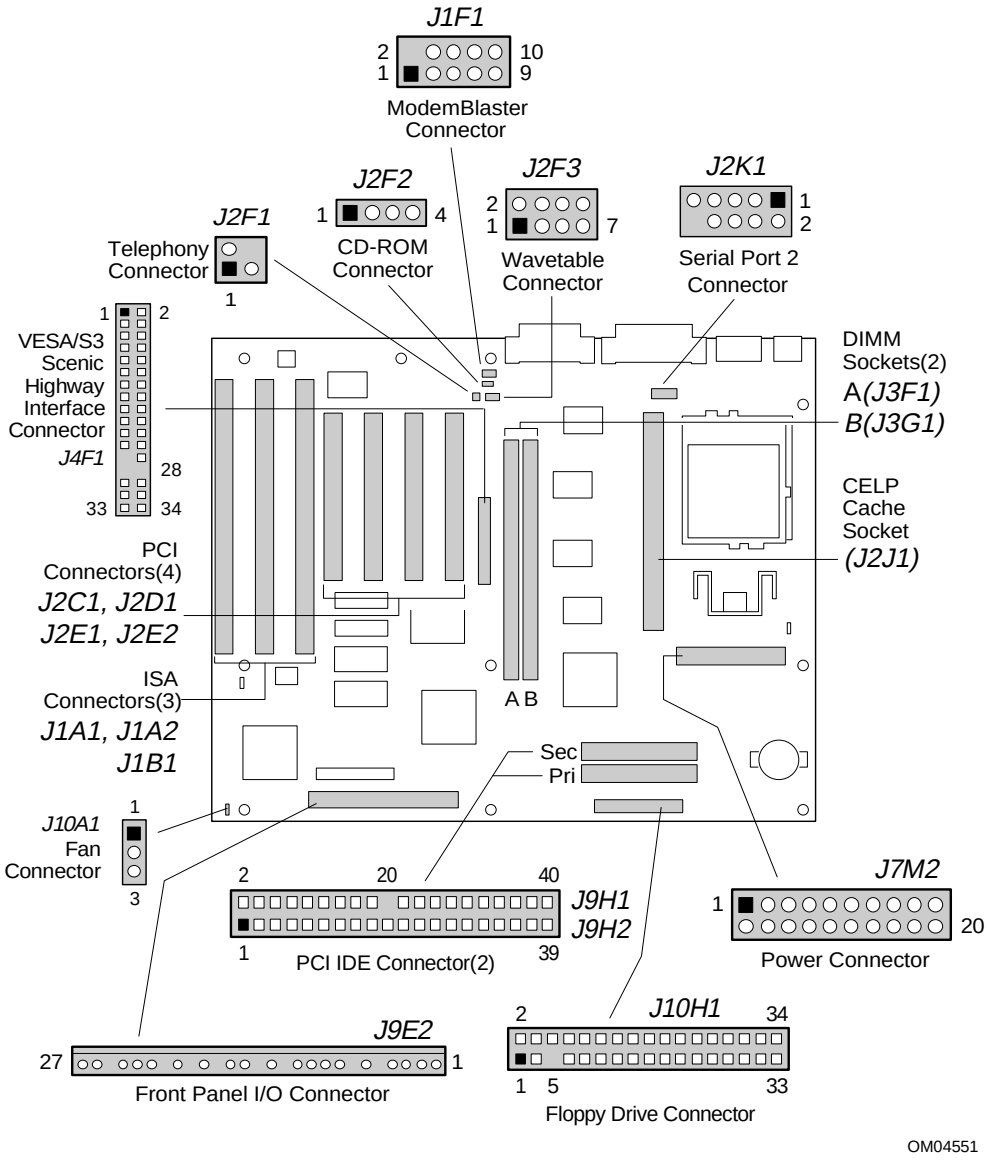

Figure 4. Motherboard Connectors

Table 2. Telephony Connector (J2F1)

Pin	Signal Name
1	Ground
2	Mono_in_MB
3	Mic_Tel
4	Key

Table 3. CD-ROM Audio Connector (J2F2)

Pin	Signal Name
1	Ground
2	CD_IN-Left
3	Ground
4	CD_IN-Right

Table 4. ModemBlaster Connector (J1F1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Key
3	Line_In_MB	4	Ground
5	Left Line Out	6	Ground
7	Right Line Out	8	Mono_In_MB
9	Ground	10	Mic_In_MB

Table 5. Wavetable Upgrade Connector (J2F3)

Pin	Signal Name	Pin	Signal Name
1	Wave In right	2	Ground
3	Wave In left	4	Ground
5	Key	6	Ground
7	No Connect	8	MIDI Out (from Host)

Note: This connector is a 2x4 male, 0.100” centerline stake header with 0.025” square pins. The mating connector is a Berg 71600-308 or equivalent.

Table 6. Serial Port 2 Connector (J2K1)

Pin	Signal Name	Pin	Signal Name
1	DCD	2	DSR#
3	Serial In#	4	RTS#
5	Serial Out#	6	CTS#
7	DTR#	8	RI
9	Ground	10	Key

Table 7. Fan Connector (J10A1)

Pin	Signal Name
1	Ground
2	+12 V
3	Ground

Table 8. Floppy Drive Connector (J10H1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN#
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	FDDS1# (Drive Select B)
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	FDM01# (Motor Enable B)
17	MSEN1	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	MSEN0	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 9. IDE Connectors (J9H1, J9H2)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select pullup)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	Address 1	34	Reserved
35	Address 0	36	Address 2
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

NOTE: Signal names in brackets ([ ]) are for the secondary IDE connector

1.12.1 Power Supply Connector

An ATX power supply supports remote power on/off through pin 14 of the power supply connector. This enables the motherboard to turn off system power through software control.

To enable soft-off control in software, advanced power management (APM) must be enabled in the Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer. For example, in the Windows 95 Start menu, the user selects Shutdown to turn off the power.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes the computer returns to the on or off state it was in before power was interrupted.

Table 10. Power Supply Connector (J7M2)

Pin	Signal Name
1	+3.3 V
2	+3.3 V
3	Ground
4	+5 V
5	Ground
6	+5 V
7	Ground
8	PWRGD (Power Good)
9	+5 VSB (Standby for real-time clock)
10	+12 V
11	+3.3 V
12	-12 V
13	Ground
14	PS-ON# (Power Supply remote On/Off control)
15	Ground
16	Ground
17	Ground
18	-5 V
19	+5 V
20	+5 V

Table 11. VESA/S3 Scenic Highway Interface Connector (J4F1)

Pin	Signal Name (Function)	Pin	Signal Name (Function)
1	DGND (Digital Ground)	2	FC0 (Pixel Data 0)
3	DGND (Digital Ground)	4	FC1 (Pixel Data 1)
5	DGND (Digital Ground)	6	FC2 (Pixel Data 2)
7	EVIDEO (External Video)	8	FC3 (Pixel Data 3)
9	ESYNC (External Sync)	10	FC4 (Pixel Data 4)
11	EDCLK (External Clock)	12	FC5 (Pixel Data 5)
13	SDA (not used)	14	FC6 (Pixel Data 6)
15	DGND (Digital Ground)	16	FC7 (Pixel Data 7)
17	DGND (Digital Ground)	18	PCLK (Pixel Clock)
19	DGND (Digital Ground)	20	BLANK#
21	DGND (Digital Ground)	22	HSYNC (Horizontal Sync)
23	SCL (not used)	24	VSYNC (Vertical Sync)
25	Key (no pin)	26	DGND (Digital Ground)
27	Key (no pin)	28	Key (no pin)
29	Ground	30	IICCLK (I^2C bus clock)
31	not used	32	IICDAT (I^2C bus data)
33*	GOP1/EN2 (Enable signal)	34*	GOP0/ENFEAT# (Enable signal)

* The signal name that applies to these pins is dependent on the operating mode of the graphics controller.

1.12.2 Front Panel Connectors

The front panel connector includes headers for these I/O connections:

- Speaker
- Reset switch
- Sleep LED
- Hard drive activity LED
- Infrared (IrDA) port
- Sleep switch
- Power switch

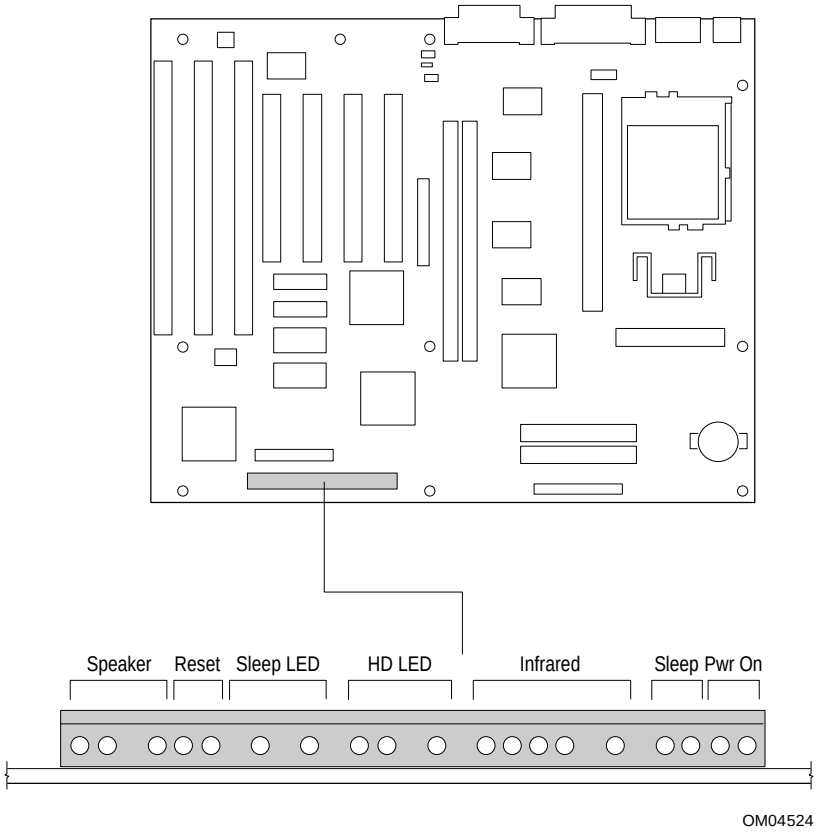

Figure 5. Front Panel I/O Connectors

Table 12. Front Panel I/O Connectors

Pin	Signal Name	Connector
1	SW_ON#	Power On
2	Ground	
3	SLEEP	Sleep/Resume
4	SLEEP_PU (pullup)	
5	No connect	none
6	+5 V	IrDA
7	Key	
8	IrRX	
9	Ground	
10	IrTX	
11	CONIR (Consumer IR)	
12	No connect	none
13	HD_PWR +5 V	HD LED
14	Key	
15	HD Active#	
16	HD_PWR	
17	No connect/Key	none
18	Ground	Sleep/Power LED
19	Key	
20	PWR_LED	
21	No connect/Key	none
22	Ground	Reset
23	SW_RST	
24	Ground	Speaker
25	Key	
26	PIEZO_IN	
27	SPKR_HDR	

1.12.2.1 Power On Connector

You can connect this header to a front panel power switch (a momentary contact, normally open switch). The switch must pull the SW_ON# pin to ground for at least 50 ms. to signal the power supply to switch on or off. (The time requirement is due to the motherboard's internal debounce circuitry.) To prevent double-clicking, at least two seconds must pass before the motherboard will recognize another on/off signal.

1.12.2.2 Sleep/Resume

When advanced power management (APM) is enabled in the system BIOS and the operating system's APM driver is loaded, the system can enter Sleep (Standby) mode in one of three ways:

- Optional front panel Sleep/Resume button
- Hot key defined in the BIOS Setup program
- Prolonged system inactivity; the default timeout is 10 minutes and can be changed in Setup

A Sleep/Resume button is supported by the 2-pin header located on the front panel I/O connector. The front panel Sleep/Resume switch must be a momentary SPST type that is normally open.

Closing the Sleep/Resume switch generates a System Management Interrupt (SMI) to the processor, which immediately goes into System Management Mode (SMM). While the system is in Sleep mode it is fully capable of responding to and servicing external interrupts (such as an incoming fax) even though the monitor turns on only if a keyboard or mouse interrupt occurs. To reactivate the system, or Resume, you must press the Sleep/Resume button again, or use the keyboard or mouse.

1.12.2.3 Infrared Connector

Serial Port 2 can be configured to support an IrDA module connected to this 6-pin header. After configuring the IrDA interface, you can transfer files to or from portable devices such as laptops, PDAs and printers using application software.

1.12.2.4 Hard Drive (HD) LED

You can connect this header to an LED to provide a visual indicator that data is being read from or written to an IDE hard drive. For the LED to function properly, the IDE drive must be connected to the onboard IDE controller on the motherboard.

1.12.2.5 Sleep/Power LED

You can connect this header to an LED that will light when the computer is powered on. This LED will also blink when the computer is in a power-managed state.

1.12.2.6 Reset

You can connect this header to a momentary SPST type switch that is normally open. When the switch is closed, the board resets and runs the POST.

1.12.2.7 Speaker

A speaker may be installed on the motherboard as a manufacturing option. The speaker option includes a jumper on pins 26-27 of the front panel connector. You can disable the onboard speaker by removing the jumper, and you can connect an offboard speaker in its place. The speaker (onboard or offboard) provides error beep code information during the Power-On Self Test (POST) in the event that the computer cannot use the video interface. The speaker is not connected to the audio subsystem, and does not receive output from the audio subsystem.

1.12.3 Back Panel Connectors

Figure 6 shows the location of the back panel I/O connectors, which include:

- PS/2-style keyboard and mouse connectors
- Two USB connectors
- One parallel port
- One serial port
- VGA† monitor connector
- MIDI/game port
- External audio jacks: Line In, Line Out, and Mic In

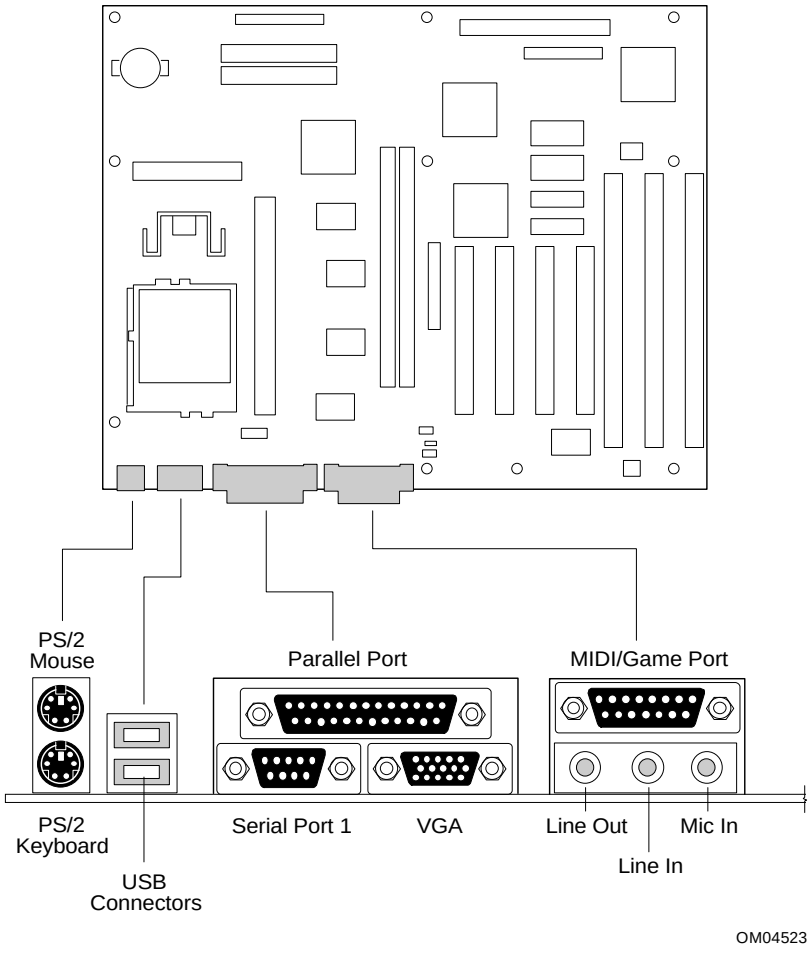

Figure 6. Back Panel I/O Connectors

Table 13. PS/2 Keyboard and Mouse Connectors

Pin	Signal Name
1	Data
2	No connect
3	Ground
4	+5 V (fused)
5	Clock
6	No connect

Table 14. USB Connectors

Pin	Signal Name
1	Power
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

Table 15. Parallel Port Connector

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data bit 0	15	Fault#
3	Data bit 1	16	INIT#
4	Data bit 2	17	SLCT IN#
5	Data bit 3	18	Ground
6	Data bit 4	19	Ground
7	Data bit 5	20	Ground
8	Data bit 6	21	Ground
9	Data bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Error	25	Ground
13	Select		

Table 16. Serial Port Connector

Pin	Signal Name
1	DCD
2	Serial In#
3	Serial Out#
4	DTR#
5	Ground
6	DSR#
7	RTS#
8	CTS#
9	RI

Table 17. VGA Video Monitor Connector

Pin	Signal Name
1	Red
2	Green
3	Blue
4	No connect
5	Ground
6	Ground
7	Ground
8	Ground
9	No connect
10	Ground
11	No connect
12	DDC Data
13	Horizontal Sync
14	Vertical Sync
15	DDC Clock

Table 18. MIDI/Game Port Connector

Pin	Signal Name
1	Joystick Vcc
2	JSButton0
3	JS_X1R
4	Ground
5	Ground
6	JS_Y1R
7	JSButton1
8	Joystick Vcc
9	Vcc
10	JSButton2
11	JS_X2R
12	MIDI_OUT
13	JS_Y2R
14	JSButton3
15	MIDI_IN

1.12.4 Add-in Board Expansion Connectors

The motherboard contains three PCI slots, two ISA slots and one shared slot (for a PCI or ISA card). The PCI bus supports up to four bus masters through the four PCI connectors (see Section 5.2 for information about compliance with the PCI specification).

Table 19. PCI Bus Connectors

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+5 V (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	no connect (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	PRSNT1#	A40	SDONE	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	SBO#	B41	+3.3 V
A11	Reserved	B11	PRSNT2#	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	Reserved	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	Reserved	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

* These signals (in parentheses) are optional in the PCI specification and are not implemented on this motherboard

Table 20. ISA Bus Connectors

Pin	Signal Name	Pin	Signal Name
B1	Ground	A1	IOCHK# (IOCHCK#)
B2	RESET (RESDRV)	A2	SD7
B3	+5 V	A3	SD6
B4	IRQ9	A4	SD5
B5	-5 V	A5	SD4
B6	DRQ2	A6	SD3
B7	-12 V	A7	SD2
B8	SRDY# (NOWS#)	A8	SD1
B9	+12 V	A9	SD0
B10	Ground	A10	IOCHRDY (CHRDY)
B11	SMEMW# (SMWTC#)	A11	AEN
B12	SMEMR# (SMRDC#)	A12	SA19
B13	IOW# (IOWC#)	A13	SA18
B14	IOR# (IORC#)	A14	SA17
B15	DACK3#	A15	SA16
B16	DRQ3	A16	SA15
B17	DACK1#	A17	SA14
B18	DRQ1	A18	SA13
B19	REFRESH#	A19	SA12
B20	BCLK	A20	SA11
B21	IRQ7	A21	SA10
B22	IRQ6	A22	SA9
B23	IRQ5	A23	SA8
B24	IRQ4	A24	SA7
B25	IRQ3	A25	SA6
B26	DACK2#	A26	SA5
B27	TC	A27	SA4
B28	BALE	A28	SA3
B29	+5 V	A29	SA2
B30	OSC	A30	SA1
B31	Ground	A31	SA0
Key		Key	
D1	MEMCS16# (M16#)	C1	SBHE#
D2	IOCS16# (IO16#)	C2	LA23
D3	IRQ10	C3	LA22

Note: Items in parentheses are alternate versions of signal names

continued ☛

Table 20. ISA Bus Connectors (continued)

Pin	Signal Name	Pin	Signal Name
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0#	C8	LA17
D9	DRQ0	C9	MEMR# (MRDC#)
D10	DACK5#	C10	MEMW# (MWTC#)
D11	DRQ5	C11	SD8
D12	DACK6#	C12	SD9
D13	DRQ6	C13	SD10
D14	DACK7#	C14	SD11
D15	DRQ7	C15	SD12
D16	+5 V	C16	SD13
D17	Master16# (MASTER#)	C17	SD14
D18	Ground	C18	SD15

Note: Items in parentheses are alternate versions of signal names

Table 21. CELP Connector for L2 Cache (J2J1)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Ground	41	D58	81	Ground	121	D59
2	TIO0	42	D56	82	TIO1	122	D57
3	TIO2	43	Ground	83	TIO7	123	Ground
4	TIO6	44	D54	84	TIO5	124	D55
5	TIO4	45	D52	85	TIO3	125	D53
6	TIO8	46	D50	86	TIO9	126	D51
7	Vcc3	47	D48	87	Vcc5	127	D49
8	TWE#	48	Ground	88	TIO10	128	Ground
9	CADS#/CAA3	49	D46	89	CADV#/CAA4	129	D47
10	Ground	50	D44	90	Ground	130	D45
11	CWE4#	51	D42	91	COE#	131	D43
12	CWE6#	52	Vcc3	92	CWE5#	132	Vcc5
13	CWE0#	53	D40	93	CWE7#	133	D41
14	CWE2#	54	D38	94	CWE1#	134	D39
15	Vcc3	55	D36	95	Vcc5	135	D37
16	CCS#/CAB4	56	Ground	96	CWE3#	136	Ground
17	GWE#	57	D34	97	CAB3	137	D35
18	BWE#	58	D32	98	CALE	138	D33
19	Ground	59	D30	99	Ground	139	D31
20	A3	60	Vcc3	100	RSVD	140	Vcc5
21	A7	61	D28	101	A4	141	D29
22	A5	62	D26	102	A6	142	D27
23	A11	63	D24	103	A8	143	D25
24	A16	64	Ground	104	A10	144	Ground
25	Vcc3	65	D22	105	Vcc5	145	D23
26	A18	66	D20	106	A17	146	D21
27	Ground	67	D18	107	Ground	147	D19
28	A12	68	Vcc3	108	A9	148	Vcc5
29	A13	69	D16	109	A14	149	D17
30	ADSP#	70	D14	110	A15	150	D15
31	ECS1#/(CS#)	71	D12	111	RSVD	151	D13
32	ECS2#	72	Ground	112	PD0	152	Ground
33	PD1	73	D10	113	PD2	153	D11
34	PD3	74	D8	114	PD4	154	D9
35	Ground	75	D6	115	Ground	155	D7
36	CLK1	76	Vcc3	116	CLK0	156	Vcc5
37	Ground	77	D4	117	Ground	157	D5
38	D62	78	D2	118	D63	158	D3
39	Vcc3	79	D0	119	Vcc5	159	D1
40	D60	80	Ground	120	D61	160	Ground

Note: This pinout meets the current specification for the COASt Flexible Cache Solution (see Section 5.2)

1.13 Jumper Settings

Figure 7 shows the location of jumper blocks on the motherboard.

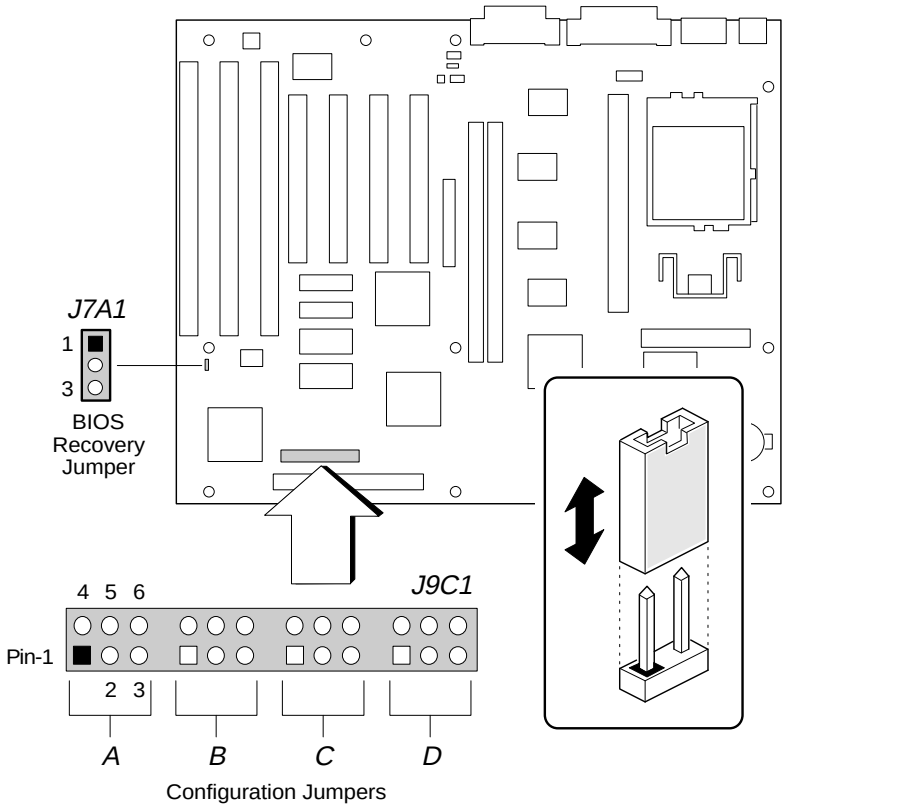

Figure 7. Jumper Locations

⚠ CAUTION

Do not move any of the jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing jumpers.

Table 22. Jumper Settings

Function	Jumper	Configuration
Password Clear	J9C1-A	1-2 Password enabled (**Default**) 2-3 Password clear/disabled
CMOS (NVRAM and ESCD) Clear	J9C1-A	4-5 Keep (**Default**) 5-6 Clear
CMOS Setup Access	J9C1-B	1-2 Access allowed (**Default**) 2-3 Access denied
Host Bus Frequency*	J9C1-C	See Table 23
Processor Frequency	J9C1-D	See Table 23
BIOS Recovery	J7A1	1-2 Normal operation (**Default**) 2-3 Recover BIOS

* These jumpers also set the PCI and ISA bus frequencies

1.13.1 Processor Configuration (J9C1-C, D)

The motherboard must be configured for the frequency of the installed processor. Table 23 shows the jumper settings for each frequency and the corresponding host bus, PCI bus, and ISA bus frequencies.

Table 23. Jumper Settings for Processor and Host Bus Frequencies

Processor Freq. (MHz)	Jumpers J9C1-C	Jumpers J9C1-D	Host Bus Freq. (MHz)	PCI Bus Freq. (MHz)	ISA Bus Freq. (MHz)	Bus/Processor Freq. Ratio
200	1-2 and 5-6	1-2 and 5-6	66	33	8.33	3
166	1-2 and 5-6	2-3 and 5-6	66	33	8.33	2.5
150	2-3 and 4-5	2-3 and 5-6	60	30	7.5	2.5
133	1-2 and 5-6	2-3 and 4-5	66	33	8.33	2
120	2-3 and 4-5	2-3 and 4-5	60	30	7.5	2
100	1-2 and 5-6	1-2 and 4-5	66	33	8.33	1.5
90	2-3 and 4-5	1-2 and 4-5	60	30	7.5	1.5
75	2-3 and 5-6	1-2 and 4-5	50	25	8.33	1.5
reserved	2-3 and 5-6	1-2 and 5-6				
reserved	2-3 and 5-6	2-3 and 4-5				
reserved	2-3 and 5-6	2-3 and 5-6				
reserved	2-3 and 4-5	2-3 and 5-6				
reserved	1-2 and 4-5	1-2 and 4-5				
reserved	1-2 and 4-5	1-2 and 5-6				
reserved	1-2 and 4-5	2-3 and 4-5				
reserved	1-2 and 4-5	2-3 and 5-6				

1.13.2 Password Clear (J9C1-A)

Use this jumper to clear the password if the password is forgotten. The default setting is pins 1-2, (password enabled). To clear the password, turn off the computer, move the jumper to pins 2-3, and turn on the computer. Then turn off the computer, and return the jumper to pins 1-2 to restore normal operation. If the jumper is in the 2-3 position (password disabled), you cannot set a password.

1.13.3 Clear CMOS (J9C1-A)

This jumper resets the CMOS settings to the default values. This procedure must be done each time the system BIOS is updated. The default setting for this jumper is pins 4-5 (keep CMOS settings). To reset the CMOS settings to the default values, turn off the computer, move the jumper to pins 5-6, then turn on the computer. When the computer displays the message "NVRAM cleared by jumper," turn off the computer and return the jumper to pins 4-5 to restore normal operation.

1.13.4 BIOS Setup Access (J9C1-B)

This jumper enables or disables access to the Setup program. The default setting is pins 1-2 (access enabled). To disable access to the Setup program, move the jumper to pins 2-3.

1.13.5 BIOS Recovery (J7A1)

This jumper lets you recover the BIOS data from a diskette in the event of a catastrophic failure. The default setting is pins 1-2 (normal operation). To recover the BIOS, turn off the computer, move the jumper to pins 2-3, then turn on the computer to perform BIOS recovery. After recovery, turn off the computer and return the jumper to pins 1-2 to restore normal operation. See Section 3.1.14 for more details.

1.14 Reliability

The Mean-Time-Between-Failures (MTBF) data is calculated from predicted data @ 55°C.

Motherboard MTBF: 80798 hours calculated

1.15 Environmental

Table 24. Motherboard Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40°C to +70°C		
Operating	0°C to +55°C (0oC to +45oC if an OverDrive processor is installed)		
Shock			
Unpackaged	50 G trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight	**Free Fall (inches)**	**Velocity Change (inches/sec)**
	<20 lbs	36	167
	21-40 lbs	30	152
	41-80 lbs	24	136
	81-100 lbs	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz : 0.02g² Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015g² Hz (flat)		
	40 Hz to 500 Hz : 0.015g² Hz sloping down to 0.00015 g² Hz		

1.16 Power Consumption

Tables 25 and 26 list voltage and current specifications for a computer that contains the motherboard, a 166 MHz Pentium processor, 32 MB RAM, 256 KB cache, 3.5-inch floppy drive, 800 MB IDE hard drive, and 4X IDE CD-ROM. This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 95 desktop mode are measured at 1024x768x256 colors and 70 Hz refresh rate. AC watts are measured with a typical 200W supply, nominal input voltage and frequency, with true RMS wattmeter at the line input.

Table 25. DC Voltage

DC Voltage	Acceptable Tolerance
+3.3 V	± 5%
+5 V	± 5%
+5 V SB (standby)	± 5%
-5 V	± 5%
+12 V	± 5%
-12 V	± 5%

Table 26. Power Usage

		DC (amps) at:				
Mode	**AC (watts)**	**+3.3 V**	**+5 V**	**-5 V**	**+12 V**	**-12 V**
DOS prompt, APM disabled	49.7	1.13	3.42	-.01	.1	-.03
Windows 95 desktop, APM disabled	51.1	.99	3.79	-.01	.1	-.03
Windows 95 desktop, APM enabled, in video sleep and IDE drive powered down mode.	32.7	.71	1.31	-.01	.1	-.03

1.16.1 Power Supply Considerations

For typical configurations, the motherboard is designed to operate with at least a 200W ATX power supply (see Section 5.2 for the specification). Use a higher wattage supply for heavily loaded configurations. The power supply must meet the following requirements:

- Rise time for power supply: 2 ms to 20 ms
- Minimum delay for Reset to Power Good: 100 ms
- Minimum Powerdown warning: 1 ms
- 3.3 V output must reach its minimum regulation level within ± 20 ms of the 5V output reaching its minimum regulation level

1.17 Regulatory Compliance

This printed circuit assembly complies with the following safety and EMI regulations when correctly installed in a compatible host system.

1.17.1 Safety

1.17.1.1 UL 1950 - CSA 950-95, 3rd edition, Dated 3-28-95

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA & Canada)

1.17.1.2 CSA C22.2 No. 950-93, 3rd Edition

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (Canada)

1.17.1.3 EN 60 950, 2nd Edition, 1992 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)

1.17.1.4 IEC 950, 2nd edition, 1991 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

1.17.1.5 EMKO-TSE (74-SEC) 207/94

Summary of Nordic deviations to EN 60 950. (Norway, Sweden, Denmark & Finland)

1.17.2 EMI

1.17.2.1 FCC Class B

Title 47 of the Code of Federal Regulations, Parts 2 & 15, Subpart B, pertaining to unintentional radiators. (USA)

1.17.2.2 CISPR 22, 2nd Edition, 1993

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)

1.17.2.3 EN 55 022, 1995

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)

1.17.2.4 EN 50 082-1 (1992)

Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)

1.17.2.5 VCCI Class 2 (ITE)

Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)

1.17.2.6 ICES-003, Issue 2

Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

1.17.3 Product Certification Markings

This printed circuit assembly has the following product certification markings:

- European CE Marking: Consists of a marking on the board or shipping container.
- UL Recognition Mark: Consists of the UL File No. E139761 on the component side of the board and the PBA No. on the solder side of the board. Board material flammability is 94V-1 or -0.
- Canadian Compliance: Consists of small c followed by a stylized backward UR on component side of board.

2 Motherboard Resources

NOTE

For more detailed information about the resources used for onboard audio, see the Audio Subsystem section in Chapter 1.

2.1 Memory Map

Table 27. Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 131072 K	100000 - 8000000	127 MB	Extended Memory
960 K - 1024 K	F0000 - FFFFF	64 K	AMI System BIOS
944 K - 960 K	EC000 - EFFFF	16 K	Main BIOS (available as UMB)
936 K - 944 K	EA000 - EBFFF	8 K	VPD ESCD (Plug and Play configuration)
932 K - 936 K	E9000 - E9FFF	4 K	Reserved for BIOS
928 K - 932 K	E8000 - E8FFF	4 K	OEM Logo or User Scan Flash (available as UMB)
896 K - 928 K	E0000 - E7FFF	32 K	POST BIOS (available as UMB)
800 K - 896 K	C8000 - DFFFF	96 K	Available High DOS memory (open to ISA and PCI bus)
640 K - 800 K	A0000 - C7FFF	160 K	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 K	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 K	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 K	Conventional memory

2.2 DMA Channels

Table 28. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Open
1	8- or 16-bits	Audio (default)
2	8- or 16-bits	Floppy Drive
3	8- or 16-bits	Parallel Port
4		Reserved - Cascade Channel
5	16-bits	Audio (default)
6	16-bits	Open
7	16-bits	Open

2.3 I/O Map

Table 29. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX3 - DMA 1
0020 - 0021	2 bytes	PIIX3 - Interrupt Controller 1
0040 - 0043	4 bytes	PIIX3 - Counter/Timer 1
0060	1 byte	Keyboard Controller Byte - Reset IRQ
0061	1 byte	PIIX3 - NMI, Speaker Control
0064	1 byte	Keyboard Controller, CMD/STAT Byte
0070, bit 7	1 bit	PIIX3 - Enable NMI
0070, bits 6:0	7 bits	PIIX3 - Real Time Clock, Address
0071	1 byte	PIIX3 - Real Time Clock, Data
0080 - 008F	16 bytes	PIIX3 - DMA Page Register
0094 - 009F	12 bytes	PIIX3 - DMA Page Register
00A0 - 00A1	2 bytes	PIIX3 - Interrupt Controller 2
00C0 - 00DE	31 bytes	PIIX3 - DMA 2
00EA - 00EB	2 bytes	Motherboard Resources
00F0 - 00FF	16 bytes	Numeric Data Processor
0170 - 0177	8 bytes	Secondary IDE Channel
01F0 - 01F7	8 bytes	Primary IDE Channel
0200 - 0207	8 bytes	Audio / Game Port
0213	1 byte	PnP Read Data Port
0220 - 022F	16 bytes	Audio Vibra16C Base
0270 - 0273	4 bytes	I/O port for Plug and Play
0279	1 byte	PnP Address Port
02F8 - 02FF	8 bytes	COM2
0330 - 0331	2 bytes	MPU-401 (MIDI)
0376	1 byte	Secondary IDE Channel Command Port
0378 - 037B	4 bytes	LPT1
0388- 038B	4 bytes	Audio - FM synthesizer
03B0 - 03BB	12 bytes	S3 Trio64 V+
03C0 - 03DF	32 bytes	S3 Trio64 V+
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 byte	Primary IDE Channel Command Port
03F7 (Write)	1 byte	Floppy Channel 1 Command
03F7, bit 7	1 bit	Floppy Disk Change Channel 1
03F7, bits 6:0	7 bits	Primary IDE Channel Status Port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC

continued ☛

Table 29. I/O Map (continued)

Address (hex)	Size	Description
LPT*n* + 400h	8 bytes	ECP port, LPT*n* base address + 400h
0A79	1 byte	PnP Write Data Port
0CF8 - 0CFB*	4 bytes	PCI Configuration Address Register
0CF9**	1 byte	Turbo and Reset Control Register
0CFC - 0CFF	4 bytes	PCI Configuration Data Register
FF00 - FF07	8 bytes	IDE Bus Master Register
FFA0 - FFA7	8 bytes	Primary Bus Master IDE Registers
FFA8 - FFAF	8 bytes	Secondary Bus Master IDE Registers

* DWORD access only

** Byte access only

NOTE

See the Audio section(s) in Chapter 1 for specific I/O addresses that can be used by the audio components on your motherboard. This table does not list I/O addresses that may be used by add-in cards in the system.

2.4 Port 80 POST Codes

During POST (power-on self test), the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires the use of an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

The following table provides the POST codes that can be generated by the motherboard's BIOS. Some codes are repeated in the table because that code applies to more than one operation.

Table 30. Port 80 Codes

Code	Description of POST Operation Currently In Progress
000	Give control to ROM in Flash - execute boot.
000	Execute boot.
002	Disable internal cache. Keyboard controller test.
008	Disable DMA controller #1, #2. Disable interrupt controller #1, #2. Reset video display.
00D	Check for signature of the board manufacturing company.
00D	If default jumper is set, go to Load CMOS Default.
00E	Check the validity of CMOS - if there is anything wrong or invalid, force to default.
00F	Load default CMOS settings.

continued ☛

Table 30. Port 80 Codes (continued)

Code	Description of POST Operation Currently In Progress
010	Clear error register, clear CMOS pending interrupt, check and set clock rate, check and set base memory size 512 KB of 640 KB.
010	If base memory size is 640 KB, allocate extended BIOS data area (EBDA) - otherwise, calculate the EBDA.
010	Set up overlay environment. Update setupFlags with current operating environment. Initialize interrupt vector pointing to the error handlers, Update setupFlags in EBDA. Initialize CMOS pointers in EBDA.
013	Program all chipset registers.
015	Initialize system timer.
01B	Go to real memory base 64 KB test.
020	16 KB base RAM Test.
023	Hook made available prior to initializing the interrupt vector table.
023	Set up interrupt vectors.
024	Initialize and load interrupt vectors.
025	Video rows initialization.
028	Set monochrome mode.
029	Set color display - color mode set.
02A	Clear parity status if any.
02B	Initialization required internal to some chipset before video initialization. Custom video initialization.
02C	Test optional video ROM.
02D	Initialize registers internal to chipset after video initialization.
02E	Check for video ROM.
02F	Display memory read/write test.
030	Test video horizontal and vertical tracing.
031	Display video memory read/write test.
032	Test video horizontal and vertical tracing - Beep if no video controller installed. Check for MDA.
034	Set up video configuration (column x row). Display copyright message.
036	Initialize messaging services. Clear the screen.
037	Display the first screen signon.
039	Update screen pointer. Display setup message. Display keyboard signon. Display mouse signon.
040	Memory test starting segment at 00000.
043	Calculate the memory size left to be tested.
04F	Disable caching, etc. Check if the system memory size is larger than zero. Test and initialize to zero all DRAM. Remap memory partition if necessary. Test one MB of memory. Update counter on screen. Repeat memory test for each MB of memory until done.
052	ChipsetAdjustMemorySize - Adjust any base of extended memory size because of chipset.
061	Test DMA master page registers.
062	Test DMA slave page registers.

continued ☛

Table 30. Port 80 Codes (continued)

Code	Description of POST Operation Currently In Progress
065	Program DMA controllers.
066	Clear DMA write control registers.
067	Unmask timer and NMI. Update master mask register.
080	Run keyboard detection. Run mouse detection.
080	Read interrupt mask - setup diskette ISR, #2, keyboard, and timer.
081	8042 interface test - Enable keyboard interrupt if keyboard is detected.
082	Enable interrupt.
083	Check and set keyboard lock bit.
088	Floppy unit initialization - Floppy controller and data setup.
08C	Set up interface between the BIOS POST and the device initialization management (DIM).
08F	Read interrupt mask. Unmask floppy interrupt. Setup floppy controller and data setup.
092	Set up COM port and LPT port timeout values. Display wait message if setup key is pressed.
096	Clear to bottom of the screen - Perform chipset initialization required before option ROM scans. Give control to ROM in Flash.
097	Verify and give control to optional ROM.
098	Perform any chipset initialization required after option ROM scans - give control to ROM in Flash.
09A	Adds MP entries for buses, I/O APIC, I/O INTRs, and LINTs.
09D	Timer data area initialization - set time and date.
0A0	Set up printer base addresses.
0A0	Enable internal cache.
0A1	Set COM base addresses - keyboard stuck key check.
0A2	Reset floating point unit.
0A3	Log and display POST errors if any. Check if manufacturing mode - if there are POST errors, display setup key and boot key options.
0A6	Call Setup program if setup was requested.
0A7	Load and wait for the valid password - unmask INT-0A redirection.
0AB	Custom floating point unit initialization.
0AC	Initialize internal floating point unit.
0AD	Update CMOS with floating point unit presence.
0AD	A fatal error results in a continuous echo of ‘DEAD’ to port 80h - echo ‘DE’ (wait 1 sec.), echo ‘AD’ (wait 1 sec.).
0AE	Set typematic rate.
0AF	Read keyboard ID.
0B0	Process POST errors.
0B1	Test cache memory.
0B3	Set up display mode (40x25, 80x25).
0B4	Jump to PreOS (pre-operating system) module.

continued ☛

Table 30. Port 80 Codes (continued)

Code	Description of POST Operation Currently In Progress
0BB	Perform work before registers and circular keyboard buffer are cleared just prior to INT 19h. Reinitialize message services. Initialize APM. Perform post SMI initialization. Circumvents EMM386's attempts to utilize the lower 32 KB area base.
0BB	Fix CMOS Read and CMOS Write so that every call does not set NMI off. Shadow product information in the compatibility segment. Give a beep for boot. Handle chipset specific manipulation before boot. Check keyboard for data before MP manipulation.
0D0	Initialize DS, ES, GS, and FS. Check if keyboard system bit is set. Check whether a hard or soft reset has occurred.
0D1	Power on initialization Initialize special chipsets in power on/hard reset. Check cache size and type, write reserved cache size information to CMOS, determine processor speed (optional).
0D2	Disable NMI reporting.
0D3	Reset video adapter.
0D4	If the microprocessor is in protected mode, load GDT 4G segment - ChipsetPreInit(), Disable L1 and L2 cache, perform any initialization required before the main chipset configuration is done.
0D5	System validity check. Calculate checksum.
0D6	Provides ability to do any special chipset initialization required before keyboard controller testing can begin.
0D7	Flush the keyboard input buffer.
0D8	Issue keyboard BAT command.
0D9	Retrieve 8042 KBC output buffer.
0DA	If keyboard initialization failed, display error message and halt.
0DB	Provide ability to do any special chipset initialization after KBC test.
0DD	Initialize keyboard controller command byte.
0DE	A fatal error results in a continuous echo of 'DEAD' to port 80h - echo 'DE' (wait 1 sec.), echo 'AD' (wait 1 sec).
0DF	Disable master/slave DMA controllers.
0E0	Initialize master/slave programmable interrupt controllers.
0E1	ChipsetInit - Preset any defaults needed to chipset registers.
0E1	Start the refresh timer(s) running.
0E1	Size all L2/L3 Cache (if present/required).
0E1	Detect EDO memory module (SIMM or DIMM).
0E1	Size memory partition boundaries.
0E1	Disable all memory holes.
0E1	The 512-640 KB must be DRAM mapped.
0E1	Gate A20 must be set and left set for POST.
0E2	Initialize timer channel 2 for speaker.
0E3	Initialize timer channel 0 for system timer.
0E4	Clear pending parity errors - disable and clear parity, reactivate parity.
0E5	Enter flat mode.

continued ☛

Table 30. Port 80h Codes (continued)

Code	Description of POST Operation Currently In Progress
0E6	Test the first 2 MB of system memory.
0E7	Get minimum memory partition size and test memory.
0E8	Remap DIMMs if failure detected and remapping supported.
0E8	Display error message and halt if remapping not supported.
0E9	After memory test, clear pending parity errors. Disable and clear parity, set bits to reactivate parity.
0EA	Set up stack for POST, enable enhanced POST, shadow FE00h block.
0EB	Look for the location of dispatcher in the packing list.
0EB	Call decompression dispatcher Init function.
0EC	Make F000h DRAM R/W enabled, force use of EDI.
0ED	Actively dispatch BIOS.
0F0	Initialize I/O cards in slots.
0F1	Enable extended NMI sources.
0F2	Test extended NMI sources.
0F3	Display EISA error message if any. Get keyboard controller vendor, program the keyboard controller.
0F4	Enable extended NMI sources.
0F5	Initialize mouse.

Note: Some port 80 codes are listed more than once because they test multiple functions. For example code 0EBh tests both of the following:
Look for the location of dispatcher in the packing list.
Call decompression dispatcher Init function.

2.5 PCI Configuration Space Map

Table 31. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82437VX (TVX)
00	07	00	Intel 82371FB (PIIX3) PCI/ISA bridge
00	07	01	Intel 82371FB (PIIX3) IDE Bus Master
00	07	02	Intel 82371FB (PIIX3) USB
00	08	00	Video (S3 Trio64 V+)*
00	0D	00	PCI Expansion Slot: J2E2
00	0E	00	PCI Expansion Slot: J2E1
00	0F	00	PCI Expansion Slot: J2D1
00	10	00	PCI Expansion Slot: J2C1

* Only on motherboards with the video manufacturing option.

2.6 Interrupts

Table 32. Interrupts

IRQ	System Resource
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard Buffer Full
2	Reserved, Cascade Interrupt From Slave PIC
3	COM2*
4	COM1*
5	Audio
6	Floppy Drive
7	LPT1*
8	Real Time Clock
9	User available
10	User available
11	User available
12	Onboard Mouse Port (if present, else user available)
13	Reserved, Math Coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ

2.7 PCI Interrupt Routing Map

The PCI specification allows for sharing of interrupts between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the normal operation or throughput of the devices. However, in some special cases where maximum performance is needed from a device, you may want to ensure that it does not share an interrupt with other PCI devices.

This section describes the interrupt sharing mechanism and how the interrupt signals are connected between the motherboard's PCI expansion slots and onboard PCI devices. Use this information to avoid sharing an interrupt for a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX3 PCI-to-ISA bridge has four Programmable Interrupt Request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt. Table 33 lists the PIRQ signals and shows how the signals are connected to the PCI expansion slots and to onboard PCI interrupt sources.

Table 33. PCI Interrupt Routing Map

PIIX3 PIRQ Signal	First PCI Expansion Slot: J2E2	Second PCI Expansion Slot: J2E1	Third PCI Expansion Slot: J2D1	Fourth PCI Expansion Slot: J2C1	Onboard Video	USB
PIRQA	INTA	INTD	INTC	INTB		
PIRQB	INTB	INTA	INTD	INTC		
PIRQC	INTC	INTB	INTA	INTD		
PIRQD	INTD	INTC	INTB	INTA	X	X

For example, assume that you plug an add-in card that has one interrupt (group INTA) into the fourth PCI slot. In this slot, an interrupt source from group INTA connects to the PIRQD signal, which is already connected to the onboard video and USB PCI sources. The add-in card shares an interrupt with these onboard interrupt sources.

Now, however, plug an add-in card that has one interrupt (group INTA) into the first PCI slot. Plug a second add-in card that has two interrupts (groups INTA and INTB) into the second PCI slot. INTA in the first slot is connected to signal PIRQA. INTA in the second slot is connected to signal PIRQB, and INTB is connected to signal PIRQC. With no other cards added, the three interrupt sources on the first two cards each have a PIRQ signal to themselves. Typically, they will not share an interrupt.

NOTE

The PIIX3 can connect each PIRQ line internally to one of the IRQ signals (3,4,5,7,9,11,14,15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

3 BIOS and Setup Utility

3.1 Introduction

The motherboard uses an Intel BIOS, which is stored in Flash EEPROM and can be upgraded using a floppy disk-based program. In addition to the BIOS, the Flash EEPROM contains the Setup program, Power-On Self Tests (POST), advanced power management (APM), the PCI auto-configuration utility, and Windows 95-ready Plug and Play. See Section 5.2 for the supported versions of these specifications.

This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a sign-on message during POST identifying the type of BIOS and a five-digit revision code. The initial production BIOS on the motherboard is identified as 1.00.0x.CY0.

Information on BIOS functions can be found in the *IBM PS/2 and Personal Computer BIOS Technical Reference* published by IBM, and the *ISA and EISA Hi-Flex AMIBIOS Technical Reference* published by AMI. Both manuals are available at most technical bookstores.

3.1.1 BIOS Flash Memory Organization

The Intel PA28FB200BX 2 Mbit Flash component is organized as 256K x 8 (256 KB). The Flash device is divided into areas as described in Table 34. The table shows the addresses in the ROM image in normal mode (the addresses change in BIOS Recovery Mode).

Table 34. Flash Memory Organization

System Address (Hex)	Size	Description
FFFF0000 - FFFFFFFF	64 KB	Main BIOS*
FFFEC000 - FFFEFFFF	16 KB	Boot Block
FFFEA000 - FFFEBFFF	8 KB	VPD ESCD (DMI configuration data / Plug and Play data)
FFFE9000 - FFFE9FFF	4 KB	Reserved for BIOS
FFFE8000 - FFFE8FFF	4 KB	OEM logo or Scan User Flash Area
FFFE0000 - FFFE7FFF	32 KB	Post BIOS (available as UMB)
FFFD0000 - FFFDFFFF	64 KB	Reserved for BIOS
FFFC0000 - FFFCFFFF	64 KB	Reserved for BIOS

* At runtime, only this section is shadowed into RAM below the 1 MB address.

3.1.2 BIOS Upgrades

Flash memory simplifies distributing BIOS upgrades. You can install a new version of the BIOS from a diskette. BIOS upgrades are available to be downloaded from the secure section on the Intel bulletin board or from Intel's FTP or World Wide Web sites (see Section 5.1).

The disk-based Flash upgrade utility, FMUP.EXE, has three options for BIOS upgrades:

- Update the Flash BIOS from a file on a disk
- Copy the current BIOS code from the Flash EEPROM to a disk file as a backup, in the event that an upgrade cannot be successfully completed
- Compare the BIOS in the Flash device with a file to make sure the system has the correct version

The upgrade utility ensures that the upgrade BIOS extension matches the target system to prevent accidentally installing a BIOS for a different type of system.

3.1.3 Plug and Play: PCI Auto-configuration

The PCI auto-configuration utility operates in conjunction with the Setup program to let you insert and remove PCI cards without user configuration (Plug and Play). When you turn on the system after adding a PCI card, the BIOS automatically configures interrupts, I/O space, and other parameters. Any interrupts set to "available" in Setup are considered free for use by PCI add-in cards. PCI interrupts are distributed to available ISA interrupts that have been not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is nondeterministic. An ISA device cannot share an interrupt allocated to PCI.

PCI system configuration information is stored in ESCD format. You can clear the ESCD data by moving the CMOS Clear jumper (see Section 1.13.3).

For information about the version of PCI and Plug and Play supported by this BIOS, see Section 5.2. You can obtain copies of the specifications from the Intel World Wide Web site (see Section 5.1). Peer-to-peer hierarchical PCI Bridge is supported, and by using an OEM-supplied option ROM or TSR, a PCI-to-PCMCIA bridge capability is possible as well.

3.1.4 PCI IDE Support

If you select "Autoconfiguration" in Setup, the BIOS automatically sets up the two local bus IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to PIO Mode 4 and recognizes any ATAPI devices, including CD-ROM drives and tape drives. The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in Setup. The ATAPI Specification recommends that ATAPI devices be configured as shown in Table 35.

Table 35. Recommendations for Configuring an ATAPI Device

	Primary Cable		Secondary Cable	
	Drive 0	Drive 1	Drive 0	Drive 1
Normal, no ATAPI	ATA			
Disk and CD-ROM for enhanced IDE systems	ATA		ATAPI	
Legacy IDE System with only one cable	ATA	ATAPI		
Enhanced IDE with CD-ROM and a tape or two CD-ROMs	ATA		ATAPI	ATAPI

3.1.5 ISA Plug and Play

If you select in Setup to boot with a Plug and Play OS (see Section 3.2.10.2), the BIOS auto-configures only ISA Plug and Play cards that are required for booting (IPL devices). If you select to not boot with a Plug and Play OS, the BIOS auto-configures all Plug and Play ISA cards.

3.1.6 ISA Legacy Devices

Since ISA legacy devices are not auto-configurable, the resources for them must be reserved. You can reserve resources in the Setup program or with an ISA configuration utility (see Section 5.1 for a Web site address).

System configuration information is stored in ESCD format. You can clear the ESCD data by moving the CMOS Clear jumper (see Section 1.13.3).

3.1.7 Desktop Management Interface

Desktop Management Interface (DMI) is a method of managing computers in an enterprise. The main component of DMI is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using DMI, a system administrator can obtain the system types, capabilities, operational status, installation date and other information about the system components. The DMI specification requires that certain information about the system's motherboard be made available to an applications program. This information is located in a series of data structures which are accessed in various ways by the DMI service layer. Component instrumentation allows the service layer to gain access to information stored in the general-purpose area of non-volatile RAM. The MIF database defines the data and provides the method for accessing the information.

The BIOS support for DMI enables the maximum benefit from applications such as LANDesk® Client Manager from Intel. The BIOS stores and can report on the following types of DMI information:

- BIOS data, such as the BIOS revision level
- Fixed system information, such as data about the motherboard, peripherals, serial numbers, and asset tags, etc.
- System information discovered during bootup, such as memory size, cache size, processor speed, etc.

An OEM can use a utility that makes DMI calls to program system and chassis-related information into the Flash memory, so the BIOS can also report that information. Once this information is written, it is locked (read-only).

Intel can provide a utility for making DMI calls to the BIOS. Contact your local Intel Sales office for further information. The latest DMI specification is available from Intel (see Section 5.1) and other sites.

DMI does not work directly under non-Plug and Play operating systems (e.g., Windows NT). However, the BIOS supports a DMI table interface for such OSs. Using this support, a DMI service-level application running on a non-Plug and Play OS can access the DMI BIOS information.

3.1.8 Advanced Power Management

The BIOS supports Advanced Power Management (APM); see Section 5.2 for the version supported. You can initiate the energy saving Standby mode in these ways:

- Optional front panel Sleep/Resume button
- Hot key defined in the BIOS Setup program
- Prolonged system inactivity; the default timeout is 10 minutes and can be changed in Setup

When in Standby mode, the motherboard reduces power consumption by using the processor's System Management Mode (SMM) capabilities and by spinning down hard drives and reducing power to or turning off VESA DPMS-compliant monitors. In Setup you can select the DPMS mode to use for the monitor: Standby, Suspend, Sleep, or Disabled (see Section 3.2.9.3).

While in Standby mode, the system retains the ability to respond to external interrupts; it can service requests such as incoming faxes or network messages while unattended. Any keyboard or mouse activity brings the system out of Standby mode and immediately restores power to the monitor.

APM is enabled in the BIOS by default; however, the system must be configured with an OS-dependent APM driver for the power-saving features to take effect. For example, Windows 95 enables APM automatically upon detecting the presence of the APM BIOS.

3.1.9 Language Support

The BIOS Setup utility and help messages can be supported in 32 languages. Five languages are available at this time: American English, German, Italian, French, and Spanish. The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

The default language is American English, which is always present unless another language is programmed into the BIOS using the Flash Memory Update Program (FMUP.EXE). See Section 5.1 for information about downloading FMUP and other utilities.

3.1.10 Boot Options

Booting from CD-ROM is supported in adherence to the "El Torito" bootable CD-ROM format specification developed by Phoenix Technologies and IBM. Under the Boot Options field in Setup, CD-ROM is one of four possible boot devices, which are defined in priority order. The default setting is for the floppy drive to be the primary boot device and the hard drive to be the secondary boot device. (By default the third and fourth devices are disabled.) If you select CD-ROM as the boot device, it must be the first device.

NOTE

A copy of the "El Torito" specification is available on the Phoenix Web site http://www.ptltd.com/techs/specs.html.

In Setup you can also select the network as a boot device, which allows booting from a network add-in card with a remote boot ROM installed.

3.1.11 OEM Logo or Scan Area

The motherboard supports a 4 KB programmable Flash user area at memory location E8000-E8FFF. You can use this area to display a custom OEM logo during POST, or can insert a binary image that executes at certain times during the POST. A utility is available from Intel to assist with installing a logo into Flash for display during POST. Contact your local Intel Sales office for further information.

3.1.12 USB Support

The USB connectors on the motherboard allows you to attach any of several USB devices as they become available. Typically, the device driver for USB devices will be managed by the OS. However, because keyboard and mouse support may be needed in the Setup program before the OS boots, the BIOS supports USB keyboards and mice. You can disable this support if necessary.

3.1.13 BIOS Setup Access Jumper

You can move the Setup Access jumper on the motherboard to enable or disable access to the Setup utility. The default is for access to be enabled. See Section 1.13.4 for the specific pins on which to place the jumper.

3.1.14 Recovering BIOS Data

Some types of failure can destroy the BIOS data. For example, the data could be lost if a power outage occurs while your are updating the BIOS in Flash memory. You can recover the BIOS data from a diskette by changing the setting of the BIOS Recovery jumper (see Section 1.13.5).

To create a BIOS recovery diskette, you must make a bootable DOS diskette and place the recovery files on it. The recovery files are available from Intel; contact your local Intel Sales office for further information.

To recover the BIOS, turn off the computer and move the jumper to the BIOS recovery setting. Insert the bootable BIOS recovery diskette in drive A:. Boot the computer to recover the BIOS. Two beeps and the end of floppy access to drive A: indicate a successful BIOS recovery. A series of continuous beeps indicates that the recovery operation failed.

NOTE

No video is displayed during the recovery process.

After a successful recovery, turn off the computer and return the jumper to the original pins to restore normal operation.

3.2 BIOS Setup Program

The Setup program lets you modify the configuration for most basic changes without opening the system. Setup is accessible only during the Power-On Self Test (POST). To enter Setup, press the <F1> key after the POST memory test has begun and before boot begins. By default, there is a prompt to press the <F1> key to access Setup, but this prompt may be disabled . See Section 1.13.4 for information on placing the jumper that prevents user access to Setup for security purposes.

3.2.1 Overview of the Setup Menu Screens

Table 36 lists the screens displayed by the Setup utility. Setup initially displays the Main menu screen. In each screen there are options for modifying the system configuration. Select a menu screen by pressing the left <←> or right <→> arrow keys. Use the up <↑> or down <↓> arrow keys to select items in a screen. Use the <Enter> key to select an item for modification. For certain items, pressing <Enter> brings up a subscreen. After you have selected an item, use the arrow keys to modify the setting.

Table 36. Overview of the Setup Menu Screens

Setup Menu Screen	**Description**
Main	Set up and modify some of the basic options of a PC, such as time, date, diskette drives, and hard drives.
Advanced	Modify the more advanced features of a PC, such as peripheral configuration and advanced chipset configuration.
Security	Specify passwords that can be used to limit access to the system.
Exit	Save or discard changes.
Setup Subscreen	**Description**
Floppy Options	Configure diskette drives.
Primary/Secondary IDE Device Configuration	Configure IDE devices such as hard disk drives.
Boot Options	Modify options that affect the system boot up, such as the boot sequence.
Peripheral Configuration	Modify options that affect the serial ports, the parallel port, disk drive interfaces, and USB.
Advanced Chipset Configuration	Modify options that affect memory and system buses.
Power Management Configuration	Access and modify Advanced Power Management (APM) options.
Plug and Play Configuration	Modify options that affect the system's Plug and Play capabilities.

3.2.2 Main BIOS Setup Screen

This section describes the Setup options found on the main menu screen. If you select certain options from the main screen (e.g., Floppy Options), Setup switches to a subscreen for the selected option.

3.2.2.1 System Date

Specifies the current date. Select the month, day, and year from a pop-up menu.

3.2.2.2 System Time

Specifies the current time.

3.2.2.3 Floppy Options

When selected, this displays the Floppy Options menu.

3.2.2.4 Primary IDE Master

Reports if an IDE device is connected to the Primary IDE master interface. When selected, this displays the IDE Device Configuration subscreen.

3.2.2.5 Primary IDE Slave

Reports if an IDE device is connected to the Primary IDE slave interface. When selected, this displays the IDE Device Configuration subscreen.

3.2.2.6 Secondary IDE Master

Reports if an IDE device is connected to the Secondary IDE master interface. When selected, this displays the IDE Device Configuration subscreen.

3.2.2.7 Secondary IDE Slave

Reports if an IDE device is connected to the Secondary IDE slave interface. When selected, this displays the IDE Device Configuration subscreen.

3.2.2.8 Language

Specifies the language of the text strings used in the Setup utility and the BIOS. The options are any installed languages.

3.2.2.9 Boot Options

When selected, this displays the Boot Options subscreen.

3.2.2.10 Video Mode

Reports the video mode. There are no options.

3.2.2.11 Mouse

Reports if a mouse is installed or not. There are no options.

3.2.2.12 Base Memory

Reports the amount of base memory. There are no options.

3.2.2.13 Extended Memory

Reports the amount of extended memory. There are no options.

3.2.2.14 BIOS Version

Reports the BIOS identification string. There are no options.

3.2.3 Floppy Options Subscreen

3.2.3.1 Floppy A:

Reports if a diskette drive is connected to the system. There are no options.

3.2.3.2 Floppy B:

Reports if a second diskette drive is connected to the system. There are no options.

3.2.3.3 Floppy A: Type

Specifies the physical size and capacity of the diskette drive. The options are:

- Disabled
- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.44/1.25 MB, 3.5-inch (default)
- 2.88 MB, 3.5-inch

3.2.3.4 Floppy B: Type

Specifies the physical size and capacity of the diskette drive. The options are:

- Disabled (default)
- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.44/1.25 MB, 3.5-inch
- 2.88 MB, 3.5-inch

3.2.3.5 Floppy Access

Specifies the access rights for all attached floppy drives. The options are:

- Read/Write (default)
- Read Only

3.2.4 Primary/Secondary IDE Master/Slave Configuration Subscreens

There are four subscreens used to enable IDE devices:

- Primary IDE Master
- Primary IDE Slave
- Secondary IDE Master
- Secondary IDE Slave

All four subscreens contain the same eight fields described below.

3.2.4.1 IDE Device Configuration

Used to manually configure the hard drive or have the system auto-configure it. The options are:

- Auto Configured (default)
- User Definable
- Disabled

If you select User Definable, you can modify the Number of Cylinders, Number of Heads, and Number of Sectors items. If you select Disabled, the BIOS will not scan for a device on that interface.

3.2.4.2 Number of Cylinders

If IDE Device Configuration is set to Auto Configured, this field reports the number of cylinders for your hard disk and cannot be modified. If IDE Device Configuration is set to User Definable, you must type the correct number of cylinders for your hard disk.

3.2.4.3 Number of Heads

If IDE Device Configuration is set to Auto Configured, this field reports the number of heads for your hard disk and cannot be modified. If IDE Device Configuration is set to User Definable, you must type the correct number of heads for your hard disk.

3.2.4.4 Number of Sectors

If IDE Device Configuration is set to Auto Configured, this field reports the number of sectors for your hard disk and cannot be modified. If IDE Device Configuration is set to User Definable, you must type the correct number of sectors for your hard disk.

3.2.4.5 Maximum Capacity

Reports the maximum capacity of your hard disk, which is calculated from the number of cylinders, heads, and sectors. There are no options.

3.2.4.6 IDE Translation Mode

Specifies the IDE translation mode. The options are:

- Standard CHS (standard cylinder head sector, for drives with fewer than 1024 cylinders)
- Logical Block (LBA)
- Extended CHS (extended cylinder head sector, for drives with more than 1024 cylinders)
- Auto Detected (BIOS detects IDE drive support for LBA) (default)

⚠ CAUTION

Do not change the IDE translation mode from the option selected when the hard drive was formatted. Changing the option after formatting can result in corrupted data.

3.2.4.7 Multiple Sector Setting

Sets the number of sectors transferred by an IDE drive per interrupt generated. The options are:

- Disabled
- 4 Sectors/Block
- 8 Sectors/Block
- Auto Detected (default)

Check the specifications for your hard disk drive to determine which setting provides optimum performance for your drive.

3.2.4.8 Fast Programmed I/O Modes

Sets how fast the transfers occur on the IDE interface. The options are:

- Disabled (transfers occur at a less than optimized speed)
- Auto Detected (transfers occur at the drive's maximum speed) (default)

3.2.5 Boot Options Subscreen

This section describes the options available on the Boot Options subscreen.

3.2.5.1 First Boot Device

Sets which drive the system checks first to find an operating system to boot from. The options are:

- Disabled
- Floppy (default)
- Hard Disk
- CD-ROM
- Network

3.2.5.2 Second Boot Device

Sets which drive the system checks second to find an operating system to boot from. The options are:

- Disabled
- Floppy
- Hard Disk (default)
- Network

3.2.5.3 Third Boot Device

Sets which drive the system checks third to find an operating system to boot from. The options are:

- Disabled (default)
- Floppy
- Hard Disk
- Network

3.2.5.4 Fourth Boot Device

Sets which drive the system checks fourth to find an operating system to boot from. The options are:

- Disabled (default)
- Floppy
- Hard Disk
- Network

3.2.5.5 System Cache

Enables or disables both primary and secondary cache memory. The options are:

- Enabled (default)
- Disabled

3.2.5.6 Boot Speed

Sets the system's boot speed. The options are:

- Deturbo (the motherboard operates at the speed of an AT† system)
- Turbo (boot-up occurs at full speed) (default)

3.2.5.7 Num Lock

Sets the beginning state of the Num Lock feature on the numeric keypad of your keyboard. The options are:

- Off (default)
- On

3.2.5.8 Setup Prompt

NOTE

The Setup Prompt option does not affect your ability to access the Setup program. It only enables or disables the prompt.

Controls whether the "Press <F1> Key if you want to run Setup" prompt is displayed during the power-up sequence. The options are:

- Enabled (default)
- Disabled

3.2.5.9 Hard Disk Pre-Delay

Sets the hard disk drive pre-delay. When enabled, this option causes the BIOS to wait the specified time before it accesses the first hard drive. If your system contains a hard drive and you don't see the drive type displayed during boot-up, the hard drive may need more time before it is able to communicate with the controller. Setting a pre-delay provides additional time for the hard drive to initialize. The options are:

- Disabled (default)
- 3 seconds
- 6 seconds
- 9 seconds
- 12 seconds
- 15 seconds
- 21 seconds
- 30 seconds

3.2.5.10 Typematic Rate Programming

Sets the typematic rates. The options are:

- Default (default)
- Override (lets you enter Typematic Rate Delay and Typematic Rate options)

3.2.5.11 Typematic Rate Delay

Sets the delay time before the key-repeat function starts when you hold down a key on the keyboard. If Typematic Rate Programming is set to Default, this option will not be visible. The options are:

- 250 milliseconds (default)
- 500 milliseconds
- 750 milliseconds
- 1000 milliseconds

3.2.5.12 Typematic Rate

Sets the speed at which characters repeat when you hold down a key on the keyboard. The higher the number, the faster the characters repeat. If Typematic Rate Programming is set to Default, this option will not be visible. The options are:

- 6 char/sec (default)
- 8 char/sec
- 10 char/sec
- 12 char/sec
- 15 char/sec
- 20 char/sec
- 24 char/sec
- 30 char/sec

3.2.5.13 Scan User Flash Area

NOTE

Regardless of the setting of this option, if an OEM logo is programmed into the user Flash area it will be displayed at bootup.

Scans the user Flash area for an executable binary to be executed during POST. The options are:

- Disabled (no scan)
- Enabled (scan occurs during POST) (default)

3.2.6 Advanced Screen

This section describes the Setup options found on the Advanced menu screen. If you select certain options from the Advanced screen (e.g., Peripheral Configuration), the Setup program switches to a subscreen for the selected option. Subscreens are described in the sections following the description of the Advanced screen options.

3.2.6.1 Processor Type

Reports the processor type. There are no options.

3.2.6.2 Processor Speed

Reports the processor clock speed. There are no options.

3.2.6.3 Cache Size

Reports the size of the secondary cache. There are no options. If your system contains no L2 cache, this item does not appear.

3.2.6.4 Peripheral Configuration

When selected, this displays the Peripheral Configuration subscreen.

3.2.6.5 Audio Configuration

This option enables or disables the onboard audio subsystem. The options are:

- Disabled (frees the I/O resources and addresses used to support the audio interface)
- Enabled (default)

3.2.6.6 Advanced Chipset Configuration

When selected, this displays the Advanced Chipset Configuration subscreen.

3.2.6.7 Power Management Configuration

When selected and enabled, this displays the Advanced Power Management subscreen.

3.2.6.8 Plug and Play Configuration

When selected, this displays the Plug and Play Configuration subscreen.

3.2.7 Peripheral Configuration Subscreen

This section describes the Setup options for the Peripheral Configuration subscreen. For peripherals set to Auto, the BIOS automatically configures the peripheral during power up.

3.2.7.1 Primary PCI IDE Interface

Disables or automatically configures the primary PCI IDE hard disk interface. The options are:

- Disabled
- Auto (default)

3.2.7.2 Secondary PCI IDE Interface

Disables or automatically configures the secondary PCI IDE hard disk interface. The options are:

- Disabled
- Auto (default)

3.2.7.3 Floppy Interface

Disables or automatically configures the diskette drive interface. The options are:

- Disabled
- Enabled
- Auto (default)

3.2.7.4 Serial Port 1 Address

Selects the logical COM port, I/O address and interrupt for Serial Port 1. The options that are displayed can vary, depending on whether you choose Windows 95 in the Boot with PnP OS screen (see Section 3.2.10.2). The options appear in the following format:

- Disabled
- <COMx>, <I/O address>, <IRQx>
- Auto (Setup assigns the first free COM port, normally COM1, 3F8h, IRQ4) (default)

3.2.7.5 Serial Port 2 Address

Selects the logical COM port, I/O address and IRQ of Serial Port 2. The options that are displayed can vary, depending on whether you choose Windows 95 in the Boot with PnP OS screen (see Section 3.2.10.2). The options appear in the following format:

- Disabled
- <COMx>, <I/O address>, <IRQx>
- Auto (Setup assigns the first free COM port, normally COM2, 2F8h, IRQ3) (default)

NOTE

If you specifically set either serial port address, that address will not appear in the list of options for the other serial port. If an ATI† mach32† *or an* ATI mach64† *video controller is active (as an add-in card), the COM4, 2E8h address will not appear in the list of options for either serial port.*

3.2.7.6 Serial Port 2 IR Mode

Makes Serial Port 2 available to infrared applications. The options are:

- Disabled (default)
- Enabled

3.2.7.7 Parallel Port Address

Selects the logical printer port, I/O address, and interrupt of the parallel port. The options that are displayed can vary, depending on the Parallel Port Mode you choose (see Section 3.2.7.8) and whether you choose Windows 95 in the Boot with PnP OS screen (see Section 3.2.10.2). The options appear in the following format:

- Disabled
- <LPTx>, <I/O address>, <IRQx>
- Auto (Setup assigns LPT1, 378h, IRQ7) (default)

3.2.7.8 Parallel Port Mode

Selects the mode for the parallel port. The options are:

- Compatible (operates in AT-compatible mode) (default)
- Bi-directional (operates in bidirectional PS/2-compatible mode)
- EPP (Enhanced Parallel Port, a high-speed bidirectional mode)
- ECP (Extended Capabilities Port, a high-speed bidirectional mode)

3.2.7.9 USB Interface

Enables or disables the USB interface. USB support requires that the BIOS allocate a PCI interrupt, which could cause an interrupt to be shared with another device. If interrupt sharing is a problem, and you do not need support for USB, you can free an interrupt by disabling USB.

- Disabled (frees the PCI interrupt used to support USB)
- Enabled (default)

3.2.7.10 Primary IDE Status

Reports if the primary IDE interface is enabled or disabled. There are no options.

3.2.7.11 Secondary IDE Status

Reports if the secondary IDE interface is enabled or disabled. There are no options.

3.2.7.12 Floppy Status

Reports if the diskette drive interface is enabled or disabled. There are no options.

3.2.7.13 Serial Port 1 Status

Reports the COM port, I/O address, and IRQ for Serial Port 1. There are no options.

3.2.7.14 Serial Port 2 Status

Reports the COM port, I/O address, and IRQ for Serial Port 2. There are no options.

3.2.7.15 Parallel Port Status

Reports the logical printer port, I/O address, and IRQ for the parallel port. There are no options.

3.2.8 Advanced Chipset Configuration Subscreen

This section describes the options available on the Advanced Chipset Configuration subscreen.

3.2.8.1 Base Memory Size

Sets the size of the base memory. The options are:

- 512 KB
- 640 KB (default)

3.2.8.2 ISA LFB Size

Sets the size of the linear frame buffer. The options are:

- Disabled (default)
- 1 MB (if selected, the ISA LFB Base Address field appears)

3.2.8.3 ISA LFB Base Address

Reports the base address of the linear frame buffer. There are no options. This field does not appear if the ISA LFB Size is set to Disabled.

3.2.8.4 Video Palette Snoop

Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card. The options are:

- Disabled (default)
- Enabled

3.2.8.5 Latency Timer (PCI Clocks)

Sets the length of time an agent on the PCI bus can hold the bus when another agent has requested the bus. The units are numbers of PCI clocks. Valid numbers are between 0 and 256. The default is 66.

3.2.8.6 Bank 0 DIMM Detected

Reports the size and type of memory found in bank 0. There are no options.

3.2.8.7 Bank 1 DIMM Detected

Reports the size and type of memory found in bank 1. There are no options.

3.2.9 Power Management Configuration Subscreen

This section describes the options available on the Power Management Configuration subscreen.

3.2.9.1 Advanced Power Management

Enables or disables the Advanced Power Management (APM) support in the BIOS. APM manages power consumption only when used with an APM-capable operating system. The options are:

- Disabled (none of the following fields in the Advanced Power Management subscreen appear)
- Enabled (default)

3.2.9.2 IDE Drive Power Down

Sets any IDE drives to spin down when the computer goes into power managed mode. The options are:

- Disabled
- Enabled (default)

3.2.9.3 VESA Video Power Down

Sets any VESA-compliant monitor to be power managed when the system goes into power managed mode. The options are:

- Disabled (the monitor is not under power management)
- Standby (minimal power reduction, HSYNC signal not active)
- Suspend (significant power reduction, VSYNC signal not active)
- Sleep (maximum power reduction, HSYNC and VSYNC not active) (default)

3.2.9.4 Inactivity Timer (Minutes)

Sets the number of minutes the computer must be inactive before it enters power-managed mode. The range is 0 - 255 minutes. The default is 10 minutes.

3.2.9.5 Hot Key

Sets the hot key for power-managed mode. When a user presses this key while holding down the <Ctrl> and <Alt> keys, the system enters power-managed mode. All alphabetic keys are valid entries for this field. The BIOS must be connected to an OS-dependent APM driver for this option to work.

NOTE

If you set the APM hot key and the Security hot key (see Section 3.2.12.6) to the same key, the APM function has priority.

3.2.10 Plug and Play Configuration Subscreen

This section describes the options in the Plug and Play configuration subscreen.

3.2.10.1 Configuration Mode

Sets how the BIOS gets information about ISA cards that do not have Plug and Play capabilities. The options are:

- Use Setup Utility (displays options for reserving resources for ISA legacy devices)
- Use ICU (displays a choice of OSs as listed in the following section) (default)

3.2.10.2 Boot with PnP OS

This option applies only to Plug and Play ISA cards; the BIOS always auto-configures PCI devices. The option lets the computer boot with an operating system capable of managing Plug and Play add-in cards. If you choose one of the Plug and Play OS options (Other or Windows 95), the BIOS assigns resources to ISA Plug and Play initial program load (IPL) devices. The OS is then responsible to enable devices and assign resources (I/O addresses, interrupts, etc.) for all remaining devices.

The options are:

- None (for DOS; BIOS configures and enables all devices at boot time, whether they are Plug and Play or not)
- Other PnP OS (BIOS auto-configures PCI devices before onboard motherboard devices)
- Windows 95 (BIOS auto-configures onboard motherboard devices before PCI devices) (default)

3.2.10.3 ISA Shared Memory Size

Lets you specify a range of memory addresses that will be usable by ISA add-in cards for shared memory, and that will not be used for shadowing ROM memory from other devices. The options are:

- Disabled (the ISA Shared Memory Base Address field does not appear) (default)
- 16 KB
- 32 KB
- 48 KB
- 64 KB
- 80 KB
- 96 KB

Enable this field only if you are using a legacy ISA add-in card without Plug and Play capabilities, and the card requires non-ROM memory space. For example, this could include LAN cards that have onboard memory buffers or video capture cards that have video buffer memory.

By default, upper memory is allocated as follows: Memory from C0000-C7FFF is automatically shadowed (this memory range is typically reserved for video BIOS). Memory from C8000-DFFFF is initially unshadowed. The BIOS scans this range for any ISA add-in cards that may be present and notes their location and size. The BIOS then auto-configures the PCI devices and Plug and

Play devices, shadowing their ROM requirements (other than video) into the area above E0000. If that area becomes full, it continues shadowing to the area between C8000 and DFFFF. If an ISA legacy card has non-ROM memory requirements, the auto-configure routine might write into an area that is needed by the ISA card. Use the ISA Shared Memory Size and ISA Shared Memory Base Address fields to reserve a block of memory that will not be used for shadowing.

3.2.10.4 ISA Shared Memory Base Address

Sets the base address for the ISA Shared Memory. The options are:

- C8000h (default)
- CC000h
- D0000h
- D4000h
- D8000h
- DC000h

The options that appear depend on the ISA Shared Memory Size field. The total amount of ISA Shared Memory cannot extend to the E0000h address. For example, if you specify a size of 64KB, options D4000h, D8000h, and DC000h will not be available.

3.2.10.5 IRQ 3, 4, 5, 7, 9, 10, 11, 14, 15

Sets the status of the IRQ. The options are:

- Available (default)
- Used By ISA Card

The PCI auto-configuration code uses these settings to determine whether these interrupts are available for use by PCI add-in cards. If an interrupt is marked available, the auto-configuration code can assign the interrupt to be used by the system. If your computer has an ISA add-in card that requires an interrupt, select Used By ISA Card for that interrupt.

NOTE

IRQs 5, 9, 10, and 11 are the default user-available IRQs. Depending on the configuration of your computer, other IRQs may be listed (for example, if you disable the parallel port and/or serial ports).

3.2.11 Security Screen

This section describes the passwords you can set to restrict access to the Setup program and to restrict who can boot the computer.

3.2.11.1 Administrative and User Access Modes

The options on the Security screen let you set a User password and/or an Administrative password. The access restrictions for the User and Administrative modes are:

- Setup options: The Administrative password gives you full access to Setup options; the User password can be limited to only certain options. Thus, by setting separate Administrative and User passwords, a system administrator can limit who can change critical Setup values. The actual limitations depend on whether one or both passwords are set. Table 37 shows how the passwords work together.

- Booting the system: To limit access to who can boot the system, set the User password. This is the password that the system asks for before booting. If only the Administrative password is set, the system boots up without asking for a password. If both passwords are set, you can enter either password to boot the system.

Table 37 shows the effects of setting the Administrative and User passwords. The table is for reference only, and is not shown on the Security screen.

Table 37. Administrative and User Password Functions

Password Set	Administrative Mode	User Mode	Password Required During Boot Process
Neither	Can change all options*	Can change all options*	None
Administrative only	Can change all options	Can change a limited number of options **	None
User only	N/A	Can change all options	User
Both	Can change all options	Can change a limited number of options **	Administrative or User

* If no password is set, any user can change all Setup options.

** Limited options include only: system date and time, power management hot key, User password, security hot key, and unattended start

3.2.12 Security Screen Options

3.2.12.1 User Password is

Reports if there is a User password set. There are no options.

3.2.12.2 Administrative Password is

Reports if there is an Administrative password set. There are no options.

3.2.12.3 Set User Password

Sets the User password. The password can be up to seven alphanumeric characters.

3.2.12.4 Set Administrative Password

Sets the Administrative password. The password can be up to seven alphanumeric characters.

3.2.12.5 Unattended Start

Controls when the security password is requested. The User password must be set to enable this field. The options are:

- Enabled (the system boots, but the keyboard is locked until the User password is entered)
- Disabled (default)

3.2.12.6 Security Hot Key (CTRL-ALT-)

Sets a hot key that locks the keyboard until the User password is entered. All alphabetic keys are valid entries for this field. When a user presses this key while holding down the <Ctrl> and <Alt> keys, the keyboard locks and the keyboard LEDs flash to indicate that the keyboard is locked.

When you enter the User password to unlock the keyboard, you do not have to press <Enter>.

NOTE

If you set the Security hot key and the APM hot key (see Section 3.2.9.5) to the same key, the APM function has priority.

3.2.13 Exit Screen

This section describes how to exit Setup with or without saving the changes you have made.

3.2.13.1 Exit Saving Changes

Exits Setup and saves the changes in CMOS RAM. You can also press the <F10> key anywhere in the Setup utility to do this.

3.2.13.2 Exit Discarding Changes

Exits Setup program without saving any changes. This means that any changes you have made while in Setup are discarded and not saved. Pressing the <Esc> key in any of the four main screens will also exit and discard changes.

3.2.13.3 Load Setup Defaults

Returns all of the Setup options to their defaults. The default Setup values are loaded from the ROM table. You can also press the <F5> key anywhere in Setup to load the defaults.

3.2.13.4 Discard Changes

Discards any changes made up to this point in Setup without exiting Setup. This selection loads the CMOS RAM values that were present when the system was turned on. You can also press the <F6> key anywhere in Setup to discard changes.

4 Error Messages and Beep Codes

4.1 BIOS Beep Codes

One long beep followed by short beeps indicates a video problem.

Beeps	Error Message	Description
1	Refresh Failure	The memory refresh circuitry on the baseboard is faulty.
3	Base 64 KB Memory Failure	Memory failure in the first 64 KB.
4	Timer Not Operational	Memory failure in the first 64 KB of memory, or Timer 1 on the motherboard is not functioning.
5	Processor Error	The processor on the motherboard generated an error.
6	Gate A20 Failure	The keyboard controller may be bad. The BIOS cannot switch to protected mode.
7	Processor Exception Interrupt Error	The processor generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM Checksum Error	ROM checksum value does not match the value encoded in BIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS RAM failed.
11	Cache Error/External Cache Bad	The external cache is faulty.

4.2 PCI Configuration Error Messages

The following PCI messages are displayed as a group with bus, device, and function information.

Message	Explanation
Bad PnP Serial ID Checksum	The Serial ID checksum of a Plug and Play card is invalid.
Floppy Disk Controller Resource Conflict	The floppy disk controller has requested a resource that is already in use.
NVRAM Checksum Error, NVRAM Cleared	The Extended System Configuration Data (ESCD) was reinitialized because of an NVRAM checksum error. Try rerunning the ISA Configuration Utility (ICU).
NVRAM Cleared By Jumper	The Clear CMOS jumper has been moved to the Clear position and CMOS RAM has been cleared.
NVRAM Data Invalid, NVRAM Cleared	Invalid entry in the ESCD.
Parallel Port Resource Conflict	The parallel port requested a resource that is already in use.
PCI Error Log is Full	More than 15 PCI conflict errors have been detected and no additional PCI errors can be logged.

continued ☛

PCI Configuration Error Messages (continued)

Message	Explanation
PCI I/O Port Conflict	Two devices requested the same I/O address, resulting in a conflict.
PCI IRQ Conflict	Two devices requested the same IRQ, resulting in a conflict.
PCI Memory Conflict	Two devices requested the same memory resource, resulting in a conflict.
Primary Boot Device Not Found	The designated primary boot device (hard disk drive, diskette drive, CD-ROM drive, or network) could not be found.
Primary IDE Controller Resource Conflict	The primary IDE controller has requested a resource that is already in use.
Primary Input Device Not Found	The designated primary input device (keyboard, mouse, or other device if input is redirected) could not be found.
Secondary IDE Controller Resource Conflict	The secondary IDE controller has requested a resource that is already in use.
Serial Port 1 Resource Conflict	Serial Port 1 has requested a resource that is already in use.
Serial Port 2 Resource Conflict	Serial Port 2 has requested a resource that is already in use.
Static Device Resource Conflict	A non Plug and Play ISA card has requested a resource that is already in use.
System Board Device Resource Conflict	A non Plug and Play ISA card has requested a resource that is already in use.

4.3 BIOS Error Messages

Error Message	Explanation
Gate A20 Error	Gate A20 on the keyboard controller is not working.
Address Line Short!	Error in the address decoding circuitry on the baseboard.
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective. Replace it.
CH-2 Timer Error	There is an error in Counter/Timer 2.
CMOS Battery State Low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS Checksum Failure	After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run Setup.
CMOS System Options Not Set	The values stored in CMOS RAM are either corrupt or nonexistent. Run Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected by the BIOS. Run Setup.
CMOS Memory Size Mismatch	The amount of memory on the motherboard is different than the amount indicated in CMOS RAM. Run Setup.
CMOS Time and Date Not Set	Run Setup to set the date and time in CMOS RAM.

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BIOS Error Messages (continued)

Error Message	Explanation
Diskette Boot Failure	The boot disk in floppy drive A: is corrupt. It cannot be used to boot the system. Use another boot disk and follow the screen instructions.
DMA Error	Error in the DMA controller.
DMA #1 Error	Error in the first DMA channel.
DMA #2 Error	Error in the second DMA channel.
FDD Controller Failure	The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered down.
HDD Controller Failure	The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down.
INTR #1 Error	Interrupt channel 1 failed POST.
INTR #2 Error	Interrupt channel 2 failed POST.
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but cannot boot the system from it. Use another boot disk.
Keyboard Is Locked...Unlock It	The keyboard lock on the system is engaged. The system must be unlocked to continue.
Keyboard Error	There is a timing problem with the keyboard.
KB/Interface Error	There is an error in the keyboard connector.

4.4 ISA NMI Messages

NMI Message	Explanation
DMA Bus Time-out	A device has driven the bus signal for more than 7.8 microseconds.

5 Specifications and Customer Support

5.1 Online Support

Find information about Intel motherboards under “Product Info” or “Customer Support” at this World Wide Web site:

`http://www.intel.com/`

or at this FTP site:

`ftp://ftp.intel.com/pub/`

5.2 Specifications

The motherboard complies with the following specifications:

Table 38. Compliance with Specifications

Specification	Description	Revision Level
ACP	Advanced Configuration and Power Interface specification	Draft Revision 0.7, June, 1996 Intel Corp., Microsoft Corporation, Toshiba Corporation
APM	Advanced Power Management BIOS interface specification	Revision 1.1, September, 1993 Intel, Microsoft
ATA-33	Synchronous DMA Transfer Protocol specification (to be proposed as Ultra DMA/33 standard)	Revision 0.7, May 21, 1996 Quantum document no. 70-108412-1
ATX	ATX form factor specification	Revision 1.1, February 1996
COASt	Flexible cache solution for the Intel 430FX, 430HX, 430VX PCIset	Revision 3.0, February 14, 1996 Intel Corporation
DDC2	Display Data Channel standard	Version 2, Revision 0, April 9, 1996 Video Electronics Standards Association
DMI	Desktop Management Interface BIOS specification	Version 2.0, October 16, 1995 American Megatrends Inc., Award Software International Inc., Dell Computer Corporation, Intel, Phoenix Technologies Ltd, SystemSoft Corporation
DPMS	Display Power Management Signaling	Revision ?, Version ?, ?, 199? Video Electronics Standards Association
“El Torito”	Bootable CD-ROM format specification	Version 1.0, January 25, 1995 Phoenix Technologies, IBM Corporation
EPP	Enhanced Parallel Port	IEEE 1284 standard

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Table 39. Compliance with Specification (continued)

Specification	Description	Revision Level
Feature Connector	Standard VGA Pass-Through Connector (VSPC)	Version ?, Revision ?, ?199? Video Electronics Standards Association
IrDA	Serial Infrared Physical Layer Link specification	Version 1.1, October 17, 1995 Infrared Data Association.
PCI	PCI Local Bus specification	Revision 2.1, June 1, 1996 PCI Special Interest Group
Plug and Play	Plug and Play BIOS specification	Version 1.0a, May 5, 1994 Compac Computer Corp, Phoenix Technologies, Intel
USB	Universal Serial Bus specification	Revision 1.0, January 15, 1996 Compac, Digital Equipment Corporation, IBM PC Company, Intel, Microsoft, NEC, Northern Telecom