Intel® Desktop Board GS810
Technical Product Specification

May 2000

Order Number 747129-002

The Intel® Desktop Board GS810 may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board GS810 Specification Update.

Revision History

Revision	Revision History	Date
-001	First Release of the Intel® GS810 Desktop Board Technical Product Specification	October 1999
-002	Second Release of the Intel GS810 Desktop Board Technical Product Specification	May 2000

This product specification applies to only standard GS810 boards with BIOS identifier GS81010A.86A or GS81011A.86A.

Changes to this specification will be published in the Intel Desktop Board GS810 Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the GS810 desktop board. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the GS810 board and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on this board
2	A map of the resources of the board
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Note, Caution, and Warning

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions that, if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the GS810 board, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
GB	Gigabyte (1,073,741,824 bytes)
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
†	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

5 Error Messages and Beep Codes

Figures

Tables

1 Product Description

What This Chapter Contains

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the GS810 board's major features.

Table 1. Feature Summary

Form Factor	FlexATX (9.0 inches by 7.5 inches)
Processor	Support for either an: • Intel® Pentium® III processor in a FCP-PGA package (Support for a Pentium III processor requires a board with an AA number of 300 or greater and with BIOS GS81011A.86A.0002.P02 or greater.) • Intel® Celeron™ processor in a PPGA package
Memory	• Two 168-pin dual inline memory module (DIMM) sockets • Supports up to 512 MB of 100 MHz non-ECC synchronous DRAM (SDRAM) • Support for serial presence detect (SPD) and non-SPD DIMMs
Chipset	Intel® 810 chipset, consisting of: • Intel® 82810 Graphics and Memory Controller Hub (GMCH0) • Intel® 82801AA I/O Controller Hub (ICH) • Intel® 82802AB 4 Mbit Firmware Hub (FWH)
Accelerated Graphics Port (AGP) Video	• Intel 82810 GMCH0 • VGA port connector on back panel
Audio	Audio Codec '97 (AC'97) compatible audio subsystem, consisting of the following: • Intel 82801AA ICH (AC link output) • Analog Devices AD1881 analog codec
I/O Control	IT8761E Low Pin Count (LPC) I/O controller
Peripheral Interfaces	• Four universal serial bus (USB) ports • Two IDE interfaces with Ultra DMA support
Expansion capabilities	One mini-PCI expansion slot
BIOS	• Intel/AMI BIOS stored in an Intel 82802AB 4 Mbit firmware hub (FWH) • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS
Instantly Available PC	• Support for *PCI Local Bus Specification*, Revision 2.2 • Suspend-to-RAM support • Wake from USB ports

⟹ NOTE

The GS810 board is designed to support only USB-aware operating systems.

For information about…	Refer to…
The board's compliance level with ACPI, Plug and Play, and SMBIOS	Table 3, page 14

1.1.2 Manufacturing Options

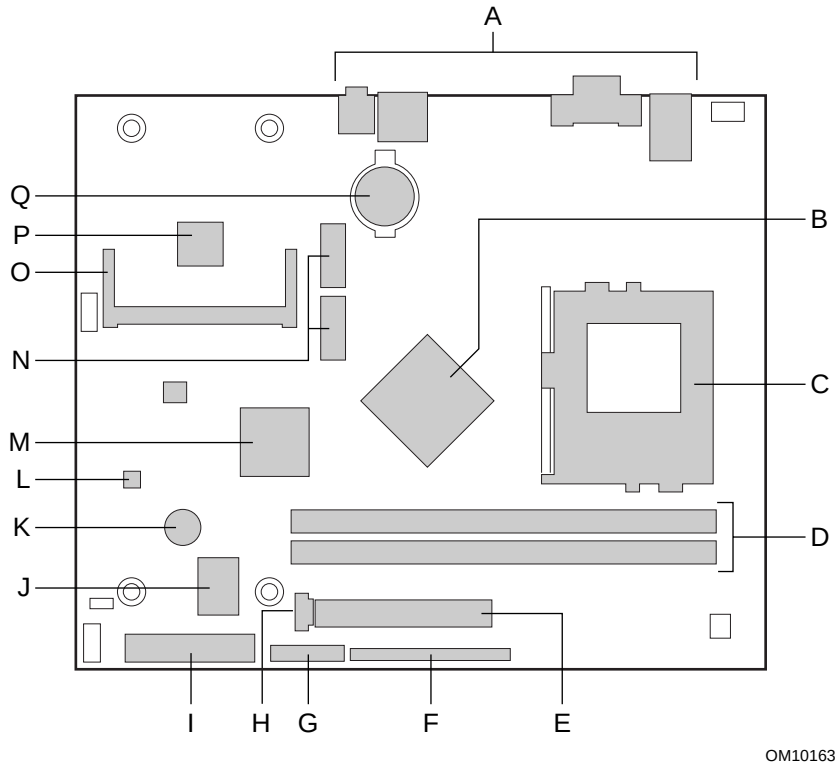
Table 2 describes the GS810 board's manufacturing options. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

Table 2. Manufacturing Options

Accelerated Graphics Port (AGP) Video	• Intel 82810 DC-100 GMCH • 4 MB SDRAM display cache
Serial Port	One internal 9-pin serial debug port connector
Management Level 5	• Intel® 82559 local area network (LAN) controller • Alert on LAN† 2 ASIC • Hardware monitor
Supplemental Cooling	Chassis fan connector

1.1.3 Board Layout

Figure 1 shows the location of the major components on the GS810 board.



A	Back panel connectors	J	IT8761E I/O controller
B	Intel 82810 GMCH	K	Speaker
C	Processor socket	L	AD1881 analog codec
D	DIMM sockets	M	Intel 82801AA ICH
E	Primary IDE connector	N	4 MB display cache (optional)
F	Slimline IDE connector	O	Mini-PCI connector
G	Front panel connector	P	Intel 82559 LAN Controller (optional)
H	ATAPI CD-ROM (optional)	Q	Battery
I	Power connector		

Figure 1. Board Components

1.1.4 Block Diagram

Figure 2 is a block diagram of the major functional areas of the GS810 board.

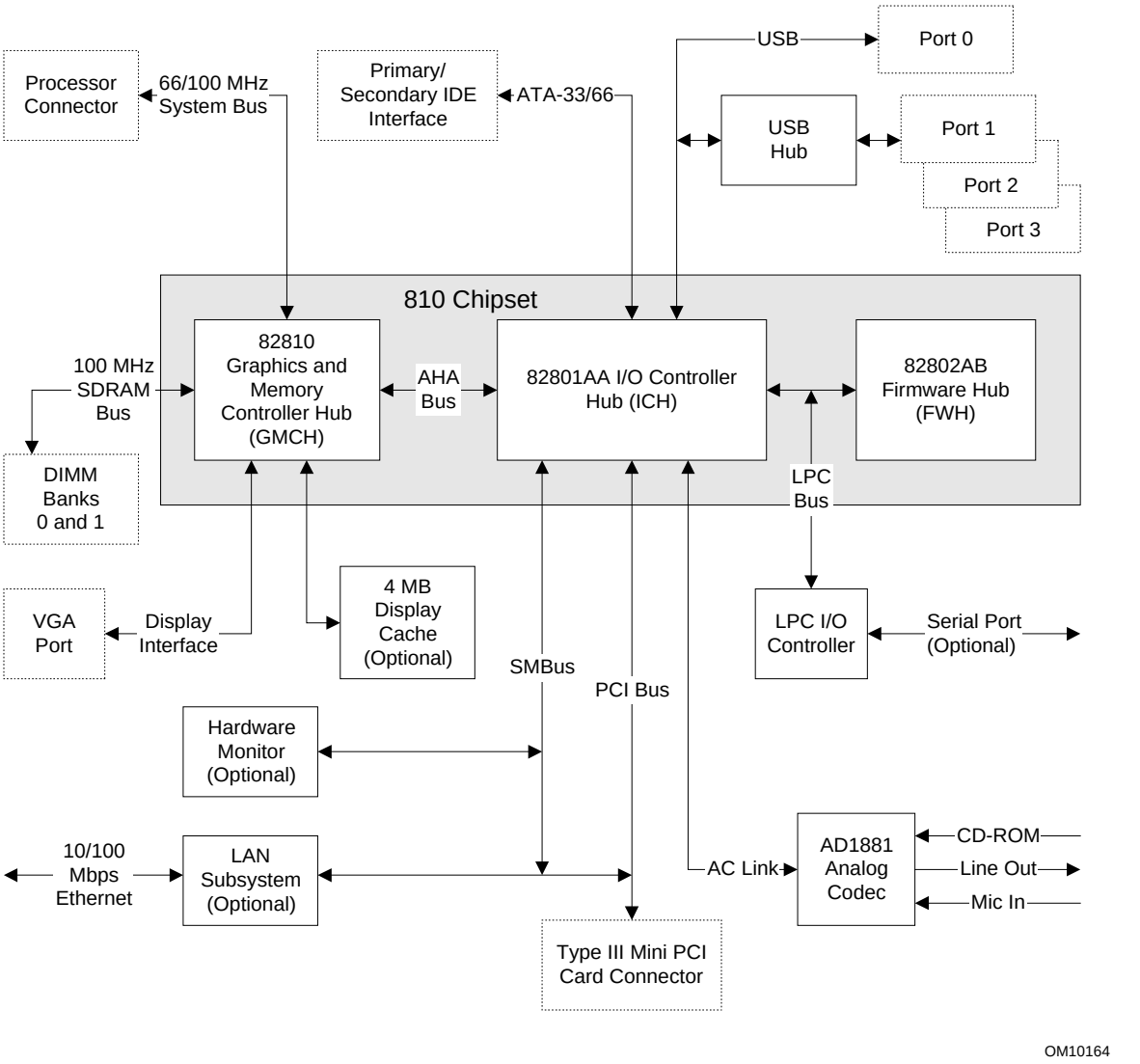


Figure 2. Block Diagram

1.2 Online Support

Find information about GS810 desktop boards under "OEM-only Products" at this World Wide Web site:

http://developer.intel.com/design/motherbd/oem/index.htm#GS810

1.3 Design Specifications

Table 3 lists the specifications applicable to the GS810 board.

Table 3. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	This specification is available at…
AC '97	*Audio Codec '97*	Version 2.1, May 22, 1998, Intel Corporation.	http://developer.intel.com/ial/scalableplatforms/audio/index.htm
ACPI	*Advanced Configuration and Power Interface Specification*	Version 1.0b, February 2, 1999, Intel Corporation, Microsoft Corporation, and Toshiba Corporation.	http://www.teleport.com/~acpi/
AGP	*Accelerated Graphics Port Interface Specification* (2X only)	Version 2.0, May 4, 1998, Intel Corporation.	http://www.intel.com/technology/agp/agp_index.htm
AMI BIOS	*American Megatrends BIOS Specification*	AMIBIOS 99, June 1999, American Megatrends, Inc.	http://www.ami.com/amibios/bios.platforms.desktop.html
ATAPI	*Information Technology AT Attachment with Packet Interface Extensions T13/1153D*	Version 18, August 19, 1998, Contact: T13 Chair, Seagate Technology.	T13 Anonymous FTP Site: ftp://fission.dt.wdc.com/x3t13/project/d1153r18.pdf
ATX	*ATX Specification*	Version 2.01, February 1997, Intel Corporation.	http://developer.intel.com/design/motherbd/atx.htm
El Torito	*Bootable CD-ROM Format Specification*	Version 1.0, January 25, 1995, Phoenix Technologies Ltd. and IBM Corporation.	the Phoenix Web site at: http://www.ptltd.com/techs/specs.html
FlexATX	*FlexATX Addendum*	Addendum version 1.0 to the microATX Specification version 1.0, March 12, 1999, Intel Corporation.	http://www.teleport.com/~ffsupprt/spec/FlexATXaddn1_0.pdf

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	This specification is available at…
Intel Celeron Processor	*Intel Celeron Processor*	January 2000, Intel Corporation.	http://developer.intel.com/design/intarch/celeron/nodoc.htm
	Intel Celeron Processor Specification Update	Version 22, February 2000, Intel Corporation.	http://developer.intel.com/design/intarch/celeron/nodoc.htm
Intel Pentium III Processor	*Pentium III Processor for the PGA370 Socket*	January 2000, Intel Corporation.	http://developer.intel.com/design/intarch/pentiumiii/nodoc.htm
	Pentium III Processor Specification Update	Version 13, February 2000, Intel Corporation.	http://developer.intel.com/design/intarch/pentiumiii/nodoc.htm
MicroATX	*microATX Motherboard Interface Specification*	Version 1.0, December 1997, Intel Corporation.	http://www.teleport.com/~ffsupprt/spec/microatxspecs.htm
	SFX Power Supply Design Guide	Version 1.1, February 1998, Intel Corporation.	http://www.teleport.com/~ffsupprt/spec/microatxspecs.htm
Mini PCI	*Mini PCI Specification*	Revision 1.0, October 25, 1999, PCI Special Interest Group.	http://www.pcisig.com/tech/availspecs.html#9
PCI	*PCI Local Bus Specification*	Version 2.2, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/tech/availspecs.html#1
	PCI Bus Power Management Interface Specification	Version 1.1, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/tech/availspecs.html#5
Plug and Play	*Plug and Play BIOS Specification*	Version 1.0a, May 5, 1994, Compaq Computer Corp., Phoenix Technologies Ltd., and Intel Corporation.	http://www.microsoft.com/hwdev/respec/pnpspecs.htm
SDRAM DIMMs (64-and 72-bit)	*PC SDRAM Unbuffered DIMM Specification*	Revision 1.0, February 1998, Intel Corporation.	http://www.intel.com/technology/memory/pcsdram/spec/
	PC Serial Presence Detect (SPD) Specification	Revision 1.2B, November 1999, Intel Corporation.	http://www.intel.com/technology/memory/pcsdram/spec/

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	This specification is available at…
SMBIOS	*System Management BIOS*	Version 2.3.1, March 16, 1999, American Megatrends Inc., Award Software International Inc., Compaq Computer Corporation, Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, and SystemSoft Corporation.	ftp://download.intel.com/ial/wfm/smbios.pdf
UHCI	*Universal Host Controller Interface Design Guide*	Version 1.1, March 1996, Intel Corporation.	http://developer.intel.com/design/USB/UHCI11D.htm
USB	*Universal Serial Bus Specification*	Version 1.1, September 23, 1998, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC.	http://www.usb.org/developers/docs.html
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation.	http://developer.intel.com/ial/WfM/wfmspecs.htm

1.4 Processor

CAUTION

The GS810 board supports processors that draw a maximum of 15.2 A. Using a processor that draws more than 15.2 A can damage the processor, the board, and the power supply. See the processor's data sheet for current usage requirements.

NOTE

Support for a Pentium III processor requires a board with an AA number suffix of 300 or greater and with BIOS GS81011A.86A.0002.P02 or greater. The AA number is a small bar-coded label that can be found on the component side of the board. The AA number follows this format, XXXXXX-XXX.

The GS810 board supports a single Celeron processor or a single Pentium III processor as shown in Table 4. The system bus frequency is automatically selected.

Table 4. Supported Processors

Type	Designation	System Bus Frequency	L2 Cache Size
Pentium III processor in a FCP-PGA package	500E MHz, 550E MHz, 600E MHz, 650 MHz, 700 MHz	100 MHz	256 KB
Celeron processor in a PPGA package	300A MHz, 333 MHz, 366 MHz, 400 MHz, 433 MHz, 466 MHz, 500 MHz	66 MHz	128 KB

All supported onboard memory can be cached, up to the cachability limit of the processor.

For information about…	Refer to…
Intel Celeron processor datasheets and specification updates	Table 3, page 14
Intel Pentium III processor datasheets and specification updates	Table 3, page 14
Processor support for the GS810 board	http://developer.intel.com/design/processor

1.5 System Memory

⚠ CAUTION

To be fully compliant with all applicable Intel® SDRAM memory specifications, the GS810 board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. If your memory modules do not support SPD, the BIOS will attempt to configure the memory controller for normal operation; however, the DIMMs may not function at the determined frequency. BIOS Recovery cannot be accomplished using non-SPD DIMMs. SPD data structure is required for the recovery process.

⚠ CAUTION

Because the main system memory is also used as video memory, the board requires 100 MHz SDRAM DIMMs even when the processor system bus is 66 MHz. It is highly recommended that SPD DIMMs be used, since this allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted.

The GS810 board has two DIMM sockets. The minimum memory size is 16 MB and the maximum memory size is 512 MB. The BIOS automatically detects memory type, size, and speed. Memory can be installed in one or both sockets. Memory size can vary between sockets.

The board supports the following memory features:

- 3.3 V, 168-pin DIMMs with gold-plated contacts
- 100 MHz SDRAM
- Serial Presence Detect (SPD) or non-SPD memory
- Non-ECC (64-bit) memory
- Unbuffered single- or double-sided DIMMs

The board is designed to support DIMMs in the configurations listed in Table 5 below.

Table 5. System Memory Configuration

DIMM Size	Non-ECC Configuration
16 MB	2 Mbit x 64
32 MB	4 Mbit x 64
64 MB	8 Mbit x 64
128 MB	16 Mbit x 64
256 MB	32 Mbit x 64

Note: 256 MB DIMMs used with this board must be built with 128 Mbit device technology.

For information about…	Refer to…
The *PC Serial Presence Detect Specification*	Table 3, page 14
Obtaining copies of PC SDRAM specifications	http://www.intel.com/technology/memory/pcsdram/spec/index.htm

1.6 Intel® 810 Chipset

The Intel 810 chipset consists of the following devices:

- 82810 Graphics Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- 82801AA I/O Controller Hub (ICH) with AHA bus
- 82802AB Firmware Hub (FWH)

The chipset provides the system, memory, AGP, and I/O interfaces shown in Figure 3.

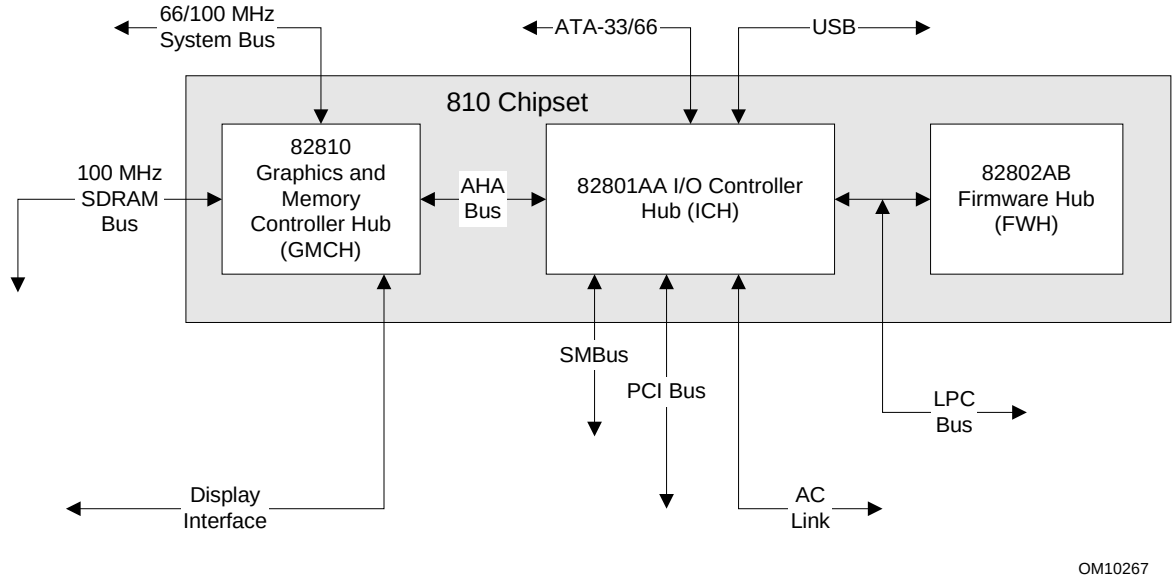


Figure 3. Intel 810 Chipset Block Diagram

For information about…	Refer to…
The Intel 810 chipset	http://developer.intel.com/
The resources used by the chipset	Chapter 2
The chipset's compliance with ACPI and AC '97	Table 3, page 14

1.6.1 AGP

Direct (integrated) AGP is a high-performance bus for graphics-intensive applications, such as 3D applications. AGP, while based on the *PCI Local Bus Specification*, Rev. 2.1, is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amount of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent bus efficiency

1.6.2 USB

The GS810 board has four USB ports; one USB peripheral can be connected to each port. For more than four USB devices, an external hub can be connected to any of the ports. Two USB ports are implemented with stacked back panel connectors. The other two ports can be routed using a cable to the front panel. The board fully supports UHCI and uses UHCI-compatible software drivers. USB features include:

- Support for self-identifying peripherals that can be connected or disconnected while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about…	Refer to…
The location of the USB connectors on the back panel	Figure 6, page 41
The signal names of the front panel USB connector	Table 22, page 44
The signal names of the USB connectors	Table 18, page 42
The USB and UHCI specifications	Table 3, page 14

1.6.3 IDE Support

The GS810 board has two independent bus-mastering IDE interfaces. These interfaces support:

- ATAPI devices (such as CD-ROM drives)
- ATA devices using the transfer modes listed in Table 52 on page 78

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The board supports laser servo (LS-120) diskette technology through its IDE interfaces. The LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

NOTE

LS-120 support is a manufacturing option in the BIOS.

The board has two IDE interface connectors. The primary IDE connector is a standard 40-pin IDE interface. The secondary IDE connector is a 50-pin Slimline IDE connector, intended for use with devices such as 2.5-inch hard disk drives and mobile CD-ROM drives. The Slimline IDE connector has the standard IDE interface pins but also includes audio and power signals.

For information about…	Refer to…
The location of the IDE connectors	Figure 7, page 43
The signal names of the primary IDE connector	Table 24, page 45
The signal names of the Slimline IDE connector	Table 25, page 46
BIOS Setup program's Boot menu	Table 56, page 81

1.6.4 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with standby voltage applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTE

If the battery and AC power fail, standard defaults, not custom defaults, will be loaded into CMOS SRAM at power on.

NOTE

The recommended method of accessing the date in systems with Intel® desktop boards is indirectly from the Real-Time Clock (RTC) via the BIOS. The BIOS on Intel desktop boards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

For information about…	Refer to…
Proper date access in systems with Intel desktop boards	http://support.intel.com/support/year2000/

1.7 I/O Controller

The IT8761E I/O controller provides the following features:

- Low pin count (LPC) interface
- One serial port
- Plug and Play compatible register set

The BIOS Setup program provides configuration options for the I/O controller.

For information about…	Refer to…
The IT8761E I/O controller	http://www.iteusa.com

1.7.1 Serial Debug Port (Optional)

The board has one internal 9-pin serial debug port connector. The serial debug port's NS16C550-compatible UART supports data transfers at speeds up to 115.2 kbits/sec with BIOS support. The serial debug port can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

For information about…	Refer to…
The location of the serial debug port connector	Figure 7, page 43
The signal names of the serial debug port connector	Table 28, page 47

1.8 Graphics Subsystem

The Intel 82810 GMCH0 Graphics and Memory Controller Hub component provides the following graphics support features:

- Integrated 2-D and 3-D graphics engines
- Integrated hardware motion compression engine
- Integrated 230 MHz DAC

A manufacturing option of this board replaces the GMCH0 component with the GMCH DC-100 component and adds a 4 MB SDRAM display cache.

Table 6 lists the refresh rates supported by the graphics subsystem. Supported graphics refresh rates may vary based on manufacturing options, BIOS, and video drivers.

Table 6. Supported Graphics Refresh Rates

Resolution	Available Refresh Rates (Hz)
640 x 200 x 16 colors	70
640 x 350 x 16 colors	70
640 x 400 x 256 colors	60, 70, 75, 85
640 x 400 x 64 K colors	60, 70, 75, 85
640 x 400 x 16 M colors	70
640 x 480 x 16 colors	60, 72, 75, 85
640 x 480 x 256 colors	60, 70, 72, 75, 85
640 x 480 x 32 K colors	60, 75, 85
640 x 480 x 64 K colors	60, 70, 72, 75, 85
640 x 480 x 16 M colors	60, 70, 72, 75, 85
800 x 600 x 256 colors	60, 75, 85
800 x 600 x 32 K colors	60, 70, 72, 75, 85
800 x 600 x 64 K colors	60, 70, 72, 75, 85
800 x 600 x 16 M colors	60, 70, 72, 75, 85
1024 x 768 x 256 colors	60, 70, 75, 85
1024 x 768 x 32 K colors	60, 75, 85
1024 x 768 x 64 K colors	60, 70, 72, 75, 85
1024 x 768 x 16 M colors	60, 70, 72, 75, 85
1056 x 800 x 16 colors	70
1280 x 1024 x 256 colors	60, 70, 72, 75, 85
1280 x 1024 x 32 K colors	60, 75, 85
1280 x 1024 x 64 K colors	60, 70, 72, 75
1280 x 1024 x 16 M colors	60, 70, 72, 75, 85

For information about…	Refer to…
Obtaining graphics software and utilities	http://support.intel.com/support/motherboards/desktop

1.9 Audio Subsystem

The GS810 board includes an Audio Codec ’97 (AC ’97) compatible audio subsystem consisting of the these devices:

- Intel 82801AA ICH (AC link output)
- Analog Devices AD1881 analog codec

Figure 4 is a block diagram of the audio subsystem.

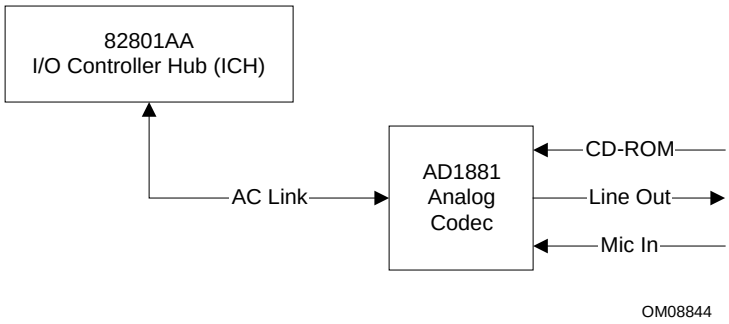


Figure 4. Block Diagram of Audio Subsystem with AD1881 Codec

Features of the audio subsystem include:

- Independent channels for PCM in, PCM out, and Mic in
- 16-bit stereo I/O up to 48 kHz
- Multiple sample rates

For information about…	Refer to…
Obtaining audio software and utilities	http://support.intel.com/support/motherboards/desktop

1.9.1 AD1881 Analog Codec

The AD1881 is a fully AC ’97 compliant codec. The codec's features include:

- 16-bit stereo full-duplex codec
- High quality CD input with ground sense
- Stereo line level output
- Power management support
- Full duplex variable sampling rate (7 kHz to 48 kHz) with 1 Hz resolution
- Phat† Stereo 3-D stereo enhancement

1.9.2 Audio Connectors

The audio connectors include the following:

- ATAPI CD-ROM (optional)
- Line out (front panel connector and back panel)
- Mic in (auxiliary audio connector)

For information about…	Refer to…
The location of the ATAPI CD-ROM connector	Figure 7, page 43
The signal names of the ATAPI CD-ROM connector	Table 26, page 46
The location of the auxiliary audio connector	Figure 7, page 43
The signal names of the auxiliary audio connector	Table 30, page 47
The back panel audio connectors	Section 2.8.1, page 41
The front panel line out connector	Section 2.8.3, page 49

NOTE

Some of the audio connectors are optional and are not installed on all versions of the board.

1.10 Hardware Monitor Component (Optional)

The hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing
- Remote thermal diode sensing for direct monitoring of processor temperature
- Power supply monitoring (+12, +5, +3.3, +2.5, V_{CCP}) to detect levels above or below acceptable values
- SMBus interface
- The hardware monitor component enables the board to be compatible with the *Wired for Management (WfM) Specification*

For information about…	Refer to…
The board's compatibility with the WfM specification	Table 3, page 14

1.11 LAN Subsystem (Optional)

The Intel 82559 Fast Ethernet Wired for Management (WfM) PCI LAN subsystem provides both 10Base-T and 100Base-TX connectivity. Features include:

- 32-bit, 33 MHz direct bus mastering on the PCI bus
- Shared memory structure in the host memory that copies data directly to/from host memory
- 10Base-T and 100Base-TX capability using a single RJ-45 connector with connection and activity status LEDs
- IEEE 802.3u Auto-Negotiation for the fastest available connection
- Jumperless configuration; the LAN subsystem is completely software-configurable

For information about…	Refer to…
The WfM specification	Table 3, page 14

1.11.1 Intel® 82559 PCI LAN Controller (Optional)

The Intel 82559 PCI LAN controller's features include:

- CSMA/CD Protocol Engine
- PCI bus interface
- DMA engine for movement of commands, status, and network data across the PCI bus
- Integrated physical layer interface, including:
  - Complete support for the 10Base-T and 100Base-TX network interfaces; when in 10 Mbit/sec mode, the interface drives the cable directly
  - A complete set of Media Independent Interface (MII) management registers for control and status reporting
  - 802.3u Auto-Negotiation for automatically establishing the best operating mode when connected to other 10Base-T or 100Base-TX devices, whether half- or full-duplex capable
  - Integrated power management features, including support for Wake on LAN† technology

For information about…	Refer to…
The LAN subsystem's PCI specification compliance	Table 3, page 14

1.11.2 LAN Subsystem Software (Optional)

The Intel 82559 Fast Ethernet WfM PCI LAN software and drivers are available from Intel's World Wide Web site.

For information about…	Refer to…
Obtaining LAN software and drivers	Section 1.2, page 14

1.11.3 RJ-45 LAN Connector LEDs (Optional)

Two LEDs are built into the RJ-45 LAN connector. Table 7 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 7. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Mbit/sec speed is selected.
	On	100 Mbit/sec speed is selected.
Yellow	Off	LAN link is not established.
	On (steady state)	LAN link is established.
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN.

1.12 Power Management Features

Power management is implemented at several levels, including:

- Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - Wake on LAN technology
  - Instantly Available technology
  - Wake on Ring
  - Resume on Ring
  - Wake from USB
  - PME# wakeup support

1.12.1 ACPI

If the board is used with an ACPI-aware operating system, the BIOS can provide ACPI support. ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires the support of an operating system that provides full ACPI functionality. ACPI features include:

- Plug and Play (including bus and device enumeration).
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives.
- Methods for achieving less than 30-watt system operation in the Power On Suspend sleeping state, and less than 5-watt system operation in the Suspend to RAM sleeping state.
- A Soft-off feature that enables the operating system to power off the computer.
- Support for multiple wake up events (see Table 10 on page 30).
- Support for a front panel power and sleep mode switch. Table 8 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 8. Effects of Pressing the Power Switch

If the system is in this state…		…and the power switch is pressed for	…the system enters this state
Off	(ACPI G2/S5 state)	Less than four seconds	Power on
On	(ACPI G0 state)	Less than four seconds	Soft off/Suspend
On	(ACPI G0 state)	More than four seconds	Fail safe power off
Sleep	(ACPI G1 state)	Less than four seconds	Wake up
Sleep	(ACPI G1 state)	More than four seconds	Power off

For information about…	Refer to…
The board's compliance level with ACPI	Table 3, page 14

1.12.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 9 lists the power states supported by the GS810 board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 9. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power (Note1)
G0 - working state	S0 – working.	C0 - working	D0 - working state	Full power > 30 W
G1 - sleeping state	S1 - CPU stopped.	C1 - stop grant	D1, D2, D3 - device specification specific.	5 W < power < 30 W
G1 - sleeping state	S3 - Suspend-to-RAM. Context saved to RAM.	No power	D3 - no power except for wake up logic.	Power < 5 W (Note2)
G2/S5	S5 - Soft off. Context not saved. Cold boot is required.	No power	D3 - no power except for wake up logic.	Power < 5 W (Note2)
G3 - mechanical off. (AC power is disconnected from the computer.)	No power to the system.	No power	D3 - no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.12.1.2 Wake Up Devices and Events

Table 10 lists the devices or specific events that can wake the computer from specific states.

Table 10. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
LAN	S1, S3, S5
Modem	S1, S3, S5
PME#	S1, S3, S5
Power switch	S1, S3, S5
RTC alarm	S1, S3, S5
USB	S1, S3

1.12.1.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure devices that do not have other hardware standards for enumeration and configuration. Onboard PCI devices are not enumerated by ACPI.

1.12.2 Hardware Support

CAUTION

If Wake on LAN and Instantly Available technology features are used, the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current can damage the power supply or cause unreliable operation of the board. The total amount of standby current required depends on the wake devices supported and manufacturing options. *Refer to Section 2.11.3 on page 57 for additional information.*

The board provides several hardware features that support power management, including:

- Power connector
- Fan connectors
- Wake on LAN technology
- Instantly Available technology
- Wake on Ring
- Resume on Ring
- Wake from USB
- PME# wakeup support

Wake on LAN technology and Instantly Available technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Wake on Ring and Resume on Ring enable telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the power management mode being used (ACPI).

NOTE

The use of Wake on Ring, Resume on Ring, and Wake from USB technologies from an ACPI state require the support of an operating system that provides full ACPI functionality.

1.12.2.1 Power Connector

When used with an ATX-compliant power supply that supports remote power on/off, the GS810 board can turn off the system power through software control.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

For information about…	Refer to…
The location of the power connector	Figure 7, page 43
The signal names of the power connector	Table 27, page 46
The ATX specification	Table 3, page 14

1.12.2.2 Fan Connectors

The board has two fan connectors, one of which is a manufacturing option. The functions of these connectors are described in Table 11.

Table 11. Fan Connector Descriptions

Connector	Function
Processor fan	Provides +12 V DC for a processor fan or active fan heatsink.
Chassis fan (optional)	Provides +12 V or 6.9 V DC for a system or chassis fan. The fan voltage can be switched to provide high and low fan speeds depending on the power management state of the computer.

For information about…	Refer to…
The location of the fan connectors	Figure 7, page 43
The signal names of the processor fan connector	Table 23, page 44
The signal names of the chassis fan connector	Table 29, page 47

1.12.2.3 Wake on LAN Technology

⚠ CAUTION

For Wake on LAN technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Wake on LAN technology can damage the power supply or cause unreliable operation of the board. Refer to Section 2.11.3 on page 57 for additional information.

Wake on LAN technology enables remote wakeup of the computer through a network. The LAN subsystem, whether onboard or as a PCI bus network adapter, monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet† frame, the LAN subsystem asserts a wakeup signal that powers up the computer. The board supports Wake on LAN technology through the PCI bus PME# signal.

1.12.2.4 Instantly Available Technology

⚠ CAUTION

For Instantly Available technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when using this feature can damage the power supply. Refer to Section 2.11.3 on page 57 for additional information.

Instantly Available technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off and the fans are off). When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 10 on page 30 lists the devices and events that can wake the computer from the S3 state.

The board supports the *PCI Bus Power Management Interface Specification*. For information on the versions of this specification, see Table 3, page 14. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

1.12.2.5 Wake on Ring

NOTE

Wake on Ring requires the use of a modem (external USB or internal PCI) that supports the Wake on Ring feature.

The operation of Wake on Ring can be summarized as follows:

- Powers up the computer from the ACPI S5 state
- Requires two calls to access the computer:
  - First call restores the computer
  - Second call enables access (when the appropriate software is loaded)
- Detects incoming calls differently for external as opposed to internal modems:
  - For external USB modems, the USB bus is monitored for the RING_DETECT signal
  - For internal PCI modems, incoming calls are detected through the PCI bus PME# signal

1.12.2.6 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from the ACPI S1 state
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems

1.12.2.7 Wake from USB

USB bus activity wakes the computer from an ACPI S1 or S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.12.2.8 PME# Wakeup Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1, S3, or S5 state.

2 Technical Reference

What This Chapter Contains

2.1 Introduction

Sections 2.2 – 2.6 contain several standalone tables. Table 12 describes the system memory map, Table 13 shows the I/O map, Table 14 lists the DMA channels, Table 15 defines the PCI configuration space map, and Table 16 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Map

Table 12. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 524288 K	100000 - 1FFFFFFF	511 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 K	Conventional memory

2.3 I/O Map

Table 13. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA Controller
0020 - 0021	2 bytes	Programmable Interrupt Control (PIC)
0040 - 0043	4 bytes	System Timer
0060	1 byte	Keyboard controller byte – reset IRQ
0061	1 byte	System Speaker
0064	1 byte	Keyboard controller, CMD/STAT byte
0070 - 0071	2 bytes	System CMOS / Real Time Clock
0072 - 0073	2 bytes	System CMOS
0080 - 008F	16 bytes	DMA Controller
0092	1 byte	Fast A20 and PIC
00A0 - 00A1	2 bytes	PIC
00B2 - 00B3	2 bytes	Reserved
00C0 - 00DF	32 bytes	DMA
00F0	1 byte	Numeric data processor
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
02E8 - 02EF[1]	8 bytes	COM4/video (8514A)
02F8 - 02FF[1]	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
03B0 - 03BB	12 bytes	Intel 82810 – DC100 GMCH
03C0 - 03DF	32 byte	Intel 82810 – GMCH
03E8 - 03EF	8 bytes	COM3
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0CF8 - 0CFB[2]	4 bytes	PCI configuration address register
0CF9[3]	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register

continued

Table 13. I/O Map (continued)

Address (hex)	Size	Description
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers
96 contiguous bytes starting on a 128-byte divisible boundary		ICH (ACPI + TCO)
64 contiguous bytes starting on a 64-byte divisible boundary		On Board Resource
256 contiguous bytes starting on a 256-byte divisible boundary		ICH Audio Mixer
64 contiguous bytes starting on a 64-byte divisible boundary		ICH Audio Bus Mixer
32 contiguous bytes starting on a 32-byte divisible boundary		ICH (USB)
16 contiguous bytes starting on a 16-byte divisible boundary		ICH (SMBus)
4096 contiguous bytes starting on a 4096-byte divisible boundary		Intel 82801AA PCI Bridge
32 contiguous bytes starting on a 32-byte divisible boundary		Intel 82559 LAN Controller
96 contiguous bytes starting on a 128-byte divisible boundary		IT8761E PME Status

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available because of ICH addresses aliasing. For information about ICH addressing, refer to this Intel Web site:

http://developer.intel.com/design/chipsets/datashts/

2.4 DMA Channels

Table 14. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Available
1	8- or 16-bits	Available
2	8- or 16-bits	Open
3	8- or 16-bits	Open / Available
4		Reserved - cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.5 PCI Configuration Space Map

Table 15. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82810 component
00	01	00	Graphics controller of Intel 82810 component
00	1E	00	Link to PCI bridge
00	1F	00	PCI-to-LPC bridge
00	1F	01	IDE controller
00	1F	02	USB controller #1
00	1F	03	SMBus controller
00	1F	04	Reserved
00	1F	05	AC ’97 audio controller
00	1F	06	AC ’97 modem controller
01	08	00	Intel 82559 PCI LAN controller
01	08	01	Mini-PCI slot

2.6 Interrupts

Table 16. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2* (available unless used for debug port)
4	COM1* (available unless used for debug port)
5	Audio / User available
6	User available
7	User available*
8	Real-time clock
9	Reserved for ICH system management bus
10	User available
11	Windows Sound System* / User available
12	User available
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

* Default, but can be changed to another IRQ.

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)

The ICH PCI-to-LPC bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the GS810 board and therefore share the same interrupt. Table 17 lists the PIRQ signals and shows how the signals are connected to the PCI bus connectors and to onboard PCI interrupt sources.

Table 17. PCI Interrupt Routing Map

PCI Interrupt Source	ICH PIRQ Signal Name			
	PIRQA	**PIRQB**	**PIRQC**	**PIRQD**
AGP Controller		INTA	INTB	
ICH Audio Controller		INTB		
ICH USB Controller				INTD
Mini PCI Connector (J2B1)	INTA	INTB	INTA	INTB
PCI LAN Controller				INTA

⟹ NOTE

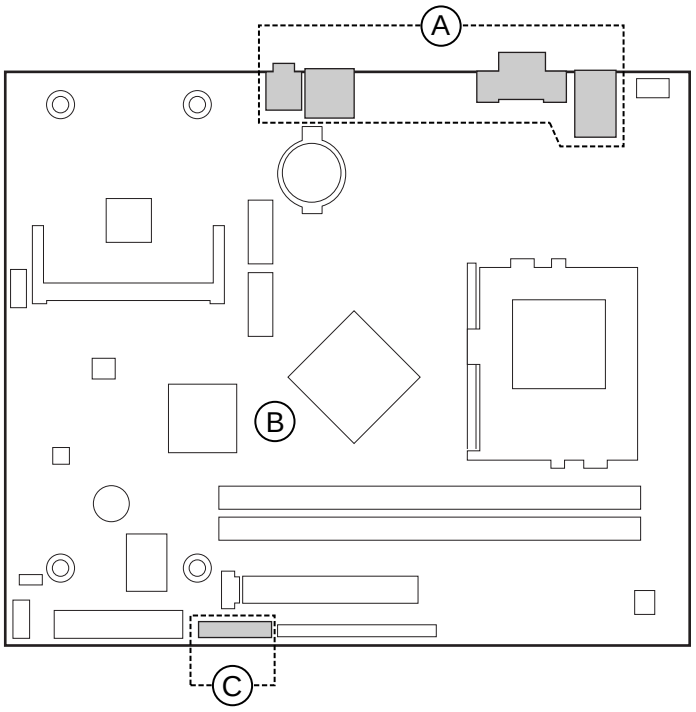
The ICH can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 10, 11, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

2.8 Connectors

CAUTION

Only the back panel connectors of the GS810 board have overcurrent protection. The internal board connectors are not overcurrent protected, and should connect only to devices inside the computer chassis, such as fans and internal peripherals. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

This section describes the board's connectors. The connectors can be divided into three groups, as shown in Figure 5.



A. Back panel connectors (see page 41)

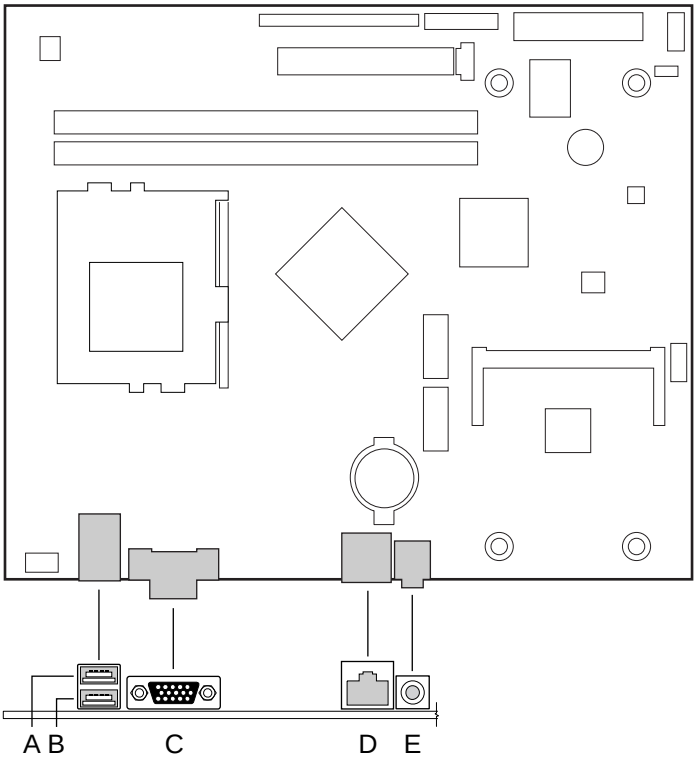
B. Midboard connectors (see page 43)

C. Front panel connectors (see page 49)

Figure 5. Connector Groups

2.8.1 Back Panel Connectors

Figure 6 shows the location of the back panel connectors.



Item	Description	
A	USB port 0	(see Table 18, page 42)
B	USB port 1	(see Table 18, page 42)
C	VGA port	(see Table 19, page 42)
D	LAN (optional)	(see Table 20, page 42)
E	Audio line out	(see Table 21, page 42)

Figure 6. Back Panel Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality may occur if passive (non-amplified) speakers are connected to this output.

Table 18. USB Connectors

Pin	Signal Name
1	+5 V (fused)
2	USBP0# / USBP1#
3	USBP0 / USBP1
4	Ground

Table 19. VGA Port Connector

Pin	Signal Name
1	Red
2	Green
3	Blue
4	No connect
5	Ground
6	Ground
7	Ground
8	Ground
9	Fused VCC
10	Ground
11	No connect
12	MONID1
13	HSYNC
14	VSYNC
15	MONID2

Table 20. LAN Connector (Optional)

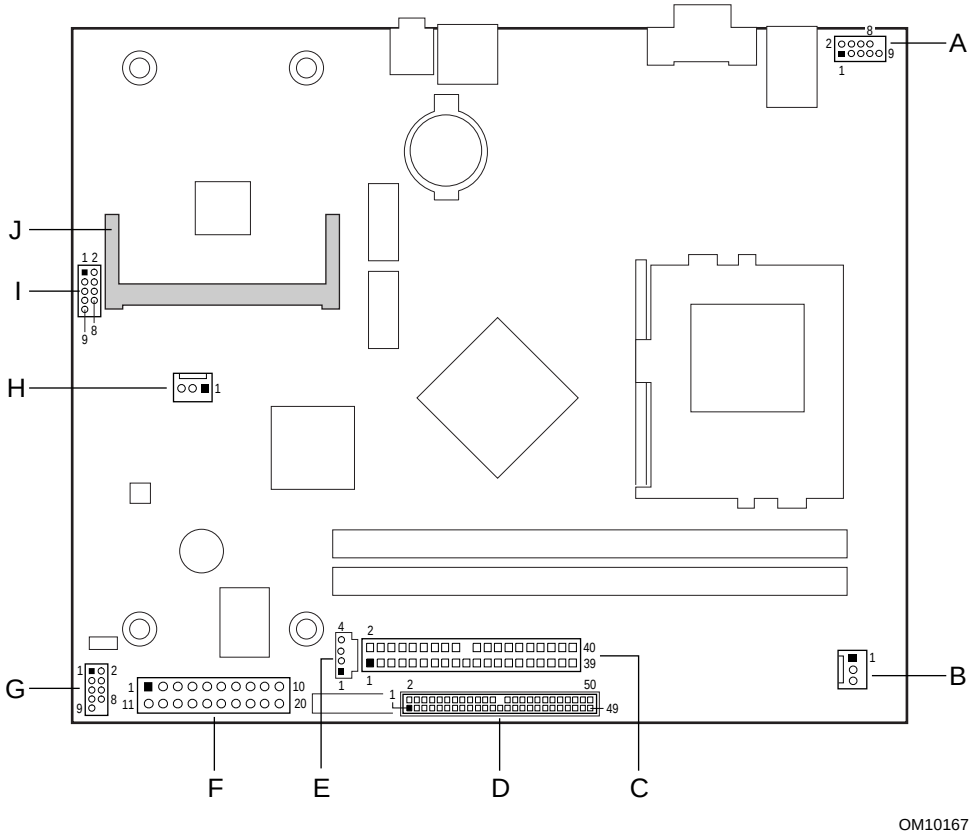
Pin	Signal Name
1	TX+
2	TX-
3	RX+
4	Ground
5	Ground
6	RX-
7	Ground
8	Ground

Table 21. Audio Line Out Connector

Pin	Signal Name
Tip	Audio left out
Ring	Audio right out
Sleeve	Ground

2.8.2 Midboard Connectors

Figure 7 shows the location of the midboard connectors.



Item	Description		Reference Designator
A	Front panel USB connector	(see Table 22, page 44)	J1J1
B	Processor fan	(see Table 23, page 44)	J7J1
C	Primary IDE	(see Table 24, page 45)	J7E1
D	Slimline IDE	(see Table 25, page 46)	J8E1
E	ATAPI CD-ROM (optional)	(see Table 26, page 46)	J7C1
F	Power	(see Table 27, page 46)	J8B1
G	Serial debug port (optional)	(see Table 28, page 47)	J8A1
H	Chassis fan (optional)	(see Table 29, page 47)	J4B1
I	Auxiliary Audio	(see Table 30, page 47)	J3A2
J	Mini-PCI	(see Table 31, page 48)	J2B1

Figure 7. Midboard Connectors

For information about…	Refer to…
The power connector	Section 1.12.2.1, page 31
The functions of the fan connectors	Section 1.12.2.2, page 31

⚠ CAUTION

The +5 V line shown in Table 22, is not fused on the GS810 board. A fuse must be provided in this line before the line reaches a user-accessible outside connector. Failure to provide a fuse in the +5 V line could damage the board and/or power supply.

Table 22. Front Panel USB Connector (J1J1)

Pin	Signal Name
1	+5 V (Not fused, see *Caution*)
2	+5 V (Not fused, see *Caution*)
3	USBP3#
4	USBP4#
5	USBP3
6	USBP4
7	Ground
8	Ground
9	Key

Table 23. Processor Fan Connector (J7J1)

Pin	Signal Name
1	Ground
2	+12 V
3	Ground

Table 24. Primary IDE Connector (J7E1)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Ground
29	DDACK0#	30	Ground
31	IRQ 14	32	No connect
33	DAG1 (Address 1)	34	GPIO_DMA66_Detect_Pri
35	DAG0 (Address 0)	36	DAG2 (Address 2)
37	Chip Select 1P#	38	Chip Select 3P#
39	Activity#	40	Ground

Table 25. Slimline IDE Connector (J8E1)

Pin	Signal Name	Pin	Signal Name
1	AUD_LCR_R	2	AUD_RCD_R
3	AUD_CDGND_R	4	AUD_CDGND_R
5	No connect	6	No connect
7	Reset IDE	8	Ground
9	Data 7	10	Data 8
11	Data 6	12	Data 9
13	Data 5	14	Data 10
15	Data 4	16	Data 11
17	Data 3	18	Data 12
19	Data 2	20	Data 13
21	Data 1	22	Data 14
23	Data 0	24	Data 15
25	Ground	26	Key
27	DMARQ	28	Ground
29	I/O Write#	30	Ground
31	I/O Read#	32	Ground
33	IOCHRDY	34	CSEL (Cable Select pull-up)
35	DDACK1#	36	Ground
37	IRQ 15	38	No connect
39	DAG1 (Address 1)	40	No connect
41	DAG0 (Address 0)	42	DAG2 (Address 2)
43	Chip Select 1S#	44	Chip Select 3S#
45	No connect	46	Ground
47	VCC	48	VCC
49	Ground	50	No connect

Table 26. ATAPI CD-ROM Connector (J7C1)

Pin	Signal Name
1	AUD_LCD_R
2	AUD_CD_GND
3	AUD_CD_GND
4	AUD_RCD_L

Table 27. Power Connector (J8B1)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	No connect
9	+5 VSB	19	+5 V
10	+12 V	20	+5 V

Table 28. Serial Debug Port Connector (J8A1)

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	DSR (Data Set Ready)
3	SIN # (Serial Data In)
4	RTS (Request to Send)
5	SOUT # (Serial Data Out)
6	CTS (Clear to Send)
7	DTR (Data Terminal Ready)
8	RI (Ring Indicator)
9	Ground

Table 29. Chassis Fan Connector (J4B1)

Pin	Signal Name
1	Ground
2	Fan Supply Voltage (6.9 V and 12 V)
3	FAN_TACH1

Table 30. Auxiliary Audio Connector (J3A2)

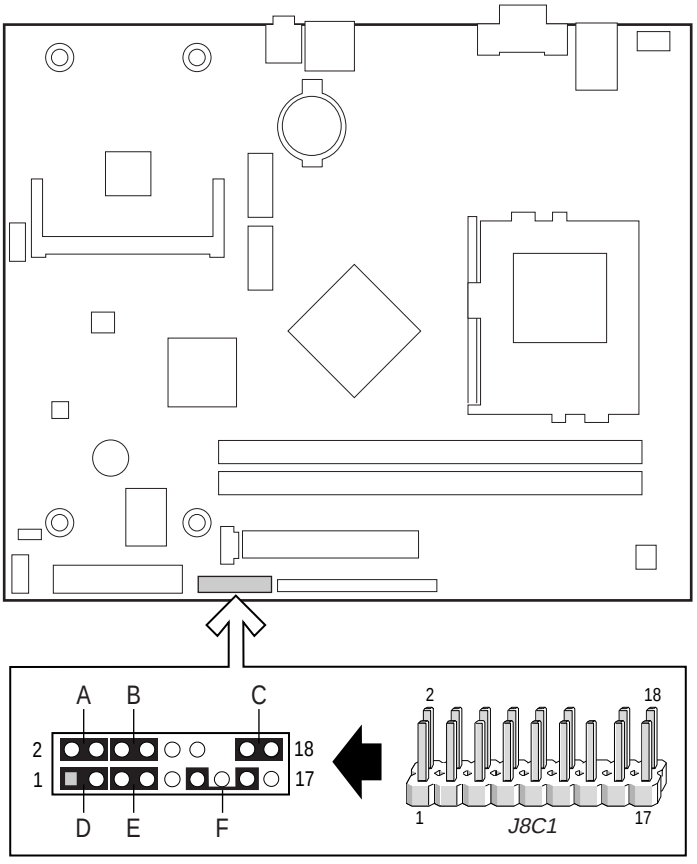
Pin	Signal Name	Pin	Signal Name
1	AUD_MIC	2	Ground
3	AUD_MIC_BIAS	4	No connect
5	Ground	6	Key
7	Reserved	8	Reserved
9	Reserved	10	Reserved

Table 31. Mini PCI Connector (J2B1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	Tip	2	Ring	63	3.3 V	64	FRAME#
3	8PMJ-3	4	8PMJ-1	65	CLKRUN#	66	TRDY#
5	8PMJ-6	6	8PMJ-2	67	SERR#	68	STOP#
7	8PMJ-7	8	8PMJ-4	69	Ground	70	3.3 V
9	8PMJ-8	10	8PMJ-5	71	PERR#	72	DEVSEL#
11	LED1_GRNP	12	LED2_YELP	73	C/BE1#	74	Ground
13	LED1_GRNN	14	LED2_YELN	75	AD14	76	AD15
15	Reserved	16	Reserved	77	Ground	78	AD13
17	INTB#	18	+5 V	79	AD12	80	AD11
19	3.3 V	20	INTA#	81	AD10	82	Ground
21	Reserved	22	Reserved	83	Ground	84	AD09
23	Ground	24	3.3VAUX	85	AD08	86	C/BE0#
25	CLK	26	RST#	87	AD07	88	3.3 V
27	Ground	28	3.3 V	89	3.3 V	90	AD06
29	REQ#	30	GNT#	91	AD05	92	AD04
31	3.3 V	32	Ground	93	Reserved	94	AD02
33	AD31	34	PME#	95	AD03	96	AD00
35	AD29	36	Reserved	97	+5 V	98	Reserved
37	Ground	38	AD30	99	AD01	100	Reserved
39	AD27	40	3.3 V	101	Ground	102	Ground
41	AD25	42	AD28	103	AC_SYNC	104	M66EN
43	Reserved	44	AD26	105	AC_SDATA_INA	106	AC_SDATA_OUT
45	C/BE3#	46	AD24	107	AC_BIT_CLK	108	AC_SDATA_INB
47	AD23	48	IDSEL	109	AC_CODEC_CLK	110	AC_RESET#
49	Ground	50	Ground	111	MOD_AUDIO_MON	112	Reserved
51	AD21	52	AD22	113	AUDIO_GND	114	Ground
53	AD19	54	AD20	115	SYS_AUDIO_OUT	116	SYS_AUDIO_IN
55	Ground	56	PAR	117	SYS_AUDIO_OUT GND	118	SYS_AUDIO_IN GND
57	AD17	58	AD18	119	AUDIO_GND	120	AUDIO_GND
59	C/BE2#	60	AD16	121	No connect	122	MPCIACT#
61	IRDY#	62	Ground	123	VCC5A	124	3.3VAUX

2.8.3 Front Panel Connector

Figure 8 shows the location of the front panel connector. Table 32 lists the signal names of the front panel connector.



OM10168

Item	Pins	Description
A	2 and 4	Power / Sleep / Message waiting LED
B	6 and 8	Power switch
C	16 and 18	Reserved
D	1 and 3	Hard drive activity LED
E	5 and 7	Reset switch
F	11 and 15	Front panel stereo audio line out

Figure 8. Front Panel Connector

Table 32. Front Panel Connector (J8C1)

Function	Pin	Signal Name	In/Out	Signal Description
Power / Sleep / Message waiting LED	2	HDR_BLNK_GRN	Out	Front panel green LED
	4	HDR_BLNK_YEL	Out	Front panel yellow LED
Power switch	6	SW_ON#	In	Power switch
	8	GND		Ground
Hard drive activity LED	1	HD_LED_PWR	Out	Hard disk LED pull-up (330 Ω) to +5 V
	3	HD_LED#	Out	Hard disk active LED
Reset switch	5	GND		Ground
	7	FP_RST#	In	Reset switch
Front panel stereo audio line out	11	AUD_LM4880_ROUT	Out	Front panel right channel audio output
	15	AUD_LM4880_LOUT	Out	Front panel left channel audio output
Miscellaneous	9	VCC	Out	+5 V
	10	ICH_SERVICE	In	Reserved
	12	GND		Ground
	13	GND		Ground
	14	(Pin removed)		No connect
	16	N/A		Reserved
	17	VCC		+5 V
	18	N/A		Reserved

2.8.3.1 Power/Sleep/Message Waiting LED Connector

Pins 2 and 4 can be connected to a single- or dual-colored LED. Table 33 shows the possible states for a single-colored LED.

Table 34 shows the possible states for a dual-colored LED.

Table 33. States for a Single-Colored Power LED

LED State	Description	ACPI State
Off	Power off	S3, S5
Steady Green	Running	S0
Blinking Green	Running/message waiting	S0

Table 34. States for a Dual-Colored Power LED

LED State	Description	ACPI State
Off	Power off	S5
Steady Green	Running	S0
Blinking Green	Running/message waiting	S0
Steady Yellow	Sleeping	S1, S3
Blinking Yellow	Sleeping/message waiting	S1, S3

NOTE

To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

2.8.3.2 Power Switch Connector

Pins 6 and 8 can be connected to a front panel power switch. The switch must pull pin-6 to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.8.3.3 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface.

2.8.3.4 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the board resets and runs the POST.

2.8.3.5 Front Panel Audio Line Output Connector

Pins 11 and 15 are left- and right-channel audio outputs.

2.9 Jumper Block

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, damage to the GS810 board could occur.

Figure 9 shows the location of the BIOS Setup jumper block. This 3-pin jumper block determines the BIOS Setup program's mode. Table 35 describes the jumper settings for the three modes: normal, configure, and recovery.

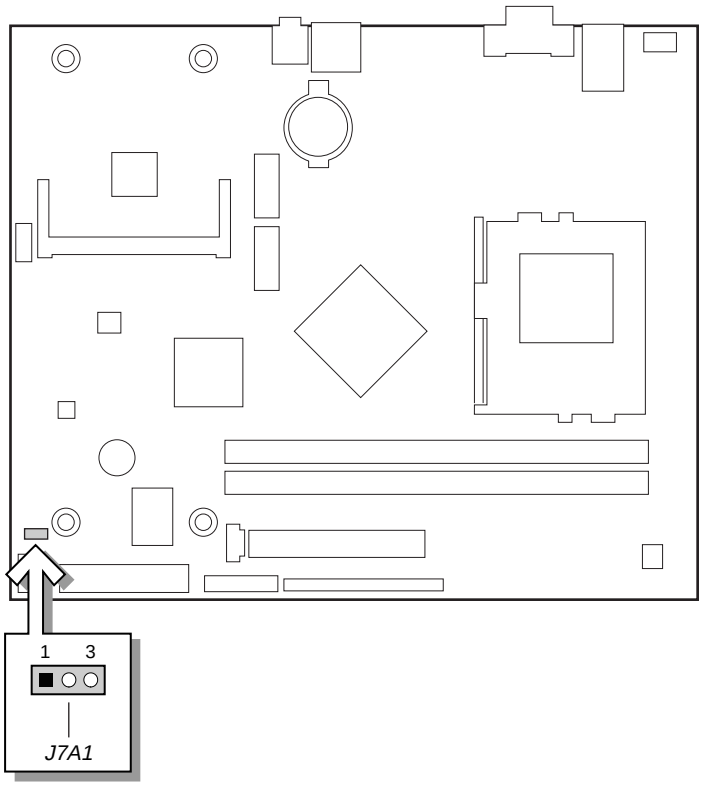
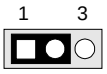
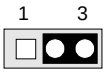
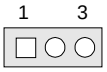


Figure 9. Location of the Jumper Block

Table 35. BIOS Setup Configuration Jumper Settings (J7A1)

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A 1.44 MB BIOS recovery diskette (LS-120) or a CD-ROM with a copy of the BIOS recovery file is required.

For information about…	Refer to…
How to access the BIOS Setup program	Section 4.1, page 73
The maintenance menu of the BIOS Setup program	Section 4.2, page 74
BIOS recovery	Section 3.7, page 69

2.10 Mechanical Considerations

2.10.1 FlexATX Form Factor

The GS810 board is designed to fit into an ATX- or microATX-form-factor chassis. Figure 10 illustrates the mechanical form factor for the board. Dimensions are given in inches (millimeters). The outer dimensions are 9.0 inches by 7.5 inches (228.60 millimeters by 190.50 millimeters). Location of the I/O connectors and mounting holes are in compliance with the FlexATX addendum of the microATX specification (see Table 3, page 14).

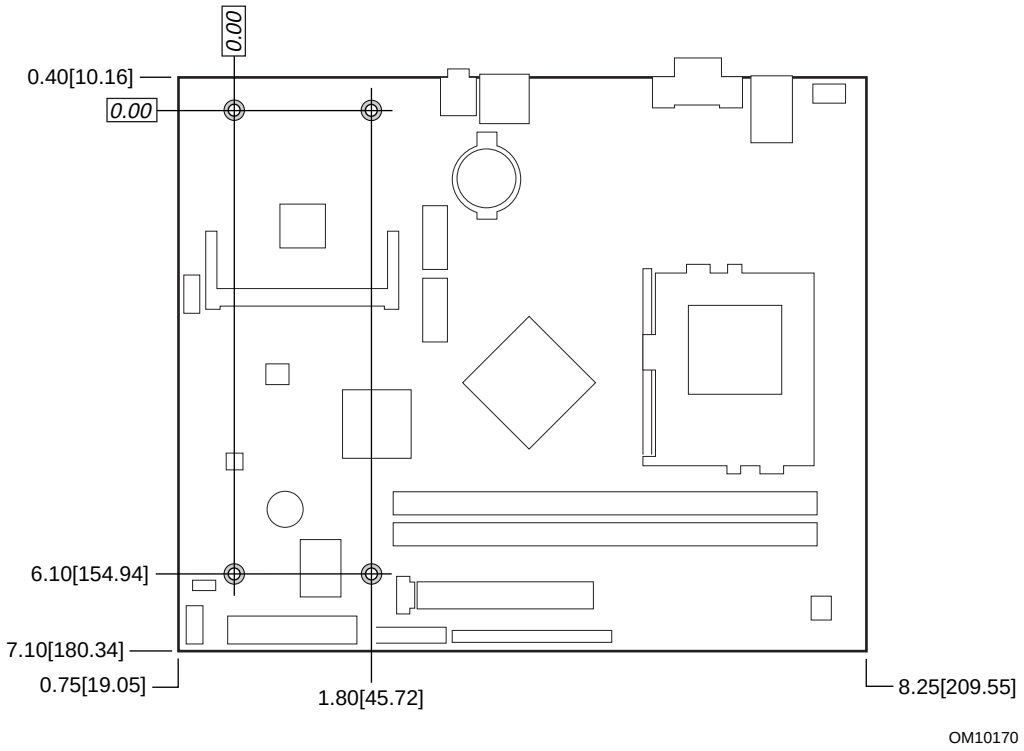


Figure 10. Board Dimensions

2.10.2 I/O Shield

The back panel I/O shield for the GS810 board must meet specific dimensional requirements. Systems based on this board need the back panel I/O shield to pass certification testing. Figure 11 shows the critical dimensions of the I/O shield. Dimensions are given in inches (millimeters). For dimensions given to two decimal places, the tolerance is ±0.02 inches (±0.51 millimeters). Both figures indicate the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Table 3, page 14 for information about the ATX specification.

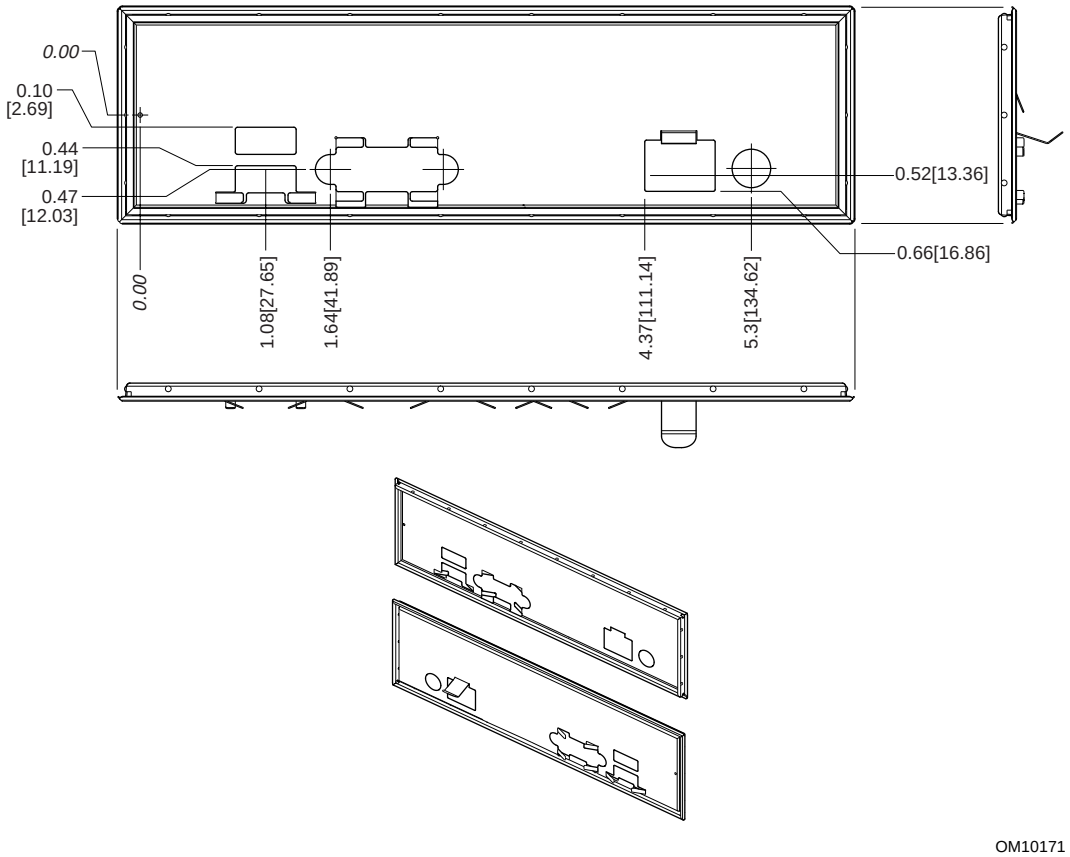


Figure 11. I/O Shield Dimensions

2.11 Electrical Considerations

2.11.1 Add-in Board Considerations

A mini-PCI card may draw a maximum of 2.0 Watts. This represents the total power drawn from all available power sources at the connector (5 V, 3.3 V, 3.3 VAUX). Mini-PCI differs from PCI local bus in the following ways:

- Mini PCI is not a dual or multiple Vcc implementation of PCI. There is only one Vcc logic supply of 3.3 V. +5 V is available for functions requiring it.
- Total power consumption from all sources (+5 V, +3.3 V, and +3.3 Vaux) is limited to 2.0 W.
- PCI 64-bit bus expansion is not supported.

For information about…	Refer to…
The mini-PCI specification	Table 3, page 14

2.11.2 Power Consumption

Table 36 lists voltage and current specifications for a computer that contains the GS810 board and the following:

- 500 MHz Intel Celeron processor with a 128 KB cache
- 128 MB SDRAM
- 3.2 GB IDE hard disk drive
- 24X Mobile IDE CD-ROM drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows† 98 desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with a typical 145 W power supply, nominal input voltage and frequency, with true RMS wattmeter at the line input.

Table 36. Power Usage

Mode	AC Watts	DC Amps at:				
		+3.3 V	+5 V	+12 V	-12 V	+5 VSB
Windows 98 ACPI S0	28 W	1.38 A	0.752 A	0.290 A	0.014 A	0.212 A
Windows 98 ACPI S1	22 W	1.23 A	0.564 A	0.225 A	0.013 A	0.180 A
Windows 98 ACPI S3 (with onboard LAN)	2 W	0.0 A	0.0 A	0.0 A	0.0 A	0.198 A
Windows 98 ACPI S3 (without onboard LAN)	<1W	0.0 A	0.0 A	0.0 A	0.0 A	0.086 A
Windows 98 ACPI S5 (with onboard LAN)	2 W	0.0 A	0.0 A	0.0 A	0.0 A	0.190 A
Windows 98 ACPI S5 (without onboard LAN)	<1W	0.0 A	0.0 A	0.0 A	0.0 A	0.078 A

2.11.3 Power Supply Considerations

System integrators should refer to the power usage values listed in Table 36 when selecting a power supply for use with this motherboard. The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

For information about…	Refer to…
The ATX form factor specification	Table 3, page 14

2.11.4 Standby Current Requirements

Table 37 lists the +5 V standby current consumed by the board itself in two configurations and does not include external peripherals or add-in cards.

Table 37. Standby Current Usage

Configuration	+5 V Standby Current Required
GS810 board with no onboard networking	0.060 A
GS810 board with onboard networking	0.204 A

NOTE

These standby current requirements are system configuration dependent.

2.11.5 Fan Power Requirements

Table 38 lists the maximum DC voltage and current requirements for the fans when the board is in sleep mode or normal operating mode. Power consumption is independent of the operating system used and other variables.

Table 38. Fan DC Power Requirements

Fan Type	Mode	Voltage	Maximum Current (Amps)
Chassis (J4B1)	Sleep	+ 6.9 VDC	0.250 mA (current limited)
	Normal	+ 12 VDC	0.250 mA (current limited)
Processor (J7J1)	Sleep	+ 12 VDC	0.250 mA (current limited)
	Normal	+ 12 VDC	0.250 mA (current limited)

For information about…	Refer to…
The location of the chassis and processor fan connectors	Figure 7, page 43
The signal names of the chassis fan connector	Table 29, page 47
The signal names of the processor fan connector	Table 23, page 44

2.12 Thermal Considerations

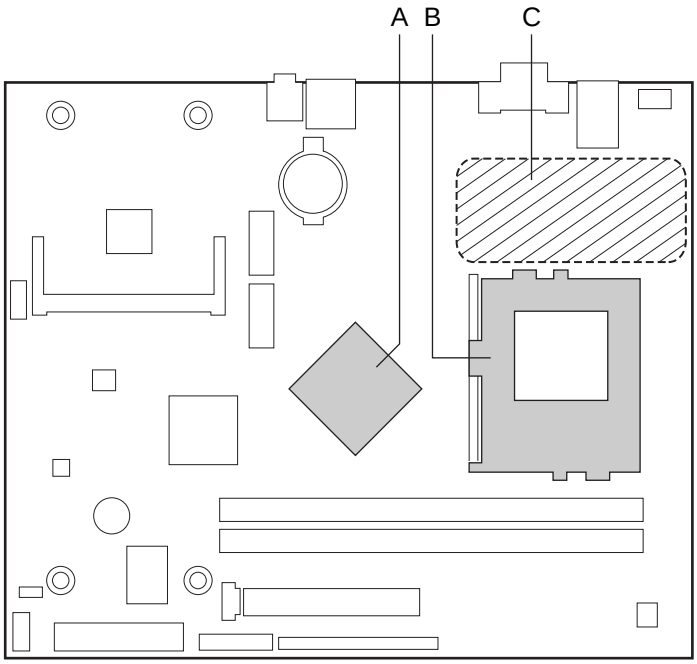
CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 °C to 10 °C could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

CAUTION

The voltage regulator area can reach a temperature of up to 85 °C in an open chassis. System integrators should ensure that proper airflow is maintained in the voltage regulator area (item C in Figure 12). Failure to do so may result in damage to the voltage regulator area.

Figure 12 shows the localized high-temperature zones.



A	Intel 82810 GMCH
B	Processor
C	Processor voltage regulator area

Figure 12. High Temperature Zones

Table 39 provides maximum component case temperatures for board components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the board.

Table 39. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium III processor, 100 MHz system bus frequency	For processor case temperature, see processor datasheets and processor specification updates.
Celeron Processor	
Intel 82810 GMCH	70 °C

For information about…	Refer to…
Intel Celeron processor datasheets and specification updates	Table 3, page 14
Intel Pentium III processor datasheets and specification updates	Table 3, page 14

2.13 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 55 ºC.

GS810 board MTBF: 221,013.52 hours

2.14 Environmental

Table 40 lists the environmental specifications for the GS810 board.

Table 40. Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	30 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz : 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz : 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the GS810 board's compliance with safety and EMC regulations.

2.15.1 Safety Regulations

Table 41 lists the safety regulations the GS810 board complies with when it is correctly installed in a compatible host system.

Table 41. Safety Regulations

Regulation	Title
UL 1950/CSA950, 3rd edition, Dated 07-28-95	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Community)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

2.15.2 EMC Regulations

Table 42 lists the EMC regulations the GS810 board complies with when it is correctly installed in a compatible host system.

Table 42. EMC Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22, 2nd Edition, 1993 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
VCCI Class B (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
EN55022 (1994) (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN50082-1 (1992)	Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)
ICES-003 (1997)	Interference-Causing Equipment Standard, Digital Apparatus, Class B (Including CRC c.1374). (Canada)
AS/NZ 3548	Australian Communications Authority (ACA), Standard for Electromagnetic Compatibility.

2.15.3 Certification Markings

This printed circuit assembly has the following product certification markings:

- UL Joint Recognition Mark: Consists of small c followed by a stylized backward UR and followed by a small US (Component side)
- Manufacturer's recognition mark: Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (Solder side)
- UL File Number for desktop boards: E139761 (Component side)
- PB Part Number: Intel bare circuit board part number (Solder side) 747129-002
- Battery "+ Side Up" marking: located on the component side of the board in close proximity to the battery holder
- FCC Logo/Declaration: (Solder side)
- ACA (C-Tick) mark: Consists of a unique letter C, with a tick mark; followed by N-232. Located on the component side of the GS810 board and on the shipping container
- CE Mark: (Component side) The CE mark should also be on the shipping container

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The GS810 board uses an Intel/AMI BIOS, which is stored in flash memory and can be updated. In addition to the BIOS, the flash memory contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

This board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

BIOS options and their function may vary if the board is an OEM manufactured product. Consult your system manufacturer for information regarding OEM manufactured products.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. Intel production BIOS can be identified by the ".86A." within the BIOS identification string. All other identifiers are custom OEM products. Consult your system manufacturer for information regarding a custom OEM manufactured product.

The initial production BIOS is identified as GS81010A.86A. The current production BIOS is identified as GS81011A.86A.

For information about…	Refer to…
The board's compliance level with Plug and Play	Table 3, page 14

3.2 BIOS Flash Memory Organization

The Intel 82802AB Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable. Figure 13 shows the organization of the flash memory.

The last two 8 KB blocks of the fault tolerance area are the parameter blocks. These blocks contain data such as BIOS updates, vital product data (VPD), logo, System Management BIOS (SMBIOS) interface, and extended system configuration data (ESCD) information. The backup block contains a copy of the fault tolerance block.

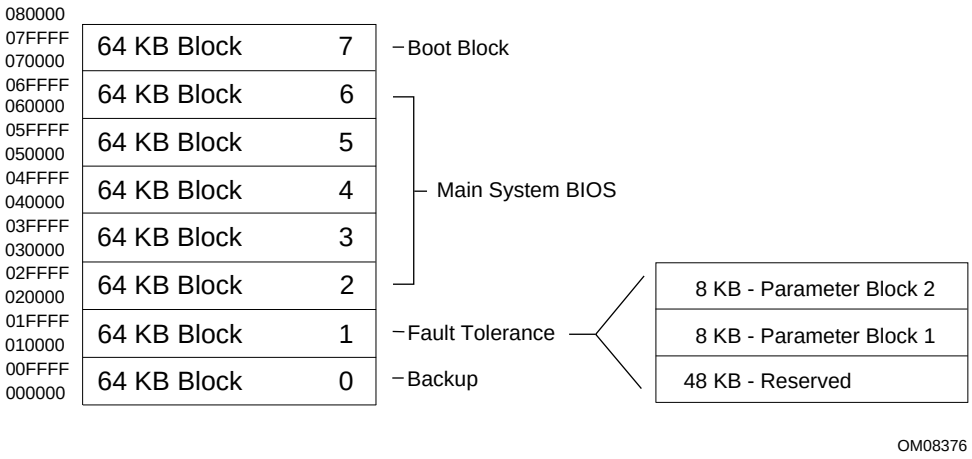


Figure 13. Memory Map of the Flash Memory Device

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or an add-in card. Autoconfiguration lets a user insert or remove a mini-PCI card without having to configure the system. When a user turns on the system after adding a mini-PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources.

PCI devices can share an interrupt. Autoconfiguration information is stored in ESCD format.

For information about…	Refer to…
The versions of PCI and Plug and Play supported by this BIOS	Table 3, page 14

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA-66 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Table 3, page 14 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66 features the following items are required:

- An ATA-66 peripheral device
- An ATA-66 compatible cable
- ATA-66 operating system device drivers

NOTE

ATA-66 compatible cables are backward compatible with drivers using slower IDE transfer protocols. If an Ultra ATA-66 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate for either drive is 33 MB/sec.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT†, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about…	Refer to…
The board's compliance level with SMBIOS	Table 3, page 14

3.5 USB Legacy Support

USB legacy support enables USB devices such as keyboards, mice, and hubs to be used even when no operating system USB drivers are in place. By default, USB legacy support is set to Auto. USB legacy support is used in accessing the BIOS Setup program and installing an operating system that supports USB.

This sequence describes how USB legacy support operates in the default (auto) mode.

1. When you power up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is temporarily enabled by the BIOS. This allows you to use a USB keyboard to enter the BIOS Setup program or the maintenance mode.
4. POST completes and disables USB legacy support (unless it was set to Enabled while in the BIOS Setup program. Or if set to Auto while in the BIOS Setup program and a USB keyboard or mouse is connected, then USB legacy support will be enabled).
5. The operating system loads. While the operating system is loading, USB keyboards and mice are not recognized (unless USB legacy support was set to Enabled while in the BIOS Setup program, or if USB legacy support was set to Auto while in the BIOS Setup program and a USB keyboard or mouse is connected). After the operating system loads the USB drivers, the USB devices are recognized by the operating system.

To install an operating system that supports USB, enable USB legacy support or set it to Auto in the BIOS Setup program and follow the operating system's installation instructions. Once the operating system is installed and the USB drivers have been configured, USB legacy support is no longer used. USB legacy support can be left enabled or set to Auto in the BIOS Setup program if needed.

Notes on using USB legacy support:

- Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non-USB aware operating system.
- USB legacy support is for keyboards, mice, and hubs only. Other USB devices are not supported.

3.6 BIOS Updates

The BIOS can be updated from a diskette or CD-ROM using the Intel® Flash Memory Update Utility that is available from Intel. This utility supports the following BIOS maintenance functions:

- Update the flash BIOS from a file on a diskette or CD-ROM
- Change the language section of the BIOS
- Verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS
- Update BIOS boot block

BIOS updates and the Intel Flash Memory Update Utility are available from Intel through the Intel World Wide Web site.

NOTE

Please review the instructions distributed with the update utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 14

3.6.1 Language Support

The BIOS Setup program and help messages are supported in five languages: US English, German, Italian, French, and Spanish. The default language is US English, which is present unless another language is selected in the BIOS Setup program.

3.6.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS update utility. Information about this capability is available on the Intel Support World Wide Web site.

For information about…	Refer to…
The Intel World Wide Web site	Section 1.2, page 14

3.7 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from either a 1.44 MB diskette (for recovery from an LS-120 diskette drive configured as an ATAPI removable IDE device), or from a CD-ROM using the BIOS recovery mode. When recovering the BIOS be aware of the following:

- Because of the small amount of code available in the nonerasable boot block area, there is no video support. You can monitor this procedure by listening to the speaker or looking at the recovery drive LED.
- Two beeps and the end of activity in the recovery drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette or CD-ROM, a bootable 1.44 MB LS-120 diskette or CD-ROM must be created and the BIOS update files copied to it. BIOS updates and the Intel Flash Memory Update Utility are available from Intel Customer Support through the Intel World Wide Web site.

NOTE

BIOS Recovery cannot be accomplished using non-SPD DIMMs. SPD data structure is required for the recovery process.

NOTE

If the computer is configured to boot from an LS-120 diskette (in the Boot menu), the BIOS recovery diskette must be a standard, bootable, DOS-formatted, 1.44-MB diskette not a 120-MB diskette.

For information about…	Refer to…
The BIOS recovery mode	Section 2.9, page 52
The Boot menu in the BIOS Setup program	Section 4.7, page 81
Contacting Intel customer support	Section 1.2, page 14

3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from an ATAPI removable media device, hard drive, CD-ROM, or the network. The default setting is for the ATAPI CD-ROM to be the primary boot device and the hard drive to be the secondary boot device. By default, the third and fourth devices are disabled.

⟹ NOTE

The BIOS cannot boot from USB devices.

3.8.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance with the El Torito *Bootable CD-ROM Format Specification*. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device.

The network can be selected as a boot device. This allows booting from either of the following:

- The Intel 82559 LAN controller
- A mini-PCI add-in LAN card with remote boot option ROM

For information about…	Refer to…
The El Torito specification	Table 3, page 14

3.8.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the keyboard and mouse are not present.

3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 43 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 43. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options(Note)	Can change all options(Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

For information about…	Refer to…
Setting user and supervisor passwords	Section 4.5, page 80

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

```
Maintenance  Main      Advanced  Security  Power     Boot      Exit
```

Table 44 lists the BIOS Setup program menu functions.

Table 44. BIOS Setup Program Menu Functions

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

NOTE

The Setup screens described in this chapter apply to boards with BIOS identifiers GS81011A.86A. Boards with other BIOS identifiers might have differences in some of the Setup screens.

NOTE

In this chapter, all examples of the BIOS Setup Program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the board is in configuration mode. Section 2.9 on page 52 tells how to put the board in configuration mode.

Table 45 lists the function keys available for menu screens.

Table 45. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen
<↑> or <↓>	Selects an item
<Tab>	Selects a field
<Enter>	Executes command or selects a submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 Maintenance Menu

Maintenance	Main	Advanced	Security	Power	Boot	Exit

The menu shown in Table 46 is for clearing Setup passwords. Setup only displays this menu in configuration mode. See Section 2.9 on page 52 for configuration mode setting information.

Table 46. Maintenance Menu

Feature	Options	Description
Clear All Passwords	No options	Clears the user and supervisor passwords.

4.3 Main Menu

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 47 describes the Main Menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 47. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
Cache RAM	No options	Displays the size of second-level cache.
Total Memory	No options	Displays the total amount of RAM on the board.
Memory Bank 0 Memory Bank 1	No options	Displays type of DIMM installed in each memory bank.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Month, day, and year	Specifies the current date.

4.4 Advanced Menu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Event Log Configuration

Table 48 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

Table 48. Advanced Menu

Feature	Options	Description
Boot Configuration	No options	Configures Plug and Play and the Numlock key, and resets configuration data. When selected, displays the Boot Settings Configuration submenu.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	No options	Specifies type of connected IDE device.
Event Log Configuration	No options	Configures Event Logging. When selected, displays the Event Log Configuration submenu.

4.4.1 Boot Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Event Log Configuration

The submenu represented by Table 49 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

Table 49. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	• No • **Yes (default)**	Specifies if a Plug and Play operating system is being used. *No* lets the BIOS configure all devices. *Yes* lets the operating system configure Plug and Play devices. Not required with a Plug and Play operating system.
Reset Config Data	• **No (default)** • Yes	Clears the BIOS configuration data on the next boot.
Numlock	• Off • **On (default)**	Specifies the power on state of the Numlock feature on the numeric keypad of the keyboard.

4.4.2 Peripheral Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Event Log Configuration

The submenu represented in Table 50 is used for enabling the onboard audio and LAN devices and legacy USB support.

Table 50. Peripheral Configuration Submenu

Feature	Options	Description
Audio Device	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
LAN Device	• Disabled • **Enabled (default)**	Enables or disables the onboard LAN controller. (Displayed only if LAN is installed.)
Legacy USB Support	• Disabled • Enabled • **Auto (default)**	Enables or disables USB legacy support. (See Section 3.5 on page 67 for more information.)
Debug Port	• **Disabled (default)** • Enabled	Enables or disables the optional serial debug port.

4.4.3 IDE Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Event Log Configuration

The menu represented in Table 51 is used to configure IDE device options.

Table 51. IDE Device Configuration

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the primary IDE controller. *Secondary* enables only the secondary IDE controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay. Selecting a predelay instructs the BIOS to wait a specified time before attempting to detect the hard-disk drive. This allows the BIOS to detect slow spin-up hard disk drives.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.4.4 IDE Configuration Sub-Submenus

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration **Primary IDE Master** **Primary IDE Slave** **Secondary IDE Master** **Secondary IDE Slave**
Event Log Configuration

The sub-submenus represented in Table 52 are used to configure IDE devices.

Table 52. IDE Configuration Sub-Submenus

Feature	Options	Description
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User* allows the cylinders, heads, and sectors fields to be changed. *Auto* automatically fills in the values for the cylinders, heads, and sectors fields.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables the LBA mode control. (Shows when anything other than *Auto* is selected in the *Type* menu above.)
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting. Shows when anything other than *Auto* is selected in the *Type* menu above.
PIO Mode	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Configures the PIO mode. Shows when anything other than *Auto* is selected in the *Type* menu above.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4	Specifies the Ultra DMA mode for the drive. Shows when anything other than *Auto* is selected in the *Type* menu above.

4.4.5 Event Log Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Event Log Configuration

The submenu represented by Table 53 is used to configure the event logging features.

Table 53. Event Log Configuration Submenu

Feature	Options	Description
Event log	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
View event log	[Enter]	Displays the event log.
Clear all event logs	• **No (default)** • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of events.
Mark events as read	[Enter]	Marks all events as read.

4.5 Security Menu

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented by Table 54 is for setting passwords and security features.

Table 54. Security Menu

Feature	Options	Description
Supervisor Password Is	No options	Reports if there is a supervisor password set.
User Password Is	No options	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password		Specifies the user password.
Clear User Password (Note 1)	[Enter]	Clears the user password.
User Access Level (Note 2)	• Limited • No Access • View Only • **Full (default)**	Sets BIOS Setup Utility access rights for user level.
Unattended Start (Note 1)	• **Disabled (default)** • Enabled	The keyboard remains locked until a password is entered.

Notes:

1. This feature appears only if a user password has been set.
2. This feature appears only if both a user password and a supervisor password have been set.

4.6 Power Menu

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit

The menu represented in Table 55 is for setting the power management features.

Table 55. Power Menu

Feature	Options	Description
ACPI Suspend State	• **S1 State (default)** • S3 State	Specifies the ACPI suspend state.

4.7 Boot Menu

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit

The menu represented in Table 56 is used for setting the boot features and the boot sequence.

Table 56. Boot Menu

Feature	Options	Description
Quiet Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays OEM logo instead of POST messages.
Quick Boot	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Stays Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC/Power loss occurs. *Stays Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred. *Power On* restores power to the computer.
First Boot Device Second Boot Device Third Boot Device Fourth Boot Device	• Disabled • 1st IDE-HDD (Note 1) • 2nd IDE-HDD • 3rd IDE-HDD • 4th IDE-HDD • ARMD-FDD (Note 2) • ARMD-HDD (Note 3) • **ATAPI CDROM (default)** • Network	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering. Not all of the devices in this list are available as second, third, and fourth boot devices. The default settings for the first through fourth boot devices are, respectively: • ATAPI CDROM • 1st IDE-HDD • Disabled • Disabled

Notes:

1. HDD = Hard Disk Drive
2. ARMD-FDD = ATAPI removable device - floppy disk drive
3. ARMD-HDD = ATAPI removable device - hard disk drive

4.8 Exit Menu

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 57 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 57. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages

Table 58 lists the error messages and provides a brief description of each.

Table 58. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate-A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive is not an ATAPI device. Run Setup to make sure device is selected correctly.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
HDC Failure	Error occurred trying to access hard disk controller.

continued

Table 58. BIOS Error Messages (continued)

Error Message	Explanation
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Is Locked	The system keyboard lock is engaged. The system must be unlocked to continue to boot.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM / CMOS / PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 59 defines the Uncompressed INIT Code Checkpoints, Table 60 describes the Boot Block Recovery Code Checkpoints, and Table 61 lists the Runtime Code Uncompressed in F000 Shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 59. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If the BIOS is in recovery mode or the main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 60. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard floppy controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller, interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize ATAPI CD-ROM drive.
EA	Try to boot from ATAPI CD-ROM. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS120, ZIP†) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from ATAPI CD-ROM failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 61. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23, 24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 5.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate display memory R/W test.
32	Alternate display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 61. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640 K memory.
48	Patterns written in base memory. Going to find out amount of memory below 1 M memory.
49	Amount of memory below 1 M found and verified. Going to find out amount of memory above 1 M memory.
4B	Amount of memory above 1 M found and verified. Check for soft reset and going to clear memory below 1 M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1 M cleared. (SOFT RESET) Going to clear memory above 1 M.
4D	Memory above 1 M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64 K memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1 M complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1 M to follow.
52	Memory testing/initialization above 1 M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 61. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done.
91	Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area.
9A	Return after setting timer. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test.
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID, and Num Lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in shadow.

continued

Table 61. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 62 describes the bus initialization checkpoints.

Table 62. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 63 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 63. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned
1	func#1, static devices init on the bus concerned
2	func#2, output device init on the bus concerned
3	func#3, input device init on the bus concerned
4	func#4, IPL device init on the bus concerned
5	func#5, general device init on the bus concerned
6	func#6, error reporting for the bus concerned
7	func#7, add-on ROM init for all buses

Table 64 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 64. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	Onboard system devices
2	ISA devices (not supported)
3	EISA devices (not supported)
4	ISA PnP devices (not supported)
5	PCI devices

5.4 Speaker

A 47 Ω inductive speaker is mounted on the GS810 board. The speaker provides audible error code (beep code) information during the Power-On Self-Test (POST).

For information about…	Refer to…
The location of the onboard speaker	Figure 1, page 12

5.5 BIOS Beep Codes

Whenever a recoverable error occurs during power-on self-test (POST), the BIOS displays an error message describing the problem (see Table 65). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 65. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)