Dual-Core Intel® Xeon® Processor 2.80 GHz

Datasheet

October 2005

Document Number: 309158-001

Contents

Figures

Tables

Revision History

Order Number	Revision Number	Description	Date
309158	-001	• Initial release of the document.	October 2005

§

Features

- Dual-Core processing
- Available at 2.80 GHz processor speed
- 90 nm process technology
- Dual processing (DP) server support
- Binary compatible with applications running on previous members of Intel's IA-32 microprocessor line
- Intel® NetBurst® micro-architecture
- Hyper-Threading Technology allowing up to 8 threads per platform
- Hardware support for multithreaded applications
- 800 MHz system bus
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper Pipelined Technology
- Advanced Dynamic Execution
- Very deep out-of-order execution
- Enhanced branch prediction
- Includes 16-KB Level 1 data cache per core (2x16-KB)
- Intel® Extended Memory 64 Technology (Intel® EM64T)
- 2-MB Advanced Transfer Cache per core (2x2-MB, On-die, full speed Level 2 (L2) Cache) with 8-way associativity and Error Correcting Code (ECC)
- Enables system support of up to 64 GB of physical memory
- 144 Streaming SIMD Extensions 2 (SSE2) instructions
- 13 Streaming SIMD Extensions 3 (SSE3) instructions
- Enhanced floating-point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- System Management mode
- Thermal Monitor
- Machine Check Architecture (MCA)
- Demand-Based Switching (DBS) with Enhanced Intel SpeedStep® Technology

The Dual-Core Intel® Xeon® processor is designed for high-performance dual-processor server applications. Based on the Intel NetBurst® microarchitecture and Hyper-Threading Technology (HT Technology), it is binary compatible with previous Intel® Architecture (IA-32) processors. The Dual-Core Intel Xeon processor is scalable to two processors in a multiprocessor system, providing exceptional performance for applications running on advanced operating systems such as Windows* XP, Windows Server 2003, Linux*, and UNIX*.

The Dual-Core Intel Xeon processor delivers compute power at unparalleled value and flexibility for powerful servers, internet infrastructure, and departmental server applications. The Intel NetBurst micro-architecture and Hyper-Threading Technology deliver outstanding performance and headroom for peak internet server workloads, resulting in faster response times, support for more users, and improved scalability.

§

1 Introduction

The Dual-Core Intel® Xeon® processor is Intel's first dual core product for dual-processor server platforms and utilizes two physical Intel NetBurst® microarchitecture cores in one package. As well, it maintains compatibility with IA-32 software while also supporting 64-bit computing with Intel® Extended Memory 64 Technology (Intel® EM64T). The processor also features Hyper Pipelined Technology, a Rapid Execution Engine, and an Execution Trace Cache. The 800 MHz system bus is a quad-pumped bus running off a 200 MHz system clock making 6.4 GB per second data transfer rates possible. The Execution Trace Cache is a level 1 cache that stores decoded micro-operations, which removes the decoder from the main execution path, thereby increasing performance.

In addition, enhanced thermal and power management capabilities are implemented including Thermal Monitor and Enhanced Intel SpeedStep® Technology. These capabilities are targeted for dual processor (DP) servers in data center and office environments. Thermal monitor provides efficient and effective cooling in high temperature situations. Enhanced Intel SpeedStep® allows trade-offs to be made between performance and power consumption. This may lower average power consumption (in conjunction with OS support).

The Dual-Core Intel® Xeon® processor supports Hyper-Threading Technology. This feature allows a single, physical processor to function as four logical processors (2 logical processors per core). While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architecture state with its own set of general-purpose registers, control registers to provide increased system responsiveness in multitasking environments, and headroom for next generation multithreaded applications. More information on Hyper-Threading Technology can be found at http://www.intel.com/technology/hyperthread.

The Dual-Core Intel Xeon processor also includes the Execute Disable Bit capability previously available in Intel® Itanium® processors. This feature, when combined with a supported operating system, allows memory to be marked as executable or non-executable. If code attempts to run in non-executable memory, the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *IA-32 Intel® Architecture Software Developer's Manual* for more detailed information.

Other features within the Intel NetBurst microarchitecture include Advanced Dynamic Execution, Advanced Transfer Cache, enhanced floating point and multi-media unit, Streaming SIMD Extensions 2 (SSE2) and Streaming SIMD Extensions 3 (SSE3). Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The Advanced Transfer Cache in each core is a 2 MB level 2 (L2) cache. The floating point and multi-media units include 128-bit wide registers and a separate register for data movement. Streaming SIMD2 (SSE2) instructions provide highly efficient double-precision floating point, SIMD integer, and memory management operations. In addition, SSE3 instructions have been added to further extend the capabilities of Intel processor technology. Other processor enhancements include core frequency improvements and microarchitectural improvements.

The Dual-Core Intel Xeon processor supports Intel Extended Memory 64 Technology (Intel EM64T) as an enhancement to Intel's IA-32 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology. Further details on Intel Extended Memory 64 Technology and its programming model can be found in the *IA-32 Intel® Architecture Software Developer's Manual*.

The Dual-Core Intel Xeon processor is intended for high performance server systems with up to two processors on one system bus. The processor will be packaged in a 604-pin Flip Chip Micro Pin Grid Array (FC-mPGA4) package and will utilize a surface mount Zero Insertion Force (ZIF) socket (mPGA604).

Table 1-1. Features of the Dual-Core Intel® Xeon® Processor

	# of Supported Symmetric Agents	L2 Advanced Transfer Cache	Front Side Bus Frequency	Package
Dual-Core Intel® Xeon® processor	1 - 4	2 MB per Core	800 MHz	604-pin FC-mPGA4

The Dual-Core Intel Xeon processor-based platforms implement independent power planes for each system bus agent. As a result, the processor core voltage (V_{CC}) and system bus termination voltage (V_{TT}) must connect to separate supplies. The processor core voltage utilizes power delivery guidelines denoted by VRM 10.1 and the associated load line (see *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.1 Design Guidelines* for further details). Implementation details can be obtained by referring to the applicable platform design guidelines.

The Dual-Core Intel Xeon processor uses a scalable system bus protocol referred to as the “system bus” in this document. The system bus utilizes a split-transaction, deferred reply protocol. The system bus uses Source-Synchronous Transfer (SST) of address and data to improve performance. The processor transfers data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a ‘double-clocked’ or the 2X address bus. In addition, the Request Phase completes in one clock cycle. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 6.4 GBytes/second (6400 MBytes/second). Finally, the system bus is also used to deliver interrupts.

1.1 Terminology

A ‘#’ symbol after a signal name refers to an active low signal, indicating a signal is in the asserted state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the ‘#’ symbol implies that the signal is inverted. For example, D[3:0] = ‘HLHL’ refers to a hex ‘A’, and D[3:0]# = ‘LHLH’ also refers to a hex ‘A’ (H= High logic level, L= Low logic level).

“Front side bus” or “System bus” refers to the interface between the processor, system core logic (a.k.a. the chipset components), and other bus agents. The system bus is a multiprocessing interface to processors, memory, and I/O. For this document, “front side bus” or “system bus” are used as generic terms for the “Dual-Core Intel Xeon processor system bus”.

Commonly used terms are explained here for clarification:

- **Dual-Core Intel Xeon processor** — Intel’s first dual-core 64/32-bit microprocessor intended for dual processor servers. The Dual-Core Intel Xeon processor is based on Intel’s 90 nanometer process and has a 2 MB per core level 2 (L2) cache. The Dual-Core Intel Xeon processor will utilize the mPGA604 socket. For this document, “processor” is used as the generic term for the “Dual-Core Intel® Xeon® Processor”.
- **Central Agent** — The central agent is the host bridge to the processor and is typically known as the chipset.

- **EVRD (Enterprise Voltage Regulator Down)** — DC-DC converter integrated onto the system board that provide the correct voltage and current for the processor based on the logic state of the VID bits.
- **FC-mPGA4 (Flip Chip Micro Pin Grid Array) Package** — The processor package is a Flip Chip Micro Pin Grid Array (FC-mPGA4), consisting of a processor cores mounted on a pinned substrate with an integrated heat spreader (IHS). This package technology employs a 1.27 mm [0.05 in.] pitch for the processor pins.
- **Front Side Bus (FSB)** — The electrical interface that connects the processor to the chipset. Also referred to as the processor system bus or the system bus. All memory and I/O transactions, as well as interrupt messages, pass between the processor and the chipset over the FSB.
- **Functional Operation** — Refers to the normal operating conditions in which all processor specifications, including DC, system bus, signal quality, mechanical and thermal are satisfied.
- **Integrated Heat Spreader (IHS)** — A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **mPGA604 socket** — The Dual-Core Intel Xeon processor mates with the baseboard through this surface mount, 604-pin, zero insertion force (ZIF) socket. See the *mPGA604 Socket Design Guidelines* for details regarding this socket.
- **Processor cores** — The processor's execution engines. All signal integrity specifications are to the pads of the processor cores.
- **Storage Conditions** — Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor pins should not be connected to any supply voltages, have any I/Os biased or receive any clocks.
- **Symmetric agent** — A symmetric agent is a processor which shares the same I/O subsystem and memory array, and runs the same operating system as another processor in a system. Systems using symmetric agents are known as Symmetric Multiprocessor (SMP) systems. The Dual-Core Intel Xeon processor should only be used in SMP systems which have two or fewer agents.
- **Thermal Design Power** — Processor/chipset thermal solution should be designed to this target. It is the highest expected sustainable power while running known power-intensive real applications. TDP is not the maximum power that the processor/chipset can dissipate.
- **VRM (Voltage Regulator Module)** — DC-DC converter built onto a module that interfaces with an appropriate card edge socket that supplies the correct voltage and current to the processor.
- $\mathbf{V_{CC}}$ — The processor core power supply.
- $\mathbf{V_{SS}}$ — The processor ground.
- $\mathbf{V_{TT}}$ — The system bus termination voltage.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

Document	Intel Order Number
mPGA604 Socket Design Guidelines	254239
AP-485, Intel® Processor Identification and CPUID Instruction	241618
ATX12V Power Supply Design Guide	http://formfactors.org
Entry-Level Electronics-Bay Specifications: A Server System Infrastructure (SSI) Specification for Entry Pedestal Servers and Workstations	http://www.ssiforum.org
EPS12V Power Supply Design Guide: A Server System Infrastructure (SSI) Specification for Entry Chassis Power Supplies	http://www.ssiforum.org
IA-32 Intel® Architecture Optimization Reference Manual	248966
IA-32 Intel® Architecture Software Developer's Manual *Volume 1: Basic Architecture* *Volume 2A: Instruction Set Reference, A-M* *Volume 2B: Instruction Set Reference, N-Z* *Volume 3: System Programming Guide*	 253665 253666 253667 253668
Dual-Core Intel® Xeon® Processor Boundary Scan Descriptor Language (BSDL) Model (V1.0) and Cell Descriptor File (V1.0)	
ITP700 Debug Port Design Guide	249679
Dual-Core Intel® Xeon® Processor 2.80 GHz Specification Update	
Thin Electronics Bay Specification (A Server System Infrastructure (SSI) Specification for Rack Optimized Servers)	http://www.ssiforum.org
Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.1 Design Guidelines	302732

NOTE: Contact your Intel representative for the latest revision of the documents without document numbers.

1.3 State of Data

The data contained within this document is subject to change. It is the most accurate information available by the publication date of this document

§

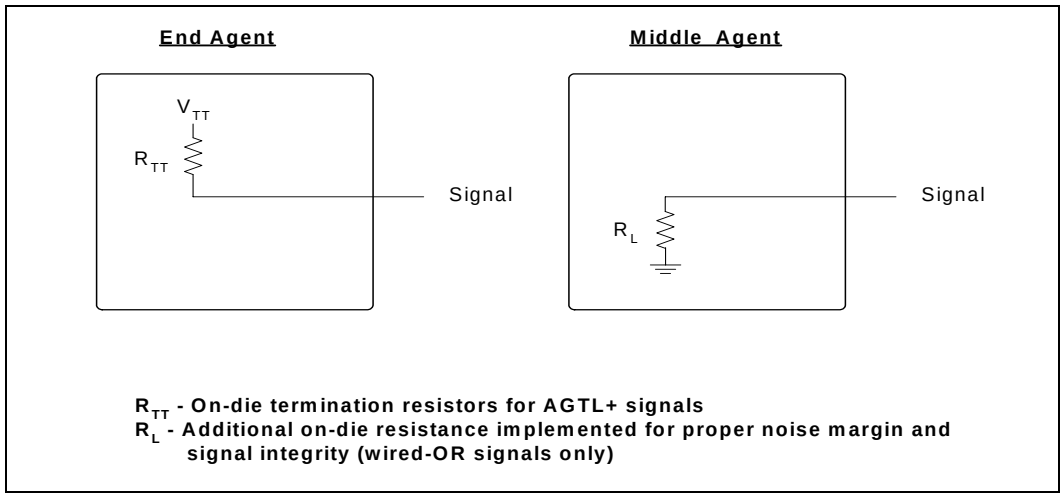
2 Electrical Specifications

2.1 Front Side Bus and GTLREF

Most Dual-Core Intel Xeon processor front side bus (FSB) signals use Assisted Gunning Transceiver Logic (AGTL+) signaling technology. This technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. AGTL+ buffers are open-drain and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to "assist" the pull-up resistors during the first clock of a low-to-high voltage transition. Platforms implement a termination voltage level for AGTL+ signals defined as V_{TT}. Because platforms implement separate power planes for each processor (and chipset), separate V_{CC} and V_{TT} supplies are necessary. This configuration allows for improved noise tolerance as processor frequency increases. Speed enhancements to data and address busses have caused signal integrity considerations and platform design methods to become even more critical than with previous processor families. Design guidelines for the processor front side bus are detailed in the appropriate platform design guide (refer to Section 1.2).

The AGTL+ inputs require a reference voltage (GTLREF) which is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the baseboard. Please refer to the applicable platform design guidelines for details. Termination resistors (R_{TT}) for AGTL+ signals are provided on the processor silicon and are terminated to V_{TT}. The on-die termination resistors are a selectable feature and can be enabled or disabled via the ODTEN signal. For end bus agents, on-die termination resistors are enabled to control reflections on the transmission line. For the middle bus agent, on-die termination R_{TT} resistors must be disabled. Intel chipsets will also provide on-die termination, thus eliminating the need to terminate the bus on the baseboard for most AGTL+ signals. Processor wired-OR signals may also include additional on-die resistors (R_L) to further insure proper noise margin and signal integrity. R_L is not configurable and is always enabled for these signals. Figure 2-1 illustrate the active on-die termination.

Figure 2-1. On-Die Front Side Bus Termination



Note: Some AGTL+ signals do not include on-die termination (R_{TT}) and must be terminated on the baseboard. See Table 2-4 for details regarding these signals.

The AGTL+ bus depends on incident wave switching. Therefore, timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the front side bus, including trace lengths, is highly recommended when designing a system.

2.2 Power and Ground Pins

For clean on-chip power distribution, the processor has 181 V_{CC} (power) and 185 V_{SS} (ground) inputs. All V_{CC} pins must be connected to the processor power plane, while all V_{SS} pins must be connected to the system ground plane. The processor V_{CC} pins must be supplied with the voltage determined by the processor **V**oltage **ID**entification (VID) pins.

Eleven signals are denoted as V_{TT}, which provide termination for the front side bus and power to the I/O buffers. The platform must implement a separate supply for these pins, which meets the V_{TT} specifications outlined in Table 2-7.

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the Dual-Core Intel Xeon processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic or aluminum-polymer capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the baseboard design to ensure that the voltage provided to the processor remains within the specifications listed in Table 2-7. Failure to do so can result in timing violations or reduced lifetime of the component. For further information and guidelines, refer to the appropriate platform design guidelines.

2.3.1 V_{CC} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and the baseboard designer must assure a low interconnect resistance from the voltage regulator (VRD or VRM pins) to the mPGA604 socket. The power delivery solution must insure the voltage and current specifications are met (defined in Table 2-7). For further information regarding power delivery, decoupling, and layout guidelines, refer to the appropriate platform design guidelines.

2.3.2 V_{TT} Decoupling

Decoupling must be provided on the baseboard. Decoupling solutions must be sized to meet the expected load. To insure optimal performance, various factors associated with the power delivery solution must be considered including regulator type, power plane and trace sizing, and component placement. A conservative decoupling solution would consist of a combination of low ESR bulk capacitors and high frequency ceramic capacitors. For further information regarding power delivery, decoupling and layout guidelines, refer to the appropriate platform design guidelines.

2.3.3 Front Side Bus AGTL+ Decoupling

The Dual-Core Intel Xeon processor integrates signal termination on the die, as well as part of the required high frequency decoupling capacitance on the processor package. However, additional high frequency capacitance must be added to the baseboard to properly decouple the return currents from the front side bus. Bulk decoupling must also be provided by the baseboard for proper AGTL+ bus operation. Decoupling guidelines are described in the appropriate platform design guidelines.

2.4 Front Side Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the front side bus interface speed as well as the core frequency of the processor. As in previous processor generations, the Dual-Core Intel Xeon processor core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier will be set during manufacturing. The default setting will be the maximum speed for the processor. It will be possible to override this setting using software (see the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3*). This will permit operation at a speed lower than the processor's tested frequency.

The BCLK[1:0] inputs directly control the operating speed of the front side bus interface. The processor core frequency is configured during reset by using values stored internally during manufacturing. The stored value sets the highest bus fraction at which the particular processor can operate. If lower speeds are desired, the appropriate ratio can be configured by setting bits [15:8] of the IA32_FLEX_BRVID_SEL MSR. For details of operation at core frequencies lower than the maximum rated processor speed, refer to the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3.*

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK[1:0] input, with exceptions for spread spectrum clocking. The Dual-Core Intel Xeon processor utilizes differential clocks. Table 2-1 contains core frequency to front side bus multipliers and their corresponding core frequencies.

2.4.1 Front Side Bus Frequency Select Signals (BSEL[1:0])

BSEL[1:0] are open-drain outputs, which must be pulled up to V_{TT}, and are used to select the front side bus frequency. Please refer to Table 2-10 for DC specifications. Table 2-1 defines the possible combinations of the signals and the frequency associated with each combination. The frequency is determined by the processor(s), chipset, and clock synthesizer. All front side bus agents must operate at the same core and front side bus frequencies. Individual processors will only operate at their specified front side bus clock frequency. See the appropriate platform design guide for further details.

Table 2-1. BSEL[1:0] Frequency Table

BSEL1	BSEL0	Bus Clock Frequency
0	0	Reserved
0	1	Reserved
1	0	200 MHz
1	1	Reserved

2.4.2 Phase Lock Loop (PLL) and Filter

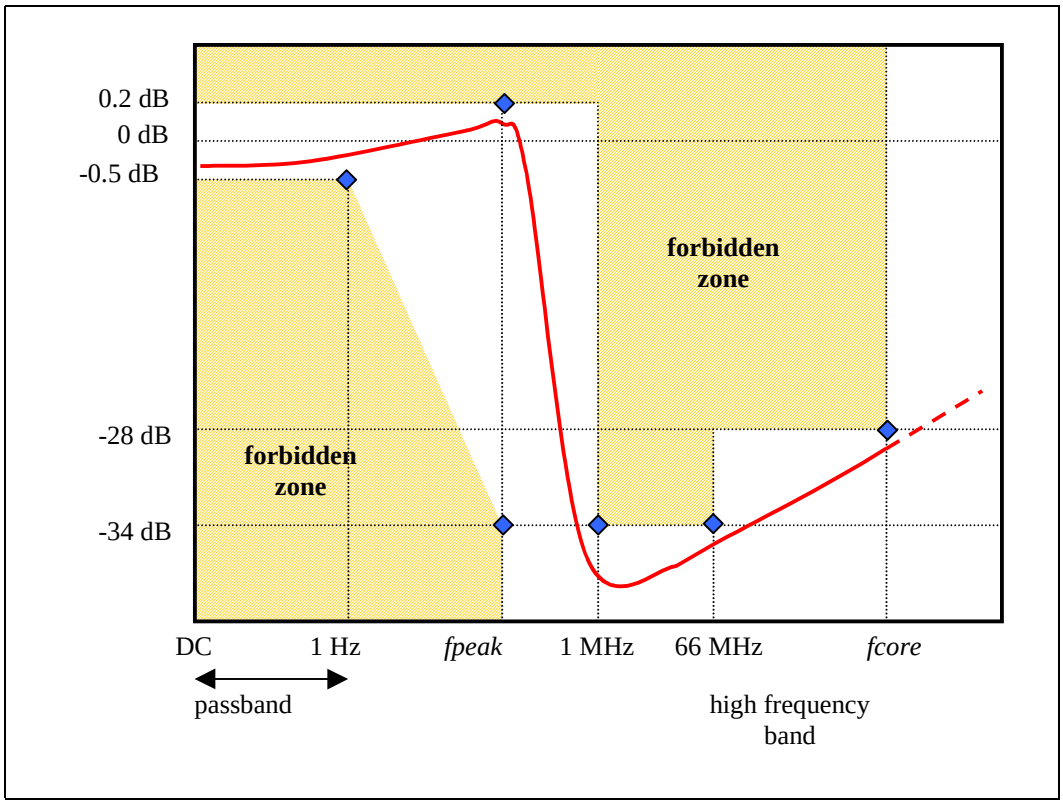
V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the Dual-Core Intel Xeon processor. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{TT}.

The AC low-pass requirements are as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in Figure 2-2. For recommendations on implementing the filter refer to the appropriate platform design guidelines.

Figure 2-2. Phase Lock Loop (PLL) Filter Requirements



NOTES:

1. Diagram not to scale.
2. No specifications for frequencies beyond f_{core} (core frequency).
3. f_{peak}, if existent, should be less than 0.05 MHz.
4. f_{core} represents the maximum core frequency supported by the platform.

2.5 Voltage Identification (VID)

The Voltage Identification (VID) specification for the Dual-Core Intel Xeon processor is defined by the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.1 Design Guidelines*. The voltage set by the VID signals is the maximum voltage allowed by the processor (please see Section 2.12.1 for V_{CC} overshoot specifications). VID signals are open drain outputs, which must be pulled up to V_{TT}. Please refer to Table 2-10 for the DC specifications for these signals. A minimum voltage is provided in Table 2-7 and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same core speed may have different default VID settings. This is reflected by the VID range values provided in Table 2-7. Refer to the *Dual-Core Intel® Xeon® Processor 2.80 GHz Specification Update* for further details on specific valid core frequency and VID values of the processor.

The Dual-Core Intel Xeon processor uses six voltage identification signals, VID[5:0], to support automatic selection of power supply voltages. Table 2-2 specifies the voltage level corresponding to the state of VID[5:0]. A ‘1’ in this table refers to a high voltage level and a ‘0’ refers to a low voltage level. If the processor socket is empty (VID[5:0] = x11111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself. See the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.1 Design Guidelines* for further details.

The Dual-Core Intel Xeon processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (V_{CC}). This will represent a DC shift in the load line. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the specified VID are not permitted. Table 2-7 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 2-8 and Figure 2-4.

The VRM or VRD utilized must be capable of regulating its output to the value defined by the new VID. DC specifications for dynamic VID transitions are included in Table 2-7 and Table 2-8. Please refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.1 Design Guidelines* for further details.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

Table 2-2. Voltage Identification Definition[2,3]

VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}		VID5	VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
0	0	1	0	1	0	0.8375		0	1	1	0	1	0	1.2125
1	0	1	0	0	1	0.8500		1	1	1	0	0	1	1.2250
0	0	1	0	0	1	0.8625		0	1	1	0	0	1	1.2375
1	0	1	0	0	0	0.8750		1	1	1	0	0	0	1.2500
0	0	1	0	0	0	0.8875		0	1	1	0	0	0	1.2625
1	0	0	1	1	1	0.9000		1	1	0	1	1	1	1.2750
0	0	0	1	1	1	0.9125		0	1	0	1	1	1	1.2875
1	0	0	1	1	0	0.9250		1	1	0	1	1	0	1.3000
0	0	0	1	1	0	0.9375		0	1	0	1	1	0	1.3125
1	0	0	1	0	1	0.9500		1	1	0	1	0	1	1.3250
0	0	0	1	0	1	0.9625		0	1	0	1	0	1	1.3375
1	0	0	1	0	0	0.9750		1	1	0	1	0	0	1.3500
0	0	0	1	0	0	0.9875		0	1	0	1	0	0	1.3625
1	0	0	0	1	1	1.0000		1	1	0	0	1	1	1.3750
0	0	0	0	1	1	1.0125		0	1	0	0	1	1	1.3875
1	0	0	0	1	0	1.0250		1	1	0	0	1	0	1.4000
0	0	0	0	1	0	1.0375		0	1	0	0	1	0	1.4125
1	0	0	0	0	1	1.0500		1	1	0	0	0	1	1.4250
0	0	0	0	0	1	1.0625		0	1	0	0	0	1	1.4375
1	0	0	0	0	0	1.0750		1	1	0	0	0	0	1.4500
0	0	0	0	0	0	1.0875		0	1	0	0	0	0	1.4625
1	1	1	1	1	1	OFF[1]		1	0	1	1	1	1	1.4750
0	1	1	1	1	1	OFF[1]		0	0	1	1	1	1	1.4875
1	1	1	1	1	0	1.1000		1	0	1	1	1	0	1.5000
0	1	1	1	1	0	1.1125		0	0	1	1	1	0	1.5125
1	1	1	1	0	1	1.1250		1	0	1	1	0	1	1.5250
0	1	1	1	0	1	1.1375		0	0	1	1	0	1	1.5375
1	1	1	1	0	0	1.1500		1	0	1	1	0	0	1.5500
0	1	1	1	0	0	1.1625		0	0	1	1	0	0	1.5625
1	1	1	0	1	1	1.1750		1	0	1	0	1	1	1.5750
0	1	1	0	1	1	1.1875		0	0	1	0	1	1	1.5875
1	1	1	0	1	0	1.2000		1	0	1	0	1	0	1.6000

NOTES:

1. When this VID pattern is observed, the voltage regulator output should be disabled.
2. Shading denotes the expected default VID range during normal operation for the Dual-Core Intel Xeon processor [1.2875 V - 1.4125 V]. Please note this is subject to change.
3. Shaded areas do not represent the entire range of VIDs that may be driven by the processor. Events causing dynamic VID transitions (See Section 2.5) may result in a more broad range of VID values.

2.6 Reserved Or Unused Pins

All Reserved pins must remain unconnected. Connection of these pins to V_{CC}, V_{TT}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 5 for a pin listing of the processor and the location of all Reserved pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. In a system level design, on-die termination has been included by the processor to allow end agents to be terminated within the processor silicon for most signals. In this context, end agent refers to the bus agent that resides on either end of the daisy-chained front side bus interface while a middle agent is any bus agent in between the two end agents. For end agents, most unused AGTL+ inputs should be left as no connects as AGTL+ termination is provided on the processor silicon. However, see Table 2-4 for details on AGTL+ signals that do not include on-die termination. For middle agents, the on-die termination must be disabled, so the platform must ensure that unused AGTL+ input signals which do not connect to end agents are connected to V_{TT} via a pull-up resistor. Unused active high inputs, should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected, however this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ±20% of the impedance of the baseboard trace for front side bus signals. For unused AGTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors (R_{TT}).

TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Inputs and utilized outputs must be terminated on the baseboard. Unused outputs may be terminated on the baseboard or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in the *ITP700 Debug Port Design Guide* (See Section 1.2)

All TESTHI[6:0] pins should be individually connected to V_{TT} via a pull-up resistor which matches the nominal trace impedance. TESTHI[3:0] and TESTHI[6:5] may be tied together and pulled up to V_{TT} with a single resistor if desired. However, utilization of boundary scan test will not be functional if these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins. For optimum noise margin, all pull-up resistor values used for TESTHI[6:0] pins should have a resistance value within ± 20 % of the impedance of the board transmission line traces. For example, if the nominal trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω should be used.

N/C (no connect) pins of the processor are not utilized by the processor. There is no connection from the pin to the die. These pins may perform functions in future processors intended for platforms utilizing the Dual-Core Intel Xeon processor. Refer to the applicable platform design guidelines for guidance that pertains to any pin labeled N/C in this document.

2.7 Front Side Bus Signal Groups

The front side bus signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving. AGTL+ asynchronous outputs can become active anytime and include an active pMOS pull-up transistor to assist during the first clock of a low-to-high voltage transition.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals whose timings are specified with respect to rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 2-3 identifies which signals are common clock, source synchronous and asynchronous.

Table 2-3. Front Side Bus Signal Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, BR[3:1]#[2,3], DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, AP[1:0]#, BINIT#[4], BNR#[4], BPM[5:0]#, BR0#[2,3], DBSY#, DP[3:0]#, DRDY#, HIT#[4], HITM#[4], LOCK#, MCERR#[4]
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#,A[16:3]#[3]</td><td>ADSTB0#</td></tr><tr><td>A[35:17]#[3]</td><td>ADSTB1#</td></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobe I/O	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
AGTL Asynchronous Output	Asynchronous	FERR#/PBE#, IERR#, PROCHOT#
GTL+ Asynchronous Input	Asynchronous	A20M#, FORCEPR#, IGNNE#, INIT#[3], LINT0/INTR, LINT1/NMI, SMI#[3], SLP#, STPCLK#
GTL+ Asynchronous Output	Asynchronous	THERMTRIP#
Front Side Bus Clock	Clock	BCLK1, BCLK0
TAP Input	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output	Synchronous to TCK	TDO
Power/Other	Power/Other	BOOT_SELECT, BSEL[1:0], COMP[0], GTLREF[3:0], ODTEN, OPTIMIZED/COMPAT#, PWRGOOD, Reserved, SKTOCC#, SLEW_CTRL, SMB_PRT, TEST_BUS, TESTHI[6:0], THERMDA, THERMDC, V_{CC}, V_{CCA}, $V_{CCIOPLL}$, V_{CCPLL}, VCCSENSE, VID[5:0], V_{SS}, V_{SSA}, VSSSENSE, V_{TT}, VIDPWRGD, VTTEN

NOTES:

1. Refer to Section 4 for signal descriptions.
2. The Dual-Core Intel Xeon processor utilizes all four of the BR0#, BR1#, BR2# and BR3# signals. For additional details regarding the BR[3:0]# signals, see Section 4 and Section 7.1.
3. The value of these pins during the active-to-inactive edge of RESET# defines the processor configuration options. See Section 7.1 for details.
4. These signals may be driven simultaneously by multiple agents (wired-OR).

Table 2-4 outlines the signals which include on-die termination (R_{TT}) and lists signals which include additional on-die resistance (R_L). Table 2-5 provides signal reference voltages.

Table 2-4. Signal Description Table

Signals with R_{TT}
A[35:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BOOT_SELECT[2], BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, FORCEPR#, HIT#, HITM#, LOCK#, MCERR#, OPTIMIZED/COMPAT#[2], REQ[4:0]#, RS[2:0]#, RSP#, TEST_BUS, TRDY#
Signals with R_L
BINIT#, BNR#, HIT#, HITM#, MCERR#

NOTES:

1. Signals that do not have R_{TT}, nor are actively driven to their high voltage level.
2. The termination for these signals is not R_{TT}. The OPTIMIZED/COMPAT# and BOOT_SELECT pins have a 500 - 5000 Ω pull-up to V_{TT}.

Table 2-5. Signal Reference Voltages

GTLREF	0.5 * V_{TT}
A20M#, A[35:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BPM[5:0]#, BPRI#, BR[3:0]#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, FORCEPR#, HIT#, HITM#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, LOCK#, MCERR#, ODTEN, RESET#, REQ[4:0]#, RS[2:0]#, RSP#, SLP#, SMI#, STPCLK#, TRDY#	BOOT_SELECT, OPTIMIZED/COMPAT#, PWRGOOD[1], TCK[1], TDI[1], TMS[1], TRST#[1], VIDPWRGD

NOTES:

1. These signals also have hysteresis added to the reference voltage. See Table 2-12 for more information.

2.8 GTL+ Asynchronous and AGTL+ Asynchronous Signals

The Dual-Core Intel Xeon processor does not utilize CMOS voltage levels on any signals that connect to the processor silicon. As a result, input signals such as A20M#, FORCEPR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, and STPCLK# utilize GTL input buffers. Legacy output THERMTRIP# utilizes a GTL+ output buffers. All of these Asynchronous GTL+ signals follow the same DC requirements as GTL+ signals, however the outputs are not driven high (during the logical 0-to-1 transition) by the processor. FERR#/PBE#, IERR#, and IGNNE# have now been defined as AGTL+ asynchrnous signals as they include an active p-MOS device. GTL+ asynchronous and AGTL+ asynchronous signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the GTL+ asynchronous and AGTL+ asynchronous signals are required to be asserted/deasserted for at least six BCLKs in order for the processor to recognize them. See Table 2-13 for the DC specifications for the asynchronous GTL+ signal groups.

2.9 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the processor(s) be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one

of the other components is capable of accepting an input of the appropriate voltage. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.

2.10 Mixing Processors

Intel only supports and validates dual processor configurations in which both Dual-Core Intel Xeon processor operate with the same front side bus frequency, core frequency, and have the same internal cache sizes. Mixing components operating at different internal clock frequencies is not supported and will not be validated by Intel [Note: Processors within a system must operate at the same frequency per bits [15:8] of the IA32_FLEX_BRVID_SEL MSR; however this does not apply to frequency transitions initiated due to thermal events, Enhanced Intel SpeedStep technology transitions, or assertion of the FORCEPR# signal (See Section 6)]. Not all operating systems can support dual processors with mixed frequencies. Intel does not support or validate operation of processors with different cache sizes. Mixing processors of different steppings but the same model (as per CPUID instruction) is supported. Please see the *Dual-Core Intel® Xeon® Processor 2.80 GHz Specification Update* (see Section 1.2) for the applicable mixed stepping table. Details regarding the CPUID instruction are provided in the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programmer's Guide* and the *AP-485 Intel® Processor Identification and the CPUID Instruction* application note.

2.11 Absolute Maximum and Minimum Ratings

Table 2-6 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 2-6. Absolute Maximum and Minimum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1,2]
V_{CC}	Core voltage with respect to V_{SS}	-0.30	1.55	V	
V_{TT}	System bus termination voltage with respect to V_{SS}	-0.30	1.55	V	
T_{CASE}	Processor case temperature	See Section 6	See Section 6	°C	
$T_{STORAGE}$	Storage temperature	-40	85	°C	3,4

NOTES:

1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Section 3. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
4. This rating applies to the processor and does not include any tray or packaging.

2.12 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Section 5 for the Dual-Core Intel Xeon processor pin listings and Section 4 for signal definitions. Voltage and current specifications are detailed in Table 2-7. For platform power delivery planning refer to Table 2-8, which provides V_{CC} static and transient tolerances. This same information is presented graphically in Figure 2-4.

BSEL[1:0] and VID[5:0] signals are specified in Table 2-10. The DC specifications for the AGTL+ signals are listed in Table 2-11. The DC specifications for the PWRGOOD input and TAP signal group are listed in Table 2-12 and the Asynchronous GTL+ signal group is listed in Table 2-13. The VIDPWRGD signal is detailed in Table 2-14.

Table 2-7 through Table 2-14 list the DC specifications for the processor and are valid only while meeting specifications for case temperature (T_{CASE} as specified in Section 6), clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 2-7. Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Notes [1]
VID range	VID range	1.2875		1.4125	V	2,3
V_{CC}	V_{CC} for processors with multiple VIDs	See Table 2-8 and Figure 2-4		VID - I_{CC} (max) * 1.25 mΩ	V	3,4,5,6
VID Transition	VID step size during a transition			±12.5	mV	17
	Total allowable DC load line shift from VID steps			450	mV	18
V_{TT}	Front Side Bus termination voltage (DC specification)	1.176	1.20	1.224	V	7
I_{CC}	I_{CC} for processors with multiple VIDs			120	A	6
I_{CC_RESET}	I_{CC_RESET} for processor with multiple VIDs			120	A	16
I_{TT}	Front Side Bus end-agent V_{TT} current			4.8	A	9
I_{TT}	Front Side Bus mid-agent V_{TT} current			1.5	A	10
I_{CC_VCCA}	I_{CC} for PLL power pins			120	mA	11
$I_{CC\_VCCIOPLL}$	I_{CC} for PLL power pins			100	mA	11

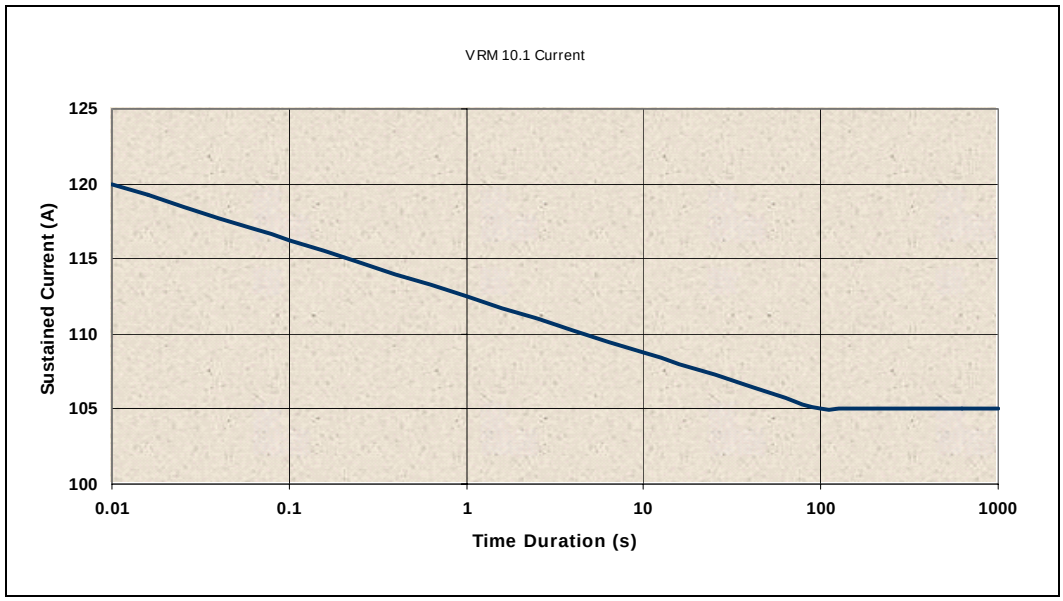
Table 2-7. Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Notes [1]
I_{CC_GTLREF}	I_{CC} for GTLREF pins			200	µA	12
I_{SGNT} I_{SLP}	I_{CC} Stop Grant			56	A	13
I_{TCC}	I_{CC} TCC Active			I_{CC}	A	14
I_{CC_TDC}	Thermal Design Current			105	A	15

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on silicon characteristics, however they may be updated as further data becomes available. List frequencies are not necessarily committed production frequencies.
2. Each processor is programmed with a maximum valid voltage identification (VID) values, which is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Please note this differs from the VID employed by the processor during a power management event (Enhanced HALT State).
3. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.5 for more information.
4. The voltage specification requirements are measured across vias on the platform for the VCCSENSE and VSSSENSE pins close to the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
5. Refer to Table 2-8 and corresponding Figure 2-4. The processor should not be subjected to any static V_{CC} level that exceeds the V_{CC_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
6. Minimum V_{CC} and maximum I_{CC} are specified at the maximum processor case temperature (T_{CASE}) shown in Table 6-1. I_{CC_MAX} is specified at the relative V_{CC_MAX} point on the V_{CC} load line. The processor is capable of drawing I_{CC_MAX} for up to 10 ms. Refer to Figure 2-3 for further details on the average processor current draw over various time durations.
7. V_{TT} must be provided via a separate voltage source and must not be connected to V_{CC}. This specification is measured at the pin.
8. Baseboard bandwidth is limited to 20 MHz.
9. This specification refers to a single processor with R_{TT} enabled. Please note the end agent and middle agent may not require I_{TT}(max) simultaneously. This parameter is based on design characterization and not tested.
10. This specification refers to a single processor with R_{TT} disabled. Please note the end agent and middle agent may not require I_{TT}(max) simultaneously.
11. These specifications apply to the PLL power pins VCCA, VCCIOPLL, and VSSA. See Section 2.4.2 for details. These parameters are based on design characterization and are not tested.
12. This specification represents a total current for all GTLREF pins.
13. The current specified is also for HALT State.
14. The maximum instantaneous current the processor will draw while the thermal control circuit is active as indicated by the assertion of the PROCHOT# signal is the maximum I_{CC} for the processor.
15. I_{CC_TDC} (Thermal Design Current) is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator temperature assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion. Please see the applicable design guidelines for further details. The processor is capable of drawing ICC_TDC indefinitely. Refer to Figure 2-3 for further details on the average processor craw over various time durations. This parameter is based on design characterization and is not tested.
16. I_{CC_RESET} is specified while PWRGOOD and RESET# are asserted.
17. This specification represents the V_{CC} reduction due to each VID transition. See Section 2.5.
18. This specification refers to the potential total reduction of the load line due to VID transitions below the specified VID.

Figure 2-3. Dual-Core Intel® Xeon® Processor Load Current Vs. Time



NOTES:

1. Processor or voltage regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

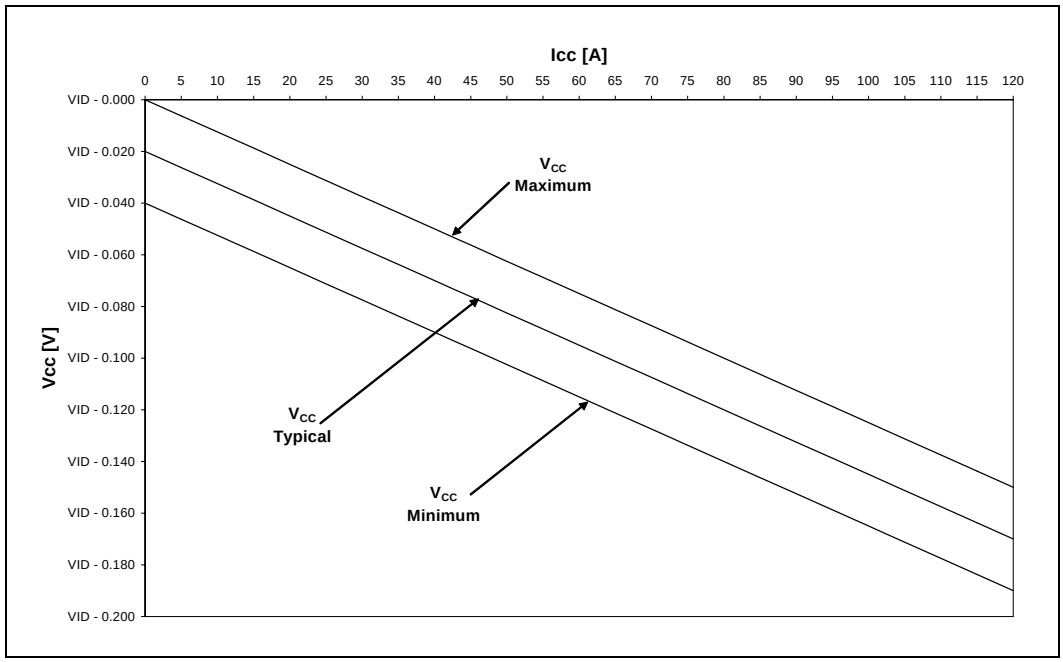
Table 2-8. V_{CC} Static and Transient Tolerance

I_{CC}	Voltage Deviation from VID Setting (V) [1,2,3]		
	V_{CC_Max}	V_{CC_Typ}	V_{CC_Min}
0	VID - 0.000	VID - 0.020	VID - 0.040
5	VID - 0.006	VID - 0.026	VID - 0.046
10	VID - 0.013	VID - 0.033	VID - 0.052
15	VID - 0.019	VID - 0.039	VID - 0.059
20	VID - 0.025	VID - 0.045	VID - 0.065
25	VID - 0.031	VID - 0.051	VID - 0.071
30	VID - 0.038	VID - 0.058	VID - 0.077
35	VID - 0.044	VID - 0.064	VID - 0.084
40	VID - 0.050	VID - 0.070	VID - 0.090
45	VID - 0.056	VID - 0.076	VID - 0.096
50	VID - 0.063	VID - 0.083	VID - 0.103
55	VID - 0.069	VID - 0.089	VID - 0.109
60	VID - 0.075	VID - 0.095	VID - 0.115
65	VID - 0.081	VID - 0.101	VID - 0.121
70	VID - 0.087	VID - 0.108	VID - 0.128
75	VID - 0.094	VID - 0.114	VID - 0.134
80	VID - 0.100	VID - 0.120	VID - 0.140
85	VID - 0.106	VID - 0.126	VID - 0.146
90	VID - 0.113	VID - 0.133	VID - 0.153
95	VID - 0.119	VID - 0.139	VID - 0.159
100	VID - 0.125	VID - 0.145	VID - 0.165
105	VID - 0.131	VID - 0.151	VID - 0.171
110	VID - 0.138	VID - 0.158	VID - 0.178
115	VID - 0.144	VID - 0.164	VID - 0.184
120	VID - 0.150	VID - 0.170	VID - 0.190

NOTES:

1. The V_{CC_MIN} and V_{CC_MAX} loadlines represent static and transient limits. Please see Section 2.12.1 for V_{CC} overshoot specifications.
2. This table is intended to aid in reading discrete points on Figure 2-4.
3. The loadlines specify voltage limits at the die measured at the VCCSENSE and VSSSENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins. Refer to the *Enterprise Voltage Regulator-Down (EVRD) 10.1 Design Guidelines* for socket loadline guidelines and VR implementation.

Figure 2-4. V_{CC} Static and Transient Tolerance



NOTES:

1. The V_{CC_MIN} and V_{CC_MAX} loadlines represent static and transient limits. Please see Section 2.12.1 for V_{CC} overshoot specifications.
2. The V_{CC_MIN} and V_{CC_MAX} loadlines are plots of the discrete point found in Table 2-8.
3. Refer to Table 2-7 for processor VID information.
4. The loadlines specify voltage limits at the die measured at the VCCSENSE and VSSSENSE pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins. Refer to the *Enterprise Voltage Regulator-Down (EVRD) 10.1 Design Guidelines* for socket loadline guidelines and VR implementation.

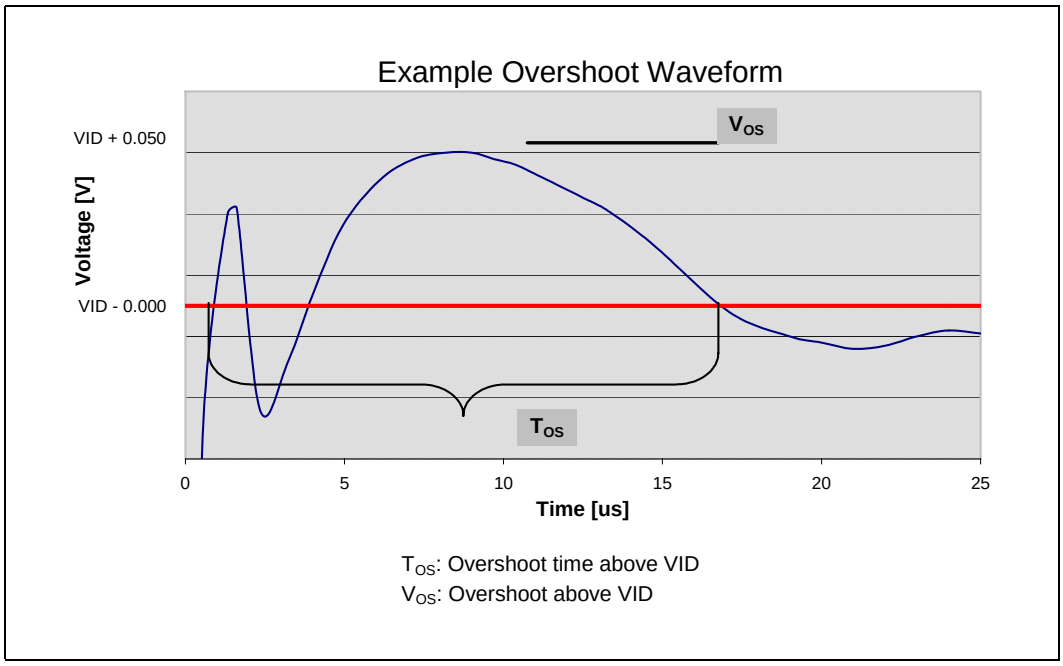
2.12.1 V_{CC} Overshoot Specification

The Dual-Core Intel Xeon processor can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V_{OS_MAX}. (V_{OS_MAX} is the maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the VCCSENSE and VSSSENSE pins.

Table 2-9. V_{CC} Overshoot Specifications

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CC} overshoot above VID		0.050	V	2-5	
T_{OS_MAX}	Time duration of V_{CC} overshoot above VID		25	µs	2-5	

Figure 2-5. V_{CC} Overshoot Example Waveform



NOTES:

1. V_{OS} is measured overshoot voltage.
2. T_{OS} is measured time duration above VID.

2.12.2 Die Voltage Validation

Overshoot events from application testing on processor must meet the specifications in Table 2-9 when measured across the VCCSENSE and VSSSENSE pins. Overshoot events that are < 10 ns in duration may be ignored. These measurement of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

Table 2-10. BSEL[1:0] and VID[5:0] Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
R_{ON}	BSEL[1:0] and VID[5:0] Buffer On Resistance	N/A		60	Ω	2
I_{OL}	Maximum Pin Current	N/A		8	mA	2
I_{LO}	Output Leakage Current	N/A		200	µA	2,3
R_{PULL_UP}	Pull-Up Resistor		500		Ω	4
V_{TOL}	Voltage Tolerance	0.95 * V_{TT}	V_{TT}	1.05 * V_{TT}	V	4

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are based on design characterization and are not tested.
3. Leakage to V_{SS} with pin held at V_{TT}.
4. Please refer to the appropriate platform design guide for implementation details.

Table 2-11. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	0.0	GTLREF - (0.10 * V_{TT})	V	2,3
V_{IH}	Input High Voltage	GTLREF + (0.10 * V_{TT})	V_{TT}	V	2,4,5
V_{OH}	Output High Voltage	0.90 * V_{TT}	V_{TT}	V	2,5
I_{OL}	Output Low Current	N/A	V_{TT} / (0.50 * R_{TT_MIN} + [R_{ON_MIN} ‖ R_L])	mA	2,6
I_{LI}	Input Leakage Current	N/A	± 200	µA	7,8
I_{LO}	Output Leakage Current	N/A	± 200	µA	7,8
R_{ON}	Buffer On Resistance	4	8	Ω	

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TT} represented in these specifications refers to instantaneous V_{TT}.
3. V_{IL} is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications in Section 3.
6. Refer to Table 2-4 to determine which signals include additional on-die termination resistance (R_L).
7. Leakage to V_{SS} with pin held at V_{TT}.
8. Leakage to V_{TT} with pin held at 300 mV.

Table 2-12. PWRGOOD Input and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes 1,2,5
V_{HYS}	Input Hysteresis	200	350	mV	3
V_{t+}	Input Low to High Threshold Voltage	0.5 * (V_{TT} + V_{HYS_MIN})	0.5 * (V_{TT} + V_{HYS_MAX})	V	4
V_{t-}	Input High to Low Threshold Voltage	0.5 * (V_{TT} - V_{HYS_MAX})	0.5 * (V_{TT} - V_{HYS_MIN})	V	4
V_{OH}	Output High Voltage	N/A	V_{TT}	V	4
I_{OL}	Output Low Current		45	mA	6
I_{LI}	Input Leakage Current	N/A	± 200	µA	
I_{LO}	Output Leakage Current	N/A	± 200	µA	
R_{ON}	Buffer On Resistance	4	8	Ω	

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open drain.
3. V_{HYS} represents the amount of hysteresis, nominally centered about 0.5 * V_{TT} for all PWRGOOD and TAP inputs.
4. The V_{TT} represented in these specifications refers to instantaneous V_{TT}.
5. PWRGOOD input and the TAP signal group must meet system signal quality specification in Section 3.
6. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.

Table 2-13. GTL+ Asynchronous and AGTL+ Asynchronous Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	0.0	GTLREF - (0.10 * V_{TT})	V	2,3
V_{IH}	Input High Voltage	GTLREF + (0.10 * V_{TT})	V_{TT}	V	2,4,5
V_{OH}	Output High Voltage	0.90 * V_{TT}	V_{TT}	V	2,5
I_{OL}	Output Low Current	N/A	V_{TT} / (0.50 * R_{TT_MIN} + [R_{ON_MIN} || R_L])	mA	2,6
I_{LI}	Input Leakage Current	N/A	± 200	µA	7,8
I_{LO}	Output Leakage Current	N/A	± 200	µA	7,8
R_{on}	Buffer On Resistance	4	8	Ω	

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TT} represented in these specifications refers to instantaneous V_{TT}.
3. V_{IL} is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications in Section 3.
6. Refer to Table 2-5 to determine which signals include additional on-die termination resistance (R_L).
7. Leakage to V_{SS} with pin held at V_{TT}.
8. Leakage to V_{TT} with pin held at 300 mV.

Table 2-14. VIDPWRGD DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	0.0	0.30	V	
V_{IH}	Input High Voltage	0.90	V_{TT}	V	

§

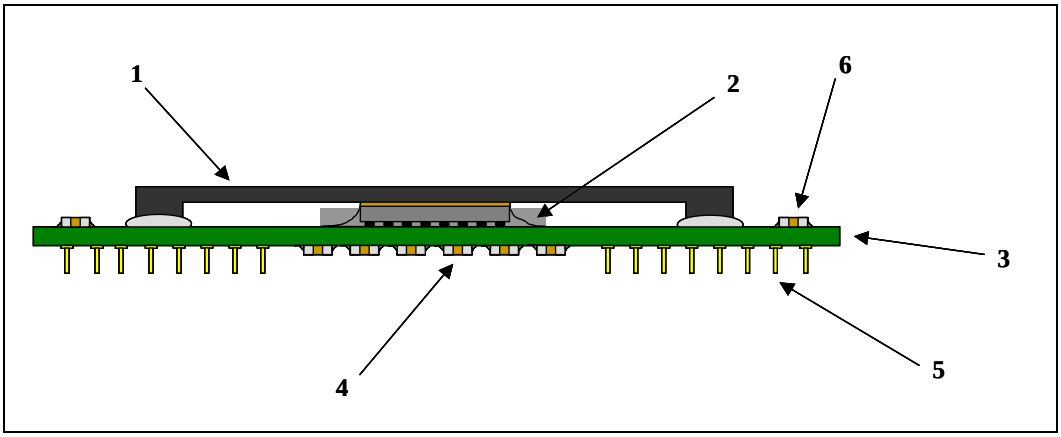
3 Mechanical Specifications

The Dual-Core Intel Xeon processor is packaged in Flip Chip Micro Pin Grid Array (FC-mPGA4) package that interfaces to the baseboard via an mPGA604 socket. The package consists of a processor core mounted on a substrate pin-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Figure 3-1 shows a sketch of the processor package components and how they are assembled together. Refer to the *mPGA604 Socket Design Guidelines* for complete details on the mPGA604 socket.

The package components shown in Figure 3-1 include the following:

1. Integrated Heat Spreader (IHS)
2. Processor Die
3. Substrate
4. Pin Side Capacitors
5. Package Pin
6. Die Side Capacitors

Figure 3-1. Processor Package Assembly Sketch



Note: This drawing is not to scale and is for reference only. The mPGA604 socket is not shown.

3.1 Package Mechanical Drawings

The package mechanical drawings are shown in Figure 3-2 and Figure 3-3. The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions include:

1. Package reference and tolerance dimensions (total height, length, width, etc.)
2. IHS parallelism and tilt
3. Pin dimensions
4. Top-side and back-side component keepout dimensions
5. Reference datums

All drawing dimensions are in mm [in.].

Figure 3-2. Processor Package Drawing (Sheet 1 of 2)

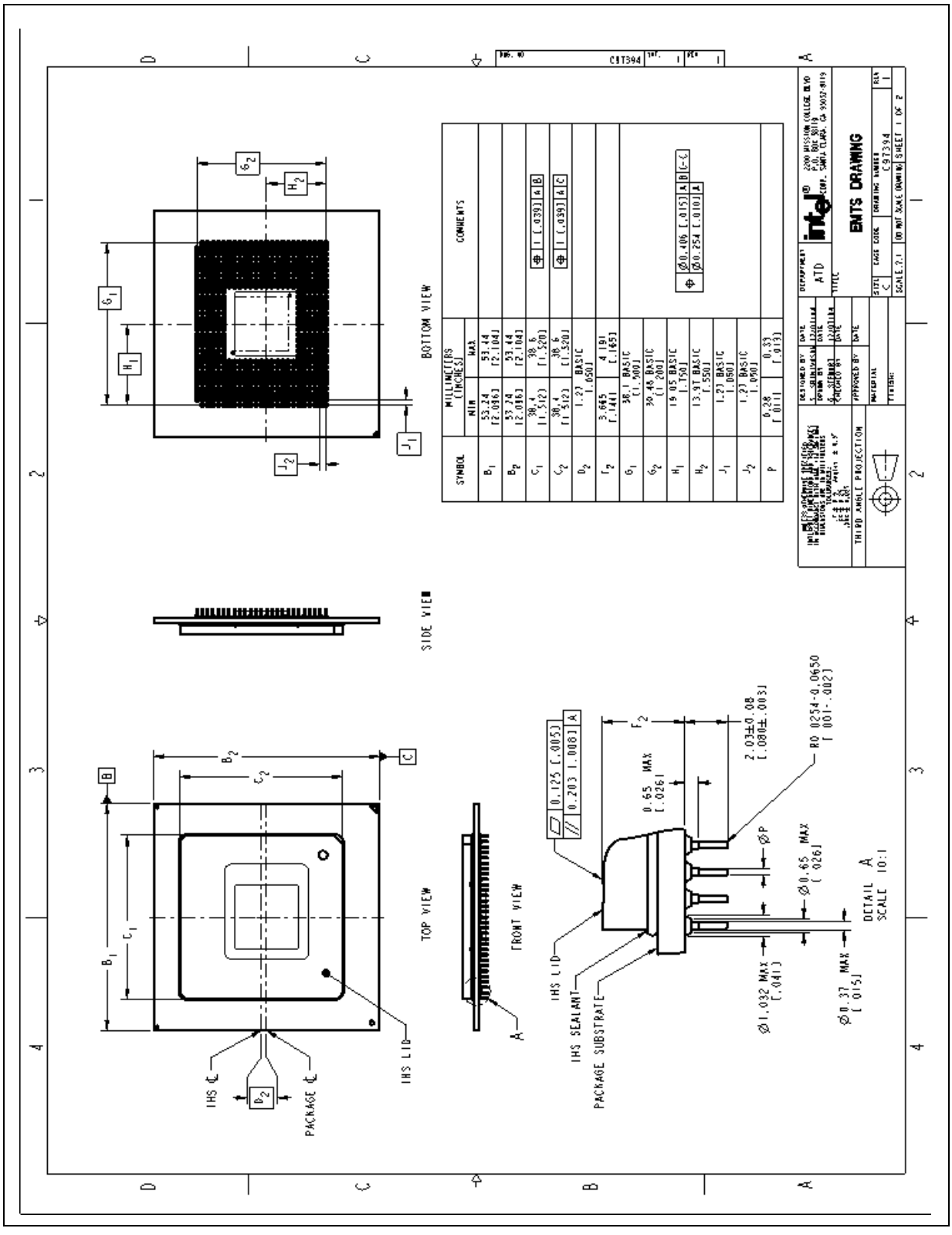
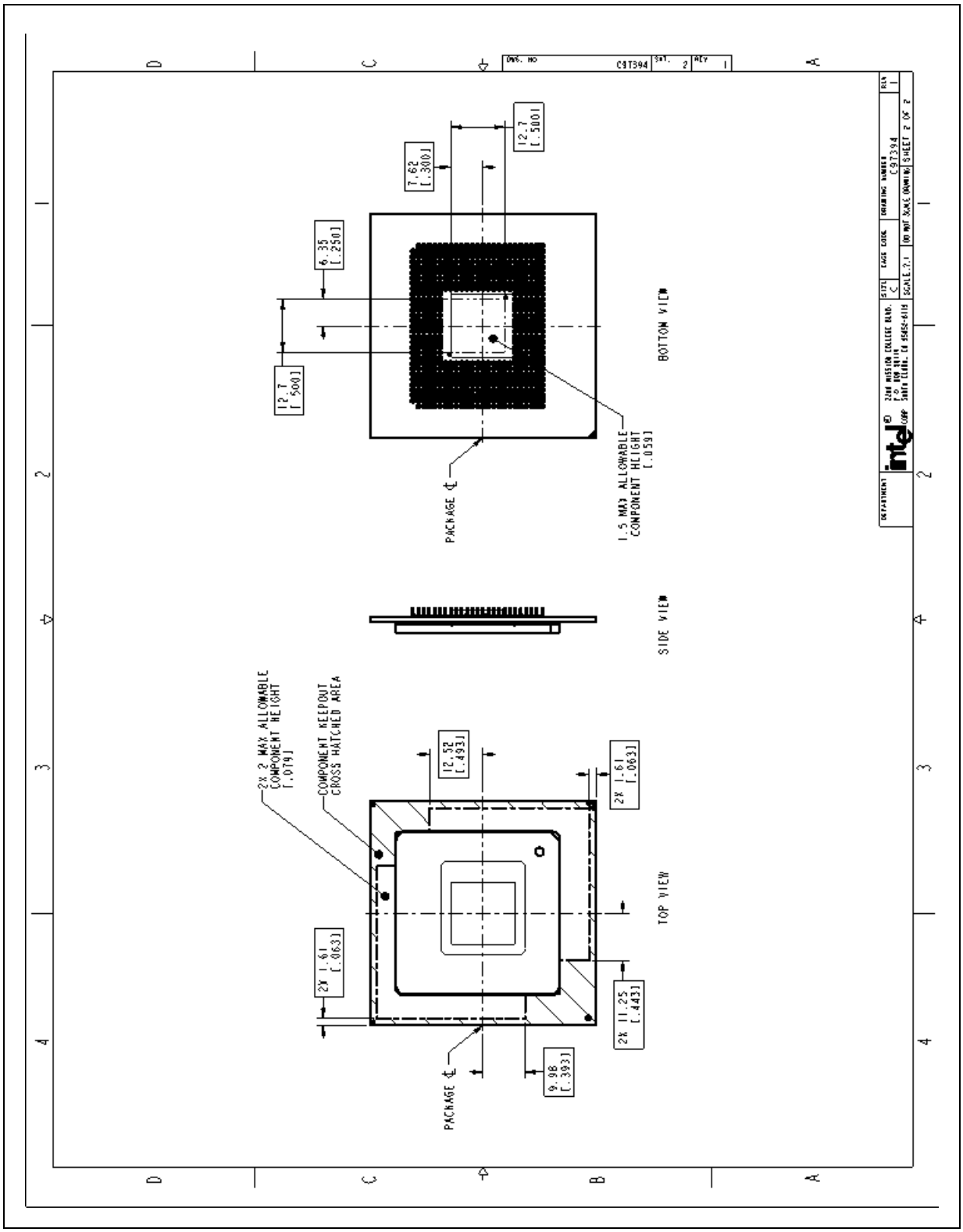


Figure 3-3. Processor Package Drawing (Sheet 2 of 2)



3.2 Processor Component Keepout Zones

The processor may contain components on the substrate that define component keepout zone requirements. A thermal and mechanical solution design must not intrude into the required keepout zones. Decoupling capacitors are typically mounted to either the topside or pin-side of the package substrate. See Figure 3-3 for keepout zones.

3.3 Package Loading Specifications

Table 3-1 provides dynamic and static load specifications for the processor package. These mechanical load limits should not be exceeded during heatsink assembly, mechanical stress testing or standard drop and shipping conditions. The heatsink attach solutions must not include continuous stress onto the processor with the exception of a uniform load to maintain the heatsink-to-processor thermal interface. Also, any mechanical system or component testing should not exceed these limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal or mechanical solutions.

Table 3-1. Processor Loading Specifications

Parameter	Min	Max	Unit	Notes
Static Compressive Load	44 10	222 50	N lbf	1,2,3,4
	44 10	288 65	N lbf	1,2,3,5
Dynamic Compressive Load	NA NA	222 N + 0.45 kg *100 G 50 lbf (static) + 1 lbm * 100 G	N lbf	1,3,4,6,7
	NA NA	288 N + 0.45 kg * 100 G 65 lbf (static) + 1 lbm * 100 G	N lbf	1,3,5,6,7
Transient	NA	445 100	N lbf	1,3,8

NOTES:

1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the minimum and maximum static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only and do not include the limits of the processor socket.
4. This specification applies for thermal retention solutions that allow baseboard deflection.
5. This specification applies either for thermal retention solutions that prevent baseboard deflection or for the Intel enabled reference solution (CEK).
6. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
7. Experimentally validated test condition used a heatsink mass of 1 lbm (~0.45 kg) with 100 G acceleration measured at heat sink mass. The dynamic portion of this specification in the product application can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this validated dynamic load (1 lbm x 100 G = 100 lb). Allowable strain in the dynamic compressive load specification is in addition to the strain allowed in static loading.
8. Transient loading is defined as a 2 second duration peak load superimposed on the static load requirement, representative of loads experienced by the package during heatsink installation.

3.4 Package Handling Guidelines

Table 3-2 includes a list of guidelines on a package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 3-2. Package Handling Guidelines

Parameter	Maximum Recommended	Notes
Shear	356 N 80 lbf	1,4,5
Tensile	156 N 35 lbf	2,4,5
Torque	8 N-m 70 lbf-in	3,4,5

NOTES:

1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. A tensile load is defined as a pulling load applied to the IHS in a direction normal to the IHS surface.
3. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.
4. These guidelines are based on limited testing for design characterization and incidental applications (one time only).
5. Handling guidelines are for the package only and do not include the limits of the processor socket.

3.5 Package Insertion Specifications

The Dual-Core Intel Xeon processor can be inserted and removed 15 times from an mPGA604 socket, which meets the criteria outlined in the *mPGA604 Socket Design Guidelines*.

3.6 Processor Mass Specifications

The typical mass of the Dual-Core Intel Xeon processor is approximately 35.750 grams. This mass [weight] includes all components which make up the entire processor product.

3.7 Processor Materials

The Dual-Core Intel Xeon processor is assembled from several components. The basic material properties are described in Table 3-3.

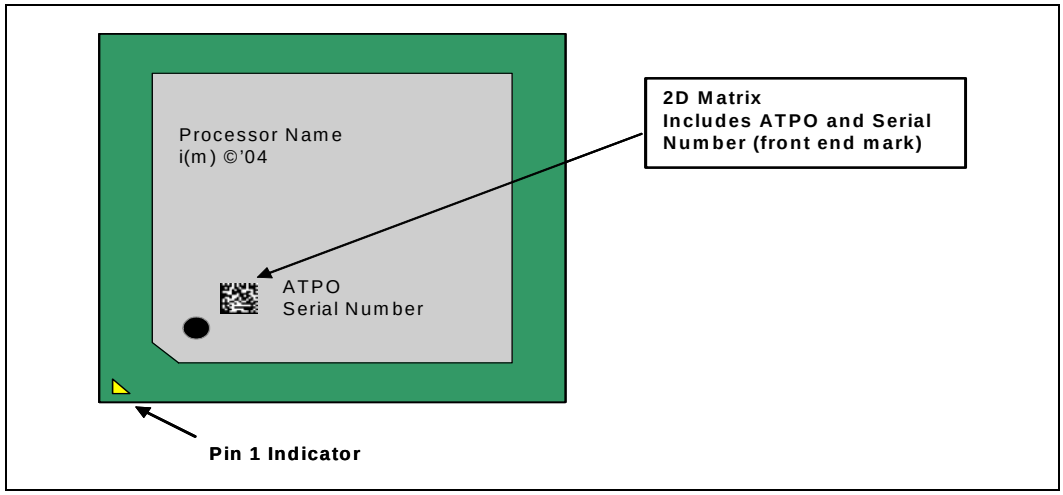
Table 3-3. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Fiber-Reinforced Resin
Substrate Pins	Gold Plated Copper

3.8 Processor Markings

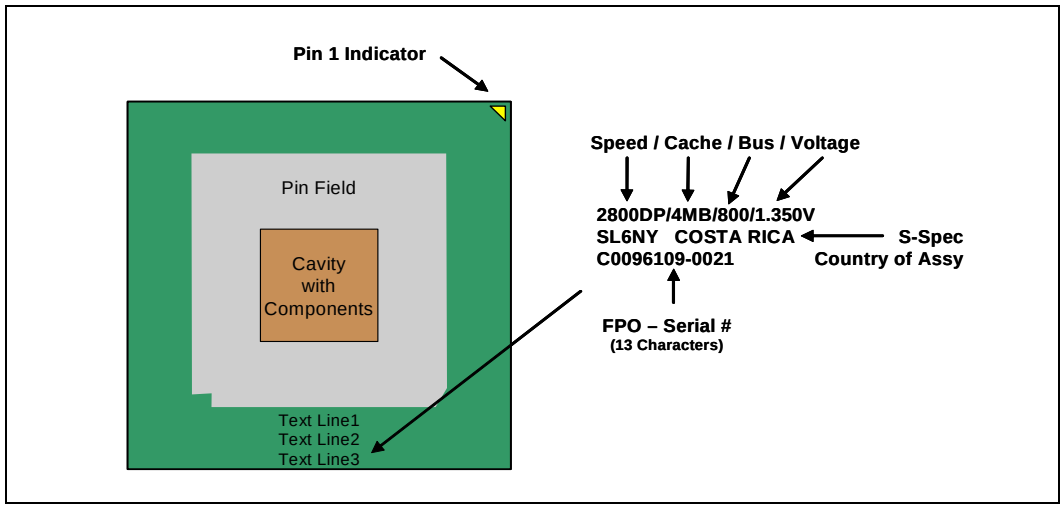
Figure 3-4 shows the topside markings and Figure 3-5 shows the bottom-side markings on the processor. These diagrams are to aid in the identification of the Dual-Core Intel Xeon processor.

Figure 3-4. Processor Top-Side Markings (Example)



NOTES:
1. All characters will be in upper case.
2. Drawing is not to scale.

Figure 3-5. Processor Bottom-Side Markings (Example)



NOTES:
1. All characters will be in upper case.
2. Drawing is not to scale.

3.9 Processor Pin-Out Coordinates

Figure 3-6 and Figure 3-7 show the top and bottom view of the processor pin coordinates, respectively. The coordinates are referred to throughout the document to identify processor pins.

Figure 3-6. Processor Pin-out Coordinates, Top View

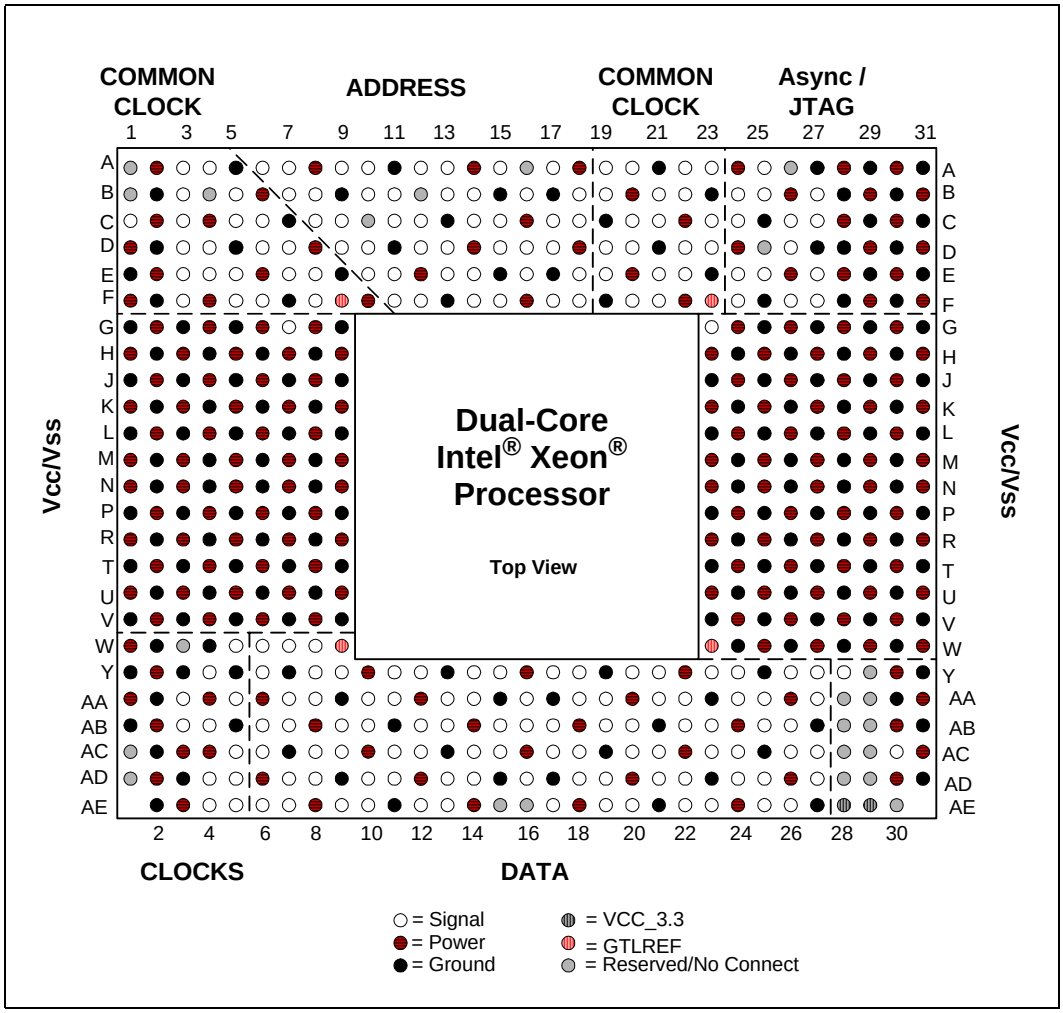
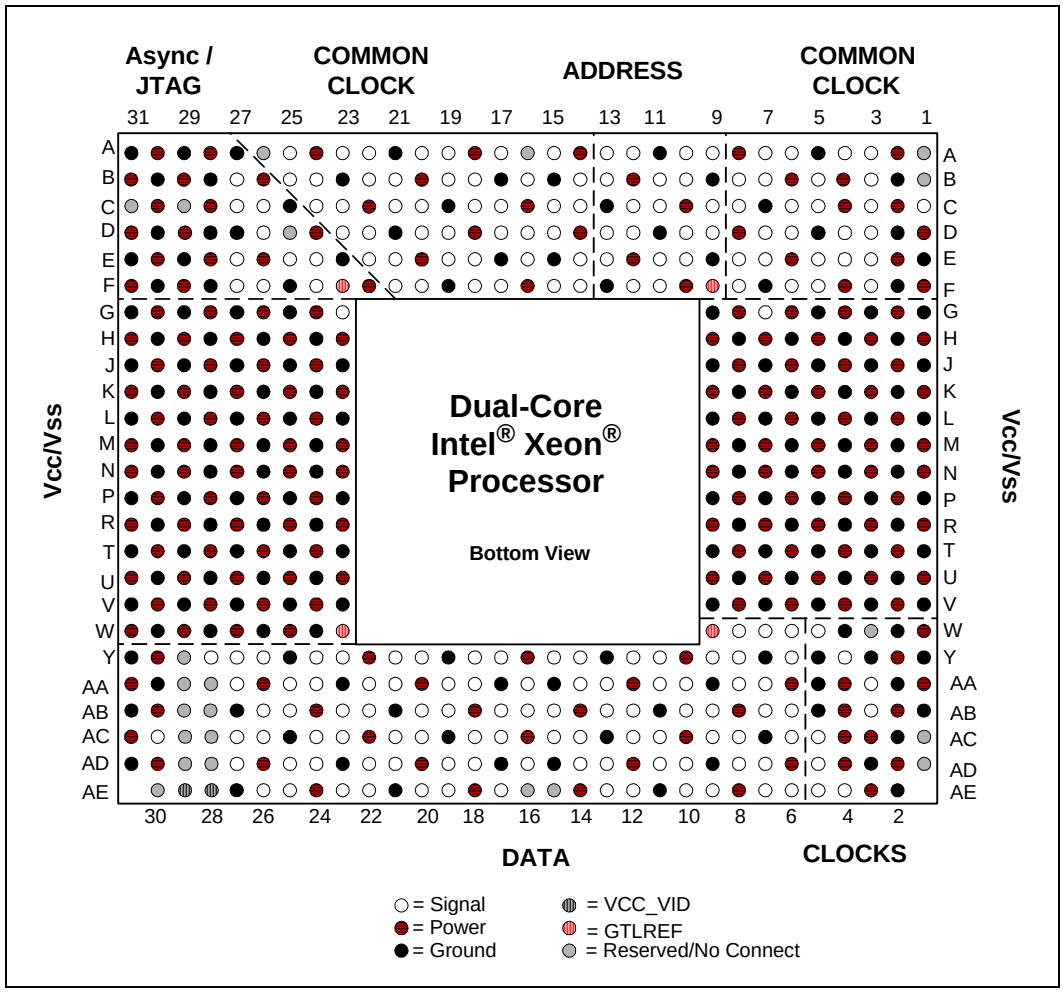


Figure 3-7. Processor Pin-out Coordinates, Bottom View



§

4 Signal Definitions

4.1 Signal Definitions

Table 4-1. Signal Definitions (Sheet 1 of 10)

Name	Type	Description	Notes
A[35:3]#	I/O	A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the front side bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processors sample a subset of the A[35:3]# pins to determine their power-on configuration. See Section 7.1.	3
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction.	2
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all (800 MHz) front side bus agents.	3
ADSTB[1:0]#	I/O	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edge. Strobes are associated with signals as shown below. **Signals** / **Associated Strobes** REQ[4:0]#, A[16:3]# — ADSTB0# A[35:17]# — ADSTB1#	3
AP[1:0]#	I/O	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]# pins. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Dual-Core Intel® Xeon® processor front side bus agents. The following table defines the coverage model of these signals. **Request Signals** / **Subphase 1** / **Subphase 2** A[35:24]# — AP0# — AP1# A[23:3]# — AP1# — AP0# REQ[4:0]# — AP1# — AP0#	3

Table 4-1. Signal Definitions (Sheet 2 of 10)

Name	Type	Description	Notes
BCLK[1:0]	I	The differential bus clock pair BCLK[1:0] determines the front side bus frequency. All processor front side bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.	3
BINIT#	I/O	BINIT# (Bus Initialization) may be observed and driven by all processor front side bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# observation is enabled during power-on configuration (see Figure 7.1) and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents **do not** reset their I/O Queue (IOQ) and transaction tracking state machines upon observation of BINIT# assertion. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the front side bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system. Since multiple agents may drive this signal at the same time, BINIT# is a wired-OR signal which must connect the appropriate pins of all processor front side bus agents. In order to avoid wired-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BINIT# is activated on specific clock edges and sampled on specific clock edges	3
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wired-OR signal which must connect the appropriate pins of all processor front side bus agents. In order to avoid wired-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.	3
BOOT_ SELECT	I	The BOOT_SELECT input informs the processor whether the platform supports the Dual-Core Intel® Xeon® processor. The processor will not operate if this signal is low. This input has a weak pull-up to V_{TT}.	
BPM[5:0]#	I/O	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all front side bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processors. BPM[5:4]# must be bussed to all bus agents. Please refer to the appropriate platform design guidelines for more detailed information. **These signals do not have on-die termination and must be terminated at the end agent. See the appropriate platform design guideline for additional information**.	2

Table 4-1. Signal Definitions (Sheet 3 of 10)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th><th>Notes</th></tr>
<tr><td>BPRI#</td><td>I</td><td>BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor front side bus. It must connect the appropriate pins of all processor front side bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.</td><td>3</td></tr>
<tr><td>BR0#
BR[1:3]#</td><td>I/O
I</td><td>BR[1:0]# (Bus Request) drive the BREQ[1:0]# signals in the system. The BREQ[1:0]# signals are interconnected in a rotating manner to individual processor pins. BR[3:2}# are connected between the two processor sockets and require termination. The tables below give the rotating interconnect between the processor and bus signals for 2-way systems.
BR[3:0]# Signals Rotating Interconnect, 2-way system
<table><tr><th>Bus Signal</th><th>Agent 0 Pins</th><th>Agent 1 Pins</th></tr><tr><td>BREQ0#</td><td>BR0#</td><td>BR1#</td></tr><tr><td>BREQ1#</td><td>BR1#</td><td>BR0#</td></tr><tr><td></td><td>BR2#</td><td>BR3#</td></tr><tr><td></td><td>BR3#</td><td>BR2#</td></tr></table>During power-on configuration, the central agent must assert the BREQ0# bus signal. All symmetric agents sample their BR[3:0]# pins on the active-to-inactive transition of RESET#. The pin which the agent samples asserted determines its agent ID.
These signals do not have on-die termination and must be terminated.</td><td>3</td></tr>
<tr><td>BSEL[1:0]</td><td>O</td><td>The BCLK[1:0] frequency select signals BSEL[1:0] are used to select the processor input clock frequency. Table 2-1 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processors, chipset, and clock synthesizer. All front side bus agents must operate at the same frequency. The Dual-Core Intel Xeon processor currently operates at a 800 MHz front side bus frequency (200 MHz BCLK[1:0] frequency). For more information about these pins, including termination recommendations, refer to the appropriate platform design guideline.</td><td></td></tr>
<tr><td>COMP[0]</td><td>I</td><td>COMP[0] must be terminated to V_{SS} on the baseboard using precision resistors. These inputs configure the GTL+ drivers of the processor. Refer to the appropriate platform design guidelines for implementation details.</td><td></td></tr>
</table>

Table 4-1. Signal Definitions (Sheet 4 of 10)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th><th>Notes</th></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor front side bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals, and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to strobes and DBI#.
<table>
<tr><th>Data Group</th><th>DSTBN#/ DSTBP#</th><th>DBI#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</td><td>3</td></tr>
<tr><td>DBI[3:0]#</td><td>I/O</td><td>DBI[3:0]# are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. If more than half the data bits, within a 16-bit group, would have been asserted electronically low, the bus agent may invert the data bus signals for that particular sub-phase for that 16-bit group.
DBI[3:0] Assignment To Data Bus
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DBI0#</td><td>D[15:0]#</td></tr>
<tr><td>DBI1#</td><td>D[31:16]#</td></tr>
<tr><td>DBI2#</td><td>D[47:32]#</td></tr>
<tr><td>DBI3#</td><td>D[63:48]#</td></tr>
</table></td><td>3</td></tr>
<tr><td>DBSY#</td><td>I/O</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor front side bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor front side bus agents.</td><td>3</td></tr>
<tr><td>DEFER#</td><td>I</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all processor front side bus agents.</td><td>3</td></tr>
<tr><td>DP[3:0]#</td><td>I/O</td><td>DP[3:0]# (Data Parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all processor front side bus agents.</td><td>3</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor front side bus agents.</td><td>3</td></tr>
</table>

Table 4-1. Signal Definitions (Sheet 5 of 10)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th><th>Notes</th></tr>
<tr><td>DSTBN[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.

<table><tr><th>Signals</th><th>Associated Strobes</th></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBN3#</td></tr></table></td><td>3</td></tr>
<tr><td>DSTBP[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.

<table><tr><th>Signals</th><th>Associated Strobes</th></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#</td></tr></table></td><td>3</td></tr>
<tr><td>FERR#/PBE#</td><td>O</td><td>FERR#/PBE# (floating-point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to Vol. 3 of the IA-32 Intel® Architecture Software Developer’s Manual and the AP-485 Intel® Processor Identification and the CPUID Instruction application note.
This signal does not have on-die termination and must be terminated at the end agent. See the appropriate platform design guideline for additional information.</td><td>3</td></tr>
<tr><td>FORCEPR#</td><td>I</td><td>The FORCEPR# input can be used by the platform to force the Dual-Core Intel Xeon processor to activate the Thermal Control Circuit (TCC). The TCC will remain active until the system deasserts FORCEPR#.</td><td></td></tr>
<tr><td>GTLREF</td><td>I</td><td>GTLREF determines the signal reference level for GTL+ input pins. GTLREF is used by the GTL+ receivers to determine if a signal is a logical 0 or a logical 1.</td><td></td></tr>
<tr><td>HIT#
HITM#</td><td>I/O
I/O</td><td>HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any front side bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
Since multiple agents may deliver snoop results at the same time, HIT# and HITM# are wired-OR signals which must connect the appropriate pins of all processor front side bus agents. In order to avoid wired-OR glitches associated with simultaneous edge transitions driven by multiple drivers, HIT# and HITM# are activated on specific clock edges and sampled on specific clock edges.</td><td>3</td></tr>
</table>

Table 4-1. Signal Definitions (Sheet 6 of 10)

Name	Type	Description	Notes
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor front side bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#. **This signal does not have on-die termination and must be terminated at the end agent. See the appropriate platform design guideline for additional information.**	2
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction.	2
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside all processors without affecting their internal caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor front side bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).	2
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all front side bus agents. When the APIC functionality is disabled, the LINT0/INTR signal becomes INTR, a maskable interrupt request signal, and LINT1/NMI becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous. These signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.	2
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor front side bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor front side bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor front side bus throughout the bus locked operation and ensure the atomicity of lock.	3

Table 4-1. Signal Definitions (Sheet 7 of 10)

Name	Type	Description	Notes
MCERR#	I/O	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor front side bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programming Guide*. Since multiple agents may drive this signal at the same time, MCERR# is a wired-OR signal which must connect the appropriate pins of all processor front side bus agents. In order to avoid wired-OR glitches associated with simultaneous edge transitions driven by multiple drivers, MCERR# is activated on specific clock edges and sampled on specific clock edges.	
ODTEN	I	ODTEN (On-die termination enable) should be connected to V_{TT} to enable on-die termination for end bus agents. For middle bus agents, pull this signal down via a resistor to ground to disable on-die termination. Whenever ODTEN is high, on-die termination will be active, regardless of other states of the bus.	
OPTIMIZED/ COMPAT#	I	This is an input pin to the processor to determine if the processor is in an optimized platform or a compatible platform. This signal does includes a weak on-die pull-up to V_{TT}.	
PROCHOT#	O	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor die temperature has reached its factory configured trip point. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. See Section 6.2.3 for more details.	
PWRGOOD	I	PWRGOOD (Power Good) is an input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 2-13, and be followed by a 1-10 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.	2
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor front side bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[1:0]#. Refer to the AP[1:0]# signal description for details on parity checking of these signals.	3

Table 4-1. Signal Definitions (Sheet 8 of 10)

Name	Type	Description	Notes
RESET#	I	Asserting the RESET# signal resets all processors to known states and invalidates their internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least 1 ms after VCC and BCLK have reached their proper specifications. On observing active RESET#, all front side bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 7.1. **This signal does not have on-die termination and must be terminated at the end agent. See the appropriate platform design guideline for additional information**.	3
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor front side bus agents.	3
RSP#	I	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor front side bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.	3
SKTOCC#	O	SKTOCC# (Socket occupied) will be pulled to ground by the processor to indicate that the processor is present. There is no connection to the processor silicon for this signal.	
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Lock Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will only recognize the assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units.	2
SMB_PRT	O	The SMBus present (SMB_PRT) pin is defined to inform the platform if the installed processor includes SMBus components such as the integrated thermal sensor and the processor information ROM (PIROM). This pin is tied to VSS by the processor if these features are not present. Platforms utilizing this pin should use a pull up resistor to the appropriate voltage level for the logic tied to this pin. Because this pin does not connect to the processor silicon, any platform voltage and termination value is acceptable.	
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tri-state its outputs.	2
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the front side bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.	2

Table 4-1. Signal Definitions (Sheet 9 of 10)

Name	Type	Description	Notes
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).	
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.	
TEST_BUS	I	Must be connected to all other processor TEST_BUS signals in the system. See the appropriate platform design guide for termination details.	
TESTHI[6:0]	I	All TESTHI inputs should be individually connected to V_{TT} via a pull-up resistor which matches the trace impedance. TESTHI[3:0] and TESTHI[6:5] may all be tied together and pulled up to V_{TT} with a single resistor if desired. However, utilization of boundary scan test will not be functional if these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins. For optimum noise margin, all pull-up resistor values used for TESTHI[6:0] should have a resistance value within ± 20% of the impedance of the baseboard transmission line traces. For example, if the trace impedance is 50 Ω, than a value between 40 Ω and 60 Ω should be used.	
THERMDA	Other	Thermal Diode Anode. See Section 6.2.7.	
THERMDC	Other	Thermal Diode Cathode. See Section 6.2.7.	
THERMTRIP#	O	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a temperature beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor its core voltage (V_{CC}) must be removed following the assertion of THERMTRIP#. Driving of the THERMTRIP# signals is enabled within 10 ms of the assertion of PWRGOOD and is disabled on de-assertion of PWRGOOD. Once activated, THERMTRIP# remains latched until PWRGOOD is de-asserted. While the de-assertion of the PWRGOOD signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 ms of the assertion of PWRGOOD.	1
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. **This signal does not have on-die termination and must be terminated at the end agent.**	
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all front side bus agents.	
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.	
V_{CCA}	I	V_{CCA} provides isolated power for the analog portion of the internal processor core PLL's. Refer to the appropriate platform design guidelines for complete implementation details.	
$V_{CCIOPLL}$	I	$V_{CCIOPLL}$ provides isolated power for digital portion of the internal processor core PLL's. Refer to the appropriate platform design guidelines for complete implementation details.	
V_{CCPLL}	I	The on-die PLL filter solution will not be implemented on this platform. The V_{CCPLL} input should be left unconnected.	

Table 4-1. Signal Definitions (Sheet 10 of 10)

Name	Type	Description	Notes
VCCSENSE VSSSENSE	O	VCCSENSE and VSSSENSE provide an isolated, low impedance connection to the processor core power and ground. They can be used to sense or measure power near the silicon with little noise.	
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). These are open drain signals that are driven by the processor and must be pulled up through a resistor. Conversely, the VR output must be disabled prior to the voltage supply for these pins becomes invalid. The VID pins are needed to support processor voltage specification variations. See Table 2-2 for definitions of these pins. The VR must supply the voltage that is requested by these pins, or disable itself.	
VIDPWRGD	I	The processor requires this input to determine that the supply voltage for BSEL[1:0] and VID[5:0] is stable and within specification.	
V_{SSA}	I	V_{SSA} provides an isolated, **internal** ground for internal PLL's. Do not connect directly to ground. This pin is to be connected to V_{CCA} and $V_{CCIOPLL}$ through a discrete filter circuit.	
V_{TT}	P	The front side bus termination voltage input pins. Refer to Table 2-7 for further details.	
VTTEN	O	The VTTEN can be used as an output enable for the VTT regulator in the event an incompatible processor is inserted into the platform. There is no connection to the processor silicon for this signal and it must be pulled up through a resistor. Refer to the appropriate platform design guidelines for implementation details.	

NOTES:
1. For this pin on Dual-Core Intel Xeon processor, the maximum number of symmetric agents is one. Maximum number of central agents is zero.
2. For this pin on Dual-Core Intel Xeon processor, the maximum number of symmetric agents is two. Maximum number of central agents is zero.
3. For this pin on Dual-Core Intel Xeon processor, the maximum number of symmetric agents is two. Maximum number of central agents is one.

5 Pin Listing

5.1 Dual-Core Intel® Xeon® Processor Pin Assignments

This section provides sorted pin lists in Table 5-1 and Table 5-2. Table 5-1 is a listing of all processor pins ordered alphabetically by pin name. Table 5-2 is a listing of all processor pins ordered by pin number.

5.1.1 Pin Listing by Pin Name

Table 5-1. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
A3#	A22	Source Sync	Input/Output
A4#	A20	Source Sync	Input/Output
A5#	B18	Source Sync	Input/Output
A6#	C18	Source Sync	Input/Output
A7#	A19	Source Sync	Input/Output
A8#	C17	Source Sync	Input/Output
A9#	D17	Source Sync	Input/Output
A10#	A13	Source Sync	Input/Output
A11#	B16	Source Sync	Input/Output
A12#	B14	Source Sync	Input/Output
A13#	B13	Source Sync	Input/Output
A14#	A12	Source Sync	Input/Output
A15#	C15	Source Sync	Input/Output
A16#	C14	Source Sync	Input/Output
A17#	D16	Source Sync	Input/Output
A18#	D15	Source Sync	Input/Output
A19#	F15	Source Sync	Input/Output
A20#	A10	Source Sync	Input/Output
A21#	B10	Source Sync	Input/Output
A22#	B11	Source Sync	Input/Output
A23#	C12	Source Sync	Input/Output
A24#	E14	Source Sync	Input/Output
A25#	D13	Source Sync	Input/Output
A26#	A9	Source Sync	Input/Output
A27#	B8	Source Sync	Input/Output
A28#	E13	Source Sync	Input/Output
A29#	D12	Source Sync	Input/Output

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
A30#	C11	Source Sync	Input/Output
A31#	B7	Source Sync	Input/Output
A32#	A6	Source Sync	Input/Output
A33#	A7	Source Sync	Input/Output
A34#	C9	Source Sync	Input/Output
A35#	C8	Source Sync	Input/Output
A20M#	F27	Async GTL+	Input
ADS#	D19	Common Clk	Input/Output
ADSTB0#	F17	Source Sync	Input/Output
ADSTB1#	F14	Source Sync	Input/Output
AP0#	E10	Common Clk	Input/Output
AP1#	D9	Common Clk	Input/Output
BCLK0	Y4	Sys Bus Clk	Input
BCLK1	W5	Sys Bus Clk	Input
BINIT#	F11	Common Clk	Input/Output
BNR#	F20	Common Clk	Input/Output
BOOT_SELECT	G7	Power/Other	Input
BPM0#	F6	Common Clk	Input/Output
BPM1#	F8	Common Clk	Input/Output
BPM2#	E7	Common Clk	Input/Output
BPM3#	F5	Common Clk	Input/Output
BPM4#	E8	Common Clk	Input/Output
BPM5#	E4	Common Clk	Input/Output
BPRI#	D23	Common Clk	Input
BR0#	D20	Common Clk	Input/Output
BR1#	F12	Common Clk	Input
BR2#	E11	Common Clk	Input

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
BR3#	D10	Common Clk	Input
BSEL0	AA3	Power/Other	Output
BSEL1	AB3	Power/Other	Output
COMP0	AD16	Power/Other	Input
D0#	Y26	Source Sync	Input/Output
D1#	AA27	Source Sync	Input/Output
D2#	Y24	Source Sync	Input/Output
D3#	AA25	Source Sync	Input/Output
D4#	AD27	Source Sync	Input/Output
D5#	Y23	Source Sync	Input/Output
D6#	AA24	Source Sync	Input/Output
D7#	AB26	Source Sync	Input/Output
D8#	AB25	Source Sync	Input/Output
D9#	AB23	Source Sync	Input/Output
D10#	AA22	Source Sync	Input/Output
D11#	AA21	Source Sync	Input/Output
D12#	AB20	Source Sync	Input/Output
D13#	AB22	Source Sync	Input/Output
D14#	AB19	Source Sync	Input/Output
D15#	AA19	Source Sync	Input/Output
D16#	AE26	Source Sync	Input/Output
D17#	AC26	Source Sync	Input/Output
D18#	AD25	Source Sync	Input/Output
D19#	AE25	Source Sync	Input/Output
D20#	AC24	Source Sync	Input/Output
D21#	AD24	Source Sync	Input/Output
D22#	AE23	Source Sync	Input/Output
D23#	AC23	Source Sync	Input/Output
D24#	AA18	Source Sync	Input/Output
D25#	AC20	Source Sync	Input/Output
D26#	AC21	Source Sync	Input/Output
D27#	AE22	Source Sync	Input/Output
D28#	AE20	Source Sync	Input/Output
D29#	AD21	Source Sync	Input/Output
D30#	AD19	Source Sync	Input/Output
D31#	AB17	Source Sync	Input/Output
D32#	AB16	Source Sync	Input/Output
D33#	AA16	Source Sync	Input/Output

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
D34#	AC17	Source Sync	Input/Output
D35#	AE13	Source Sync	Input/Output
D36#	AD18	Source Sync	Input/Output
D37#	AB15	Source Sync	Input/Output
D38#	AD13	Source Sync	Input/Output
D39#	AD14	Source Sync	Input/Output
D40#	AD11	Source Sync	Input/Output
D41#	AC12	Source Sync	Input/Output
D42#	AE10	Source Sync	Input/Output
D43#	AC11	Source Sync	Input/Output
D44#	AE9	Source Sync	Input/Output
D45#	AD10	Source Sync	Input/Output
D46#	AD8	Source Sync	Input/Output
D47#	AC9	Source Sync	Input/Output
D48#	AA13	Source Sync	Input/Output
D49#	AA14	Source Sync	Input/Output
D50#	AC14	Source Sync	Input/Output
D51#	AB12	Source Sync	Input/Output
D52#	AB13	Source Sync	Input/Output
D53#	AA11	Source Sync	Input/Output
D54#	AA10	Source Sync	Input/Output
D55#	AB10	Source Sync	Input/Output
D56#	AC8	Source Sync	Input/Output
D57#	AD7	Source Sync	Input/Output
D58#	AE7	Source Sync	Input/Output
D59#	AC6	Source Sync	Input/Output
D60#	AC5	Source Sync	Input/Output
D61#	AA8	Source Sync	Input/Output
D62#	Y9	Source Sync	Input/Output
D63#	AB6	Source Sync	Input/Output
DBSY#	F18	Common Clk	Input/Output
DEFER#	C23	Common Clk	Input
DBI0#	AC27	Source Sync	Input/Output
DBI1#	AD22	Source Sync	Input/Output
DBI2#	AE12	Source Sync	Input/Output
DBI3#	AB9	Source Sync	Input/Output
DP0#	AC18	Common Clk	Input/Output
DP1#	AE19	Common Clk	Input/Output

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
DP2#	AC15	Common Clk	Input/Output
DP3#	AE17	Common Clk	Input/Output
DRDY#	E18	Common Clk	Input/Output
DSTBN0#	Y21	Source Sync	Input/Output
DSTBN1#	Y18	Source Sync	Input/Output
DSTBN2#	Y15	Source Sync	Input/Output
DSTBN3#	Y12	Source Sync	Input/Output
DSTBP0#	Y20	Source Sync	Input/Output
DSTBP1#	Y17	Source Sync	Input/Output
DSTBP2#	Y14	Source Sync	Input/Output
DSTBP3#	Y11	Source Sync	Input/Output
FERR#/PBE#	E27	Async GTL+	Output
FORCEPR#	A15	Async GTL+	Input
GTLREF	W23	Power/Other	Input
GTLREF	W9	Power/Other	Input
GTLREF	F23	Power/Other	Input
GTLREF	F9	Power/Other	Input
HIT#	E22	Common Clk	Input/Output
HITM#	A23	Common Clk	Input/Output
IERR#	E5	Async GTL+	Output
IGNNE#	C26	Async GTL+	Input
INIT#	D6	Async GTL+	Input
LINT0/INTR	B24	Async GTL+	Input
LINT1/NMI	G23	Async GTL+	Input
LOCK#	A17	Common Clk	Input/Output
MCERR#	D7	Common Clk	Input/Output
N/C	Y29	N/C	N/C
N/C	AA28	N/C	N/C
N/C	AA29	N/C	N/C
N/C	AB28	N/C	N/C
N/C	AB29	N/C	N/C
N/C	AC28	N/C	N/C
N/C	AC29	N/C	N/C
N/C	AD28	N/C	N/C
N/C	AD29	N/C	N/C
N/C	AE30	N/C	N/C
ODTEN	B5	Power/Other	Input

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
OPTIMIZED/ COMPAT#	C1	Power/Other	Input
PROCHOT#	B25	Async GTL+	Output
PWRGOOD	AB7	Async GTL+	Input
REQ0#	B19	Source Sync	Input/Output
REQ1#	B21	Source Sync	Input/Output
REQ2#	C21	Source Sync	Input/Output
REQ3#	C20	Source Sync	Input/Output
REQ4#	B22	Source Sync	Input/Output
Reserved	A26	Reserved	Reserved
Reserved	D25	Reserved	Reserved
Reserved	W3	Reserved	Reserved
Reserved	Y3	Reserved	Reserved
Reserved	AC1	Reserved	Reserved
Reserved	AE15	Reserved	Reserved
Reserved	AE16	Reserved	Reserved
Reserved	AE28	Reserved	Reserved
Reserved	AE29	Reserved	Reserved
RESET#	Y8	Common Clk	Input
RS0#	E21	Common Clk	Input
RS1#	D22	Common Clk	Input
RS2#	F21	Common Clk	Input
RSP#	C6	Common Clk	Input
SKTOCC#	A3	Power/Other	Output
SLP#	AE6	Async GTL+	Input
SMB_PRT	AE4	Power/Other	Output
SMI#	C27	Async GTL+	Input
STPCLK#	D4	Async GTL+	Input
TCK	E24	TAP	Input
TDI	C24	TAP	Input
TDO	E25	TAP	Output
TEST_BUS	A16	Power/Other	Input
TESTHI0	W6	Power/Other	Input
TESTHI1	W7	Power/Other	Input
TESTHI2	W8	Power/Other	Input
TESTHI3	Y6	Power/Other	Input
TESTHI4	AA7	Power/Other	Input
TESTHI5	AD5	Power/Other	Input

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
TESTHI6	AE5	Power/Other	Input
THERMDA	Y27	Power/Other	Output
THERMDC	Y28	Power/Other	Output
THERMTRIP#	F26	Async GTL+	Output
TMS	A25	TAP	Input
TRDY#	E19	Common Clk	Input
TRST#	F24	TAP	Input
VCC	A2	Power/Other	
VCC	A8	Power/Other	
VCC	A14	Power/Other	
VCC	A18	Power/Other	
VCC	A24	Power/Other	
VCC	A28	Power/Other	
VCC	A30	Power/Other	
VCC	B6	Power/Other	
VCC	B20	Power/Other	
VCC	B26	Power/Other	
VCC	B29	Power/Other	
VCC	B31	Power/Other	
VCC	C2	Power/Other	
VCC	C4	Power/Other	
VCC	C16	Power/Other	
VCC	C22	Power/Other	
VCC	C28	Power/Other	
VCC	C30	Power/Other	
VCC	D1	Power/Other	
VCC	D8	Power/Other	
VCC	D14	Power/Other	
VCC	D18	Power/Other	
VCC	D24	Power/Other	
VCC	D29	Power/Other	
VCC	D31	Power/Other	
VCC	E2	Power/Other	
VCC	E6	Power/Other	
VCC	E20	Power/Other	
VCC	E26	Power/Other	
VCC	E28	Power/Other	
VCC	E30	Power/Other	

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	F1	Power/Other	
VCC	F4	Power/Other	
VCC	F16	Power/Other	
VCC	F22	Power/Other	
VCC	F29	Power/Other	
VCC	F31	Power/Other	
VCC	G2	Power/Other	
VCC	G4	Power/Other	
VCC	G6	Power/Other	
VCC	G8	Power/Other	
VCC	G24	Power/Other	
VCC	G26	Power/Other	
VCC	G28	Power/Other	
VCC	G30	Power/Other	
VCC	H1	Power/Other	
VCC	H3	Power/Other	
VCC	H5	Power/Other	
VCC	H7	Power/Other	
VCC	H9	Power/Other	
VCC	H23	Power/Other	
VCC	H25	Power/Other	
VCC	H27	Power/Other	
VCC	H29	Power/Other	
VCC	H31	Power/Other	
VCC	J2	Power/Other	
VCC	J4	Power/Other	
VCC	J6	Power/Other	
VCC	J8	Power/Other	
VCC	J24	Power/Other	
VCC	J26	Power/Other	
VCC	J28	Power/Other	
VCC	J30	Power/Other	
VCC	K1	Power/Other	
VCC	K3	Power/Other	
VCC	K5	Power/Other	
VCC	K7	Power/Other	
VCC	K9	Power/Other	
VCC	K23	Power/Other	

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	K25	Power/Other	
VCC	K27	Power/Other	
VCC	K29	Power/Other	
VCC	K31	Power/Other	
VCC	L2	Power/Other	
VCC	L4	Power/Other	
VCC	L6	Power/Other	
VCC	L8	Power/Other	
VCC	L24	Power/Other	
VCC	L26	Power/Other	
VCC	L28	Power/Other	
VCC	L30	Power/Other	
VCC	M1	Power/Other	
VCC	M3	Power/Other	
VCC	M5	Power/Other	
VCC	M7	Power/Other	
VCC	M9	Power/Other	
VCC	M23	Power/Other	
VCC	M25	Power/Other	
VCC	M27	Power/Other	
VCC	M29	Power/Other	
VCC	M31	Power/Other	
VCC	N1	Power/Other	
VCC	N3	Power/Other	
VCC	N5	Power/Other	
VCC	N7	Power/Other	
VCC	N9	Power/Other	
VCC	N23	Power/Other	
VCC	N25	Power/Other	
VCC	N27	Power/Other	
VCC	N29	Power/Other	
VCC	N31	Power/Other	
VCC	P2	Power/Other	
VCC	P4	Power/Other	
VCC	P6	Power/Other	
VCC	P8	Power/Other	
VCC	P24	Power/Other	
VCC	P26	Power/Other	

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	P28	Power/Other	
VCC	P30	Power/Other	
VCC	R1	Power/Other	
VCC	R3	Power/Other	
VCC	R5	Power/Other	
VCC	R7	Power/Other	
VCC	R9	Power/Other	
VCC	R23	Power/Other	
VCC	R25	Power/Other	
VCC	R27	Power/Other	
VCC	R29	Power/Other	
VCC	R31	Power/Other	
VCC	T2	Power/Other	
VCC	T4	Power/Other	
VCC	T6	Power/Other	
VCC	T8	Power/Other	
VCC	T24	Power/Other	
VCC	T26	Power/Other	
VCC	T28	Power/Other	
VCC	T30	Power/Other	
VCC	U1	Power/Other	
VCC	U3	Power/Other	
VCC	U5	Power/Other	
VCC	U7	Power/Other	
VCC	U9	Power/Other	
VCC	U23	Power/Other	
VCC	U25	Power/Other	
VCC	U27	Power/Other	
VCC	U29	Power/Other	
VCC	U31	Power/Other	
VCC	V2	Power/Other	
VCC	V4	Power/Other	
VCC	V6	Power/Other	
VCC	V8	Power/Other	
VCC	V24	Power/Other	
VCC	V26	Power/Other	
VCC	V28	Power/Other	
VCC	V30	Power/Other	

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	W1	Power/Other	
VCC	W25	Power/Other	
VCC	W27	Power/Other	
VCC	W29	Power/Other	
VCC	W31	Power/Other	
VCC	Y2	Power/Other	
VCC	Y16	Power/Other	
VCC	Y22	Power/Other	
VCC	Y30	Power/Other	
VCC	AA1	Power/Other	
VCC	AA4	Power/Other	
VCC	AA6	Power/Other	
VCC	AA20	Power/Other	
VCC	AA26	Power/Other	
VCC	AA31	Power/Other	
VCC	AB2	Power/Other	
VCC	AB8	Power/Other	
VCC	AB14	Power/Other	
VCC	AB18	Power/Other	
VCC	AB24	Power/Other	
VCC	AB30	Power/Other	
VCC	AC3	Power/Other	
VCC	AC4	Power/Other	
VCC	AC16	Power/Other	
VCC	AC22	Power/Other	
VCC	AC31	Power/Other	
VCC	AD2	Power/Other	
VCC	AD6	Power/Other	
VCC	AD20	Power/Other	
VCC	AD26	Power/Other	
VCC	AD30	Power/Other	
VCC	AE3	Power/Other	
VCC	AE8	Power/Other	
VCC	AE14	Power/Other	
VCC	AE18	Power/Other	
VCC	AE24	Power/Other	
VCCA	AB4	Power/Other	Input
VCCIOPLL	AD4	Power/Other	Input

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VCCPLL	AD1	Power/Other	Input
VCCSENSE	B27	Power/Other	Output
VID0	F3	Power/Other	Output
VID1	E3	Power/Other	Output
VID2	D3	Power/Other	Output
VID3	C3	Power/Other	Output
VID4	B3	Power/Other	Output
VID5	A1	Power/Other	Output
VIDPWRGD	B1	Power/Other	Input
VSS	A5	Power/Other	
VSS	A11	Power/Other	
VSS	A21	Power/Other	
VSS	A27	Power/Other	
VSS	A29	Power/Other	
VSS	A31	Power/Other	
VSS	B2	Power/Other	
VSS	B9	Power/Other	
VSS	B15	Power/Other	
VSS	B17	Power/Other	
VSS	B23	Power/Other	
VSS	B28	Power/Other	
VSS	B30	Power/Other	
VSS	C7	Power/Other	
VSS	C13	Power/Other	
VSS	C19	Power/Other	
VSS	C25	Power/Other	
VSS	C29	Power/Other	
VSS	C31	Power/Other	
VSS	D2	Power/Other	
VSS	D5	Power/Other	
VSS	D11	Power/Other	
VSS	D21	Power/Other	
VSS	D27	Power/Other	
VSS	D28	Power/Other	
VSS	D30	Power/Other	
VSS	E9	Power/Other	
VSS	E15	Power/Other	
VSS	E17	Power/Other	

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	E23	Power/Other	
VSS	E29	Power/Other	
VSS	E31	Power/Other	
VSS	F2	Power/Other	
VSS	F7	Power/Other	
VSS	F13	Power/Other	
VSS	F19	Power/Other	
VSS	F25	Power/Other	
VSS	F28	Power/Other	
VSS	F30	Power/Other	
VSS	G1	Power/Other	
VSS	G3	Power/Other	
VSS	G5	Power/Other	
VSS	G9	Power/Other	
VSS	G25	Power/Other	
VSS	G27	Power/Other	
VSS	G29	Power/Other	
VSS	G31	Power/Other	
VSS	H2	Power/Other	
VSS	H4	Power/Other	
VSS	H6	Power/Other	
VSS	H8	Power/Other	
VSS	H24	Power/Other	
VSS	H26	Power/Other	
VSS	H28	Power/Other	
VSS	H30	Power/Other	
VSS	J1	Power/Other	
VSS	J3	Power/Other	
VSS	J5	Power/Other	
VSS	J7	Power/Other	
VSS	J9	Power/Other	
VSS	J23	Power/Other	
VSS	J25	Power/Other	
VSS	J27	Power/Other	
VSS	J29	Power/Other	
VSS	J31	Power/Other	
VSS	K2	Power/Other	
VSS	K4	Power/Other	

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	K6	Power/Other	
VSS	K8	Power/Other	
VSS	K24	Power/Other	
VSS	K26	Power/Other	
VSS	K28	Power/Other	
VSS	K30	Power/Other	
VSS	L1	Power/Other	
VSS	L3	Power/Other	
VSS	L5	Power/Other	
VSS	L7	Power/Other	
VSS	L9	Power/Other	
VSS	L23	Power/Other	
VSS	L25	Power/Other	
VSS	L27	Power/Other	
VSS	L29	Power/Other	
VSS	L31	Power/Other	
VSS	M2	Power/Other	
VSS	M4	Power/Other	
VSS	M6	Power/Other	
VSS	M8	Power/Other	
VSS	M24	Power/Other	
VSS	M26	Power/Other	
VSS	M28	Power/Other	
VSS	M30	Power/Other	
VSS	N2	Power/Other	
VSS	N4	Power/Other	
VSS	N6	Power/Other	
VSS	N8	Power/Other	
VSS	N24	Power/Other	
VSS	N26	Power/Other	
VSS	N28	Power/Other	
VSS	N30	Power/Other	
VSS	P1	Power/Other	
VSS	P3	Power/Other	
VSS	P5	Power/Other	
VSS	P7	Power/Other	
VSS	P9	Power/Other	
VSS	P23	Power/Other	

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	P25	Power/Other	
VSS	P27	Power/Other	
VSS	P29	Power/Other	
VSS	P31	Power/Other	
VSS	R2	Power/Other	
VSS	R4	Power/Other	
VSS	R6	Power/Other	
VSS	R8	Power/Other	
VSS	R24	Power/Other	
VSS	R26	Power/Other	
VSS	R28	Power/Other	
VSS	R30	Power/Other	
VSS	T1	Power/Other	
VSS	T3	Power/Other	
VSS	T5	Power/Other	
VSS	T7	Power/Other	
VSS	T9	Power/Other	
VSS	T23	Power/Other	
VSS	T25	Power/Other	
VSS	T27	Power/Other	
VSS	T29	Power/Other	
VSS	T31	Power/Other	
VSS	U2	Power/Other	
VSS	U4	Power/Other	
VSS	U6	Power/Other	
VSS	U8	Power/Other	
VSS	U24	Power/Other	
VSS	U26	Power/Other	
VSS	U28	Power/Other	
VSS	U30	Power/Other	
VSS	V1	Power/Other	
VSS	V3	Power/Other	
VSS	V5	Power/Other	
VSS	V7	Power/Other	
VSS	V9	Power/Other	
VSS	V23	Power/Other	
VSS	V25	Power/Other	
VSS	V27	Power/Other	

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	V29	Power/Other	
VSS	V31	Power/Other	
VSS	W2	Power/Other	
VSS	W4	Power/Other	
VSS	W24	Power/Other	
VSS	W26	Power/Other	
VSS	W28	Power/Other	
VSS	W30	Power/Other	
VSS	Y1	Power/Other	
VSS	Y5	Power/Other	
VSS	Y7	Power/Other	
VSS	Y13	Power/Other	
VSS	Y19	Power/Other	
VSS	Y25	Power/Other	
VSS	Y31	Power/Other	
VSS	AA2	Power/Other	
VSS	AA9	Power/Other	
VSS	AA15	Power/Other	
VSS	AA17	Power/Other	
VSS	AA23	Power/Other	
VSS	AA30	Power/Other	
VSS	AB1	Power/Other	
VSS	AB5	Power/Other	
VSS	AB11	Power/Other	
VSS	AB21	Power/Other	
VSS	AB27	Power/Other	
VSS	AB31	Power/Other	
VSS	AC2	Power/Other	
VSS	AC7	Power/Other	
VSS	AC13	Power/Other	
VSS	AC19	Power/Other	
VSS	AC25	Power/Other	
VSS	AD3	Power/Other	
VSS	AD9	Power/Other	
VSS	AD15	Power/Other	
VSS	AD17	Power/Other	
VSS	AD23	Power/Other	
VSS	AD31	Power/Other	

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	AE2	Power/Other	
VSS	AE11	Power/Other	
VSS	AE21	Power/Other	
VSS	AE27	Power/Other	
VSSA	AA5	Power/Other	Input
VSSSENSE	D26	Power/Other	Output
VTT	A4	Power/Other	
VTT	B4	Power/Other	
VTT	C5	Power/Other	

Table 5-1. Pin Listing by Pin Name (Cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
VTT	B12	Power/Other	
VTT	C10	Power/Other	
VTT	E12	Power/Other	
VTT	F10	Power/Other	
VTT	Y10	Power/Other	
VTT	AA12	Power/Other	
VTT	AC10	Power/Other	
VTT	AD12	Power/Other	
VTTEN	E1	Power/Other	Output

5.1.2 Pin Listing by Pin Number

Table 5-2. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
A1	VID5	Power/Other	Output
A2	VCC	Power/Other	
A3	SKTOCC#	Power/Other	Output
A4	VTT	Power/Other	
A5	VSS	Power/Other	
A6	A32#	Source Sync	Input/Output
A7	A33#	Source Sync	Input/Output
A8	VCC	Power/Other	
A9	A26#	Source Sync	Input/Output
A10	A20#	Source Sync	Input/Output
A11	VSS	Power/Other	
A12	A14#	Source Sync	Input/Output
A13	A10#	Source Sync	Input/Output
A14	VCC	Power/Other	
A15	FORCEPR#	Async GTL+	Input
A16	TEST_BUS	Power/Other	Input
A17	LOCK#	Common Clk	Input/Output
A18	VCC	Power/Other	
A19	A7#	Source Sync	Input/Output
A20	A4#	Source Sync	Input/Output
A21	VSS	Power/Other	
A22	A3#	Source Sync	Input/Output
A23	HITM#	Common Clk	Input/Output
A24	VCC	Power/Other	
A25	TMS	TAP	Input
A26	Reserved	Reserved	Reserved
A27	VSS	Power/Other	
A28	VCC	Power/Other	
A29	VSS	Power/Other	
A30	VCC	Power/Other	
A31	VSS	Power/Other	
B1	VIDPWRGD	Power/Other	Input
B2	VSS	Power/Other	
B3	VID4	Power/Other	Output
B4	VTT	Power/Other	
B5	ODTEN	Power/Other	Input

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
B6	VCC	Power/Other	
B7	A31#	Source Sync	Input/Output
B8	A27#	Source Sync	Input/Output
B9	VSS	Power/Other	
B10	A21#	Source Sync	Input/Output
B11	A22#	Source Sync	Input/Output
B12	VTT	Power/Other	
B13	A13#	Source Sync	Input/Output
B14	A12#	Source Sync	Input/Output
B15	VSS	Power/Other	
B16	A11#	Source Sync	Input/Output
B17	VSS	Power/Other	
B18	A5#	Source Sync	Input/Output
B19	REQ0#	Source Sync	Input/Output
B20	VCC	Power/Other	
B21	REQ1#	Source Sync	Input/Output
B22	REQ4#	Source Sync	Input/Output
B23	VSS	Power/Other	
B24	LINT0/INTR	Async GTL+	Input
B25	PROCHOT#	Power/Other	Output
B26	VCC	Power/Other	
B27	VCCSENSE	Power/Other	Output
B28	VSS	Power/Other	
B29	VCC	Power/Other	
B30	VSS	Power/Other	
B31	VCC	Power/Other	
C1	OPTIMIZED/ COMPAT#	Power/Other	Input
C2	VCC	Power/Other	
C3	VID3	Power/Other	Output
C4	VCC	Power/Other	
C5	VTT	Power/Other	
C6	RSP#	Common Clk	Input
C7	VSS	Power/Other	
C8	A35#	Source Sync	Input/Output
C9	A34#	Source Sync	Input/Output
C10	VTT	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
C11	A30#	Source Sync	Input/Output
C12	A23#	Source Sync	Input/Output
C13	VSS	Power/Other	
C14	A16#	Source Sync	Input/Output
C15	A15#	Source Sync	Input/Output
C16	VCC	Power/Other	
C17	A8#	Source Sync	Input/Output
C18	A6#	Source Sync	Input/Output
C19	VSS	Power/Other	
C20	REQ3#	Source Sync	Input/Output
C21	REQ2#	Source Sync	Input/Output
C22	VCC	Power/Other	
C23	DEFER#	Common Clk	Input
C24	TDI	TAP	Input
C25	VSS	Power/Other	
C26	IGNNE#	Async GTL+	Input
C27	SMI#	Async GTL+	Input
C28	VCC	Power/Other	
C29	VSS	Power/Other	
C30	VCC	Power/Other	
C31	VSS	Power/Other	
D1	VCC	Power/Other	
D2	VSS	Power/Other	
D3	VID2	Power/Other	Output
D4	STPCLK#	Async GTL+	Input
D5	VSS	Power/Other	
D6	INIT#	Async GTL+	Input
D7	MCERR#	Common Clk	Input/Output
D8	VCC	Power/Other	
D9	AP1#	Common Clk	Input/Output
D10	BR3#	Common Clk	Input
D11	VSS	Power/Other	
D12	A29#	Source Sync	Input/Output
D13	A25#	Source Sync	Input/Output
D14	VCC	Power/Other	
D15	A18#	Source Sync	Input/Output
D16	A17#	Source Sync	Input/Output
D17	A9#	Source Sync	Input/Output

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
D18	VCC	Power/Other	
D19	ADS#	Common Clk	Input/Output
D20	BR0#	Common Clk	Input/Output
D21	VSS	Power/Other	
D22	RS1#	Common Clk	Input
D23	BPRI#	Common Clk	Input
D24	VCC	Power/Other	
D25	Reserved	Reserved	Reserved
D26	VSSSENSE	Power/Other	Output
D27	VSS	Power/Other	
D28	VSS	Power/Other	
D29	VCC	Power/Other	
D30	VSS	Power/Other	
D31	VCC	Power/Other	
E1	VTTEN	Power/Other	Output
E2	VCC	Power/Other	
E3	VID1	Power/Other	Output
E4	BPM5#	Common Clk	Input/Output
E5	IERR#	Async GTL+	Output
E6	VCC	Power/Other	
E7	BPM2#	Common Clk	Input/Output
E8	BPM4#	Common Clk	Input/Output
E9	VSS	Power/Other	
E10	AP0#	Common Clk	Input/Output
E11	BR2#	Common Clk	Input
E12	VTT	Power/Other	
E13	A28#	Source Sync	Input/Output
E14	A24#	Source Sync	Input/Output
E15	VSS	Power/Other	
E17	VSS	Power/Other	
E18	DRDY#	Common Clk	Input/Output
E19	TRDY#	Common Clk	Input
E20	VCC	Power/Other	
E21	RS0#	Common Clk	Input
E22	HIT#	Common Clk	Input/Output
E23	VSS	Power/Other	
E24	TCK	TAP	Input
E25	TDO	TAP	Output

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
E26	VCC	Power/Other	
E27	FERR#/PBE#	Async GTL+	Output
E28	VCC	Power/Other	
E29	VSS	Power/Other	
E30	VCC	Power/Other	
E31	VSS	Power/Other	
F1	VCC	Power/Other	
F2	VSS	Power/Other	
F3	VID0	Power/Other	Output
F4	VCC	Power/Other	
F5	BPM3#	Common Clk	Input/Output
F6	BPM0#	Common Clk	Input/Output
F7	VSS	Power/Other	
F8	BPM1#	Common Clk	Input/Output
F9	GTLREF	Power/Other	Input
F10	VTT	Power/Other	
F11	BINIT#	Common Clk	Input/Output
F12	BR1#	Common Clk	Input
F13	VSS	Power/Other	
F14	ADSTB1#	Source Sync	Input/Output
F15	A19#	Source Sync	Input/Output
F16	VCC	Power/Other	
F17	ADSTB0#	Source Sync	Input/Output
F18	DBSY#	Common Clk	Input/Output
F19	VSS	Power/Other	
F20	BNR#	Common Clk	Input/Output
F21	RS2#	Common Clk	Input
F22	VCC	Power/Other	
F23	GTLREF	Power/Other	Input
F24	TRST#	TAP	Input
F25	VSS	Power/Other	
F26	THERMTRIP#	Async GTL+	Output
F27	A20M#	Async GTL+	Input
F28	VSS	Power/Other	
F29	VCC	Power/Other	
F30	VSS	Power/Other	
F31	VCC	Power/Other	
G1	VSS	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
G2	VCC	Power/Other	
G3	VSS	Power/Other	
G4	VCC	Power/Other	
G5	VSS	Power/Other	
G6	VCC	Power/Other	
G7	BOOT_SELECT	Power/Other	Input
G8	VCC	Power/Other	
G9	VSS	Power/Other	
G23	LINT1/NMI	Async GTL+	Input
G24	VCC	Power/Other	
G25	VSS	Power/Other	
G26	VCC	Power/Other	
G27	VSS	Power/Other	
G28	VCC	Power/Other	
G29	VSS	Power/Other	
G30	VCC	Power/Other	
G31	VSS	Power/Other	
H1	VCC	Power/Other	
H2	VSS	Power/Other	
H3	VCC	Power/Other	
H4	VSS	Power/Other	
H5	VCC	Power/Other	
H6	VSS	Power/Other	
H7	VCC	Power/Other	
H8	VSS	Power/Other	
H9	VCC	Power/Other	
H23	VCC	Power/Other	
H24	VSS	Power/Other	
H25	VCC	Power/Other	
H26	VSS	Power/Other	
H27	VCC	Power/Other	
H28	VSS	Power/Other	
H29	VCC	Power/Other	
H30	VSS	Power/Other	
H31	VCC	Power/Other	
J1	VSS	Power/Other	
J2	VCC	Power/Other	
J3	VSS	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
J4	VCC	Power/Other	
J5	VSS	Power/Other	
J6	VCC	Power/Other	
J7	VSS	Power/Other	
J8	VCC	Power/Other	
J9	VSS	Power/Other	
J23	VSS	Power/Other	
J24	VCC	Power/Other	
J25	VSS	Power/Other	
J26	VCC	Power/Other	
J27	VSS	Power/Other	
J28	VCC	Power/Other	
J29	VSS	Power/Other	
J30	VCC	Power/Other	
J31	VSS	Power/Other	
K1	VCC	Power/Other	
K2	VSS	Power/Other	
K3	VCC	Power/Other	
K4	VSS	Power/Other	
K5	VCC	Power/Other	
K6	VSS	Power/Other	
K7	VCC	Power/Other	
K8	VSS	Power/Other	
K9	VCC	Power/Other	
K23	VCC	Power/Other	
K24	VSS	Power/Other	
K25	VCC	Power/Other	
K26	VSS	Power/Other	
K27	VCC	Power/Other	
K28	VSS	Power/Other	
K29	VCC	Power/Other	
K30	VSS	Power/Other	
K31	VCC	Power/Other	
L1	VSS	Power/Other	
L2	VCC	Power/Other	
L3	VSS	Power/Other	
L4	VCC	Power/Other	
L5	VSS	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
L6	VCC	Power/Other	
L7	VSS	Power/Other	
L8	VCC	Power/Other	
L9	VSS	Power/Other	
L23	VSS	Power/Other	
L24	VCC	Power/Other	
L25	VSS	Power/Other	
L26	VCC	Power/Other	
L27	VSS	Power/Other	
L28	VCC	Power/Other	
L29	VSS	Power/Other	
L30	VCC	Power/Other	
L31	VSS	Power/Other	
M1	VCC	Power/Other	
M2	VSS	Power/Other	
M3	VCC	Power/Other	
M4	VSS	Power/Other	
M5	VCC	Power/Other	
M6	VSS	Power/Other	
M7	VCC	Power/Other	
M8	VSS	Power/Other	
M9	VCC	Power/Other	
M23	VCC	Power/Other	
M24	VSS	Power/Other	
M25	VCC	Power/Other	
M26	VSS	Power/Other	
M27	VCC	Power/Other	
M28	VSS	Power/Other	
M29	VCC	Power/Other	
M30	VSS	Power/Other	
M31	VCC	Power/Other	
N1	VCC	Power/Other	
N2	VSS	Power/Other	
N3	VCC	Power/Other	
N4	VSS	Power/Other	
N5	VCC	Power/Other	
N6	VSS	Power/Other	
N7	VCC	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
N8	VSS	Power/Other	
N9	VCC	Power/Other	
N23	VCC	Power/Other	
N24	VSS	Power/Other	
N25	VCC	Power/Other	
N26	VSS	Power/Other	
N27	VCC	Power/Other	
N28	VSS	Power/Other	
N29	VCC	Power/Other	
N30	VSS	Power/Other	
N31	VCC	Power/Other	
P1	VSS	Power/Other	
P2	VCC	Power/Other	
P3	VSS	Power/Other	
P4	VCC	Power/Other	
P5	VSS	Power/Other	
P6	VCC	Power/Other	
P7	VSS	Power/Other	
P8	VCC	Power/Other	
P9	VSS	Power/Other	
P23	VSS	Power/Other	
P24	VCC	Power/Other	
P25	VSS	Power/Other	
P26	VCC	Power/Other	
P27	VSS	Power/Other	
P28	VCC	Power/Other	
P29	VSS	Power/Other	
P30	VCC	Power/Other	
P31	VSS	Power/Other	
R1	VCC	Power/Other	
R2	VSS	Power/Other	
R3	VCC	Power/Other	
R4	VSS	Power/Other	
R5	VCC	Power/Other	
R6	VSS	Power/Other	
R7	VCC	Power/Other	
R8	VSS	Power/Other	
R9	VCC	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
R23	VCC	Power/Other	
R24	VSS	Power/Other	
R25	VCC	Power/Other	
R26	VSS	Power/Other	
R27	VCC	Power/Other	
R28	VSS	Power/Other	
R29	VCC	Power/Other	
R30	VSS	Power/Other	
R31	VCC	Power/Other	
T1	VSS	Power/Other	
T2	VCC	Power/Other	
T3	VSS	Power/Other	
T4	VCC	Power/Other	
T5	VSS	Power/Other	
T6	VCC	Power/Other	
T7	VSS	Power/Other	
T8	VCC	Power/Other	
T9	VSS	Power/Other	
T23	VSS	Power/Other	
T24	VCC	Power/Other	
T25	VSS	Power/Other	
T26	VCC	Power/Other	
T27	VSS	Power/Other	
T28	VCC	Power/Other	
T29	VSS	Power/Other	
T30	VCC	Power/Other	
T31	VSS	Power/Other	
U1	VCC	Power/Other	
U2	VSS	Power/Other	
U3	VCC	Power/Other	
U4	VSS	Power/Other	
U5	VCC	Power/Other	
U6	VSS	Power/Other	
U7	VCC	Power/Other	
U8	VSS	Power/Other	
U9	VCC	Power/Other	
U23	VCC	Power/Other	
U24	VSS	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
U25	VCC	Power/Other	
U26	VSS	Power/Other	
U27	VCC	Power/Other	
U28	VSS	Power/Other	
U29	VCC	Power/Other	
U30	VSS	Power/Other	
U31	VCC	Power/Other	
V1	VSS	Power/Other	
V2	VCC	Power/Other	
V3	VSS	Power/Other	
V4	VCC	Power/Other	
V5	VSS	Power/Other	
V6	VCC	Power/Other	
V7	VSS	Power/Other	
V8	VCC	Power/Other	
V9	VSS	Power/Other	
V23	VSS	Power/Other	
V24	VCC	Power/Other	
V25	VSS	Power/Other	
V26	VCC	Power/Other	
V27	VSS	Power/Other	
V28	VCC	Power/Other	
V29	VSS	Power/Other	
V30	VCC	Power/Other	
V31	VSS	Power/Other	
W1	VCC	Power/Other	
W2	VSS	Power/Other	
W3	Reserved	Reserved	Reserved
W4	VSS	Power/Other	
W5	BCLK1	Sys Bus Clk	Input
W6	TESTHI0	Power/Other	Input
W7	TESTHI1	Power/Other	Input
W8	TESTHI2	Power/Other	Input
W9	GTLREF	Power/Other	Input
W23	GTLREF	Power/Other	Input
W24	VSS	Power/Other	
W25	VCC	Power/Other	
W26	VSS	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
W27	VCC	Power/Other	
W28	VSS	Power/Other	
W29	VCC	Power/Other	
W30	VSS	Power/Other	
W31	VCC	Power/Other	
Y1	VSS	Power/Other	
Y2	VCC	Power/Other	
Y3	Reserved	Reserved	Reserved
Y4	BCLK0	Sys Bus Clk	Input
Y5	VSS	Power/Other	
Y6	TESTHI3	Power/Other	Input
Y7	VSS	Power/Other	
Y8	RESET#	Common Clk	Input
Y9	D62#	Source Sync	Input/Output
Y10	VTT	Power/Other	
Y11	DSTBP3#	Source Sync	Input/Output
Y12	DSTBN3#	Source Sync	Input/Output
Y13	VSS	Power/Other	
Y14	DSTBP2#	Source Sync	Input/Output
Y15	DSTBN2#	Source Sync	Input/Output
Y16	VCC	Power/Other	
Y17	DSTBP1#	Source Sync	Input/Output
Y18	DSTBN1#	Source Sync	Input/Output
Y19	VSS	Power/Other	
Y20	DSTBP0#	Source Sync	Input/Output
Y21	DSTBN0#	Source Sync	Input/Output
Y22	VCC	Power/Other	
Y23	D5#	Source Sync	Input/Output
Y24	D2#	Source Sync	Input/Output
Y25	VSS	Power/Other	
Y26	D0#	Source Sync	Input/Output
Y27	THERMDA	Power/Other	Output
Y28	THERMDC	Power/Other	Output
Y29	N/C	N/C	N/C
Y30	VCC	Power/Other	
Y31	VSS	Power/Other	
AA1	VCC	Power/Other	
AA2	VSS	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
AA3	BSEL0	Power/Other	Output
AA4	VCC	Power/Other	
AA5	VSSA	Power/Other	Input
AA6	VCC	Power/Other	
AA7	TESTHI4	Power/Other	Input
AA8	D61#	Source Sync	Input/Output
AA9	VSS	Power/Other	
AA10	D54#	Source Sync	Input/Output
AA11	D53#	Source Sync	Input/Output
AA12	VTT	Power/Other	
AA13	D48#	Source Sync	Input/Output
AA14	D49#	Source Sync	Input/Output
AA15	VSS	Power/Other	
AA16	D33#	Source Sync	Input/Output
AA17	VSS	Power/Other	
AA18	D24#	Source Sync	Input/Output
AA19	D15#	Source Sync	Input/Output
AA20	VCC	Power/Other	
AA21	D11#	Source Sync	Input/Output
AA22	D10#	Source Sync	Input/Output
AA23	VSS	Power/Other	
AA24	D6#	Source Sync	Input/Output
AA25	D3#	Source Sync	Input/Output
AA26	VCC	Power/Other	
AA27	D1#	Source Sync	Input/Output
AA28	N/C	N/C	N/C
AA29	N/C	N/C	N/C
AA30	VSS	Power/Other	
AA31	VCC	Power/Other	
AB1	VSS	Power/Other	
AB2	VCC	Power/Other	
AB3	BSEL1	Power/Other	Output
AB4	VCCA	Power/Other	Input
AB5	VSS	Power/Other	
AB6	D63#	Source Sync	Input/Output
AB7	PWRGOOD	Async GTL+	Input
AB8	VCC	Power/Other	
AB9	DBI3#	Source Sync	Input/Output

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
AB10	D55#	Source Sync	Input/Output
AB11	VSS	Power/Other	
AB12	D51#	Source Sync	Input/Output
AB13	D52#	Source Sync	Input/Output
AB14	VCC	Power/Other	
AB15	D37#	Source Sync	Input/Output
AB16	D32#	Source Sync	Input/Output
AB17	D31#	Source Sync	Input/Output
AB18	VCC	Power/Other	
AB19	D14#	Source Sync	Input/Output
AB20	D12#	Source Sync	Input/Output
AB21	VSS	Power/Other	
AB22	D13#	Source Sync	Input/Output
AB23	D9#	Source Sync	Input/Output
AB24	VCC	Power/Other	
AB25	D8#	Source Sync	Input/Output
AB26	D7#	Source Sync	Input/Output
AB27	VSS	Power/Other	
AB28	N/C	N/C	N/C
AB29	N/C	N/C	N/C
AB30	VCC	Power/Other	
AB31	VSS	Power/Other	
AC1	Reserved	Reserved	Reserved
AC2	VSS	Power/Other	
AC3	VCC	Power/Other	
AC4	VCC	Power/Other	
AC5	D60#	Source Sync	Input/Output
AC6	D59#	Source Sync	Input/Output
AC7	VSS	Power/Other	
AC8	D56#	Source Sync	Input/Output
AC9	D47#	Source Sync	Input/Output
AC10	VTT	Power/Other	
AC11	D43#	Source Sync	Input/Output
AC12	D41#	Source Sync	Input/Output
AC13	VSS	Power/Other	
AC14	D50#	Source Sync	Input/Output
AC15	DP2#	Common Clk	Input/Output
AC16	VCC	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
AC17	D34#	Source Sync	Input/Output
AC18	DP0#	Common Clk	Input/Output
AC19	VSS	Power/Other	
AC20	D25#	Source Sync	Input/Output
AC21	D26#	Source Sync	Input/Output
AC22	VCC	Power/Other	
AC23	D23#	Source Sync	Input/Output
AC24	D20#	Source Sync	Input/Output
AC25	VSS	Power/Other	
AC26	D17#	Source Sync	Input/Output
AC27	DBI0#	Source Sync	Input/Output
AC28	N/C	N/C	N/C
AC29	N/C	N/C	N/C
AC30	SLEW_CTRL	Power/Other	Input
AC31	VCC	Power/Other	
AD1	VCCPLL	Power/Other	Input
AD2	VCC	Power/Other	
AD3	VSS	Power/Other	
AD4	VCCIOPLL	Power/Other	Input
AD5	TESTHI5	Power/Other	Input
AD6	VCC	Power/Other	
AD7	D57#	Source Sync	Input/Output
AD8	D46#	Source Sync	Input/Output
AD9	VSS	Power/Other	
AD10	D45#	Source Sync	Input/Output
AD11	D40#	Source Sync	Input/Output
AD12	VTT	Power/Other	
AD13	D38#	Source Sync	Input/Output
AD14	D39#	Source Sync	Input/Output
AD15	VSS	Power/Other	
AD16	COMP0	Power/Other	Input
AD17	VSS	Power/Other	
AD18	D36#	Source Sync	Input/Output
AD19	D30#	Source Sync	Input/Output
AD20	VCC	Power/Other	
AD21	D29#	Source Sync	Input/Output
AD22	DBI1#	Source Sync	Input/Output
AD23	VSS	Power/Other	

Table 5-2. Pin Listing by Pin Number (Cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
AD24	D21#	Source Sync	Input/Output
AD25	D18#	Source Sync	Input/Output
AD26	VCC	Power/Other	
AD27	D4#	Source Sync	Input/Output
AD28	N/C	N/C	N/C
AD29	N/C	N/C	N/C
AD30	VCC	Power/Other	
AD31	VSS	Power/Other	
AE2	VSS	Power/Other	
AE3	VCC	Power/Other	
AE4	SMB_PRT	Power/Other	Output
AE5	TESTHI6	Power/Other	Input
AE6	SLP#	Async GTL+	Input
AE7	D58#	Source Sync	Input/Output
AE8	VCC	Power/Other	
AE9	D44#	Source Sync	Input/Output
AE10	D42#	Source Sync	Input/Output
AE11	VSS	Power/Other	
AE12	DBI2#	Source Sync	Input/Output
AE13	D35#	Source Sync	Input/Output
AE14	VCC	Power/Other	
AE15	Reserved	Reserved	Reserved
AE16	Reserved	Reserved	Reserved
AE17	DP3#	Common Clk	Input/Output
AE18	VCC	Power/Other	
AE19	DP1#	Common Clk	Input/Output
AE20	D28#	Source Sync	Input/Output
AE21	VSS	Power/Other	
AE22	D27#	Source Sync	Input/Output
AE23	D22#	Source Sync	Input/Output
AE24	VCC	Power/Other	
AE25	D19#	Source Sync	Input/Output
AE26	D16#	Source Sync	Input/Output
AE27	VSS	Power/Other	
AE28	Reserved	Reserved	Reserved
AE29	Reserved	Reserved	Reserved
AE30	N/C	N/C	N/C

§

6 Thermal Specifications

6.1 Package Thermal Specifications

The Dual-Core Intel Xeon processor requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor Integrated Heat Spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

For more information on designing a component level thermal solution, refer to the *Dual-Core Intel® Xeon® Processor 2.80 GHz Thermal/Mechanical Design Guidelines*.

Note: The boxed processor will ship with a component thermal solution.

6.1.1 Thermal Specifications

To allow the optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum case temperature (T_{CASE}) specifications as defined by the applicable thermal profile (see Figure 6-1, Table 6-2 and Table 6-3). Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, please refer to the appropriate processor thermal/mechanical design guideline.

The Dual-Core Intel Xeon processor utilizes a methodology for managing processor temperatures which is intended to support acoustic noise reduction through fan speed control and assure processor reliability. Selection of the appropriate fan speed will be based on the temperature reported by the processor's Thermal Diode. If the diode temperature is greater than or equal to Tcontrol (see Section 6.2.6), then the processor case temperature must remain at or below the temperature as specified by the thermal profile (see Figure 6-1). If the diode temperature is less than Tcontrol, then the case temperature is permitted to exceed the thermal profile, but the diode temperature must remain at or below Tcontrol. Systems that implement fan speed control must be designed to take these conditions into account. Systems that do not alter the fan speed only need to guarantee the case temperature meets the thermal profile specifications.

Intel has developed two thermal profiles, either of which can be implemented with the Dual-Core Intel Xeon processor. Both ensure adherence to Intel reliability requirements. Thermal Profile A is representative of a volumetrically unconstrained thermal solution (i.e. industry enabled 2U heat sink). In this scenario, it is expected that the Thermal Control Circuit (TCC) would only be activated for very brief periods of time when running the most power intensive applications. Thermal Profile B is indicative of a constrained thermal environment (i.e. 1U). Because of the reduced cooling capability represented by this thermal solution, the probability of TCC activation and performance loss is increased. Additionally, utilization of a thermal solution that does not meet Thermal Profile B will violate the thermal specifications and may result in permanent damage to

the processor. Intel has developed these thermal profiles to allow OEMs to choose the thermal solution and environmental parameters that best suit their platform implementation. Refer to the appropriate thermal/mechanical design guide for details on system thermal solution design, thermal profiles, and environmental considerations.

The upper point of the thermal profile consists of the Thermal Design Power (TDP) defined in Table 6-1 and the associated T_{CASE} value. It should be noted that the upper point associated with Thermal Profile B (x = TDP and y = $T_{CASE\_MAX\_B}$ @ TDP) represents a thermal solution design point. In actuality the processor case temperature will never reach this value due to TCC activation (see Figure 6-1). The lower point of the thermal profile consists of x = $P_{CONTROL\_BASE}$ and y = T_{CASE_MAX} @ $P_{CONTROL\_BASE}$. Pcontrol is defined as the processor power at which T_{CASE}, calculated from the thermal profile, corresponds to the lowest possible value of Tcontrol. This point is associated with the Tcontrol value (see Section 6.2.6) However, because Tcontrol represents a diode temperature, it is necessary to define the associated case temperature. This is T_{CASE_MAX} @ $P_{CONTROL\_BASE}$. Please see Section 6.2.6 and the appropriate thermal/mechanical design guide for proper usage of the Tcontrol specification.

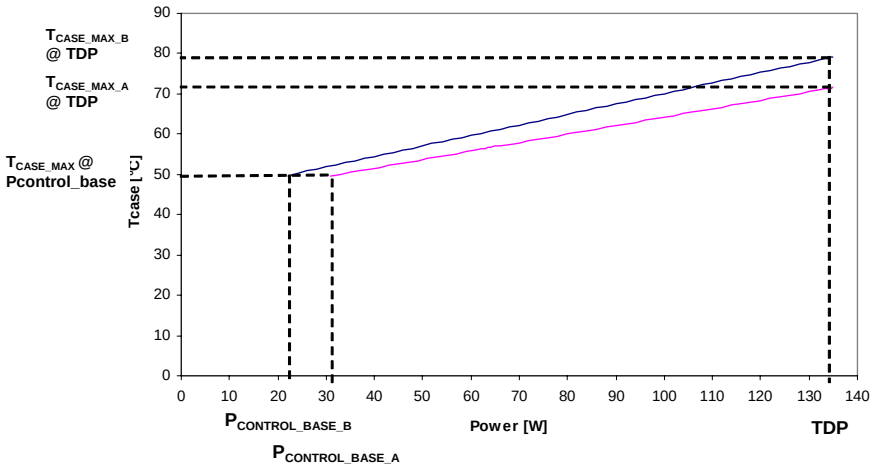
The case temperature is defined at the geometric top center of the processor IHS. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 6-1, instead of the maximum processor power consumption. The Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. For more details on this feature, refer to Section 6.2. **Thermal Monitor feature must be enabled for the processor to remain within specification.**

Table 6-1. Dual-Core Intel® Xeon® Processor Thermal Specifications

Core Frequency (GHz)	Maximum Power (W)	Thermal Design Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)	Notes
2.80 GHz	150	135	5	See Figure 6-1; Table 6-2 or Table 6-3	1, 2, 3, 4, 5, 6

NOTES:
1. These values are specified at V_{CC_MAX} for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to the V_{CC} static and transient tolerance specifications in Section 2.
2. Listed frequencies are not necessarily committed production frequencies.
3. Maximum Power is the maximum thermal power that can be dissipated by the processor through the integrated heat spreader (IHS). Maximum Power is measured at maximum T_{CASE}.
4. Thermal Design Power (TDP) should be used for processor/chipset thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
5. These specifications are based on final silicon characterization.
6. Power specifications are defined at all VIDs found in Table 2-7. The Dual-Core Intel Xeon processor may be shipped under multiple VIDs listed for each frequency.

Figure 6-1. Dual-Core Intel® Xeon® Processor Thermal Profiles A and B



NOTES:

1. Thermal Profile A is representative of a volumetrically unconstrained platform. Please refer to Table 6-2 for discrete points that constitute the thermal profile.
2. Implementation of Thermal Profile A should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet processor Thermal Profile A will result in increased probability of TCC activation and may incur measurable performance loss. (See Section 6.2 for details on TCC activation).
3. Thermal Profile B is representative of a volumetrically constrained platform. Please refer to Table 6-2 for discrete points that constitute the thermal profile.
4. Implementation of Thermal Profile B will result in increased probability of TCC activation and may incur measurable performance loss. Furthermore, utilization of thermal solutions that do not meet Thermal Profile B do not meet the processor's thermal specifications and may result in permanent damage to the processor.
5. Refer to the *Dual-Core Intel® Xeon® Processor 2.80 GHz Thermal/Mechanical Design Guidelines* for system and environmental implementation details.

Table 6-2. Dual-Core Intel® Xeon® Processor Thermal Profile A

Power [W]	T_{CASE_MAX} [deg C]		Power [W]	T_{CASE_MAX} [deg C]
$P_{CONTROL\_BASE\_A}$ = 31	43		82	60
32	50		84	61
34	50		86	61
36	51		88	62
38	51		90	62
40	52		92	63
42	52		94	63
44	52		96	63
46	53		98	64
48	53		100	64
50	54		102	65
52	54		104	65
54	54		106	65
56	55		108	66
58	55		110	66
60	56		112	67
62	56		114	67
64	57		116	68
66	57		118	68
64	57		120	68
66	57		122	69
68	57		124	69
70	58		126	70
72	58		128	70
74	59		130	71
76	59		132	71
78	60		134	71
80	60		135	72

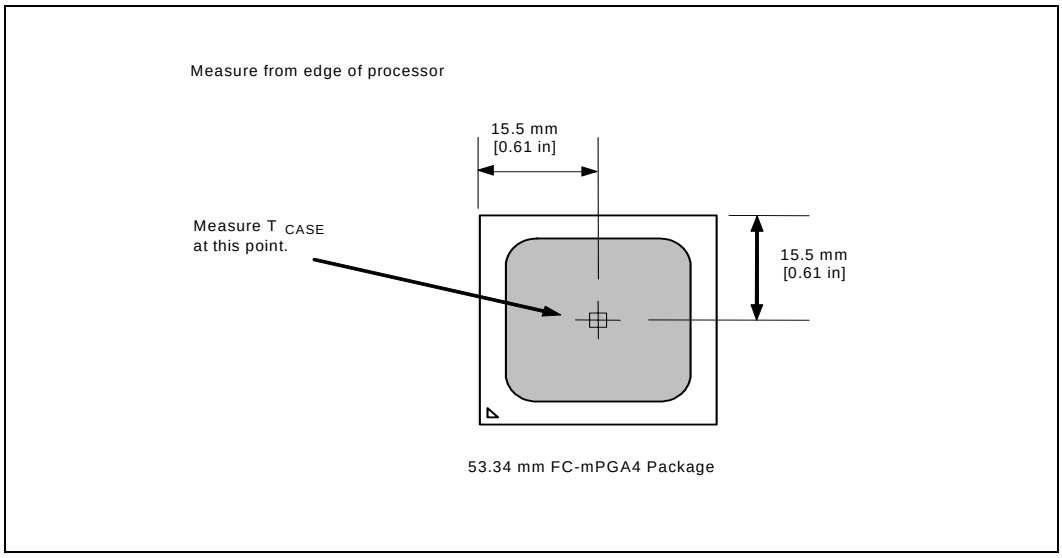
Table 6-3. Dual-Core Intel® Xeon® Processor Thermal Profile B

Power [W]	T_{CASE_MAX} [deg C]		Power [W]	T_{CASE_MAX} [deg C]
$P_{CONTROL\_BASE\_B}$ = 22	44		80	65
24	50		82	65
26	51		84	66
28	51		86	66
30	52		88	67
32	52		90	67
34	53		92	68
36	53		94	69
38	54		96	69
40	54		98	70
42	55		100	70
44	55		102	71
46	56		104	71
48	57		106	72
50	57		108	72
52	58		110	73
54	58		112	73
56	59		114	74
58	59		116	74
60	60		118	75
62	60		120	75
64	61		122	76
66	61		124	76
68	62		126	77
70	62		128	77
72	63		130	78
74	63		132	78
76	64		134	79
78	64		135	79

6.1.2 Thermal Metrology

The maximum case temperatures (T_{CASE}) are specified in Table 6-2 and Table 6-3 measured at the geometric top center of the processor integrated heat spreader (IHS). Figure 6-2 illustrates the location where T_{CASE} temperature measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the appropriate thermal/mechanical design guide.

Figure 6-2. Case Temperature (T_{CASE}) Measurement Location



Note: Figure is not to scale and is for reference only.

6.2 Processor Thermal Features

6.2.1 Thermal Monitor

The Thermal Monitor feature helps control the processor temperature by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption as needed by modulating (starting and stopping) the internal processor core clocks. The Thermal Monitor feature must be enabled for the processor to be operating within specifications. The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor is enabled, and a high temperature situation exists (i.e. TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30 -50%). Clocks will not be off for more than 3 microseconds when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/ inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a thermal solution designed to meet Thermal Profile A, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. A thermal solution that is designed to Thermal Profile B may cause a noticeable performance loss due to increased TCC activation. Thermal Solutions that exceed Thermal Profile B will exceed the maximum temperature specification and affect the long-term reliability of the processor. In addition, a thermal solution

that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the appropriate thermal/mechanical design guide for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

6.2.2 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as “On-Demand” mode and is distinct from the Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems utilizing the Dual-Core Intel Xeon processor must not rely on software usage of this mechanism to limit the processor temperature.

If bit 4 of the IA32_CLOCK_MODULATION MSR is written to a ‘1’, the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same IA32_CLOCK_MODULATION MSR. In On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Thermal Monitor. If the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

6.2.3 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot) is asserted when the processor die temperature has reached its factory configured trip point. If Thermal Monitor is enabled (note that Thermal Monitor must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. Refer to the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programmer's Guide* for specific register and programming details.

PROCHOT# is designed to assert at or a few degrees higher than maximum T_{CASE} (as specified by Thermal Profile A) when dissipating TDP power, and cannot be interpreted as an indication of processor case temperature. This temperature delta accounts for processor package, lifetime and manufacturing variations and attempts to ensure the Thermal Control Circuit is not activated below maximum T_{CASE} when dissipating TDP power. There is no defined or fixed correlation between the PROCHOT# trip temperature, the case temperature or the thermal diode temperature. Thermal solutions must be designed to the processor specifications and cannot be adjusted based on experimental measurements of T_{CASE}, PROCHOT#, or Tdiode on random processor samples.

6.2.4 FORCEPR# Signal Pin

The FORCEPR# (force power reduction) input can be used by the platform to cause the Dual-Core Intel Xeon processor to activate the TCC of each core. If the Thermal Monitor is enabled, the TCC will be activated upon the assertion of the FORCEPR# signal. The TCC will remain active until the system deasserts FORCEPR#. FORCEPR# is an asynchronous input. FORCEPR# can be used to

thermally protect other system components. To use the VR as an example, when the FORCEPR# pin is asserted, the TCC circuit of each core within the processor will activate, reducing the current consumption of the processor and the corresponding temperature of the VR.

If should be noted that assertion of the FORCEPR# does not automatically assert PROCHOT#. As mentioned previously, the PROCHOT# signal is asserted when a high temperature situation is detected. A minimum pulse width of 500 µs is recommend when the FORCEPR# is asserted by the system. Sustained activation of the FORCEPR# pin may cause noticeable platform performance degradation.

Refer to the appropriate platform design guidelines for details on implementing the FORCEPR# signal feature.

6.2.5 THERMTRIP# Signal Pin

Regardless of whether or not Thermal Monitor is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Table 4-1). At this point, the system bus signal THERMTRIP# will go active and stay active as described in Table 4-1. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

6.2.6 $T_{CONTROL}$ and Fan Speed Reduction

Tcontrol is a temperature specification based on a temperature reading from the thermal diode. The value for Tcontrol will be calibrated in manufacturing and configured for each processor. The Tcontrol temperature for a given processor can be obtained by reading the IA32_TEMPERATURE_TARGET MSR in the processor. Each core within the processor will have an IA32_TEMPERATURE_TARGET MSR that will be programmed to the same value. The Tcontrol value that is read from the IA32_TEMPERATURE_TARGET MSR must be converted from Hexadecimal to Decimal and added to a base value. The base value is 50 °C for the Dual-Core Intel Xeon processor.

The value of Tcontrol may vary from 0x00h to 0x1Eh. Refer to the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programmer's Guide* for specific register and implementation details.

When Tdiode is above Tcontrol, then T_{CASE} must be at or below T_{CASE_MAX} as defined by the thermal profile. (See Figure 6-1; Table 6-2 and Table 6-3). Otherwise, the processor temperature can be maintained at Tcontrol.

6.2.7 Thermal Diode

The processor incorporates an on-die thermal diode. A thermal sensor located on the system board may monitor the die temperature of the processor for thermal management/long term die temperature change purposes. This thermal diode is separate from the Thermal Monitor’s thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

§

7 Features

7.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The Dual-Core Intel Xeon processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifics on these options, please refer to Table 7-1.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor, for reset purposes, the processor does not distinguish between a “warm” reset and a “power-on” reset.

Table 7-1. Power-On Configuration Option Pins

Configuration Option	Pin	Notes
Output tri state	SMI#	1,2,4
Execute BIST (Built-In Self Test)	INIT#	1,2,4
In Order Queue de-pipelining (set IOQ depth to 1)	A7#	1,2,4
Disable MCERR# observation	A9#	1,2,4
Disable BINIT# observation	A10#	1,2,4
Disable bus parking	A15#	1,2,4
Symmetric agent arbitration ID	BR[3:0]#	1,2,3,4
Enable Single Logical Processor Mode	A31#	1,2,5

NOTES:

1. Asserting this signal during RESET# will select the corresponding option.
2. Address pins not identified in this table as configuration options should not be asserted during RESET#.
3. The Dual-Core Intel Xeon processor utilizes all four BR0#, BR1#, BR2# and BR3# signals. Please refer to the appropriate platform design guide for further details
4. All power-on configuration settings affect both cores of the processor.
5. This mode not tested.

7.2 Clock Control and Low Power States

The processor allows the use of HALT, Stop-Grant and Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 7-1 for a visual representation of the processor low power states.

The Dual-Core Intel Xeon processor adds supports for the Enhanced HALT state. Refer to Figure 7-1 and the following sections. For more configuration details also refer to the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programmer's Guide*.

The Stop Grant state requires chipset and BIOS support on multiprocessor systems. In a multiprocessor system, all the STPCLK# signals are bussed together, thus all processors are affected in unison. The Hyper-Threading Technology feature adds the conditions that all logical processors share the same STPCLK# signal internally. When the STPCLK# signal is asserted, the processor enters the Stop Grant state, issuing a Stop Grant Special Bus Cycle (SBC) for each processor or logical processor. The chipset needs to account for a variable number of processors asserting the Stop Grant SBC on the bus before allowing the processor to be transitioned into one

of the lower processor power states. Refer to the applicable chipset specification and the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programmer's Guide* for more information.

Due to the inability of processors to recognize bus transactions during the Sleep state, multiprocessor systems are not allowed to simultaneously have one processor in Sleep state and the other processors in Normal or Stop-Grant state.

7.2.1 Normal State

This is the normal operating state for the processor.

7.2.2 HALT or Enhanced HALT States

The Enhanced HALT power down state is enabled by default in the Dual-Core Intel Xeon processor. The Enhanced HALT power down state must remain enabled via the BIOS. Refer to the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programmer's Guide*. The Enhanced HALT state requires support for dynamic VID transitions in the platform.

7.2.2.1 HALT Powerdown State

HALT is a low power state entered when the processor executes the HALT or MWAIT instruction. When one of the logical processors executes the HALT or MWAIT instruction, that logical processor is halted; however, the other processor continues normal operation. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, LINT[1:0] (NMI, INTR), or an interrupt delivered over the front side bus. RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the HALT Power Down state. See the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the HALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in HALT Power Down state, the processor will process front side bus snoops and interrupts.

7.2.2.2 Enhanced HALT Powerdown State

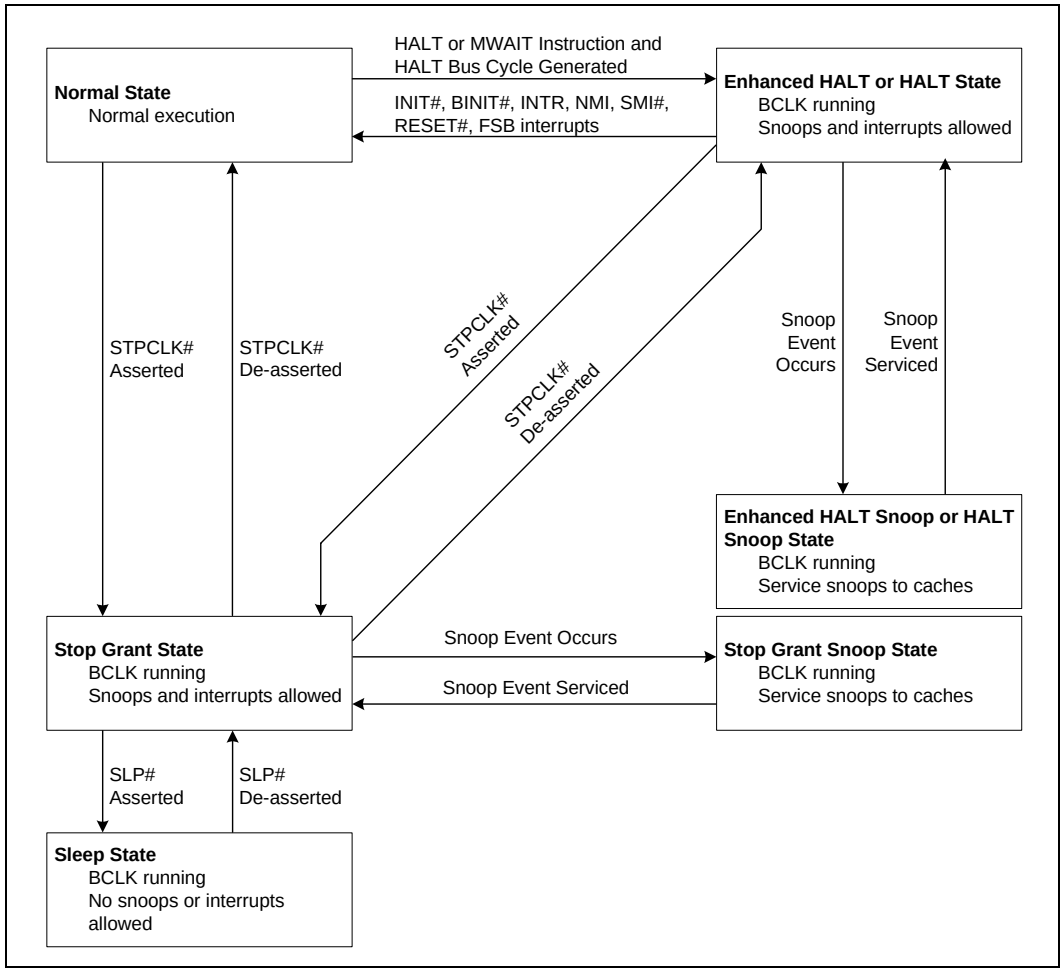
Enhanced HALT state is a low power state entered when all logical processors have executed the HALT or MWAIT instruction and Enhanced HALT state has been enabled via the BIOS. When one of the logical processors executes the HALT instruction, that logical processor is halted; however, the other processor continues normal operation. The Enhanced HALT state is generally a lower power state than the Stop Grant state.

The processor will automatically transition to a lower core frequency and voltage operating point before entering the Enhanced HALT state. Note that the processor FSB frequency is not altered; only the internal core frequency is changed. When entering the low power state, the processor will first switch to the lower bus ratio and then transition to the lower VID.

While in the Enhanced HALT state, the processor will process bus snoops.

The processor exits the Enhanced HALT state when a break event occurs. When the processor exists the Enhanced HALT state, it will first transition the VID to the original value and then change the bus ratio back to the original value.

Figure 7-1. Stop Clock State Machine



7.2.3 Stop-Grant State

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle. Once the STPCLK# pin has been asserted, it may only be deasserted once the processor is in the Stop Grant state. For the Dual-Core Intel Xeon processor, all logical processors must be in the Stop Grant state before the deassertion of STPCLK#.

Since the AGTL+ signal pins receive power from the front side bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the front side bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should only be deasserted one or more bus clocks after the deassertion of SLP#.

A transition to the Grant Snoop state will occur when the processor detects a snoop on the front side bus (see Section 7.2.4). A transition to the Sleep state (see Section 7.2.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant state, SMI#, INIT#, BINIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process snoops on the front side bus and it will latch interrupts delivered on the front side bus.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

7.2.4 Enhanced HALT Snoop or HALT Snoop State, Stop Grant Snoop State

The Enhanced HALT Snoop state is used in conjunction with the Enhanced HALT state. If Enhanced HALT state is not enabled in the BIOS, the default Snoop state entered will be the HALT Snoop state. Refer to the sections below for details on HALT Snoop state, Grant Snoop state and Enhanced HALT Snoop state.

7.2.4.1 HALT Snoop State, Stop Grant Snoop State

The processor will respond to snoop or interrupt transactions on the front side bus while in Stop-Grant state or in HALT Power Down state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the front side bus has been serviced (whether by the processor or another agent on the front side bus) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor will return to the Stop-Grant state or HALT Power Down state, as appropriate.

7.2.4.2 Enhanced HALT Snoop State

The Enhanced HALT Snoop state is the default Snoop state when the Enhanced HALT state is enabled via the BIOS. The processor will remain in the lower bus ratio and VID operating point of the Enhanced HALT state.

While in the Enhanced HALT Snoop state, snoops and interrupt transactions are handled the same way as in the HALT Snoop state. After the snoop is serviced or the interrupt is latched, the processor will return to the Enhanced HALT state.

7.2.5 Sleep State

The Sleep state is a very low power state in which each processor maintains its context, maintains the phase-locked loop (PLL), and has stopped most of internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the processor will enter the Sleep state

upon the assertion of the SLP# signal. The SLP# pin has a minimum assertion of one BCLK period. The SLP# pin should only be asserted when the processor is in the Stop Grant state. For Dual-Core Intel® Xeon® processors, the SLP# pin may only be asserted when all logical processors are in the Stop-Grant state. SLP# assertions while the processors are not in the Stop-Grant state are out of specification and may results in illegal operation.

Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the front side bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the reset sequence.

When the processor is in Sleep state, it will not respond to interrupts or snoop transactions.

7.3 Enhanced Intel SpeedStep® Technology

Enhanced Intel SpeedStep Technology enables the processor to switch between **multiple** frequency and voltage points, which may result in platform power savings. In order to support this technology, the system must support dynamic VID transitions. Switching between voltage / frequency states is software controlled. For more configuration details also refer to the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programmer's Guide*.

Note: Not all processors are capable of supporting Enhanced Intel SpeedStep Technology. Details on which processor frequencies support this feature are provided in the *Dual-Core Intel® Xeon® Processor 2.80 GHz Specification Update*.

Enhanced Intel SpeedStep Technology is a technology that creates processor performance states (P-states). P-states are power consumption and capability states within the Normal state. Enhanced Intel SpeedStep Technology enables real-time dynamic switching between frequency and voltage points. It alters the performance of the processor by changing the bus to core frequency ratio and voltage. This allows the processor to run at different core frequencies and voltages to best serve the performance and power requirements of the processor and system. Note that the front side bus is not altered; only the internal core frequency is changed. In order to run at reduced power consumption, the voltage is altered in step with the bus ratio. The Dual-Core Intel Xeon processor includes hardware logic that coordinates the requested processor voltage between the cores. The highest voltage that is requested for either of the processor cores is selected for that processor.

The following are key features of Enhanced Intel SpeedStep Technology:

1. Multiple voltage / frequency operating points provide optimal performance at reduced power consumption.
2. Voltage / Frequency selection is software controlled by writing to processor MSR’s (Model Specific Registers), thus eliminating chipset dependency.

If the target frequency is higher than the current frequency, V_{CC} is incremented in steps (+12.5 mV) by placing a new value on the VID signals. The Phase Lock Loop (PLL) then locks to the new frequency. Note that the top frequency for the processor can not be exceeded.

If the target frequency is lower than the current frequency, the PLL locks to the new frequency. The V_{CC} is then decremented in step (-12.5 mV) by changing the target VID through the VID signals.

Refer to the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programmer's Guide* for specific information to enable and configure Enhanced Intel SpeedStep Technology in BIOS.

§

8 Boxed Processor Specifications

8.1 Introduction

Intel boxed processors are intended for system integrators who build systems from components available through distribution channels. The Dual-Core Intel Xeon processor is offered as an Intel boxed processor.

Intel offers boxed processors with three product configurations available for each processor frequency: 1U passive, 2U passive and 2U+ Active. Although the active thermal solution mechanically fits into a 2U keepout, additional design considerations may need to be addressed to provide sufficient airflow to the fan inlet.

The active thermal solution is primarily designed to be used in a pedestal chassis where sufficient air inlet space is present and side directional airflow is not an issue. The 1U and 2U passive thermal solutions require the use of chassis ducting and are targeted for use in rack mount servers. The retention solution used for these products is called the Common Enabling Kit, or CEK. The CEK base is compatible with all three thermal solutions.

The active heat sink solution for the boxed processor will be a 4-pin pulse width modulated (PWM) T-diode controlled solution. Use of a 4-pin PWM T-diode controlled active thermal solution helps customers meet acoustic targets in pedestal platforms through the platform's ability to directly control the active thermal solution. It may be necessary to modify existing baseboard designs with 4-pin CPU fan headers and other required circuitry for PWM operation. If a 4-pin PWM T-diode controlled active thermal solution is connected to an older 3-pin CPU fan header, the thermal solution will revert back to a thermistor controlled mode. Please see the Section 8.3, "Electrical Requirements" on page 8-95 for more details.

Figure 8-1 through Figure 8-3 are representations of the three heat sink solutions that will be offered as part of a boxed processor. Figure 8-4 shows an exploded view of the boxed processor thermal solution and the other CEK retention components.

Figure 8-1. 1U Passive CEK Heat Sink

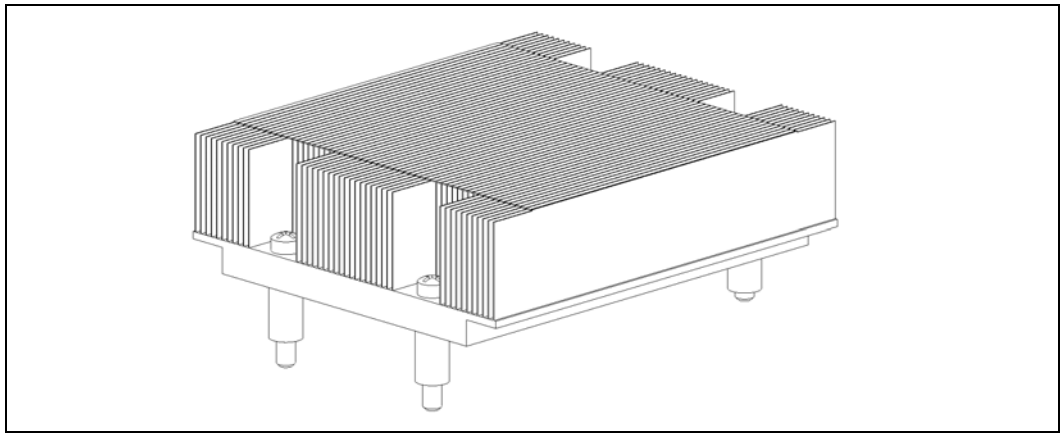


Figure 8-2. 2U Passive CEK Heat Sink

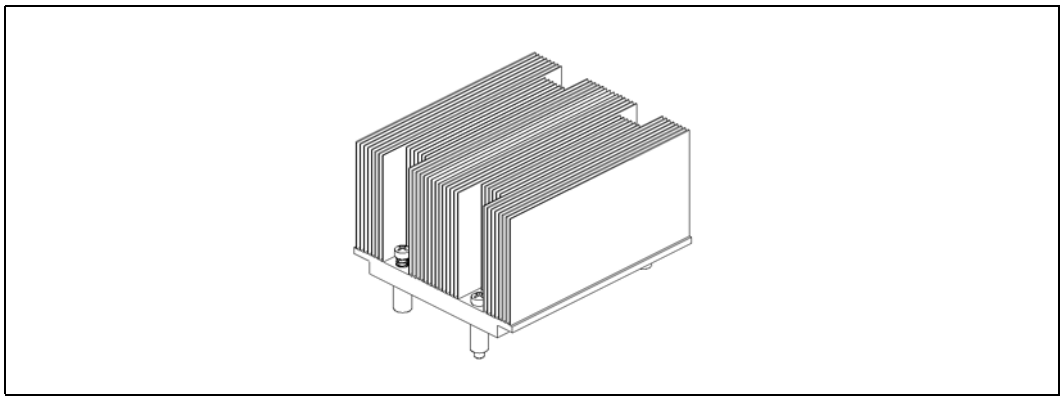


Figure 8-3. Active CEK Heat Sink (Representation Only)

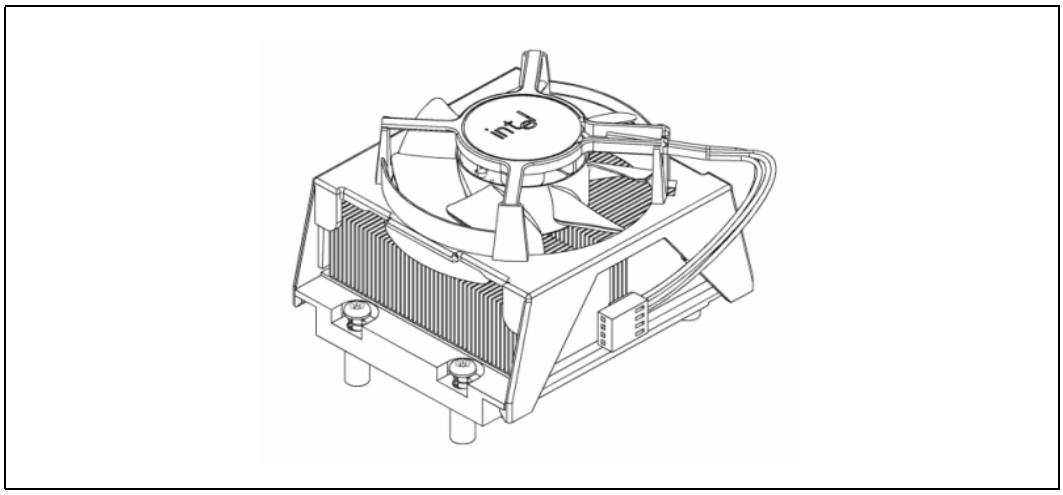
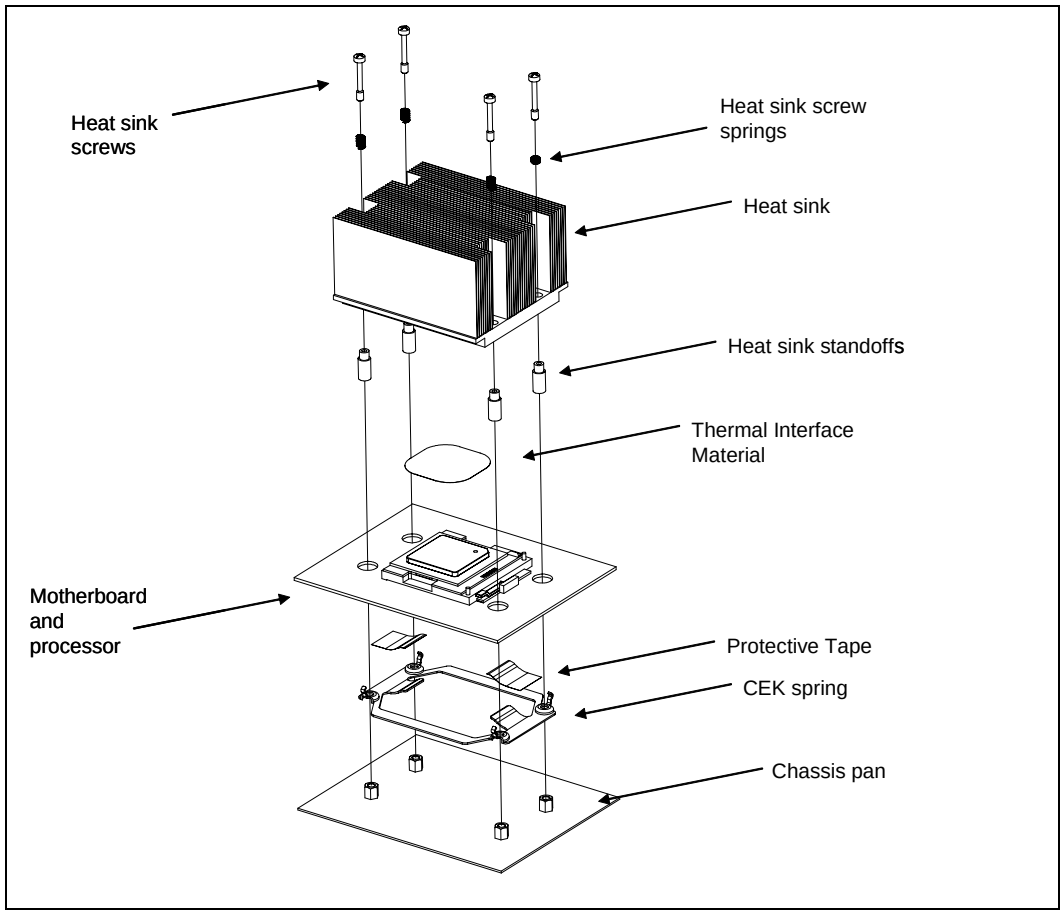


Figure 8-4. Passive Thermal Solution (2U and larger)



NOTE:
1. The heat sink in this image is for reference only, and may not represent any of the actual boxed processor heat sinks.
2. The screws, springs, and standoffs will be captive to the heat sink. This image shows all of the components in an exploded view.
3. It is intended that the CEK spring will ship with the base board and be pre-attached prior to shipping.

8.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed processor.

8.2.1 Boxed Processor Heat Sink Dimensions (CEK)

The boxed processor will be shipped with an unattached thermal solution. Clearance is required around the thermal solution to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor and assembled heat sink are shown in Figure 8-5 through Figure 8-9. Figure 8-10 through Figure 8-11 are the mechanical drawings for the 4-pin server board fan header and 4-pin connector used for the active CEK fan heat sink solution.

Figure 8-5. Top Side Board Keep-Out Zones (Part 1)

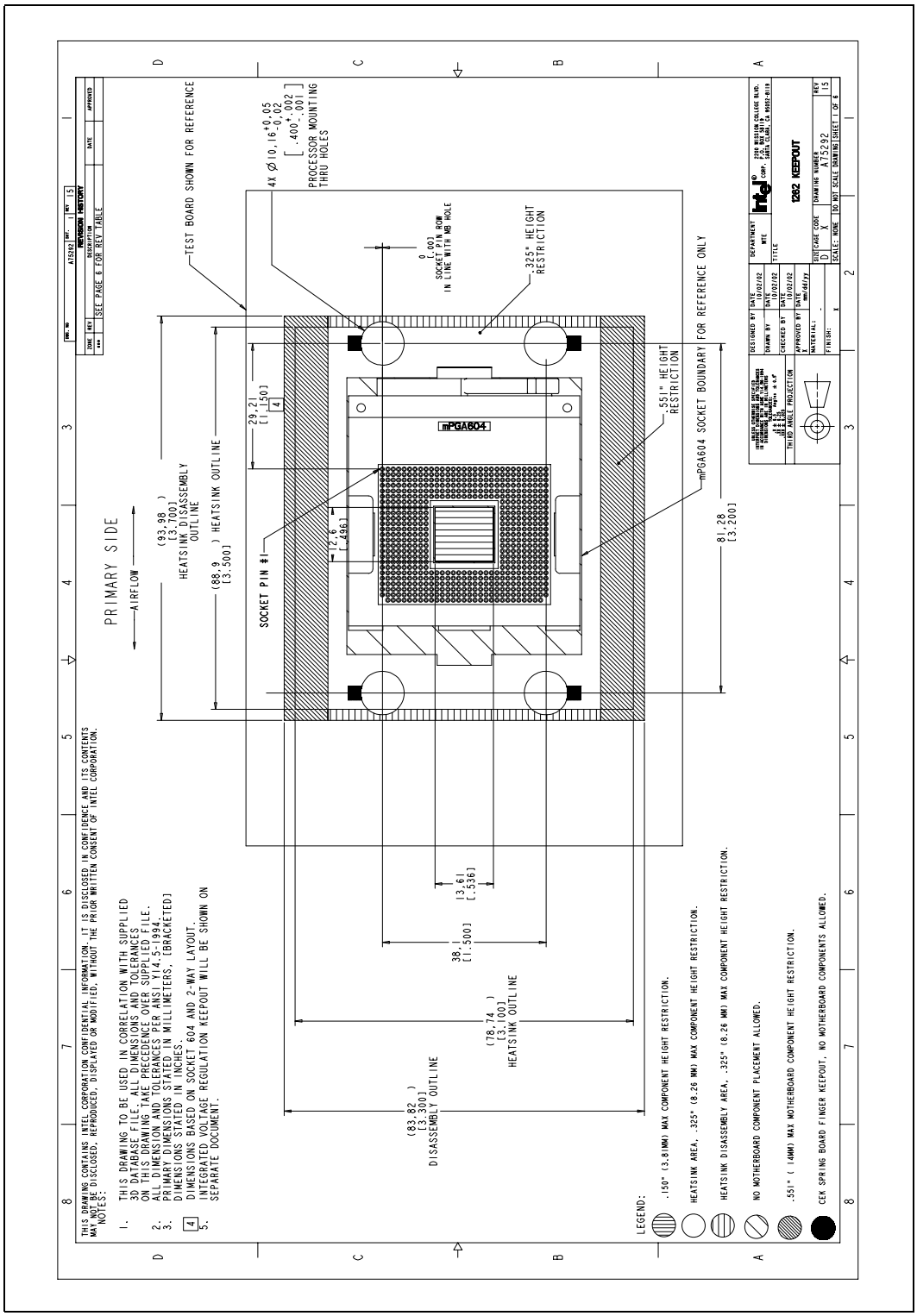


Figure 8-6. Top Side Board Keep-Out Zones (Part 2)

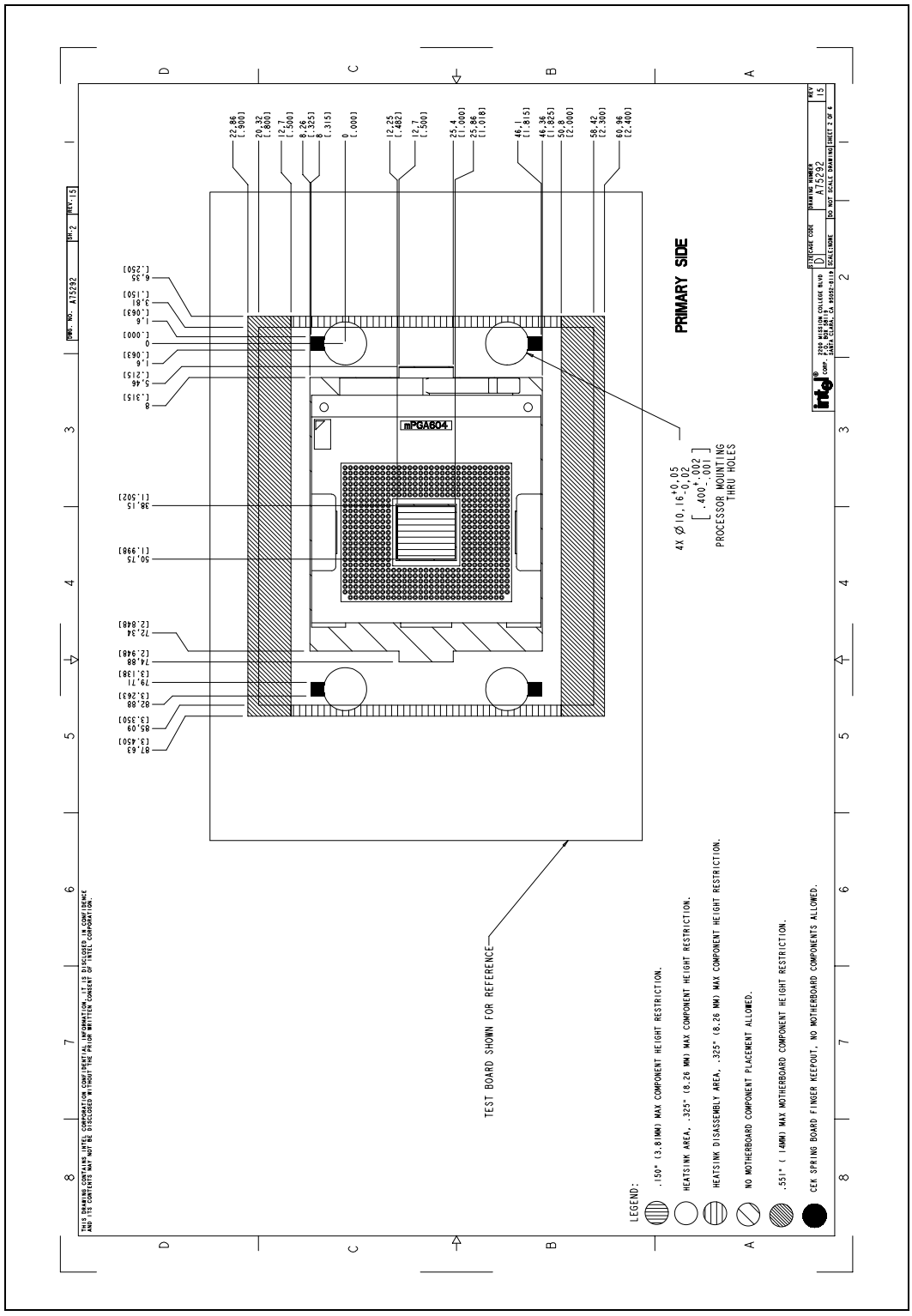


Figure 8-7. Bottom Side Board Keep-Out Zones

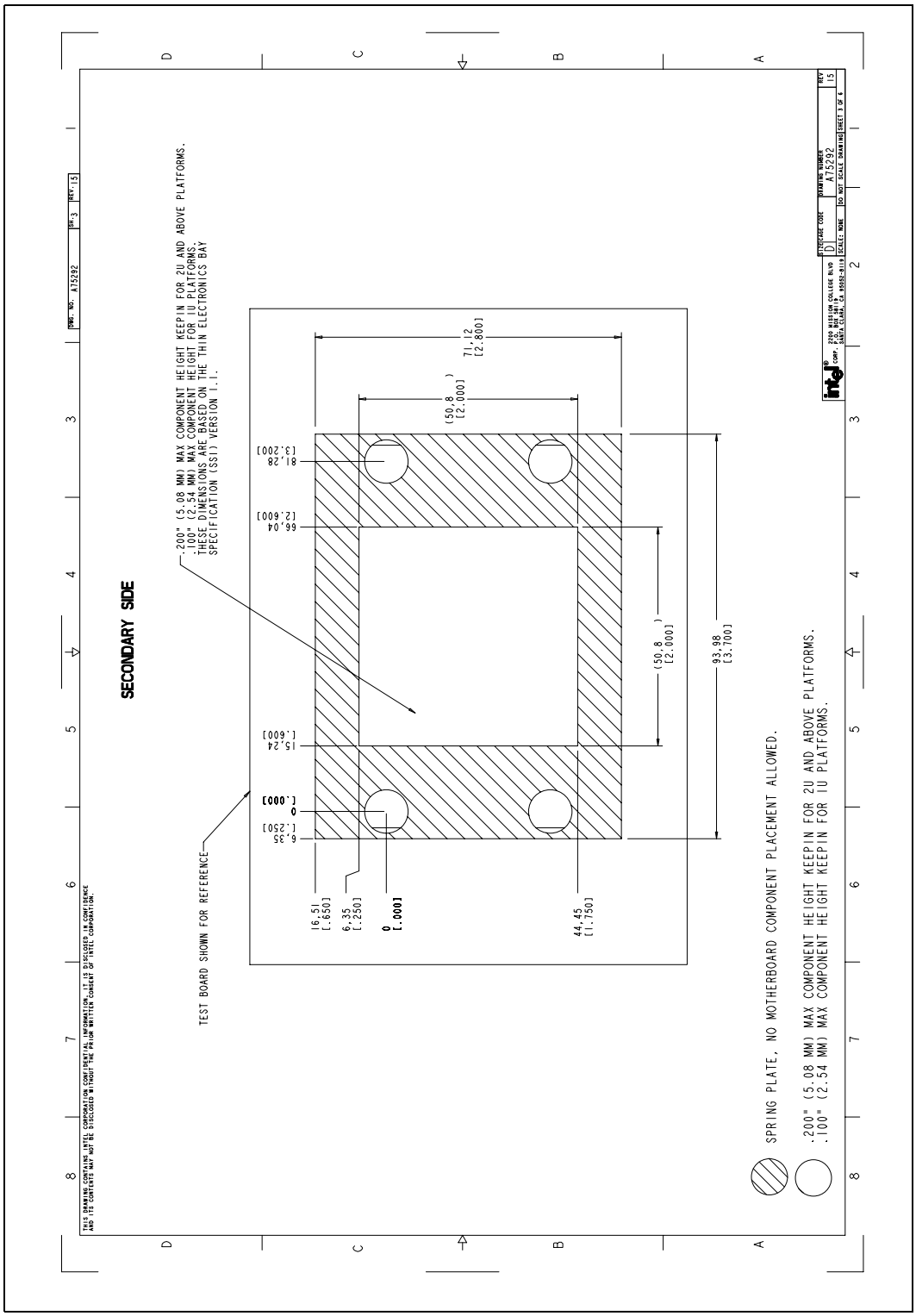


Figure 8-8. Board Mounting Hole Keep-Out Zones

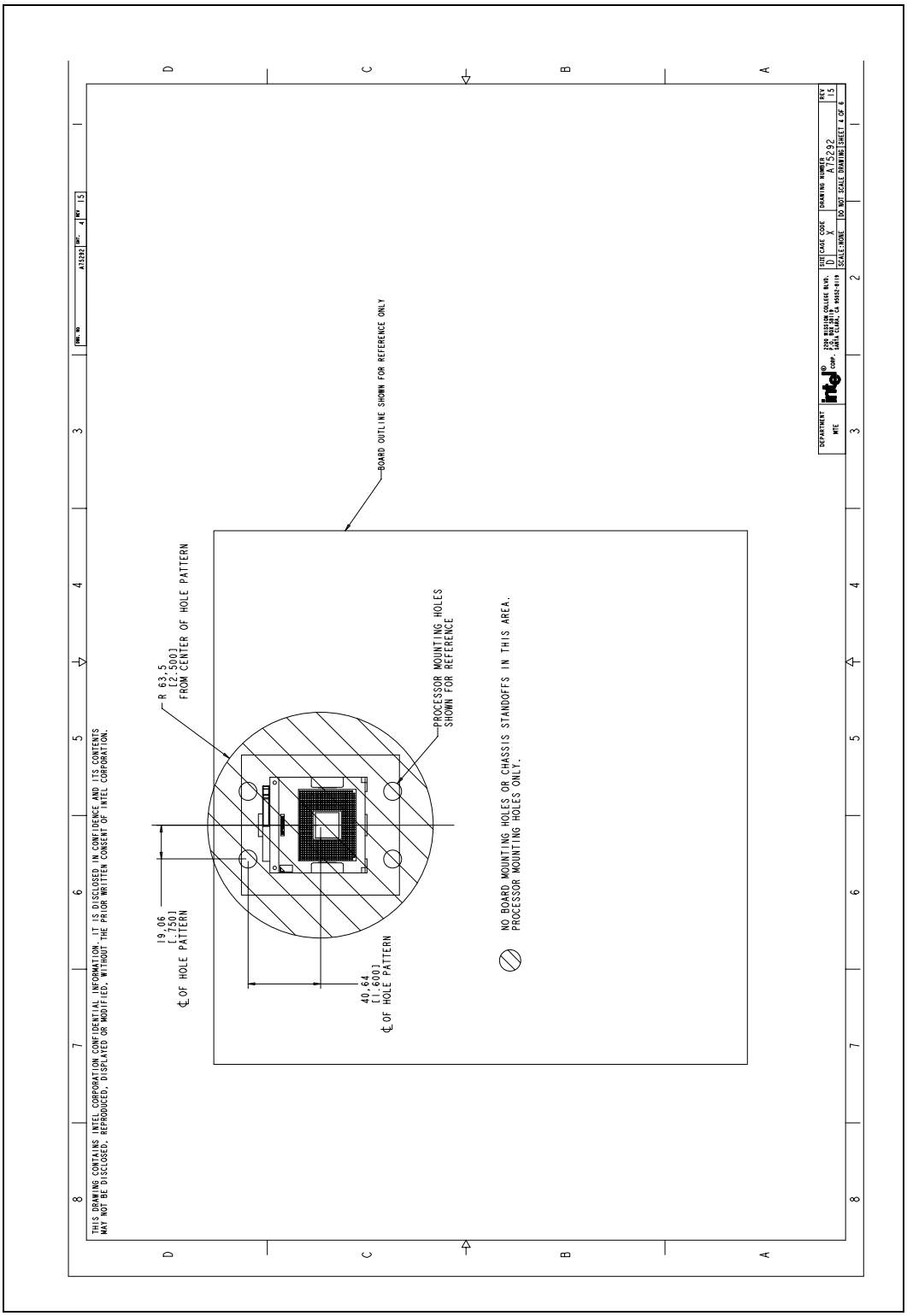


Figure 8-9. Volumetric Height Keep-Ins

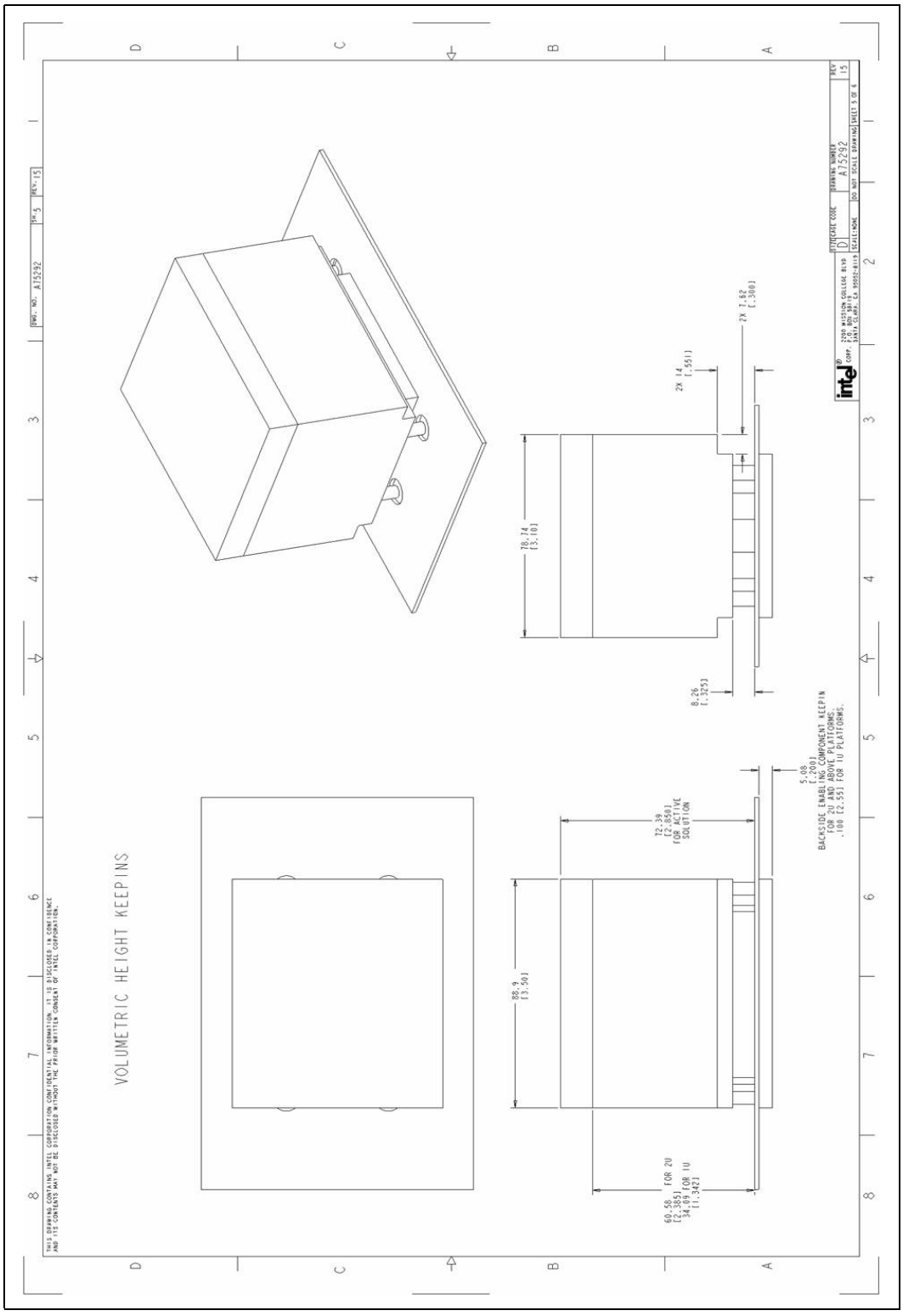


Figure 8-10. 4-Pin Fan Cable Connector (For Active CEK Heat Sink)

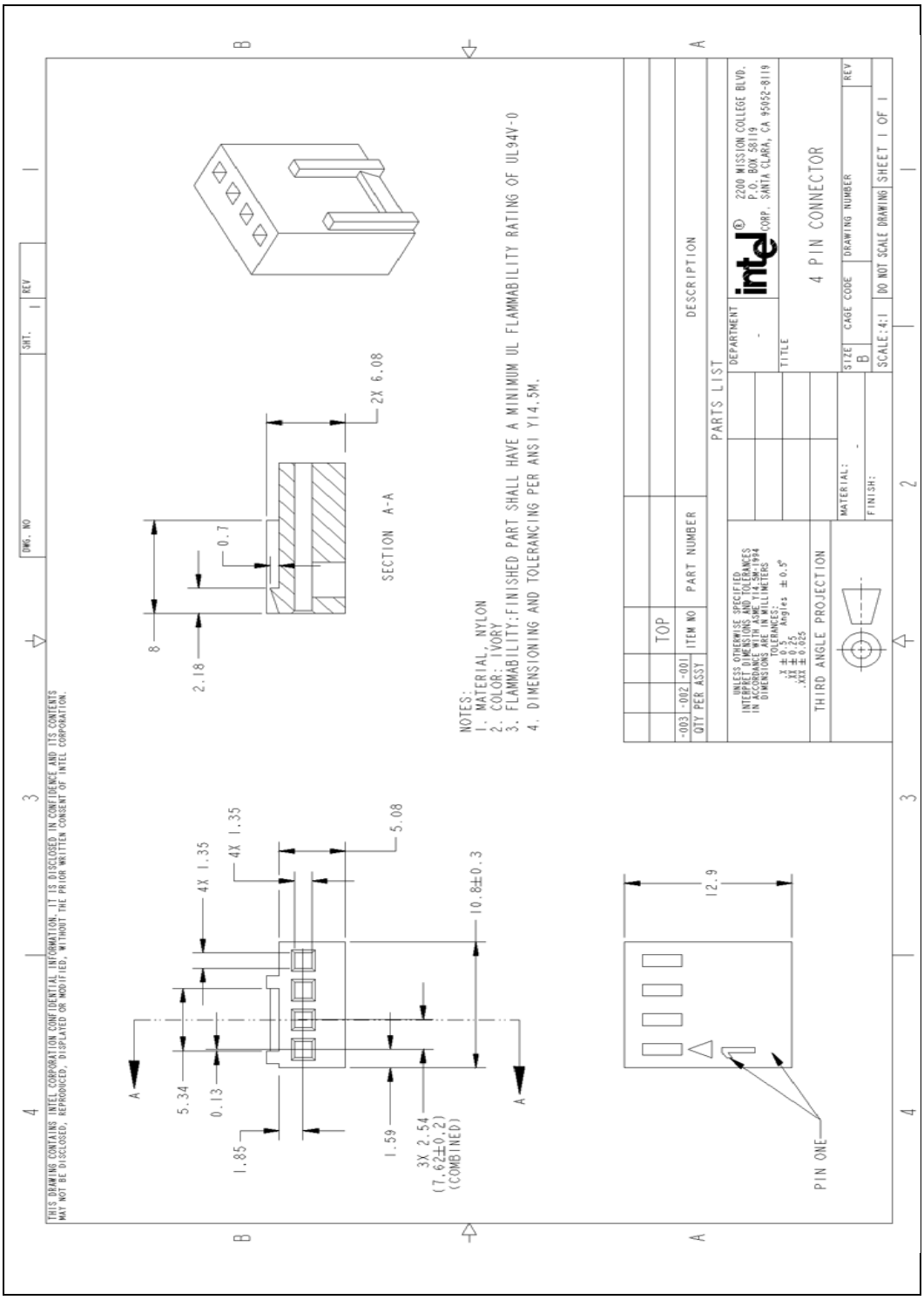
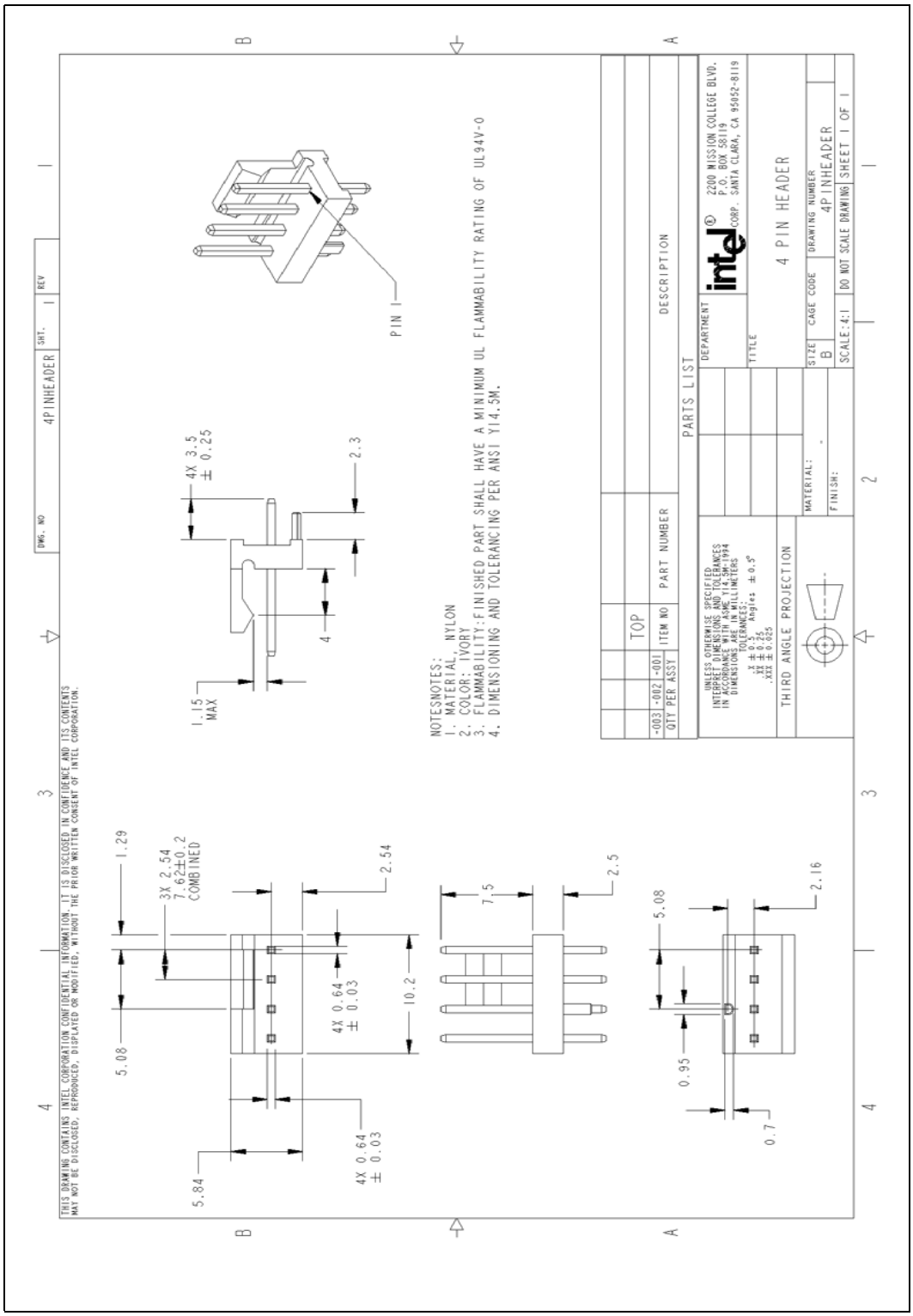


Figure 8-11. 4-Pin Base Board Fan Header (For Active CEK Heat Sink)



8.2.2 Boxed Processor Heat Sink Weight

8.2.2.1 Thermal Solution Weight

The 2U passive and 2U+ active heat sink solutions will not exceed a mass of 1050 grams. Note that this is per processor, therefore a dual processor system will likely have up to 2100 grams of total mass for the heat sinks alone. The 1U CEK heat sink will not exceed a mass of 700 grams, for a total of 1400 grams of heat sink mass in a dual processor system. This large mass requires that minimum chassis stiffness be met in order to withstand reasonable shock and vibration forces.

Please refer to Section 3.6 for details on the weight of the processor.

8.2.3 Boxed Processor Retention Mechanism and Heat Sink Support (CEK)

Baseboards and chassis designed for use by a system integrator should include holes that are in proper alignment with each other to support the boxed processor. Refer to the *Server System Infrastructure Specification (SSI-EEB 3.51)* or see http://www.ssiforum.org for details on the hole locations.

Figure 8-4 illustrates the new Common Enabling Kit (CEK) retention solution. The CEK is designed to extend air-cooling capability through the use of larger heat sinks with minimal airflow blockage and bypass. CEK retention mechanisms can allow the use of much heavier heat sink masses compared to legacy limits by using a load path directly attached to the chassis pan. The CEK spring on the secondary side of the baseboard provides the necessary compressive load for the thermal interface material. The baseboard is intended to be isolated such that the dynamic loads from the heat sink are transferred to the chassis pan via the stiff screws and standoffs. The retention scheme reduces the risk of package pullout and solder joint failures.

The baseboard mounting holes for the CEK solution are the same location as the legacy server processor hole locations, as specified by the SSI EEB 3.5. However, the CEK assembly requires larger diameter holes to compensate for the CEK spring embosses. The holes now need to be 10.2 mm [0.402 in.] in diameter.

All components of the CEK heat sink solution will be captive to the heat sink and will only require a Phillips screwdriver to attach to the chassis pan. When installing the CEK, the CEK screws should be tightened until they will no longer turn easily. This should represent approximately 8 inch-pounds of torque. Avoid applying more than 10 inch-pounds of torque; otherwise, damage may occur to retention mechanism components.

For further details on the CEK thermal solution, refer to the *Dual-Core Intel® Xeon® Processor 2.80 GHz Thermal/Mechanical Design Guidelines* (see Section 1.2).

8.3 Electrical Requirements

8.3.1 Power Supply Requirements

Due to the design differences between the Dual-Core Intel Xeon processor and the 64-bit Intel® Xeon® processor with 2MB L2 cache, the Dual-Core Intel Xeon processor has slightly greater +12V rail current requirements. Systems using Dual-Core Intel Xeon processors require power supply designs with split +12V rails capable of supplying a minimum of 15 amps of continuous

current while also being able to supply up to 17.5 amps at peak load times. Power supplies not meeting these criteria should not be used in systems using the Dual-Core Intel Xeon processor as these systems may exhibit unstable behavior, particularly during peak load times.

8.3.2 Fan Power Supply (Active CEK)

The 4-pin PWM/T-diode controlled active thermal solution is being offered to help provide better control over pedestal chassis acoustics. This is achieved though more accurate measurement of processor die temperature through the processor's temperature diode (T-diode). Fan RPM is modulated through the use of an ASIC located on the baseboard, that sends out a PWM control signal to the 4th pin of the connector labeled as **Control**. This thermal solution requires a constant +12 V supplied to pin 2 of the active thermal solution and does not support variable voltage control or 3-pin PWM control. See Table 8-2 for details on the 3- and 4-pin active heat sink solution connectors.

If the new 4-pin active fan heat sink solution is connected to an older 3-pin baseboard CPU fan header it will default back to a thermistor controlled mode, allowing compatibility with existing designs. When operating in thermistor controlled mode, fan RPM is automatically varied based on the T_{INLET} temperature measured by a thermistor located at the fan inlet. It may be necessary to change existing baseboard designs to support the new 4-pin active heat sink solution if PWM/ T-diode control is desired. It may also be necessary to verify that the larger 4-pin fan connector will not interfere with other components installed on the baseboard.

The fan power header on the baseboard must be positioned to allow the fan heat sink power cable to reach it. The fan power header identification and location must be documented in the suppliers platform documentation, or on the baseboard itself. The baseboard fan power header should be positioned within 177.8 mm [7 in.] from the center of the processor socket.

Table 8-1. PWM Fan Frequency Specifications for 4-Pin Active CEK Thermal Solution

Description	Min Frequency	Nominal Frequency	Max Frequency	Unit
PWM Control Frequency Range	21,000	25,000	28,000	Hz

Table 8-2. Fan Specifications for 4-pin Active CEK Thermal Solution

Description	Min	Typ Steady	Max Steady	Max Startup	Unit
+12 V: 12 volt fan power supply	10.8	12	12	13.2	V
IC: Fan Current Draw	N/A	1	1.25	1.5	A
SENSE: SENSE frequency	2	2	2	2	Pulses per fan revolution

Figure 8-12. Fan Cable Connector Pin Out for 4-Pin Active CEK Thermal Solution

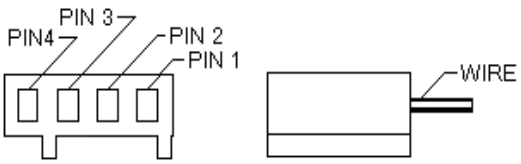


Table 8-3. Fan Cable Connector Pin Out for 4-Pin Active CEK Thermal Solution

Pin Number	Signal	Color
1	Ground	Black
2	**Power:** (+12 V)	Yellow
3	**Sense:** 2 pulses per revolution	Green
4	**Control:** 21 KHz-28 KHz	Blue

Table 8-4. Fan Cable Connector Supplier & Part Number

Vendor	3-Pin Connector Part Number	4-Pin Connector Part Number
AMP	Fan Connector: 643815-3 Header: 640456-3	N/A
Walden Molex	Fan Connector: 22-01-3037 Header: 22-23-2031	Fan Connector: 47054-1000 Header: 47053-1000
Wieson	N/A	Fan Connector: 2510C888-001 Header: 2366C888-007
Foxconn	N/A	Fan Connector: N/A Header: HF27040-M1

This section describes the cooling requirements of the heat sink solution utilized by the boxed processor.

8.3.3 Boxed Processor Cooling Requirements

As previously stated the boxed processor will be available in three product configurations. Each configuration will require unique design considerations. Meeting the processor's temperature specifications is also the function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specifications are found in Section 6 of this document.

8.3.3.1 1U Passive CEK Heat Sink (1U form factor)

In the 1U configuration it is assumed that a chassis duct will be implemented to provide 15 CFM [x m^3/hr] of airflow to pass through the heat sink fins. The duct should be designed as precisely as possible and should not allow any air to bypass the heat sink (0" bypass) and a back pressure of 0.375 in. H_2O [y dP] (25.5m^3/hr @ 93.3Pa). It is assumed that a 40° C T_{LA} is met. This requires a

superior chassis design to limit the T_{RISE} at or below 5° C with an external ambient temperature of 35° C. Following these guidelines will allow the designer to meet Thermal Profile B and conform to the thermal requirements of the processor.

8.3.3.2 2U Passive CEK Heat Sink (2U and above form factor)

Once again a chassis duct is required for the 2U passive heat sink. In this configuration Thermal Profile A (see Section 6) should be followed by supplying 22 CFM [x m^3/hr] of airflow through the fins of the heat sink with a 0" or no duct bypass and a back pressure of 0.142 in. H_2O [y dP] (37.4m^3/hr @ 35.5 Pa). The T_{LA} temperature of 40° C should be met. This may require the use of superior design techniques to keep T_{RISE} at or below 5° C based on an ambient external temperature of 35° C.

8.3.3.3 2U+ Active CEK Thermal Solution (2U+ and above pedestal)

This thermal solution was designed to help pedestal chassis users to meet the thermal processor requirements without the use of chassis ducting. It may be necessary to implement some form of chassis air guide or air duct to meet the T_{LA} temperature of 40° C depending on the pedestal chassis layout. Also, while the active thermal solution is designed to mechanically fit into a 2U chassis, it may require additional space at the top of the thermal solution to allow sufficient airflow into the heat sink fan. Therefore, additional design criteria may need to be considered if this thermal solution is used in a 2U rack mount chassis, or in a chassis that has drive bay obstructions above the inlet to the fan heat sink.

Thermal Profile A should be used to help determine the thermal performance of the platform.

Once again it is recommended that the ambient air temperature outside of the chassis be kept at or below 35° C. The air passing directly over the processor thermal solution should not be preheated by other system components. Meeting the processor's temperature specification is the responsibility of the system integrator.

8.4 Boxed Processor Contents

A direct chassis attach method must be used to avoid problems related to shock and vibration, due to the weight of the thermal solution required to cool the processor. The board must not bend beyond specification in order to avoid damage. The boxed processor contains the components necessary to solve both issues. The boxed processor will include the following items:

- Dual-Core Intel Xeon processor
- Unattached (Active or Passive) Thermal Solution
- 4 screws, 4 springs, and 4 heat sink standoffs (all captive to the heat sink)
- Thermal Interface Material (pre-applied on heat sink)
- Installation Manual
- Intel Inside®, Logo

The other items listed in Figure 8-4 that are required to compete this solution will be shipped with either the chassis or boards. They are as follows:

- Heat sink standoffs (supplied by chassis vendors)

§

9 Debug Tools Specifications

Please refer to the *ITP700 Debug Port Design Guide* for information regarding debug tool specifications. Section 1.2 provides collateral details.

9.1 Debug Port System Requirements

The Dual-Core Intel Xeon processor debug port is the command and control interface for the In-Target Probe (ITP) debugger. The ITP enables run-time control of the processors for system debug. The debug port, which is connected to the front side bus, is a combination of the system, JTAG and execution signals. There are several mechanical, electrical and functional constraints on the debug port that must be followed. The mechanical constraint requires the debug port connector to be installed in the system with adequate physical clearance. Electrical constraints exist due to the mixed high and low speed signals of the debug port for the processor. While the JTAG signals operate at a maximum of 75 MHz, the execution signals operate at the common clock front side bus frequency (200 MHz). The functional constraint requires the debug port to use the JTAG system via a handshake and multiplexing scheme.

In general, the information in this chapter may be used as a basis for including all run-control tools in Dual-Core Intel Xeon processor-based system designs, including tools from vendors other than Intel.

Note: The debug port and JTAG signal chain must be designed into the processor board to utilize the ITP for debug purposes.

9.2 Target System Implementation

9.2.1 System Implementation

Specific connectivity and layout guidelines for the Debug Port are provided in the *ITP700 Debug Port Design Guide*.

9.3 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Dual-Core Intel Xeon processor systems. Tektronix and Agilent should be contacted to obtain specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Dual-Core Intel Xeon processor-based multiprocessor systems, the LAI is critical in providing the ability to probe and capture front side bus signals. There are two sets of considerations to keep in mind when designing a Dual-Core Intel Xeon processor-based system that can make use of an LAI: mechanical and electrical.

9.3.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI pins plug into the socket, while the processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include differerent requirements from the space normally occupied by the heat sink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

9.3.2 Electrical Considerations

The LAI will also affect the electrical performance of the front side bus, therefore it is critical to obtain electrical load models from each of the logic analyzer vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

§