Intel® Pentium® 4 Processor Extreme Edition on 0.13 Micron Process in the 775-land Package

Datasheet

November 2004

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[1] Hyper-Threading Technology requires a computer system with a Intel® Pentium® 4 processor on 90 nm process or an Intel® Pentium® 4 processor supporting HT technology and a Hyper-Threading Technology enabled chipset, BIOS and operating system. Performance will vary depending on the specific hardware and software you use. See <<http://www.intel.com/info/hyperthreading/>> for more information including details on which processors support HT Technology.

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Contents

Figures

Tables

Revision History

Revision No.	Description	Date
-001	• Initial release	June 2004
-002	• Added 3.46/1066 MHz FSB electrical and thermal specifications • Updated the Marking diagram • Updated the Boxed Processor Specification chapter	November 2004

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Intel® Pentium® 4 Processor Extreme Edition on 0.13 Micron Process in the 775-land Package Features

- Available at 3.40 GHz and 3.46 GHz
- Supports Hyper-Threading Technology (HT Technology)
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel NetBurst® microarchitecture
- System bus frequency at 800 MHz and 1066 MHz
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper-Pipelined Technology
  - —Advance Dynamic Execution
  - —Very deep out-of-order execution
- Enhanced branch prediction
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- 8-KB Level 1 data cache
- Level 1 Execution Trace Cache stores 12-K micro-ops and removes decoder latency from main execution loops
- 512-KB Advanced Transfer Cache (on-die, full-speed Level 2 (L2) cache) with 8-way associativity and Error Correcting Code (ECC)
- 2-MB Integrated Level 3 (L3) cache with 8-way associativity
- 144 Streaming SIMD Extensions 2 (SSE2) instructions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
  - —System Management mode
  - —Multiple low-power states
- 8-way cache associativity provides improved cache hit rate on load/store operations
- 775-land Package

The Intel® Pentium® 4 processor Extreme Edition family supporting Hyper-Threading Technology[1] (HT Technology) delivers Intel's advanced, powerful processors for desktop PCs and entry-level workstations, which are based on the Intel NetBurst® microarchitecture. The Pentium 4 processor Extreme Edition is designed to deliver performance across applications and usages where end-users can truly appreciate and experience the performance. These applications include Internet audio and streaming video, image processing, video content creation, speech, 3D, CAD, games, multimedia, and multitasking user environments. The Intel® Pentium® 4 processor Extreme Edition supporting HT Technology features 2 MB of L3 cache and offers high levels of performance targeted specifically for high-end gamers and computing power users.

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1 Introduction

The Intel® Pentium® 4 processor Extreme Edition on 0.13 micron process in 775-land package is a follow on to the Intel® Pentium® 4 processor Extreme Edition in the 478-pin package with Intel NetBurst® microarchitecture. The Pentium 4 processor Extreme Edition on 0.13 micron process in 775-land package uses Flip-Chip Land Grid Array (FC-LGA4) package technology, and plugs into a 775-land surface mount, Land Grid Array (LGA) socket, referred to as the LGA775 socket. The Pentium 4 processor Extreme Edition in the 775-land package, like its predecessor, the Pentium 4 processor Extreme Edition in the 478-pin package, is based on the same Intel 32-bit microarchitecture and maintains the tradition of compatibility with IA-32 software.

Note: In this document the Intel® Pentium® 4 processor Extreme Edition on 0.13 micron process in the 775-land package is also referred to as Pentium 4 processor Extreme Edition in the 775-land package (or simply as “processor”).

The Pentium 4 processor Extreme Edition in the 775-land package supports Hyper-Threading Technology[1]. Hyper-Threading Technology allows a single, physical processor to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architecture state with its own set of general-purpose registers, control registers to provide increased system responsiveness in multitasking environments, and headroom for next generation multithreaded applications. Intel recommends enabling Hyper-Threading Technology with Microsoft Windows* XP Professional or Windows* XP Home, and disabling Hyper-Threading Technology via the BIOS for all previous versions of Windows operating systems. For more information on Hyper-Threading Technology, see www.intel.com/info/hyperthreading. Refer to Section 6.1, for Hyper-Threading Technology configuration details.

The Intel NetBurst microarchitecture features include hyper pipelined technology, a rapid execution engine, 800 MHz system bus, and an execution trace cache. The hyper pipelined technology doubles the pipeline depth in the Pentium 4 processor Extreme Edition in the 775-land package, allowing the processor to reach much higher core frequencies. The rapid execution engine allows the two integer ALUs in the processor to run at twice the core frequency, which allows many integer instructions to execute in 1/2 clock tick. The 800 MHz or 1066 MHz system bus is a quad-pumped bus running off a 200 MHz or 266 MHz system clock making 6.4 GB/sec or 8.5 GB/sec data transfer rates possible. The execution trace cache is a first level cache that stores approximately 12k decoded micro-operations, which removes the instruction decoding logic from the main execution path, thereby increasing performance.

Additional features within the Intel NetBurst microarchitecture include advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 512-KB, on-die Level 2 (L2) cache. A new floating point and multi media unit has been implemented which provides superior performance for multi-media and mathematically intensive applications. Finally, SSE2 adds 144 new instructions for double-precision floating point, SIMD integer, and memory management.

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition. The new packed double-precision floating-point instructions enhance performance for applications that require greater range and precision, including scientific and engineering applications and advanced 3-D geometry techniques, such as ray tracing.

The 2-MB L3 cache is available with the Pentium 4 processor Extreme Edition in the 775-land package. The additional third level of cache is located on the processor die and is designed specifically to meet the compute needs of high-end gamers and other power users. The integrated L3 cache is available in 2-MB and is coupled with the 800 MHz or 1066 MHz system bus to provide a high bandwidth path to memory. The efficient design of the integrated L3 cache provides a faster path to large data sets stored in cache on the processor. This results in reduced average memory latency and increased throughput for larger workloads.

The processor’s Intel NetBurst microarchitecture front side bus (FSB) uses a split-transaction, deferred reply protocol like the Pentium 4 processor. The Intel NetBurst microarchitecture FSB uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a “double-clocked” or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 8.5 GB/sec.

Intel will enable support components for the processor including heatsink, heatsink retention mechanism, and socket. Manufacturability is a high priority; hence, mechanical assembly may be completed from the top of the baseboard and should not require any special tooling.

The processor includes an address bus powerdown capability that removes power from the address and data pins when the FSB is not in use. This feature is always enabled on the processor.

1.1 Terminology

A ‘#’ symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the ‘#’ symbol implies that the signal is inverted. For example, D[3:0] = ‘HLHL’ refers to a hex ‘A’, and D[3:0]# = ‘LHLH’ also refers to a hex ‘A’ (H= High logic level, L= Low logic level).

“FSB” refers to the interface between the processor and system core logic (a.k.a. the chipset components). The FSB is a multiprocessing interface to processors, memory, and I/O.

1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- **Intel® Pentium® 4 processor Extreme Edition on 0.13 micron process in 775-land package** — Processor in the FC-LGA4 package with a 2 MB L3 cache and 512-KB L2 cache.
- **Processor** — For this document, the term processor is the generic form of the Pentium 4 processor Extreme Edition on 0.13 micron process in 775-land package.
- **Keep-out zone** — The area on or near the processor that system design cannot utilize.
- **Intel® 925X Express Chipset** — Chipset that supports DDR2 memory technology for the Pentium 4 processor Extreme Edition in the 775-land package.
- **Processor core** — Processor core die with Level 2 (L2) and Level 3 (L3) cache.
- **FC-LGA4 package** — The Pentium 4 processor Extreme Edition in the 775-land package is available in a Flip-Chip Land Grid Array 4 package, consisting of a processor core mounted on a substrate with an integrated heat spreader (IHS).
- **LGA775 socket** — The Pentium 4 processor Extreme Edition in the 775-land package mates with the system board through a surface mount, 775-land, LGA socket.
- **Hyper-Threading Technology** — Hyper-Threading Technology allows a single, physical Pentium 4 processor to function as two logical processors when the necessary system ingredients are present. For more information, see: www.intel.com/info/hyperthreading.
- **Integrated heat spreader (IHS)** —A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Retention mechanism (RM)**—Since the LGA775 socket does not include any mechanical features for heatsink attach, a retention mechanism is required. Component thermal solutions should attach to the processor via a retention mechanism that is independent of the socket.
- **Storage conditions**—Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor lands should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to “free air” (i.e. unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
- **Functional operation**—Refers to normal operating conditions in which all processor specifications, including DC, AC, system bus, signal quality, mechanical and thermal, are satisfied.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document:

Table 1-1. References

Document	Doc Number / Location
Intel® Pentium® 4 Processor Specification Update	http://intel.com/design/Pentium4/specupdt/249199.htm
Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775	http://intel.com/design/Pentium4/guides/302356.htm
Intel® Architecture Software Developer's Manual: *IA-32 Intel® Architecture Software Developer's Manual Volume 1: Basic Architecture* *IA-32 Intel® Architecture Software Developer's Manual Volume 2A: Instruction Set Reference Manual A–M* *IA-32 Intel® Architecture Software Developer's Manual Volume 2B: Instruction Set Reference Manual, N–Z* *IA-32 Intel® Architecture Software Developer's Manual Volume 3: System Programming Guide*	http://developer.intel.com/design/pentium4/manuals/index_new.htm

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2 Electrical Specifications

This chapter describes the electrical characteristics of the processor interfaces and signals. DC electrical characteristics are provided.

2.1 FSB and GTLREF0

Most processor FSB signals use Gunning Transceiver Logic (GTL+) signaling technology. Pentium 4 processor Extreme Edition in the 775-land package terminates all on-die terminations to $V_{CC.}$ V_{TT} must be provided via a separate voltage source and not be connected to V_{CC}. This configuration allows for improved noise tolerance as processor frequency increases. Because of the speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families. Contact your Intel representative for details on design guidelines for the Pentium 4 processor Extreme Edition in the 775-land package.

The GTL+ inputs require a reference voltage (GTLREF0) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF0 must be generated on the system board (see Table 2-13 for GTLREF0 specifications). Termination resistors are provided on the processor silicon and are terminated to V_{CC}. Intel chipsets will also provide on-die termination, thus eliminating the need to terminate the bus on the system board for most GTL+ signals.

Some GTL+ signals do not include on-die termination and must be terminated on the system board. The GTL+ bus depends on incident wave switching. Therefore, timing calculations for GTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the FSB, including trace lengths, is highly recommended when designing a system.

2.2 Power and Ground Lands

For clean on-chip power distribution, the Pentium 4 processor Extreme Edition in the 775-land package has 226 VCC (power), 24 VTT and 273 VSS (ground) lands. All power lands must be connected to V_{CC}, all VTT lands must be connected to V_{TT}, while all VSS lands must be connected to a system ground plane.The processor VCC lands must be supplied the voltage determined by the VID (Voltage identification) signals.

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 2-5. Failure to do so can result in timing violations or reduced lifetime of the component. For further information and design guidelines, refer to the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775*.

2.3.1 V_{CC} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep a low interconnect resistance from the regulator to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low power states, must be provided by the voltage regulator solution (VR). In addition, a sufficient quality of low ESR ceramic capacitors are required in the socket cavity to ensure proper high frequency noise suppression. For more details on this topic, contact your Intel representative for further documentation and the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775*.

2.3.2 FSB GTL+ Decoupling

The Pentium 4 processor Extreme Edition in the 775-land package integrates signal termination on the die as well as incorporating high frequency decoupling capacitance on the processor package. Decoupling must also be provided by the system baseboard for proper GTL+ bus operation. For more information and documentation, contact your Intel representative.

2.4 Voltage Identification

The VID specification for the Pentium 4 processor Extreme Edition in the 775-land package is supported by the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775*. The voltage set by the VID signals is the reference VR output voltage to be delivered to the processor VCC pins. The specifications have been set such that one voltage regulator can work with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same speed may have different VID settings.

The Pentium 4 processor Extreme Edition in the 775-land package uses six voltage identification signals, VID[5:0], to support automatic selection of power supply voltages. Table 2-1 specifies the voltage level corresponding to the state of VID[5:0]. A ‘1’ in this table refers to a high voltage level and a ‘0’ refers to low voltage level. If the processor socket is empty (VID[5:0] = 111111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself. See the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775* for more details.

Table 2-1. Voltage Identification Definition

VID5	VID4	VID3	VID2	VID1	VID0	VID
1	0	1	1	0	1	1.5250
1	0	1	1	0	0	1.5500
1	0	1	0	1	1	1.5750
1	0	1	0	1	0	1.6000

2.4.1 Phase Lock Loop (PLL) Power and Filter

V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the Pentium 4 processor Extreme Edition in the 775-land package. Since these PLLs are analog, they require low noise power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{CC}.

Note: **The PLL filter for the Pentium 4 Extreme Edition in the 775-land package has been implemented inside the package. The VSSA, VCCA, and VCCIOPLL lands are not connected for this processor.** These signals are used for compatible processors. For further details, contact your Intel representative.

2.5 Reserved, Unused, and TESTHI Signals

All RESERVED signals must remain unconnected. Connection of these signals to V_{CC}, V_{SS}, $V_{TT,}$ or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Chapter 4 for a land listing of the processor and the location of all RESERVED signals.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. In a system level design, on-die termination has been included on the Pentium 4 processor Extreme Edition in the 775-land package to allow signals to be terminated within the processor silicon. Most unused GTL+ inputs should be left as no connects, as GTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected, however this may interfere with some test access port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused GTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors (R_{TT}). See Table 2-13.

TAP, GTL+ Asynchronous inputs, and GTL+ Asynchronous outputs do not include on-die termination. Inputs and used outputs must be terminated on the system board. Unused outputs may be terminated on the system board or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. For further information on termination for these signal types contact your Intel representative.

The TESTHI[12:1] signals must be tied to the processor’s appropriate power source (refer to the VTT_OUT_LEFT and VTT_OUT_RIGHT signal description in Chapter 4) using a matched resistor, where a matched resistor has a resistance value within 20% of the impedance of the board transmission line traces. For example, if the trace impedance is 60 Ω, a value between 48 Ω and 72 Ω is required. For TESTHI0 termination recommendations contact your Intel representative for further details and documentation.

The TESTHI signals may use individual pull-up resistors or be grouped together as detailed below. A matched resistor must be used for each group:

- TESTHI0 – cannot be grouped with other TESTHI signals
- TESTHI1 – cannot be grouped with other TESTHI signals
- TESTHI[7:2]
- TESTHI8 – cannot be grouped with other TESTHI signals
- TESTHI9 – cannot be grouped with other TESTHI signals
- TESTHI10 – cannot be grouped with other TESTHI signals
- TESTHI11 – cannot be grouped with other TESTHI signals
- TESTHI12 – cannot be grouped with other TESTHI signals

2.6 FSB Signal Groups

The FSB signals have been combined into groups by buffer type. GTL+ input signals have differential input buffers that use GTLREF0 as a reference level. In this document, the term "GTL+ Input" refers to the GTL+ input group as well as the GTL+ I/O group when receiving. Similarly, "GTL+ Output" refers to the GTL+ output group as well as the GTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals that are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 2-2 identifies which signals are common clock, source synchronous, and asynchronous.

Table 2-2. FSB Signal Groups

Signal Group	Type	Signals[1]
GTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
GTL+ Common Clock I/O	Synchronous to BCLK[1:0]	AP[1:0]#, ADS#, BINIT#, BNR#, BPM[5:0]#, BR0#, DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#
GTL+ Source Synchronous I/O	Synchronous to assoc. strobe	**Signals** **Associated Strobe** REQ[4:0]#, A[16:3]#[2], ADSTB0# A[35:17]#[2]ADSTB1# D[15:0]#, DBI0# DSTBP0#, DSTBN0# D[31:16]#, DBI1# DSTBP1#, DSTBN1# D[47:32]#, DBI2# DSTBP2#, DSTBN2# D[63:48]#, DBI3# DSTBP3#, DSTBN3#
GTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
GTL+Asynchronous Input		A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, STPCLK#
GTL+Asynchronous Output		FERR#/PBE#, IERR#, THERMTRIP#
GTL+ Asynchronous Input/ Output		PROCHOT#
TAP Input	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output	Synchronous to TCK	TDO
FSB Clock	Clock	BCLK[1:0], ITP_CLK[1:0][3]
Power/Other		VCC, VTT, VCCA, VCCIOPLL, VID[5:0], VSS, VSSA, GTLREF0, COMP[1:0], RESERVED, TESTHI[12:0], THERMDA, THERMDC, VCC_SENSE, VSS_SENSE, BSEL[2:0], SKTOCC#, DBR#[3], VTTPWRGD[4], PWRGOOD, VTT_SEL, LL_ID[1:0], GTLREF_SEL, VTT_OUT_LEFT, VTT_OUT_RIGHT

NOTES:

1. Refer to Section 4.2 for signal descriptions.
2. The value of these signals during the active-to-inactive edge of RESET# defines the processor configuration options. See Section 6.1 for details.
3. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
4. VTTPWRGD is not a feature of the Pentium 4 processor Extreme Edition in the 775-land package. This pin is included here for compatible processors. **VTTPWRGD is required for compatibility with *Voltage Regulator Down (VRD) 10.1 Design Guide* standards.**

2.7 GTL+ Asynchronous Signals

The Pentium 4 processor Extreme Edition in the 775-land package does not use CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, and STPCLK# use GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals (THERMTRIP#) use GTL+ output buffers. PROCHOT# uses a GTL+ input/output buffer. All of these signals follow the same DC requirements as AGTL+ signals; however, the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs for the processor to recognize them. See Section 2.11 for the DC characteristics for the Asynchronous GTL+ signal groups. See Section 6.2 for additional timing requirements for entering and leaving the low power states.

2.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Pentium 4 processor Extreme Edition in the 775-land package be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage level. Similar considerations must be made for TCK, TMS, TRST#, TDI, and TDO. Two copies of each signal may be required, with each driving a different voltage level.

2.9 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). Table 2-3 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All agents must operate at the same frequency.

The Pentium 4 processor Extreme Edition in the 775-land package currently operates at a 800 MHz FSB frequency (selected by a 200 MHz BCLK[1:0] frequency). Individual processors will only operate at their specified FSB frequency. For more information about these signals, refer to Section 4.2.

Table 2-3. BSEL[2:0] FSB Frequency Selections

BSEL2	BSEL1	BSEL0	Function
L	H	L	200 MHz
L	H	L	266 MHz

2.10 Absolute Maximum and Minimum Ratings

Table 2-4 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within the functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 2-4. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1,2]
V_{CC}	Core voltage with respect to V_{SS}	- 0.3	1.75	V	—
V_{TT}	Miscellaneous voltage supply	- 0.3	1.75	V	3
T_C	Processor case temperature	See Chapter 5	See Chapter 5	°C	
$T_{STORAGE}$	Processor storage temperature	–40	+85	°C	4, 5
V_{inGTL+}	GTL+ buffer DC input voltage with respect to V_{SS}	-0.1	1.75	V	—
$V_{inAsynch\_GTL+}$	Asynch GTL+ buffer DC input voltage with respect to V_{SS}	-0.1	1.75	V	—
I_{VID}	Max VID land current	—	5	mA	—

NOTES:

1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Refer to the *Voltage Regulator Down (VRD) 10.1 Design Guide* for more details on V_{TT} levels and how to implement current sink capabilities.
4. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, refer to the processor case temperature specifications.
5. This rating applies to the processor and does not include any tray or packaging.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core silicon and not at the package lands unless noted otherwise. See Chapter 4 for the signal definitions and signal assignments. Most of the signals on the processor FSB are in the GTL+ signal group. The DC specifications for these signals are listed in Table 2-7.

Previously, legacy signals and Test Access Port (TAP) signals to the processor used low-voltage CMOS buffer types. However, these interfaces now follow DC specifications similar to GTL+. The DC specifications for these signal groups are listed in Table 2-8 and Table 2-9.

Table 2-5 through Table 2-11 list the DC specifications for the Pentium 4 processor Extreme Edition in the 775-land package and are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 2-5. Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
VID range	VID	1.525	—	1.600	V	2
V_{CC}	V_{CC} for 775_VR_CONFIG_04B	See Table 2-6 and Figure 2-1.			V	3, 4, 5, 6
I_{CC}	I_{CC} for processor with multiple VID: 3.40 GHz 3.46 GHz	—	—	83.9 84.8	A	6, 7
I_{SGNT} I_{SLP}	I_{CC} Stop-Grant	—	—	40	A	8, 9
I_{TCC}	I_{CC} TCC active	—	—	I_{CC}	A	10
$I_{CC\ PLL}$	I_{CC} for PLL lands	—	—	60	mA	—
V_{TT}	Miscellaneous voltage supply	1.14	1.20	1.26	V	11, 12
VTT_OUT I_{CC}	DC current that may be drawn from VTT_OUT per pin	—	—	580	mA	—

NOTES:

1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range.
3. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.4 and Table 2-1 for more information.
4. The voltage specification requirements are measured across VCC_SENSE and VSS_SENSE lands at the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
5. Refer to Table 2-6 and Figure 2-1 for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_max} for a given current.
6. Adherence to this loadline specification for the processor is required to ensure reliable processor operation.
7. I_{CC_max} is specified at V_{CC_max}.
8. The current specified is also for AutoHALT State.
9. Icc Stop-Grant and Icc Sleep are specified at V_{CC_max}.
10. The maximum instantaneous current the processor will draw while the thermal control circuit is active as indicated by the assertion of PROCHOT# is the same as the maximum Icc for the processor.
11. V_{TT} must be provided via a separate voltage source and not connected to V_{CC}. This specification is measured at the land.
12. Baseboard bandwidth is limited to 20 MHz.

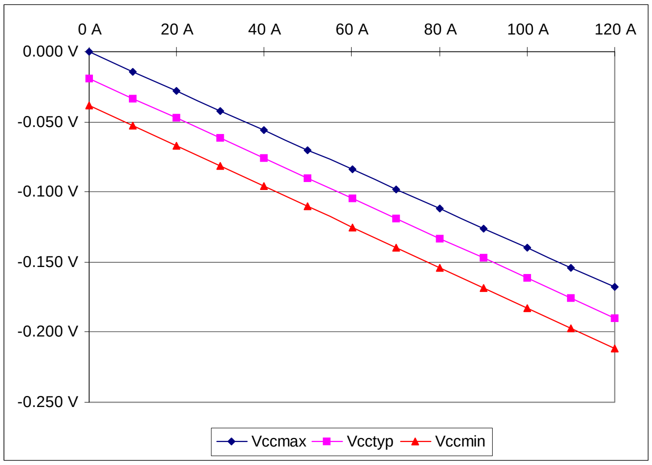
Table 2-6. V_{CC} Static and Transient Tolerance

Icc (A)	Voltage Deviation from VID Setting (V)[1, 2, 3, 4, 5]		
	Maximum Voltage	Typical Voltage	Minimum Voltage
0 A	0.000 V	-0.019 V	-0.038 V
10 A	-0.014 V	-0.033 V	-0.053 V
20 A	-0.028 V	-0.048 V	-0.067 V
30 A	-0.042 V	-0.062 V	-0.082 V
40 A	-0.056 V	-0.076 V	-0.096 V
50 A	-0.070 V	-0.090 V	-0.111 V
60 A	-0.084 V	-0.105 V	-0.125 V
70 A	-0.098 V	-0.119 V	-0.140 V
80 A	-0.112 V	-0.133 V	-0.154 V
90 A	-0.126 V	-0.147 V	-0.169 V
100 A	-0.140 V	-0.162 V	-0.183 V
110 A	-0.154 V	-0.176 V	-0.198 V
120 A	-0.168 V	-0.190 V	-0.212 V

NOTES:

1. The loadline specification includes both static and transient limits except for overshoot allowed as shown in Section 2.12.
2. This table is intended to aid in reading discrete points on Figure 2-1.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE lands. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS lands. Refer to the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775* for socket loadline guidelines and VR implementation details.
4. Adherence to this loadline specification for the processor is required to ensure reliable processor operation.
5. Loadline information: Vccmin = 1.45 mΩ, Vccmax = 1.40 mΩ, Tolerance = ±19 mV, Nominal design set point = VID - Tolerance.

Figure 2-1. V_{CC} Static and Transient Tolerance[1, 2, 3, 4]



NOTES:
1. The loadline specification includes both static and transient limits except for overshoot allowed as shown in Section 2.12.
2. This loadline specification shows the deviation from the VID set point.
3. The loadlines specify voltage limits at the die measured at the VCC_SENSE and VSS_SENSE lands. Voltage regulation feedback for voltage regulator circuits must be taken from processor VCC and VSS lands. Refer to the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775* for socket loadline guidelines and VR implementation details.
4. Adherence to this loadline specification for the processor is required to ensure reliable processor operation.

Table 2-7. GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
GTLREF0	Reference Voltage	$(0.0986V_{CC}+0.6106V_{TT}) – 10.21\%$	$(0.0986V_{CC}+0.6106V_{TT}) + 4.6\%$	V	2
V_{IH}	Input High Voltage	1.10*GTLREF0	V_{CC}	V	3,4
V_{IL}	Input Low Voltage	0.0	0.9*GTLREF0	V	4,5,6
V_{OH}	Output High Voltage	N/A	V_{CC}	V	4
I_{OL}	Output Low Current	N/A	50	mA	—
I_{HI}	Land Leakage High	N/A	100	µA	7
I_{LO}	Land Leakage Low	N/A	500	µA	8
R_{ON}	Buffer On Resistance	8.4	13.2	Ω	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and voltages.
2. This is the measured value after the processor is plugged into the platform. The typical GTLREF0 of $(0.0986V_{CC}+0.6106V_{TT})$ is based on V_{TT} of 1.2 V, V_{CC} of 1.575 V, and typical GTLREF0 resistor values on the platform.
3. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
4. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.
5. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
6. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications.
7. Leakage to V_{SS} with land held at V_{CC}.
8. Leakage to V_{CC} with land held at 300 mV.

Table 2-8. Asynchronous GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IH}	Input High Voltage, Asynch GTL+	1.10*GTLREF0	V_{CC}	V	2,3,4
V_{IL}	Input Low Voltage, Asynch. GTL+	0	0.9*GTLREF0	V	4
V_{OH}	Output High Voltage	N/A	V_{CC}	V	2,3,5
I_{OL}	Output Low Current	N/A	50	mA	6
I_{HI}	Land Leakage High	N/A	100	µA	7
I_{LO}	Land Leakage Low	N/A	500	µA	8
R_{ON}	Buffer On Resistance, Asynch GTL+	8.4	13.2	Ω	4

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and voltages.
2. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications.
3. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
4. This specification applies to the asynchronous GTL+ signal group.
5. All outputs are open-drain.
6. The maximum output current is based on maximum current handling capability of the buffer.
7. Leakage to V_{SS} with land held at V_{CC}.
8. Leakage to V_{CC} with land held at 300 mV.

Table 2-9. PWRGOOD and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{HYS}	Input Hysteresis	200	300	mV	2
V_{T+}	Input Low-to-High Threshold Voltage	$1/2*(V_{CC}+V_{HYS\_MIN})$	$1/2*(V_{CC}+V_{HYS\_MAX})$	V	3
V_{T-}	Input High-to-Low Threshold Voltage	$1/2*(V_{CC}–V_{HYS\_MAX})$	$1/2*(V_{CC}–V_{HYS\_MIN})$	V	3
V_{OH}	Output High Voltage	N/A	V_{CC}	V	3,4,5
I_{OL}	Output Low Current	N/A	40	mA	6
I_{HI}	Land Leakage High	N/A	100	µA	7
I_{LO}	Land Leakage Low	N/A	500	µA	8
R_{ON}	Buffer On Resistance	8.75	13.75	Ω	

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and voltages.
2. V_{HYS} represents the amount of hysteresis, nominally centered about 1/2 V_{CC} for all TAP inputs.
3. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
4. All outputs are open-drain.
5. The TAP signal group must comply with the signal quality specifications. Contact your Intel representative for further documentation.
6. The maximum output current is based on maximum current handling capability of the buffer.
7. Leakage to V_{SS} with land held at V_{CC}.
8. Leakage to V_{CC} with land held at 300 mV.

Table 2-10. VTTPWRGD DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{IL}	Input Low Voltage	—	—	0.3	V	
V_{IH}	Input High Voltage	0.9	—	—	V	

NOTES:

1. VTTPWRGD is not a feature of the Pentium 4 processor Extreme Edition in the 775-land package. This pin is used by compatible processors. **This pin is required for compatibility with *Voltage Regulator Down (VRD) 10.1 Design Guide* standards.**

Table 2-11. BSEL [2:0] and VID[5:0] DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
R_{ON} (BSEL)	Buffer On Resistance	9.2	14.3	Ω	2
R_{ON} (VID)	Buffer On Resistance	7.8	12.8	Ω	2
I_{HI}	Land Leakage Hi	N/A	100	µA	3

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and voltages.
2. These parameters are not tested and are based on design simulations.
3. Leakage to Vss with land held at 2.50 V.

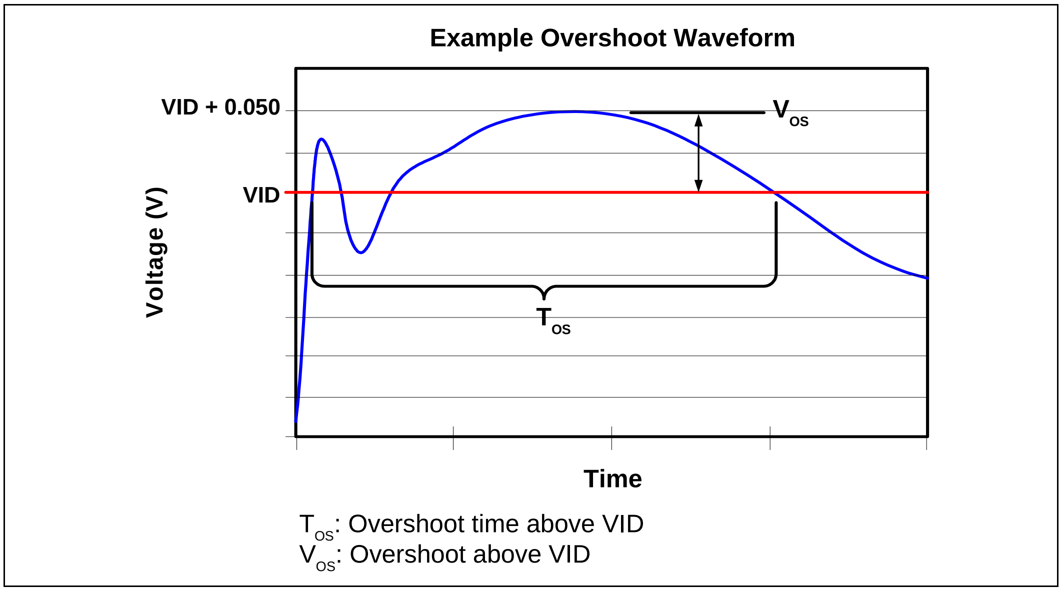
2.12 V_{CC} Overshoot Specification

The Pentium 4 processor Extreme Edition in the 775-land package can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V_{OS_MAX} where: V_{OS_MAX} is the maximum allowable overshoot voltage. The time duration of the overshoot event must not exceed T_{OS_MAX} where: T_{OS_MAX} is the maximum allowable time duration above VID. These specifications apply to the processor die voltage as measured across the VCC_SENSE and VSS_SENSE lands. Consult *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775* for proper application of the overshoot specification.

Table 2-12. V_{CC} Overshoot Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure
V_{os_max}	Magnitude of V_{CC} overshoot above VID	—	—	0.050	V	2-2
T_{os_max}	Time duration of V_{CC} overshoot above VID	—	—	25	µs	2-2

Figure 2-2. V_{CC} Overshoot Example Waveform



NOTES:

1. V_{OS} is measured overshoot voltage.
2. T_{OS} is measured time duration above VID.

2.12.1 Die Voltage Validation

Overshoot events from application testing on real processors must meet the specifications in Table 2-12 when measured across the VCC_SENSE and VSS_SENSE lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

2.13 GTL+FSB Specifications

Termination resistors are not required for most GTL+ signals, as these are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers that compare a signal’s voltage with a reference voltage called GTLREF0.

Table 2-13 lists the GTLREF0 specifications. The GTL+ reference voltage (GTLREF0) should be generated on the system board using high precision voltage divider circuits. For more details on platform design, contact your Intel representative.

Table 2-13. GTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
GTLREF0	Bus Reference Voltage	$(0.0986V_{CC}+0.6106V_{TT}) - 10.21\%$	$(0.0986V_{CC}+0.6106V_{TT})$	$(0.0986V_{CC}+0.6106V_{TT}) + 4.6\%$	V	2,3,4,5
R_{TT}	Termination Resistance	54	60	66	Ω	6
COMP[1:0]	COMP Resistance	59.8	60.4	61	Ω	7

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and voltages.
2. The tolerances for this specification have been stated generically to enable the system designer to calculate the minimum and maximum values across the range of V_{CC} and V_{TT}.
3. GTLREF0 should be generated from V_{CC} and V_{TT} by a voltage divider of 1% tolerance resistors or 1% tolerance, matched resistors. For implementation details, contact your Intel representative.
4. The V_{CC} and V_{TT} referred to in these specifications is the instantaneous V_{CC} and V_{TT}.
5. This is the measured value after the processor is plugged into the platform. The Typical GTLREF0 of $(0.0986V_{CC}+0.6106V_{TT})$ is based on V_{TT} of 1.2 V, V_{CC} of 1.575 V, and typical GTLREF0 resistor values on the platform.
6. R_{TT} is the on-die termination resistance measured at V_{OL} of the GTL+ output driver.
7. COMP resistance must be provided on the system board with 1% tolerance resistors. For implementation details, contact your Intel representative.

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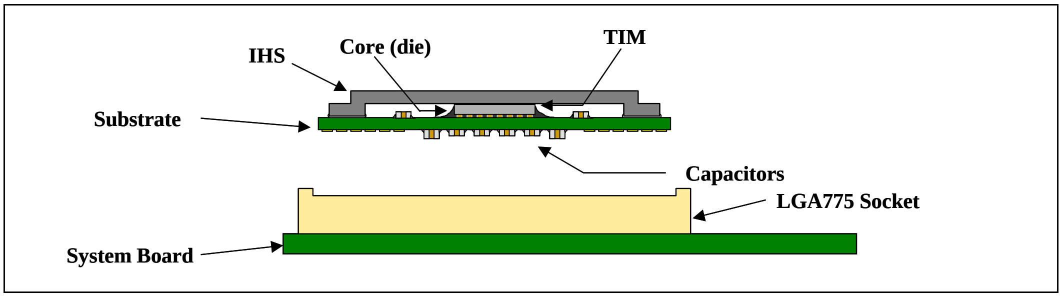
3 Package Mechanical Specifications

The Pentium 4 processor Extreme Edition in the 775-land package is packaged in a Flip-Chip Land Grid Array (FC-LGA4) package that interfaces with the motherboard via an LGA775 socket. The package consists of a processor core mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Figure 3-1 shows a sketch of the processor package components and how they are assembled together. Refer to the *LGA775 Socket Mechanical Design Guide* for complete details on the LGA775 socket.

The package components shown in Figure 3-1 include the following:

- Integrated Heat Spreader (IHS)
- Thermal Interface Material (TIM)
- Processor core (die)
- Package substrate
- Capacitors

Figure 3-1. Processor Package Assembly Sketch



NOTE:
1. Socket and motherboard are included for reference and are not part of processor package.

3.1 Package Mechanical Drawing

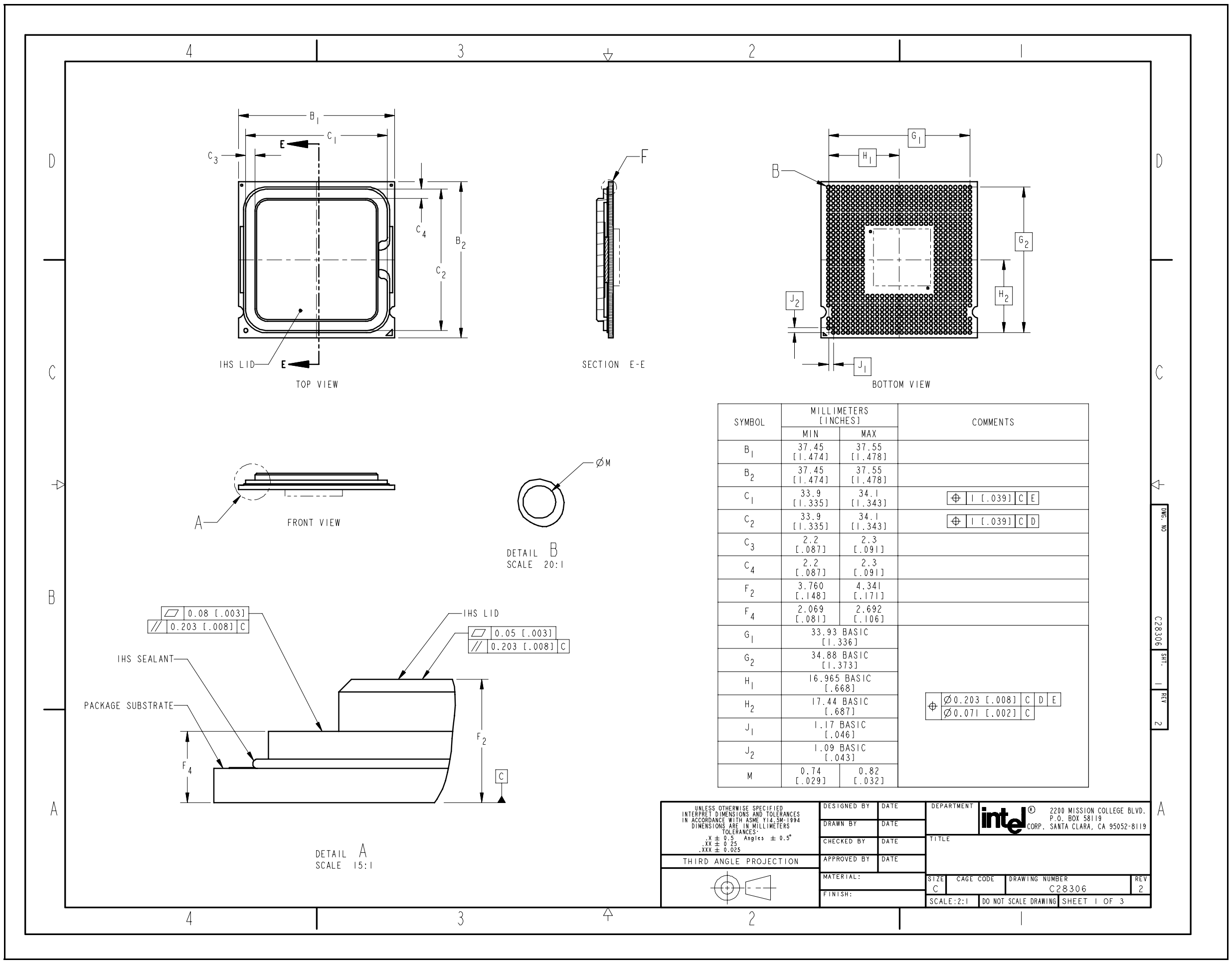
The package mechanical drawings are shown in Figure 3-2 through Figure 3-4. The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions include:

- Package reference with tolerances (total height, length, width, etc.)
- IHS parallelism and tilt
- Land dimensions
- Top-side and back-side component keep-out dimensions
- Reference datums

All drawing dimensions are in mm [in].

Note: **Guidelines on potential IHS flatness variation with socket load plate actuation and installation of the cooling solution is available in the processor thermal/mechanical design guidelines.**

Figure 3-2. Processor Package Drawing Sheet 1 of 3



SYMBOL	MILLIMETERS [INCHES] MIN	MILLIMETERS [INCHES] MAX	COMMENTS
B_1	37.45 [1.474]	37.55 [1.478]	
B_2	37.45 [1.474]	37.55 [1.478]	
C_1	33.9 [1.335]	34.1 [1.343]	⌖ 1 [.039] C E
C_2	33.9 [1.335]	34.1 [1.343]	⌖ 1 [.039] C D
C_3	2.2 [.087]	2.3 [.091]	
C_4	2.2 [.087]	2.3 [.091]	
F_2	3.760 [.148]	4.341 [.171]	
F_4	2.069 [.081]	2.692 [.106]	
G_1	33.93 BASIC [1.336]		⌖ Ø0.203 [.008] C D E Ø0.071 [.002] C
G_2	34.88 BASIC [1.373]		
H_1	16.965 BASIC [.668]		
H_2	17.44 BASIC [.687]		
J_1	1.17 BASIC [.046]		
J_2	1.09 BASIC [.043]		
M	0.74 [.029]	0.82 [.032]	

UNLESS OTHERWISE SPECIFIED
INTERPRET DIMENSIONS AND TOLERANCES
IN ACCORDANCE WITH ASME Y14.5M-1994
DIMENSIONS ARE IN MILLIMETERS
TOLERANCES:
.X ± 0.5 Angles ± 0.5°
.XX ± 0.25
.XXX ± 0.025

THIRD ANGLE PROJECTION

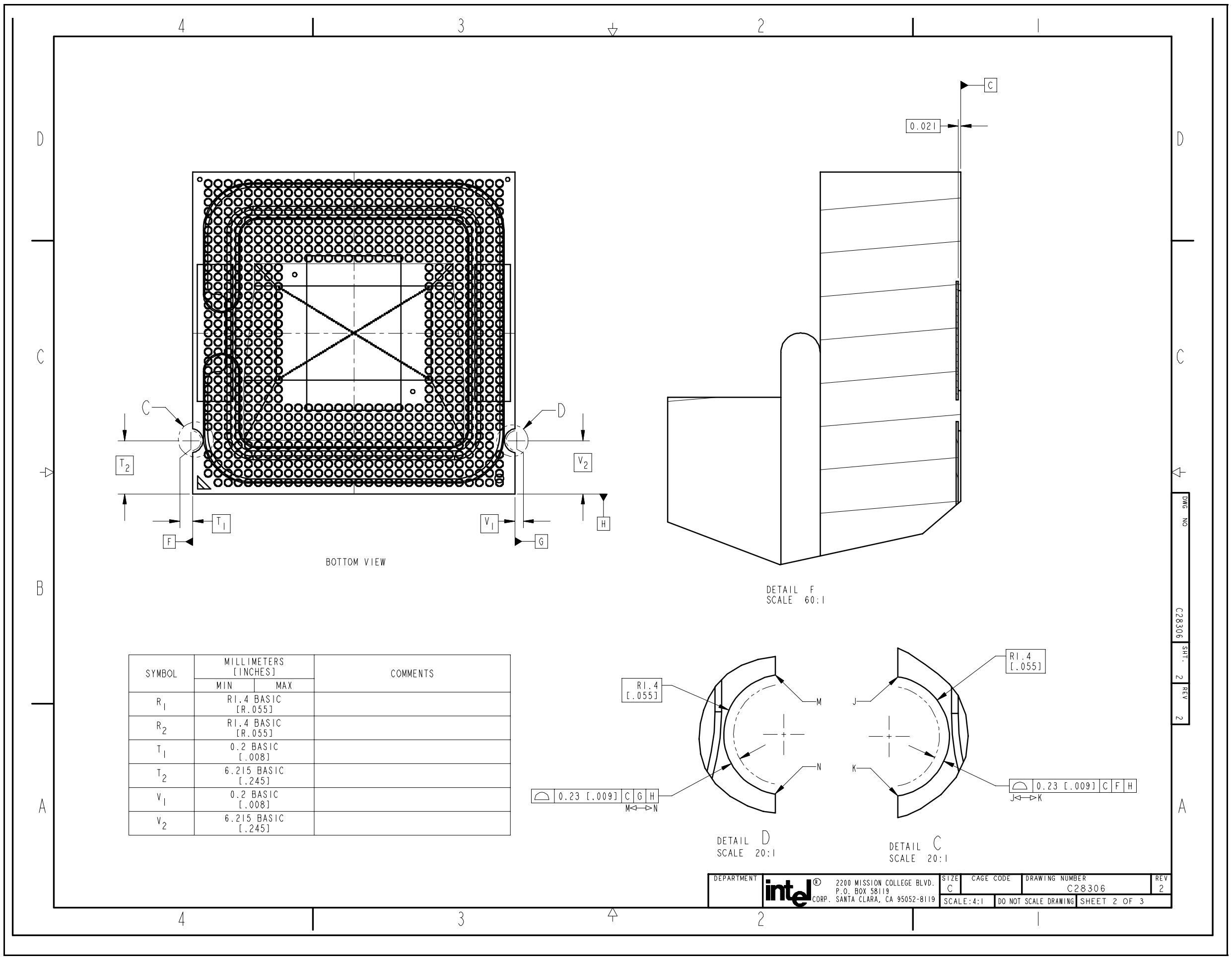
DESIGNED BY | DATE
DRAWN BY | DATE
CHECKED BY | DATE
APPROVED BY | DATE
MATERIAL:
FINISH:
DEPARTMENT

intel® CORP.
2200 MISSION COLLEGE BLVD.
P.O. BOX 58119
SANTA CLARA, CA 95052-8119

TITLE

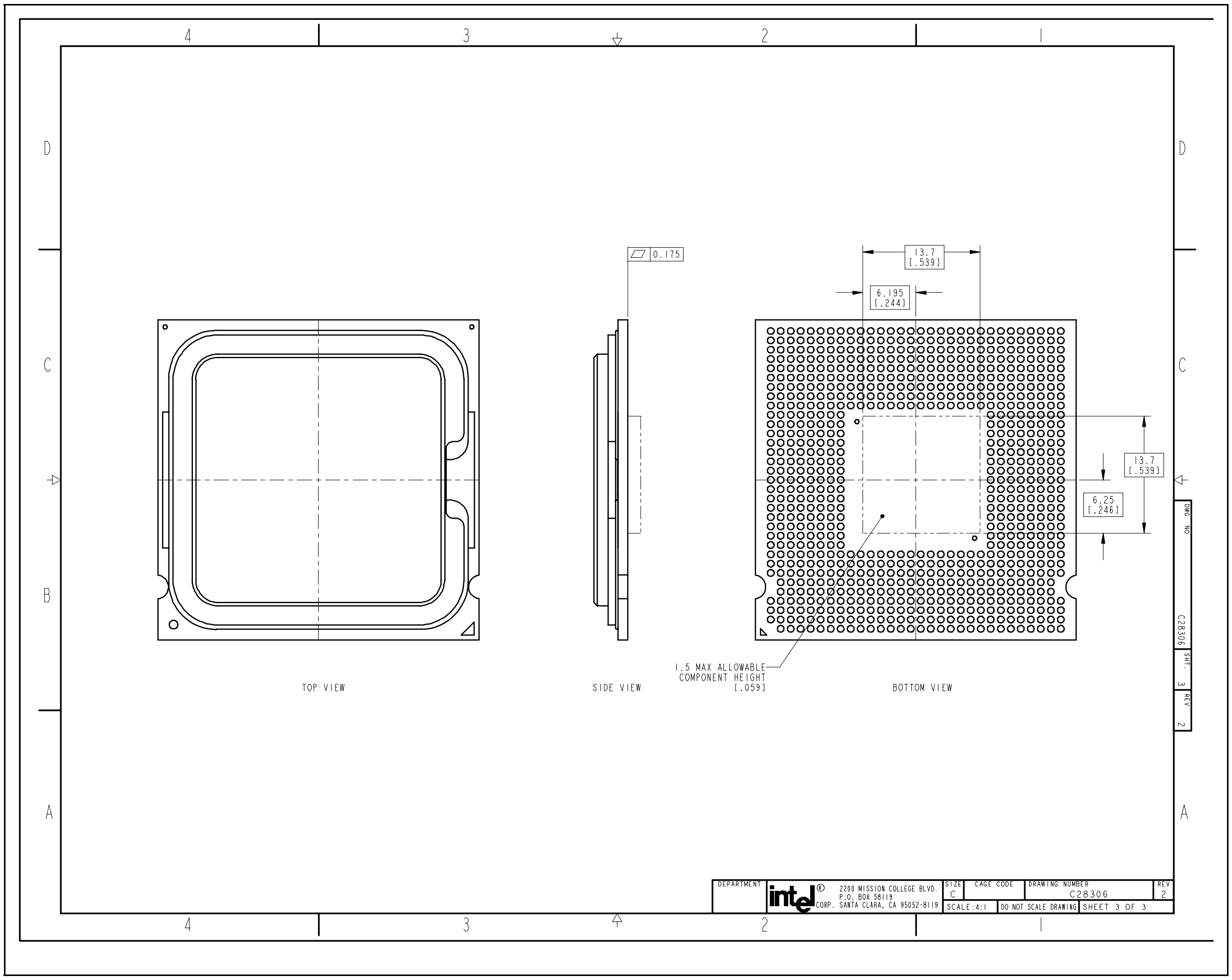
SIZE C | CAGE CODE | DRAWING NUMBER C28306 | REV 2
SCALE:2:1 | DO NOT SCALE DRAWING | SHEET 1 OF 3

Figure 3-3. Processor Package Drawing Sheet 2 of 3



SYMBOL	MILLIMETERS [INCHES]		COMMENTS
	MIN	MAX	
R_1	R1.4 BASIC [R.055]		
R_2	R1.4 BASIC [R.055]		
T_1	0.2 BASIC [.008]		
T_2	6.215 BASIC [.245]		
V_1	0.2 BASIC [.008]		
V_2	6.215 BASIC [.245]		

Figure 3-4. Processor Package Drawing Sheet 3 of 3



3.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted to either the topside or land-side of the package substrate. See Figure 3-4 for keep-out zones.

The location and quantity of package capacitors may change due to manufacturing efficiencies but will remain within the component keep-in.

3.3 Package Loading Specifications

Table 3-1 provides dynamic and static load specifications for the processor package. These mechanical maximum load limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Also, any mechanical system or component testing should not exceed the maximum limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solution. The minimum loading specification must be maintained by any thermal and mechanical solutions.

Table 3-1. Processor Loading Specifications

Parameter	Minimum	Maximum	Notes
Static	18 lbf	70 lbf	1, 2, 3
Dynamic	—	170 lbf	1, 3, 4

NOTES:

1. These specifications apply to uniform compressive loading in a direction normal to the processor IHS.
2. This is the maximum force that can be applied by a heatsink retention clip. The clip must also provide the minimum specified load on the processor package.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only and does not include the limits of the processor socket.
4. Dynamic loading is defined as the sum of the load on the package, from a 1 lb heatsink mass accelerating through an 11 ms trapezoidal pulse of 50 g, and the maximum static load.

3.4 Package Handling Guidelines

Table 3-2 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 3-2. Package Handling Guidelines

Parameter	Maximum Recommended	Notes
Shear	70 lbf	1, 4
Tensile	25 lbf	2, 4
Torque	35 lbf-in	3, 4

NOTES:

1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. A tensile load is defined as a pulling load applied to the IHS in a direction normal to the IHS surface.
3. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.
4. These guidelines are based on limited testing for design characterization.

3.5 Package Insertion Specifications

The Pentium 4 processor Extreme Edition in the 775-land package can be inserted into and removed from a LGA775 socket 15 times. The socket should meet the LGA775 requirements. For more details contact your Intel representative.

3.6 Processor Mass Specification

The typical mass of the Pentium 4 processor Extreme Edition in the 775-land package is 21.5 g [0.76 oz]. This mass [weight] includes all the components that are included in the package.

3.7 Processor Materials

Table 3-3 lists some of the package components and associated materials.

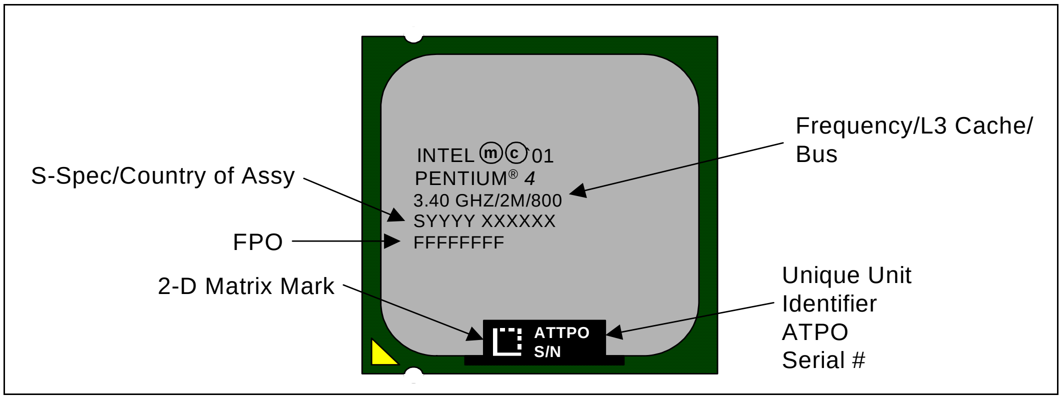
Table 3-3. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Fiber Reinforced Resin
Substrate Lands	Gold Plated Copper

3.8 Processor Markings

Figure 3-5 shows the topside markings on the processor. These diagrams are to aid in the identification of the Pentium 4 processor Extreme Edition in the 775-land package.

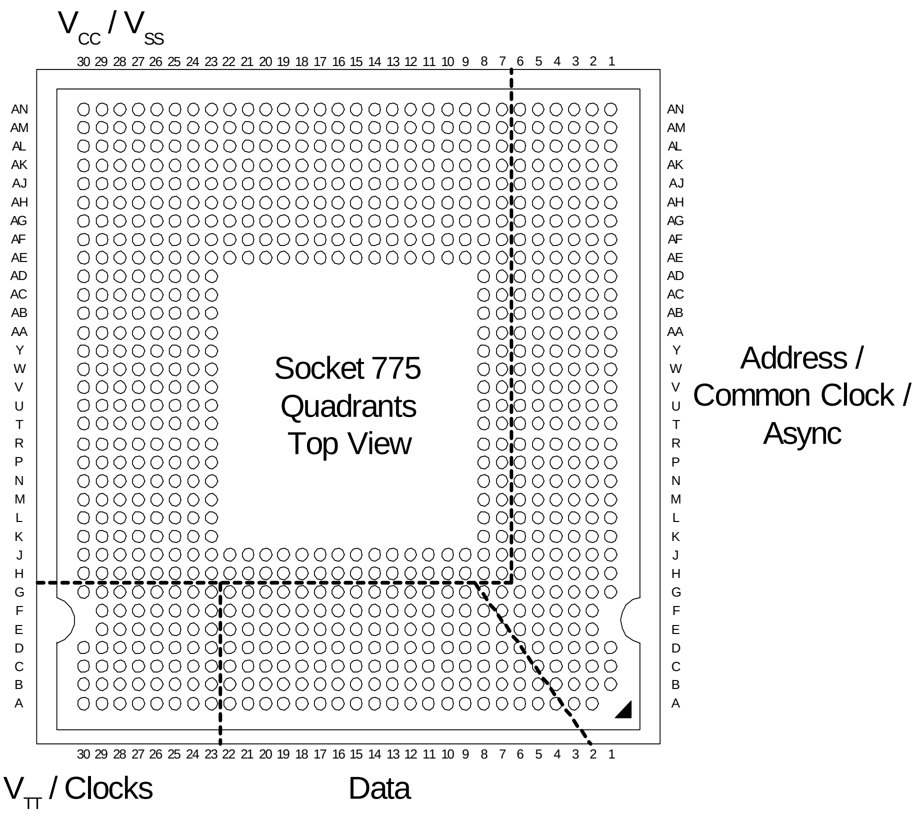
Figure 3-5. Processor Top-Side Markings



3.9 Processor Land Coordinates

Figure 3-6 shows the top view of the processor land coordinates. The coordinates are referred to throughout the document to identify processor lands.

Figure 3-6. Processor Land Coordinates (Top View)



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4 Land Listing and Signal Descriptions

This chapter provides the processor land assignment and signal descriptions.

4.1 Processor Land Assignments

This section contains the land listings for the Pentium 4 processor Extreme Edition in the 775-land package. The landout footprint is shown in Figure 4-1 and Figure 4-2. These figures represent the landout arranged by land number and they show the physical location of each signal on the package land array (top view). Table 4-1 is a listing of all processor lands ordered alphabetically by land (signal) name. Table 4-2 is also a listing of all processor lands; the ordering is by land number.

Figure 4-1. Landout Diagram (Top View – Left Side)

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15
AN	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AM	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AL	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AK	VSS	VSS	VSS	VSS	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AJ	VSS	VSS	VSS	VSS	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AH	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AG	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AF	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC	VCC	VCC	VSS	VCC	VCC	VSS	VSS	VCC
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AB	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
Y	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
W	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
U	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
T	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
R	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
P	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
N	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
M	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
L	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
K	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
J	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	DP3#	DP0#	VCC
H	BSEL1	GTLREF_SEL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	DP2#	DP1#
G	BSEL2	BSEL0	BCLK1	TESTHI4	TESTHI5	TESTHI3	TESTHI6	RESET#	D47#	D44#	DSTBN2#	DSTBP2#	D35#	D36#	D32#	D31#
F		RSVD	BCLK0	VTT_SEL	TESTHI0	TESTHI2	TESTHI7	RSVD	VSS	D43#	D41#	VSS	D38#	D37#	VSS	D30#
E		VSS	VSS	VSS	VSS	VSS	FC10	RSVD	D45#	D42#	VSS	D40#	D39#	VSS	D34#	D33#
D	VTT	VTT	VTT	VTT	VTT	VTT	VSS	FC9	D46#	VSS	D48#	DBI2#	VSS	D49#	RSVD	VSS
C	VTT	VTT	VTT	VTT	VTT	VTT	VSS	VCCIOPLL	VSS	D58#	DBI3#	VSS	D54#	DSTBP3#	VSS	D51#
B	VTT	VTT	VTT	VTT	VTT	VTT	VSS	VSSA	D63#	D59#	VSS	D60#	D57#	VSS	D55#	D53#
A	VTT	VTT	VTT	VTT	VTT	VTT	VSS	VCCA	D62#	VSS	RSVD	D61#	VSS	D56#	DSTBN3#	VSS
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15

Figure 4-2. Landout Diagram (Top View – Right Side)

14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VCC	VSS	VCC	VCC	VSS	VCC	VCC	FC16	VSS_MB_ REGULATION	VCC_MB_ REGULATION	VSS_ SENSE	VCC_ SENSE	VSS	VSS	AN
VCC	VSS	VCC	VCC	VSS	VCC	VCC	FC12	VTTPWRGD	FC11	VSS	VID2	VID0	VSS	AM
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VID3	VID1	VID5	VSS	PROCHOT#	THERMDA	AL
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	FC8	VSS	VID4	ITP_CLK0	VSS	THERMDC	AK
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	A35#	A34#	VSS	ITP_CLK1	BPM0#	BPM1#	AJ
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	A33#	A32#	VSS	RSVD	VSS	AH
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	A29#	A31#	A30#	BPM5#	BPM3#	TRST#	AG
VCC	VSS	VCC	VCC	VSS	VCC	VCC	VSS	VSS	A27#	A28#	VSS	BPM4#	TDO	AF
VCC	VSS	VCC	VCC	VSS	VCC	SKTOCC#	VSS	RSVD	VSS	RSVD	RSVD	VSS	TCK	AE
						VCC	VSS	A22#	ADSTB1#	VSS	BINIT#	BPM2#	TDI	AD
						VCC	VSS	VSS	A25#	RSVD	VSS	DBR#	TMS	AC
						VCC	VSS	A17#	A24#	A26#	MCERR#	IERR#	VSS	AB
						VCC	VSS	VSS	A23#	A21#	VSS	LL_ID1	VTT_OUT_ RIGHT	AA
						VCC	VSS	A19#	VSS	A20#	RSVD	VSS	FC0	Y
						VCC	VSS	A18#	A16#	VSS	TESTHI1	TESTHI12	FC13	W
						VCC	VSS	VSS	A14#	A15#	VSS	LL_ID0	FC14	V
						VCC	VSS	A10#	A12#	A13#	AP1#	AP0#	VSS	U
						VCC	VSS	VSS	A9#	A11#	VSS	FC4	COMP1	T
						VCC	VSS	ADSTB0#	VSS	A8#	FERR#/ PBE#	VSS	FC2	R
						VCC	VSS	A4#	RSVD	VSS	INIT#	SMI#	TESTHI11	P
						VCC	VSS	VSS	RSVD	RSVD	VSS	IGNNE#	PWRGOOD	N
						VCC	VSS	REQ2#	A5#	A7#	STPCLK#	THER- MTRIP#	VSS	M
						VCC	VSS	VSS	A3#	A6#	VSS	SLP#	LINT1	L
						VCC	VSS	REQ3#	VSS	REQ0#	A20M#	VSS	LINT0	K
VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	REQ4#	REQ1#	VSS	RSVD	FC3	VTT_OUT_ LEFT	J
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	TESTHI10	RSP#	VSS	FC6	GTLREF0	H
D29#	D27#	DSTBN1#	DBI1#	RSVD	D16#	BPRI#	DEFER#	RSVD	FC7	TESTHI9	TESTHI8	FC1	VSS	G
D28#	VSS	D24#	D23#	VSS	D18#	D17#	VSS	RSVD	RS1#	VSS	BR0#	FC5		F
VSS	D26#	DSTBP1#	VSS	D21#	D19#	VSS	RSVD	RSVD	RSVD	HITM#	TRDY#	VSS		E
RSVD	D25#	VSS	D15#	D22#	VSS	D12#	D20#	VSS	VSS	HIT#	VSS	ADS#	RSVD	D
D52#	VSS	D14#	D11#	VSS	RSVD	DSTBN0#	VSS	D3#	D1#	VSS	LOCK#	BNR#	DRDY#	C
VSS	RSVD	D13#	VSS	D10#	DSTBP0#	VSS	D6#	D5#	VSS	D0#	RS0#	DBSY#	VSS	B
D50#	COMP0	VSS	D9#	D8#	VSS	DBI0#	D7#	VSS	D4#	D2#	RS2#	VSS		A
14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
A3#	L5	Source Synch	Input/Output
A4#	P6	Source Synch	Input/Output
A5#	M5	Source Synch	Input/Output
A6#	L4	Source Synch	Input/Output
A7#	M4	Source Synch	Input/Output
A8#	R4	Source Synch	Input/Output
A9#	T5	Source Synch	Input/Output
A10#	U6	Source Synch	Input/Output
A11#	T4	Source Synch	Input/Output
A12#	U5	Source Synch	Input/Output
A13#	U4	Source Synch	Input/Output
A14#	V5	Source Synch	Input/Output
A15#	V4	Source Synch	Input/Output
A16#	W5	Source Synch	Input/Output
A17#	AB6	Source Synch	Input/Output
A18#	W6	Source Synch	Input/Output
A19#	Y6	Source Synch	Input/Output
A20#	Y4	Source Synch	Input/Output
A20M#	K3	Asynch GTL+	Input
A21#	AA4	Source Synch	Input/Output
A22#	AD6	Source Synch	Input/Output
A23#	AA5	Source Synch	Input/Output
A24#	AB5	Source Synch	Input/Output
A25#	AC5	Source Synch	Input/Output
A26#	AB4	Source Synch	Input/Output
A27#	AF5	Source Synch	Input/Output
A28#	AF4	Source Synch	Input/Output
A29#	AG6	Source Synch	Input/Output
A30#	AG4	Source Synch	Input/Output
A31#	AG5	Source Synch	Input/Output
A32#	AH4	Source Synch	Input/Output
A33#	AH5	Source Synch	Input/Output
A34#	AJ5	Source Synch	Input/Output
A35#	AJ6	Source Synch	Input/Output
ADS#	D2	Common Clock	Input/Output
ADSTB0#	R6	Source Synch	Input/Output
ADSTB1#	AD5	Source Synch	Input/Output
AP0#	U2	Common Clock	Input/Output
AP1#	U3	Common Clock	Input/Output
BCLK0	F28	Clock	Input

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
BCLK1	G28	Clock	Input
BINIT#	AD3	Common Clock	Input/Output
BNR#	C2	Common Clock	Input/Output
BPM0#	AJ2	Common Clock	Input/Output
BPM1#	AJ1	Common Clock	Input/Output
BPM2#	AD2	Common Clock	Input/Output
BPM3#	AG2	Common Clock	Input/Output
BPM4#	AF2	Common Clock	Input/Output
BPM5#	AG3	Common Clock	Input/Output
BPRI#	G8	Common Clock	Input
BR0#	F3	Common Clock	Input/Output
BSEL0	G29	Power/Other	Output
BSEL1	H30	Power/Other	Output
BSEL2	G30	Power/Other	Output
COMP0	A13	Power/Other	Input
COMP1	T1	Power/Other	Input
D0#	B4	Source Synch	Input/Output
D1#	C5	Source Synch	Input/Output
D2#	A4	Source Synch	Input/Output
D3#	C6	Source Synch	Input/Output
D4#	A5	Source Synch	Input/Output
D5#	B6	Source Synch	Input/Output
D6#	B7	Source Synch	Input/Output
D7#	A7	Source Synch	Input/Output
D8#	A10	Source Synch	Input/Output
D9#	A11	Source Synch	Input/Output
D10#	B10	Source Synch	Input/Output
D11#	C11	Source Synch	Input/Output
D12#	D8	Source Synch	Input/Output
D13#	B12	Source Synch	Input/Output
D14#	C12	Source Synch	Input/Output
D15#	D11	Source Synch	Input/Output
D16#	G9	Source Synch	Input/Output
D17#	F8	Source Synch	Input/Output
D18#	F9	Source Synch	Input/Output
D19#	E9	Source Synch	Input/Output
D20#	D7	Source Synch	Input/Output
D21#	E10	Source Synch	Input/Output
D22#	D10	Source Synch	Input/Output
D23#	F11	Source Synch	Input/Output

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
D24#	F12	Source Synch	Input/Output
D25#	D13	Source Synch	Input/Output
D26#	E13	Source Synch	Input/Output
D27#	G13	Source Synch	Input/Output
D28#	F14	Source Synch	Input/Output
D29#	G14	Source Synch	Input/Output
D30#	F15	Source Synch	Input/Output
D31#	G15	Source Synch	Input/Output
D32#	G16	Source Synch	Input/Output
D33#	E15	Source Synch	Input/Output
D34#	E16	Source Synch	Input/Output
D35#	G18	Source Synch	Input/Output
D36#	G17	Source Synch	Input/Output
D37#	F17	Source Synch	Input/Output
D38#	F18	Source Synch	Input/Output
D39#	E18	Source Synch	Input/Output
D40#	E19	Source Synch	Input/Output
D41#	F20	Source Synch	Input/Output
D42#	E21	Source Synch	Input/Output
D43#	F21	Source Synch	Input/Output
D44#	G21	Source Synch	Input/Output
D45#	E22	Source Synch	Input/Output
D46#	D22	Source Synch	Input/Output
D47#	G22	Source Synch	Input/Output
D48#	D20	Source Synch	Input/Output
D49#	D17	Source Synch	Input/Output
D50#	A14	Source Synch	Input/Output
D51#	C15	Source Synch	Input/Output
D52#	C14	Source Synch	Input/Output
D53#	B15	Source Synch	Input/Output
D54#	C18	Source Synch	Input/Output
D55#	B16	Source Synch	Input/Output
D56#	A17	Source Synch	Input/Output
D57#	B18	Source Synch	Input/Output
D58#	C21	Source Synch	Input/Output
D59#	B21	Source Synch	Input/Output
D60#	B19	Source Synch	Input/Output
D61#	A19	Source Synch	Input/Output
D62#	A22	Source Synch	Input/Output
D63#	B22	Source Synch	Input/Output

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
DBI0#	A8	Source Synch	Input/Output
DBI1#	G11	Source Synch	Input/Output
DBI2#	D19	Source Synch	Input/Output
DBI3#	C20	Source Synch	Input/Output
DBR#	AC2	Power/Other	Output
DBSY#	B2	Common Clock	Input/Output
DEFER#	G7	Common Clock	Input
DP0#	J16	Common Clock	Input/Output
DP1#	H15	Common Clock	Input/Output
DP2#	H16	Common Clock	Input/Output
DP3#	J17	Common Clock	Input/Output
DRDY#	C1	Common Clock	Input/Output
DSTBN0#	C8	Source Synch	Input/Output
DSTBN1#	G12	Source Synch	Input/Output
DSTBN2#	G20	Source Synch	Input/Output
DSTBN3#	A16	Source Synch	Input/Output
DSTBP0#	B9	Source Synch	Input/Output
DSTBP1#	E12	Source Synch	Input/Output
DSTBP2#	G19	Source Synch	Input/Output
DSTBP3#	C17	Source Synch	Input/Output
FC0	Y1	Other	
FC1	G2	Other	
FC2	R1	Other	
FC3	J2	Other	
FC4	T2	Other	
FC5	F2	Other	
FC6	H2	Other	
FC7	G5	Other	
FC8	AK6	Other	
FC9	D23	Other	
FC10	E24	Other	
FC11	AM5	Other	
FC12	AM7	Other	
FC13	W1	Other	
FC14	V1	Other	
FC16	AN7	Other	
FERR#/PBE#	R3	Asynch GTL+	Output
GTLREF_SEL	H29	Power/Other	Output
GTLREF0	H1	Power/Other	Input
HIT#	D4	Common Clock	Input/Output

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
HITM#	E4	Common Clock	Input/Output
IERR#	AB2	Asynch GTL+	Output
IGNNE#	N2	Asynch GTL+	Input
INIT#	P3	Asynch GTL+	Input
ITP_CLK0	AK3	TAP	Input
ITP_CLK1	AJ3	TAP	Input
LINT0	K1	Asynch GTL+	Input
LINT1	L1	Asynch GTL+	Input
LL_ID0	V2	Power/Other	Output
LL_ID1	AA2	Power/Other	Output
LOCK#	C3	Common Clock	Input/Output
MCERR#	AB3	Common Clock	Input/Output
PROCHOT#	AL2	Asynch GTL+	Input/Output
PWRGOOD	N1	Power/Other	Input
REQ0#	K4	Source Synch	Input/Output
REQ1#	J5	Source Synch	Input/Output
REQ2#	M6	Source Synch	Input/Output
REQ3#	K6	Source Synch	Input/Output
REQ4#	J6	Source Synch	Input/Output
RESERVED	A20		
RESERVED	AC4		
RESERVED	AE3		
RESERVED	AE4		
RESERVED	AE6		
RESERVED	AH2		
RESERVED	C9		
RESERVED	D1		
RESERVED	D14		
RESERVED	D16		
RESERVED	E23		
RESERVED	E5		
RESERVED	E6		
RESERVED	E7		
RESERVED	F23		
RESERVED	F29		
RESERVED	F6		
RESERVED	G10		
RESERVED	B13		
RESERVED	J3		
RESERVED	N4		

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
RESERVED	N5		
RESERVED	P5		
RESERVED	Y3		
RESERVED	G6		
RESET#	G23	Common Clock	Input
RS0#	B3	Common Clock	Input
RS1#	F5	Common Clock	Input
RS2#	A3	Common Clock	Input
RSP#	H4	Common Clock	Input
SKTOCC#	AE8	Power/Other	Output
SLP#	L2	Asynch GTL+	Input
SMI#	P2	Asynch GTL+	Input
STPCLK#	M3	Asynch GTL+	Input
TCK	AE1	TAP	Input
TDI	AD1	TAP	Input
TDO	AF1	TAP	Output
TESTHI0	F26	Power/Other	Input
TESTHI1	W3	Power/Other	Input
TESTHI2	F25	Power/Other	Input
TESTHI3	G25	Power/Other	Input
TESTHI4	G27	Power/Other	Input
TESTHI5	G26	Power/Other	Input
TESTHI6	G24	Power/Other	Input
TESTHI7	F24	Power/Other	Input
TESTHI8	G3	Power/Other	Input
TESTHI9	G4	Power/Other	Input
TESTHI10	H5	Power/Other	Input
TESTHI11	P1	Power/Other	Input
TESTHI12	W2	Power/Other	Input
THERMDA	AL1	Power/Other	
THERMDC	AK1	Power/Other	
THERMTRIP#	M2	Asynch GTL+	Output
TMS	AC1	TAP	Input
TRDY#	E3	Common Clock	Input
TRST#	AG1	TAP	Input
VCC	AA8	Power/Other	
VCC	AB8	Power/Other	
VCC	AC23	Power/Other	
VCC	AC24	Power/Other	
VCC	AC25	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VCC	AC26	Power/Other	
VCC	AC27	Power/Other	
VCC	AC28	Power/Other	
VCC	AC29	Power/Other	
VCC	AC30	Power/Other	
VCC	AC8	Power/Other	
VCC	AD23	Power/Other	
VCC	AD24	Power/Other	
VCC	AD25	Power/Other	
VCC	AD26	Power/Other	
VCC	AD27	Power/Other	
VCC	AD28	Power/Other	
VCC	AD29	Power/Other	
VCC	AD30	Power/Other	
VCC	AD8	Power/Other	
VCC	AE11	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE15	Power/Other	
VCC	AE18	Power/Other	
VCC	AE19	Power/Other	
VCC	AE21	Power/Other	
VCC	AE22	Power/Other	
VCC	AE23	Power/Other	
VCC	AE9	Power/Other	
VCC	AF11	Power/Other	
VCC	AF12	Power/Other	
VCC	AF14	Power/Other	
VCC	AF15	Power/Other	
VCC	AF18	Power/Other	
VCC	AF19	Power/Other	
VCC	AF21	Power/Other	
VCC	AF22	Power/Other	
VCC	AF8	Power/Other	
VCC	AF9	Power/Other	
VCC	AG11	Power/Other	
VCC	AG12	Power/Other	
VCC	AG14	Power/Other	
VCC	AG15	Power/Other	
VCC	AG18	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VCC	AG19	Power/Other	
VCC	AG21	Power/Other	
VCC	AG22	Power/Other	
VCC	AG25	Power/Other	
VCC	AG26	Power/Other	
VCC	AG27	Power/Other	
VCC	AG28	Power/Other	
VCC	AG29	Power/Other	
VCC	AG30	Power/Other	
VCC	AG8	Power/Other	
VCC	AG9	Power/Other	
VCC	AH11	Power/Other	
VCC	AH12	Power/Other	
VCC	AH14	Power/Other	
VCC	AH15	Power/Other	
VCC	AH18	Power/Other	
VCC	AH19	Power/Other	
VCC	AH21	Power/Other	
VCC	AH22	Power/Other	
VCC	AH25	Power/Other	
VCC	AH26	Power/Other	
VCC	AH27	Power/Other	
VCC	AH28	Power/Other	
VCC	AH29	Power/Other	
VCC	AH30	Power/Other	
VCC	AH8	Power/Other	
VCC	AH9	Power/Other	
VCC	AJ11	Power/Other	
VCC	AJ12	Power/Other	
VCC	AJ14	Power/Other	
VCC	AJ15	Power/Other	
VCC	AJ18	Power/Other	
VCC	AJ19	Power/Other	
VCC	AJ21	Power/Other	
VCC	AJ22	Power/Other	
VCC	AJ25	Power/Other	
VCC	AJ26	Power/Other	
VCC	AJ8	Power/Other	
VCC	AJ9	Power/Other	
VCC	AK11	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VCC	AK12	Power/Other	
VCC	AK14	Power/Other	
VCC	AK15	Power/Other	
VCC	AK18	Power/Other	
VCC	AK19	Power/Other	
VCC	AK21	Power/Other	
VCC	AK22	Power/Other	
VCC	AK25	Power/Other	
VCC	AK26	Power/Other	
VCC	AK8	Power/Other	
VCC	AK9	Power/Other	
VCC	AL11	Power/Other	
VCC	AL12	Power/Other	
VCC	AL14	Power/Other	
VCC	AL15	Power/Other	
VCC	AL18	Power/Other	
VCC	AL19	Power/Other	
VCC	AL21	Power/Other	
VCC	AL22	Power/Other	
VCC	AL25	Power/Other	
VCC	AL26	Power/Other	
VCC	AL29	Power/Other	
VCC	AL30	Power/Other	
VCC	AL8	Power/Other	
VCC	AL9	Power/Other	
VCC	AM11	Power/Other	
VCC	AM12	Power/Other	
VCC	AM14	Power/Other	
VCC	AM15	Power/Other	
VCC	AM18	Power/Other	
VCC	AM19	Power/Other	
VCC	AM21	Power/Other	
VCC	AM22	Power/Other	
VCC	AM25	Power/Other	
VCC	AM26	Power/Other	
VCC	AM29	Power/Other	
VCC	AM30	Power/Other	
VCC	AM8	Power/Other	
VCC	AM9	Power/Other	
VCC	AN11	Power/Other	
VCC	AN12	Power/Other	
VCC	AN14	Power/Other	
VCC	AN15	Power/Other	
VCC	AN18	Power/Other	
VCC	AN19	Power/Other	
VCC	AN21	Power/Other	
VCC	AN22	Power/Other	
VCC	AN25	Power/Other	
VCC	AN26	Power/Other	
VCC	AN29	Power/Other	
VCC	AN30	Power/Other	
VCC	AN8	Power/Other	
VCC	AN9	Power/Other	
VCC	J10	Power/Other	
VCC	J11	Power/Other	
VCC	J12	Power/Other	
VCC	J13	Power/Other	
VCC	J14	Power/Other	
VCC	J15	Power/Other	
VCC	J18	Power/Other	
VCC	J19	Power/Other	
VCC	J20	Power/Other	
VCC	J21	Power/Other	
VCC	J22	Power/Other	
VCC	J23	Power/Other	
VCC	J24	Power/Other	
VCC	J25	Power/Other	
VCC	J26	Power/Other	
VCC	J27	Power/Other	
VCC	J28	Power/Other	
VCC	J29	Power/Other	
VCC	J30	Power/Other	
VCC	J8	Power/Other	
VCC	J9	Power/Other	
VCC	K23	Power/Other	
VCC	K24	Power/Other	
VCC	K25	Power/Other	
VCC	K26	Power/Other	
VCC	K27	Power/Other	
VCC	K28	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VCC	K29	Power/Other	
VCC	K30	Power/Other	
VCC	K8	Power/Other	
VCC	L8	Power/Other	
VCC	M23	Power/Other	
VCC	M24	Power/Other	
VCC	M25	Power/Other	
VCC	M26	Power/Other	
VCC	M27	Power/Other	
VCC	M28	Power/Other	
VCC	M29	Power/Other	
VCC	M30	Power/Other	
VCC	M8	Power/Other	
VCC	N23	Power/Other	
VCC	N24	Power/Other	
VCC	N25	Power/Other	
VCC	N26	Power/Other	
VCC	N27	Power/Other	
VCC	N28	Power/Other	
VCC	N29	Power/Other	
VCC	N30	Power/Other	
VCC	N8	Power/Other	
VCC	P8	Power/Other	
VCC	R8	Power/Other	
VCC	T23	Power/Other	
VCC	T24	Power/Other	
VCC	T25	Power/Other	
VCC	T26	Power/Other	
VCC	T27	Power/Other	
VCC	T28	Power/Other	
VCC	T29	Power/Other	
VCC	T30	Power/Other	
VCC	T8	Power/Other	
VCC	U23	Power/Other	
VCC	U24	Power/Other	
VCC	U25	Power/Other	
VCC	U26	Power/Other	
VCC	U27	Power/Other	
VCC	U28	Power/Other	
VCC	U29	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VCC	U30	Power/Other	
VCC	U8	Power/Other	
VCC	V8	Power/Other	
VCC	W23	Power/Other	
VCC	W24	Power/Other	
VCC	W25	Power/Other	
VCC	W26	Power/Other	
VCC	W27	Power/Other	
VCC	W28	Power/Other	
VCC	W29	Power/Other	
VCC	W30	Power/Other	
VCC	W8	Power/Other	
VCC	Y23	Power/Other	
VCC	Y24	Power/Other	
VCC	Y25	Power/Other	
VCC	Y26	Power/Other	
VCC	Y27	Power/Other	
VCC	Y28	Power/Other	
VCC	Y29	Power/Other	
VCC	Y30	Power/Other	
VCC	Y8	Power/Other	
VCC_MB_REGULATION	AN5	Power/Other	Output
VCC_SENSE	AN3	Power/Other	Output
VCCA	A23	Power/Other	
VCCIOPLL	C23	Power/Other	
VID0	AM2	Power/Other	Output
VID1	AL5	Power/Other	Output
VID2	AM3	Power/Other	Output
VID3	AL6	Power/Other	Output
VID4	AK4	Power/Other	Output
VID5	AL4	Power/Other	Output
VSS	A12	Power/Other	
VSS	A15	Power/Other	
VSS	A18	Power/Other	
VSS	A2	Power/Other	
VSS	A21	Power/Other	
VSS	A24	Power/Other	
VSS	A6	Power/Other	
VSS	A9	Power/Other	
VSS	AA23	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	AA24	Power/Other	
VSS	AA25	Power/Other	
VSS	AA26	Power/Other	
VSS	AA27	Power/Other	
VSS	AA28	Power/Other	
VSS	AA29	Power/Other	
VSS	AA3	Power/Other	
VSS	AA30	Power/Other	
VSS	AA6	Power/Other	
VSS	AA7	Power/Other	
VSS	AB1	Power/Other	
VSS	AB23	Power/Other	
VSS	AB24	Power/Other	
VSS	AB25	Power/Other	
VSS	AB26	Power/Other	
VSS	AB27	Power/Other	
VSS	AB28	Power/Other	
VSS	AB29	Power/Other	
VSS	AB30	Power/Other	
VSS	AB7	Power/Other	
VSS	AC3	Power/Other	
VSS	AC6	Power/Other	
VSS	AC7	Power/Other	
VSS	AD4	Power/Other	
VSS	AD7	Power/Other	
VSS	AE10	Power/Other	
VSS	AE13	Power/Other	
VSS	AE16	Power/Other	
VSS	AE17	Power/Other	
VSS	AE2	Power/Other	
VSS	AE20	Power/Other	
VSS	AE24	Power/Other	
VSS	AE25	Power/Other	
VSS	AE26	Power/Other	
VSS	AE27	Power/Other	
VSS	AE28	Power/Other	
VSS	AE29	Power/Other	
VSS	AE30	Power/Other	
VSS	AE5	Power/Other	
VSS	AE7	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	AF10	Power/Other	
VSS	AF13	Power/Other	
VSS	AF16	Power/Other	
VSS	AF17	Power/Other	
VSS	AF20	Power/Other	
VSS	AF23	Power/Other	
VSS	AF24	Power/Other	
VSS	AF25	Power/Other	
VSS	AF26	Power/Other	
VSS	AF27	Power/Other	
VSS	AF28	Power/Other	
VSS	AF29	Power/Other	
VSS	AF3	Power/Other	
VSS	AF30	Power/Other	
VSS	AF6	Power/Other	
VSS	AF7	Power/Other	
VSS	AG10	Power/Other	
VSS	AG13	Power/Other	
VSS	AG16	Power/Other	
VSS	AG17	Power/Other	
VSS	AG20	Power/Other	
VSS	AG23	Power/Other	
VSS	AG24	Power/Other	
VSS	AG7	Power/Other	
VSS	AH1	Power/Other	
VSS	AH10	Power/Other	
VSS	AH13	Power/Other	
VSS	AH16	Power/Other	
VSS	AH17	Power/Other	
VSS	AH20	Power/Other	
VSS	AH23	Power/Other	
VSS	AH24	Power/Other	
VSS	AH3	Power/Other	
VSS	AH6	Power/Other	
VSS	AH7	Power/Other	
VSS	AJ10	Power/Other	
VSS	AJ13	Power/Other	
VSS	AJ16	Power/Other	
VSS	AJ17	Power/Other	
VSS	AJ20	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	AJ23	Power/Other	
VSS	AJ24	Power/Other	
VSS	AJ27	Power/Other	
VSS	AJ28	Power/Other	
VSS	AJ29	Power/Other	
VSS	AJ30	Power/Other	
VSS	AJ4	Power/Other	
VSS	AJ7	Power/Other	
VSS	AK10	Power/Other	
VSS	AK13	Power/Other	
VSS	AK16	Power/Other	
VSS	AK17	Power/Other	
VSS	AK2	Power/Other	
VSS	AK20	Power/Other	
VSS	AK23	Power/Other	
VSS	AK24	Power/Other	
VSS	AK27	Power/Other	
VSS	AK28	Power/Other	
VSS	AK29	Power/Other	
VSS	AK30	Power/Other	
VSS	AK5	Power/Other	
VSS	AK7	Power/Other	
VSS	AL10	Power/Other	
VSS	AL13	Power/Other	
VSS	AL16	Power/Other	
VSS	AL17	Power/Other	
VSS	AL20	Power/Other	
VSS	AL23	Power/Other	
VSS	AL24	Power/Other	
VSS	AL27	Power/Other	
VSS	AL28	Power/Other	
VSS	AL3	Power/Other	
VSS	AL7	Power/Other	
VSS	AM1	Power/Other	
VSS	AM10	Power/Other	
VSS	AM13	Power/Other	
VSS	AM16	Power/Other	
VSS	AM17	Power/Other	
VSS	AM20	Power/Other	
VSS	AM23	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	AM24	Power/Other	
VSS	AM27	Power/Other	
VSS	AM28	Power/Other	
VSS	AM4	Power/Other	
VSS	AN1	Power/Other	
VSS	AN10	Power/Other	
VSS	AN13	Power/Other	
VSS	AN16	Power/Other	
VSS	AN17	Power/Other	
VSS	AN2	Power/Other	
VSS	AN20	Power/Other	
VSS	AN23	Power/Other	
VSS	AN24	Power/Other	
VSS	AN27	Power/Other	
VSS	AN28	Power/Other	
VSS	B1	Power/Other	
VSS	B11	Power/Other	
VSS	B14	Power/Other	
VSS	B17	Power/Other	
VSS	B20	Power/Other	
VSS	B24	Power/Other	
VSS	B5	Power/Other	
VSS	B8	Power/Other	
VSS	C10	Power/Other	
VSS	C13	Power/Other	
VSS	C16	Power/Other	
VSS	C19	Power/Other	
VSS	C22	Power/Other	
VSS	C24	Power/Other	
VSS	C4	Power/Other	
VSS	C7	Power/Other	
VSS	D12	Power/Other	
VSS	D15	Power/Other	
VSS	D18	Power/Other	
VSS	D21	Power/Other	
VSS	D24	Power/Other	
VSS	D3	Power/Other	
VSS	D5	Power/Other	
VSS	D6	Power/Other	
VSS	D9	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	E11	Power/Other	
VSS	E14	Power/Other	
VSS	E17	Power/Other	
VSS	E2	Power/Other	
VSS	E20	Power/Other	
VSS	E25	Power/Other	
VSS	E26	Power/Other	
VSS	E27	Power/Other	
VSS	E28	Power/Other	
VSS	E29	Power/Other	
VSS	E8	Power/Other	
VSS	F10	Power/Other	
VSS	F13	Power/Other	
VSS	F16	Power/Other	
VSS	F19	Power/Other	
VSS	F22	Power/Other	
VSS	F4	Power/Other	
VSS	F7	Power/Other	
VSS	G1	Power/Other	
VSS	H10	Power/Other	
VSS	H11	Power/Other	
VSS	H12	Power/Other	
VSS	H13	Power/Other	
VSS	H14	Power/Other	
VSS	H17	Power/Other	
VSS	H18	Power/Other	
VSS	H19	Power/Other	
VSS	H20	Power/Other	
VSS	H21	Power/Other	
VSS	H22	Power/Other	
VSS	H23	Power/Other	
VSS	H24	Power/Other	
VSS	H25	Power/Other	
VSS	H26	Power/Other	
VSS	H27	Power/Other	
VSS	H28	Power/Other	
VSS	H3	Power/Other	
VSS	H6	Power/Other	
VSS	H7	Power/Other	
VSS	H8	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	H9	Power/Other	
VSS	J4	Power/Other	
VSS	J7	Power/Other	
VSS	K2	Power/Other	
VSS	K5	Power/Other	
VSS	K7	Power/Other	
VSS	L23	Power/Other	
VSS	L24	Power/Other	
VSS	L25	Power/Other	
VSS	L26	Power/Other	
VSS	L27	Power/Other	
VSS	L28	Power/Other	
VSS	L29	Power/Other	
VSS	L3	Power/Other	
VSS	L30	Power/Other	
VSS	L6	Power/Other	
VSS	L7	Power/Other	
VSS	M1	Power/Other	
VSS	M7	Power/Other	
VSS	N3	Power/Other	
VSS	N6	Power/Other	
VSS	N7	Power/Other	
VSS	P23	Power/Other	
VSS	P24	Power/Other	
VSS	P25	Power/Other	
VSS	P26	Power/Other	
VSS	P27	Power/Other	
VSS	P28	Power/Other	
VSS	P29	Power/Other	
VSS	P30	Power/Other	
VSS	P4	Power/Other	
VSS	P7	Power/Other	
VSS	R2	Power/Other	
VSS	R23	Power/Other	
VSS	R24	Power/Other	
VSS	R25	Power/Other	
VSS	R26	Power/Other	
VSS	R27	Power/Other	
VSS	R28	Power/Other	
VSS	R29	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VSS	R30	Power/Other	
VSS	R5	Power/Other	
VSS	R7	Power/Other	
VSS	T3	Power/Other	
VSS	T6	Power/Other	
VSS	T7	Power/Other	
VSS	U1	Power/Other	
VSS	U7	Power/Other	
VSS	V23	Power/Other	
VSS	V24	Power/Other	
VSS	V25	Power/Other	
VSS	V26	Power/Other	
VSS	V27	Power/Other	
VSS	V28	Power/Other	
VSS	V29	Power/Other	
VSS	V3	Power/Other	
VSS	V30	Power/Other	
VSS	V6	Power/Other	
VSS	V7	Power/Other	
VSS	W4	Power/Other	
VSS	W7	Power/Other	
VSS	Y2	Power/Other	
VSS	Y5	Power/Other	
VSS	Y7	Power/Other	
VSS_MB_REGULATION	AN6	Power/Other	Output
VSS_SENSE	AN4	Power/Other	Output
VSSA	B23	Power/Other	
VTT	A25	Power/Other	
VTT	A26	Power/Other	
VTT	A27	Power/Other	
VTT	A28	Power/Other	
VTT	A29	Power/Other	
VTT	A30	Power/Other	
VTT	B25	Power/Other	
VTT	B26	Power/Other	
VTT	B27	Power/Other	
VTT	B28	Power/Other	
VTT	B29	Power/Other	
VTT	B30	Power/Other	
VTT	C25	Power/Other	

Table 4-1. Alphabetical Land Assignments

Land Name	Land #	Signal Buffer Type	Direction
VTT	C26	Power/Other	
VTT	C27	Power/Other	
VTT	C28	Power/Other	
VTT	C29	Power/Other	
VTT	C30	Power/Other	
VTT	D25	Power/Other	
VTT	D26	Power/Other	
VTT	D27	Power/Other	
VTT	D28	Power/Other	
VTT	D29	Power/Other	
VTT	D30	Power/Other	
VTT_OUT_LEFT	J1	Power/Other	Output
VTT_OUT_RIGHT	AA1	Power/Other	Output
VTT_SEL	F27	Power/Other	Output
VTTPWRGD	AM6	Power/Other	Input

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
A2	VSS	Power/Other	
A3	RS2#	Common Clock	Input
A4	D2#	Source Synch	Input/Output
A5	D4#	Source Synch	Input/Output
A6	VSS	Power/Other	
A7	D7#	Source Synch	Input/Output
A8	DBI0#	Source Synch	Input/Output
A9	VSS	Power/Other	
A10	D8#	Source Synch	Input/Output
A11	D9#	Source Synch	Input/Output
A12	VSS	Power/Other	
A13	COMP0	Power/Other	Input
A14	D50#	Source Synch	Input/Output
A15	VSS	Power/Other	
A16	DSTBN3#	Source Synch	Input/Output
A17	D56#	Source Synch	Input/Output
A18	VSS	Power/Other	
A19	D61#	Source Synch	Input/Output
A20	RESERVED		
A21	VSS	Power/Other	
A22	D62#	Source Synch	Input/Output
A23	VCCA	Power/Other	
A24	VSS	Power/Other	
A25	VTT	Power/Other	
A26	VTT	Power/Other	
A27	VTT	Power/Other	
A28	VTT	Power/Other	
A29	VTT	Power/Other	
A30	VTT	Power/Other	
B1	VSS	Power/Other	
B2	DBSY#	Common Clock	Input/Output
B3	RS0#	Common Clock	Input
B4	D0#	Source Synch	Input/Output
B5	VSS	Power/Other	
B6	D5#	Source Synch	Input/Output
B7	D6#	Source Synch	Input/Output
B8	VSS	Power/Other	
B9	DSTBP0#	Source Synch	Input/Output
B10	D10#	Source Synch	Input/Output
B11	VSS	Power/Other	
B12	D13#	Source Synch	Input/Output

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
B13	RESERVED		
B14	VSS	Power/Other	
B15	D53#	Source Synch	Input/Output
B16	D55#	Source Synch	Input/Output
B17	VSS	Power/Other	
B18	D57#	Source Synch	Input/Output
B19	D60#	Source Synch	Input/Output
B20	VSS	Power/Other	
B21	D59#	Source Synch	Input/Output
B22	D63#	Source Synch	Input/Output
B23	VSSA	Power/Other	
B24	VSS	Power/Other	
B25	VTT	Power/Other	
B26	VTT	Power/Other	
B27	VTT	Power/Other	
B28	VTT	Power/Other	
B29	VTT	Power/Other	
B30	VTT	Power/Other	
C1	DRDY#	Common Clock	Input/Output
C2	BNR#	Common Clock	Input/Output
C3	LOCK#	Common Clock	Input/Output
C4	VSS	Power/Other	
C5	D1#	Source Synch	Input/Output
C6	D3#	Source Synch	Input/Output
C7	VSS	Power/Other	
C8	DSTBN0#	Source Synch	Input/Output
C9	RESERVED		
C10	VSS	Power/Other	
C11	D11#	Source Synch	Input/Output
C12	D14#	Source Synch	Input/Output
C13	VSS	Power/Other	
C14	D52#	Source Synch	Input/Output
C15	D51#	Source Synch	Input/Output
C16	VSS	Power/Other	
C17	DSTBP3#	Source Synch	Input/Output
C18	D54#	Source Synch	Input/Output
C19	VSS	Power/Other	
C20	DBI3#	Source Synch	Input/Output
C21	D58#	Source Synch	Input/Output
C22	VSS	Power/Other	
C23	VCCIOPLL	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
C24	VSS	Power/Other	
C25	VTT	Power/Other	
C26	VTT	Power/Other	
C27	VTT	Power/Other	
C28	VTT	Power/Other	
C29	VTT	Power/Other	
C30	VTT	Power/Other	
D1	RESERVED		
D2	ADS#	Common Clock	Input/Output
D3	VSS	Power/Other	
D4	HIT#	Common Clock	Input/Output
D5	VSS	Power/Other	
D6	VSS	Power/Other	
D7	D20#	Source Synch	Input/Output
D8	D12#	Source Synch	Input/Output
D9	VSS	Power/Other	
D10	D22#	Source Synch	Input/Output
D11	D15#	Source Synch	Input/Output
D12	VSS	Power/Other	
D13	D25#	Source Synch	Input/Output
D14	RESERVED		
D15	VSS	Power/Other	
D16	RESERVED		
D17	D49#	Source Synch	Input/Output
D18	VSS	Power/Other	
D19	DBI2#	Source Synch	Input/Output
D20	D48#	Source Synch	Input/Output
D21	VSS	Power/Other	
D22	D46#	Source Synch	Input/Output
D23	FC9	Other	
D24	VSS	Power/Other	
D25	VTT	Power/Other	
D26	VTT	Power/Other	
D27	VTT	Power/Other	
D28	VTT	Power/Other	
D29	VTT	Power/Other	
D30	VTT	Power/Other	
E2	VSS	Power/Other	
E3	TRDY#	Common Clock	Input
E4	HITM#	Common Clock	Input/Output
E5	RESERVED		

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
E6	RESERVED		
E7	RESERVED		
E8	VSS	Power/Other	
E9	D19#	Source Synch	Input/Output
E10	D21#	Source Synch	Input/Output
E11	VSS	Power/Other	
E12	DSTBP1#	Source Synch	Input/Output
E13	D26#	Source Synch	Input/Output
E14	VSS	Power/Other	
E15	D33#	Source Synch	Input/Output
E16	D34#	Source Synch	Input/Output
E17	VSS	Power/Other	
E18	D39#	Source Synch	Input/Output
E19	D40#	Source Synch	Input/Output
E20	VSS	Power/Other	
E21	D42#	Source Synch	Input/Output
E22	D45#	Source Synch	Input/Output
E23	RESERVED		
E24	FC10	Other	
E25	VSS	Power/Other	
E26	VSS	Power/Other	
E27	VSS	Power/Other	
E28	VSS	Power/Other	
E29	VSS	Power/Other	
F2	FC5	Other	
F3	BR0#	Common Clock	Input/Output
F4	VSS	Power/Other	
F5	RS1#	Common Clock	Input
F6	RESERVED		
F7	VSS	Power/Other	
F8	D17#	Source Synch	Input/Output
F9	D18#	Source Synch	Input/Output
F10	VSS	Power/Other	
F11	D23#	Source Synch	Input/Output
F12	D24#	Source Synch	Input/Output
F13	VSS	Power/Other	
F14	D28#	Source Synch	Input/Output
F15	D30#	Source Synch	Input/Output
F16	VSS	Power/Other	
F17	D37#	Source Synch	Input/Output
F18	D38#	Source Synch	Input/Output

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
F19	VSS	Power/Other	
F20	D41#	Source Synch	Input/Output
F21	D43#	Source Synch	Input/Output
F22	VSS	Power/Other	
F23	RESERVED		
F24	TESTHI7	Power/Other	Input
F25	TESTHI2	Power/Other	Input
F26	TESTHI0	Power/Other	Input
F27	VTT_SEL	Power/Other	Output
F28	BCLK0	Clock	Input
F29	RESERVED		
G1	VSS	Power/Other	
G2	FC1	Other	
G3	TESTHI8	Power/Other	Input
G4	TESTHI9	Power/Other	Input
G5	FC7	Other	
G6	RESERVED		
G7	DEFER#	Common Clock	Input
G8	BPRI#	Common Clock	Input
G9	D16#	Source Synch	Input/Output
G10	RESERVED		
G11	DBI1#	Source Synch	Input/Output
G12	DSTBN1#	Source Synch	Input/Output
G13	D27#	Source Synch	Input/Output
G14	D29#	Source Synch	Input/Output
G15	D31#	Source Synch	Input/Output
G16	D32#	Source Synch	Input/Output
G17	D36#	Source Synch	Input/Output
G18	D35#	Source Synch	Input/Output
G19	DSTBP2#	Source Synch	Input/Output
G20	DSTBN2#	Source Synch	Input/Output
G21	D44#	Source Synch	Input/Output
G22	D47#	Source Synch	Input/Output
G23	RESET#	Common Clock	Input
G24	TESTHI6	Power/Other	Input
G25	TESTHI3	Power/Other	Input
G26	TESTHI5	Power/Other	Input
G27	TESTHI4	Power/Other	Input
G28	BCLK1	Clock	Input
G29	BSEL0	Power/Other	Output
G30	BSEL2	Power/Other	Output

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
H1	GTLREF0	Power/Other	Input
H2	FC6	Other	
H3	VSS	Power/Other	
H4	RSP#	Common Clock	Input
H5	TESTHI10	Power/Other	Input
H6	VSS	Power/Other	
H7	VSS	Power/Other	
H8	VSS	Power/Other	
H9	VSS	Power/Other	
H10	VSS	Power/Other	
H11	VSS	Power/Other	
H12	VSS	Power/Other	
H13	VSS	Power/Other	
H14	VSS	Power/Other	
H15	DP1#	Common Clock	Input/Output
H16	DP2#	Common Clock	Input/Output
H17	VSS	Power/Other	
H18	VSS	Power/Other	
H19	VSS	Power/Other	
H20	VSS	Power/Other	
H21	VSS	Power/Other	
H22	VSS	Power/Other	
H23	VSS	Power/Other	
H24	VSS	Power/Other	
H25	VSS	Power/Other	
H26	VSS	Power/Other	
H27	VSS	Power/Other	
H28	VSS	Power/Other	
H29	GTLREF_SEL	Power/Other	Output
H30	BSEL1	Power/Other	Output
J1	VTT_OUT_LEFT	Power/Other	Output
J2	FC3	Other	
J3	RESERVED		
J4	VSS	Power/Other	
J5	REQ1#	Source Synch	Input/Output
J6	REQ4#	Source Synch	Input/Output
J7	VSS	Power/Other	
J8	VCC	Power/Other	
J9	VCC	Power/Other	
J10	VCC	Power/Other	
J11	VCC	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
J12	VCC	Power/Other	
J13	VCC	Power/Other	
J14	VCC	Power/Other	
J15	VCC	Power/Other	
J16	DP0#	Common Clock	Input/Output
J17	DP3#	Common Clock	Input/Output
J18	VCC	Power/Other	
J19	VCC	Power/Other	
J20	VCC	Power/Other	
J21	VCC	Power/Other	
J22	VCC	Power/Other	
J23	VCC	Power/Other	
J24	VCC	Power/Other	
J25	VCC	Power/Other	
J26	VCC	Power/Other	
J27	VCC	Power/Other	
J28	VCC	Power/Other	
J29	VCC	Power/Other	
J30	VCC	Power/Other	
K1	LINT0	Asynch GTL+	Input
K2	VSS	Power/Other	
K3	A20M#	Asynch GTL+	Input
K4	REQ0#	Source Synch	Input/Output
K5	VSS	Power/Other	
K6	REQ3#	Source Synch	Input/Output
K7	VSS	Power/Other	
K8	VCC	Power/Other	
K23	VCC	Power/Other	
K24	VCC	Power/Other	
K25	VCC	Power/Other	
K26	VCC	Power/Other	
K27	VCC	Power/Other	
K28	VCC	Power/Other	
K29	VCC	Power/Other	
K30	VCC	Power/Other	
L1	LINT1	Asynch GTL+	Input
L2	SLP#	Asynch GTL+	Input
L3	VSS	Power/Other	
L4	A6#	Source Synch	Input/Output
L5	A3#	Source Synch	Input/Output
L6	VSS	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
L7	VSS	Power/Other	
L8	VCC	Power/Other	
L23	VSS	Power/Other	
L24	VSS	Power/Other	
L25	VSS	Power/Other	
L26	VSS	Power/Other	
L27	VSS	Power/Other	
L28	VSS	Power/Other	
L29	VSS	Power/Other	
L30	VSS	Power/Other	
M1	VSS	Power/Other	
M2	THERMTRIP#	Asynch GTL+	Output
M3	STPCLK#	Asynch GTL+	Input
M4	A7#	Source Synch	Input/Output
M5	A5#	Source Synch	Input/Output
M6	REQ2#	Source Synch	Input/Output
M7	VSS	Power/Other	
M8	VCC	Power/Other	
M23	VCC	Power/Other	
M24	VCC	Power/Other	
M25	VCC	Power/Other	
M26	VCC	Power/Other	
M27	VCC	Power/Other	
M28	VCC	Power/Other	
M29	VCC	Power/Other	
M30	VCC	Power/Other	
N1	PWRGOOD	Power/Other	Input
N2	IGNNE#	Asynch GTL+	Input
N3	VSS	Power/Other	
N4	RESERVED		
N5	RESERVED		
N6	VSS	Power/Other	
N7	VSS	Power/Other	
N8	VCC	Power/Other	
N23	VCC	Power/Other	
N24	VCC	Power/Other	
N25	VCC	Power/Other	
N26	VCC	Power/Other	
N27	VCC	Power/Other	
N28	VCC	Power/Other	
N29	VCC	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
N30	VCC	Power/Other	
P1	TESTHI11	Power/Other	Input
P2	SMI#	Asynch GTL+	Input
P3	INIT#	Asynch GTL+	Input
P4	VSS	Power/Other	
P5	RESERVED		
P6	A4#	Source Synch	Input/Output
P7	VSS	Power/Other	
P8	VCC	Power/Other	
P23	VSS	Power/Other	
P24	VSS	Power/Other	
P25	VSS	Power/Other	
P26	VSS	Power/Other	
P27	VSS	Power/Other	
P28	VSS	Power/Other	
P29	VSS	Power/Other	
P30	VSS	Power/Other	
R1	FC2	Other	
R2	VSS	Power/Other	
R3	FERR#/PBE#	Asynch GTL+	Output
R4	A8#	Source Synch	Input/Output
R5	VSS	Power/Other	
R6	ADSTB0#	Source Synch	Input/Output
R7	VSS	Power/Other	
R8	VCC	Power/Other	
R23	VSS	Power/Other	
R24	VSS	Power/Other	
R25	VSS	Power/Other	
R26	VSS	Power/Other	
R27	VSS	Power/Other	
R28	VSS	Power/Other	
R29	VSS	Power/Other	
R30	VSS	Power/Other	
T1	COMP1	Power/Other	Input
T2	FC4	Other	
T3	VSS	Power/Other	
T4	A11#	Source Synch	Input/Output
T5	A9#	Source Synch	Input/Output
T6	VSS	Power/Other	
T7	VSS	Power/Other	
T8	VCC	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
T23	VCC	Power/Other	
T24	VCC	Power/Other	
T25	VCC	Power/Other	
T26	VCC	Power/Other	
T27	VCC	Power/Other	
T28	VCC	Power/Other	
T29	VCC	Power/Other	
T30	VCC	Power/Other	
U1	VSS	Power/Other	
U2	AP0#	Common Clock	Input/Output
U3	AP1#	Common Clock	Input/Output
U4	A13#	Source Synch	Input/Output
U5	A12#	Source Synch	Input/Output
U6	A10#	Source Synch	Input/Output
U7	VSS	Power/Other	
U8	VCC	Power/Other	
U23	VCC	Power/Other	
U24	VCC	Power/Other	
U25	VCC	Power/Other	
U26	VCC	Power/Other	
U27	VCC	Power/Other	
U28	VCC	Power/Other	
U29	VCC	Power/Other	
U30	VCC	Power/Other	
V1	FC14	Other	
V2	LL_ID0	Power/Other	Output
V3	VSS	Power/Other	
V4	A15#	Source Synch	Input/Output
V5	A14#	Source Synch	Input/Output
V6	VSS	Power/Other	
V7	VSS	Power/Other	
V8	VCC	Power/Other	
V23	VSS	Power/Other	
V24	VSS	Power/Other	
V25	VSS	Power/Other	
V26	VSS	Power/Other	
V27	VSS	Power/Other	
V28	VSS	Power/Other	
V29	VSS	Power/Other	
V30	VSS	Power/Other	
W1	FC13	Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
W2	TESTHI12	Power/Other	Input
W3	TESTHI1	Power/Other	Input
W4	VSS	Power/Other	
W5	A16#	Source Synch	Input/Output
W6	A18#	Source Synch	Input/Output
W7	VSS	Power/Other	
W8	VCC	Power/Other	
W23	VCC	Power/Other	
W24	VCC	Power/Other	
W25	VCC	Power/Other	
W26	VCC	Power/Other	
W27	VCC	Power/Other	
W28	VCC	Power/Other	
W29	VCC	Power/Other	
W30	VCC	Power/Other	
Y1	FC0	Other	
Y2	VSS	Power/Other	
Y3	RESERVED		
Y4	A20#	Source Synch	Input/Output
Y5	VSS	Power/Other	
Y6	A19#	Source Synch	Input/Output
Y7	VSS	Power/Other	
Y8	VCC	Power/Other	
Y23	VCC	Power/Other	
Y24	VCC	Power/Other	
Y25	VCC	Power/Other	
Y26	VCC	Power/Other	
Y27	VCC	Power/Other	
Y28	VCC	Power/Other	
Y29	VCC	Power/Other	
Y30	VCC	Power/Other	
AA1	VTT_OUT_RIGHT	Power/Other	Output
AA2	LL_ID1	Power/Other	Output
AA3	VSS	Power/Other	
AA4	A21#	Source Synch	Input/Output
AA5	A23#	Source Synch	Input/Output
AA6	VSS	Power/Other	
AA7	VSS	Power/Other	
AA8	VCC	Power/Other	
AA23	VSS	Power/Other	
AA24	VSS	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AA25	VSS	Power/Other	
AA26	VSS	Power/Other	
AA27	VSS	Power/Other	
AA28	VSS	Power/Other	
AA29	VSS	Power/Other	
AA30	VSS	Power/Other	
AB1	VSS	Power/Other	
AB2	IERR#	Asynch GTL+	Output
AB3	MCERR#	Common Clock	Input/Output
AB4	A26#	Source Synch	Input/Output
AB5	A24#	Source Synch	Input/Output
AB6	A17#	Source Synch	Input/Output
AB7	VSS	Power/Other	
AB8	VCC	Power/Other	
AB23	VSS	Power/Other	
AB24	VSS	Power/Other	
AB25	VSS	Power/Other	
AB26	VSS	Power/Other	
AB27	VSS	Power/Other	
AB28	VSS	Power/Other	
AB29	VSS	Power/Other	
AB30	VSS	Power/Other	
AC1	TMS	TAP	Input
AC2	DBR#	Power/Other	Output
AC3	VSS	Power/Other	
AC4	RESERVED		
AC5	A25#	Source Synch	Input/Output
AC6	VSS	Power/Other	
AC7	VSS	Power/Other	
AC8	VCC	Power/Other	
AC23	VCC	Power/Other	
AC24	VCC	Power/Other	
AC25	VCC	Power/Other	
AC26	VCC	Power/Other	
AC27	VCC	Power/Other	
AC28	VCC	Power/Other	
AC29	VCC	Power/Other	
AC30	VCC	Power/Other	
AD1	TDI	TAP	Input
AD2	BPM2#	Common Clock	Input/Output
AD3	BINIT#	Common Clock	Input/Output

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AD4	VSS	Power/Other	
AD5	ADSTB1#	Source Synch	Input/Output
AD6	A22#	Source Synch	Input/Output
AD7	VSS	Power/Other	
AD8	VCC	Power/Other	
AD23	VCC	Power/Other	
AD24	VCC	Power/Other	
AD25	VCC	Power/Other	
AD26	VCC	Power/Other	
AD27	VCC	Power/Other	
AD28	VCC	Power/Other	
AD29	VCC	Power/Other	
AD30	VCC	Power/Other	
AE1	TCK	TAP	Input
AE2	VSS	Power/Other	
AE3	RESERVED		
AE4	RESERVED		
AE5	VSS	Power/Other	
AE6	RESERVED		
AE7	VSS	Power/Other	
AE8	SKTOCC#	Power/Other	Output
AE9	VCC	Power/Other	
AE10	VSS	Power/Other	
AE11	VCC	Power/Other	
AE12	VCC	Power/Other	
AE13	VSS	Power/Other	
AE14	VCC	Power/Other	
AE15	VCC	Power/Other	
AE16	VSS	Power/Other	
AE17	VSS	Power/Other	
AE18	VCC	Power/Other	
AE19	VCC	Power/Other	
AE20	VSS	Power/Other	
AE21	VCC	Power/Other	
AE22	VCC	Power/Other	
AE23	VCC	Power/Other	
AE24	VSS	Power/Other	
AE25	VSS	Power/Other	
AE26	VSS	Power/Other	
AE27	VSS	Power/Other	
AE28	VSS	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AE29	VSS	Power/Other	
AE30	VSS	Power/Other	
AF1	TDO	TAP	Output
AF2	BPM4#	Common Clock	Input/Output
AF3	VSS	Power/Other	
AF4	A28#	Source Synch	Input/Output
AF5	A27#	Source Synch	Input/Output
AF6	VSS	Power/Other	
AF7	VSS	Power/Other	
AF8	VCC	Power/Other	
AF9	VCC	Power/Other	
AF10	VSS	Power/Other	
AF11	VCC	Power/Other	
AF12	VCC	Power/Other	
AF13	VSS	Power/Other	
AF14	VCC	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VSS	Power/Other	
AF18	VCC	Power/Other	
AF19	VCC	Power/Other	
AF20	VSS	Power/Other	
AF21	VCC	Power/Other	
AF22	VCC	Power/Other	
AF23	VSS	Power/Other	
AF24	VSS	Power/Other	
AF25	VSS	Power/Other	
AF26	VSS	Power/Other	
AF27	VSS	Power/Other	
AF28	VSS	Power/Other	
AF29	VSS	Power/Other	
AF30	VSS	Power/Other	
AG1	TRST#	TAP	Input
AG2	BPM3#	Common Clock	Input/Output
AG3	BPM5#	Common Clock	Input/Output
AG4	A30#	Source Synch	Input/Output
AG5	A31#	Source Synch	Input/Output
AG6	A29#	Source Synch	Input/Output
AG7	VSS	Power/Other	
AG8	VCC	Power/Other	
AG9	VCC	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AG10	VSS	Power/Other	
AG11	VCC	Power/Other	
AG12	VCC	Power/Other	
AG13	VSS	Power/Other	
AG14	VCC	Power/Other	
AG15	VCC	Power/Other	
AG16	VSS	Power/Other	
AG17	VSS	Power/Other	
AG18	VCC	Power/Other	
AG19	VCC	Power/Other	
AG20	VSS	Power/Other	
AG21	VCC	Power/Other	
AG22	VCC	Power/Other	
AG23	VSS	Power/Other	
AG24	VSS	Power/Other	
AG25	VCC	Power/Other	
AG26	VCC	Power/Other	
AG27	VCC	Power/Other	
AG28	VCC	Power/Other	
AG29	VCC	Power/Other	
AG30	VCC	Power/Other	
AH1	VSS	Power/Other	
AH2	RESERVED		
AH3	VSS	Power/Other	
AH4	A32#	Source Synch	Input/Output
AH5	A33#	Source Synch	Input/Output
AH6	VSS	Power/Other	
AH7	VSS	Power/Other	
AH8	VCC	Power/Other	
AH9	VCC	Power/Other	
AH10	VSS	Power/Other	
AH11	VCC	Power/Other	
AH12	VCC	Power/Other	
AH13	VSS	Power/Other	
AH14	VCC	Power/Other	
AH15	VCC	Power/Other	
AH16	VSS	Power/Other	
AH17	VSS	Power/Other	
AH18	VCC	Power/Other	
AH19	VCC	Power/Other	
AH20	VSS	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AH21	VCC	Power/Other	
AH22	VCC	Power/Other	
AH23	VSS	Power/Other	
AH24	VSS	Power/Other	
AH25	VCC	Power/Other	
AH26	VCC	Power/Other	
AH27	VCC	Power/Other	
AH28	VCC	Power/Other	
AH29	VCC	Power/Other	
AH30	VCC	Power/Other	
AJ1	BPM1#	Common Clock	Input/Output
AJ2	BPM0#	Common Clock	Input/Output
AJ3	ITP_CLK1	TAP	Input
AJ4	VSS	Power/Other	
AJ5	A34#	Source Synch	Input/Output
AJ6	A35#	Source Synch	Input/Output
AJ7	VSS	Power/Other	
AJ8	VCC	Power/Other	
AJ9	VCC	Power/Other	
AJ10	VSS	Power/Other	
AJ11	VCC	Power/Other	
AJ12	VCC	Power/Other	
AJ13	VSS	Power/Other	
AJ14	VCC	Power/Other	
AJ15	VCC	Power/Other	
AJ16	VSS	Power/Other	
AJ17	VSS	Power/Other	
AJ18	VCC	Power/Other	
AJ19	VCC	Power/Other	
AJ20	VSS	Power/Other	
AJ21	VCC	Power/Other	
AJ22	VCC	Power/Other	
AJ23	VSS	Power/Other	
AJ24	VSS	Power/Other	
AJ25	VCC	Power/Other	
AJ26	VCC	Power/Other	
AJ27	VSS	Power/Other	
AJ28	VSS	Power/Other	
AJ29	VSS	Power/Other	
AJ30	VSS	Power/Other	
AK1	THERMDC	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AK2	VSS	Power/Other	
AK3	ITP_CLK0	TAP	Input
AK4	VID4	Power/Other	Output
AK5	VSS	Power/Other	
AK6	FC8	Other	
AK7	VSS	Power/Other	
AK8	VCC	Power/Other	
AK9	VCC	Power/Other	
AK10	VSS	Power/Other	
AK11	VCC	Power/Other	
AK12	VCC	Power/Other	
AK13	VSS	Power/Other	
AK14	VCC	Power/Other	
AK15	VCC	Power/Other	
AK16	VSS	Power/Other	
AK17	VSS	Power/Other	
AK18	VCC	Power/Other	
AK19	VCC	Power/Other	
AK20	VSS	Power/Other	
AK21	VCC	Power/Other	
AK22	VCC	Power/Other	
AK23	VSS	Power/Other	
AK24	VSS	Power/Other	
AK25	VCC	Power/Other	
AK26	VCC	Power/Other	
AK27	VSS	Power/Other	
AK28	VSS	Power/Other	
AK29	VSS	Power/Other	
AK30	VSS	Power/Other	
AL1	THERMDA	Power/Other	
AL2	PROCHOT#	Asynch GTL+	Input/Output
AL3	VSS	Power/Other	
AL4	VID5	Power/Other	Output
AL5	VID1	Power/Other	Output
AL6	VID3	Power/Other	Output
AL7	VSS	Power/Other	
AL8	VCC	Power/Other	
AL9	VCC	Power/Other	
AL10	VSS	Power/Other	
AL11	VCC	Power/Other	
AL12	VCC	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AL13	VSS	Power/Other	
AL14	VCC	Power/Other	
AL15	VCC	Power/Other	
AL16	VSS	Power/Other	
AL17	VSS	Power/Other	
AL18	VCC	Power/Other	
AL19	VCC	Power/Other	
AL20	VSS	Power/Other	
AL21	VCC	Power/Other	
AL22	VCC	Power/Other	
AL23	VSS	Power/Other	
AL24	VSS	Power/Other	
AL25	VCC	Power/Other	
AL26	VCC	Power/Other	
AL27	VSS	Power/Other	
AL28	VSS	Power/Other	
AL29	VCC	Power/Other	
AL30	VCC	Power/Other	
AM1	VSS	Power/Other	
AM2	VID0	Power/Other	Output
AM3	VID2	Power/Other	Output
AM4	VSS	Power/Other	
AM5	FC11	Other	
AM6	VTTPWRGD	Power/Other	Input
AM7	FC12	Other	
AM8	VCC	Power/Other	Output
AM9	VCC	Power/Other	
AM10	VSS	Power/Other	
AM11	VCC	Power/Other	
AM12	VCC	Power/Other	
AM13	VSS	Power/Other	
AM14	VCC	Power/Other	
AM15	VCC	Power/Other	
AM16	VSS	Power/Other	
AM17	VSS	Power/Other	
AM18	VCC	Power/Other	
AM19	VCC	Power/Other	
AM20	VSS	Power/Other	
AM21	VCC	Power/Other	
AM22	VCC	Power/Other	
AM23	VSS	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AM24	VSS	Power/Other	
AM25	VCC	Power/Other	
AM26	VCC	Power/Other	
AM27	VSS	Power/Other	
AM28	VSS	Power/Other	
AM29	VCC	Power/Other	
AM30	VCC	Power/Other	
AN1	VSS	Power/Other	
AN2	VSS	Power/Other	
AN3	VCC_SENSE	Power/Other	Output
AN4	VSS_SENSE	Power/Other	Output
AN5	VCC_MB_ REGULATION	Power/Other	Output
AN6	VSS_MB_ REGULATION	Power/Other	Output
AN7	FC16	Other	
AN8	VCC	Power/Other	
AN9	VCC	Power/Other	
AN10	VSS	Power/Other	
AN11	VCC	Power/Other	
AN12	VCC	Power/Other	
AN13	VSS	Power/Other	

Table 4-2. Numerical Land Assignment

Land #	Land Name	Signal Buffer Type	Direction
AN14	VCC	Power/Other	
AN15	VCC	Power/Other	
AN16	VSS	Power/Other	
AN17	VSS	Power/Other	
AN18	VCC	Power/Other	
AN19	VCC	Power/Other	
AN20	VSS	Power/Other	
AN21	VCC	Power/Other	
AN22	VCC	Power/Other	
AN23	VSS	Power/Other	
AN24	VSS	Power/Other	
AN25	VCC	Power/Other	
AN26	VCC	Power/Other	
AN27	VSS	Power/Other	
AN28	VSS	Power/Other	
AN29	VCC	Power/Other	
AN30	VCC	Power/Other	

4.2 Alphabetical Signals Reference

Table 4-3. Signal Description (Sheet 1 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>A[35:3]#</td><td>Input/ Output</td><td>A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these signals transmit the address of a transaction. In sub-phase 2, these signals transmit transaction type information. These signals must connect the appropriate pins/lands of all agents on the processor FSB. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#.
On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# signals to determine power-on configuration. See Section 6.1 for more details.</td></tr>
<tr><td>A20M#</td><td>Input</td><td>If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode.
A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td></tr>
<tr><td>ADS#</td><td>Input/ Output</td><td>ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# signals. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.</td></tr>
<tr><td>ADSTB[1:0]#</td><td>Input/ Output</td><td>Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB0#</td></tr>
<tr><td>A[35:17]#</td><td>ADSTB1#</td></tr>
</table></td></tr>
<tr><td>AP[1:0]#</td><td>Input/ Output</td><td>AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins/lands of all Intel® Pentium® 4 processor Extreme Edition in the 775-land package FSB agents. The following table defines the coverage model of these signals.
<table>
<tr><th>Request Signals</th><th>Subphase 1</th><th>Subphase 2</th></tr>
<tr><td>A[35:24]#</td><td>AP0#</td><td>AP1#</td></tr>
<tr><td>A[23:3]#</td><td>AP1#</td><td>AP0#</td></tr>
<tr><td>REQ[4:0]#</td><td>AP1#</td><td>AP0#</td></tr>
</table></td></tr>
<tr><td>BCLK[1:0]</td><td>Input</td><td>The differential pair BCLK (Bus Clock) determines the FSB frequency. All processor FSB agents must receive these signals to drive their outputs and latch their inputs.
All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.</td></tr>
</table>

Table 4-3. Signal Description (Sheet 1 of 9)

Name	Type	Description
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor FSB agents and if used, must connect the appropriate pins/lands of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the FSB and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins/lands of all processor FSB agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Contact your Intel representative for further details and documentation. These signals do not have on-die termination. Refer to Section 2.5.
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor FSB. It must connect the appropriate pins/lands of all processor FSB agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by de-asserting BPRI#.
BR0#	Input/ Output	BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this signal is sampled to determine the agent ID = 0. This signal does not have on-die termination and must be terminated.
BSEL[2:0]	Output	The BCLK[1:0] frequency select signals BSEL[2:0] are used to select the processor input clock frequency. Table 2-3 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. For more information about these signals, including termination recommendations, refer to Section 2.9. Contact your Intel representative for further details and documentation.
COMP[1:0]	Analog	COMP[1:0] must be terminated to V_{SS} on the system board using precision resistors. Contact your Intel representative for further details and documentation.

Table 4-3. Signal Description (Sheet 1 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>D[63:0]#</td><td>Input/ Output</td><td>
<p>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor FSB agents, and must connect the appropriate pins/ lands on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.</p>
<p>D[63:0]# are quad-pumped signals and will, thus, be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#.</p>
<p>Quad-Pumped Signal Groups</p>
<table>
<tr><th>Data Group</th><th>DSTBN#/ DSTBP#</th><th>DBI#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>
<p>Furthermore, the DBI# signals determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</p>
</td></tr>
<tr><td>DBI[3:0]#</td><td>Input/ Output</td><td>
<p>DBI[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals.The DBI[3:0]# signals are activated when the data on the data bus is inverted. If more than half the data bits, within a 16-bit group, would have been asserted electrically low, the bus agent may invert the data bus signals for that particular sub-phase for that 16-bit group.</p>
<p>DBI[3:0] Assignment To Data Bus</p>
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DBI3#</td><td>D[63:48]#</td></tr>
<tr><td>DBI2#</td><td>D[47:32]#</td></tr>
<tr><td>DBI1#</td><td>D[31:16]#</td></tr>
<tr><td>DBI0#</td><td>D[15:0]#</td></tr>
</table>
</td></tr>
<tr><td>DBR#</td><td>Output</td><td>DBR# (Debug Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.</td></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor FSB to indicate that the data bus is in use. The data bus is released after DBSY# is de-asserted. This signal must connect the appropriate pins/lands on all processor FSB agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or input/output agent. This signal must connect the appropriate pins/lands of all processor FSB agents.</td></tr>
<tr><td>DP[3:0]#</td><td>Input/ Output</td><td>DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins/lands of all processor FSB agents.</td></tr>
</table>

Table 4-3. Signal Description (Sheet 1 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DRDY#</td><td>Input/
Output</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be de-asserted to insert idle clocks. This signal must connect the appropriate pins/lands of all processor FSB agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/
Output</td><td>DSTBN[3:0]# are the data strobes used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DBI0#</td><td>DSTBN0#</td></tr>
<tr><td>D[31:16]#, DBI1#</td><td>DSTBN1#</td></tr>
<tr><td>D[47:32]#, DBI2#</td><td>DSTBN2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBN3#</td></tr>
</table></td></tr>
<tr><td>DSTBP[3:0]#</td><td>Input/
Output</td><td>DSTBP[3:0]# are the data strobes used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#</td></tr>
<tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#</td></tr>
<tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#</td></tr>
</table></td></tr>
<tr><td>FC[14:0]</td><td>Other</td><td>Future compatible lands are reserved to be used with future or compatible processors. Contact your Intel representative for further documentation.</td></tr>
<tr><td>FC16</td><td>Other</td><td>Future compatible lands are reserved to be used with future or compatible processors. Contact your Intel representative for further documentation.</td></tr>
<tr><td>FERR#/PBE#</td><td>Output</td><td>FERR#/PBE# (floating point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to volume 3 of the <i>Intel Architecture Software Developer's Manual</i> and the <i>Intel Processor Identification and the CPUID Instruction</i> application note.</td></tr>
<tr><td>GTLREF0</td><td>Input</td><td>GTLREF0 determines the signal reference level for GTL+ input signals. GTLREF0 is used by the GTL+ receivers to determine if a signal is a logical 0 or logical 1. Contact your Intel representative for further details and documentation.</td></tr>
<tr><td>GTLREF_SEL</td><td>Output</td><td>GTLREF_SEL is used to select the appropriate chipset GTLREF0 voltage. Contact your Intel representative for further details and documentation.</td></tr>
<tr><td>HIT#</td><td>Input/
Output</td><td rowspan="2">HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.</td></tr>
<tr><td>HITM#</td><td>Input/
Output</td></tr>
</table>

Table 4-3. Signal Description (Sheet 1 of 9)

Name	Type	Description
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#. This signal does not have on-die termination. Refer to Section 2.5 for termination requirements.
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is de-asserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins/lands of all processor FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins/lands of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these signals as LINT[1:0] is the default configuration.
LL_ID[1:0]	Output	The LL_ID[1:0] signals are used to select the correct loadline slope for the processor. LL_ID[1:0] = 00 for the Pentium 4 processor Extreme Edition in the 775-land package.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins/lands of all processor FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor FSB, it will wait until it observes LOCK# de-asserted. This enables symmetric agents to retain ownership of the processor FSB throughout the bus locked operation and ensure the atomicity of lock.

Table 4-3. Signal Description (Sheet 1 of 9)

Name	Type	Description
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor FSB agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.
PROCHOT#	Input/ Output	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#. See Section 5.2.3 for more details.
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins/lands of all processor FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, all FSB agents will de-assert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 6.1. This signal does not have on-die termination and must be terminated on the system board.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins/lands of all processor FSB agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins/lands of all processor FSB agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.

Table 4-3. Signal Description (Sheet 1 of 9)

Name	Type	Description
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this signal to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, and de-assertion of SLP#. If SLP# is de-asserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the de-assertion of RESET#, the processor will tri-state its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is de-asserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12:0]	Input	TESTHI[12:0] must be connected to the processor's appropriate power source (refer to VTT_OUT_LEFT and VTT_OUT_RIGHT signal description) through a resistor for proper processor operation. See Section 2.5 for more details.
THERMDA	Other	Thermal Diode Anode. See Section 5.2.5.
THERMDC	Other	Thermal Diode Cathode. See Section 5.2.5.
THERMTRIP#	Output	In the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature approximately 20 °C above the maximum T_C. Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond where permanent silicon damage may occur. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus, halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (V_{CC}) must be removed following the assertion of THERMTRIP#. Driving of the THERMTRIP# signal is enabled within 10 µs of the assertion of PWRGOOD and is disabled on de-assertion of PWRGOOD. Once activated, THERMTRIP# remains latched until PWRGOOD is de-asserted. While the de-assertion of the PWRGOOD signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 µs of the assertion of PWRGOOD.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins/lands of all FSB agents.

Table 4-3. Signal Description (Sheet 1 of 9)

Name	Type	Description
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. Contact your Intel representative for complete implementation details.
VCC	Input	VCC are the power pins for the processor. The voltage supplied to these pins is determined by the VID[5:0] pins.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. **NOTE:** VCCA is for compatible processors. VCCA is not used in the Pentium 4 processor Extreme Edition in 775-land package. Contact your Intel representative for further details and documentation.
VCCIOPLL	Input	VCCIOPLL provides isolated power for internal processor FSB PLLs. **NOTE:** VCCIOPLL is for compatible processors. VCCIOPLL is not used in the Pentium 4 processor Extreme Edition in 775-land package. Contact your Intel representative for further details and documentation.
VCC_SENSE	Output	VCC_SENSE is an isolated low impedance connection to processor core power (V_{CC}). It can be used to sense or measure voltage near the silicon with little noise.
VCC_MB_ REGULATION	Output	This land is provided as a voltage regulator feedback sense point for V_{CC}. It is connected internally in the processor package to the sense point land U27 as described in the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775*.
VID[5:0]	Output	VID[5:0] (Voltage ID) signals are used to support automatic selection of power supply voltages (V_{CC}). These are open drain signals that are driven by the Pentium 4 processor Extreme Edition in the 775-land package and must be pulled up on the motherboard. Refer to the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775* for more information. The voltage supply for these signals must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID signals becomes valid. The VID signals are needed to support the processor voltage specification variations. See Table 2-1 for definitions of these signals. The VR must supply the voltage that is requested by the signals, or disable itself.
VSS	Input	VSS are the ground pins for the processor and should be connected to the system ground plane.
VSSA	Input	VSSA is the isolated ground for internal PLLs. **NOTE:** VSSA is for future and compatible processors. VSSA is not used in the Pentium 4 processor Extreme Edition in 775-land package.
VSS_SENSE	Output	VSS_SENSE is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise.
VSS_MB_ REGULATION	Output	This land is provided as a voltage regulator feedback sense point for V_{SS}. It is connected internally in the processor package to the sense point land V27 as described in the *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775*.
VTT		Miscellaneous voltage supply.

Table 4-3. Signal Description (Sheet 1 of 9)

Name	Type	Description
VTT_OUT_LEFT VTT_OUT_RIGHT	Output	The VTT_OUT_LEFT and VTT_OUT_RIGHT signals are included to provide a voltage supply for some signals that require termination to V_{TT} on the motherboard. Contact your Intel representative for further details and documentation. For future processor compatibility some signals are required to be pulled up to VTT_OUT_LEFT or VTT_OUT_RIGHT. Refer to the following table for the signals that should be pulled up to VTT_OUT_LEFT and VTT_OUT_RIGHT. <table><tr><th>Pull-up Signal</th><th>Signals to be Pulled Up</th></tr><tr><td>VTT_OUT_RIGHT</td><td>VTT_PWRGOOD, VID[5:0], GTLREF0, TMS, TDI, TDO, BPM[5:0], other VRD components</td></tr><tr><td>VTT_OUT_LEFT</td><td>RESET#, BR0#, PWRGOOD, TESTHI1, TESTHI8, TESTHI9, TESTHI10, TESTHI11, TESTHI12</td></tr></table> **NOTE:** For the Pentium 4 processor Extreme Edition in the 775-land package, the voltage level for VTT_OUT_LEFT is equal to the processor V_{CC}. The VTT_OUT_RIGHT voltage levels will be at the V_{TT} level.
VTT_SEL	Output	The VTT_SEL signal is used to select the correct V_{TT} voltage level for the processor.
VTTPWRGD	Input	The processor requires this input to determine that the V_{TT} voltages are stable and within specification. **NOTE:** VTTPWRGD is for compatible processors. VTTPWRGD is not used in the Pentium 4 processor Extreme Edition in 775-land package. This pin is required for compatibility with Voltage Regulator Down (VRD10) 10.1 Design Guide standards.

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5 Thermal Specifications and Design Considerations

5.1 Processor Thermal Specifications

The Pentium 4 processor Extreme Edition in the 775-land package requires a thermal solution to maintain temperatures within operating limits as set forth in Section 5.1.1. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor Integrated Heat Spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

For more information on designing a component level thermal solution, refer to the *Intel® Pentium® 4 Processor Extreme Edition on 0.13 Micron Process in the 775-land package Thermal Design Guide*.

Note: The boxed processor will ship with a component thermal solution. Refer to Chapter 7 for details on the boxed processor.

5.1.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum case temperature (T_C) specifications when operating at or below the Thermal Design Power (TDP) value listed per frequency in Table 5-1. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, refer to the appropriate processor thermal design guidelines.

The case temperature is defined at the geometric top center of the processor. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained periods of time. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 5-1 instead of the maximum processor power consumption. The Thermal Monitor feature is intended to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 5.2. **In all cases, the Thermal Monitor feature must be enabled for the processor to remain within specification.**

Table 5-1. Processor Thermal Specifications

Core Frequency (GHz)	Thermal Design Power (W)	Minimum T_C (°C)	Maximum T_C (°C)	Notes
3.40	109.6	5	66	1, 2
3.46	110.7	5	66	1, 2

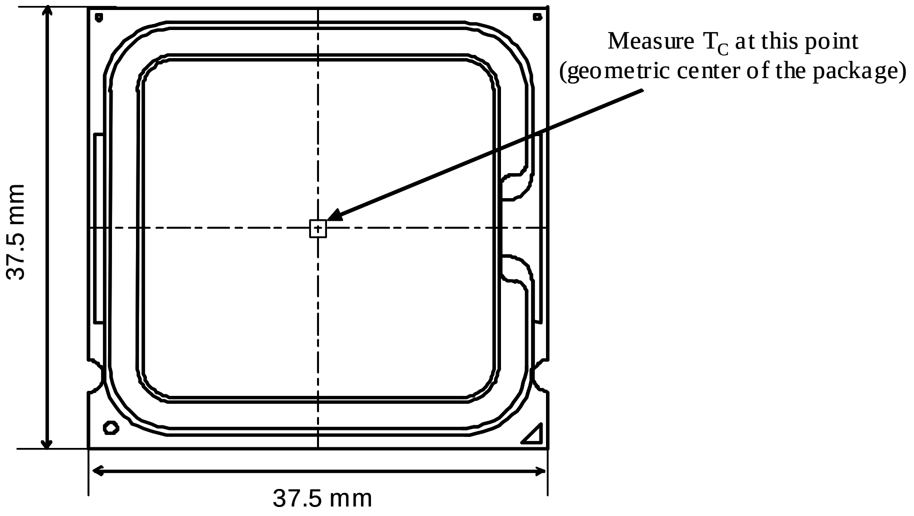
NOTES:

1. These values are specified at V_{cc_max} for the processor. Systems must be designed to ensure that the processor is not subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{cc_max} at specified I_{CC}. Refer to loadline specification in Chapter 2.
2. Thermal Design Power (TDP) should be used for processor thermal solution design targets. The TDP is not the maximum power that the processor can dissipate.

5.1.2 Thermal Metrology

The maximum and minimum case temperatures (T_C) are specified in Table 5-1. These temperature specifications are meant to help ensure proper operation of the processor. Figure 5-1 illustrates where Intel recommends T_C thermal measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the *Intel® Pentium® 4 Processor Extreme Edition on 0.13 Micron Process in the 775-land package Thermal Design Guide*.

Figure 5-1. Case Temperature (T_C) Measurement Location



5.2 Processor Thermal Features

5.2.1 Thermal Monitor

The Thermal Monitor feature helps control the processor temperature by activating the TCC when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption as needed by modulating (starting and stopping) the internal processor core clocks. **The Thermal Monitor feature must be enabled for the processor to be operating within specifications.** The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor feature is enabled, and a high temperature situation exists (i.e., TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30–50%). Clocks often will not be off for more than 3.0 microseconds when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may result in a T_C that exceeds the specified maximum temperature and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the *Intel® Pentium® 4 Processor Extreme Edition on 0.13 Micron Process in the 775-land package Thermal Design Guide* for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

5.2.2 On-Demand Mode

The Pentium 4 processor Extreme Edition in the 775-land package provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as “On-Demand” mode and is distinct from the Thermal Monitor feature. On-Demand mode is intended as a means to reduce system level power consumption. Systems utilizing the Pentium 4 processor Extreme Edition in the 775-land package must not rely on software usage of this mechanism to limit the processor temperature.

If bit 4 of the ACPI P_CNT Control Register (located in the processor IA32_THERM_CONTROL MSR) is written to a '1', the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI P_CNT Control Register. In On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Thermal Monitor. If the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

5.2.3 PROCHOT# Signal

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If the Thermal Monitor is enabled (note that the Thermal Monitor must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. Refer to the *Intel Architecture Software Developer's Manuals* for specific register and programming details.

The Pentium 4 processor Extreme Edition in the 775-land package implements a bi-directional PROCHOT# capability to allow system designs to protect various components from over-temperature situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

One application of PROCHOT# is the thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR can cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR, and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its Thermal Design Power. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss. Refer to he *Voltage Regulator-Down (VRD) 10.1 Design Guide for Desktop and Transportable Socket 775* for details on implementing the bi-directional PROCHOT# feature. Contact your Intel representative for further details and documentation.

5.2.4 THERMTRIP# Signal

Regardless of whether or not the Thermal Monitor feature is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Table 4-3). At this point, the FSB signal THERMTRIP# will go active and stay active as described in Table 4-3. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. If THERMTRIP# is asserted, processor core voltage (V_{CC}) must be removed within the timeframe defined in Table 2-7.

5.2.5 Thermal Diode

The processor incorporates an on-die thermal diode. A thermal sensor located on the system board may monitor the die temperature of the processor for thermal management/long term die temperature change purposes. Table 5-2 and Table 5-3 provide the diode parameter and interface specifications. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 5-2. Thermal Diode Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5	—	300	µA	1
n	Diode Ideality Factor	1.0011	1.0021	1.0030	—	2, 3, 4
R_T	Series Resistance	—	3.64	—	Ω	2, 3, 5

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized at 75 °C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

   $$I_{FW} = I_S * (e^{qV_D/nkT} - 1)$$

   where I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, R_T, is provided to allow for a more accurate measurement of the diode temperature. R_T, as defined, includes the lands of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. R_T can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:

   $$T_{error} = [R_T * (N-1) * I_{FWmin}] / [nk/q * \ln N]$$

   where: T_{error} = sensor temperature error, N = sensor current ratio, k = Boltzmann Constant, q = electronic charge.

Table 5-3. Thermal Diode Interface

Signal Name	Land Number	Signal Description
THERMDA	AL1	diode anode
THERMDC	AK1	diode cathode

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6 Features

This chapter contains power-on configuration options and clock control/low power state descriptions.

6.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The Pentium 4 processor Extreme Edition in the 775-land package samples the hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, refer to Table 6-1.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor; for reset purposes, the processor does not distinguish between a “warm” reset and a “power-on” reset.

Table 6-1. Power-On Configuration Option Signals

Configuration Option	Signal[1]
Output tristate	SMI#
Execute BIST	INIT#
In Order Queue pipelining (set IOQ depth to 1)	A7#
Disable MCERR# observation	A9#
Disable BINIT# observation	A10#
APIC Cluster ID (0-3)	A[12:11]#
Disable bus parking	A15#
Disable Hyper-Threading Technology	A31#
Symmetric agent arbitration ID	BR0#

NOTES:

1. Asserting this signal during RESET# will select the corresponding option.

6.2 Clock Control and Low Power States

The processor allows the use of AutoHALT, Stop-Grant, and Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 6-1 for a visual representation of the processor low power states.

6.2.1 Normal State—State 1

This is the normal operating state for the processor.

6.2.2 AutoHALT Powerdown State—State 2

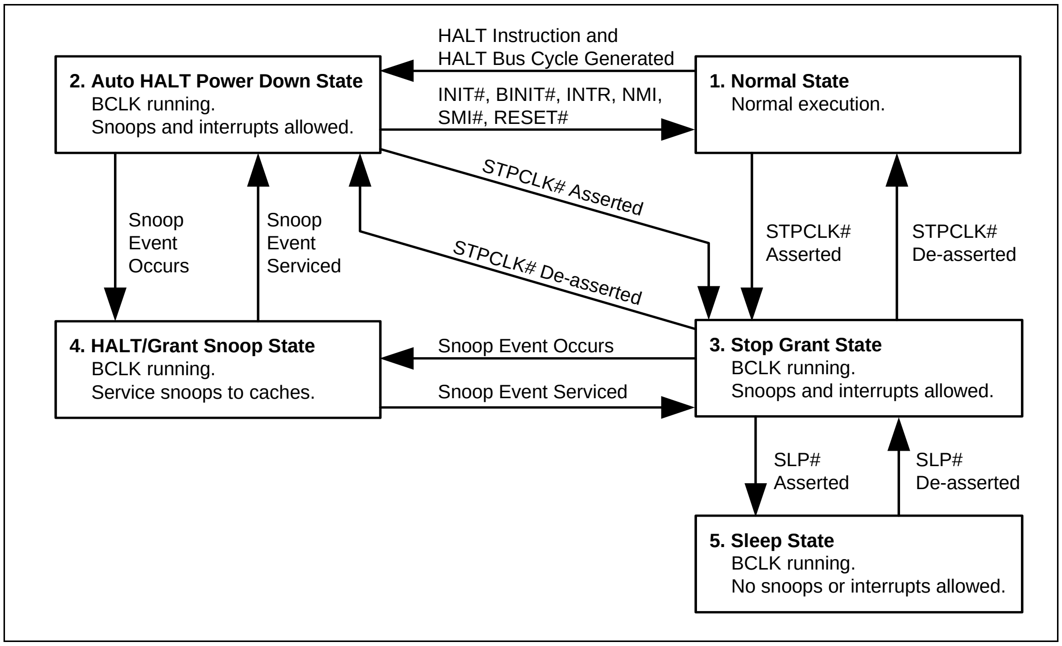
AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system de-asserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Power Down state, the processor will process FSB snoops and interrupts.

Figure 6-1. Stop Clock State Machine



6.2.3 Stop-Grant State—State 3

When the STPCLK# signal is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle.

Since the GTL+ signal receive power from the FSB, these signals should not be driven (allowing the level to return to V_{CC}) for minimum power drawn by the termination resistors in this state. In addition, all other input signals on the FSB should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop Grant state.

RESET# causes the processor to immediately initialize itself, but the processor stays in Stop-Grant state. A transition back to the Normal state occurs with the de-assertion of the STPCLK# signal. When re-entering the Stop Grant state from the Sleep state, STPCLK# should only be de-asserted one or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state occurs when the processor detects a snoop on the FSB (see Section 6.2.4). A transition to the Sleep state (see Section 6.2.5) occurs with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, BINIT# and LINT[1:0] are latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor processes snoops on the FSB and latches interrupts delivered on the FSB.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

6.2.4 HALT/Grant Snoop State—State 4

The processor responds to snoop or interrupt transactions on the FSB while in Stop-Grant state or in AutoHALT Power Down state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor stays in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor returns to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

6.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the processor enters the Sleep state upon the assertion of the SLP# signal. The SLP# signal should only be asserted when the processor is in the Stop Grant state. SLP# assertions while the processor is not in the Stop Grant state is out of specification and may result in erroneous processor operation.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the FSB while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# signal specification, then the processor resets itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be de-asserted immediately after RESET# is asserted to ensure the processor correctly executes the reset sequence.

Once in the Sleep state, the SLP# signal must be de-asserted if another asynchronous FSB event needs to occur. The SLP# signal has a minimum assertion of one BCLK period.

When the processor is in the Sleep state, it does not respond to interrupts or snoop transactions.

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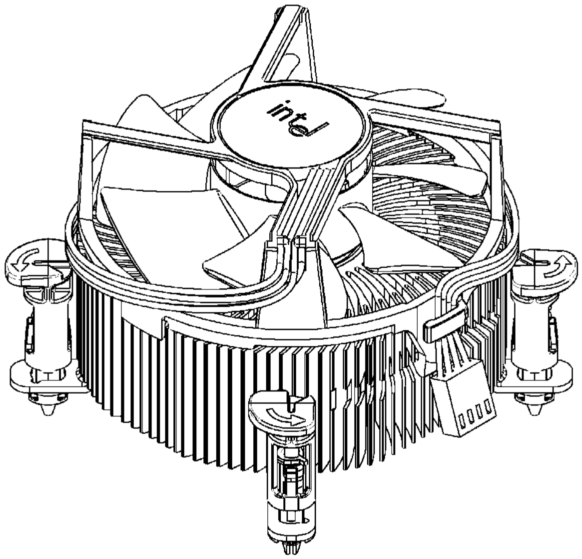
7 Boxed Processor Specifications

The Pentium 4 processor Extreme Edition in the 775-land package will also be offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from baseboards and standard components. The boxed Pentium 4 processor Extreme Edition in the 775-land package will be supplied with a cooling solution. This chapter documents baseboard and system requirements for the cooling solution that will be supplied with the boxed Pentium 4 processor Extreme Edition in the 775-land package. This chapter is particularly important for OEMs that manufacture baseboards for system integrators. Figure 7-1 shows a mechanical representation of a boxed Pentium 4 processor Extreme Edition in the 775-land package.

Note: Unless otherwise noted, all figures in this chapter are dimensioned in millimeters and inches [in brackets].

Note: Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designer's responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platforms and chassis. Refer to the *Intel® Pentium® 4 Processor Extreme Edition on 0.13 Micron Process in the 775-land package Thermal Design Guide*.

Figure 7-1. Mechanical Representation of the Boxed Processor



NOTE: The airflow of the fan heatsink is into the center and out of the sides of the fan heatsink.

7.1 Mechanical Specifications

7.1.1 Boxed Processor Cooling Solution Dimensions

This section documents the mechanical specifications of the boxed Pentium 4 processor Extreme Edition in the 775- land package fan heatsink. The boxed processor will be shipped with an unattached fan heatsink. Figure 7-2 shows a mechanical representation of the boxed Pentium 4 processor Extreme Edition in the 775-land package.

Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor with assembled fan heatsink are shown in Figure 7-2 (Side View), and Figure 7-3 (Top View). The airspace requirements for the boxed processor fan heatsink must also be incorporated into new baseboard and system designs. Airspace requirements are shown in Figure 7-7 and Figure 7-8. Note that some figures have center lines shown (marked with alphabetic designations) to clarify relative dimensioning.

Figure 7-2. Space Requirements for the Boxed Processor (Side View)

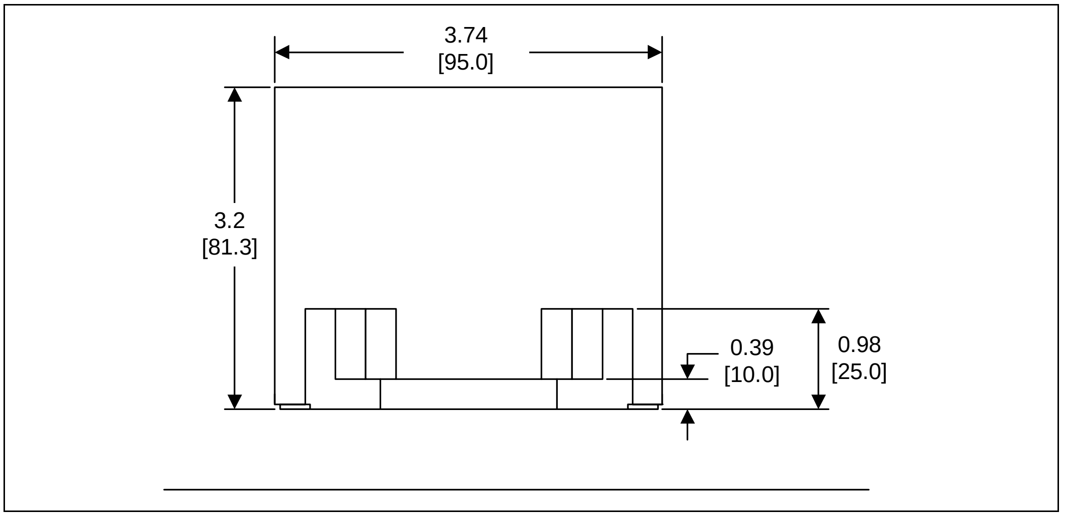
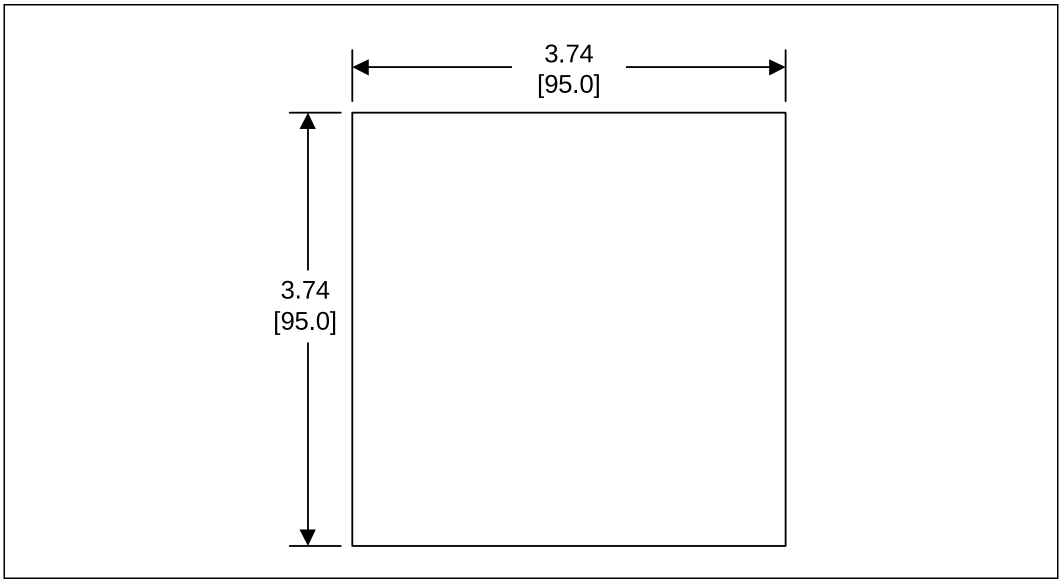


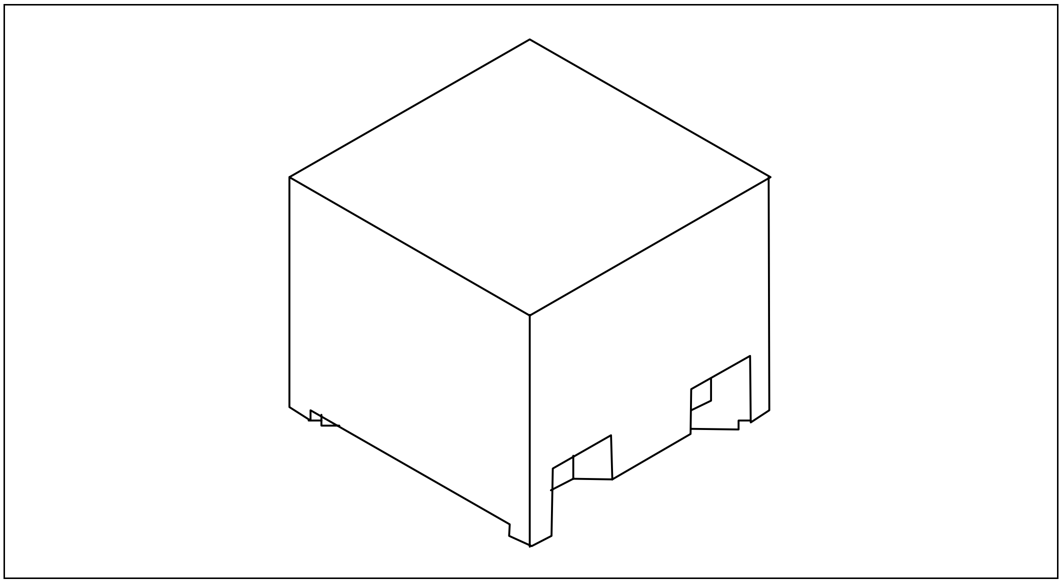
Figure 7-3. Space Requirements for the Boxed Processor (Top View)



NOTES:

1. Diagram does not show the attached hardware for the clip design and is provided only as a mechanical representation.

Figure 7-4. Space Requirements for the Boxed Processor (Overall View)



7.1.2 Boxed Processor Fan Heatsink Weight

The boxed processor fan heatsink will not weigh more than 450 grams. Refer to Chapter 5 and the *Intel® Pentium® 4 Processor Extreme Edition on 0.13 Micron Process in the 775-land package Thermal Design Guide* for details on the processor weight and heatsink requirements.

7.1.3 Boxed Processor Retention Mechanism and Heatsink Attach Clip Assembly

The boxed processor thermal solution requires a heatsink attach clip assembly to secure the processor and fan heatsink in the baseboard socket. The boxed processor will ship with the heatsink attach clip assembly.

7.2 Electrical Requirements

7.2.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12 V power supply. An attached fan power cable will be shipped with the boxed processor to draw power from a power header on the baseboard. The power cable connector and pinout are shown in Figure 7-5. Baseboards must provide a matched power header to support the boxed processor. Table 7-1contains specifications for the input and output signals at the fan heatsink connector.

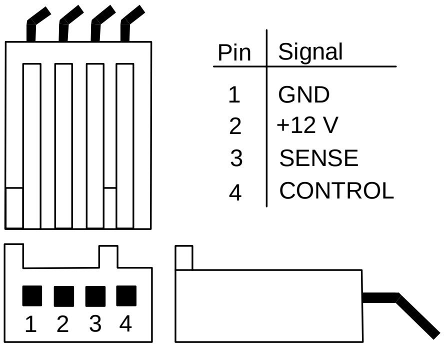
The fan heatsink outputs a SENSE signal that is an open- collector output that pulses at a rate of 2 pulses per fan revolution. A baseboard pull-up resistor provides V_{OH} to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The Pentium 4 processor Extreme Edition manufactured on the 0.13 micron process technology does not support T-diode based fan speed control hence the 4th pin (labeled CONTROL) of the fan connector for this processor is null. (The fan speed will be controlled by the integrated fan controller)

Note: The boxed processor’s fan heatsink requires a constant +12 V supplied to pin 2 and does not support variable voltage control or 3-pin PWM control.

The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. Figure 7-6 shows the location of the fan power connector relative to the processor socket. The baseboard power header should be positioned within 4.33 inches from the center of the processor socket.

Figure 7-5. Boxed Processor Fan Heatsink Power Cable Connector Description



Pin	Signal
1	GND
2	+12 V
3	SENSE
4	CONTROL

Straight square pin, 4-pin terminal housing with polarizing ribs and friction locking ramp.

0.100" pitch, 0.025" square pin width.

Match with straight pin, friction lock header on mainboard.

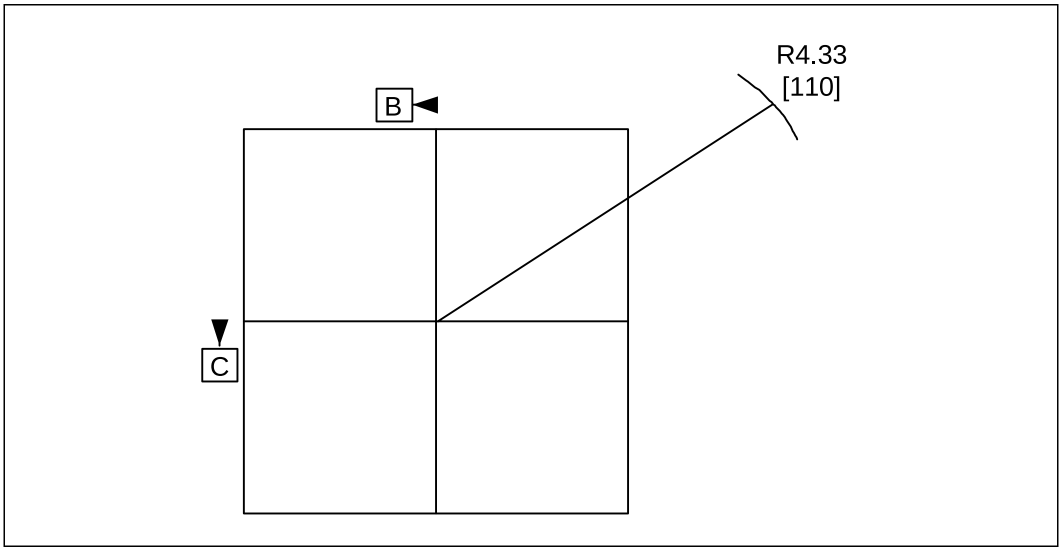
Table 7-1. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max	Unit	Notes
+12 V: 12 volt fan power supply	10.2	12	13.8	V	—
IC: • Peak Fan current draw • Fan start-up current draw • Fan start-up current draw maximum duration	—	1.1	1.5 2.2 1.0	A A Second	—
SENSE: SENSE frequency	—	2	—	pulses per fan revolution	1
CONTROL	null	null	null		2

NOTES:

1. Baseboard should pull this pin up to 5 V with a resistor.
2. The Pentium 4 processor Extreme Edition on the 0.13 micron process technology does not support T-diode based fan speed control hence the 4th pin (labeled CONTROL) of the fan connector for this processor is null.

Figure 7-6. Baseboard Power Header Placement Relative to Processor Socket



7.3 Thermal Specifications

This section describes the cooling requirements of the fan heatsink solution used by the boxed processor.

7.3.1 Boxed Processor Cooling Requirements

The boxed processor may be directly cooled with a fan heatsink. However, meeting the processor's temperature specification is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is found in Chapter 5. The boxed processor fan heatsink is able to keep the processor temperature within the specifications (see Table 5-1) in chassis that provide good thermal management. For the boxed processor fan heatsink to operate properly, it is critical that the airflow provided to the fan heatsink is unimpeded. Airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 7-7 and Figure 7-8 illustrate an acceptable airspace clearance for the fan heatsink. The air temperature entering the fan should be kept below 38 °C. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

Note: The processor fan is the primary source of airflow for cooling the Vcc voltage regulator. Dedicated voltage regulator cooling components may be necessary if the selected fan is not capable of keeping regulator components below maximum rated temperatures.

Figure 7-7. Boxed Processor Fan Heatsink Airspace Keep-out Requirements (Top View)

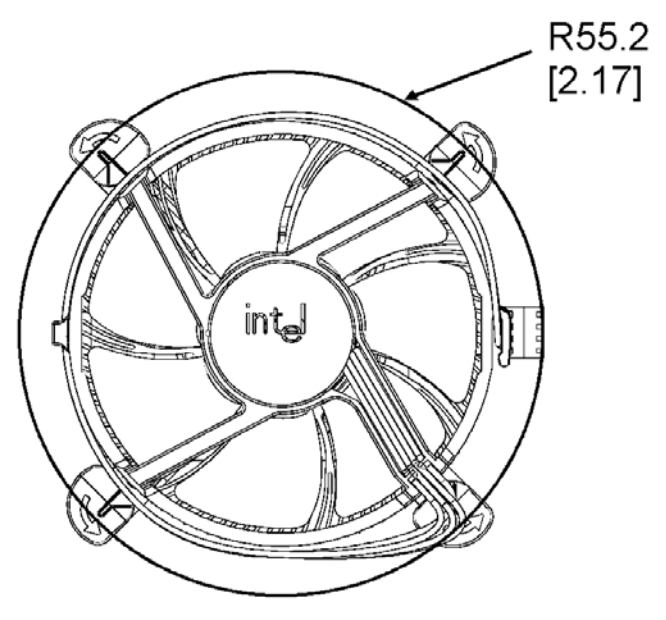
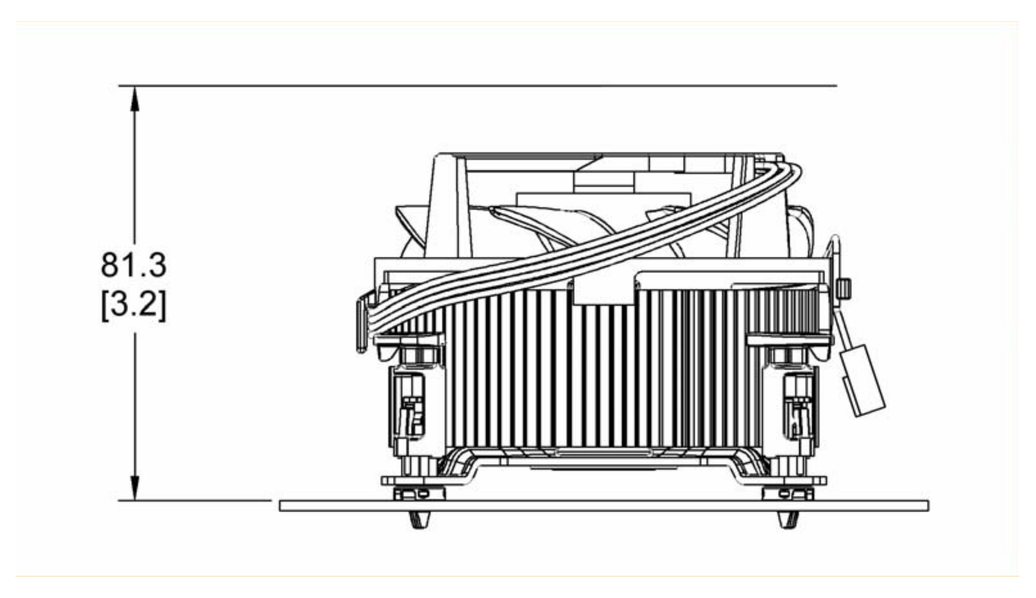


Figure 7-8. Boxed Processor Fan Heatsink Airspace Keep-out Requirements (Side View)



7.3.2 Variable Speed Fan

The boxed processor fan will operate at different speeds over a short range of internal chassis temperatures. This allows the processor fan to operate at a lower speed and noise level, while internal chassis temperatures are low. If internal chassis temperature increases beyond a lower set point, the fan speed will rise linearly with the internal temperature until the higher set point is reached. At that point, the fan speed is at its maximum. As fan speed increases, so does fan noise levels. Systems should be designed to provide adequate air around the boxed processor fan heatsink that remains cooler then lower set point. These set points, represented in Figure 7-9 and Table 7-2, can vary by a few degrees from fan heatsink to fan heatsink. The internal chassis temperature should be kept below 38ºC. Meeting the processor's temperature specification (see Chapter 5) is the responsibility of the system integrator.

Note: The motherboard must supply a constant +12 V to the processor's power header to ensure proper operation of the variable speed fan for the boxed processor (refer to Table 7-1) for the specific requirements).

Figure 7-9. Boxed Processor Fan Heatsink Set Points

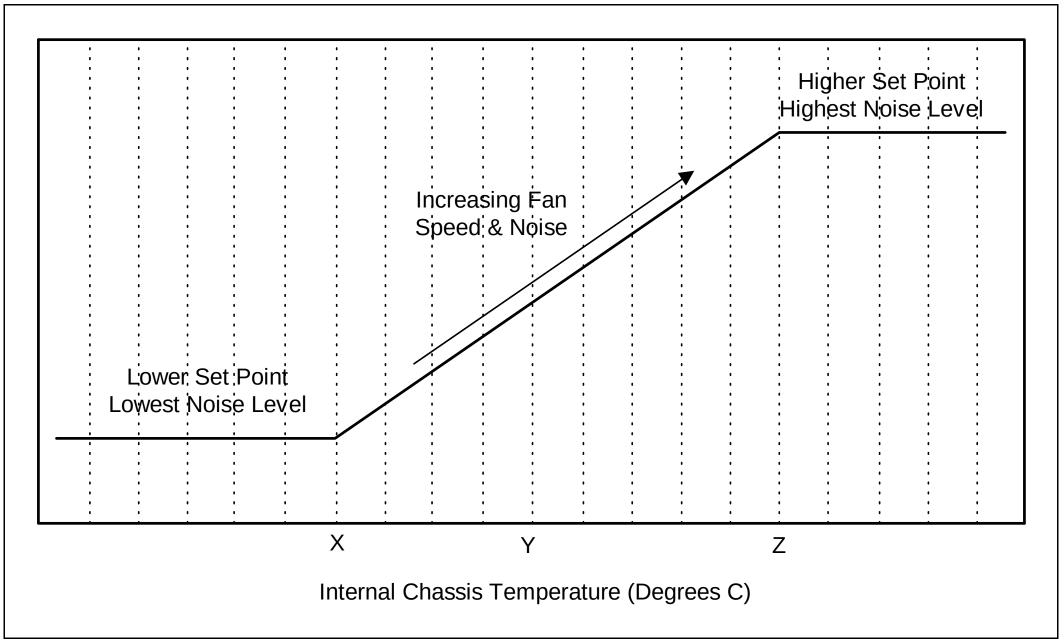


Table 7-2. Boxed Processor Fan Heatsink Set Points

Boxed Processor Fan Heatsink Set Point (ºC)	Boxed Processor Fan Speed	Notes
X ≤ 30	When the internal chassis temperature is below or equal to this set point, the fan operates at its lowest speed. Recommended maximum internal chassis temperature for nominal operating environment.	1
Y = 34	When the internal chassis temperature is at this point, the fan operates between its lowest and highest speeds. Recommended maximum internal chassis temperature for worst-case operating environment.	—
Z ≥ 38	When the internal chassis temperature is above or equal to this set point, the fan operates at its highest speed.	1

NOTES:

1. Set point variance is approximately ±1°C from fan heatsink to fan heatsink.

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8 Debug Tools Specifications

Refer to the *ITP700 Debug Port Design Guide* for information regarding debug tools specifications. The *ITP700 Debug Port Design Guide* is located on http://developer.intel.com.

8.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Pentium 4 processor Extreme Edition in the 775-land package systems. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Pentium 4 processor Extreme Edition in the 775-land package systems, the LAI is critical in providing the ability to probe and capture FSB signals. There are two sets of considerations to keep in mind when designing a Pentium 4 processor Extreme Edition in the 775-land package system that can make use of an LAI: mechanical and electrical.

8.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the Pentium 4 processor Extreme Edition in the 775-land package. The LAI lands plug into the socket, while the Pentium 4 processor Extreme Edition in the 775-land package lands plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Pentium 4 processor Extreme Edition in the 775-land package and a logic analyzer. The maximum volume occupied by the LAI, known as the keep-out volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the Pentium 4 processor Extreme Edition in the 775-land package heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

8.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the FSB; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

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