423 Pin Socket (PGA423)

Design Guidelines

November, 2000
Order Number: *249207-001*

LIST OF FIGURES

423 Pin Socket Design Guidelines

1. INTRODUCTION

1.1. Objective:

This document defines a ZIF (Zero Insertion Force) socket intended for desktop and workstation platforms based on the Intel® Pentium® 4 microprocessor. The socket provides I\O, power and ground contacts and must be low cost, low risk, robust, high volume manufacturable (HVM), and multi-sourceable. This socket has 423 contacts with a pitch of 100mil and an interstitial pattern that mates with the pins on the Pentium 4 processor package.

1.2. Purpose:

To define the functional, quality, reliability, and material (that is, visual, dimensional and physical) requirements and specifications of the 423 Pin Socket. To provide a 423 Pin Socket which meets or exceeds applicable standards and specifications.

1.3. Scope:

This specification applies to all 423-pin ZIF sockets designed to the requirements of this specification.

2. PROCESSOR PACKAGE DESCRIPTION

Information provided in this section is to ensure dimensional compatibility of the 423 Pin Socket with that of the Intel® Pentium® 4 processor. The processor must be inserted into the 423 pin socket with zero insertion force when the lever arm is not actuated.

2.1. Package Outline:

The outline of the package that can be used with the 423 Pin Socket is illustrated in Figure 1. This drawing does not include potential heat sinks since these are used at the OEM's discretion. Specific details should be obtained from Intel® Pentium® 4 Processor In the 423-Pin Package Datasheet.

2.2. Pin Dimensions:

Details of the pin dimensions are shown in Figure 2. The package Critical To Function (CTF) Dimensions from the socket interface perspective are presented in Table 1.

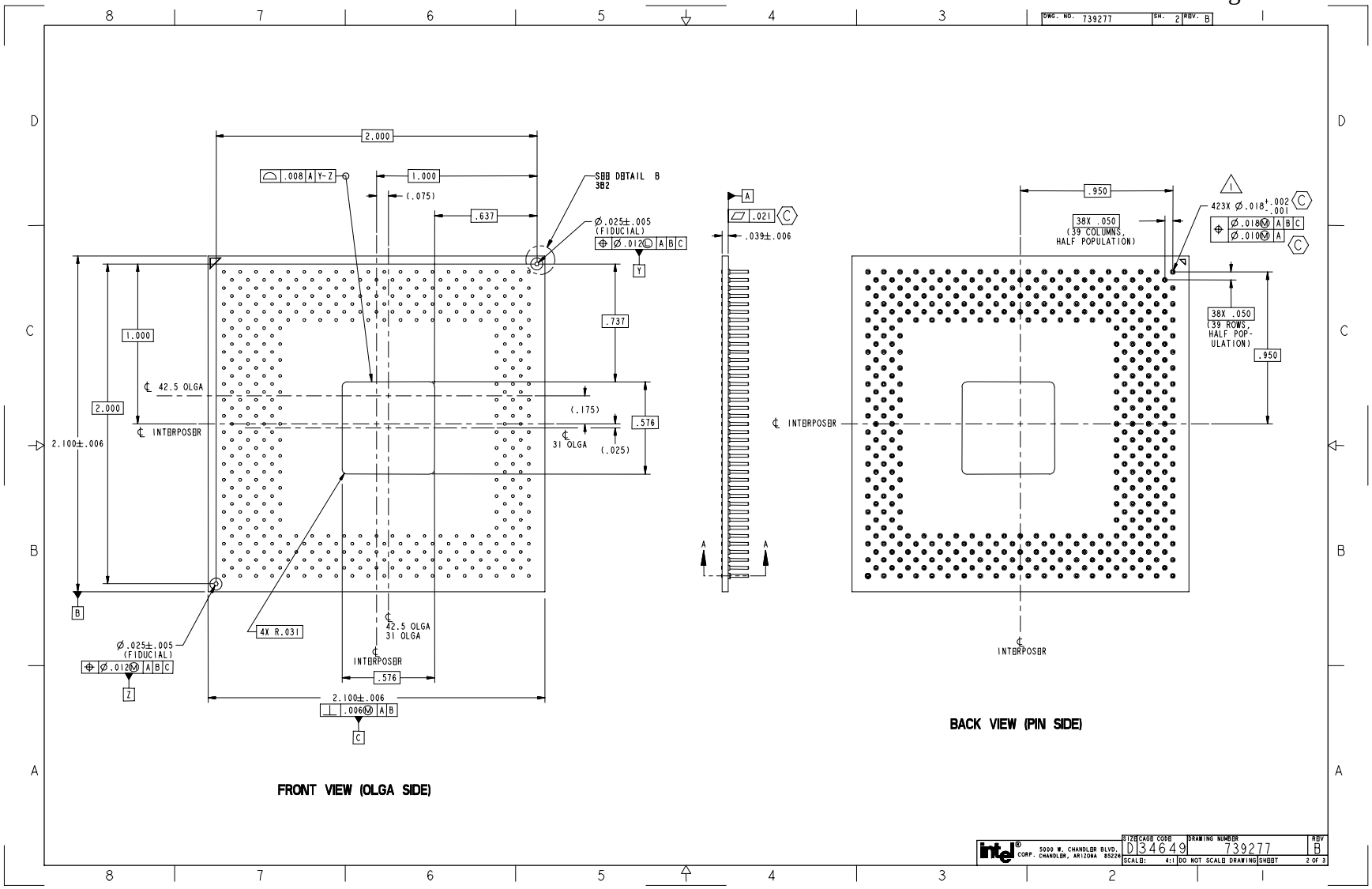
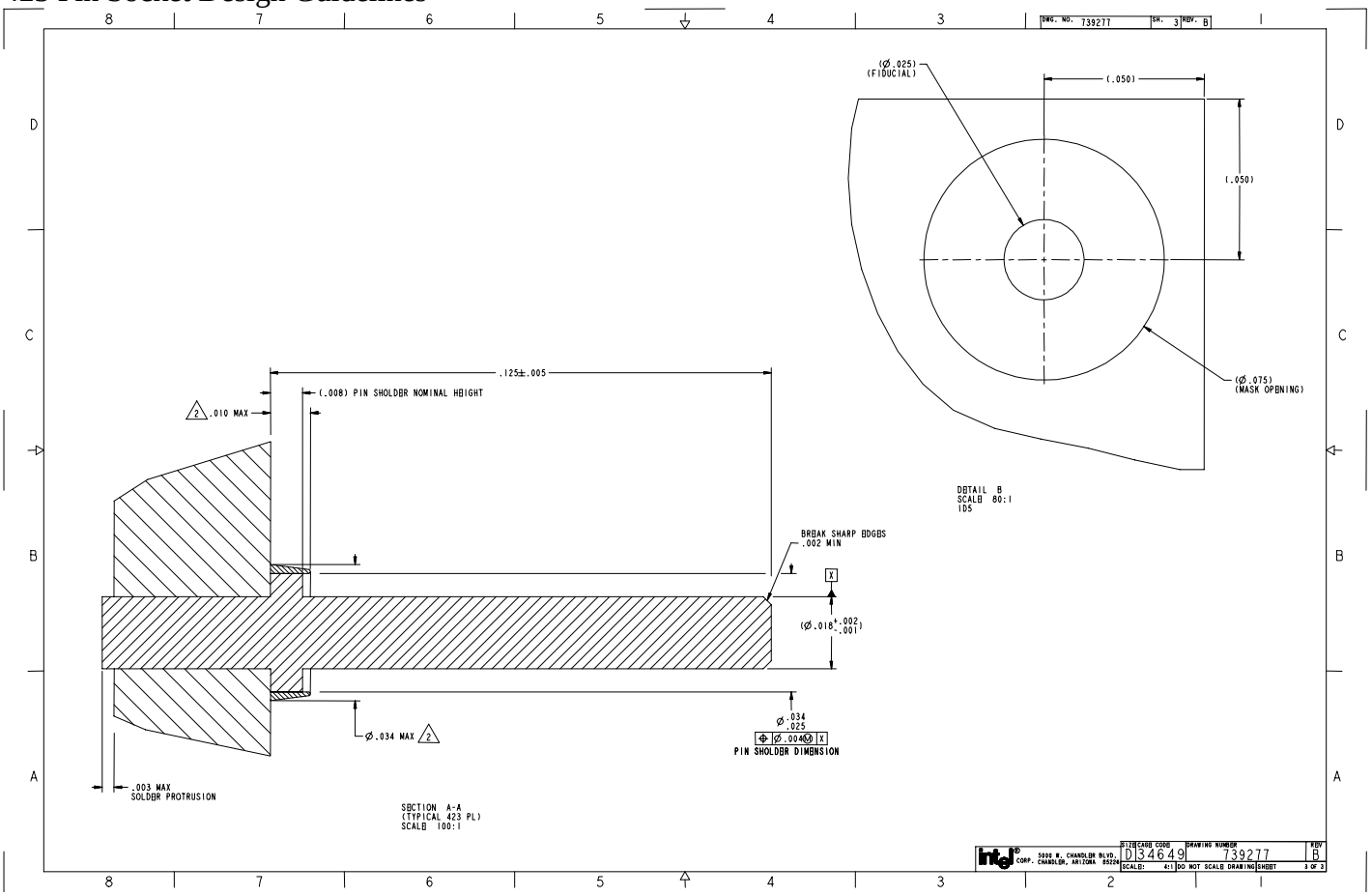


Figure 1: Outline of the Intel® Pentium® 4 Processor Package

Note: Dimensions Shown in Inches



Note: Dimensions Shown In Inches

Figure 2: Intel® Pentium® 4 Processor Package Pin Field Pin Details

Table 1: Package Critical To Function (CTF) Dimensions

Dimension	Minimum in	Maximum in
Shoulder Diameter keep out (Land Solder Fillet Shoulder Inclusion)	N/A	0.034 max
Pin Diameter	0.017	0.020
Shoulder Diameter Protrusion (Land Solder Fillet Shoulder Inclusion)	N/A	0.010
Pin Length*	0.120	0.130
Pin TP	N/A	0.010
Flatness of package across the total length of package diagonal	N/A	0.021

3. MECHANICAL REQUIREMENTS

3.1. Pin-Out and Orientation Diagram:

The pin-out for the 423 pin socket is shown in Figure 3. This diagram is viewed from the TOP of the SOCKET. The socket dimensions, the tab and stopper details are provided in Figure 4, Figure 5, and Figure 6.

3.2. Mechanical Supports:

Socket tabs shall be used with a heat sink clip to isolate the mass of the package and the associated heat sink from the socket during the shock and vibration conditions outlined in Sections 5.3 and 5.4. The socket must pass the mechanical shock and vibration requirements listed in Sections 5.3 and 5.4 with the associated mass of 300g (max) for socket attach, and 450g (max) for retention module support.

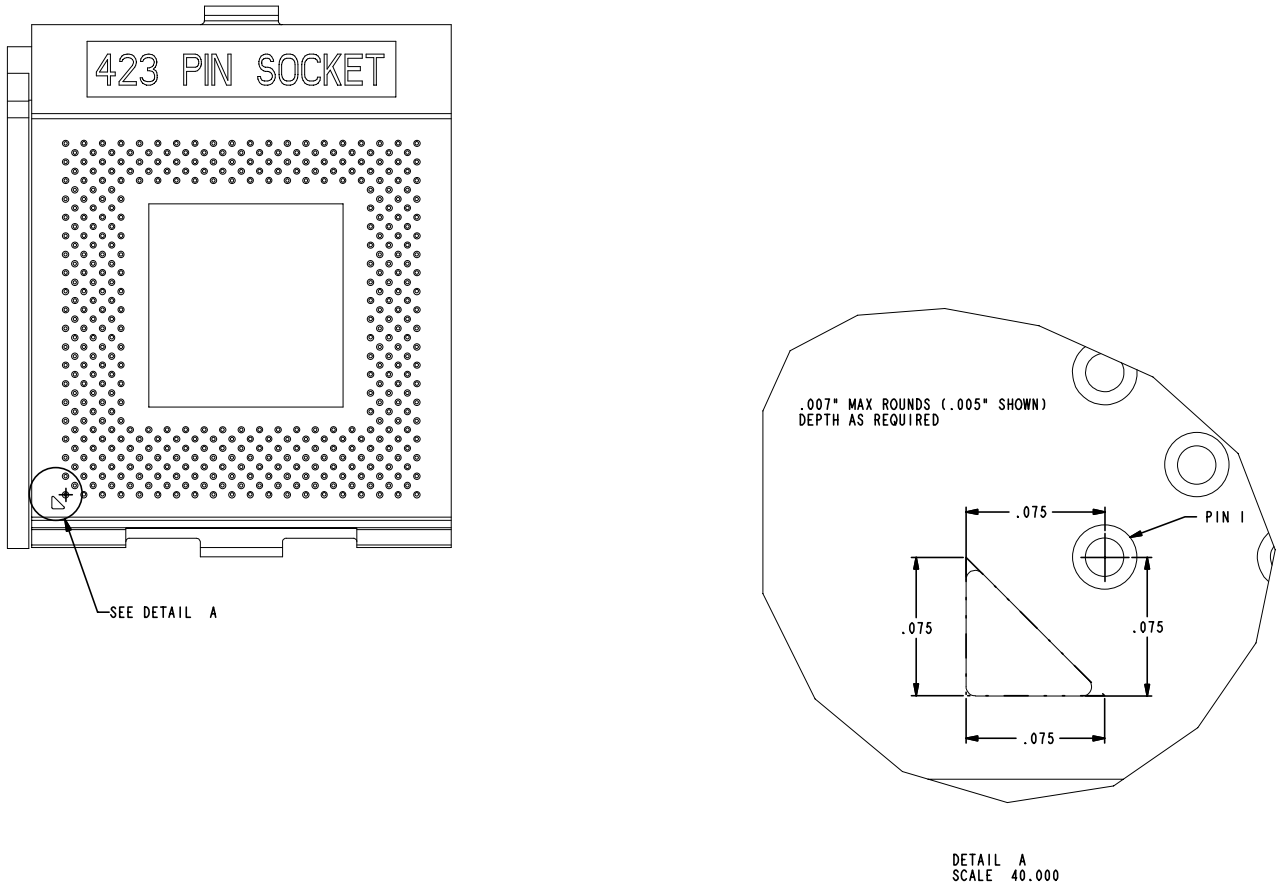


Figure 3: Top View Of The Socket nd Pin One Indicator.

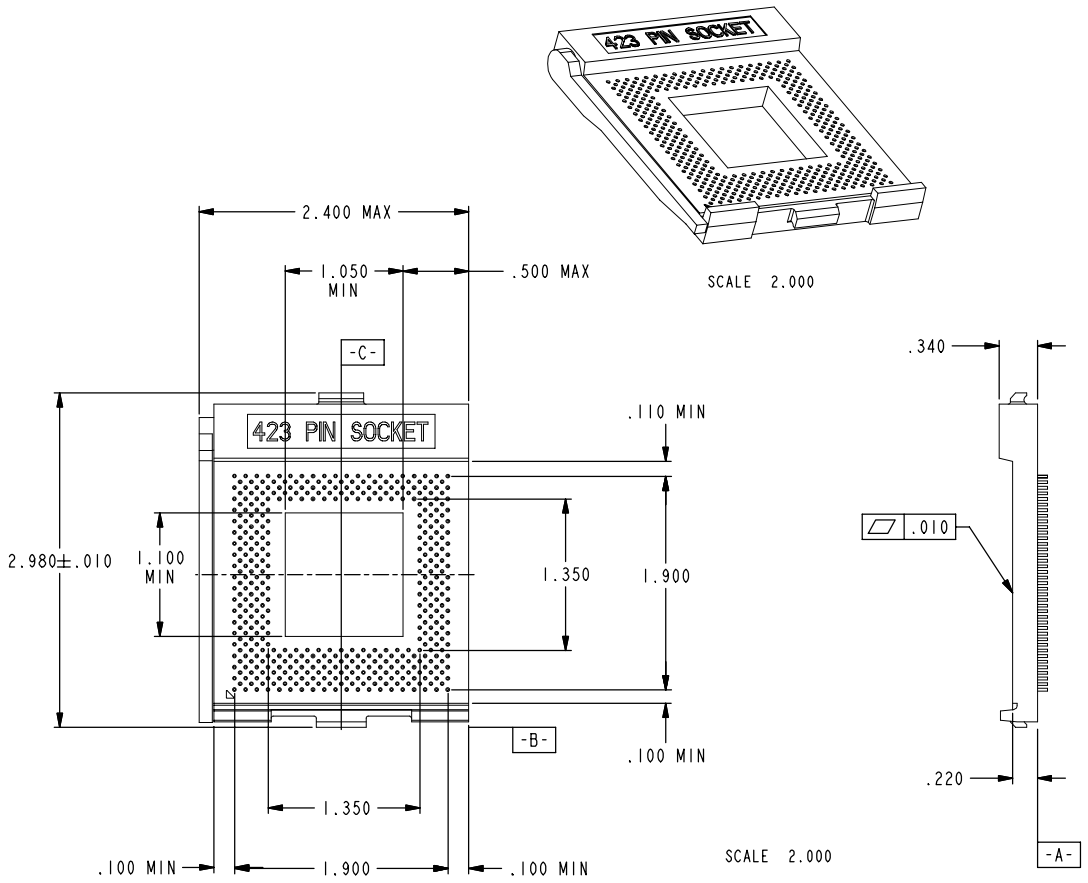


Figure 4: 423 Pin Socket Dimensions

Note: Dimensions shown in inches

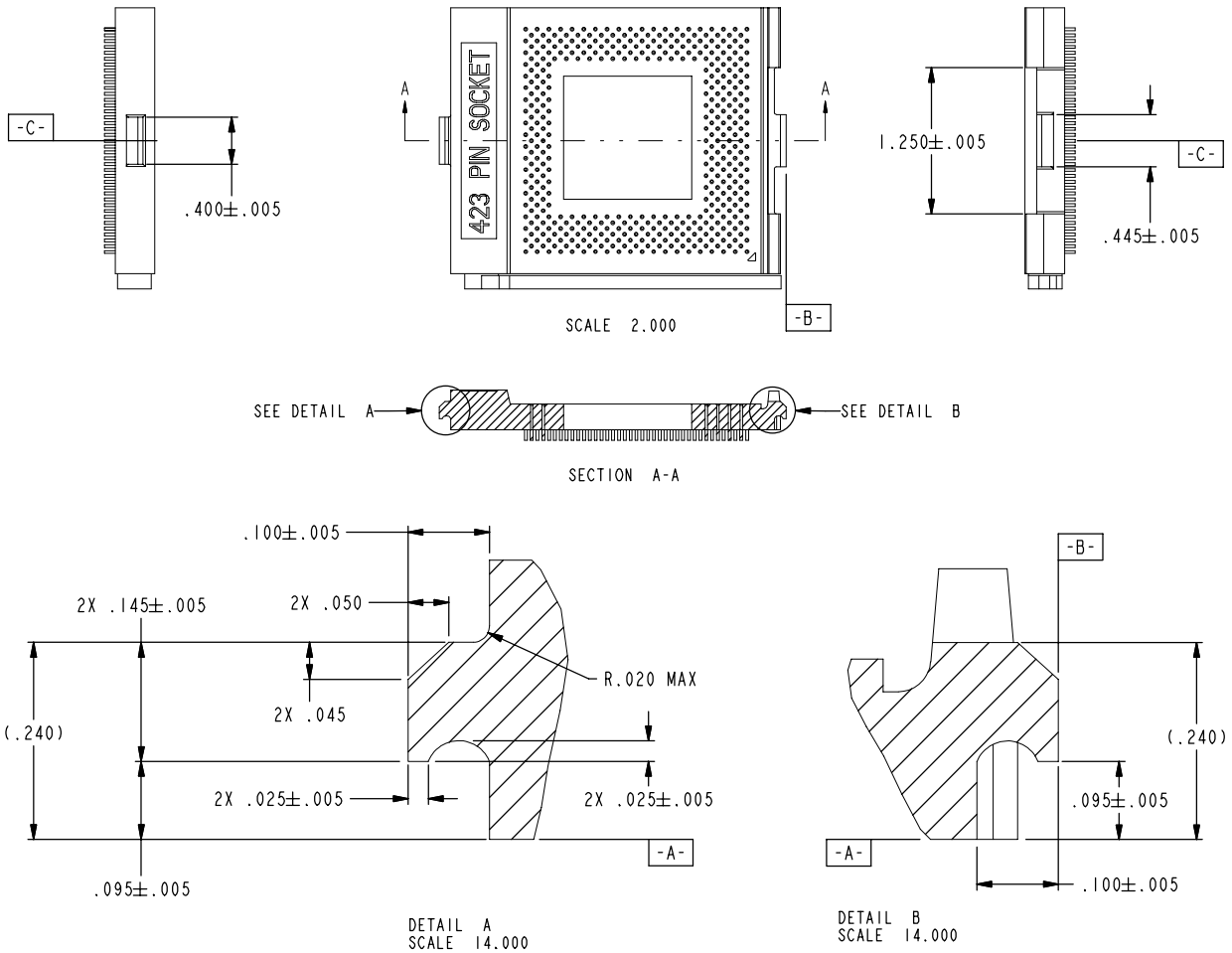


Figure 5: Socket Tab Geometry and Dimensions

Note: Dimensions shown in inches

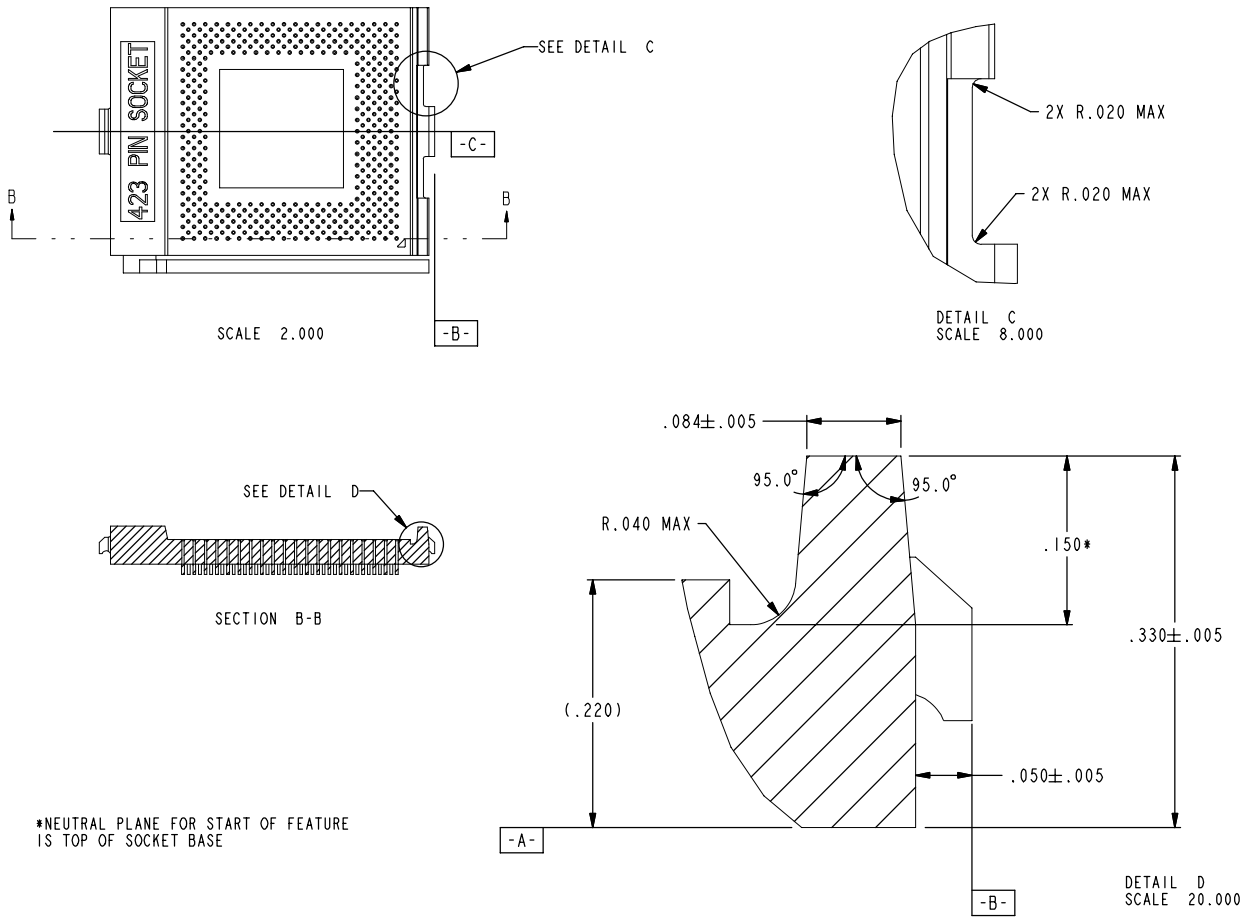


Figure 6: Socket Stopper Geometry and Dimensions

Note: Dimensions shown in inches

3.3. Materials:

3.3.1. Socket Housing:

Liquid Crystal Polymer (LCP), UL 94V-0, or equivalent. Flame rating, temperature rating and design capable of withstanding reflow solder process per Section 5.8.

3.3.2. Color:

The 423 Pin Socket will have uniform color. The color requirement does not apply to the actuation lever arm.

3.3.3. Markings:

3.3.3.1.Name:

423 Pin Socket (Font type is Helvetica - 16 point Bold).

This mark shall be molded or laser marked into the top of the cam housing.

Manufacturer's insignia (font size at supplier's discretion).

This mark shall be molded or laser marked into the socket housing. Both marks must be visible when first seated in the motherboard. The marks must pass the reflow solder process of Section 5.8 and the solvent resistance test in Section 5.11. Any requests for variation from this marking requires a written description (detailing size and location) to be provided to Intel for approval.

3.3.3.2.Lot Traceability:

Each socket will be marked with lot identification code that will allow traceability of all components, date of manufacture (year and week), and assembly location. This mark can be an ink mark or a laser mark but must be able to withstand a temperature of 225°C for 40s (minimum) per Section 5.8 and must pass the solvent resistance test in Section 5.11. The mark must be placed on a surface that is visible when mounted on a printed circuit board. In addition, this identification code must be marked on the exterior of the box in which the units ship.

3.3.3.3.Socket Size:

The 423 Pin Socket must fit within 2.400in x 2.990in x 0.230in, allowing full insertion of the pins in the socket, without interference

between the socket and the pin field. Actuation lever arm in locked position must have the same profile as the socket cam and housing, and must not interfere with the heatsink protrusion. The total thickness of the cam house must reside within 0.350in from the bottom surface of the socket.

3.3.3.4. Socket/Package pin field Movement

The socket will be built so that the package pin field displacement will not exceed 0.060in during engagement and disengagement.

3.3.4. Contact Characteristics:

3.3.4.1. Number of contacts:

Total number of contacts: 423

3.3.4.2. Base Material:

High strength copper alloy.

3.3.4.3. Contact Area Plating:

15µin (min) gold plating over 50µin (min) nickel underplate in critical contact areas (area on socket contacts where package pins will mate), and plating must be able to pass the tests outlined in sections 4 and 5.

3.3.4.4. Solder tails plating:

100µin (min) tin lead over 50µin (min) nickel underplate.

3.3.4.5. Lubricants:

No lubricants shall be used on the socket contacts or in the cam.

3.3.5. Environmental Concerns Requirements:

Cadmium shall not be used in the painting or plating of the socket. CFCs and HFCs shall not be used in manufacturing the socket.

3.4. Socket Manufacturability Requirements:

The socket must be a thru-hole socket design.

3.4.1. Overall Assembly Sequence:

Solder socket to motherboard

Insert processor into socket and lock it in using actuation lever.

Assemble heat sink onto the package.

3.4.2. Socket Engagement/Disengagement Force:

The force on the actuation lever arm must not exceed 10 lbf to engage or disengage the package into the 423 Pin Socket. Movement of the cover is limited to the plane parallel to the motherboard.

3.4.3. Visual Aids:

The socket top will have markings identifying open and closed positions for the actuation lever arm.

3.4.4. Solderability Test:

Must pass 95% solder tail coverage per tail

3.5. Assembly Requirements to the Motherboard:

3.5.1. Pre- Solder Attachment:

A method of securing the socket to the motherboard is required to assist in the manufacturing process. The securing method shall be consistent with low-cost, high-volume printed circuit board assembly lines. It is not acceptable to use a retention feature to achieve this goal. The socket pins should be designed to be strong enough to secure the socket to the motherboard during wave soldering.

3.5.2. Solder Tail Design and Alignment:

The socket solder tails must be designed and aligned such that the end of the solder tails must enter a virtual-condition hole that is 0.029in ± 0.003in in diameter.

3.6. Socket Critical To Function (CTF) Dimensions:

The 423 Pin Socket shall accept an Intel® Pentium® 4 processor package as shown in Figure 1 and shall hold the package so that it is parallel with the motherboard. The asymmetric pinout will help to properly align the socket to the motherboard and prevent the socket from being assembled incorrectly to the motherboard.

Critical to function dimensions are identified in Figure 8**.** Each of the dimensions must meet the requirements given in Table 2. These dimensions will be verified as part of the qualification process. (See Table 3) Also, supplier will provide and maintain Critical Process Parameters controlling these CTFs or will provide direct measurements to meet ongoing quality requirements.

Table 2: Socket Critical To Function Dimensions

Dimension	Index	Minimum in	Maximum in
Socket Housing Overall Length	A	2.970	2.990
Socket Housing Overall Width	B	N/A	2.400
Socket Housing Height (pin field)	C	0.210	0.230
Socket Housing Height (cam)	D	0.330	0.350
Socket Flatness – Cover Top	E	N/A	0.010
Socket Through Cavity Length	F	1.100	N/A
Socket Through Cavity Width	G	1.050	N/A
Lever Arm Height in Locked position	H	N/A	0.210 or Must not exceed the cover top surface
Cover Lead-in Chamfer Diameter	HH	Package pin shoulder MUST be fully accommodated in the lead-in feature in the socket cover. 1x inspection.	
Cover Lead-in Chamfer Depth	J		
Cover Pin Hole True Position	K	N/A	0.010
Cover Pin Hole Diameter	L	0.021	N/A
Cover Travel	M	N/A	0.060
Tab1 Length (cam end)	N	0.395	0.405
Tab2 Length (non-cam end)	NN	0.440	0.450
Tab width	P	0.095	0.105
Tab Curvature Depth	Q	0.020	0.030
Tab Height	R	0.140	0.150
Tab Lip Length	S	0.020	0.030
Solder Tail True Position	V	N/A	0.010
Heat sink protrusion height	W	0.325	0.335
Heat sink protrusion width at top	X	0.079	0.089
Heat sink protrusion edge	Y	0.142	0.152
Gap between heat sink protrusions	Z	1.245	1.255
Tab Height from Socket Bottom	AA	0.090	0.100
HS Protrusion Offset from Tab	BB	0.045	0.055
Socket Flatness – Housing Bottom	EE	N/A	0.010

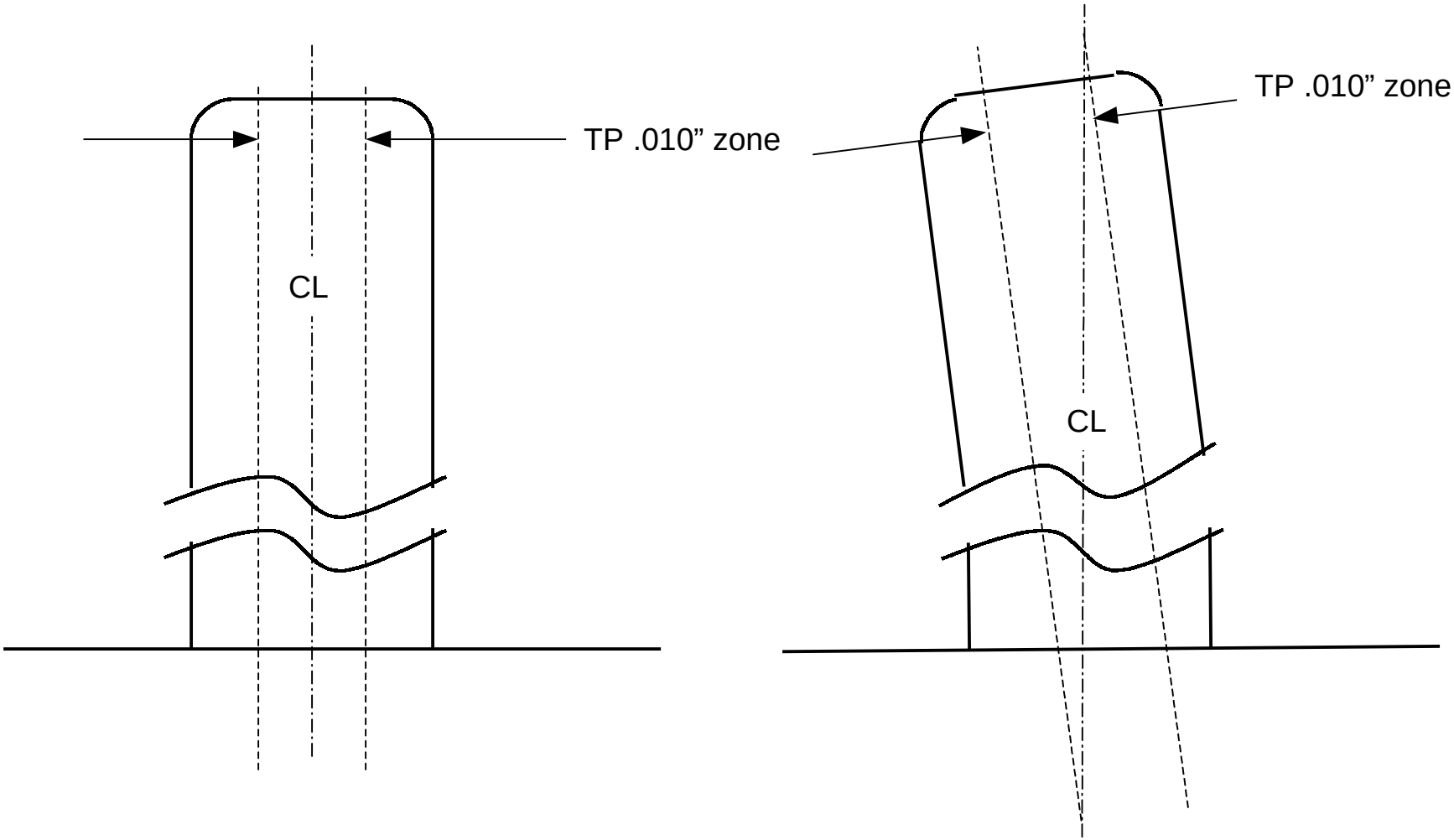


Figure 7: Socket Pin True Position Acceptability

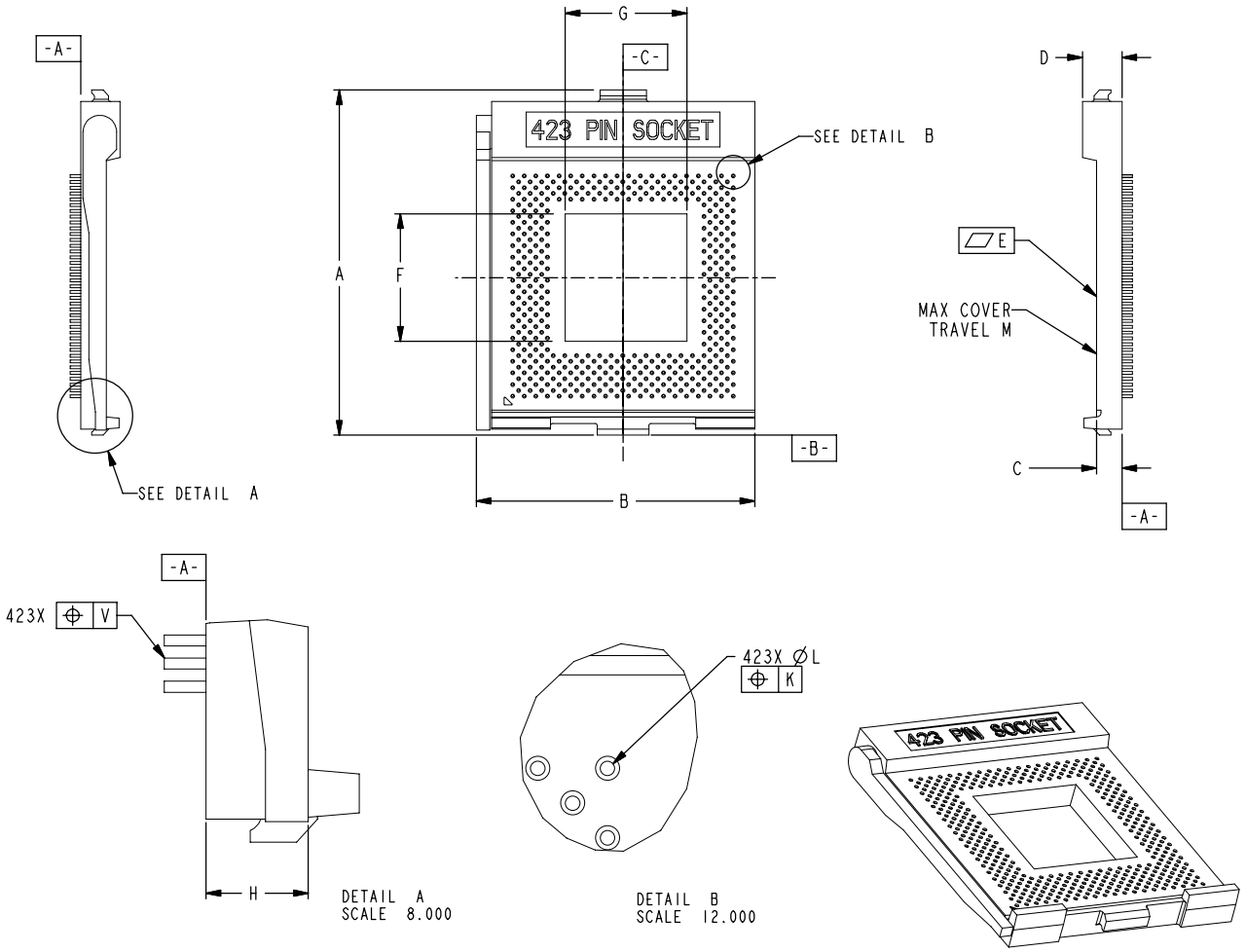


Figure 8: 423 Pin Socket Critical To Function (CTF) Dimensions

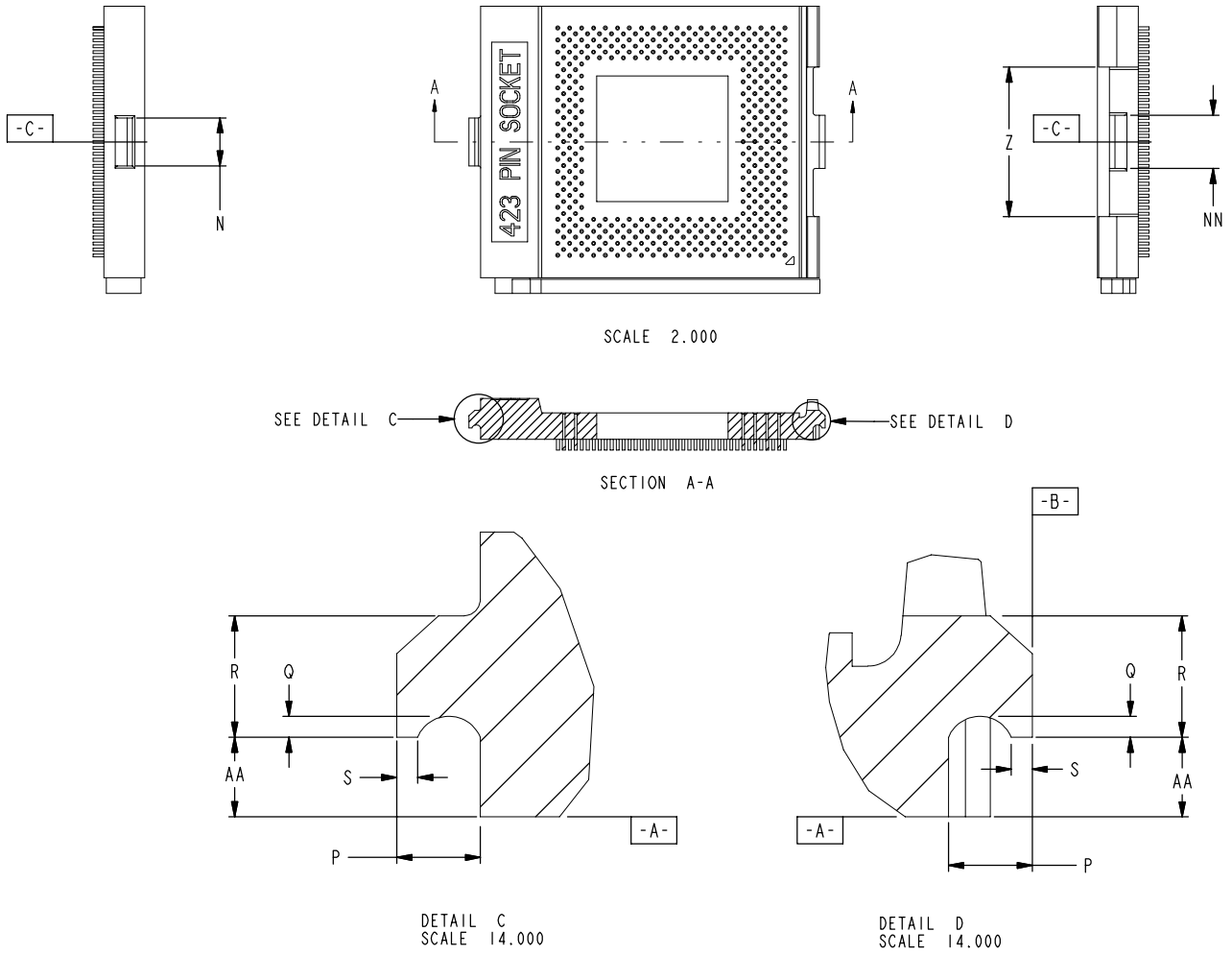


Figure 9: 423 Pin Socket Critical To Function (CTF) Dimensions Details

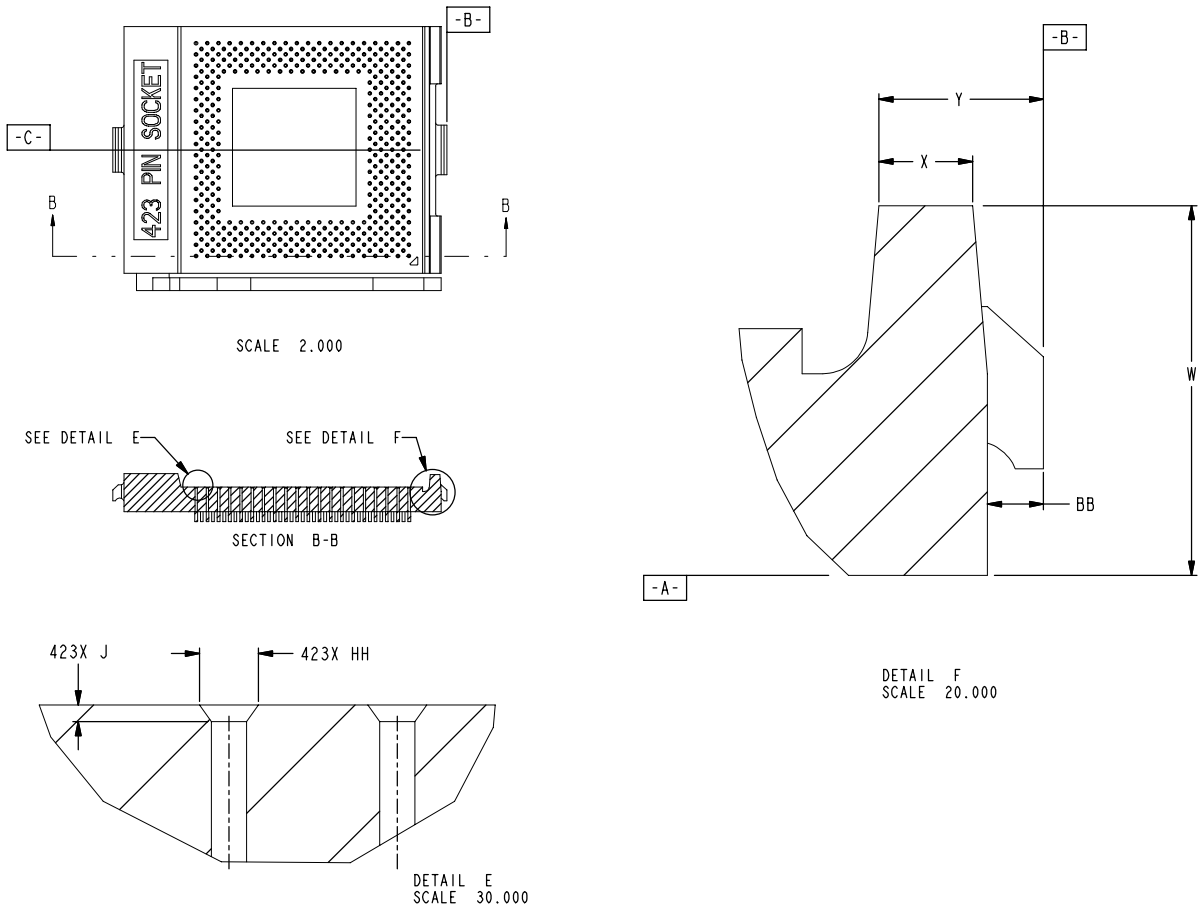
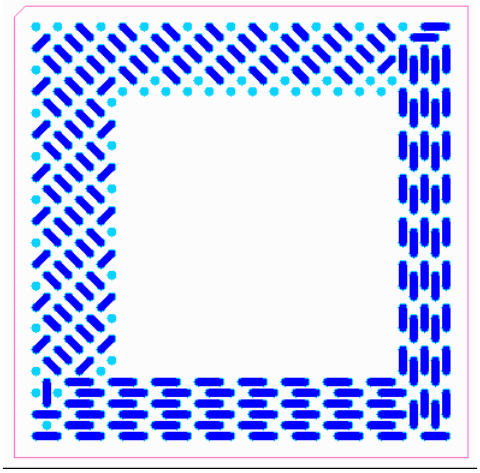


Figure 10: 423 Pin Socket Critical To Function (CTF) Dimensions Details

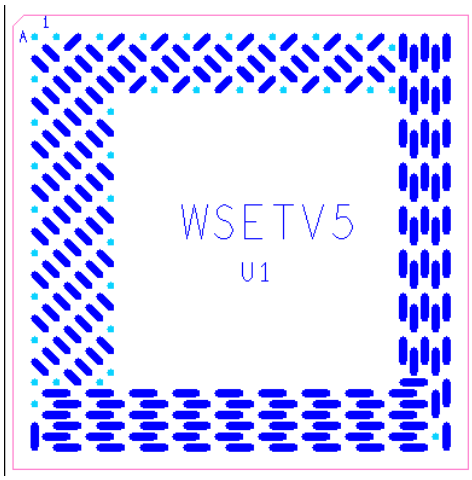
4. ELECTRICAL REQUIREMENTS

Socket electrical requirements are measured from the socket-seating plane of the package to the component side of the socket PCB to which it is attached. All specifications are maximum values (unless otherwise stated) for a single socket pin, but includes effects of adjacent pins where indicated. Pin and socket inductance includes exposed pin from mated contact to bottom of the package pin field.

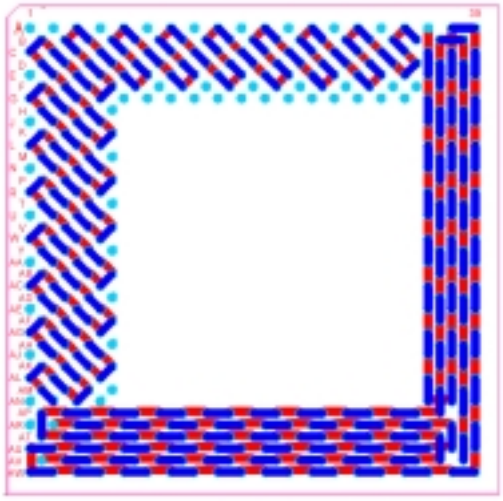
4.1. Electrical Resistance:



Primary Side of the MB



Primary Side of the Package



Superimposed (MB and Package)

Figure 11: Electrical Resistance Fixture

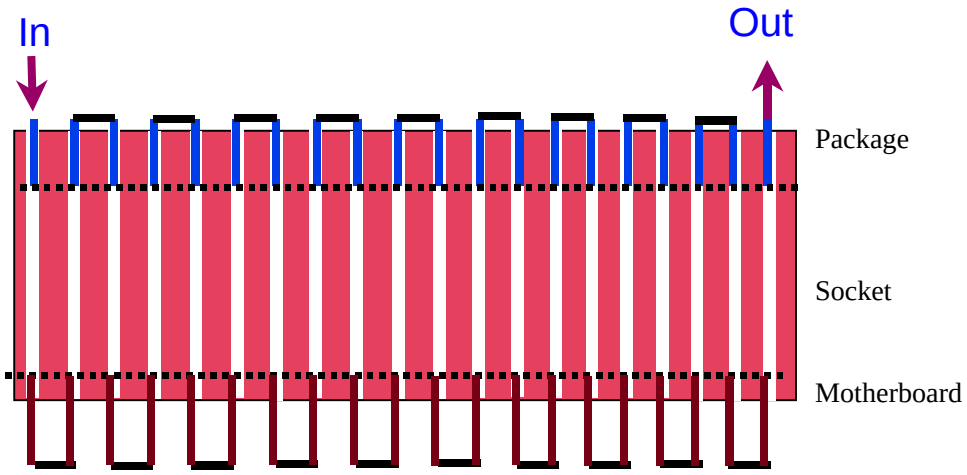


Figure 12: Methodology for Measuring Total Electrical Resistance

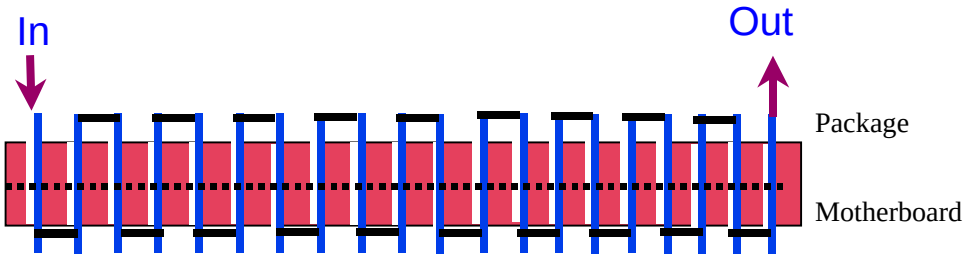


Figure 13: Methodology for Measuring Electrical Resistance of the Jumper

Determination of Average Electrical Resistance:

Figure 12 and Figure 13 show the proposed methodology for measuring the final electrical resistance. The methodology requires measuring package fixtures flush-mounted directly to the motherboard fixtures, so that the pin shoulder is flush with the motherboard, to get the averaged jumper resistance, Rjumper. All measurement should be taken from the solder tail side of the board. The Rjumper should come from a good statistical average of many package fixtures flush mounted to a motherboard fixture. For each chain, one measurement per chain will be taken; there are 3 chains per board. The same measurements are then made with a package fixture mounted on a vendor's socket, and both are mounted on a motherboard fixture; this provides the Rtotal.

Every Rtotal will be applied to equations 1-3, where the Rjumper in the following equations comes from a statistical average of many measurements. The resistance requirement, Rreq, can be calculated for each chain with the measurements as shown in the following equations.

From Pin#	To Pin#		
C35	AR5	Rreq = (Rtotal – Rjumper) / 108 pins	(equation 1)
AV38	AV4	Rreq = (Rtotal – Rjumper) / 88 pins	(equation 2)
B34	AN3	Rreq = (Rtotal – Rjumper) / 178 pins	(equation 3)

4.1.1. Determination of Maximum Electrical Resistance:

As in Section 4.1, measure the following pin-to-pin configurations on a good number of packages flush mounted to motherboard fixtures to get a statistical average for Rjumper. Measure the same configurations to get Rtotal with the package fixture mounted on the socket, which is mounted on a motherboard fixture. All of the following pin pairs will be measured, and the Rreq of equation 4 must be satisfied for every measured socket.

Pin Pairs.

B2-C3	B38-D38	AV2-AV4	AU35-AU37
C1-D2	A37-C37	AU3-AU5	AW19-AW21
B4-A5	E39-G39	AW39-AU39	U39-W39
B6-C7	AW1-AU1	AW35-AW37	B20-A21
A39-C39	AW3-AW5	AV34-AV36	W1-Y2

Rreq = (Rtotal – Rjumper) / 2 pins (equation 4)

4.1.2. Initial/Final Electrical Resistance:

The electrical resistance is for the socket plus the part of the engaged package pin inside the socket. The final electrical resistance refers to the resistance measured after all the environmental testing such as shock and vibration has been conducted. (See Section 5.)

There are two requirements:
(1) Final electrical resistance, Rreq from equations 1 - 3, shall not exceed 12mΩ.
(2) No single pin, Rreq from equation 4, shall exceed the electrical resistance of 17mΩ.

4.2. Inductance:

The bottom fixture for the inductance is a ground plane on the secondary side of the motherboard with all pins grounded. The component side of the socket PCB does not contain a plane. The top fixture shown is for the package test fixture, which contains pins that will connect to the socket. Figure 14 presents the inductance measurement fixture cross-section. The first figure shows the entire assembly. The second figure shows the assembly without the socket; the socket-seating plane of the package is directly mounted to the component side of the socket PCB. This is used to calibrate out the fixture contribution. The materials for the fixture must match the materials used in the package. Figure 16 presents the inductance measurement methodology. Note the probe pad features exist on the topside of the top fixture, and the shorting plane exists only on the bottom side of the bottom fixture.

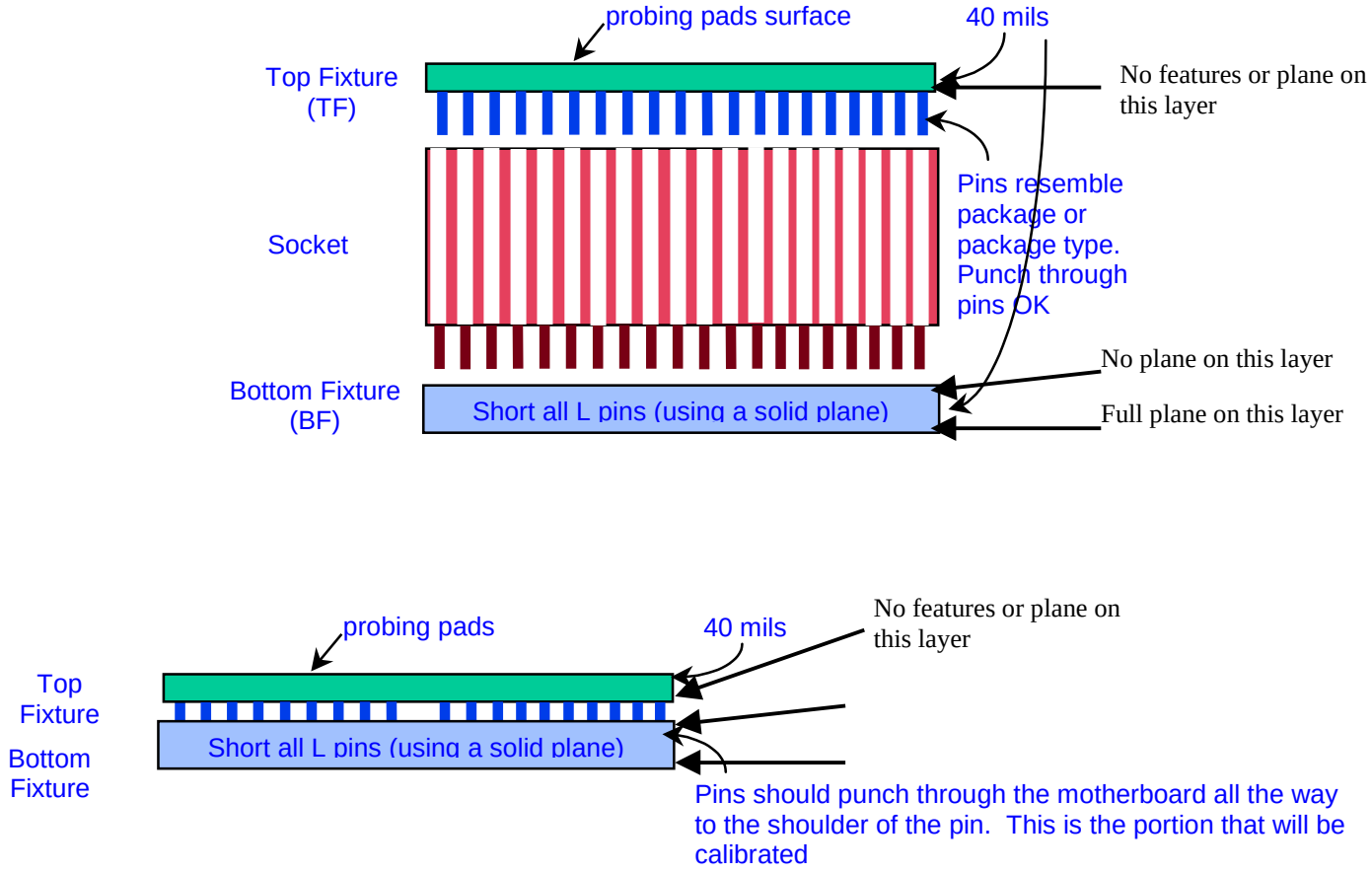


Figure 14: Inductance Measurement Fixture Cross-Section.

Solder must be formed full and consistent.

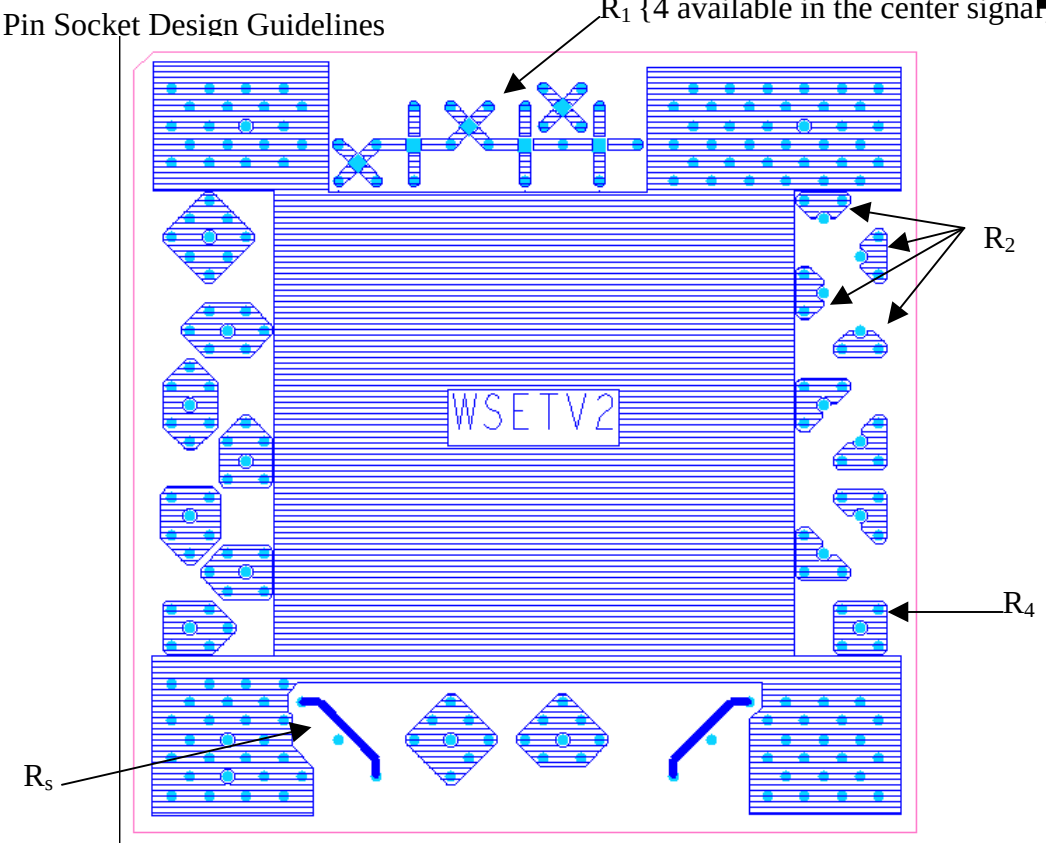


Figure 15: Inductance and Capacitance Fixture Design

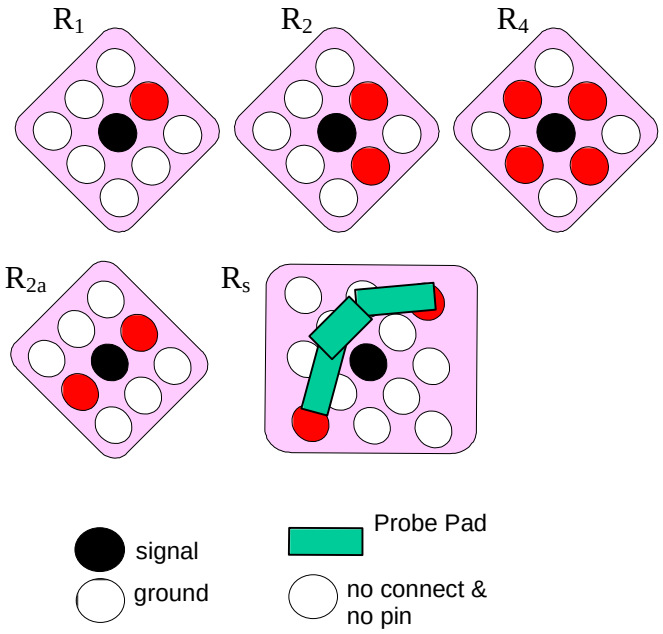


Figure 16: Inductance Measurement Configuration

4.2.1. Procedure for Inductance Measurements:

4.2.1.1. Mounted Directly to Motherboard Fixture:

Measure the inductance of the 4 different configurations of the package fixture flush-mounted to the motherboard fixture. The configurations can be seen in Figure 16. This will force spacing between the bottom of the package and top of the motherboard fixture to be 0.010in, which matches the height of the pin shoulder. The values that this measurement will produce will be labeled with a prime to note the fact that this is the fixture; R_1', R_2', R_{2a}', R_4', and R_s'.

The different configurations consider one signal and different numbers of return paths.

These inductance measurements will be used to characterize the fixture contribution for each case.

4.2.1.2. Mounted to Socket:

Measure the inductance of the 4 configurations of the package fixture mounted on the socket, which is mounted to the motherboard fixture. The values that this measurement will produce will be labeled according to configuration: R_1, R_2, R_{2a}, R_4, and R_s.

As in Section 4.2.1.1, the different configurations consider one signal as the ground and different numbers of return paths.

Matching the correct configuration in Section 4.2.1.1with the configurations of inductance measurements taken in this step, the inductance measurements of Section 4.2.1.1will be subtracted from the inductance measurements taken in this step.

4.2.1.3. Equations:

Using the following equations, the mutual inductance for the 71mil-pitch (M_{71}), the 142mil-pitch (M_{142}), and the 100mil-pitch (M_{100}); and the self-inductance of a pin (L_s) can be calculated. R_1', R_2', and R_4' come from the measured configurations in Section 4.2.1.2subtracted from the same measured configurations in Section 4.2.1.1, with the values R_1, R_2, and R_4.

Calculate using the following equations:

$$R_1 - R_1' = 2*(L_s - M_{71}) \qquad \text{(equation 5)}$$

$R_2 – R_2' = (3*L_s/2 – 2*M_{71}) + M_{100}/2$ (equation 6)

$R_4 – R_4' = 5*L_s/4 – 2* M_{71} + M_{100}/2 + M_{142}/4$ (equation 7)

$R_s – R_s' = 3*L_s/2 – 2* M_{142} + 0.5M_{280}$ (equation 8)

*note: M_{280} is the mutual at 280mils away. Since that value is small and we only use half of that value, we will neglect it for equation 8.

4.2.2. Loop Inductance:

To qualify, the socket must meet the loop inductance (L_{Loop}) as shown in equation 9.

$L_{Loop} = 2 * (L_S – M)$ (equation 9)

M refers to the closest adjacent mutual inductance term at the 71-mil pitch

The loop inductance from the calculation in equation 9, using this methodology, shall not exceed 4.3nH at 1GHz.

4.3. Pin-to-Pin Capacitance:

Pin-to-pin capacitance shall be measured using configuration R_1, with the motherboard not connected and only the measurements with the same test vehicle mounted on the socket will be taken. Capacitance for the two pins shall not exceed 1.0 pF at 400MHz.

4.4. Contact Current Rating:

Contact current rating shall be tested at 1.0A/pin. At this current rating, record the temperature rise. Testing shall be measured per EIA 364, Test Procedure 70A. The power supply is connected between B2 and AN3 and the input voltage needs to be adjusted to draw 1A through the daisy chain. The temperature is measured at Y4. This measurement technique is detailed in Figure 17.

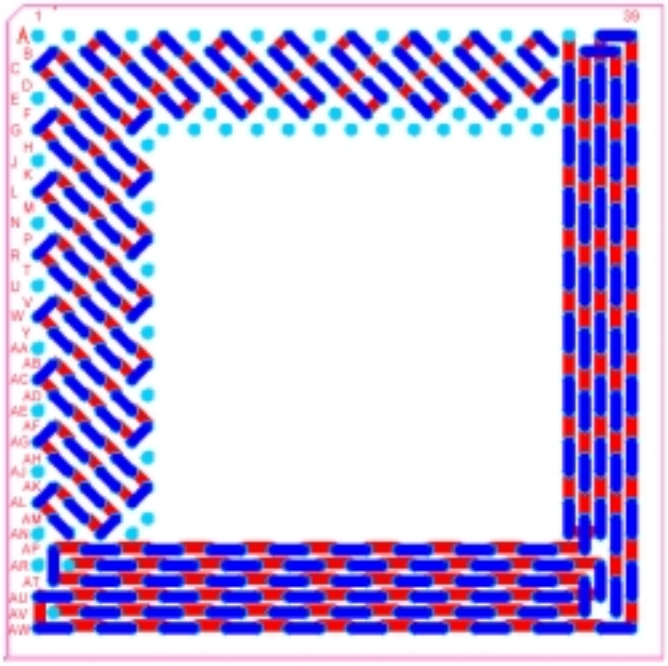


Figure 17: Contact Current Rating Measurement

4.5. Dielectric Withstand Voltage:

Dielectric withstand voltage shall be a minimum requirement of 400VRMS as measured per EIA 364, Test Procedure 20A, Method B. Dielectric withstand voltage will be measured at 8 test points between adjacent pins (D4 and E5, D36 and C37, AT4 and AR5, AT36 and AU37, D20 and C19, AT20 and AR19, Y4 and W5, Y36 and AA37).

4.6. Insulation Resistance:

Insulation resistance shall be a minimum requirement of 800MΩ as measured per EIA 364, Test Procedure 21. Insulation resistance will be measured at 8 test points between adjacent pins (D4 and E5, D36 and C37, AT4 and AR5, AT36 and AU37, D20 and C19, AT20 and AR19, Y4 and W5, Y36 and AA37).

5. ENVIRONMENTAL REQUIREMENTS

Design, including materials, shall be consistent with the manufacture of units that meet the following environmental reference points.

5.1. Temperature Range:

5.1.1. Operating:

0ºC to +85ºC

5.1.2. Shipping and Storage:

-40ºC to + 70ºC

5.1.3. Operating Humidity

55ºC/85% RH (non-condensing)

5.2. Durability:

Mate and unmate samples for 50 cycles at a rate of 500cph (max), using the same socket. One package is to be used for 1st and 51st cycles. Measure electrical resistance when mated in 1st and 51st cycles. A spare package shall be used for 2nd through 50th cycles. **A** pair of new packages are to be used for each of the socket samples.

5.3. Shock:

Tested at 50G, 11ms duration, Trapezoidal waveform. Three shocks applied in each of three perpendicular axes (18 total). The socket must be mated with the mechanical sample outlined in Section 6.8.4 and retained with mechanical supports outlined in Section 3.2. The total minimum velocity change shall be 170in/s. Figure 18 provides the schematic for this requirement.

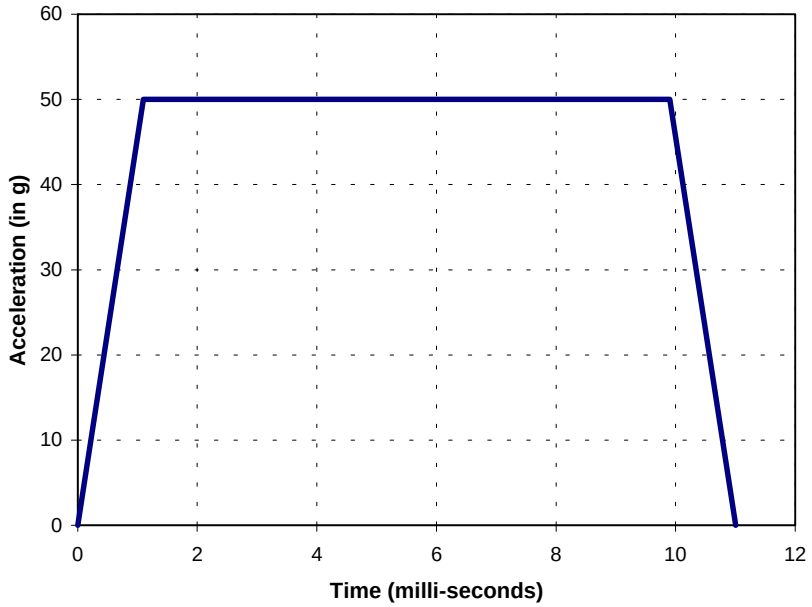


Figure 18: Shock Pulse Curve

5.4. Vibration, Random:

Frequency Range: 5Hz to 500Hz

Vibration test to be performed for two durations:

Duration 1: 10min/axis (derived from Intel® Corporation customary board vibration specifications).
Power Spectral Density (PSD) Profile: 3.13GRMS.

Figure 19 presents the PSD curves used for the vibration testing.
Sample Size: 9 for contact resistance, 9 for electrical discontinuity.

Input Accelerometer Location: Input (Control) accelerometer to be mounted on the vibration table.
Socket to be mounted to Micro-ATX motherboard. The mechanical vibration and shock fixture for the Micro-ATX motherboard is shown in Figure 20. The layout details of the Micro-ATX motherboard are shown in Figure 21. The board thickness is 0.062in + 0.008in – 0.005in.

The 423 Pin Socket must meet all the electrical contact resistance requirements following random vibration test. The socket must be mated with the mechanical sample outlined in Section 6.8.4 and retained with mechanical supports outlined in Section 3.1.

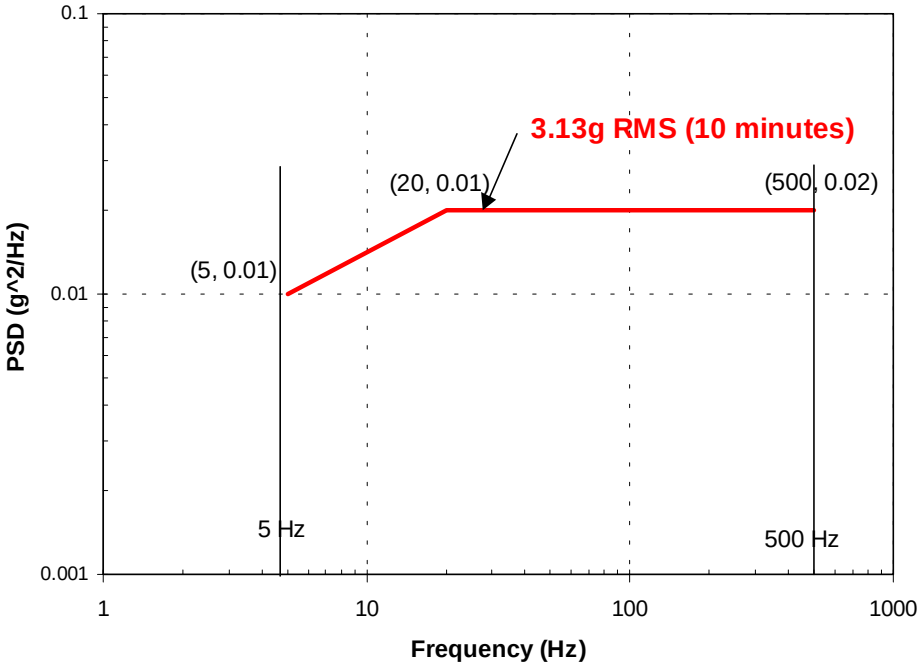


Figure 19: Power Spectral Density Curve

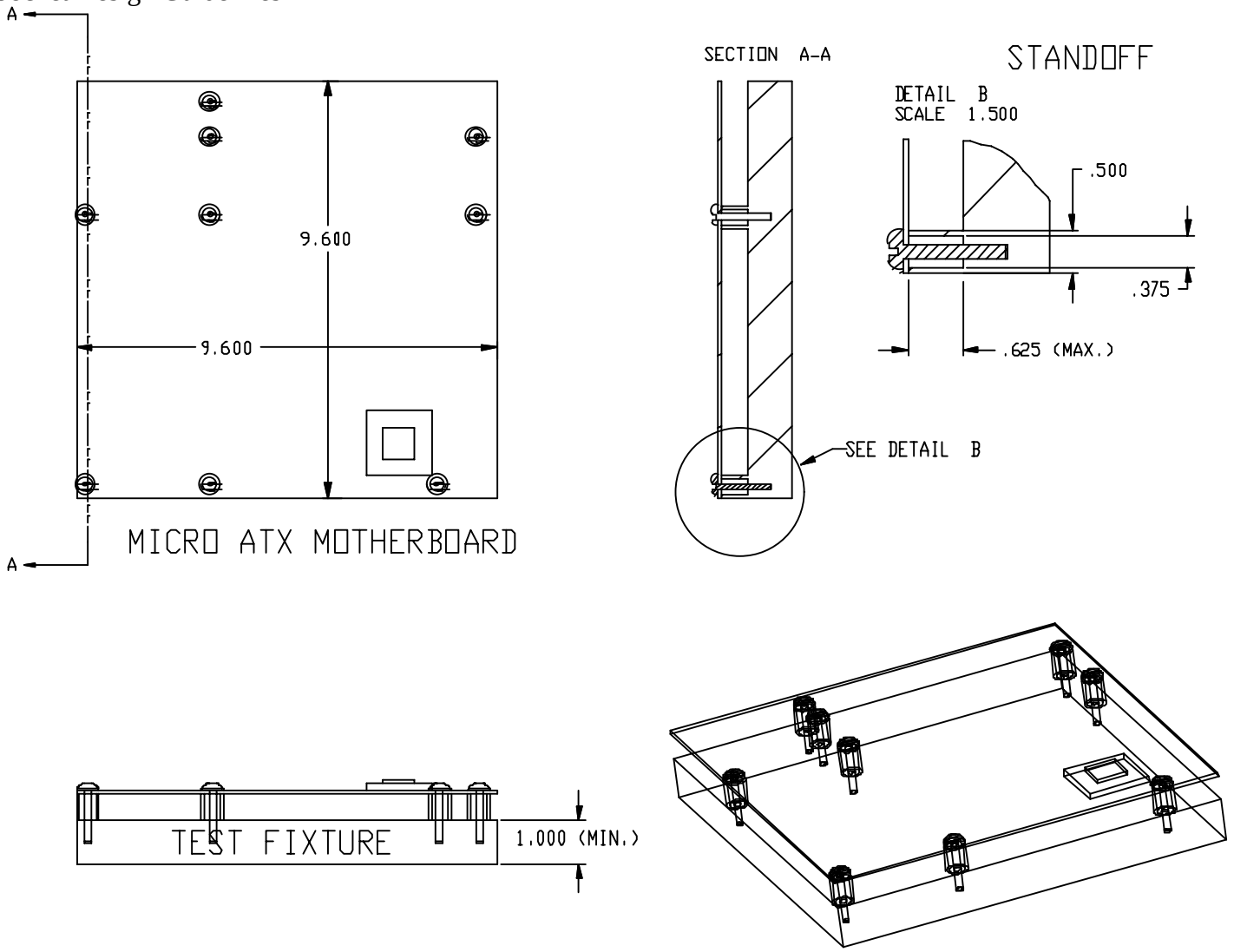


Figure 20: Mechanical Shock and Vibration Fixture

Note: Dimensions shown in inches

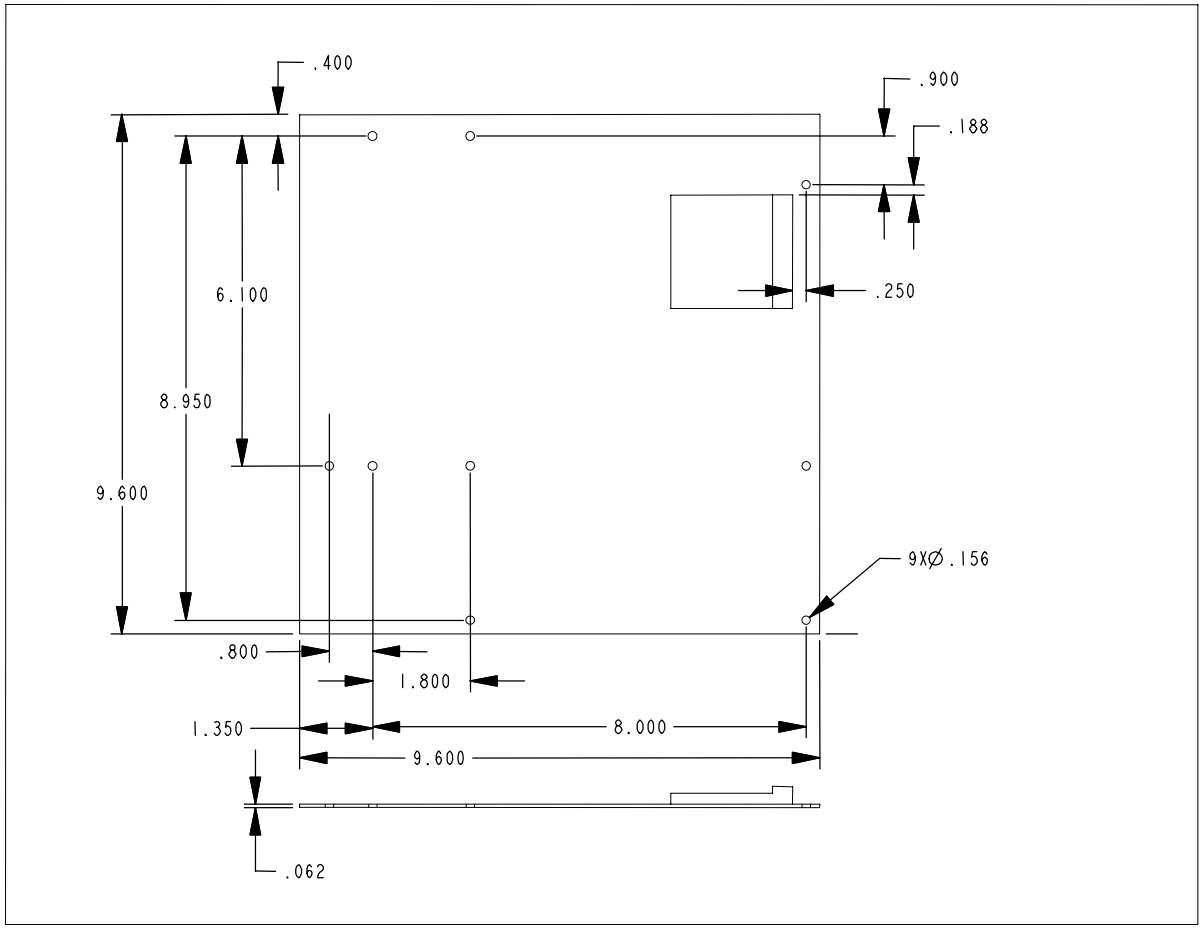


Figure 21: ATX Motherboard Layout Details

Note: Dimensions shown in inches

5.5. Temperature Shock:

Test per EIA 364 TP 32B, Test Condition (I) for 5 cycles.

5.6. Cyclic Humidity:

Test per EIA 364 Test Procedure 31 and Test Condition B for 240 hours.

5.7. Temperature Life (Bake Test):

Test per EIA 364 Test Procedure 17 at 85 °C for 500 hours. Precondition samples with three insertion/extractions (min).

5.8. Solder Withstand Temperature:

Test per EIA 364, Test Procedure 56A, Procedure 5.

5.9. Porosity Test:

5.9.1. Porosity Test Method:

EIA 364, Test Procedure 60, paragraph 7 or 8.

5.9.2. Porosity Test Criteria:

Maximum of two pores per set of 20 contacts, as measured per EIA 364, Test Procedure 60.

5.10. Plating Thickness:

Record thickness of plating on contact surface per EIA 364, Test Procedure 48, Method A or C. Test to be performed using 20 randomly selected contacts per socket. No plating thickness measured shall be less than the minimum plating thickness specified in Sections 3.3.4.3 and 3.3.4.4.

5.11. Solvent Resistance:

Requirement: No damage to ink markings if applicable and socket body.
EIA 364, Test Procedure 11A.

5.12. Solderability:

Requirement: 95% coverage per tail.
EIA 364, Test Procedure 52, Class 2, Category 3. Test to be performed on 20 randomly selected contacts per socket.

5.13. Post Reliability Testing Inspection of Package pin field:

In case of electrical failures post shock and vibration testing: remove the package from the socket. Inspect for visual evidence of fretting corrosion on the pins. When a pass/fail decision cannot be made based on the visual inspection of the package pin field, the part may be sent out for SEM analysis.

Requirement: No visual evidence of fretting corrosion on any package pins.

6. QUALIFICATION TESTING REQUIREMENTS

This section of the document outlines the tests that must be successfully completed in order for the supplier's socket to pass the design guidelines validation. It provides the test plan and procedure required for validation.

6.1. Applicable Documents:

Intel® Pentium® 4 Processor In the 423-Pin Package Datasheet

6.2. Testing Facility:

Testing will be performed by Intel's designated test facility.

6.3. Funding:

Socket supplier will fund socket qualification testing for its socket. Any additional testing that is required due to design modifications will also be at the expense of the supplier.

6.4. Socket Design Verification:

At the earliest possible date, a detailed drawing of the socket supplier's 423 Pin Socket must be provided to Intel for review. This drawing should include all of the features called out in this specification (marking, pinout, cam location, date code location and explanation, etc.) as well as dimensional and board layout information. This drawing will be used to confirm compliance to this specification.

6.5. Reporting:

Test reports of the socket qualification testing will be provided directly from the independent test facility to Intel. Intel will also be given access to contact the test facility directly to obtain socket qualification status, explanation of test results and recommendations based on the test results.

6.6. Process Changes:

Any significant change to the socket will require submission of a detailed explanation of the change at least 60 days prior to the planned implementation. Intel® will review the modification and establish the necessary re-qualification procedure that the socket must pass. Any testing that is required MUST be completed before the change is implemented.

Typical examples of significant changes include, but are not limited to, the following: Plastic material changes including base material or color; contact changes including base material, plating material or thickness; and design modifications.

6.7. Quality Assurance Requirements:

The OEM's will work with the socket supplier(s) they choose to ensure socket quality.

6.8. Socket Test Plan:

6.8.1. Submission of a 423 Pin Socket for Socket Qualification Testing:

The socket supplier's 423 Pin Socket will be sent to Intel's designated third party test house for socket qualification testing. The sockets submitted must be per the drawing required in Section 6.4 and must be reviewed and approved (for submittal) by Intel before the start of testing. Refer to Sections 6.10 and 6.11.1 for production lot definition and number of samples required for qualification testing.

6.8.2. Test Flow:

The test flow is outlined in Section 6.10. Sample sizes and test requirements are given for each test group. For specific test procedures, please refer to the applicable test specifications referenced in Section 6.1.

6.8.3. Retest Restrictions:

Failures of particular sections of the test plan for a given socket footprint will require re-testing of at least a portion of the test flow defined in Section 6.10. The definition of the tests required will be at Intel's discretion. The modifications that will be made to the socket to improve a failing condition must be provided to Intel in writing and must be approved by Intel prior to retest. If failures occur after retest, further testing will be at Intel's discretion.

6.8.4. Mechanical Samples:

A mechanical sample of the 423 Pin Socket, package substrate, and heat sink (or suitable mockups that approximate size and mass of the planned heat sink) will be used during the mated socket qualification testing. The recommended maximum mass for the Intel® Pentium® 4 processor package heat sink is 300g for socket attach, and 450g for board retention mechanism. It is the suppliers responsibility

to procure electrical test vehicles and required mechanical components from Intel®.

6.9. Socket Qualification Notification:

Upon completion of the test plan, the test facility will prepare a summary report for the socket supplier that will provide notification as to whether the socket has passed or failed. A copy of the test report will be provided to Intel and the socket supplier.

6.10. Production Lot Definition:

A production lot is defined as a separate process run through the major operations including molding, contact stamping, contact plating, and assembly. These lots should be produced on separate shifts or days of the week. Lot identification marking needs to be provided to Intel as verification of this process.

6.11. Socket Qualification:

The 423 Pin Socket must pass socket qualification testing to be considered for inclusion on the Intel List of Qualified Sockets. The details of the tests are outlined in the Socket Qualification Requirements in Sections 4 and 5.

6.11.1. Sample size per group:

(Shown at top of each test group in Table 3)

The socket supplier shall provide Intel with total number of sockets specified in Table 3. Each sample shall be prepared in accordance to the documents specified in Section 6.1.

6.11.2. Test Sequence:

Each group of samples is tested per the numbered sequence outlined in Table 3**.** The following is an example of how the test sequence works: In Test Group 7, the first test is (1), visual inspection, followed by test (2), solvent resistance. Samples are tested in this test group, as outlined in Section 6.11.

Table 3: Test Group and Test Flow Diagram

Group 1 (for socket attach)	Group 2 (for board RM attach)	Group 3	Group 4	Group 5	Group 6	Group 7	Group 8	Group 9
9	9	4	4	2	1	4	4	1
LLCR	LLCR	Precondition	Visual Inspection	DWV	SWT	Visual Inspection	Mated Loop inductance	Current Rating
Mech. Shock	Mech. Shock	LLCR	CTF Dimensional Verification	IR	Solvent Resistance	Porosity		
Vibration	Vibration	Bake Test	LLCR	Thermal Shock	Visual Inspection	Visual Inspection	Pin to Pin Capacitance	
LLCR	LLCR	LLCR	Thermal Shock	Cyclic Humidity		Plating Thickness		
Visual Inspection	Visual Inspection		Durability	DWV		Solderability		
			LLCR	IR		Visual Inspection		
			Cyclic Humidity					
			LLCR					

LLCR: Low level Contact Resistance
DWV: Dielectric Withstanding Voltage
IR: Insulation Resistance
SWT: Solder Withstand Temperature

7. SAFETY REQUIREMENTS

Design, including materials, shall be consistent with the manufacture of units that meet the following safety standards:

UL 1950 most current editions

CSA 950 most current edition

EN60 950 most current edition and amendments

IEC60 950 most current edition and amendments

8. DOCUMENTATION REQUIREMENTS

The socket supplier shall provide Intel® with the following documentation:

Multi-Line Coupled SPICE models for socket.

Product specification incorporating the requirements of these specifications.

Recommended board layout guidelines for the socket consistent with low cost, high volume printed circuit board technology.

The test facility shall provide Intel and the supplier with the following document:

Qualification Testing and Test Report supporting successful compliance with these specifications.