VRM 8.5 DC–DC Converter Design Guidelines

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Contents

Applications and terminology

This document defines a range of DC-to-DC converters to meet the power requirements of computer systems using Intel® microprocessors. It does not attempt to define a specific on-board voltage regulator (VRD) or voltage regulator module (VRM) implementation. VRM requirements will vary according to the needs of different computer systems, including the range of processors a specific VRM is expected to support in a system. The "VRM" designation may refer a voltage regulator on a system board, as well as to the module defined in Section 3.

The VRM 8.5 definition is specifically intended to meet the needs of Intel® Pentium® III processor-based systems**.**

Each guideline is placed into one of three categories. The category immediately follows the section heading and is one of the following:

REQUIRED: An essential part of the design—necessary to meet processor voltage and current specifications.

EXPECTED: Part of Intel's processor power definitions; necessary for consistency with the designs of many systems and power devices.

PROPOSED: Normally met by of this type of DC-to-DC converter and, therefore, included as a design target. May be specified or expanded by system manufacturers.

1 Scope

A VRM 8.5 DC-DC converter supplies the required voltage and current to a single processor as shown in the following tables. The reference voltage is determined by the five-bit VID code provided to the VRM, as described in Section 2.3.4. The term "reference voltage" indicates that the VID provides a reference point for the static and transient voltage tolerance values provided in Section 2.1.1. Due to voltage regulator tolerances and current draw variations, the average voltage seen at the processor may be slightly higher or lower than the reference value. However, VRM designers must meet the entire range of processor loads and processor static and transient tolerance limits.

It should be noted that these guidelines refer to three different processor configurations and that the output requirements of the VRM may differ for each:

1. A single- or uni-Processor (UP) based configuration supporting a Celeron® or Pentium® III processor
2. A two- or dual-Processor (DP) capable configuration supporting Pentium III processors
3. A two- or dual-Processor (DP) capable configuration supporting Low Voltage Pentium III processors with 512K cache

Further, the design guidelines in this document accommodate DC-DC converters which can be either a complete voltage regulator circuit on the motherboard (VRD) or a plug-in module (VRM) with a defined form factor and pin-out, defined in Section 3.

The VRM requires a certain amount of external capacitance to maintain the proper voltage at the processor socket pins (for configurations 1 and 2 above) or package balls (for configuration 3). For either implementation, Vcc_{CORE} must meet the specifications of the processor at the socket pins or package balls.

For dual-processor applications, a separate processor power plane, with one VRM or VRD for each processor, is recommended. Due to the requirements of transient and static tolerances vs. Icc load characteristics detailed in Figure 2 and Figure 3, a single (large) VRD that provides voltage and current to two processors sharing a common power plane is not recommended.

Table 1 – Processor support by VRM type

VRM Type	Processors Supported
VRM 8.5–5	Pentium® III processor (CPUID 068xh) Celeron® and Pentium III processor on 0.13 micron process **Supported on a UP-configured system board** (5mΩ)
VRM 8.5–4	Low Voltage Pentium III processor with 512K cache **Supported on a DP-configured system board** (4mΩ)
VRM 8.5–3	Pentium III processor (CPUID 068xh) and Pentium III processor with 512KB L2 cache **Supported on a DP-configured system board** (3.214mΩ)

2 Electrical Specifications

The following conditions apply to the specifications:

- Specifications apply to all frequencies unless specific frequencies are listed.
- Icc_{CORE} is measured at the Typical Reference Vcc_{CORE} value under maximum signal loading conditions such as running a power virus program.
- The Typical Reference voltage, voltage tolerance, and maximum current values in Section 2.1.1 are for reference only. Please refer to the appropriate processor datasheet for the latest specifications.

2.1 Output Requirements

2.1.1 Voltage and Current **REQUIRED**

2.1.1.1 Pentium® III processor

The following details the VRM output voltage and current requirements to support a single Pentium® III processor (CPUID 068xh) operating in either a single or dual processor platform.

Table 2 – Pentium® III processor (CPUID 068xh) Voltage and Current Specifications at Processor Socket Pins see note 1

Symbol	Parameter	Core Frequency	Min	Typical Reference see note 3	Max	Unit
Vcc_{CORE}	VID	All		1.75		V
	Vcc_{CORE} Static Tolerance	All	-0.080		0.040	V
	Vcc_{CORE} Transient Tolerance	< 933 MHz see note 3	-0.130		0.080	V
		≥ 933 MHz see note 3	-0.110		0.080	
Icc_{CORE}	Current for Vcc_{CORE}	FMB see note 4			22.6	A
$Icc_{SGNT}CORE$	Icc for Stop-Grant Vcc_{CORE}				6.9	A
$Icc_{DSLP}CORE$	Icc for Deep-SleepVcc_{CORE}				6.6	A
$DIcc_{CORE}/dt$	Icc slew rate				Refer to Section 5.1	A/µs

Notes:

1. Specifications apply to the processor socket pins on the solder-side of the motherboard
2. CPUID 0686h and CPUID 068Ah processors at 1.0 GHz and below can operate in platforms designed for the Intel® Pentium® III processor with 512KB L2 Cache specifications (i.e. in boards designed to the 3.2mΩ load line). These processors have allowable tolerance on the Vcc Static Maximum voltage specification, and as a result, can operate with the additional 25mV in Vcc static voltage.
3. Please refer to the appropriate component documentation for the most current specifications.
4. FMB is the flexible motherboard guideline provided as an estimation of the worst-case values the appropriate processors may have over their product lifetimes.

2.1.1.2 Celeron® and Pentium® III Processors on 0.13 Micron Process

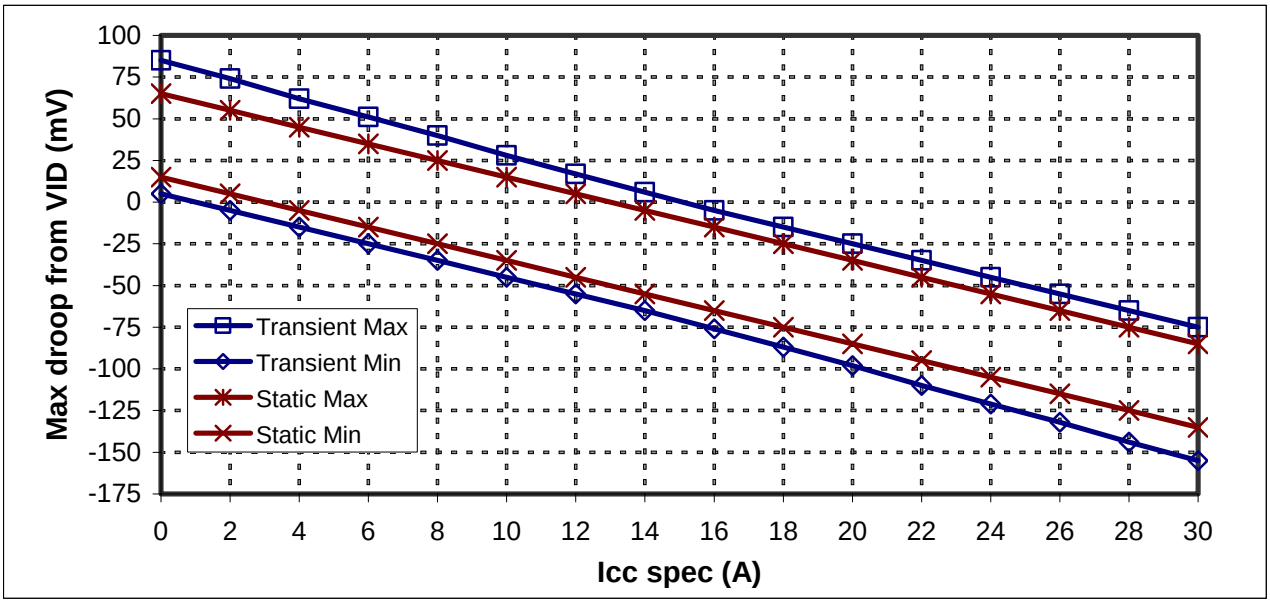
The following details the VRM output voltage and current requirements to support a single Celeron or Pentium III processor on 0.13 micron process operating in a single-processor platform.

Table 3 – Celeron® and Pentium® III Processor on 0.13 Micron Process Voltage and Current Specifications at Processor Socket Pins see note 1

Symbol	Parameter	Core Frequency	Min	Typical Reference	Max	Unit
Vcc_{CORE}	VID	FMB1 see note 2		1.475		V
		FMB1-E see note 2		1.500		
	Vcc_{CORE} Static Tolerance	All Frequencies including FMB1-E	Refer to Figure 1 or Table 4			V
	Vcc_{CORE} Transient Tolerance	All Frequencies including FMB1-E	Refer to Figure 1 or Table 4			V
Icc_{CORE}	Current for Vcc_{CORE}	FMB1 see note 2			22.6	A
		FMB1-E see note 2			25.5	
$Icc_{SGNT}CORE$	Icc for Stop-Grant VccCORE				14.0	A
$Icc_{DSLP}CORE$	Icc for Deep-Sleep VccCORE				11.0	A
$dIcc_{CORE}/dt$	Icc slew rate				Refer to Section 5.2	A/µs

1. Specifications apply to the processor socket pins on the solder-side of the motherboard
2. FMB is the flexible motherboard guideline provided as an estimation of the worst-case values the appropriate processors may have over their product lifetime.

Figure 1 – Celeron® and Pentium® III Processors on 0.13 Micron Process Static and Transient Load Lines at Processor Socket Pins



NOTE: The VR must meet the specifications defined in Table 3 for every load and load change condition corresponding to the following equation:

Static minimum regulation requirements: VID set point +15mV – (5mΩ x Icc A)
Static maximum regulation requirements: VID set point +65mV – (5mΩ x Icc A)
Transient minimum regulation requirements: VID set point +5mV – (5mΩ x Icc A)
Transient maximum regulation requirements: VID set point +85mV – (5mΩ x Icc A)

Table 4 – Celeron® and Pentium® III Processors on 0.13 Micron Process Static and Transient Load Lines at Processor Socket Pins

	Voltage Specifications from VID (mV)			
	Static Tolerance		Transient Tolerance	
Icc (A)	Minimum	Maximum	Minimum	Maximum
0	15	65	5	85
2	5	55	-5	74
4	-5	45	-15	62
6	-15	35	-25	51
8	-25	25	-35	40
10	-35	15	-45	28
12	-45	5	-55	17
14	-55	-5	-65	6
16	-65	-15	-76	-5
18	-75	-25	-87	-15
20	-85	-35	-98	-25
22	-95	-45	-110	-35
24	-105	-55	-121	-45
26	-115	-65	-132	-55
28	-125	-75	-144	-65
30	-135	-85	-155	-75

NOTE: The VRM must meet the Static and Transient Specifications for each Icc level. This includes any load change events as described in Section 2.1.3.
Example: Operating at 6A requires that the VRM meet the 6A Static and Transient specifications. If a load change occurs up to 18A, the VRM must meet the Static and Transient specifications for 18A including the response to the load change event.

2.1.1.3 Pentium® III Processor with 512KB L2 Cache

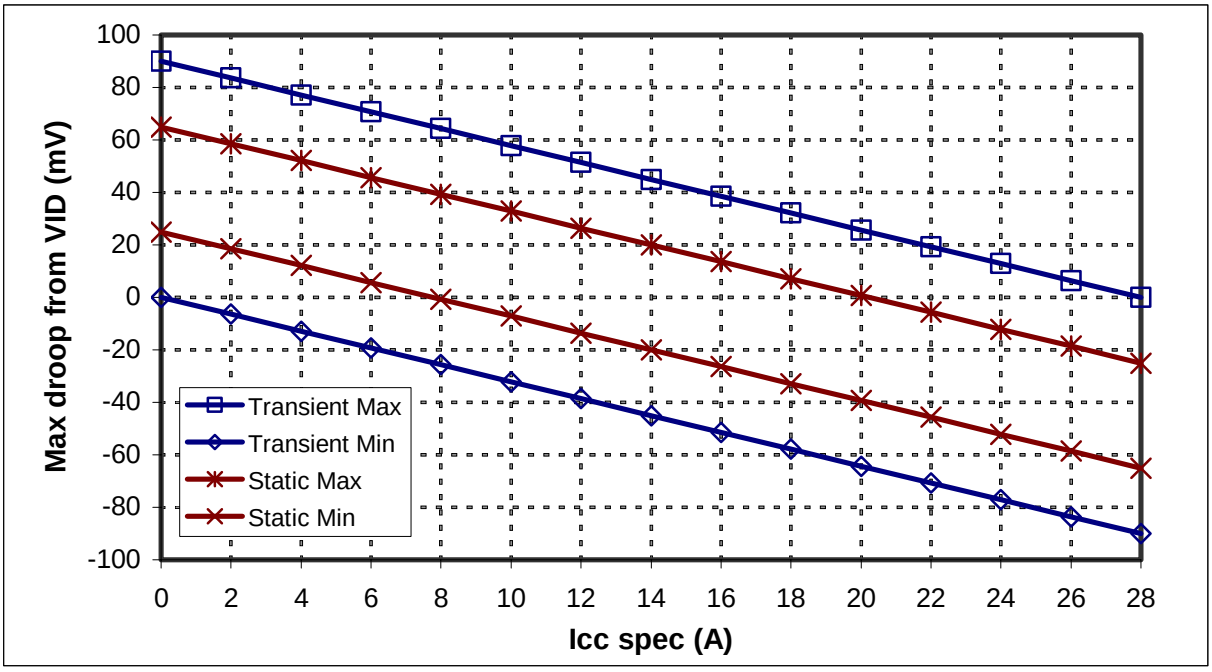
The following details the VRM output voltage and current requirements to support a single Intel Pentium III Processor with 512KB L2 Cache operating in a dual processor capable platform only.

Table 5 – Pentium® III Processor with 512KB L2 Cache Voltage and Current Specifications at Processor Socket Pins see note 1

Symbol	Parameter	Min	Typical Reference	Max	Unit
Vcc_{CORE}	VID		1.475 1.45		V
	Vcc_{CORE} Static Tolerance	Refer to Figure 2 or Table 6			V
	Vcc_{CORE} Transient Tolerance	Refer to Figure 2 or Table 6			V
Icc_{CORE}	Maximum Vcc_{CORE} current see note 2			28.0	A
$Icc_{SGNT}CORE$	Icc for Stop-Grant VccCORE			14.0	A
$Icc_{DSLP}CORE$	Icc for Deep-Sleep VccCORE			8.8	A
$dIcc_{CORE}/dt$	Icc slew rate			Refer to Section 5.2	A/µs

1. Specifications apply to the processor socket pin on the solder-side of the motherboard
2. An estimate of the worst-case current the processor can expect over the platform lifetime. Please refer to the product datasheet for actual processor requirements.

Figure 2 –Pentium® III Processor with 512KB L2 Cache Static and Transient Load Lines at Processor Socket Pins



NOTE: The VR must meet the specifications defined in Table 5 for every load and load change condition corresponding to the following equation:

Static minimum regulation requirements: VID set point +25mV - (3.214mΩ x Icc A)
Static maximum regulation requirements: VID set point +65mV - (3.214mΩ x Icc A)
Transient minimum regulation requirements: VID set point - (3.214mΩ x Icc A)
Transient maximum regulation requirements: VID set point +90mV – (3.214mΩ x Icc A)

Table 6 – Pentium® III Processor with 512KB L2 Cache
Static and Transient Load Lines at Processor Socket Pins

	Voltage Specifications from VID (mV)			
	Static Tolerance		Transient Tolerance	
Icc (A)	Minimum	Maximum	Minimum	Maximum
0	25	65	0	90
2	19	59	-6	84
4	12	52	-13	77
6	6	46	-19	71
8	-1	39	-26	64
10	-7	33	-32	58
12	-14	26	-39	51
14	-20	20	-45	45
16	-26	14	-51	39
18	-33	7	-58	32
20	-39	1	-64	26
22	-46	-6	-71	19
24	-52	-12	-77	13
26	-59	-19	-84	6
28	-65	-25	-90	0

NOTE: The VRM must meet the Static and Transient Specifications for each Icc level. This includes any load change events as described in Section 2.1.3.
Example: Operating at 6A requires that the VRM meet the 6A Static and Transient specifications. If a load change occurs up to 18A, the VRM must meet the Static and Transient specifications for 18A including the response to the load change event.

2.1.1.4 Low Voltage Pentium® III Processor with 512K Cache

The following tables and figures detail the VRM output voltage and current requirements to support a single Low Voltage Pentium III processor with 512K cache.

Table 7 – Low Voltage Pentium® III Processor with 512K Cache Voltage and Current Specifications at Processor Package Balls

Symbol	Parameter	Min	Typical Reference	Max	Unit
Vcc_{CORE}	VID		1.05 1.10 1.15		V
	Vcc_{CORE} Static Tolerance	Refer to Figure 3 and Table 8			V
	Vcc_{CORE} Transient Tolerance	Refer to Figure 3 and Table 8			V
Icc	Vcc_{CORE} current [See Note 1] @1.15V			12.32	A
$dIcc_{CORE}/dt$	Icc slew rate			Refer to Section 5.2	A/µs

1. An estimate of the worst-case current the processor can expect over the platform lifetime. Please refer to the product datasheet for actual processor requirements.

Figure 3 – Low Voltage Pentium® III Processor with 512K Cache Static and Transient Load Lines at Processor Package Balls

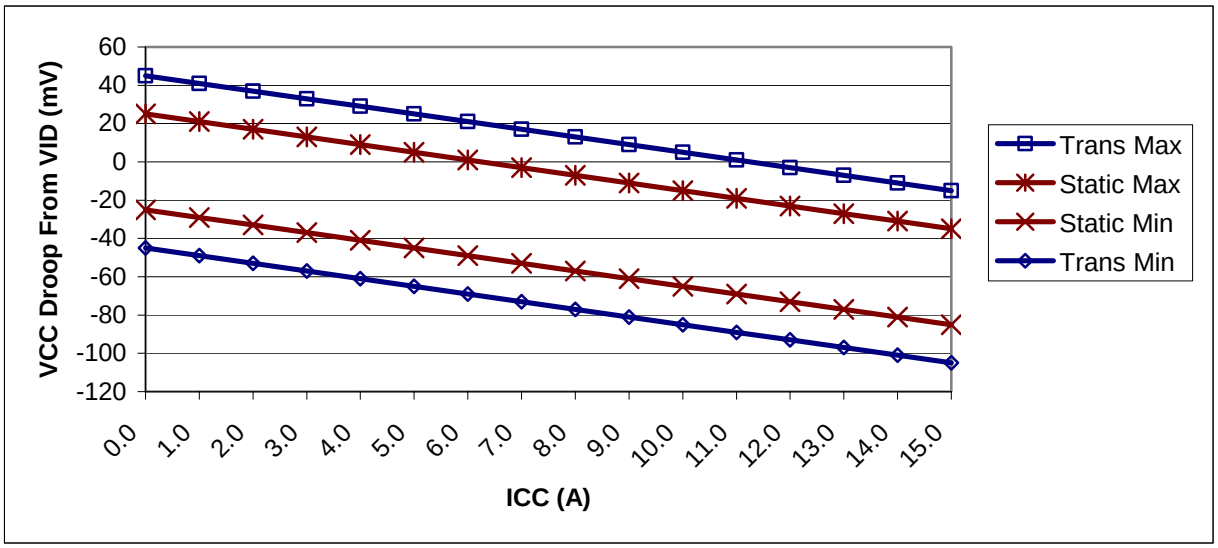


Table 8 – Low Voltage Pentium® III Processor with 512K Cache Static and Transient Load Lines at Processor Package Balls

I_{CC} (A)	V_{CC} (mV)			
	Static Min	Static Max	Transient Min	Transient Max
0.0	-25	25	-45	45
1.0	-29	21	-49	41
2.0	-33	17	-53	37
3.0	-37	13	-57	33
4.0	-41	9	-61	29
5.0	-45	5	-65	25
6.0	-49	1	-69	21
7.0	-53	-3	-73	17
8.0	-57	-7	-77	13
9.0	-61	-11	-81	9
10.0	-65	-15	-85	5
11.0	-69	-19	-89	1
12.0	-73	-23	-93	-3
13.0	-77	-27	-97	-7
14.0	-81	-31	-101	-11
15.0	-85	-35	-105	-15

2.1.2 Static Voltage Regulation **REQUIRED**

The output voltage measured with an instrument bandwidth limit of 20MHz on the motherboard must be within the static ranges shown in Figure 1/Table 4, Figure 2/Table 6 and Figure 3/Table 8. Exceptions to the Static Voltage specifications are limited to input voltage turn-on and turn-off and for current transitions as shown under “Transient Voltage Regulation” below. The static limits apply to ambient temperatures between 0°C and 60°C. Static voltage regulation includes:

- Output ripple and noise
- Voltage regulator tolerance
- Operation at any fixed load condition
- Temperature and warm up specified in Section 4.2.

Due to the combination of factors in Static regulation, VRM designs should nominally meet the Static Nominal Load Line where the Output ripple and noise is centered on the Static Nominal condition. This allows a 0.8% tolerant regulator to meet the Static Maximum and Minimum specifications even when delivering voltage at the ± 0.8% extremes.

2.1.3 Transient Voltage Regulation **REQUIRED**

The peak output voltage measured with an instrument bandwidth limit of 20MHz on the motherboard must be within the transient ranges shown in Figure 1/Table 4, Figure 2/Table 6 and Figure 3/Table 8. These Transient Voltage specifications include the condition where the current draw changes at the rate indicated in the appropriate table in Section 5, either in the low to high or the high to low direction. This includes the transition from $Icc_{SGNTCORE}$ (Stop-Grant state) to Icc_{CORE} (Maximum) or Icc_{CORE} (Maximum) to $Icc_{SGNTCORE}$ (Stop-Grant state), except as noted for input voltage turn-on and turn-off. This tolerance includes the variations described under the static voltage regulation Section 2.1.2 plus the effects of the output load transient.

Peak output voltage during a single transient event may not exceed the static voltage specification for longer than 100 μsec and must remain within the transient voltage specification at all times. The toggle rate for the output load transition must range from 100 Hz to 500kHz. Under the above conditions and for all toggle rates, the transient response must be measured at ambient temperatures between 25°C and 50°C.

2.1.4 Testing of Transient & Static Voltage Regulation EXPECTED

Due to the current draw changes that occur during typical processor operation with varying duration, Intel recommends testing VRM performance to Transient and Static Voltage specifications through the use of a Voltage Transient Tool (VTT). The tool provides a convenient and repeatable method of validating VRM performance for a given current load. This approach also aids in testing for worst-case load changes that affect processor performance, which may not be generated by other test methods such as Stop-Grant with a high power application.

2.1.5 Icc Slew Rate REQUIRED

Icc Slew Rate graphs and accompanying Piece Wise Linear (PWL) data is provided in Section 5. The data for processors is the minimum rate of change of current that the motherboard must be able to supply to the processor. The data for Voltage Regulator Modules is the minimum rate of change of current that a VRM must be able to supply to the motherboard. Meeting these requirements can be demonstrated by a measurement showing that the output current of the VRM fully changes from the minimum to maximum and from the maximum to minimum processor current ratings within the time period indicated by the leading edge of the appropriate graph.

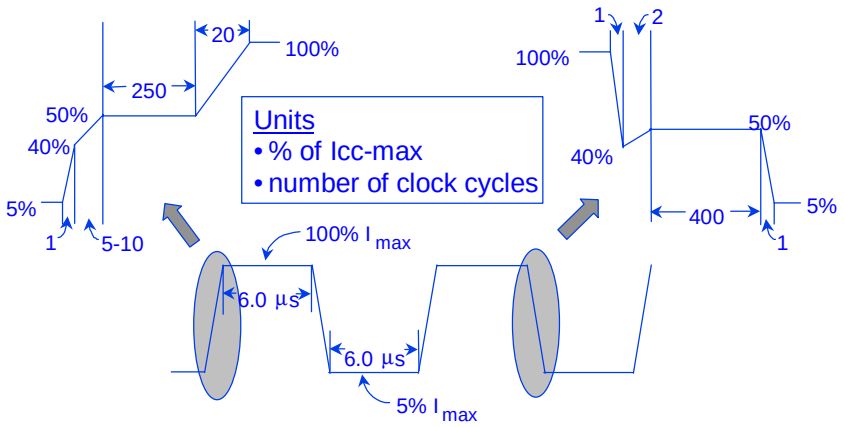
Adequate performance of a VRM (or on-board VRD) can be determined by testing the power delivery circuitry under max load change conditions as defined by the processor specifications detailed in the tables in Section 2.1.1. Failure to provide adequate Slew Rates will result in excessive Transient Voltage spikes during the period described by the Icc Slew Rate graphs.

2.1.6 Converter Stability REQUIRED

The VRM DC-DC converter needs to be unconditionally stable under all output voltage ranges and current transients with system board capacitance ranging from 1800μF to 20,000 μF and with less than 2.0 mΩ ESR. A voltage regulator embedded on a system board needs to meet stability requirements with the output filter capacitance design on that board.

Stability requirements include a thermal-management operating condition in which the processor may periodically stop to reduce its average power dissipation in response to a high-temperature alert. Figure 4 shows worst-case thermal-management operation (maximum current in the ON state).

Figure 4 – Processor Current during Thermal Management



Note: Duration of on-off periods depends on processor speed, but will be a minimum of 6.0us – faster processors have shorter duration.

2.1.7 Output Ripple and Noise **REQUIRED**

Ripple and noise are defined as periodic or random signals within a 20 MHz frequency band at the output pins under constant load. Output ripple must be accounted for in the static voltage requirements.

2.1.8 VRM Tolerance **EXPECTED**

Due to the tight static voltage tolerance bands, Intel recommends a maximum voltage regulator tolerance of 0.8%. The VRM should be designed to the Static Nominal condition such that any variation due to VRM tolerance still meets the Static and Transient voltage tolerances.

2.1.9 Turn-on Response Time **PROPOSED**

The output voltage should be within its specified range within 10ms of the input reaching 95% of its nominal voltage. The maximum load current that the VRM shall be presented with at turn-on shall be 50% of the maximum I_{CC}CORE value.

2.1.10 Overshoot at Turn-On or Turn-Off **REQUIRED**

Overshoot upon the application or removal of the input voltage under the conditions specified in Section 2.2 must be less than 10% above the static no-load output voltage. No negative voltage may be present on any output during turn-on or turn-off.

2.2 Input Voltage and Current

2.2.1 Input Supply Voltages **EXPECTED**

Available inputs for an on-board VRD are 12V ±5%, 5V ±5% and 3.3V ±5% and for a VRM module are 12V ±5% and 5V ±5% (see VRM connector pin-out in Section 3.1). The VRM may use any single voltage or combination. These voltages are supplied by a conventional computer power supply through a cable to the motherboard. Input voltage requirements should be clearly marked on modules.

2.2.2 V_{TT} REQUIRED

V_{TT} is the processor AGTL termination voltage plane at 1.25V. The processor also uses V_{TT} to generate the VID codes to the VRM. The system board must supply a V_{TT} sense and a V_{TT_PWRGD} signal to a VRM module so that the regulator may sense the V_{TT} plane during system power-up to determine if V_{TT} has reached a minimum threshold level of 1.13V (V_{TT} -9%). A minimum of 1ms after V_{TT} crosses the 1.13V threshold, V_{TT_PWRGD} must be asserted by the VRM. Refer to Section 2.3.2 for V_{TT_PWRGD} functionality and onboard VRM implementations.

For 1U form factor VRMs (Figure 9), it is recommended that the VTT regulator circuit be located on the system board due to space limitations of that form factor.

2.2.3 Load Transient Effects on Input Voltages PROPOSED

The VRM should be able to provide for an output current step at the load from Icc_{CORE} (Stop-Grant state) to Icc_{CORE} (Maximum) or Icc_{CORE} (Maximum) to Icc_{CORE} (Stop-Grant state) within the time interval listed in Section 1.1. During this step response the input current di/dt should not exceed 0.1A/µsec. For applications with multiple VRMs supplied by any voltage source on a board the step response di/dt of an individual VRM should not exceed 0.04A/ µsec.

2.3 Control Signals

These are signals that control the VRM (corresponding module pins are shown in Table 14).

2.3.1 Output Enable — OUTEN EXPECTED

The VRM should accept an open-collector, open-drain, or open-switch-to-ground signal to enable the output. This input circuit should have a pull-up resistor between 10 kΩ and 20 kΩ to a voltage in the 3.3V-5V range. The VRM should also accept the output of a standard or low-voltage TTL or CMOS device. A logic low or connect-to-ground state where the voltage on the OUTEN pin is less than 0.8V disables the VRM output; a voltage greater than 1.7V on this pin enables the output. This input should be capable of withstanding up to 5.5V.

When disabled, the VRM should not sink or source current on the processor core voltage plane.

Table 9 – OUTEN Specifications

Design Parameter	Specification
Signal Type	Input (Active HIGH) – Open-Collector, Open-Drain or Open-switch-to-ground
Voltage Range	3.3V – 5V (5.5V tolerant)
Pull-up Resistor	10kΩ – 20kΩ
V_{IH}	1.7V
V_{IL}	0.8V

2.3.2 V_{TT_PWRGD} REQUIRED

V_{TT_PWRGD} is an active HIGH signal used to indicate to the processor and to the clock generator that the processor V_{TT} plane is above the minimum specified level of 1.14V. Because of the interaction with the V_{TT} plane, there are three possible approaches to designing an on-board regulator solution:

1. Integrated Vcc_{CORE} and V_{TT} Regulator
   - Single Voltage Regulator that generates both Vcc_{CORE} and V_{TT} to the processor
   - V_{TT} is sensed internally and V_{TT_PWRGD} is an input and an output

2. Multi-part Vcc_{CORE} and V_{TT} Regulator solution
   - Vcc_{CORE} Regulator takes V_{TT_PWRGD} as an input only
     – Relies on the V_{TT} regulator circuit to control V_{TT_PWRGD}
   - V_{TT} Regulator provides V_{TT_PWRGD} as an output to indicate when the V_{TT} plane is stable
     – Initially holds V_{TT_PWRGD} inactive, then releases it when V_{TT} has been stable for the required 1ms
3. Independent Vcc_{CORE} and V_{TT} Regulator solution
   - Vcc_{CORE} Regulator takes in V_{TT} and implements V_{TT_PWRGD} as an input and an output
     – Initially holds V_{TT_PWRGD} inactive, then releases it when V_{TT} has been stable for the required 1ms
   - V_{TT} Regulator (legacy) provides no V_{TT_PWRGD} functionality

To ensure compatibility between VRM modules and system boards, VRM modules (except 1U form-factor versions) must implement solution 3 “Independent Vcc_{CORE} and V_{TT} Regulator solution”.

Regardless of the implementation, V_{TT_PWRGD} must observe the following operational characteristics:

1. V_{TT_PWRGD} should be glitch free when held LOW and be monotonic when transitioning from the LOW to HIGH state.
2. V_{TT_PWRGD} must be driven LOW BEFORE the processor V_{TT} plane begins to power up.
3. V_{TT_PWRGD} must be held LOW (inactive) until 1ms minimum, after V_{TT} crosses a minimum threshold of 1.14V. After the minimum 1ms delay, the V_{TT_PWRGD} signal is released and pulled up to processor V_{TT} by a pull-up resistor. **NOTE:** The V_{TT_PWRGD} output driver must support V_{TT_PWRGD} being shorted to ground.
4. After V_{TT_PWRGD} is released, the VRM must sample V_{TT_PWRGD} HIGH prior to reading the VID signals and driving the processor voltage.
5. If the processor V_{TT} plane is turned off without shutting down the VRM input voltage, then V_{TT_PWRGD} will become inactive and the VRM must stop driving the processor voltage.

Notes: V_{TT_PWRGD} is not intended for platform usage other than described within this document.

The VRM must NOT latch the VID signals.

Table 10 – V_{TT_PWRGD} Specifications

Design Parameter	Specification
Signal Type	Output/Input (Active HIGH) – Open-Drain
Voltage Range	V_{TT} = 1.25V (typical) – same voltage plane as the processor V_{TT}
Pull-up Resistor	1kΩ
V_{OH}	1.0V
V_{OL}	0.4V
$I_{LEAKAGE}$	50µA (maximum processor input leakage)

Figure 5 – V_{TT_PWRGD} Block Diagram

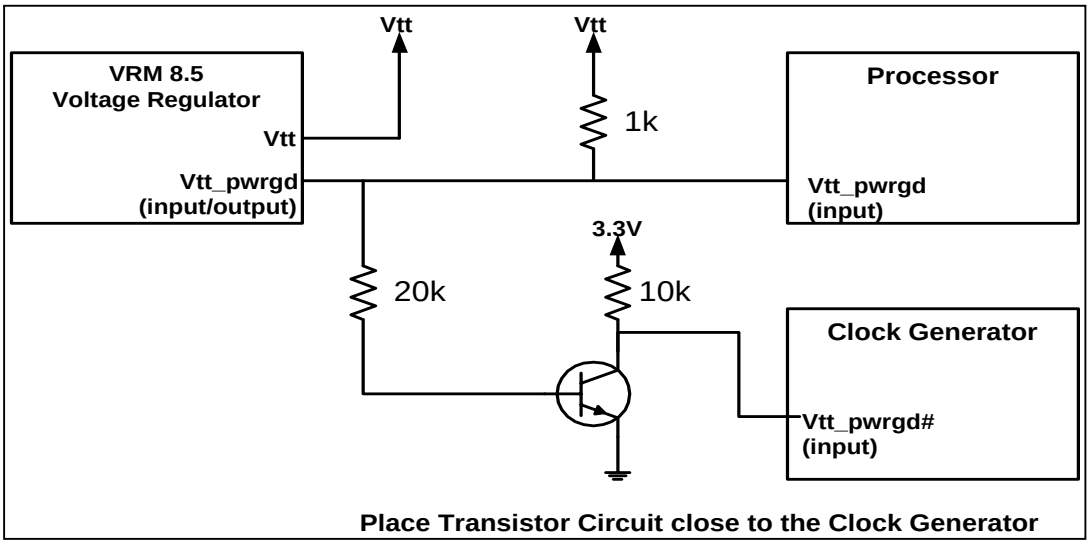
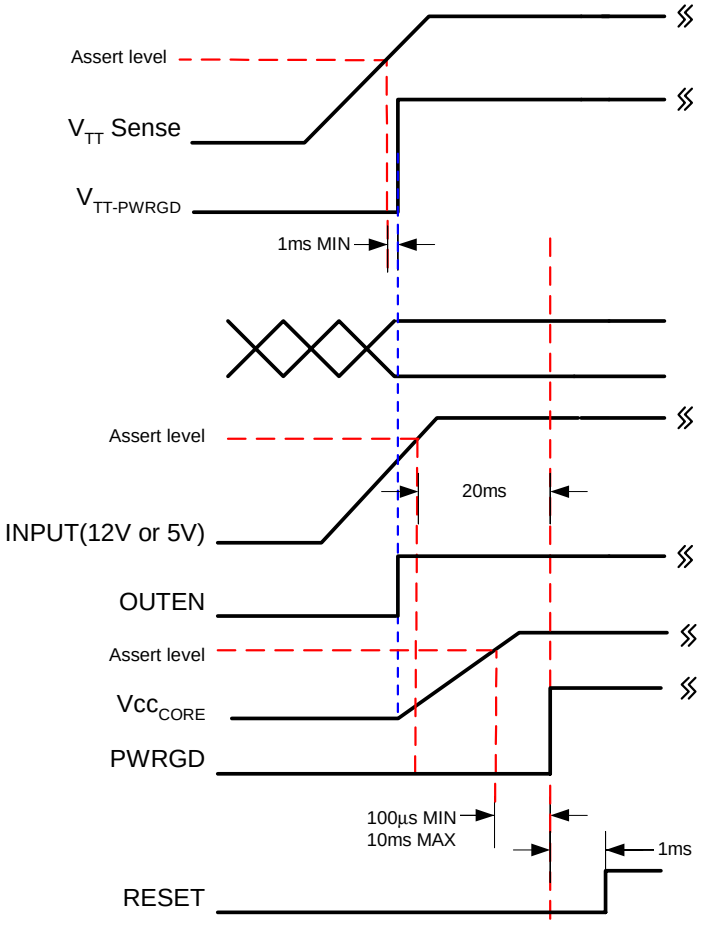


Figure 6 – Power and Control Sequencing



NOTE: VRM Vcc core should not ramp until after both $V_{TTPWRGD}$ and OUTEN are asserted

2.3.3 Power Good Output—PWRGD EXPECTED

An open collector signal consistent with TTL DC specifications should be provided. This signal should transition to the open (>100kΩ) state under the following conditions:

- within 20ms of the input stabilizing within the range specified in Section 1.2 and
- between 100µs and 10ms of Vcc_{CORE} crossing the low threshold point (VID nominal – 12%).

The signal should be in the low-impedance (to ground) state whenever Vout is more than ±12% from nominal and be in the open state whenever Vcc_{CORE} is within its specified range. Some systems logically combine power-good signals from multiple processors and reset all processors if any processor's Vcc_{CORE} source fails.

NOTE: PWRGD should not be directly connected to the processor PWRGOOD input due to processor input voltage level requirements. This signal is intended for system board logic usage.

Table 11 – PWRGD Specifications

Design Parameter	Specification
Signal Type	Output (Active HIGH) – Open-Collector
Voltage Range	3.3V – 5V (5.5V tolerant)
Pull-up Resistor	10kΩ – 20kΩ
V_{OH}	1.7V
V_{OL}	0.8V

2.3.4 Voltage Identification—VID[3:0, 25mV] REQUIRED

The VRM should accept five voltage identification (VID) signals from the processor, which are used to indicate the reference voltage required by the processor, as defined by Table 13. This reference voltage in conjunction with the Static and Transient voltage specifications then determines the voltage delivered to the processor for any given load.

The VID signals are dynamically configured during system power-up. To ensure correct detection of the VID signals, the voltage regulator must wait until V_{TT_PWRGD} is ACTIVE before reading the VID signals and delivering power. See Figure 6 for Power and Control sequencing information.

VRM designs may use internal (to the controller silicon) or external pull-up resistors to pull VID lines to 3.3V, where such pull-ups should have a resistance ≥ 1kΩ.

The VID table includes the entire 1.05V–1.825V range and values are based upon:

Table 12 – VID Specifications

Design Parameter	Specification
Signal Type	Input – Open-Drain
Voltage Range	3.3V (3.3V + 5% maximum DC)
Signal Levels	0 = Pull-down to V_{SS} 1 = Pull-up to 3.3V
Pull-up Resistor	1kΩ (minimum)
V_{IH}	2.0V
V_{IL}	0.8V
$I_{LEAKAGE}$	100µA (maximum processor input leakage per VID pin or ball)

Table 13 – Voltage Identification Code

Voltage Identification Code at Processor Pins or Balls					Vcc_{CORE}
VID25mV[2]	VID3[1]	VID2[1]	VID1[1]	VID0[1]	(V_{DC})
0	0	1	0	0	1.050
1	0	1	0	0	1.075
0	0	0	1	1	1.100
1	0	0	1	1	1.125
0	0	0	1	0	1.150
1	0	0	1	0	1.175
0	0	0	0	1	1.200
1	0	0	0	1	1.225
0	0	0	0	0	1.250
1	0	0	0	0	1.275
0	1	1	1	1	1.300
1	1	1	1	1	1.325
0	1	1	1	0	1.350
1	1	1	1	0	1.375
0	1	1	0	1	1.400
1	1	1	0	1	1.425
0	1	1	0	0	1.450
1	1	1	0	0	1.475
0	1	0	1	1	1.500
1	1	0	1	1	1.525
0	1	0	1	0	1.550
1	1	0	1	0	1.575
0	1	0	0	1	1.600
1	1	0	0	1	1.625
0	1	0	0	0	1.650
1	1	0	0	0	1.675
0	0	1	1	1	1.700
1	0	1	1	1	1.725
0	0	1	1	0	1.750
1	0	1	1	0	1.775
0	0	1	0	1	1.800
1	0	1	0	1	1.825

1. VID [3:0] correspond to legacy VRM 8.4 voltage levels for 1.3V – 1.8V.
2. VID 25mV provides a 25mV increment.

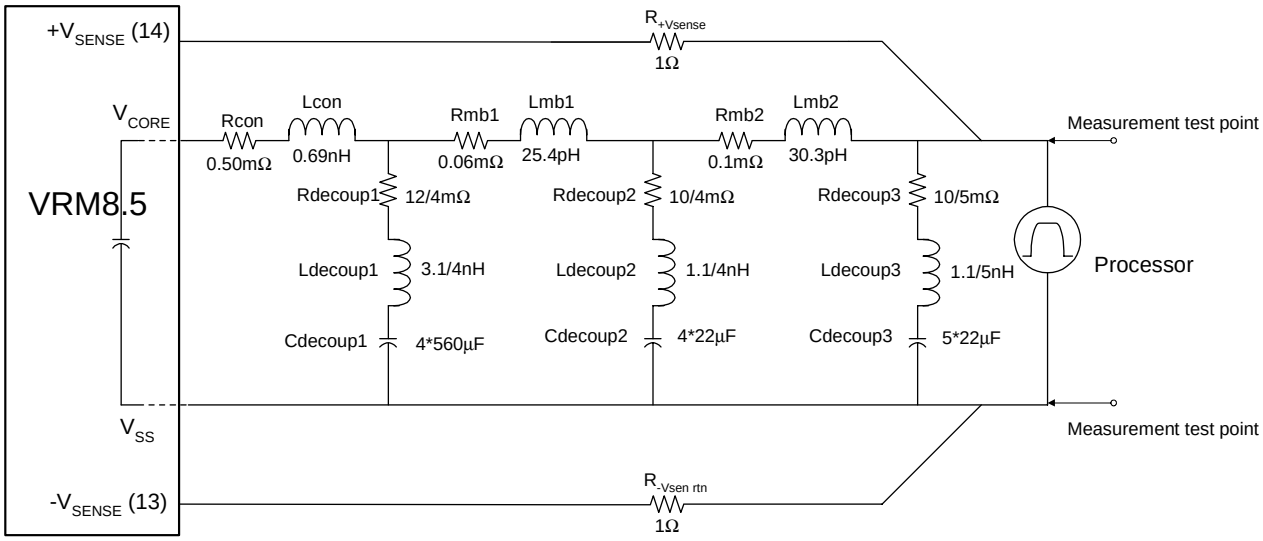
2.3.5 Remote Sense **EXPECTED**

The Remote Sense input lines ($+V_{SENSE}$ and $-V_{SENSE}$) are operational when these pins are connected on the system board to the $+Vcc_{CORE}$ and Vss at the load (processor socket pins or package balls) through an impedance of less than 1Ω. Figure 7 represents the distribution path and sense line for test purposes.

2.4 Module Test Conditions **EXPECTED**

Voltage regulator modules are expected to require bulk capacitance near the processor connector. Figure 7 represents the distribution load model for test purposes.

Figure 7 – VRM Test Circuit w/ Remotely Sensed Vcc_{CORE}
(Values are minimum except as noted)



* Typical value, based on four OS-CON capacitors, each 560µF. The actual value depends on board-specific requirements to meet the Vcc specifications at the processor socket pin or package ball.

2.5 Efficiency **PROPOSED**

The efficiency of the VRM should be greater than 80% at maximum output current and input voltage. It should not dissipate more power under any load condition than it does at maximum output current and maximum input voltage.

2.6 Fault Protection

These are features built into the VRM to prevent damage to itself or the circuits it powers.

2.6.1 Over Voltage Protection **PROPOSED**

Protection Level: The VRM should provide over-voltage protection by shutting itself off when the output voltage rises beyond Vtrip. Vtrip should be set between 110% and 125% of the voltage demanded by the processor (via the VID pins or balls) based upon the static no-load condition.

Voltage Sequencing: No combination of input voltages should falsely trigger an OVP event.

2.6.2 Short Circuit Protection **PROPOSED**

Load short circuit is defined as load impedance of less than approximately 40 mΩ. The VRM should be capable of withstanding a continuous short-circuit to the output without damage or over-stress to the unit.

2.6.3 Reset After Shutdown **PROPOSED**

If the VRM goes into a shutdown state due to a fault condition on its outputs it should return to normal operation after the fault has been removed, or after the fault has been removed and power has been cycled off and on.

2.7 Current Sharing **PROPOSED**

The pin designated I_{SHARE} is intended to permit two or more VRMs to balance the total current load between them. There is no expectation of interoperability between the sharing mechanisms of different VRM or system implementations.

3 Module Requirements

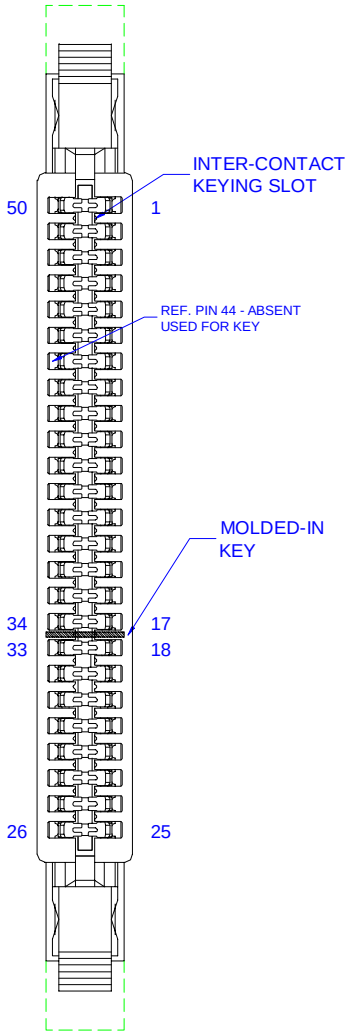
3.1 VRM Connector **EXPECTED**

The VRM interface with the system board is a 0.100" pitch, 50-pin edge connector, with an overall 3.04" length: AMP* 145432, FOXCONN* ES02599, or equivalent (Intel does not endorse third-party products mentioned in this document). The connector contains a retention mechanism to hold the VRM in place with a maximum open length of 4.00" from retention arm to retention arm. Assume 4-oz. copper lands on the VRM PCB to get a 44A current rating. Table 14 shows the VRM pin-out definitions. Figure 8 shows the connector details.

Table 14 – Module Pin-out

Pin #	Row A	Pin #	Row B
1	5Vin	50	5Vin
2	5Vin	49	5Vin
3	5Vin	48	5Vin
4	5Vin	47	5Vin
5	12Vin	46	12Vin
6	12Vin	45	12Vin
7	Reserved	44	No Contact
8	VID 0	43	VID 1
9	VID 2	42	VID 3
10	VID 25mV	41	PWRGD
11	OUTEN	40	I_{SHARE}
12	V_{TT_PWRGD}	39	V_{TT}
13	$-V_{SENSE}$ (rtn)	38	V_{SS}
14	$+V_{SENSE}$	37	V_{SS}
15	Vcc_{CORE}	36	Vcc_{CORE}
16	V_{SS}	35	V_{SS}
17	Vcc_{CORE}	34	Vcc_{CORE}
Mechanical		Key	
18	V_{SS}	33	V_{SS}
19	Vcc_{CORE}	32	Vcc_{CORE}
20	V_{SS}	31	V_{SS}
21	Vcc_{CORE}	30	Vcc_{CORE}
22	V_{SS}	29	V_{SS}
23	Vcc_{CORE}	28	Vcc_{CORE}
24	V_{SS}	27	V_{SS}
25	Vcc_{CORE}	26	Vcc_{CORE}

Figure 8 – VRM Connector

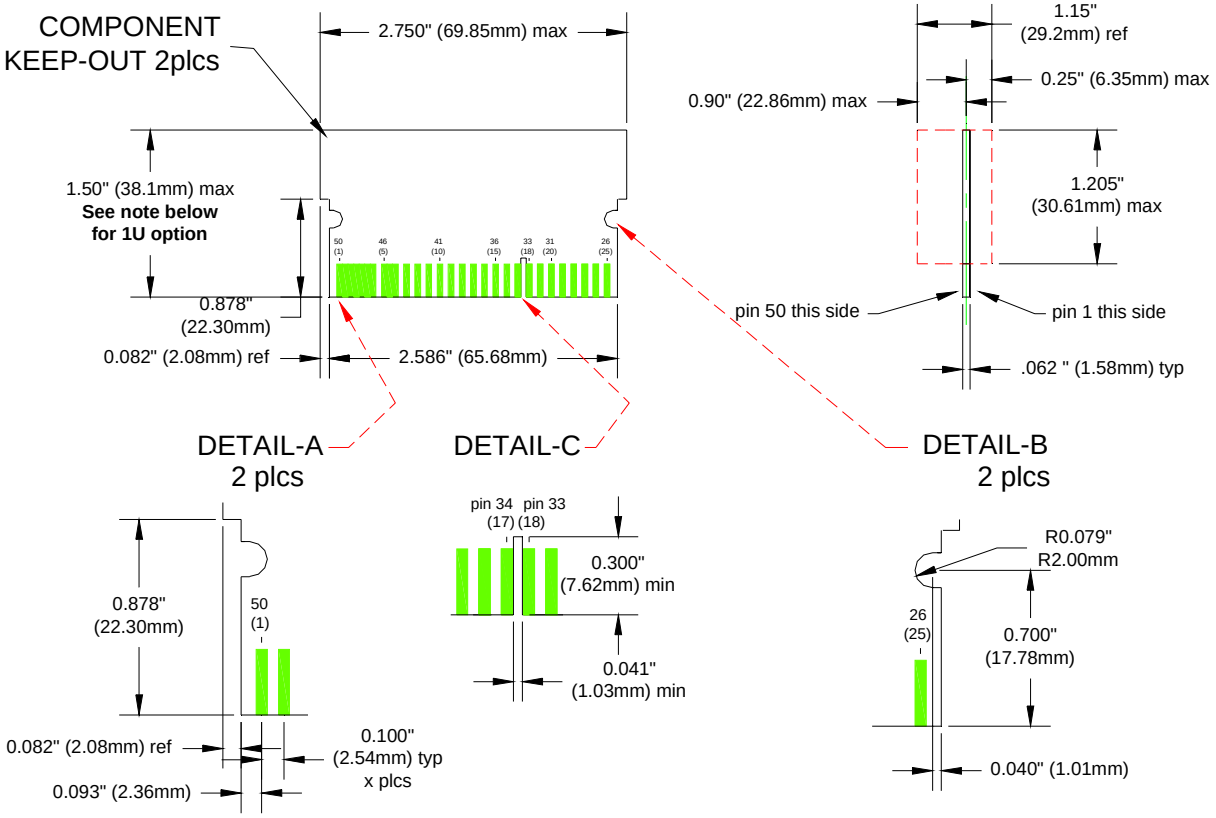


3.2 Mechanical Dimensions

EXPECTED

The converter dimensions should be equal to or less than 2.75” x 1.15” x 1.5” (which should include converter edge tabs) as illustrated in Figure 9. Maximum component height should be 0.90" on pin 50 side and 0.25" on pin 1 side of the module. Note that the 1.15” dimension is total width; non-symmetrical dimensions about the centerline are indicated in Figure 9

Figure 9 – Voltage Regulator Module Dimensions



Note: An alternate form factor can be adopted for application into 1U Server Systems by reducing the requirements of this dimension (height) to 1.00" (25.4mm) maximum.

3.3 Connector key

The VRM shall contain a single notch between pins 17 & 18 and pins 33 & 34 – see detail C

3.4 Heat Sink Connection

Heat sinks cannot be connected to any potential other than ground.

4 Tests and Standards

4.1 Reliability

The VRM should be designed to function to electrical specifications, within the environmental specifications, with 60°C air at a velocity of 100 LFM directed along the connector axis.

4.1.1 Component De-rating **PROPOSED**

The following component de-rating guidelines should be followed:

- Semiconductor junction temperatures should be < 115°C with ambient at 50°C.
- Capacitor case temperature should not exceed 80 % of rated temperature.
- Resistor wattage de-rating should be consistent with the resistor type.
- Component voltage and current de-rating should be > 20%, the effects of ripple current heating should be accounted for in this de-rating.

4.1.2 Mean-Time-Between-Failures (MTBF) PROPOSED

Design, including materials, should be consistent with the manufacture of units with an MTBF of 500,000 hours of continuous operation at 55°C, maximum-outputs load, and worst-case line, while meeting specified requirements. MTBF should be calculated in accordance with MIL-STD-217F (parts stress method).

4.2 Environmental PROPOSED

Design, including materials, should be consistent with the manufacture of units that meet the environmental reference points in Table 15.

Table 15 – Environmental Specifications

	Operating	Non-Operating
Temperature	Ambient 0°C to +60°C at full load with a maximum rate of change of 5°C/10 minutes minimum but no more than 10°C/hour. [1]	Ambient –40°C to 70°C with a maximum rate of change of 20°C/hour. [2]
Humidity	To 85% relative humidity.	To 95% relative humidity.
Altitude	0 to 10,000 feet	0 to 50,000 feet.
Electrostatic discharge	15 KV initialization level. The direct ESD event shall cause no out-of-regulation conditions. [3]	25 KV initialization level.

[1] See Section 2.1.4 for static and transient test conditions.
[2] Thermal shock of –40°C to +70°C, 10 cycles; transfer time shall not exceed 5 minutes, duration of exposure to temperature extremes shall be 20 minutes.
[3] Includes overshoot, undershoot, and nuisance trips of the over-voltage protection, over-current protection or remote shutdown circuitry.

4.3 Shock and Vibration PROPOSED

The VRM should not be damaged and the interconnect integrity not compromised during:

- A shock of 50G with an 11 millisecond half sine wave, non-operating, the shock to be applied in each of the orthogonal axes.
- Vibration of 0.01G² per Hz at 5 Hz, sloping to 0.02G² per Hz at 20 Hz and maintaining 0.02G² per Hz from 20 Hz to 500 Hz, non-operating, applied in each of the orthogonal axes.

4.4 Electromagnetic Compatibility PROPOSED

Design, including materials, should be consistent with the manufacture of units that comply with the limits of FCC Class B and VDE 243 Level B for radiated emissions, given the existence of an external package around the VRM with 20dB of shielding.

4.5 Safety PROPOSED

Design, including materials, should be consistent with the manufacture of units that meet the standards of UL flammability specifications per 94V-0.

5 Icc Slew Rate Specifications

This section contains typical current slew rate data for processors covered by this design guideline. Actual slew rate values and wave-shapes may vary slightly depending on the type and size of decoupling capacitors used in a particular implementation.

5.1 Intel® Pentium® III Processor (CPUID 068xh) Slew Rate

Note: All slew rate data correspond to the processor socket pins on the solder side of the motherboard and should be used for embedded voltage regulator-down (VRD) designs.

5.1.1 Slew Rate – 23A Load Step

Figure 10 – Slew Rate (23A)

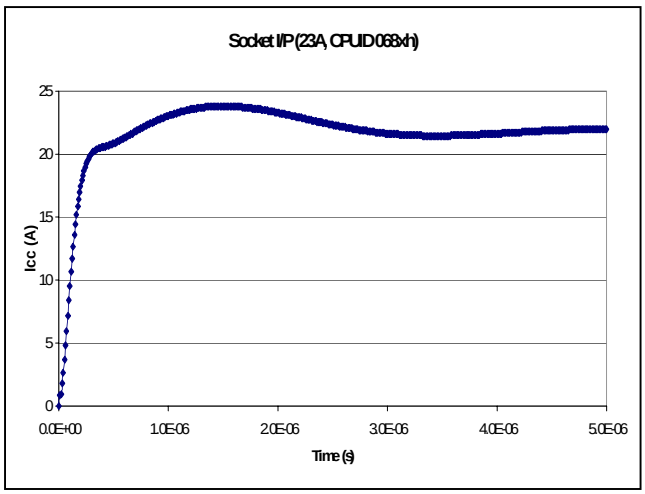


Table 16 – PWL Slew Rate Data (23A)

Time (µs)	Icc (A)
0.1	9.55
0.15	14.4
0.5	20.85
1	23.04
1.5	23.44
2	23.28
2.5	22.32
3	21.63
3.5	21.45
4	21.63
4.5	21.88
5	22.01

5.2 Intel® Pentium® III Processor on 0.13 Micron Process Slew Rate

Note: All slew rate data correspond to the processor socket pins on the solder side of the motherboard or the processor package balls and should be used for embedded voltage regulator designs (VRD).

5.2.1 Slew Rate – 28A Load Step

Figure 11 – Slew Rate (28A)

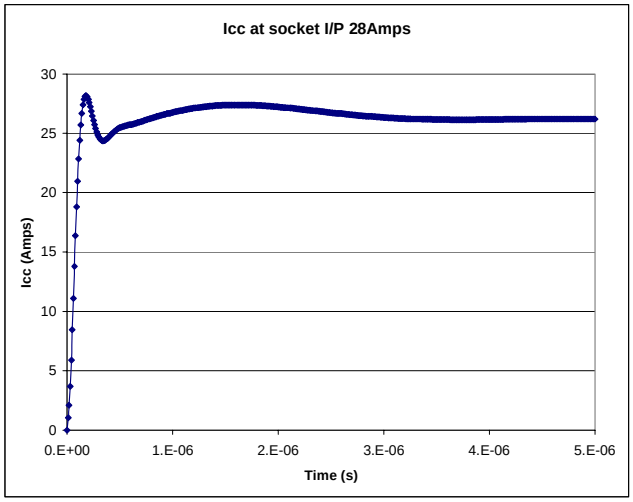


Table 17 – PWL Slew Rate Data (28A)

Time (µs)	Icc (A)
0.1	20.95
0.15	27.40
0.5	25.47
1	26.76
1.5	27.37
2	27.22
2.5	26.74
3	26.33
3.5	26.16
4	26.15
4.5	26.2
5	26.2

5.2.2 Slew Rate – 21A Load Step

Figure 12 – Slew Rate (21A)
(21A)

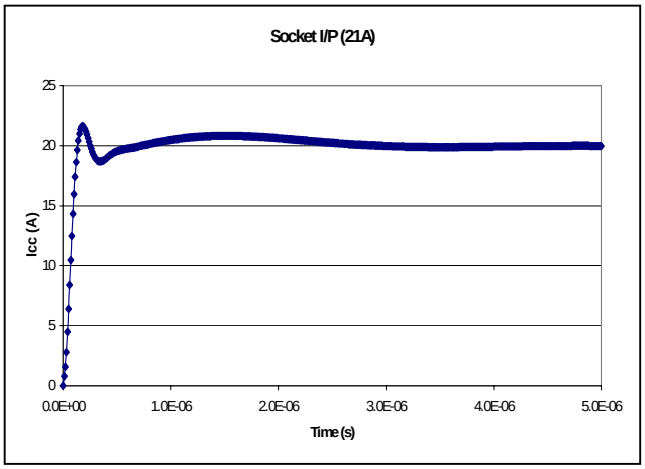


Table 18 – PWL Slew Rate Data

Time (µs)	Icc (A)
0.1	15.97
0.15	20.98
0.5	19.55
1	20.48
1.5	20.82
2	20.61
2.5	20.23
3	19.96
3.5	19.88
4	19.92
4.5	19.97
5	19.97

5.3 VRM Slew Rate

Note: All slew rate data correspond to the voltage regulator module socket pins on the solder side of the motherboard and should be used in combination with 5.1 and 5.2 for VRM design.

5.3.1 Slew Rate – 28A Load Step

Figure 13 – Slew Rate (28A)

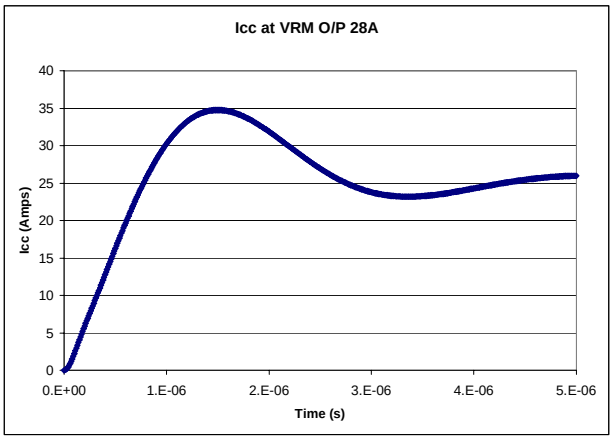


Table 19 – PWL Slew Rate Data (28A)

Time (µs)	Icc (A)
0.1	2.2
0.15	4.11
0.5	16.3
1	30.3
1.5	34.8
2	31.9
2.5	27.0
3	23.8
3.5	23.3
4	24.3
4.5	25.5
5	26.0

5.3.2 Slew Rate – 21A Load Step

Figure 14 – Slew Rate (21A)

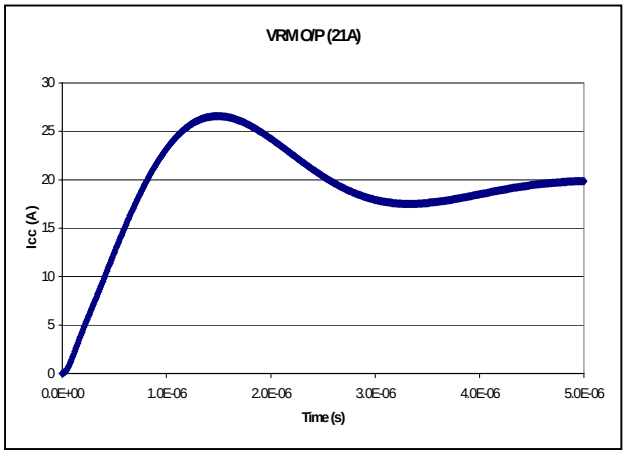


Table 20 – PWL Slew Rate Data (21A)

Time (µs)	Icc (A)
0.1	1.7
0.15	3.14
0.5	12.5
1	23.2
1.5	26.6
2	24.2
2.5	20.4
3	17.9
3.5	17.6
4	18.5
4.5	19.4
5	19.9

5.3.3 Slew Rate – CPUID 068xh – 23A Load Step

Figure 15 – Slew Rate (23A)

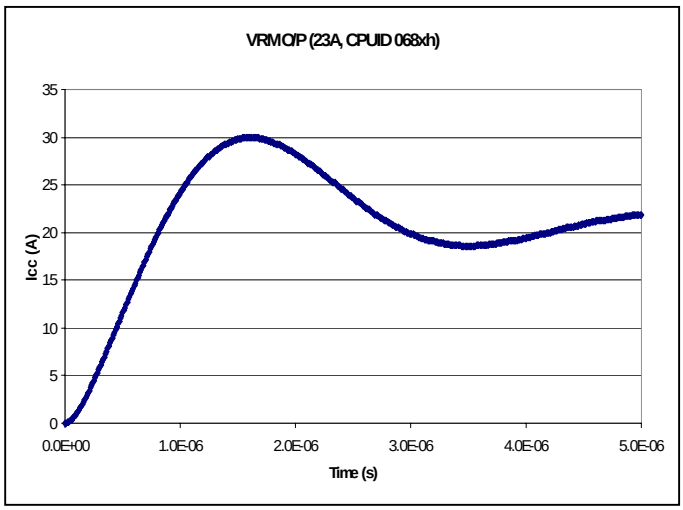


Table 21 – PWL Slew Rate Data (23A)

Time (µs)	Icc (A)
0.1	1.01
0.15	2.02
0.5	11.6
1	24.2
1.5	26.8
2	28.2
2.5	23.6
3	19.9
3.5	18.6
4	19.4
4.5	20.9
5	21.9