Intel® Server System SR1680MV

Technical Product Specification

Intel order number E76653-003

Revision 1.3

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Enterprise Platforms and Services Division – Marketing

Revision History

Date	Revision Number	Modifications
July 2009	0.1	First release.
July 2009	1.0	Updated IO Board Pin definition and Regulator Information.
Aug 2009	1.1	Updated Pin definition for PDB, SATA board, and Function Jumper.
Nov 2009	1.2	Updated Pin definition for PDB,SATA board, Server board power connector, and Function Jumper.
March 2010	1.3	Updated Regulation Section and remove CNCA(China- CCC) Certification content.

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1. Introduction

This Technical Product Specification (TPS) provides system-specific information detailing the features, functionality, and high-level architecture of the Intel® Server System SR1680MV.

The Intel® Server System SR1680MV may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Refer *Intel® Server System SR1680MV Specification Update* for published errata.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Product Overview
- Chapter 3 – System Board
- Chapter 4 – Power Subsystem
- Chapter 5 – Cooling Subsystem
- Chapter 6 – System Board Interconnects
- Chapter 7 – Hard Disk Drive Support
- Chapter 8 – System LED, Button and Jumper Functionality
- Chapter 9 – IO Board extended Assembly
- Chapter 10 – Basic Input/Output System (BIOS)
- Chapter 11 – System Management System
- Chapter 12 – Environmental Specifications
- Chapter 13 – Regulatory and Certification Requirements
- Appendix A – Integration and Usage Tips
- Glossary
- Reference Documents

1.2 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own system development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel-developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of airflow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Overview

The Intel® Server System SR1680MV is a rack mount 1U server system with features designed to support the twin high-density high-performance computing server market. The system offers the following configuration:

- Intel® Server System SR1680MV

This chapter provides a high-level overview of the system features. The following chapters provide greater detail for each major system component or feature.

Table 1. System Feature Set

Feature	Description
Processor	▪ Support for one or two Intel® Xeon® Processor 5500 series and Intel® Xeon® Processor 5600 series processors in FC-LGA 1366 Socket B package with up to 95 W Thermal Design Power (TDP) . ▪ Located on LGA 1366-pin processor socket
Chipset	▪ Intel® 5500 Chipset (IOH 24D) ▪ Intel® ICH10R I/O Controller Hub
System Memory	▪ Three channels per processor; up to three DIMMs per channel ▪ 72 GB max per processor; 8GB DIMM modules available at launch ▪ Support DDR3 speeds of 800/1066/1333 MHz ▪ Support up to three registered DIMMs per channel, 8GB max per registered DIMM (4GB qualified), up to 144 GB total ▪ Support up to two unbuffered DIMMs per channel, 4GB max per unbuffered DIMM ▪ Support single-rank (SR), dual-rank (DR), and quad-rank (QR) DIMM modules
Video	▪ On-board SeverEngines* Pilot II controller ▪ Integrated 2D Video Controller ▪ High speed Integrated 24-bit RAMDAC ▪ Single lane PCI-Express host interface
LAN	Two 10/100/1000 ports provided by Intel® 82576 PHYs
Expansion Capabilities	One PCI Express* Gen2 riser slot supporting half-length/low-profile riser cards
Hard Drives	▪ Up to four 2.5-inch SATA drivers with two backplanes (two for each node) ▪ Intel® Matrix RAID with Software RAID levels 0/1
Peripheral Interfaces	**Front connections:** ▪ One DB-15 video connector ▪ One DB-9 Serial connector ▪ Two USB 2.0 connector **Rear connections:** ▪ Two RJ-45 10/100/1000 Mbps network connections
Power Supply	One 1100-W power supply module
Fans	▪ Six system fans (three for each node) ▪ One power supply fans

Feature	Description
Server Management	On-board Server Engines* Pilot II Controller ▪ Integrated Baseboard Management Controller (Integrated BMC), IPMI 2.0 compliant

2.1 System Overview

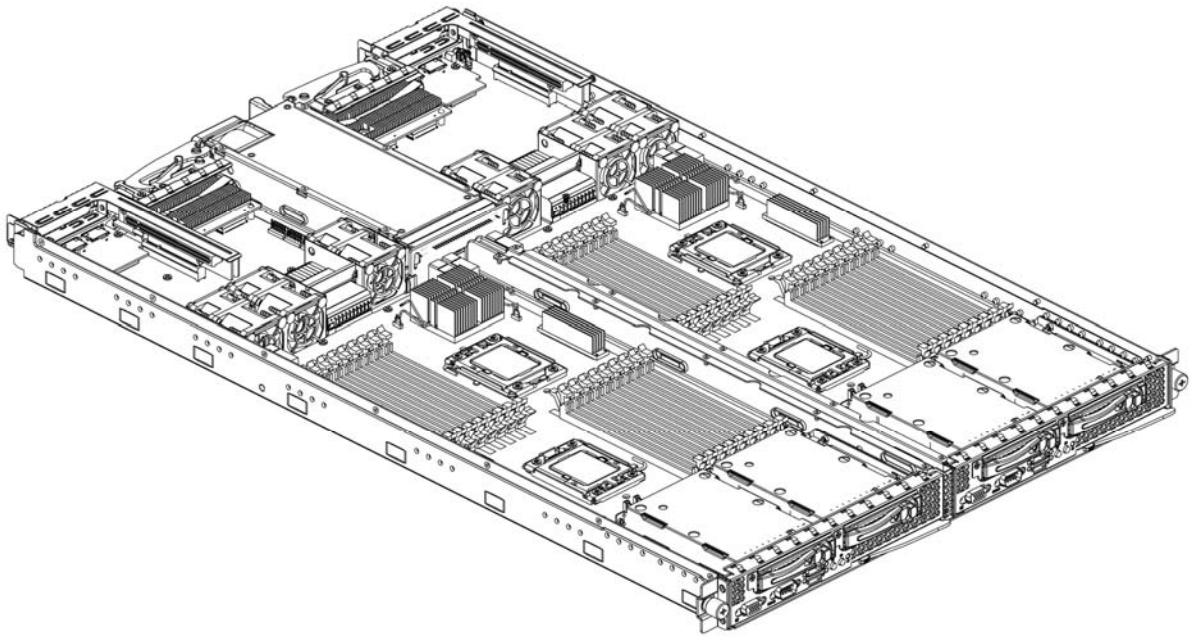


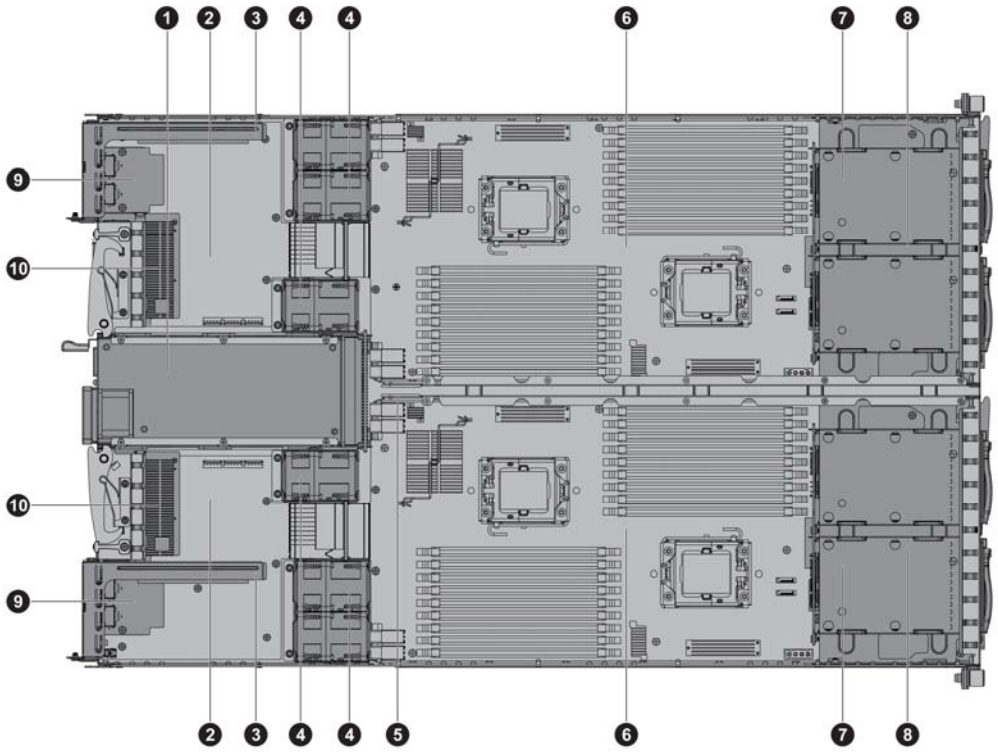
Figure 1. Intel® Server System SR1680MV with 2.5-inch Pluggable HDDs

2.2 System Dimensions

Table 2. System Dimensions

Height	43.2 mm
Width	448 mm
Depth (without front panel)	714.2 mm
Minimum Weight	11.7 kg
Maximum Weight	17.16 kg

2.3 System Components

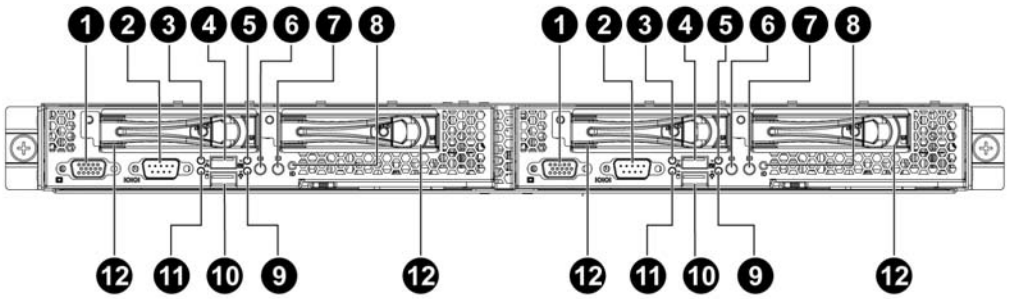


❶ Power Supply	❺ Power Distributon Boards
❷ IO Boards	❻ Motherboards
❸ Riser Card Assemblies	❼ SATA HDD Backplane
❹ System Fans	❽ 2.5” Pluggable HDD Bays

Figure 2. Server Components with 2.5-inch Pluggable HDDs

2.4 Server System Front layout

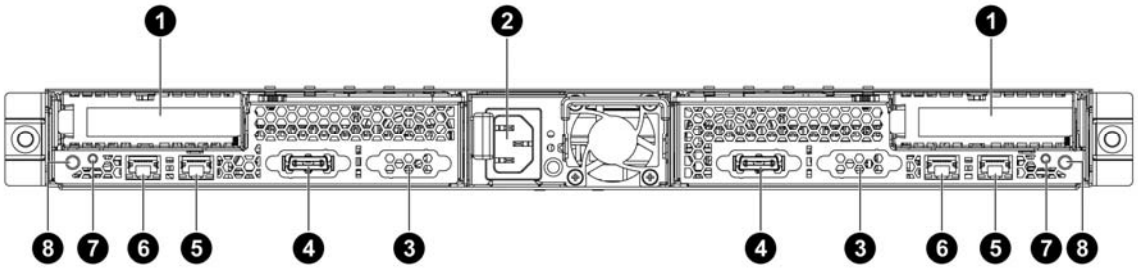
The system is designed to support 2.5-inch hot-swap SATA hard disk drives.



❶ VGA Port	❼ UID Button
❷ Serial Port	❽ UID LED
❸ NIC LED	❾ Power LED
❹ Front Panel USB Port	❿ Front Panel USB Port
❺ System Health LED	⓫ HDD LED
❻ Power Button	⓬ 2.5-inch Pluggable HDDs

Figure 3. System Front View

2.5 Server System Rear Layout



❶ PCI-E Cages	❺ Rear NIC1 Ports
❷ AC Power Outlet	❻ Rear NIC2 Ports
❸ IO Port	❼ Rear UID LEDs
❹ IO Port	❽ Rear UID Buttons

Figure 4. System rear layout

3. System Board

This chapter describes the system board for the Intel® Server System SR1680MV.

3.1 Introduction

The Intel® Server SR1680MV system Board provides most of the basic functions for the system. Nearly all of the boards from the board set plug into or cable to the main board.

3.2 System Board Overview

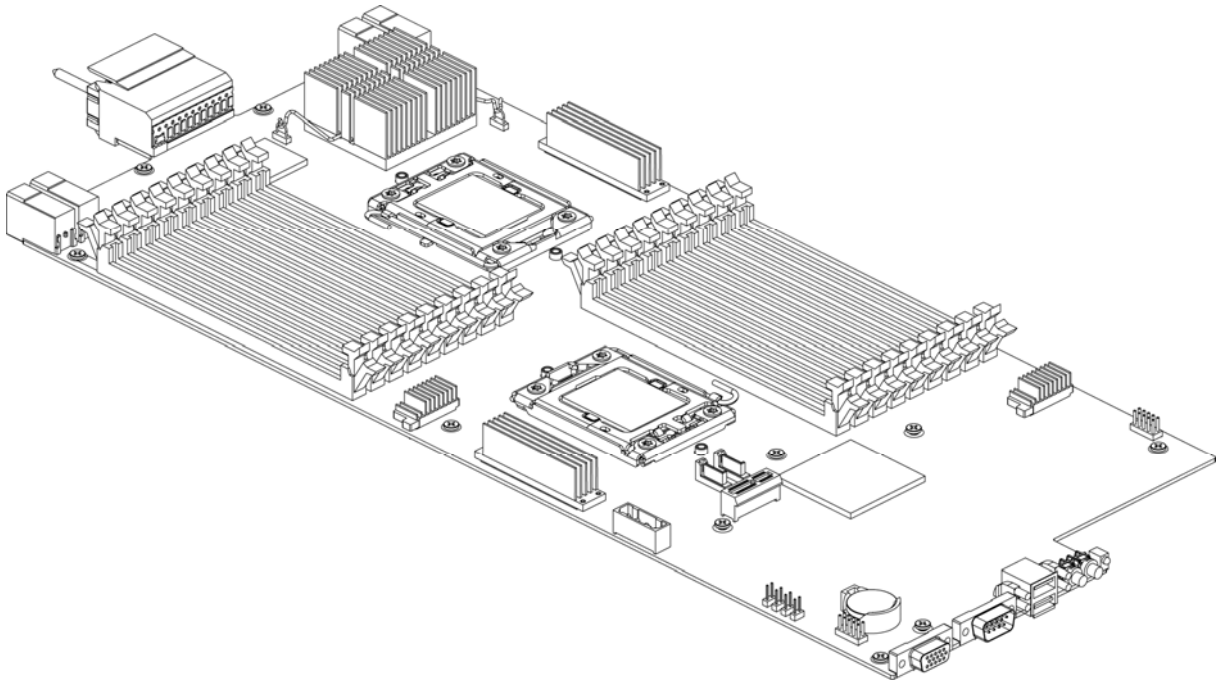


Figure 5. Server Board Overview

The following figure shows the server board's layout. Each connector and major component is identified by a number or letter, and a description is given below the figure.

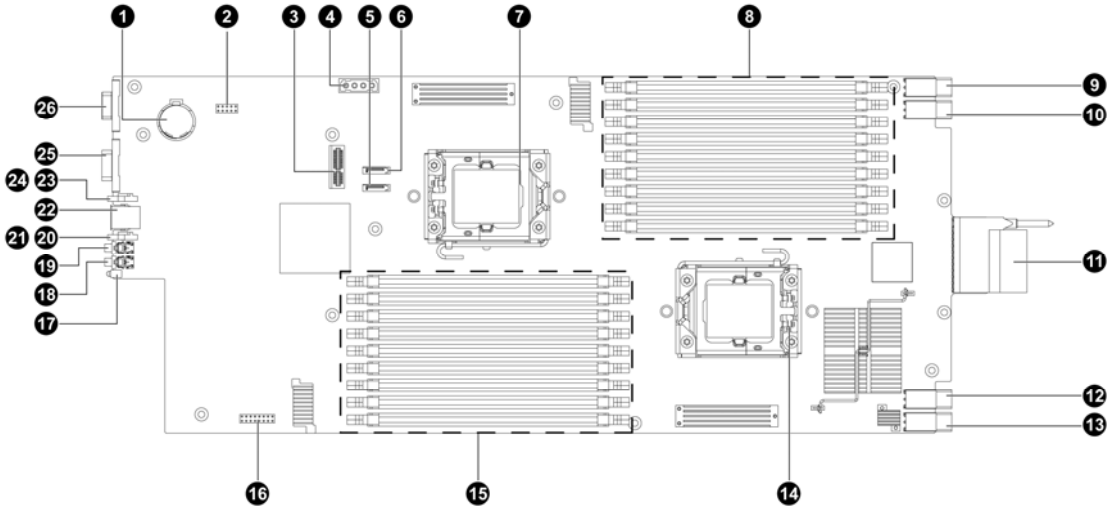


Figure 6. Server Board Components

Table 3. Major Board Components

1 System Battery (BH1)	14 Processor 2 (CPU 2)
2 ICH Functions Jumper (J30)	15 DIMM Socket Group 2 (J17, J18, J19, J20, J21, J22, J23, J24, J25)
3 HDD Backplane Connector	16 MISC Jumper
4 SATA Power Connector (J47)	17 Front UID LED
5 Motherboard SATA4 Connector (J29)	18 Front UID Button
6 Motherboard SATA3 Connector (J31)	19 Power Button
7 Processor 1 (CPU 1)	20 System Health LED
8 DIMM Socket Group1 (J7, J8, J9, J10, J11, J12, J13, J14, J15)	21 Power LED
9 Motherboard Power Connector4 (J5)	22 Front USB Ports
10 Motherboard Power Connector3 (J4)	23 NIC LED
11 Motherboard IO Connector (J1)	24 HDD LED
12 Motherboard Power Connector2 (J3)	25 Serial Port
13 Motherboard Power Connector1 (J2)	26 VGA Port

3.3 Functional Architecture

This section describes the primary functions, blocks, and components that reside on the main board. The section is laid out as follows:

- Chipset components
- Primary interfaces to the memory and I/O riser
- Additional information regarding other functional blocks on the board

3.3.1 Processors Support

Each system board is designed to support dual Intel® Xeon® Processor series and Intel® Xeon® Processor 5600 series. This section provides more information on the processor sequence and its supported technologies.
The following table lists the processor sequence and each processor property that the board can support.

Table 4. Processor Support Chart

Processor Generation	Intel® Xeon® Processor 5500 series and Intel® Xeon® Processor 5600 series					
Processor Technology	45 nm and 32nm					
Package	FC-LGA 1366 Lands					
Processor Sequence	X5570/X5560/X5550	E5540/E5530/E5520	E5506/E5504/E5502	L5530	L5520	L5506
Clock speed (GHz)/Watt	2.93/2.80/266/95W	2.53/2.40/2.26/80W	2.13/2.00/1.86/80W	2.40/60W	2.26/60W	2.13/60W
QPI Speed (GT/sec)	6.4	5.86	4.8	5.86	5.86	4.8
Cache	8 MB	8 MB	4 MB	8 MB	8 MB	4 MB
Memory Speed (DDR3 only)	1333/1066/800	1066/800	800	1066/800	1066/800	800
Applied Technology						
DBS	v	V	v	v	v	V
Virtualization Technology	v	V	v	v	v	V
FlexMigration	v	V	v	v	v	V

The Intel® Xeon® 5500 series processor and Intel® Xeon® Processor 5600 series are multi-core processors based on 45 nm and 32nm process technology. Intel QuickPath Interconnection, a cache-coherent point to point links capable of up to 6.4GT/s, up to 8MB of shared cache, and an integrated memory controller.

3.3.2 Intel® 5500 Chipset (IOH 24D) and 82801JR(ICH10R)

The Intel® SR1680MV Server System board implements Intel® 5500 (IOH 24D) chipset and 82801JR (ICH10R). This section describes the general functionality and features of this chipset.

The Intel® 5500 IOH 24D chipset provides the connection point between the Intel® processor QuickPath Interconnection and a variety of I/O components.

The Intel® 5500 IOH 24D has the following capabilities:

- Two Intel® QuickPath Interconnection full-width links with 20 lanes in each direction
- One x16 PCI Express* Gen2 port or two x8 PCI Express* Gen2 ports, each supporting up to 5 GB/s/direction peak bandwidth
- One x4 ESI link interface supporting PCI Express* Gen1 (2.5 Gbps) transfer rate
- Dedicated legacy bridge (Intel® I/O Controller Hub (ICH)) interface
- Intel® I/O Acceleration Technology (I/OAT) 3 support
- Intel® Virtualization Technology for Directed I/O (Intel® VT-d), 2nd revision support
- Servers supported by Intel® Manageability Engine (Intel® ME)
- Improved RAS features achieved by protecting internal data paths through ECC and parity protection mechanism
- Power management supports system states (S0, S1, S3, S4, S5)
- Server security supported by TPM 1.2 and Intel VT-d

ICH10R functions and capabilities include:

- Provides up to six PCI Express* root ports. Each root port supports 2.5 Gb/s bandwidth in each direction. PCI Express* is compliant with PCI Express* Base Specification, Rev 1.1. Each PCI-E bus support for 33 MHz PCI operations.
- Two integrated SATA controllers that support independent DMA operation on up to six ports and support data transfer rates of up to 3.0 Gb/s.
- Provides up to 12 USB 2.0 ports. Data transfer speed up to 480 Mb/s, 40 times faster than full-speed USB.
- Gigabit Ethernet Controller incorporated. The LAN controller operates at multiple speeds (10/100/1000 MB/s) either in duplex or half-duplex mode.
- Low pin count interface
- System Management Bus (SMBus) 2.0 compliant

- Intel® Matrix Storage Technology support. The industry-leading technology provides RAID 0, 1, 5, 10 functionality on up to six SATA ports.
- Supports Intel® High Definition Audio
- Supports Intel® Trusted Execution Technology
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support
- Intel® Quiet System Technology (Intel® QST)

The ICH10 integrates four fan speed sensors (four Tach signals) and three fan speed controllers that allow the monitoring and controlling up to four system fans on the system. Coupled with Intel® QST, the server provides more effective thermal and acoustic management for the platform.

- Intel® Anti-Theft Technology: This feature helps the end-user the ability to restrict access to HDD data by unknown parties.
- Integrated Intel Trusted Platform Module (TPM) Rev.1.2.

3.3.3 Memory support

This section contains information on memory topology, memory type, capacity and population rules.

Memory Topology

Intel® Xeon® 5500 platform offers a wide variety of configurations; the following are generic population requirements:

- All DIMMs must be DDR3 DIMMs.
- If 1.35V (DDR3L) and 1.50V (DDR3) DIMMs are mixed, the DIMMs will run at 1.50V.
- Registered DIMMs must be ECC only, Unbuffered DIMMs can be ECC or non-ECC.
- Mixing of Registered and Unbuffered DIMMs is not allowed.
- It is allowed to mix ECC and non-ECC Unbuffered DIMMs. The presence of a single non-ECC Unbuffered DIMM will result in disabling ECC functionality.
- DIMMs with different timing parameters can be installed on different slots within the same channel, but only timings that support the slowest DIMM will be applied to all. As a consequence, faster DIMMs will be operated at timings supported by the slowest DIMM populated. The same interface frequency (DDR3-800, DDR3-1066, or DDR3-1333) will be applied to all DIMMs on all channels on the platform (both processors).
- DIMM with DDR3-1333 speed is allowed only when one DIMM per Channel (1DPC) is populated. If two 1333 MT/s capable UDIMMs or RDIMMs are detected in the same channel, BIOS would flag this as a warning and force the speed to 1066 MT/s.

- When one quad rank DIMMs is used, it must be populated in DIMM slot0 (farthest away from the CPU) of a given channel.
- Mixing of quad ranks DIMMs in one channel and three DIMMs in other channel (3DPC) on the same CPU socket is not allowed. If such configuration is detected on a CPU socket, BIOS would flag this as a warning and disable the QR DIMM channel(s)

For the following sub-sections, there will be more information on the DIMM population rules for your reference.

Memory Controller integrated in processor:

- DDR3 – 1333/1066/800 MT/s depending on DIMM population
- Supports both registered (RDIMM) and unbuffered (UDIMM) DIMM modules
- Supports single-rank (SR), dual-rank (DR), and quad-rank (QR) DIMM modules
- 72 GB max memory limit per processor, 8GB DIMM modules available at launch
- Three channels per processor
- Up to three DIMMs-per-channel (DPC), depending on platform implementation
- RAS – Independent, Mirrored, Combined Channel (Lockstep) functionality

DIMM Population Rules for Three Slots Configuration

For three slots per channel configurations, the Intel Xeon platform requires DIMMs within a channel to be populated starting with the DIMMs farthest from the processor in a “fill farthest” approach. Intel recommends checking for correct DIMM placement during BIOS initialization. Additionally, Intel strongly recommends that all designs follow the DIMM ordering, command clock, and control signal routing. This addressing must be maintained to be compliant with the reference BIOS code supplied by Intel.

Table 5. RDIMM Population Configuration for Three Slots per Channel

Configuration Number	POR Speed	1N or 2N	DIMM3	DIMM2	DIMM1
1	DDR3-1333,1066&800	1N	Empty	Empty	Single-rank
2	DDR3-1333,1066&800	1N	Empty	Empty	Dual-rank
3	DDR3-1066&800	1N	Empty	Empty	Quad-rank
4	DDR3-1066&800	1N	Empty	Single-rank	Single-rank
5	DDR3-1066&800	1N	Empty	Single-rank	Dual-rank
6	DDR3-1066&800	1N	Empty	Dual-rank	Single-rank
7	DDR3-1066&800	1N	Empty	Dual-rank	Dual-rank
8	DDR3-800	1N	Empty	Single-rank	Quad-rank
9	DDR3-800	1N	Empty	Dual-rank	Quad-rank

Configuration Number	POR Speed	1N or 2N	DIMM3	DIMM2	DIMM1
10	DDR3-800	1N	Empty	Quad-rank	Quad-rank
11	DDR3-800	1N	Single-rank	Single-rank	Single-rank
12	DDR3-800	1N	Single-rank	Single-rank	Dual-rank
13	DDR3-800	1N	Single-rank	Dual-rank	Single-rank
14	DDR3-800	1N	Dual-rank	Single-rank	Single-rank
15	DDR3-800	1N	Single-rank	Dual-rank	Dual-rank
16	DDR3-800	1N	Dual-rank	Single-rank	Dual-rank
17	DDR3-800	1N	Dual-rank	Dual-rank	Single-rank
18	DDR3-800	1N	Dual-rank	Dual-rank	Dual-rank

Table 6. UDIMM Population Configurations for Three Slots per Channel

Configuration Number	POR Speed	1N or 2N	DIMM3	DIMM2	DIMM1
1	DDR3-1333,1066&800	1N	Empty	Empty	Single-rank
2	DDR3-1333,1066&800	1N	Empty	Empty	Dual-rank
3	DDR3-1066&800	2N	Empty	Single-rank	Single-rank
4	DDR3-1066&800	2N	Empty	Single-rank	Dual-rank
5	DDR3-1066&800	2N	Empty	Dual-rank	Single-rank
6	DDR3-1066&800	2N	Empty	Dual-rank	Dual-rank

Table 7. RDIMM Population Configurations (Intel® Xeon® Processor 5600 series only) for three slots per Channel

Configuration Number	POR Speed	1N or 2N	DIMM3	DIMM2	DIMM1
1	DDR3L-1066&800	1N	Empty	Empty	Single-rank
2	DDR3L-1066&800	1N	Empty	Empty	Dual-rank
3	DDR3L-800	1N	Empty	Empty	Quad-rank
4	DDR3L-800	1N	Empty	Dual-rank	Single-rank
5	DDR3L-800	1N	Empty	Single-rank	Dual-rank
6	DDR3L-800	1N	Empty	Dual-rank	Single-rank
7	DDR3L-800	1N	Empty	Dual-rank	Dual-rank

Table 8. UDIMM Population Configurations (Intel® Xeon® Processor 5600 series only) for three slots per Channel

Configuration Number	POR Speed	1N or 2N	DIMM3	DIMM2	DIMM1
1	DDR3L-1066&800	1N	Empty	Empty	Single-rank
2	DDR3L-1066&800	1N	Empty	Empty	Dual-rank
3	DDR3L-800	1N	Empty	Single-rank	Single-rank
4	DDR3L-800	1N	Empty	Single-rank	Dual-rank
5	DDR3L-800	1N	Empty	Dual-rank	Single-rank
6	DDR3L-8000	1N	Empty	Dual-rank	Dual-rank

Channel Population Rules for Memory RAS Mode Configuration

Different RAS mode used comes with different rules on channel population. No matter what RAS mode it is, the requirements for populating within a channel should follow the RDIMM/UDIMM slots configurations in a channel at all times. RAS modes that demands matching DIMM population between channels (Sparing, Mirroring, Lockstep) require that ECC DIMMs be populated.
For RAS modes that require matching populations, the same slot positions across channels must hold the same DIMM type with regards to size and organization. DIMM timings do not have to match but timings will be lowered down due to slower timings.

The following modes are supported in the system.

- Independent Mode

Channels can be populated in any order in Independent Channel Mode--there are no matching requirements. All channels must run at the same interface frequency but individual channels may run at different DIMM timings (RAS latency, CAS latency, and so forth).

- Mirrored Channel Mode

  Three Channels under Mirrored Channel Mode, only Channel 0 and Channel 1 are used. The memory contents are mirrored between Channel 0 and 1. That means the total physical memory available to the server would appear as only half of what is populated. DIMMs populated in Channel 0 and Channel 1 must be identical with regards to size and organization. Within a channel, the DIMM slot population could be in any order, but the same DIMM slot location across Channel 0 and Channel 1 must be populated the same.

- Lockstep Channel Mode

  In Lockstep Channel Mode, each memory access is a 128-bit data access that spans Channel 0 and Channel 1. Lockstep Channel mode is the only RAS mode that supports x8 SDDC. Lockstep Channel Mode requires that Channel 0 and Channel 1 must be populated identically with regards to size and organization. DIMM slot populations within a channel do not have to be identical but the same DIMM slot location across Channel 0 and Channel 1 must be populated the same. Channel 2 is unused in Lockstep Channel Mode.

3.4 Graphics Controller

The system board implements the Pilot-II ServerEngines * ASIC and the Graphics controller features list as:

- Graphics Controller
- Integrated Graphics Core
- 2D Hardware Graphics Acceleration
- DDR2 memory interface supports up to 128 Mbytes of memory
- Supports all display resolutions up to 1600 x 1200 16 bpp at 75 Hz
- High speed Integrated 24-bit RAMDAC
- Single lane PCI-Express* host interface

3.5 IO Boards support

The system board supports one IO board. For more detailed information, refer to the IO board information in Chapter 6.

3.6 System Management

The system management sub-system is based on Pilot-II using for Baseboard Management Controller (BMC) for the motherboard. The system management is IPMI2.0 compliant. The Sever Management Controller (Pilot-II) facilitates the system management being accessible. .It is a highly integrated single-chip solution, integrating several devices typically found servers. Pilot-II is mainly targeted at next generation servers, and provides a highly integrated server class product. The following functionality is integrated into Pilot-II:

- Server Class Super I/O function
- Baseboard Management Controller
- Graphics Controller

4. Power Subsystem

The power sub-system is designed to configure one single 1100-W Power Supply (PS) module with an integrated Power Distribution Board.

This chapter provides technical details on the operation of the power supply module and power sub-system.

4.1 Power Supply Mechanical Overview

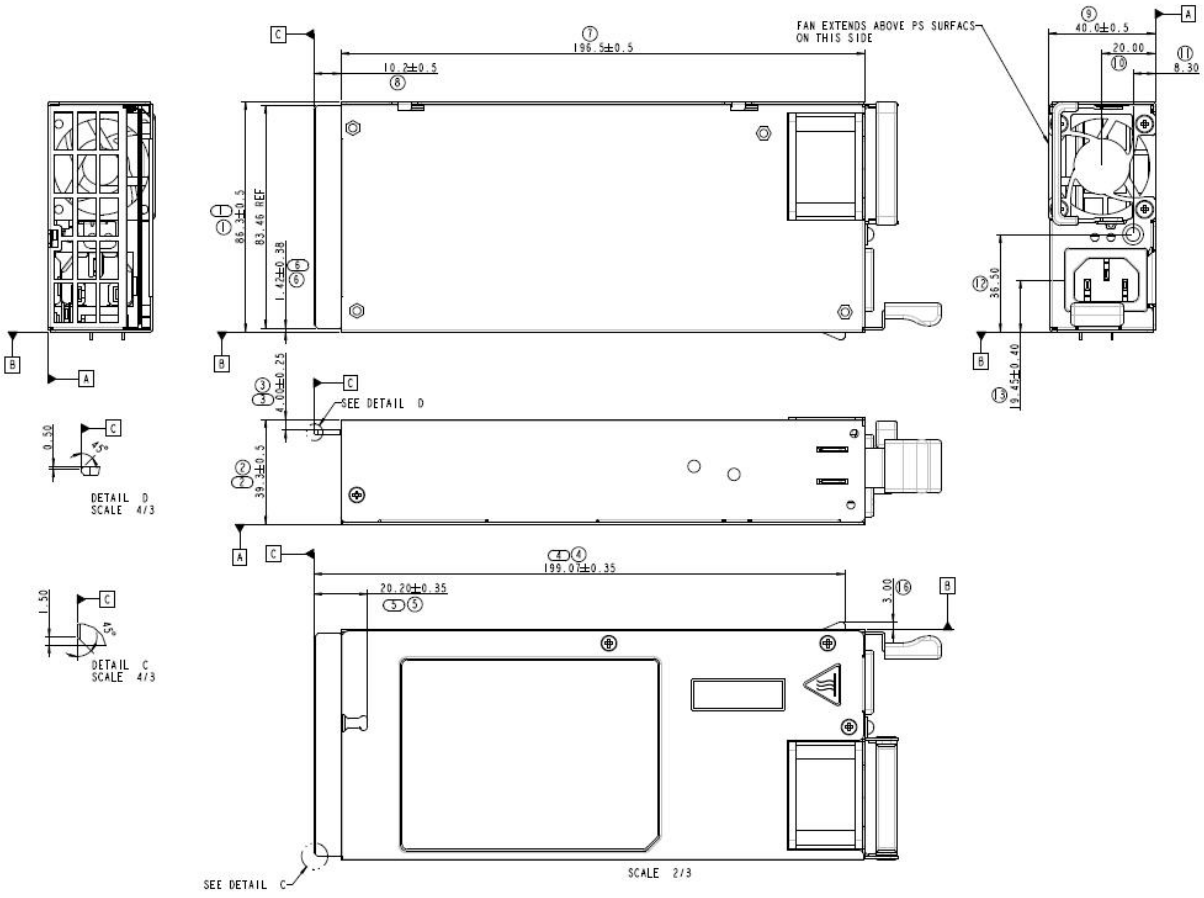


Figure 7. Power Supply Module Dimensional Drawing

4.1.1 Output Connection (Card Edge)

Output connector is card edge extension of PCB and blind mates with 32 positions each side (Tyco 1761469(vertical) and 1761468(right angle) or FCI pn 10046971-100LF (vertical) and 10053363-200LF (right angle)

Table 9 DC output Top Side connection

PCB Top Side			
Pin #	Signal Name	Amps/PinRating	Application Usage
53-64	+12V	5.5 A rms	90A / 24pins = 3.75A
41-52	RTN	5.5 A rms	90A / 24pins = 3.75A
40	Remote Sense +	5.5 A rms	<100mA
39	12v_SB	5.5 A rms	Standby = 2A rms
38	PS_A0	5.5 A rms	<100mA
37	POK	5.5 A rms	<100mA
36	Return	5.5 A rms	<100mA
35	SCL	5.5 A rms	Short Pin <100mA
34	-PS_Present	5.5 A rms	Short Pin <100mA
33	SDA	5.5 A rms	Short Pin <100mA

.Table 10 DC Output Connection (Card Edge)

PCB Bottom Side			
Pin #	Signal Name	Amps/PinRating	Application Usage
1-12	+12V	5.5 A rms	90A / 24pins = 3.75A
13-24	RTN	5.5 A rms	90A / 24pins = 3.75A
25	Tach	5.5 A rms	<100mA
26	Remote Sense -	5.5 A rms	<100mA
27	Vin_Good	5.5 A rms	See Exception #1 (<100mA)
28	Cshare	5.5 A rms	<100mA
29	-PS_On	5.5 A rms	<100mA
30	PS_Kill	5.5 A rms	(Short Pin)<100mA
31	**Reset**	5.5 A rms	(Short Pin)<100mA
32	Alert	5.5 A rms	(Short Pin)<100mA

4.2 Power system component and Connector Overview

A power distribution board (PDB) provides a connection between the power supply and two server boards. The PDB is shown below:

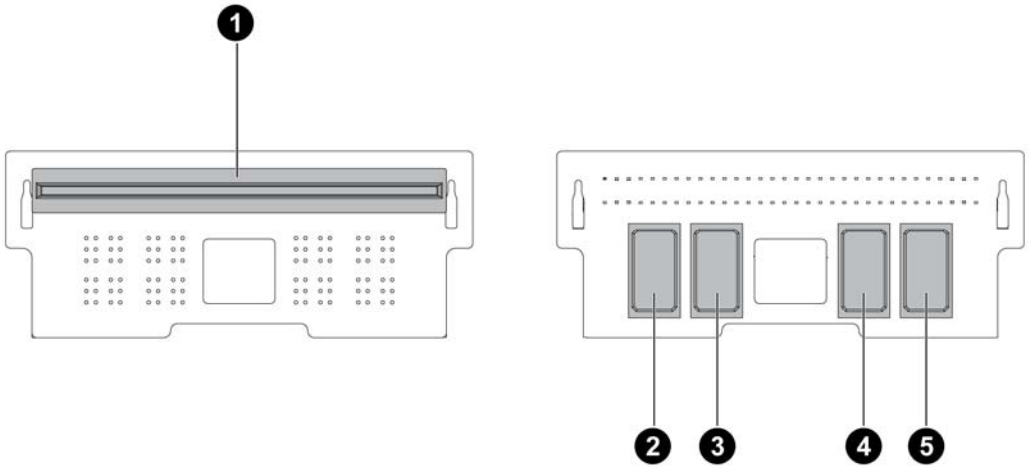


Figure 8. Power Distribution Board Connector

❶ Power Supply Slot	❹ Power Connector 3 (J3)
❷ Power Connector 1 (J5)	❺ Power Connector 4 (J2)
❸ Power Connector 2 (J4)	

4.2.1 Power Distribution Board Connector to Power supply (J1)

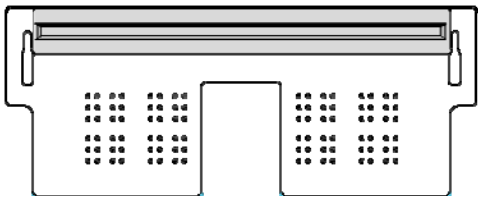


Figure 9. PDB Connector to Power Supply

Table 11. Pin Definition of PDB Connector to Power Supply

Signal Name	Pin	Pin	Signal Name
P12V	1	33	I2C_SDA_PS
P12V	2	34	PS_PRSNT_N
P12V	3	35	I2C_SCL_PS
P12V	4	36	Ground
P12V	5	37	PGD_PS

Signal Name	Pin	Pin	Signal Name
P12V	6	38	PS_ADD_A0
P12V	7	39	P12V_STBY
P12V	8	40	RMT_SNS_DP
P12V	9	41	Ground
P12V	10	42	Ground
P12V	11	43	Ground
P12V	12	44	Ground
Ground	13	45	Ground
Ground	14	46	Ground
Ground	15	47	Ground
Ground	16	48	Ground
Ground	17	49	Ground
Ground	18	50	Ground
Ground	19	51	Ground
Ground	20	52	Ground
Ground	21	53	P12V
Ground	22	54	P12V
Ground	23	55	P12V
Ground	24	56	P12V
FAN_TACH	25	57	P12V
RMT_SNS_DN	26	58	P12V
VIN_GOOD	27	59	P12V
PS_CSHARE	28	60	P12V
PS_ON_N	29	61	P12V
PS_KILL	30	62	P12V
RST_PS_N	31	63	P12V
I2C_ALERT_PS	32	64	P12V

4.2.2 Power Distrubution Board (PDB) Connectors to Sever board (J2, J3, J4, J5)

There are four connectors from the PDB to the server board. Connectors designated J2 and J4 share the same pin definition while J3 and J5 share the same pin definition.

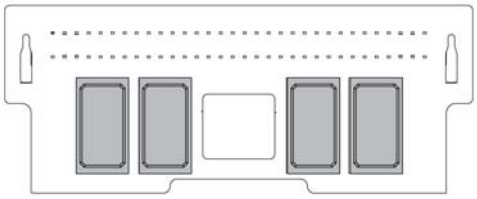


Figure 10. PDB Connectors to Server Board

Table 12. Pin Definition of PDB Connectors to Motherboard (J2, J4)

Signal Name	Pin	Pin	Signal Name
Ground	A1	B1	P12V
Ground	A2	B2	P12V

Table 13. Pin Definition of PDB Connectors to Mohterboard (J3, J5)

Signal Name	Pin	Pin	Signal Name
I2C_SDA_PS	A1	B1	2C_SCL_PS
Ground	A2	B2	P12V

4.2.3 Server Board Power Connectors

There are four power connectors on one server board and they have the same pin definition.

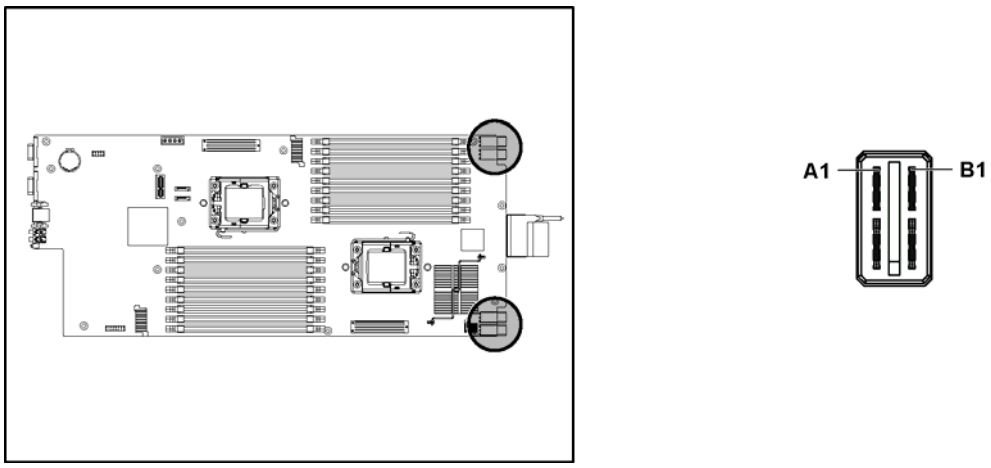


Figure 11. Server Board Power Connectors

Table 14. Pin Definition of Server Board Power Connectors (J2, J4)

Signal Name	Pin	Pin	Signal Name
Ground	A1	B1	P12V_PS
Ground	A2	B2	P12V_PS

Table 15. Pin Definition of Server Board Power Connectors (J3)

Signal Name	Pin	Pin	Signal Name
Ground	A1	B1	I2C_SCL_PS
Ground	A2	B2	P12V_PS

Table 16. Pin Definition of Server Board Power Connectors (J5)

Signal Name	Pin	Pin	Signal Name
Ground	A1	B1	NC
Ground	A2	B2	P12V_PS

4.3 AC Input Requirements

4.3.1 AC Input Voltage Range

Table 17. AC Input Voltage Specification

Parameter Description	Min	Typ	Max	Units	MFR Test 1
Vin (Voltage 1st Range)	90	115/230	264	Vrms	Yes
Vin (Voltage 2nd Range)	-	N/A		Vrms	x
Vin (frequency)	47	50/60	63	Hz	Yes
Iin (90VAC)	-	-	14.0	Arms	Yes
Iin(100VAC)	-	-	12.0	Arms	-
Iin (180VAC)	-	-	7.0	Arms	Yes
Vin (turn-on)	85	-	90	Vrms	Yes
Vin (turn-off)	80	-	85	Vrms	Yes
Max Input Power	-	-	1400	Watts	Yes

4.3.2 AC Power Cord Specification Requirements

The AC power cord used must meet the minimum specification requirements listed in the following table.

Table 18. AC Power Cord Specification

Cable Type	SVT
Wire Size	18 AWG
Temperature Rating	60ºC
Amperage Rating	10 A
Voltage Rating	125 V

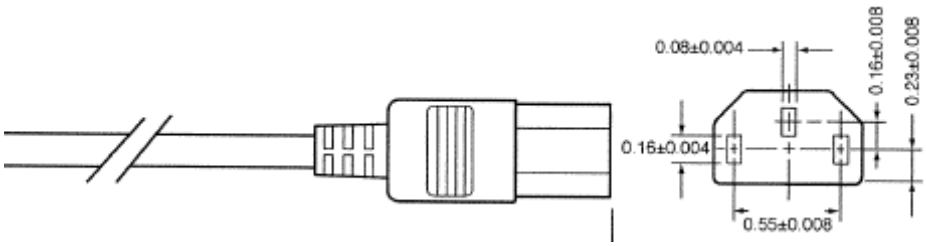


Figure 12. AC Power Cord

4.3.3 Efficiency

The power supply meets recommended efficiency levels at various conditions as discussed in the following table, tested over the full-specified AC input voltage range.

Table 19. Efficiency

115VAC Input Voltage	Minimum Efficiency (%)
20% Loading	87
50% Loading	90
100% Loading	87
230VAC Input Voltage	Minimum Efficiency (%)
10% Loading	80
20% Loading	88
50% Loading	92
100% Loading	88

4.3.4 AC Input Voltage Specification

The power supply must operate within all specified limits over the input voltage range shown in the following table.

Table 20. AC Input Rating

Parameter	Minimum	Rated	Maximum	Startup VAC	Power-off VAC	Maximum Input AC Current
Line Voltage (110)	90 V_{rms}	100-115 V_{rms}	140 V_{rms}	85VAC	80VAC	12 A_{rms} [1,3]
Line Voltage (220)	180 V_{rms}	200-230 V_{rms}	264 V_{rms}	90VAC	85VAC	7.0 A_{rms} [2,3]
Frequency	47 Hz	50/60 Hz	63 Hz	-	-	-

Notes:

1. Maximum input current at low input voltage range is measured at 90 VAC, at maximum load.
2. Maximum input current at high input voltage range is measured at 180 VAC, at maximum load.
3. This is not to be used for determining agency input current markings.
4. Maximum rated input current is measured at 100 VAC and 200 VAC.

Harmonic distortion of up to 10% of the rated AC input voltage must not cause the power supply to go out of specified limits. The power supply powers off on or after/below 75 VAC ± 5 VAC range. The power supply starts up on or before/above 85 VAC ± 4 VAC. Application of an input voltage below 85 VAC does not cause damage to the power supply or blow a fuse.

4.3.5 AC Line Dropout / Holdup

Table 21. AC Line Dropout / Holdup

Parameter Description	Min	Typ	Max	Units
AC Line Dropout	12	-	-	msec
Dropout Loading Conditions	-	100	-	%max output load
Hold-up Time Applicable Voltages	90	-	264	Vrms
Hold-up Time Duration	12	-	-	Msec

4.3.6 AC Line Leakage Current

The maximum leakage current to ground for each power supply is not more than 3.5 mA when tested at 254 VAC/60HZ.

4.3.7 AC Inrush

Table 22. AC In-rush

Parameter Description	Max	Units
Initial In-rush Current	55	Amps(peak)
Secondary In-rush Current	35	Amps(peak

4.3.8 Power Factor Correction

The power supply incorporates a Power Factor Correction circuit.
The power factor is 0.98 at 230VAC input voltages and >=90% load.

4.4 DC Output Specification

The following provides a summary of specifications for each individual output. These requirements apply under all conditions unless otherwise stated. Note that maximum continuous total output power should not 1024 W at Low Line and 100W at High line.

4.4.1 Output Power / Currents

The following table defines the power requirements for the power supply module.

Table 23. Power Supply Module Load Ratings

	1100 W		
Voltage	Minimum	Maximum	Peak
+12 V [2,4]	1 A	89.6 A (83.25,low	105A

	1100 W		
Voltage	Minimum	Maximum	Peak
		line)	
Standby [1,2,4]	0 A	2.00 A	2.7 A

Notes:

1. Peak standby current specification is only valid during the ramp up from 0V to the point where standby is within regulation. (250 mS)
2. Peak +12V output power not to exceed 100 mS seconds in duration. Maximum duty cycle is 5%.
3. +12V rail at loading conditions of 0 A to 1 A must comply with all +12V specification parameters except for load regulation.
4. Max current ratings based on a nominal 12.0 V main and standby rail with a remote sense voltage compensation of 0 V.

4.4.2 Output Voltage Regulation

The power supply output voltages must stay within the voltage limits defined in the following table when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise. All outputs are measured with reference to the return remote sense signal (ReturnS). The +12 V and +12 VSB voltages are measured at the PDB output harness connector.

Table 24. Voltage Regulation Limits

Output	Minimum	Normal	Maximum	Units
+ 12 V	+11.64	+12.00	+12.60	Volts
+ 12 VSB	+11.40	+12.00	+12.60	Volts

Note: Min and Max regulation limits represent absolute limits. Under normal operating conditions (static or dynamic), the +12V rail or standby exceeds these limits.

4.5 Protection Circuits

Protection circuits inside the PDB (and the power supply) shall cause only the power supply's main outputs to shutdown. The microprocessor and its I^2C communication bus is expected to continue operational. 12VSB output shall remain powered on if the failure does not involve this output. When a protection circuit shuts down the power supply, the green LED shall change to unlighted status and the PS OK signal shall be asserted LOW. If the power supply latches off due to a protection circuit tripping, AC input or PSON# signal toggle shall release latch condition and the power supply shall attempt to provide output power to the load. Minimum time delay for the toggle function shall be AC input OFF for 15sec, PSON# cycle HIGH for 1sec. Power to Micro controller circuitry associated with I^2C communication to the system shall be logic OR between internal source and system side 12 Vsb.

4.5.1 Over-current Protection (OCP)

Power supply provides limited output current to the load for protecting the power supply from damage under indefinite over load conditions. Table 25 describes output minimum and maximum current levels required from each output during an overload condition. 12 V over current protection is the current type. Over-current limit level is maintained for a period of 1 sec. minimum and 2 sec. maximum. After this time the power supply latches off. The latch is cleared

by toggling PSON# signal or by an AC input re-cycle. A sustained overload should not latch off 12SB output. Over current limit level shall be maintained for a period of 100 msec. minimum and 500 msec maximum for 12 VSB.

Table 25. Over Current Limits (Lout Limit)

Output Voltage	Min OCP Trip Limits	Max OCP Trip Limits
+12V	120%	150%
+12VSB	3.5A	5A

4.5.2 Over-voltage Protection (OVP)

Each DC/DC converter output on PDB has individual OVP protection circuits built-in and is locally sensed. The PS+PDB combo shuts down and latches off when an over-voltage condition occurs. This latch is cleared by toggling the PSON# signal or by an AC power interruption. Table 26 contains the over voltage limits. The values are measured at the PDB harness connectors. The voltage cannot exceed the maximum levels when measured at the power pins of the output harness connector during any single point of fail. The voltage cannot trip any lower than the minimum levels when measured at the power pins of the PDB connector.

Table 26. Over-voltage Limits

Output Voltage	OVP MIN	OVP MAX
+12V	13.6	15.0
+12VSB	13.6	15.0

4.5.3 Over-temperature Protection (OTP)

The power supply shall be protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature which could cause internal part/s failures. In an over temperature condition the PS shall shutdown. The Standby output shall not shut down during an OTP condition on the main outputs. When the temperature drops to within safe operating limit for internal parts, the power supply shall restore power automatically. The OTP circuit shall incorporate built-in hysteresis such that the power supply does not oscillate on and off due to temperature recovering condition. The power supply shall alert the system of the OTP condition through the power supply DC OK signal changing to a false state and the green LED changing to an unlighted condition. The OTP condition shall be stored in a register for troubleshooting purposes.

4.6 Power Supply LED

The power supply module has a single green LED to indicate power supply status. The LED light green indicates +12V is output, if the LED does not light, it indicates no AC on or no main power on. The LED is visible on the rear panel of the power supply module.

5. Cooling Subsystem

The chassis cooling system, designed in a 35 C maximum environment, consists of several components. These include one set of three system fans, air ducts, and one fan of power supply. Three key essential components shape out the complete and sound thermal solution provided for the chassis.

5.1 System Fan Module and Air Ducts

The system fan, three on each IO board, is a 40x40x56 mm non-hot-swappable module.

Three kinds of air ducts are built into the system and are designed to isolate and direct air flow to the main components. For which components these air ducts aid, refer to the zones of processor, DIMM, and HDDs. One is located on the IO board module; one is located between processor1 and according to DIMM group1. The third kind of air duct consists of blank DIMMs inserted in DIMM slots.

The air ducts intensify the air flow being emphasized on the fore-mentioned main zones in case the event of a single fan/motor occurs. The two sets of system fans would be boosted according the BMC's commands to provide sufficient cooling for the system and can hold for a while until the out-of-order fan/motor is replaced. However, acoustic noise will reach the maximum due to the highest speed operated on the remaining fans. The noise is also another reminder to you of a potentially harmful fan condition and instant component replacement.

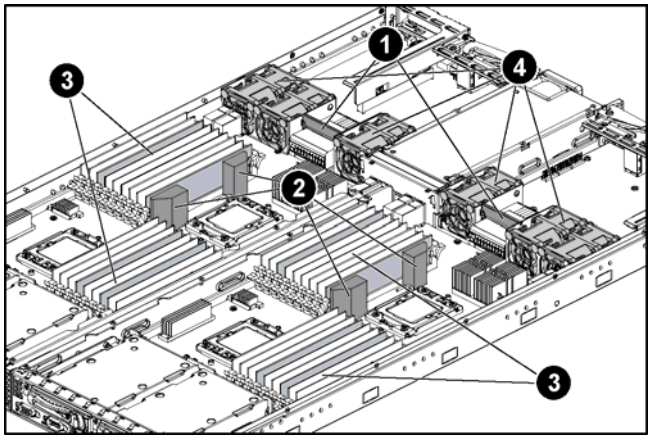


Figure 13. System Fans and Air Ducts

❶ IOB Air Duct	❸ DIMM Blank
❷ MLB Air Duct	❹ System Fans

There are temperature sensors designed to locate around selective main components on the motherboard to monitor crucial components and the ambient temperature for the system. The BMC generates information parameters detected by temperatures sensors and carries out adequate management over the thermal limits control. The most known parameter is the fan's RPM (revolutions per minute). The BMC adjusts the fan speeds to the RPM and, if the temperature exceeds the regulated thermal limits, the BMC sends out log errors to the System Event Log (SEL) in order to report the abnormality.

The third cooling solution is one 40x40x28 mm power fan inside the 1100-W single power supply module. This fan generates cooling air from the back and provides the power system ideal thermal condition. It acts to provide appropriate cooling to the power module and maintain the stability of system temperature within the specified range set by the BMC.

5.2 System Fan Connectors

System fan connectors on the two IO boards have different designators. Connectors on the left IO board are designated as J6, J7, and J8; while on the right IO board, they are J7, J8, and J9. Two J7 connectors share the same pin definition: J6 connector on left IO board and J8 connector on right IO board share the same pin definition; while the J8 connector on the left IO board and J9 connector on the right IO board share the same pin definition.

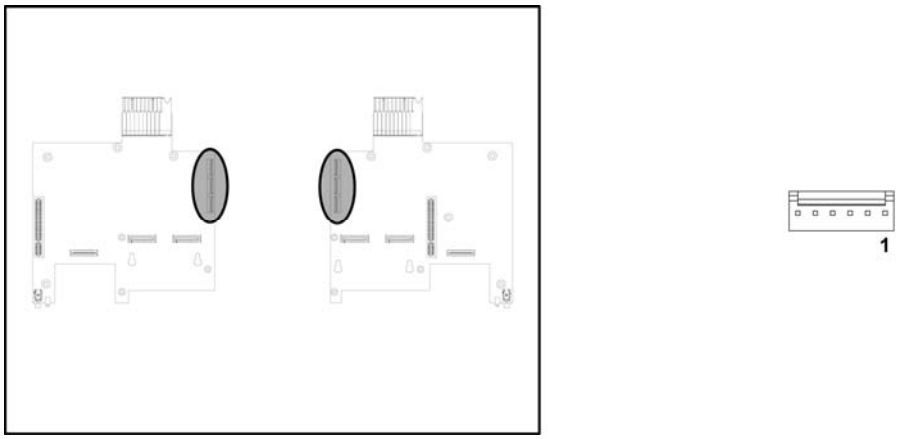


Figure 14. System Fan Connectors for IOB

Table 27. System Fan Connector Pin Definition (J7)

Pin	Signal Name
1	FAN_BMC_TACH0
2	FAN_BMC_PWM0_R
3	FAN_BMC_TACH3
4	P12V
5	Ground
6	P12V

Table 28. Fan Connectors Pin Definition (J6, J8 – J6 on Left IO Board / J8 on Right IO Board)

Pin	Signal Name
1	FAN_BMC_TACH2
2	FAN_BMC_PWM1_R
3	FAN_BMC_TACH5
4	P12V
5	Ground
6	P12V

Table 29. Fan Connectors Pin Definitions (J8, J9 – J8 on Left IO Board / J9 on Right IO Board)

Pin	Signal Name
1	FAN_BMC_TACH1
2	FAN_BMC_PWM0_R
3	FAN_BMC_TACH4
4	P12V
5	Ground
6	P12V

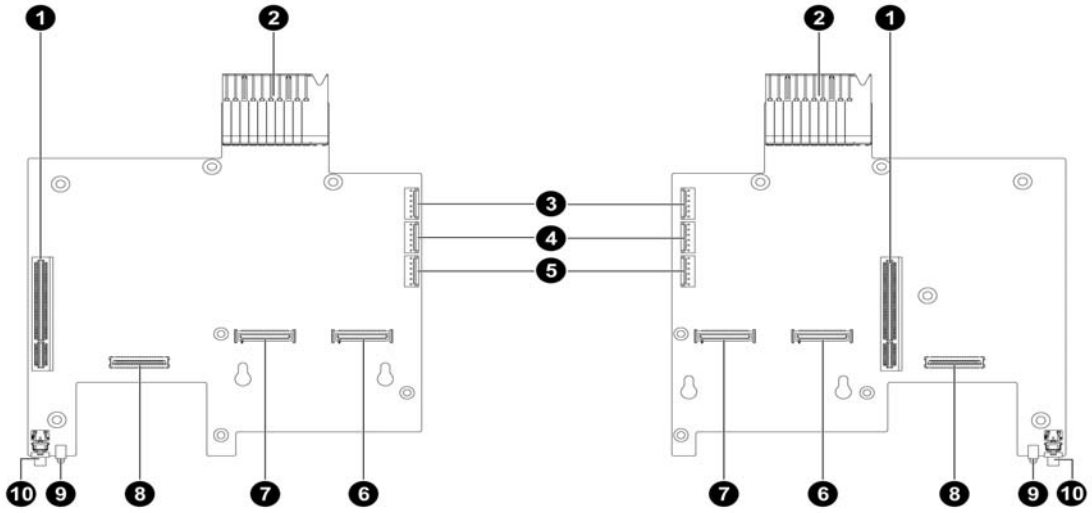
6. System Board Interconnects

System boards within the system include an IO board, hard drive backplane, and PCI riser board. This chapter describes the interconnect features of each and defines the pin-outs for each of their connectors. Later chapters describe the functional details of each system board.

6.1 IO Board

IO boards are designed to specify NIC functionality. The main IO functions are listed:

- Connection between motherboard and riser card
- Connection between motherboard and NIC board
- PCI-E connection
- Three system fans



Description	Location		Description	Location	
	Left	Right		Left	Right
❶ PCI-E X 8 Slots	J5	J5	❻ PCI-E 2 Connectors	J2	J2
❷ IO Board IO Connectors	J10	J10	❼ PCI-E 1 Connectors	J3	J3
❸ System Fan1 Connectors	J6	J7	❽ IO Board NIC Connectors	J4	J4
❹ System Fan2 Connectors	J8	J9	❾ Rear UID LEDs	CR6	CR6
❺ System Fan3 Connectors	J7	J8	❿ Rear UID Buttons	SW2	SW2

Figure 15. Connectors and Component Location of IO Board

6.1.1 IO Board IO Connectors

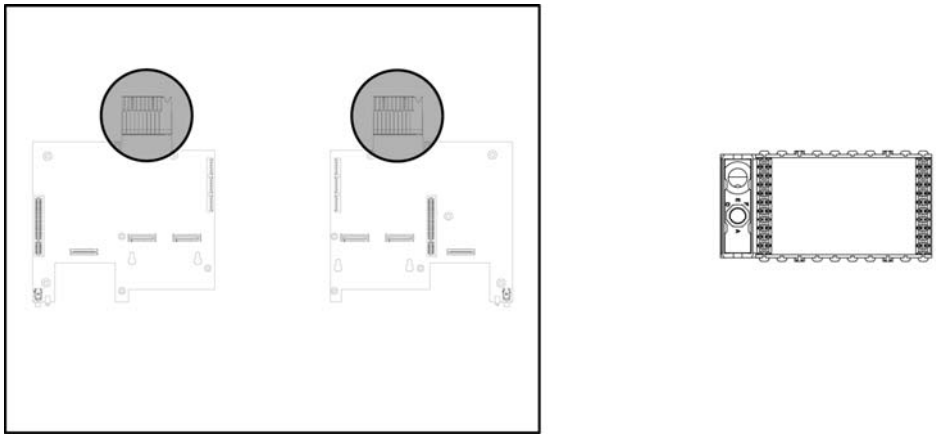


Figure 16. IO Boards IO Connectors

Table 30. Pin Definitions of IO Boards IO Connector

Signal Name	Pin	Pin	Signal Name
Ground	A1A	F1B	Ground
NCSI_TXD0	A2A	F2B	CLK_100M_PE_SLOT1_R_DN
NC	A3A	F3B	Ground
IO_PRSNT_N	A4A	F4B	Ground
PE_WAKE_N	A5A	F5B	Ground
NC	A6A	F6B	Ground
P12V	A7A	F7B	Ground
P12V	A8A	F8B	Ground
P12V	A9A	F9B	FAN_BMC_PWM1
P12V	A10A	F10B	Ground
Ground	A1B	G1A	NCSI_RXD1
PGD_P12V	A2B	G2A	CLK_100M_PE_SLOT2_R_DP
NC	A3B	G3A	PE10_IOH_TX_C_DN<2>
NIC0_DISABLE_N	A4B	G4A	PE10_IOH_RX_DN<0>
USB_OC01_N	A5B	G5A	PE9_IOH_TX_C_DN<1>
SYS_ID2	A6B	G6A	PE8_IOH_TX_C_DN<3>
NC	A7B	G7A	PE8_IOH_RX_DN<3>
P12V	A8B	G8A	PE7_IOH_TX_C_DP<1>
P12V	A9B	G9A	Ground
P3V3_STBY	A10B	G10A	PE3_IOH_TX_C_DP<0>
NC	B1A	G1B	NCSI_TX_EN
Ground	B2A	G2B	CLK_100M_PE_SLOT2_R_DN
BTN_UID_N	B3A	G3B	PE10_IOH_TX_C_DP<2>
LAN_DEV_OFF_N	B4A	G4B	PE10_IOH_RX_DP<0>
SYS_ID3	B5A	G5B	PE9_IOH_TX_C_DP<1>
LED_LINK_ACT_N	B6A	G6B	PE8_IOH_TX_C_DP<3>

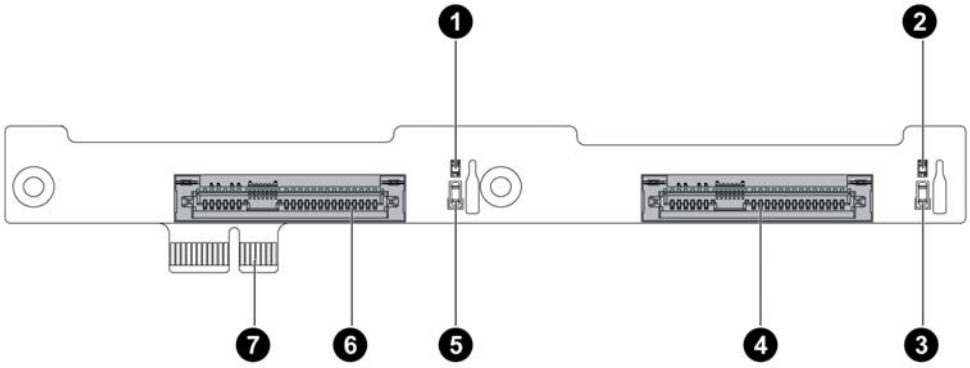
Signal Name	Pin	Pin	Signal Name
NC	B7A	G7B	PE7_IOH_RX_DP<3>
P12V	B8A	G8B	PE7_IOH_TX_C_DN<1>
FAN_BMC_TACH1	B9A	G9B	Ground
P3V3_STBY	B10A	G10B	PE3_IOH_TX_C_DN<0>
NC	B1B	H1A	Ground
Ground	B2B	H2A	Ground
NIC1_DISABLE_N	B3B	H3A	PE10_IOH_RX_DN<3>
PGD_SYS_BUFFER	B4B	H4A	PE9_IOH_RX_DP<3>
PGD_IO	B5B	H5A	PE8_IOH_RX_DP<3>
P12V	B6B	H6A	PE8_IOH_RX_DP<2>
P12V	B7B	H7A	PE8_IOH_RX_DP<1>
P12V	B8B	H8A	PE7_IOH_TX_C_DP<0>
FAN_BMC_TACH5	B9B	H9A	PE3_IOH_RX_DN<3>
P3V3_STBY	B10B	H10A	PE3_IOH_RX_DP<2>
NC	C1A	H1B	Ground
NCSI_CRS_DV	C2A	H2B	Ground
Ground	C3A	H3B	PE10_IOH_RX_DP<3>
Ground	C4A	H4B	PE9_IOH_RX_DN<3>
Ground	C5A	H5B	PE8_IOH_RX_DN<3>
SYS_ID4	C6A	H6B	PE8_IOH_RX_DN<2>
I2C_SDA_NIC	C7A	H7B	PE8_IOH_RX_DN<1>
Ground	C8A	H8B	PE7_IOH_TX_C_DN<0>
FAN_BMC_TACH4	C9A	H9B	PE3_IOH_RX_DP<3>
P12V	C10A	H10B	PE3_IOH_RX_DN<2>
NC	C1B	J1A	MAC_REFCLK_B
NC	C2B	J2A	NC
Ground	C3B	J3A	Ground
LED_UID_BUF_N	C4B	J4A	Ground
NC	C5B	J5A	Ground
NC	C6B	J6A	Ground
I2C_SCL_NIC	C7B	J7A	Ground
Ground	C8B	J8A	Ground
FAN_BMC_TACH0	C9B	J9A	Ground
P12V	C10B	J10A	Ground
Ground	D1A	J1B	MAC_REFCLK_A
NC	D2A	J2B	NC
PE10_IOH_TX_C_DN<1>	D3A	J3B	Ground
RST_PCIE_SLOT_N	D4A	J4B	Ground
SYS_ID1	D5A	J5B	Ground
Ground	D6A	J6B	Ground
Ground	D7A	J7B	Ground
PE7_IOH_RX_DP<0>	D8A	J8B	Ground
Ground	D9A	J9B	Ground
Ground	D10A	J10B	Ground
Ground	D1B	K1A	Ground
NC	D2B	K2A	Ground
PE10_IOH_TX_C_DP<1>	D3B	K3A	PE10_IOH_RX_DP<2>
Ground	D4B	K4A	PE9_IOH_TX_C_DP<2>

Signal Name	Pin	Pin	Signal Name
SYS_ID0	D5B	K5A	PE9_IOH_RX_DP<1>
Ground	D6B	K6A	PE8_IOH_TX_C_DP<1>
Ground	D7B	K7A	PE8_IOH_RX_DN<0>
PE7_IOH_RX_DN<0>	D8B	K8A	PE7_IOH_RX_DP<2>
Ground	D9B	K9A	PE3_IOH_TX_C_DP<1>
Ground	D10B	K10A	PE3_IOH_RX_DN<0>
NCSI_TXD1	E1A	K1B	Ground
Ground	E2A	K2B	Ground
PE10_IOH_TX_C_DN<3>	E3A	K3B	PE10_IOH_RX_DN<2>
PE10_IOH_TX_C_DN<0>	E4A	K4B	PE9_IOH_TX_C_DN<2>
PE9_IOH_RX_DP<2>	E5A	K5B	PE9_IOH_RX_DN<1>
PE9_IOH_TX_C_DN<0>	E6A	K6B	PE8_IOH_TX_C_DN<1>
PE8_IOH_TX_C_DP<0>	E7A	K7B	PE8_IOH_RX_DP<0>
PE7_IOH_TX_C_DN<2>	E8A	K8B	PE7_IOH_RX_DN<2>
FAN_BMC_TACH3	E9A	K9B	PE3_IOH_TX_C_DN<1>
PE3_IOH_TX_C_DP<3>	E10A	K10B	PE3_IOH_RX_DP<0>
NCSI_RXD0	E1B	L1A	CLK_100M_NIC0_R_DP
Ground	E2B	L2A	NC
PE10_IOH_TX_C_DP<3>	E3B	L3A	PE10_IOH_RX_DN<1>
PE10_IOH_TX_C_DP<0>	E4B	L4A	PE9_IOH_TX_C_DN<3>
PE9_IOH_RX_DN<2>	E5B	L5A	PE9_IOH_RX_DP<0>
PE9_IOH_TX_C_DP<0>	E6B	L6A	PE8_IOH_TX_C_DN<2>
PE8_IOH_TX_C_DN<0>	E7B	L7A	PE7_IOH_TX_C_DP<3>
PE7_IOH_TX_C_DP<2>	E8B	L8A	PE7_IOH_RX_DP<1>
FAN_BMC_TACH2	E9B	L9A	PE3_IOH_TX_C_DP<2>
PE3_IOH_TX_C_DN<3>	E10B	L10A	PE3_IOH_RX_DN<1>
Ground	F1A	L1B	CLK_100M_NIC0_R_DN
CLK_100M_PE_SLOT1_R_DP	F2A	L2B	NC
Ground	F3A	L3B	PE10_IOH_RX_DP<1>
Ground	F4A	L4B	PE9_IOH_TX_C_DP<3>
Ground	F5A	L5B	PE9_IOH_RX_DN<0>
Ground	F6A	L6B	PE8_IOH_TX_C_DP<2>
Ground	F7A	L7B	PE7_IOH_TX_C_DN<3>
Ground	F8A	L8B	PE7_IOH_RX_DN<1>
FAN_BMC_PWN0	F9A	L9B	PE3_IOH_TX_C_DN<2>
Ground	F10A	L10B	PE3_IOH_RX_DP<1>

6.2 Hard Drivers Backplane

Each server board has one backplane to support up to two 2.5-inch pluggable HDDs. The design incorporates a hot-swappable feature to allow for easy replacement of HDDs. The backplane features list as:

- Connection between server board and backplane
- Connection between backplane and 2.5-inch pluggable HDDs
- Functionality of the HDD LED activity



❶ HDD 0 Fail LED (CR4)	❺ HDD 0 Active LED (CR3)
❷ HDD 1 Fail LED (CR2)	❻ SATA 0 HDD Connector
❸ HDD 1 Active LED (CR1)	❼ Golden Fingers
❹ SATA 1 Connector	

Figure 17. Connectors and Component Locations of 2.5-inch SATA HDD Backplane

6.2.1 HDD Backplane SATA Connectors (J2, J3)

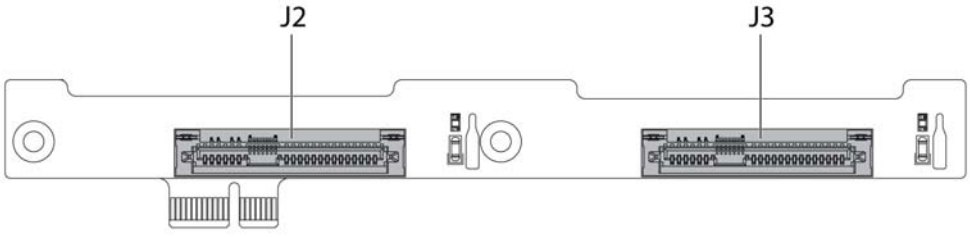


Figure 18. HDD Backplane SATA Connectors

Table 31. Pin Definition of HDD Backplane SATA Connector (J2)

Signal Name	Pin	Pin	Signal Name
Ground	S1	P3	NC
SATA_TX0_C_DP	S2	P4	Ground
SATA_TX0_C_DN	S3	P5	HDD_PRNT_N<0>
Ground	S4	P6	Ground
SATA_RX0_C_DN	S5	P7	P5V
SATA_RX0_C_DP	S6	P8	P5V
Ground	S7	P9	P5V
Ground	S8	P10	Ground
NC	S9	P11	HDD_ACT_N<0>
NC	S10	P12	Ground
Ground	S11	P13	P12V
NC	S12	P14	P12V
NC	S13	P15	P12V
Ground	S14	P16	Ground
NC	P1	P17	Ground
NC	P2		

Table 32. Pin Definition of HDD Backplane SATA Connector (J3)

Signal Name	Pin	Pin	Signal Name
Ground	S1	P3	NC
SATA_TX1_C_DP	S2	P4	Ground
SATA_TX1_C_DN	S3	P5	HDD_PRNT_N<1>
Ground	S4	P6	Ground
SATA_RX1_C_DN	S5	P7	P5V
SATA_RX1_C_DP	S6	P8	P5V
Ground	S7	P9	P5V
Ground	S8	P10	Ground
NC	S9	P11	HDD_ACT_N<1>
NC	S10	P12	Ground
Ground	S11	P13	P12V
NC	S12	P14	P12V
NC	S13	P15	P12V
Ground	S14	P16	Ground
NC	P1	P17	Ground
NC	P2		

7. Hard Disk Drive Support

The system is designed with two types of HDDs. One SATA HDD backplane supports two 2.5-inch pluggable HDDs, and up to four 2.5-inch pluggable HDDs can be installed in the server.

7.1 Hard Drive Bays

The system can be configured to support up to four hot-swap 2.5 inch SATA hard disk drives. The hard drives are mounted to hot-swap drive trays for easy insertion or extraction from the drive bay.

7.1.1 Hot-swap Drive Trays

Each hard drive must be mounted to a hot-swap drive tray and each drive tray has its own dual-purpose latching mechanism used to insert and extract drives from the system, and lock the tray assembly in place. Each drive tray supports two light pipes viewable from the front of the system. The light pipes provide a green drive activity indicator and amber drive fault indicator. The drive activity and fault LEDs are located on the backplane next to each drive connector.

7.1.2 Hard Driver Activity and Fault LEDs

The backplanes support an activity and fault LED for each of the hard drive connectors. The LED illuminates blue for activity and red for a drive fault.

Table 33. Hard Drive LED Function Definitions

Type of LED	Status LED	Definition
Activity LED	Blue	Blinking: HDD accessing
		Off: No HDD accessing
Fault LED	Red	On: Error detected or RAID failed
		Blinking: RAID rebuilt

8. System LED, Button and Jumper Functionality

8.1 Front Panel LED and Button information

The front panel LED information displays details regarding the NIC LED, system health LED, power LED, and UID LED of the server.

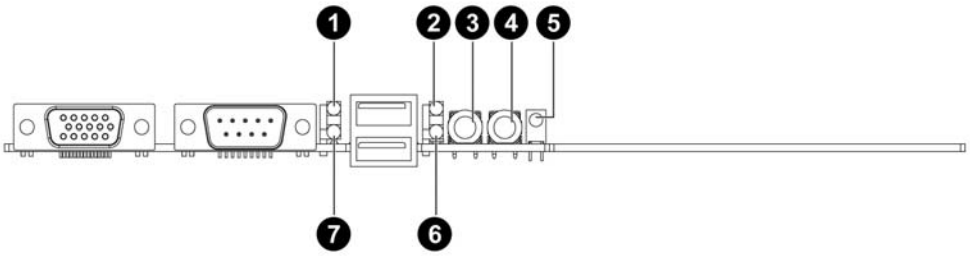


Figure 19. Front Panel LEDs and Buttons

❶ NIC LED	❺ UID LED
❷ System Health LED	❻ Power LED
❸ Power Button	❼ SATA LED
❹ UID Button	

Table 34. Front Panel LEDs information

Type of LED	Color	Status
Power LED	Amber	On: System has AC power but in standby mode
	Green	On: System has AC power and is turned on
	-	Off: No AC power to the system
System Health LED	Red	Blinking: System has non-critical errors. After error condition is cleared, LED is off.
		On: System has critical errors. LED needs to remain active until the next power-off and power-on provided that the error condition is cleared.
	-	Off: System off / System OK
HDD Activity LED	Green	Blinking: Drive activity
	-	Off: No drive activity
NIC 1&2 LED	Green	Blinking: LAN activity on the network
		On:: Linked to network
	-	Off: LAN not connected
UID LED	Blue	Blinking : System is being managed by IPMI command
		On: Identification
	-	Off: Disabled

8.2 Rear Panel LED information

LED information of rear panel2 displays details regarding the NIC LEDs and UID LED of the server. Each NIC port contains two LEDs that show the status of network activity, link, or speed.

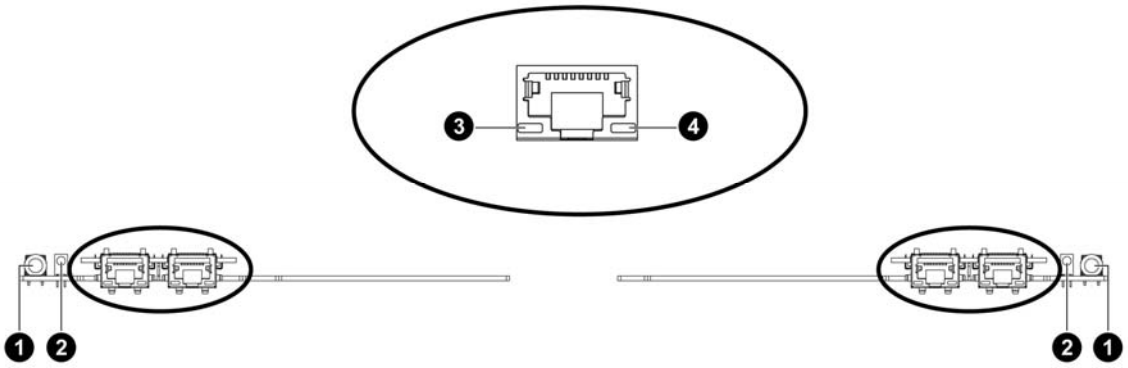


Figure 20. Rear Panel LEDs

❶ Rear UID Button	❸ NIC 1&2 Activity LED
❷ Rear UID LEDs	❹ NIC 1&2 Link LED

Table 35. Rear LED information

Type of LED	Color	Status
NIC 1&2 Activity LED	Green	Blinking: Activity on the network
	-	Off: No connection
NIC 1&2 Link LED	Green	On: Linked to the network
	-	Off: No connection
UID LED	Blue	Blinking: System is being remotely managed
		On: Identification
	-	Off: Disabled
AC Power LED		
AC Power LED	Green	On: +12V is output
	-	Off: No AC on or no main power on

8.3 System Confirguration Jumpers

The server board involves two system maintenance jumpers. One is MISC jumper, one is a functions jumper. Two jumpers are divided into five pin groups. The location of the two system maintenance jumpers on the server board are shown in Figure 21 and Figure 22:

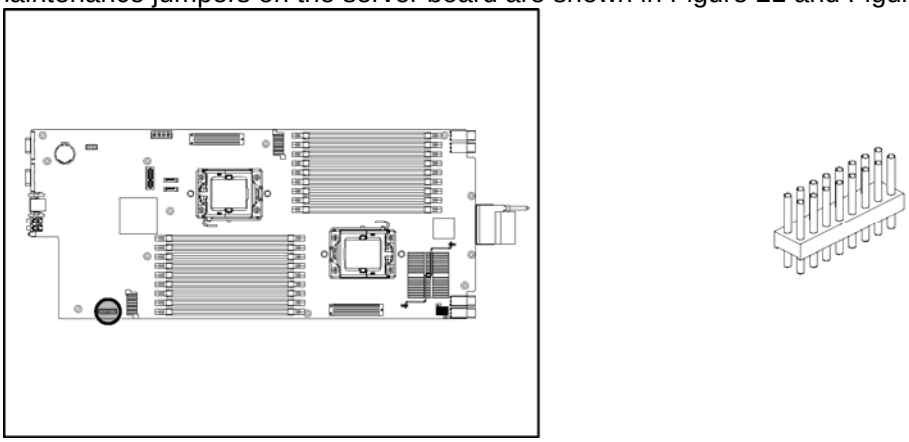


Figure 21. Location of MISC Jumper

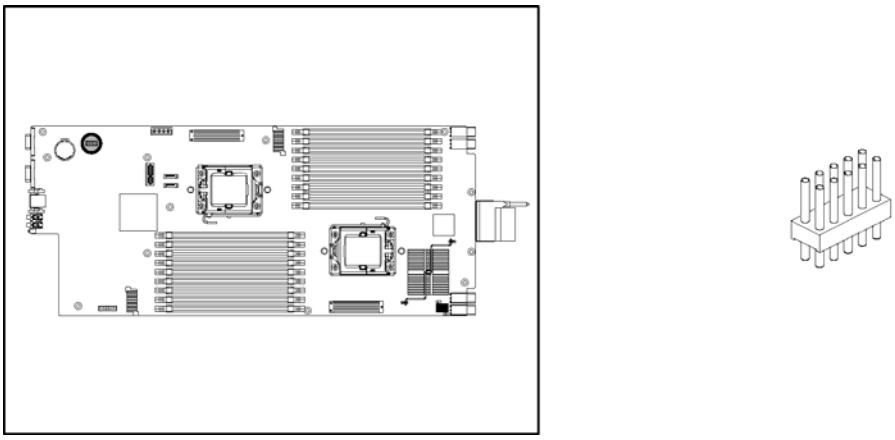


Figure 22. Location of Function Jumper

The functions of the two system configuration jumpers are shown in the following table.

Table 36. Function of MISC Jumper

Jumper	Function
A	Reserved
B	Clear BMC Password
C	Reserved
D	Reserved
E	Reserved

Jumper	Function
F	Reserved
G	Reserved
H	Reserved

Table 37. Function of Functions Jumper

Jumper	Function
A	Clear CMOS
B	Clear Password
C	Recovery FWH
D	BIOS Protect
E	RTC Reset

8.4 MISC Jumper (J48)

The MISC jumper on motherboard is designed for MISC protection, override, and debugging. It includes four function pin groups, Clear BMC password, manufacturing detect, CUP DDR3 low voltage enable, and four reserved pins for future use—they are all 2 x 8.

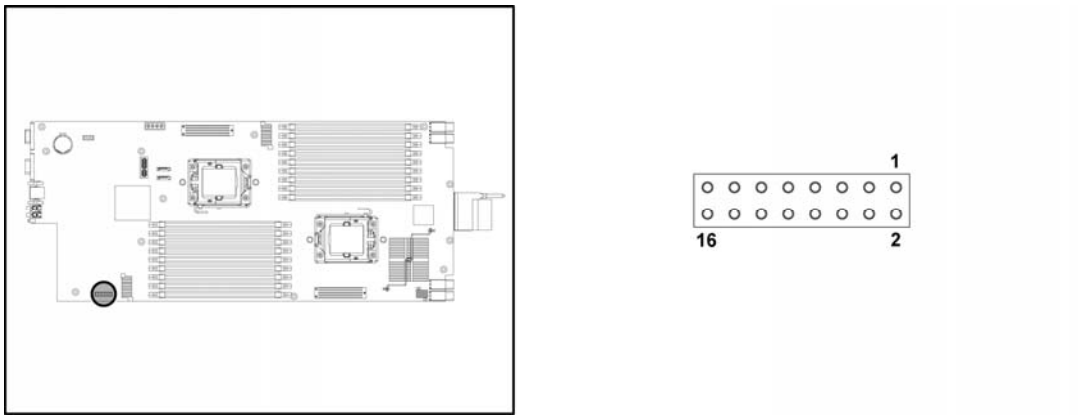


Figure 23. MISC Jumper

Table 38. Pin Definition of MISC Jumper (J48)

Signal Name	Pin	Pin	Signal Name
Ground	1	2	Ground
Ground	3	4	Ground
Ground	5	6	Ground
Ground	7	8	Ground
MANUFACTURING_DEN_N	9	10	SET_CLR_PASSWD_BMC_N

Signal Name	Pin	Pin	Signal Name
CPU0_LV_DDR3_EN_N	11	12	CPU1_LV_DDR3_EN_N
BTN_FP_RST_N	13	14	CPLD_R6
CPLD_R8	15	16	CPLD_R10

8.5 ICH Functions Jumper (J30)

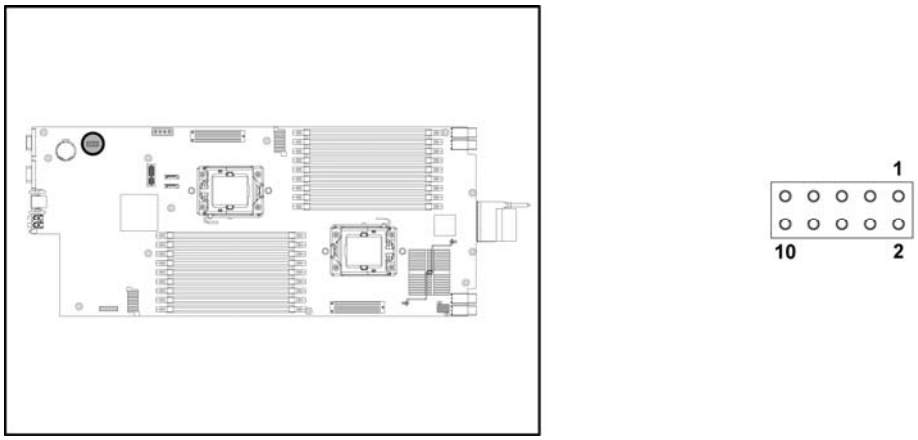


Figure 24. Functions Jumpers

Table 39. Pin Definition of Functions Jumper

Signal Name	Pin	Pin	Signal Name
Ground	1	2	SET_CLR_CMOS_BUF_N
Ground	3	4	SET_CLR_PASSWD_BUF_N
Ground	5	6	SET_RCVRY_BUF_N
Ground	7	8	BIOS_PROTECT_N
Ground	9	10	ICH_RTCRST_N

9. IO Board extended Assembly

The Intel® Server System SR1680MV IO Board provides the following optional I/O function.

9.1 Riser Card

The IO board supports a low-profile PCI-E expansion card. The slot can support a PCI-E x8, x1, x4, or x8 card. The PCI-E slots are supposed to support 25 W maximum.

The LP PCI-E riser card is shown:

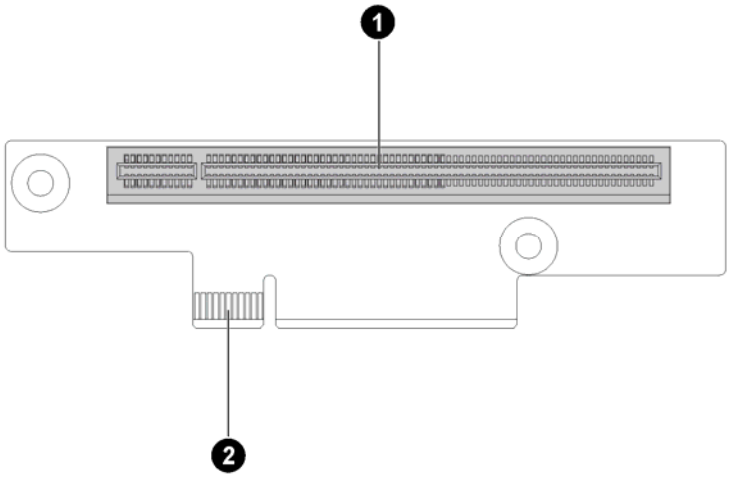


Figure 25. PCI Riser Card

1	PCI-E x16 Slot
2	Golden Fingers

9.2 NIC Board

The IO boards support a NIC board with two RJ-45 controlled by 82576 on each IO Board. The back network port with LEDs are connected to Vaux (standby) voltage in order to provide the same functionality as stand-up NIC cards for WOL (Wake-on LAN) support.

The NIC board is shown below:

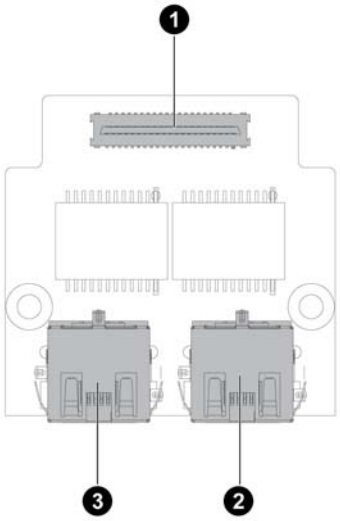


Figure 26. Connectors and Component Locations of NIC Board

❶ Connector	❸ Rear NIC1 Port
❷ Rear NIC2 Port	

9.3 Daughter Cards (Optional)

IO boards support two kinds of daughter cards. The following sections separately give details on their configuration.

9.3.1 10 GB IO Card

The 10 GB IO card is shown:

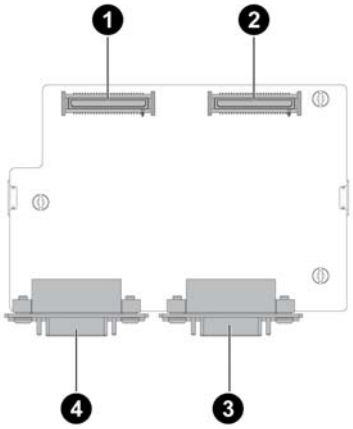


Figure 27. Connectors and Component Locations of 10 GB IO Card

❶ PCI-E 2 Connector	❸ 10 GB IO Port1
❷ PCI-E 1 Connector	❹ 10G B IO Port2

9.3.2 InfiniBand Card

The InfiniBand card is shown:

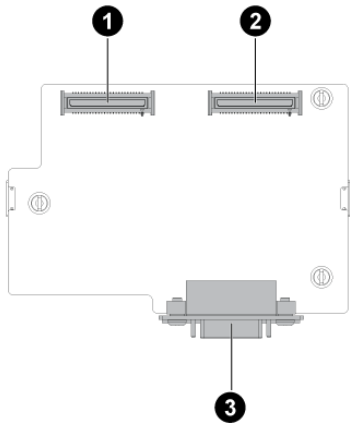


Figure 28. Connectors and Component Locations of InfiniBand Card

❶ PCI-E 2 Connector	❸ InfiniBand X4 Port
❷ PCI-E 1 Connector	

10. Basic Input/Output System (BIOS)

10.1 BIOS Architecture

This chapter includes the introduction of many BIOS features provided by the system and provides detailed descriptions of POST errors, POST codes, and beep codes. Note that such information may help you diagnosis the system when it does not function properly.

10.2 BIOS Feature

The system BIOS includes the following features:

- PC/AT Compatible System ROM
- ACPI 3.0, Compliance/Support, S0, S5 support
- Wake-up On LAN/RTC
- SMBIOS 2.5
- Support PXE 2.1 function of onboard NIC
- Plug and Play (PnP) BIOS specific 1.0a
- BBS 1.01
- System Bus Support
- PCI 3.0
- PCI-PCI Bridge
- PCI 64-bit
- Native 64bit MMIO Support
- Peer PCI bus
- Full bus master capability
- PCI Express* (PCIe) 2.0
- USB Support
- Keyboard, mouse, hub, and Storage
- Low-, Full-, and High-Speed
- UHCI (USB 1.1)
- EHCI (USB 2.0)
- Boot from Mass Storage Devices, HD/CD-ROM/DVD-ROM/Disk-on-key support

- Legacy USB Keyboard/Mouse
- SATA, CD-ROM/DVD-ROM boot
- Boot Block Recovery mode
- Jumper
- Ctrl+Home control function key
- Error Handling Support
- Log CPU-related error
- Log System-related error
- ECC Error Correction & Logging
- Memory re-mapping above 4GB
- POST Memory Manager(PMM 3.0)
- Disable onboard PCI devices(2*NIC) by Hardware configuration
- POST Support
- Fast POST(Quick Boot)
- Error Management
- Pause with Warning Message
- Quiet Boot
- MS SLP 1.0/2.0 (System-Locked Pre-installation)
- Support IPMI 2.0
- Advanced CPU Support
- Multi-Processor
- Multi-Core Processing
- Intel® Speed SpeedStep™ Technology
- Intel® CPU Hyperthreading/Quad Cores, Extended Memory 64 Technology (EM64T),Virtualization Technology(VT)
- Intel Machine Check Architecture (MCA)
- Console Redirection via Serial Port (POST & Setup)
- Resume system into previous state when AC Power back

- Restore on AC Power Loss
- Security
- Multi-Level Password Protection
- Password on boot or Setup Menu
- TPM Security
- BIOS update in DOS environment
- Headless Operation for rack servers
- MPS 1.4
- RAID System on board
- SATA 2.0
- Drive Auto-Detection & Configuration
- Flash ROM protected

10.3 BIOS POST (Power On Self Test) Code

Table 40. POST Code Information

Checkpoint	Description
03	Disables NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, and Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Checks CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update the CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Sets up boot strap processor Information
C2	Sets up boot strap processor for POST
C5	Enumerates and sets up application processors
C6	Re-enables cache for boot strap processor

Checkpoint	Description
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompresses and initializes any platform specific BIOS modules.
30	Initializes System Management Interrupt.
2A	Initializes different devices through DIM.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that has optional ROMs.
2E	Initializes all the output devices.
31	Allocates memory for ADM module and uncompresses it. Gives control to ADM module for initialization. Initializes language and font modules for ADM. Activates ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM.
39	Initializes DMAC-1 & DMAC-2.
3A	Initializes RTC date/time.
3B	Test for total memory installed in the system. Also, checks for F1 or ESC keys to limit memory test. Displays total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detects different devices (Parallel ports, serial ports, and coprocessor in CPU, and so forth) successfully installed in the system and update the BDA, EBDA, and so forth.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generates and writes contents of ESCD in NVRam.
84	Logs errors encountered during POST.
85	Displays errors to the user and gets the user response for error.
87	Executes the BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8D	Builds ACPI tables (if ACPI is supported)
8E	Programs the peripheral parameters. Enables/Disables NMI as selected
90	Late POST initialization of system management interrupt.
A0	Checks boot password if installed.
A1	Cleans-up work needed before booting to operating system.
A2	Takes care of runtime image preparation for different BIOS modules. Fills the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime

Checkpoint	Description
	language module. Disables the system configuration display if needed.
A4	Initializes runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRRs.
A8	Prepares CPU for operating system boot including final MTRR values.
A9	Waits for user input at configuration display if needed.
AA	Uninstalls POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepares BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Saves system context for ACPI.
00	Passes control to OS Loader (typically INT19h).

10.4 Beep Codes

When the server fails its POST, the beep codes are often the only clue to determine what is wrong. To decode the meaning of POST beep codes, the following table gives detailed descriptions you can consult when trying to solve problems.

Table 41. Beep Code Information

Number of Beeps	Description
1	Memory refreshes timer error.
2	Parity error
3	Main memory read / write test error.
4	Motherboard timer not operational
5	Processor error
6	Keyboard controller BAT test error.
7	General exception error.
8	Display memory error.
9	ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory bad

11. System Management

The system management sub-system is based on Pilot-II using for Baseboard Management Controller (BMC) for the motherboard. The system management is IPMI2.0 compliant.

For sub-sections, the following sections will highlight more detailed features of system management.

11.1 System Block Diagram

The following diagram is an overview of the system management architecture used on the server board. The diagram shows how the chip interacts and links to each other.

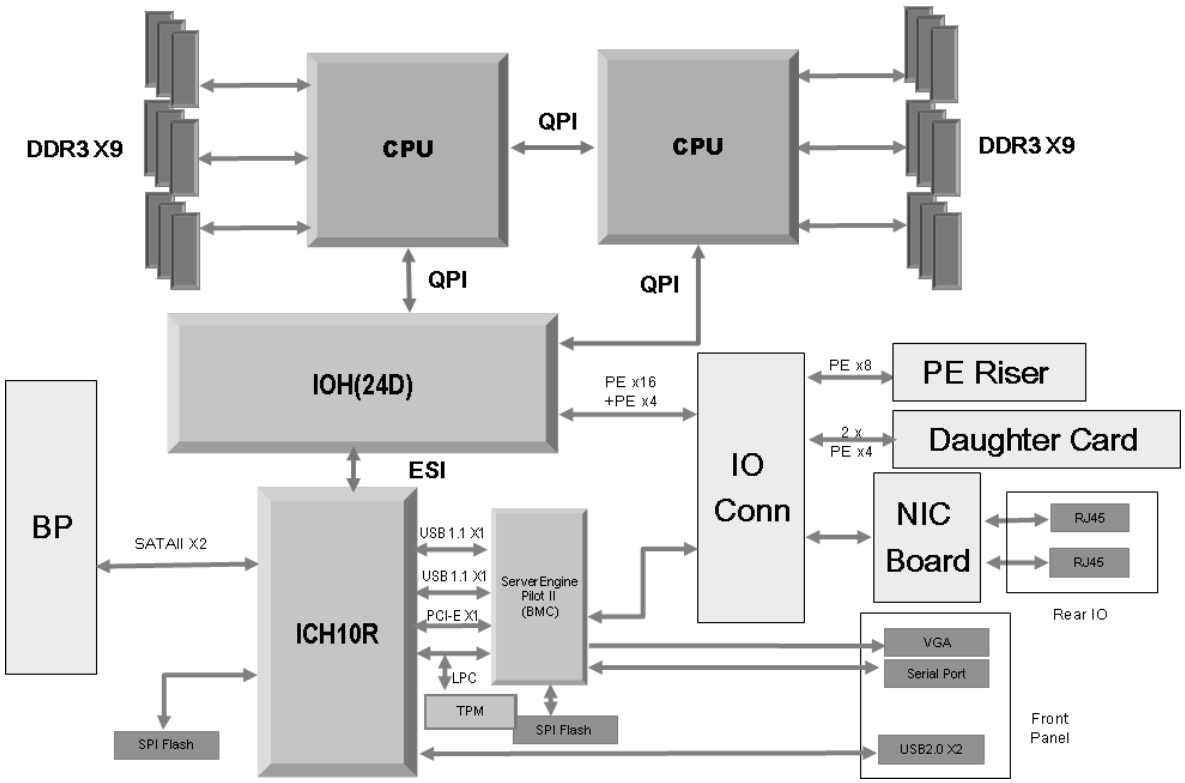


Figure 29. System Block Diagram

The Sever Management Controller (Pilot-II) allows the system management to be accessible. .It is a highly integrated single-chip solution, integrating several devices typically found in servers. Pilot-II is mainly targeted at next generation servers, and provides a highly integrated server class product. The following functionality is integrated into Pilot-II:

- Server Class Super I/O function
- Baseboard Management Controller
- Graphics Controller

11.2 Serial-Over LAN

Serial-over-LAN provides a mechanism that enables the serial controller of a managed system to be redirected over an IPMI session over IP. This enables remote console applications to provide access to text-based interfaces for the BIOS, utilities, operating systems, and applications while simultaneously providing access to IPMI platform management functions.

11.3 KVM Over IP

Remote KVM provides greater control over hardware, including access to power controls and monitoring functions through the BMC. Remote KVM solutions provide more direct access to out-of-band system performance data and efficient integration with system-level monitoring information.

Table 42. KVM Features

VNC	RFB protocol v3.8
Encoding Type	ZRLE, Hextile
Higher Resolutions	1024*768, 16bpp; 1280*1280, 8bpp

11.4 Virtual Storage

The firmware supports USB floppy, keyboard, mouse, and CD/DVD-ROM. These are supported as a composite device. If the virtual storage client is not available, the storage devices report media as unavailable. The USB keyboard and mouse traffic is bridged to the KVM connections.

11.5 LED Control

Te BMC has controlled UID LED and System Health LED.

The System Health LED depends on the following sensors to change the state:
Fan: 0x01, 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08.
Voltage: 0x11, 0x15, 0x16, 0x17, 0x18, 0x19, 0x1C, 0x51, 0x52, 0x55, 0x56, 0x59, 0x5A.
Temperature: 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27, 0x28, 0x41, 0x42, 0x61, 0x62.

When the BMC runs INITIALIZATION AGENT, the two LEDs are set as follows:

Table 43. State of UID LED and System Health LED

Type of LED	State
UID LED	Off
System Health LED	Off

11.6 The Concept Of Message Channel

In IPMI v1.0, there is only one channel available, for example, IPMB. In v2.0, this concept is expanded, and channel means not only IPMB, but also LAN, serial/modem, and so forth. With the help of message channel, the BMC can now accept requests from remote clients and send response messages back to other places far away. Because of security consideration, remote

clients are required to log in before sending IPMI commands. Users from System Interface and IPMB are regarded as local users. No user authentication is required for these two channels.

The following table lists BMC supported channels. For detailed implementation of LAN and serial/modem channels, refer to their respective sections. Please note this implementation does not support the serial channel. The default system base address for an I/O mapped KCS SMS Interface is CA2h. For more information, refer to the *IPMI Specification*.

Table 44. KCS Interface Register

Status	S1	S0	OEM2	OEM1	C/D#	SMS_ATN	IBF	OBF	Base+1
Command									Base+1
Data In									Base+0
Data Out									Base+0

Table 45. BMC Supported Channels

Channel Number	Protocol Type	Medium Type	Authentication Type	Access Mode
00h (Connect not insert)	IPMB (01h)	IPMB, 12C (01h)	None	Not supported
01h (Dedicated NIC)	IPMB (01h)	802.3 LAN (04h)	None / MD2/ MD5/ Straight Password	Always available
08h (Share NIC)	KCS (05h)	System I/F (0Ch)	None	Always available

11.7 PEF And Alerting Design

The PEF and Alerting mechanism is implemented in BMC. In order to make it active, the user must configure the Event Filter Table and Alert Policy Table correctly. For detailed configuration methods, refer to the *IPMI v2.0 Specification*. Note that an improperly configured E.F.T. may cause the system to perform the power cycle action repeatedly—in a loop. The supported PEF actions are listed:

- Power down
- Power cycle
- Reset
- Diagnostic interrupt(NMI)
- Send alert

The default PEF startup delay is 60 seconds. There is neither built-in E.F.T. entry nor built-in alert destinations in the system.Set this configuration at your own risk. BMC support 40 E.F.T entries, 60 A.P.T entries, and four alert strings.

Note: The PEF startup delay time must be more than 35 seconds. If not, the system performs a “Power Cycle”, “Reset”, or “Power Down” repeatedly—in a loop, and the user has no choice but to close the PEF function.

11.8 Summary Of Sensors

There is a list about the sensor data records. The following list explains the abbreviations in this table, which you can refer to obtain the full name.

SC: Sensor Capabilities (This value doesn’t include bit7)
AM: Assertion Mask
DM: Reassertion Mask
RM: Reading Mask
TM: Settable/Readable Threshold Mask

Table 46. Sensor Data Records

SENSOR #	SENSOR NAME	SENSOR TYPE	EVENT/READING TYPE	OFFSET	STANDBY
21h	MLB TEMP 1	Temperature (01h)	Threshold (01h)	SI: 7Ch SC: E8h AM: 0A80h 7/9/11/ DM: 7000h 12/13/14/ TM: 3838h 3/4/5/11/12/13/	Non-Standby
22h	MLB TEMP 2				Non-Standby
23h	MLB TEMP 3				Non-Standby
24h	MLB TEMP 4				Non-Standby
25h	MLB TEMP 5				Non-Standby
26h	MLB TEMP 6				Non-Standby
27h	MLB TEMP 7				Non-Standby
28h	MLB TEMP 8				Non-Standby
61h	CPU 1 Temp				Non-Standby
62h	CPU 2 Temp				Non-Standby
11h	STBY 5V	Voltage (02h)	Threshold (01h)	SI: 7Ch SC: E8h	Standby
15h	PS 5V				Non-Standby

SENSOR #	SENSOR NAME	SENSOR TYPE	EVENT/READING TYPE	OFFSET	STANDBY
16h	PS 12V			AM: 7A95h 0/2/4/7/9/11/12/13/14/	Non-Standby
17h	PS 3.3V			DM: 7000h 12/13/14/	Non-Standby
18h	STBY 3.3V			TM: 3F3Fh 0/1/2/3/4/5/8/9/10/11/12/13/	Standby
19h	PS 1.5V				Non-Standby
1Ch	PS 1.1V				Non-Standby
51h	VCORE 1				Non-Standby
52h	VCORE 2				Non-Standby
55h	CPU1 VTT				Non-Standby
56h	CPU2 VTT				Non-Standby
59h	CPU1 DDR 1.5V				Non-Standby
5Ah	CPU2 DDR 1.5V				Non-Standby
01h	SYS FAN 1 front	Fan (04h)	Threshold (01h)	SI: 73h SC: E8h AM: 4015h 0/2/4/14/ DM: 0000h TM: 3F3Fh 0/1/2/3/4/5/8/9/10/11/12/13/	Non-Standby
02h	SYS FAN 1 rear				Non-Standby
03h	SYS FAN 2 front				Non-Standby
04h	SYS FAN 2 rear				Non-Standby
05h	SYS FAN 3 front				Non-Standby
06h	SYS FAN 3 rear				Non-Standby
41h	CPU 1 Status	Processor (07h)	Sensor-specific (6Fh)	SI:63h SC:C0h AM:0001h 0 DM:0000h TM:0001h 0	Non-Standby
42h	CPU 2 Status				Non-Standby

SENSOR #	SENSOR NAME	SENSOR TYPE	EVENT/READING TYPE	OFFSET	STANDBY
4Fh	Thermal Trip	Processo r (07h)	Sensor-specific (6Fh)	SI: 63h SC: C0h AM: 0002h 1/ DM: 0000h RM: 0002h 1/	Standby
71h	PEF Action	System Event (12h)	Sensor-specific (6Fh)	SI: 63h SC: 40h AM: 0010h 4/ DM: 0000h RM: 0010h 4/	Non-Standby
72h	Watchdog 2	Watchdo g2 (23h)	Sensor-specific (6Fh)	SI:63h SC:40h AM:010Fh 0/1/2/3/8/ DM:0000h TM:010Fh 0/1/2/3/8/	Non-Standby
74h	AC Power On	Power Unit (09h)	Sensor-specific (6Fh)	SI: 63h SC: 40h AM: 0000h DM: 0010h 4/ RM: 0010h 4/	Standby
78h	NMI Action	Critical Interrupt (13h)	Sensor-specific (6Fh)	SI: 63h SC: 40h AM: 0009h 3/0 DM: 0000h RM: 0009h 3/0	Non-Standby
7Ah	clean SEL	System Event (12h)	Generic (03h)	SI: 63h SC: 40h AM: 0002h 1 DM: 0000h RM: 0003h 0/1	Standby

11.9 Summary Of Supported IPMI Command

The following is a list of all commands defined in *IPMI Spec v2.0*. This project is an IPMI v2.0-comformance machine (for example, all mandatory commands are supported). Some optional functions are supported, too. Special functions beyond the scope of IPMI v2.0 are implemented as OEM commands. For detailed information, refer to the following tables.

Table 47. Defined Commands

M	MANDATORY IN THE IPMI SPEC. AND IS IMPLEMENTED
O	OPTION COMMAND AND SUPPORTED IN THIS IMPLEMENTATION.
N	NOT SUPPORTED IN THIS IMPLEMENTATION.
TBD	TO BE DETERMINED

11.9.1 IPMI Device Global Commands

Table 48. IPMI Device Global Commands

GET DEVICE ID	APP	01H	M DEVICE ID: 20H (AMI BMC FOR PILOT II) DEVICE REVISION: 01H IPMI VERSION: 02H DEVICE SUPPORT: BFH RECEIVER, FRU, SEL, SDR AND SENSOR DEVICE. MANUFACTURER ID: 0019A9H = INVENTEC PRODUCT ID: 0020H (ARCTUNA)
COLD RESET	APP	02H	O
WARM RESET	APP	03H	O
GET SELF TEST RESULTS	APP	04H	M
MANUFACTURING TEST ON	APP	05H	O [REQUEST] BYTE 1 - 49H (I) BYTE 2 - 45H (E) BYTE 3 - 53H (S) [RESPONSE] BYTE 1 - COMPLETION CODE.

SET ACPI POWER STATE	APP	06H	O
GET ACPI POWER STATE	APP	07H	O
GET DEVICE GUID	APP	08H	O

11.9.2 Broadcast Commands

Table 49. Broadcast Commands

BROADCAST 'GET DEVICE ID'	APP	01H	O (UNSUPPORTED)

11.9.3 Messaging Support Commands

Table 50. Messaging Support Commands

SET BMC GLOBAL ENABLES	APP	2EH	M
GET BMC GLOBAL ENABLES	APP	2FH	M
CLEAR MESSAGE FLAGS	APP	30H	M
GET MESSAGE FLAGS	APP	31H	M
ENABLE MESSAGE CHANNEL RECEIVE	APP	32H	O
GET MESSAGE	APP	33H	M
SEND MESSAGE	APP	34H	M
READ EVENT MESSAGE BUFFER	APP	35H	O
GET BT INTERFACE CAPABILITIES	APP	36H	O (UNSUPPORTED)
MASTER WRITE-READ	APP	52H	M
GET SYSTEM GUID	APP	37H	O
SET SYSTEM INFO PARAMETERS	APP	58H	N
GET SYSTEM INFO PARAMETERS	APP	59H	N
GET CHANNEL AUTHEN CAPABILITIES	APP	38H	O
GET SESSION CHALLENGE	APP	39H	O
ACTIVATE SESSION	APP	3AH	O
SET SESSION PRIVILEGE LEVEL	APP	3BH	O
CLOSE SESSION	APP	3CH	O
GET SESSION INFO	APP	3DH	O
GET AUTHCODE	APP	3FH	O
SET CHANNEL ACCESS	APP	40H	O
GET CHANNEL ACCESS	APP	41H	O
GET CHANNEL INFO	APP	42H	O
SET USER ACCESS	APP	43H	O
GET USER ACCESS	APP	44H	O
SET USER NAME	APP	45H	O
GET USER NAME	APP	46H	O
SET USER PASSWORD	APP	47H	O

GET CHANNEL CIPHER SUITES	APP	54H	M
SET CHANNEL SECURITY KEYS	APP	56H	M
GET SYSTEM INTERFACE CAPABILITIES	APP	57H	M

11.9.4 Firmware Firewall & Command Discovery

Table 51 Firmware Firewall and Command Discovery

GET NETFN SUPPORT	APP	9H	O
GET COMMAND SUPPORT	APP	AH	O
GET COMMAND SUB-FUNCTION SUPPORT	APP	BH	O
GET CONFIGURABLE COMMANDS	APP	CH	O
GET CONFIGURABLE COMMAND SUB-FUNCTIONS	APP	DH	O
SET COMMAND ENABLES	APP	60H	O
GET COMMAND ENABLES	APP	61H	O
SET COMMAND SUB-FUNCTION ENABLES	APP	62H	O
GET COMMAND SUB-FUNCTION ENABLES	APP	63H	O
GET OEM NETFN IANA SUPPORT	APP	64H	O

11.9.5 RMCP+ Support And Payload Commands

Table 52. RMCP+ Support and Payload Commands

ACTIVATE PAYLOAD	APP	48H	M
DEACTIVATE PAYLOAD	APP	49H	M
GET PAYLOAD ACTIVATION STATUS	APP	4AH	M
GET PAYLOAD INSTANCE INFO	APP	4BH	M
SET USER PAYLOAD ACCESS	APP	4CH	M
GET USER PAYLOAD ACCESS	APP	4DH	M
GET CHANNEL PAYLOAD SUPPORT	APP	4EH	M
GET CHANNEL PAYLOAD VERSION	APP	4FH	M
GET CHANNEL OEM PAYLOAD INFO	APP	50H	M
GET CHANNEL CIPHER SUITES	APP	54H	M
SUSPEND/RESUME PAYLOAD ENCRYPTION	APP	55H	M
SET CHANNEL SECURITY KEYS	APP	56H	M

11.9.6 IPMI LAN Commands

Table 53. IPMI LAN Commands

SET LAN CONFIGURATION PARAMETERS	TRANSPORT	01H	M
GET LAN CONFIGURATION PARAMETERS	TRANSPORT	02H	M
SUSPEND BMC ARPS	TRANSPORT	03H	O
GET IP/UDP/RMCP STATISTICS	TRANSPORT	04H	O (UNSUPPORTED)

11.9.7 IPMI Serial/Modem Commands

Table 54. IPMI Serial / Modem Commands

SET SERIAL/MODEM CONFIGURATION	TRANSPORT	10H	O (UNSUPPORTED)
GET SERIAL/MODEM CONFIGURATION	TRANSPORT	11H	O (UNSUPPORTED)
SET SERIAL/MODEM MUX	TRANSPORT	12H	O (UNSUPPORTED)
GET TAP RESPONSE CODES	TRANSPORT	13H	O (UNSUPPORTED)
SET PPP UDP PROXY TRANSMIT DATA	TRANSPORT	14H	O (UNSUPPORTED)
GET PPP UDP PROXY TRANSMIT DATA	TRANSPORT	15H	O (UNSUPPORTED)
SEND PPP UDP PROXY PACKET	TRANSPORT	16H	O (UNSUPPORTED)
GET PPP UDP PROXY PACKET	TRANSPORT	17H	O (UNSUPPORTED)
SERIAL/MODEM CONNECTION ACTIVE	TRANSPORT	18H	O (UNSUPPORTED)
CALLBACK	TRANSPORT	19H	O (UNSUPPORTED)
SET USER CALLBACK OPTIONS	TRANSPORT	1AH	O (UNSUPPORTED)
GET USER CALLBACK OPTIONS	TRANSPORT	1BH	O (UNSUPPORTED)
SET SERIAL ROUTING MUX	TRANSPORT	1CH	N

11.9.8 SOL Commands

Table 55. SOL Commands

SOL ACTIVATING	TRANSPORT	20H	M
SET SOL CONFIGURATION PARAMETERS	TRANSPORT	21H	M
GET SOL CONFIGURATION PARAMETERS	TRANSPORT	22H	M

11.9.9 BMC Watchdog Timer Commands

Table 56. BMC Watchdog Timer Commands

RESET WATCHDOG TIMER	APP	22H	M
SET WATCHDOG TIMER	APP	24H	M
GET WATCHDOG TIMER	APP	25H	M

11.9.10 Chassis Commands

Table 57. Chassis Commands

GET CHASSIS CAPABILITIES	CHASSIS	00H	M
GET CHASSIS STATUS	CHASSIS	01H	M
CHASSIS CONTROL	CHASSIS	02H	M

CHASSIS RESET	CHASSIS	03H	O (UNSUPPORTED)
CHASSIS IDENTIFY	CHASSIS	04H	O
SET CHASSIS CAPABILITIES	CHASSIS	05H	O
SET POWER RESTOR POLICY	CHASSIS	06H	O
GET SYSTEM RESTART CAUSE	CHASSIS	07H	O BH: POWER-UP VIA RTC (UNSUPPORTED)
SET SYSTEM BOOT OPTIONS	CHASSIS	08H	O QUIET MODE/ BOOT INTO BIOS SETUP (UNSUPPORTED)
GET SYSTEM BOOT OPTIONS	CHASSIS	09H	O
SET FRONT BUTTON ENABLES	CHASSIS	0AH	O (HARDWARE UNSUPPORT)
SET POWER CYCLE INTERVAL	CHASSIS	0BH	O (DEFAULT : 10 SECONDS)
GET POH COUNTER	CHASSIS	0FH	M

11.9.11 Event Commands

Table 58. Event Commands

SET EVENT RECEIVER	S/E	00H	O
GET EVENT RECEIVER	S/E	01H	O
PLATFORM EVENT (A.K.A. “EVENT MESSAGE”)	S/E	02H	M

11.9.12 PEF And Alerting Commands

Table 59. PEF and Alerting Commands

GET PEF CAPABILITIES	S/E	10H	O
ARM PEF POSTPONE TIMER	S/E	11H	O
SET PEF CONFIGURATION PARAMETERS	S/E	12H	O
GET PEF CONFIGURATION PARAMETERS	S/E	13H	O
SET LAST PROCESSED EVENT ID	S/E	14H	O
GET LAST PROCESSED EVENT ID	S/E	15H	O
ALERT IMMEDIATE	S/E	16H	O
PEF ACKNOWLEDGE	S/E	17H	O

11.9.13 SEL Commands

Table 60. SEL Commands

GET SEL INFO	STORAGE	40H	M
GET SEL ALLOCATION INFO	STORAGE	41H	O
RESERVE SEL	STORAGE	42H	O
GET SEL ENTRY	STORAGE	43H	M
ADD SEL ENTRY	STORAGE	44H	M
PARTIAL ADD SEL ENTRY	STORAGE	45H	O
DELETE SEL ENTRY	STORAGE	46H	O (UNSUPPORTED)
CLEAR SEL	STORAGE	47H	M
GET SEL TIME	STORAGE	48H	M
SET SEL TIME	STORAGE	49H	M
GET AUXILIARY LOG STATUS	STORAGE	5AH	O (UNSUPPORTED)
SET AUXILIARY LOG STATUS	STORAGE	5BH	O (UNSUPPORTED)

11.9.14 SDR Repository Commands

Table 61. SDR Repository Commands

GET SDR REPOSITORY INFO	STORAGE	20H	M
GET SDR REPOSITORY ALLOCATION INFO	STORAGE	21H	O
RESERVE SDR REPOSITORY	STORAGE	22H	M
GET SDR	STORAGE	23H	M
ADD SDR	STORAGE	24H	M
PARTIAL ADD SDR	STORAGE	25H	O
DELETE SDR	STORAGE	26H	O (UNSUPPORTED)
CLEAR SDR REPOSITORY	STORAGE	27H	M
GET SDR REPOSITORY TIME	STORAGE	28H	O
SET SDR REPOSITORY TIME	STORAGE	29H	O (UNSUPPORTED)
ENTER SDR REPOSITORY UPDATE MODE	STORAGE	2AH	O
EXIT SDR REPOSITORY UPDATE MODE	STORAGE	2BH	O
RUN INITIALIZATION AGENT	STORAGE	2CH	O

11.9.15 FRU Inventory Device Commands

Table 62. FRU Inventory Device Commands

GET FRU INVENTORY AREA INFO	STORAGE	10H	M FRU DEVICE ID = 00H FOR BMC'S FRU
READ FRU DATA	STORAGE	11H	M FRU DEVICE ID = 00H FOR BMC'S FRU
WRITE FRU DATA	STORAGE	12H	M FRU DEVICE ID = 00H FOR BMC'S FRU

11.9.16 Sensor Device Commands

Table 63. Sensor Device Commands

GET DEVICE SDR INFO	S/E	20H	O (UNSUPPORTED)
GET DEVICE SDR	S/E	21H	O (UNSUPPORTED)
RESERVE DEVICE SDR REPOSITORY	S/E	22H	O (UNSUPPORTED)
GET SENSOR READING FACTORS	S/E	23H	O
SET SENSOR HYSTERESIS	S/E	24H	O
GET SENSOR HYSTERESIS	S/E	25H	O
SET SENSOR THRESHOLD	S/E	26H	O
GET SENSOR THRESHOLD	S/E	27H	O
SET SENSOR EVENT ENABLE	S/E	28H	O
GET SENSOR EVENT ENABLE	S/E	29H	O
RE-ARM SENSOR EVENTS	S/E	2AH	O (UNSUPPORTED)
GET SENSOR EVENT STATUS	S/E	2BH	O (UNSUPPORTED)
GET SENSOR READING	S/E	2DH	M
SET SENSOR TYPE	S/E	2EH	O (UNSUPPORTED)
GET SENSOR TYPE	S/E	2FH	O (UNSUPPORTED)
SET SENSOR READING AND EVENT STATUS	S/E	30H	N

11.9.17 OEM Commands

Table 64. OEM Commands

Get build info (Not ready)	OEM	b0h	[Request] N/A [Response] Byte 1 - Completion code. 20 - bytes Build date
stop sensor polling	OEM	b1h	[Request] Byte 1 – H/W Monitor Sensor polling start/stop. 1: indicate stop H/W monitor sensor polling. 0: indicate start H/W monitor sensor polling. [Response] Byte 1 – Completion code.

SET port80 code	OEM	b2h	[Request] Byte 1 – Port80 Code that need to be log in FRB2 event. [Response] Byte 1 – Completion code
set system guid	OEM	b3h	[Request] 16-bytes System GUID. [Response] Byte 1 – Completion code.
set Device guid	OEM	b4h	[Request] 16-bytes Device GUID. [Response] Byte 1 – Completion code.
set PECI OFFSET	OEM	b5h	[Request] Byte 1 – Sensor Number. Byte 2 – Offset Value. [Response] Byte 1 – Completion code.
GET PECI OFFSET	OEM	b6h	[Request] Byte 1 – Sensor Number. [Response] Byte 1 – Completion code. Byte 2 – Offset Value
set OEM Fan table	OEM	b7h	[Request] Byte 1 – Parameter selector. Byte 2 to N – Configuration parameter data. [Response] Byte 1 – Completion code. Detail information please refers Notice 1.

Get OEM Fan table	OEM	b8h	[Request] Byte 1 – Parameter selector. Byte 2 – Data 1. (if nothing, reserve 00) Byte 3 – Data 2. (if nothing, reserve 00) [Response] Byte 1 – Completion code. Byte 2 to N – Configuration Parameter data. Detail information please refers Notice 1.
Notice 1: Parameter Selector and Configuration parameter data.			

parameter	#	Parameter data
Set current status	0	0-Static status 1-Oem status
Global fan enable	1	0-Oem disable 1-Oem enable
Each fan setting 1	2	Request: Data 1:Table number Response: Data 1:Table number Data 2: Each enable Data 3: Temperature sensor number Data 4: PWM pin number
Each fan setting 2	3	Request: Data 1:Table number Data 2:Format Setting 00 – rise temperature table 01 – rise PWM value table 10 – decline temperature setting 11 – decline PWM value table Response: Data 1: Table Number Data 2: format setting

		Data 3 - 15 The table values
Min PWM value	4	The min PWM value of fan table
Max PWM value	5	The max PWM value of fan table

12. Environmental Specifications

The following specifications pertain to the PCAs, hard drives, and other system components when placed in the target system.

12.1 Operational Environment

Purpose:
To verify proper operation over specified operating environments.

Description:
The PCAs, hard drives, and other system components should function properly when placed in a system in the following conditions (excluding rack effects):

- Ambient Temperature: 0 to 35 C
- Relative Humidity: 20% to 80%

System design should guarantee proper thermal cooling to allow operation under the above specified conditions. Design should ensure thermal shutdown to guarantee component safety in the event the operating range was exceeded.

12.2 Storage Environmental Extremes

Purpose:
To verify the PCAs, hard drives, and other system components' ability to withstand adverse storage conditions to identify potential environmental failure mechanisms.

Description:
The PCAs, hard drives, and other system components should function properly when placed in a system and operated in the ranges specified above after being shipped or stored in the following conditions:

- Temperature: -40 to 70 C
- Relative Humidity: 5% to 95%

12.3 Shock

Purpose:
To verify all components in system ability to withstand shock encountered during use and shipment.

Description:
PCAs, hard drives, and other systems components are placed in a target system, which is subjected to specified shock pulses.

- Test Parameters/Conditions:

- Operating:
  - Half sine wave shock - 5 G, 11 ms duration, half sine wave shock in each direction of three mutually perpendicular axes. 10 pulse per face.

- Non-operating:
  - Half sine wave shock (engineering evaluation only) - 120 G, 2 ms duration, half sine wave shock in each direction of three mutually perpendicular axes. There shall be one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs.
  - Square wave shock - 40 G, velocity change is associated with the weight of fully-packed unit, square wave shock in each direction of three mutually perpendicular axes. There shall be one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs.

Table 65. Velocity Change for Fully Packing Weight

Fully Packing Weight	Velocity Change
0<W≦20 lbs	180 in/sec
20<W≦50 lbs	166 in/sec
50<W≦80 lbs	152 in/sec
80<W≦150 lbs	136 in/sec

12.4 Vibration

Purpose:
To verify the PCAs, hard drives, and other system components' ability to withstand vibrations encountered during use and shipment.

Description:
PCAs, hard drives, and other system components are subjected to specified vibration sweeps while installed in a target system.

Test Parameters/Conditions:
- Operating:
  - Sinusoidal Vibration (engineering evaluation only) - 0.2 G zero-to-peak, 5 ~ 350 ~5 Hz, 0.25 Oct/min in each of three mutually perpendicular axes. The number of sweeps from 5 to 350 to 5 Hz in each axis shall be sufficient so that each mass storage device can be operationally exercised throughout the entire sweep frequency range.
  - Random Vibration - 0.00grms to 0.3grms, increased by 0.05grms for each of three mutually perpendicular axes. The test duration in each axis shall be sufficient so that each mass storage device can be operationally exercised.

- Non-operating:
  - Sinusoidal Vibration (engineer evaluation only) - 0.75 G zero-to-peak, 10~500~10 Hz, 0.5 Oct/min. The test duration shall be one sweep from 10 to 500 to 10 Hz in each of three mutually perpendicular axes.
  - Random Vibration - 2 G, 10~500 Hz, in each of three mutually perpendicular axes. The test duration shall be one hour/axis for total test duration of three hours.

12.5 Rotational Vibration

Purpose:

To judge the performance of a functional storage device when subject internal vibration

Description:

Tested unit should be railed and fixed on the fixture, and running performance measurement software, I/O meter is used here. Run the unit which sustains no fan vibration to establish a baseline I/O rates. Set the unit to running both at normal (low) and full (high) fan speed while taking their own I/O rates.

SATAII system degradation shall be less than or equal to 15% (low) and 20% (high)

12.6 Acoustics

(1) Test Purpose: To validate if the product could be easy in acoustic feeling while it is in use
(2) Test method: Acoustic noise measurement shall be conducted in accordance with ISO 7779: 1999(E) and declared verified in accordance with ISO 9296: 1988(E).
(3) Sample size: 1 unit.
(4) Test criteria:
The following levels in the product specification shall not be exceeded when the computer is operated in an ambient environment where the temperature is 25 C or less:

Table 66. Acoustics Test Criteria

System Operating Mode	Declared A-weighted Sound Power Level Lwad re 1pW, bels
Idle	7.0 Bels
Operating	7.0 Bels

Declared noise values (The declared sound power level per ISO 9296) shall be 0.3 Bels higher than the measured values when only 1 sample of the same system is tested. This test must be performed on undamaged units. Dynamics tests and temperature/ humidity tests may cause increased noise levels.
Packaging

12.6.1 Drop Test

Table 67. Drop Test

Package Gross Weight (Pounds)	Design Drop Height (Inches)
0 **[0.0]** < W ≤ 10 **[4.5]**	48
10 **[4.5]** < W ≤ 24 **[11.0]**	42
24 **[11.0]** < W ≤ 45 **[20.5]**	36
45 **[20.5]** < W ≤ 80 **[34.0]**	30

Drop sequence: 1 corner, 3 edges and 6 faces

12.6.2 Vibration Test

Table 68. Vibration Test

Frequency (Hz)	PSD Level (g^2/Hz)
1	0.0001
4	0.01
100	0.01
200	0.001

Input acceleration is 1.15 g RMS.
Three axes on all samples.
The test duration shall be one hour/axis for total test duration of three hours.
Random control limit tolerance is + 3 dB.

12.7 Replacing the Backup Battery

The lithium battery on the server board powers the real time clock (RTC) for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (e.g., the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

ADVARSEL!

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

13. Regulatory and Certification Information

Chassis Level Requirements

13.1 Product Regulatory Compliance

The server chassis product, when correctly integrated per this guide, complies with the following safety and electromagnetic compatibility (EMC) regulations.

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation.

Notifications to Users on Product Regulatory Compliance and Maintaining Compliance – To ensure regulatory compliance, you must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products / components will void the UL or other NRTL listings and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in the region(s) in which the product is sold.

To help ensure EMC compliance with your local regional rules and regulations, before computer integration, make sure that the chassis, power supply, and other modules have passed EMC testing using a server board with a microprocessor from the same family (or higher) and operating at the same (or higher) speed as the microprocessor used on this server board. The final configuration of your end system product may require additional EMC compliance testing. For more information please contact your local Intel Representative. This is an FCC Class A device and its use is intended for a commercial type market place.

13.2 Use of Specified Regulated Components

To maintain the NRTL listings and compliance to other regulatory certifications and/or declarations, the following regulated components must be used and conditions adhered to. Interchanging or use of other component will void the NRTL listing and other product certifications and approvals.

Updated product information for configurations can be found on the Intel Server Builder Web site at the following URL:
http://channel.intel.com/go/serverbuilder
If you do not have access to Intel's Web address, please contact your local Intel representative.

Server chassis (base chassis is provided with power supply and fans) – NRTL listed.

Add-in boards – must have a printed wiring board flammability rating of minimum UL94V-1. Add-in boards containing external power connectors and/or lithium batteries must be UL recognized or UL listed. Any add-in board containing modem telecommunication circuitry must be UL listed. In addition, the modem must have the appropriate telecommunications, safety, and EMC approvals for the region in which it is sold.

Peripheral Storage Devices – must be UL recognized or UL listed accessory and TUV or VDE licensed. Maximum power rating of any one device or combination of devices can not exceed manufacturer's specifications. Total server configuration is not to exceed the maximum loading conditions of the power supply.

The following table references Server Chassis Compliance and markings that may appear on the product. Markings below are typical markings however, may vary or be different based on how certification is obtained.

Note: Certifications Emissions requirements are to Class A.

Table 69. Product Safety & Electromagentic (EMC) Compliance

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
Australia / New Zealand	AS/NZS 3548 (Emissions)	 N232
Argentina	IRAM Certification (Safety)	
Canada / USA	CSA 60950 – UL 60950 (Safety) - CONFORMS TO ANSI/UL STD. 60950-1 CERTIFIED TO CAN/CSA STD. C22.2 No. 60950-1	 3178574
	Industry Canada ICES-003 (Emissions)	CANADA ICES-003 CLASS A CANADA NMB-003 CLASSE A
	FCC CFR 47, Part 15 (Emissions)	This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept interference receive, including interference that may cause undesired operation.
CENELEC Europe	Low Voltage Directive EMC Directive EN55022 (Emissions) EN55024 (Immunity) EN61000-3-2 (Harmonics) EN61000-3-3 (Voltage Flicker) CE Declaration of Conformity	

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
Germany	GS Certification – EN60950	
International	CB Certification – IEC60950 CISPR 22 / CISPR 24	None Required
Japan	VCCI Certification	この装置は、クラスA情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。VCCI-A
Korea	KCC Certification	 방송통신위원회 인증번호: SR1680 (A)
Russia	GOST-R Certification	 MO04
Ukraine	Ukraine Certification	None Required
Taiwan	BSMI CNS13438	 R33025
		警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策

13.3 Electromagnetic Compatibility Notices

13.3.1 USA

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable

protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient or relocate the receiving antenna.

Increase the separation between the equipment and the receiver.

Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.

Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

13.3.2 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

(English translation of the notice above) This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

13.3.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

13.3.4 Japan EMC Compatibility

Electromagnetic Compatibility Notices (International)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:

This is a Class A product based on the standard of the Voluntary Control Council For Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

13.3.5 BSMI (Taiwan)

The BSMI Certification number and the following warning is located on the product safety label which is located on the bottom side (pedestal orientation) or side (rack mount configuration).

警告使用者：

這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策。

13.3.6 KCC (Korea)

Following is the RRL certification information for Korea.

방송통신위원회

인증번호: CPU-SR1690 (A

13.4 Rack Mount Installation Guidelines

Anchor the equipment rack: The equipment rack must be anchored to an unmovable support to prevent it from falling over when one or more servers are extended in front of the rack on slides. You must also consider the weight of any other device installed in the rack. A crush hazard exists should the rack tilt forward which could cause serious injury.
Temperature: The temperature, in which the server operates when installed in an equipment rack, must not go below 5 °C (41 °F) or rise above 40 °C (104 °F). Extreme fluctuations in temperature can cause a variety of problems in your server.
Ventilation: The equipment rack must provide sufficient airflow to the front of the server to maintain proper cooling. The rack must also include ventilation sufficient to exhaust a maximum of 1023 BTUs (British Thermal Units) per hour for the server. The rack selected and the ventilation provided must be suitable to the environment in which the server will be used.
If AC power supplies are installed:

Mains AC power disconnection: The AC power cord(s) is considered the mains disconnect for the server and must be readily accessible when installed. If the individual server power cord(s) will not be readily accessible for disconnection then you are responsible for installing an AC power disconnect for the entire rack unit. This main disconnect must be readily accessible, and it must be labeled as controlling power to the entire rack, not just to the server(s).

Grounding the rack installation: To avoid the potential for an electrical shock hazard, you must include a third wire safety ground conductor with the rack installation. If the server power cord is plugged into an AC outlet that is part of the rack, then you must provide proper grounding for the rack itself. If the server power cord is plugged into a wall AC outlet, the safety ground conductor in the power cord provides proper grounding only for the server. You must provide additional, proper grounding for the rack and other devices installed in it.

Over current protection: The server is designed for an AC line voltage source with up to 20 amperes of over current protection per cord feed. If the power system for the equipment rack is installed on a branch circuit with more than 20 amperes of protection, you must provide supplemental protection for the server.

If DC power supplies are installed:

Connection with a DC (Direct Current) source should only be performed by trained service personnel. The server with DC input is to be installed in a Restricted Access Location in accordance with articles 110-16, 110-17, and 110-18 of the National Electric Code, ANSI/NFPA 70. The DC source must be electrically isolated by double or reinforced insulation from any hazardous AC source.

Main DC power disconnect: You are responsible for installing a properly rated DC power disconnect for the server system. This mains disconnect must be readily accessible, and it must be labeled as controlling power to the server. The circuit breaker of a centralized DC power system may be used as a disconnect device when easily accessible and should be rated no more than 10 amps. Grounding the server: To avoid the potential for an electrical shock hazard, you must reliably connect an earth grounding conductor to the server. The earth grounding conductor must be a minimum 18AWG connected to the earth ground stud(s) on the rear of the server. The safety ground conductor should be connected to the chassis stud with a Listed closed two-hole crimp terminal having 5/8 inch pitch. The nuts on the chassis earth ground studs should be installed with a 10 in/lbs torque. The safety ground conductor provides proper grounding only for the server. You must provide additional, proper grounding for the rack and other devices installed in it.

Over current protection: Overcurrent protection circuit breakers must be provided as part of each host equipment rack and must be incorporated in the field wiring between the DC source and the server. The branch circuit protection shall be rated minimum 75Vdc, 10 A maximum per feed pair. If the DC power system for the equipment rack is installed with more than 10 amperes of protection, you must provide supplemental protection for the server.

13.5 Power Cord Usage Guidelines

Warning: Do not attempt to modify or use an AC power cord set that is not the exact type required.

You must use a power cord set that meets the following criteria:

• Rating: In the U.S. and Canada, cords must be UL (Underwriters Laboratories, Inc.) Listed/CSA (Canadian Standards Organization) Certified type SJT, 18-3 AWG (American Wire Gauge). Outside of the U.S. and Canada, cords must be flexible harmonized (<HAR>) or VDE (Verband Deutscher Electrotechniker, German Institute of Electrical Engineers) certified cord with 3 x 0.75 mm conductors rated 250 VAC (Volts Alternating Current). • Connector, wall outlet end: Cords must be terminated in grounding-type male plug designed for use in your region.

The connector must have certification marks showing certification by an agency acceptable in your region and for U.S. must be Listed and rated 125% of overall current rating of the server.
• Connector, server end: The connectors that plug into the AC receptacle on the server must be an approved IEC (International Electrotechnical Commission) 320, sheet C13, type female connector.
• Cord length and flexibility: Cords must be less than 4.5 meters (14.76 feet) long.

13.6 Product Ecology Compliance

Intel has a system in place to restrict the use of banned substances in accordance with world wide product ecology regulatory requirements. The following is Intel's product ecology compliance criteria.

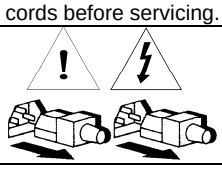
Table 70. Product Ecology Compliance

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
California	California Code of Regulations, Title 22, Division 4.5; Chapter 33: Best Management Practices for Perchlorate Materials.	Special handling may apply. See www.dtsc.ca.gov/hazardouswaste/perchlorate This notice is required by California Code of Regulations, Title 22, Division 4.5; Chapter 33: Best Management Practices for Perchlorate Materials. This product / part includes a battery which contains Perchlorate material.
China	**China RoHS** Administrative Measures on the Control of Pollution Caused by Electronic Information Products" (EIP) #39. Referred to as China RoHS. Mark requires to be applied to retail products only. Mark used is the Environmental Friendly Use Period (EFUP). Number represents years. **China Recycling (GB18455-2001)** Mark requires to be applied to be retail product only. Marking applied to bulk packaging and single packages. Not applied to internal packaging such as plastics, foams, etc.	 

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
Intel Internal Specification	All materials, parts and subassemblies must not contain restricted materials as defined in Intel's ***Environmental Product Content Specification*** of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm	None Required
Europe	**Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC** – Mark applied to system level products only.	
	European Directive 2002/95/EC - Restriction of Hazardous Substances (RoHS) Threshold limits and banned substances are noted below. Quantity limit of 0.1% by mass (1000 PPM) for: Lead, Mercury, Hexavalent Chromium, Polybrominated Biphenyls Diphenyl Ethers (PBB/PBDE) Quantity limit of 0.01% by mass (100 PPM) for: Cadmium	None Required
Germany	**German Green Dot** Applied to Retail Packaging Only for Boxed Boards	
Intel Internal Specification	All materials, parts and subassemblies must not contain restricted materials as defined in Intel's ***Environmental Product Content Specification*** of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm	None Required
International	**ISO11469** - Plastic parts weighing >25gm are intended to be marked with per ISO11469.	>PC/ABS<
	Recycling Markings – Fiberboard (FB) and Cardboard (CB) are marked with international recycling marks. Applied to outer bulk packaging and single package.	 

13.7 Other Markings

Table 71. Other Markings

Compliance Description	Compliance Reference	Compliance Reference Marking Example
Stand-by Power	60950 Safety Requirement Applied to product is stand-by power switch is used.	
Multiple Power Cords (only for product with more than 1 power cord)	60950 Safety Requirement Applied to product if more than one power cord is used.	English: This unit has more than one power supply cord. To reduce the risk of electrical shock, disconnect (2) two power supply cords before servicing.
		
		Simplified Chinese: 注意： 本设备包括多条电源系统电缆。为避免遭受电击，在进行维修之前应断开两（2）条电源系统电缆。
		Traditional Chinese: 注意： 本設備包括多條電源系統電纜。爲避免遭受電擊，在進行維修之前應斷開兩（2）條電源系統電纜。
		German: Dieses Geräte hat mehr als ein Stromkabel. Um eine Gefahr des elektrischen Schlages zu verringern trennen sie beide (2) Stromkabeln bevor Instandhaltung.
Ground Connection	60950 Deviation for Nordic Countries	Line1 : "WARNING:" Swedish on line2: "Apparaten skall anslutas till jordat uttag, när den ansluts till ett nätverk." Finnish on line 3: "Laite on liitettävä suojamaadoituskoskettimilla varustettuun pistorasiaan." English on line 4: "Connect only to a properly earth grounded outlet."
Country of Origin	Logistic Requirements Applied to products to indicate where product was made.	Made in China

Appendix A: Integration and Usage Tips

This section provides a list of useful information unique to the Intel® Server System SR1680MV.

- Processor fans are not supported and not needed in the server system. The system fan module and power supply fans provide the necessary cooling needed for the system.
- The air duct and DIMM Blanks must be used to maintain system thermals.
- To maintain system thermals, all hard drive bays must be populated with either a hard drive or drive blank.
- System fans are not hot-swappable
- The FRUSDR utility must be run to load the proper Sensor Data Records for the server system onto the server board.
- Make sure the latest system software is loaded on the server. This includes system BIOS, integrated BMC firmware, You can download the latest system software from: http://support.intel.com/support/motherboards/server/SR1680MV/

Glossary

This appendix contains important terms used in this document. For ease of use, numeric entries are listed first (for example, “82460GX”) followed by alpha entries (for example, “AGP 4x”). Acronyms are followed by non-acronyms.

Word / Acronym	Definition
ACA	Australian Communication Authority
ANSI	American National Standards Institute
BMC	Baseboard Management Controller
BIOS	Basic Input/Output System
CMOS	Complementary Metal-oxide-semiconductor
D2D	DC-to-DC
EMP	Emergency Management Port
FP	Front Panel
FRB	Fault Resilient Boot
FRU	Field Replaceable Unit
I^2C	Inter-integrated Circuit bus
LCD	Liquid Crystal Display
LPC	Low-pin Count
LSB	Least Significant Bit
MSB	Most Significant Bit
MTBF	Mean Time Between Failure
MTTR	Mean Time to Repair
NIC	Network Interface Card
NMI	Non-maskable Interrupt
OTP	Over-temperature Protection
OVP	Over-voltage Protection
PCI	Peripheral Component Interconnect
PCB	Printed Circuit Board
PCIe*	Peripheral Component Interconnect Express*
PCI-X	Peripheral Component Interconnect Extended
PFC	Power Factor Correction
POST	Power-on Self Test
PSU	Power Supply Unit
RAM	Random Access Memory
RI	Ring Indicate
SCA	Single Connector Attachment
SDR	Sensor Data Record
SE	Single-Ended
THD	Total Harmonic Distortion
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VCCI	Voluntary Control Council for Interference
VSB	Voltage Standby

Reference Documents

Refer to the following documents for additional information:

- *Intel® Server System SR1680MV Spares/Parts List and Configuration Guide*
- *Intel® Server System SR1680MV Service Guide*