
Intel® Server Board SE7520JR2

Intel® Server Chassis SR1400

Intel® Server Chassis SR1450

Intel® Server Chassis SR2400

Technical Specification Update

December 2005



Enterprise Platforms & Services Division

Revision History

Date	Revision Number	Modifications
Jan 2005	1.0	Initial Release
March 2005	2.0	2 nd external release
June	3.0	Added SR1450, updates to Errata List, Update to Useful Info
December	4.0	Updated the erratum #10, added the erratum #14 and the documentation changes #5, #6, #7

Disclaimers

The Intel® Server Board SE7520JR2, Intel® Server Chassis SR1400, SR1450, and SR2400 may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

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I. Preface

This document is an update to the product definition specified in the *Intel® Server Board SE7520JR2 Technical Product Specifications*, *Intel® Server Chassis SR1400 Technical Product Specifications*, *Intel® Server Chassis SR1450 Technical Product Specification*, and the *Intel® Server Chassis SR2400 Technical Product Specifications* (Order Numbers C78844-002, C78846-001, D11535-001, and C78845-001). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain specification changes, specification clarifications, errata, and document changes.

Refer to the *Intel® Xeon™ Processor Specification Update* (Document Number 249678-029) for specification updates concerning the Xeon™ processor. Items contained in the *Xeon™ Processor Specification Update* that either do not apply to the Intel® Server board SE7520JR2 or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

1 Nomenclature

- **Specification Changes** are modifications to the current published specifications for the Intel® Server Board SE7520JR2, Intel® Server Chassis SR1400, SR1450, and SR2400. These changes will be incorporated in a future release of the given document.
- **Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in a future release of the given document.
- **Documentation Changes** include typos, errors, or omissions from documents that are currently published. These documents may include Product Specs and Users Guides. These changes will be incorporated in a future release of the given document.
- **Errata** are design defects or errors. Errata may cause the Intel® Server Board SE7520JR2, Intel® Server Chassis SR1400, SR1450, and SR2400 behavior to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

2 Product Scope

In this document, the name SE7520JR2 is will describe the family of boards that are made available under a common product name. The core features for each board will be common; however each board will have the following distinctions:

Table 1. Intel® Server Board SE7520JR2 SKUs

Product Code	Feature Distinctions
SE7520JR2SCSID2	Onboard SCSI + Onboard SATA (RAID) + DDR2 – 400 MHz
SE7520JR2SCSID1	Onboard SCSI + Onboard SATA (RAID) + DDR – 266/333 MHz
SE7520JR2ATAD2	Onboard SATA (RAID) + DDR2 – 400 MHz
SE7520JR2ATAD1	Onboard SATA (RAID) + DDR – 266/333 MHz

This document will also include errata and specification changes for the **Intel® Server Chassis SR1400, Intel® Server Chassis SR1450, and Intel® Server Chassis SR2400**, including the following Intel factory inegrated SKUs:

Table 2. Intel® Server Board SE7520JR2 Integrated System SKUs

Product Code	Feature Distinctions
SR1400SYS	1U Server Platform, SCSI, DDR 266/333
SR1400SYSNA	1U Server Platform, SCSI, DDR 266/333, w/North America Power Cord
SR2400SYS	2U Server Platform, SCSI, DDR 266/333
SR2400SYSNA	2U Server Platform, SCSI, DDR 266/333, w/North America Power Cord
SR2400SYSD2	2U Server Platform, SCSI, DDR2 400
SR2400SYSD2NA	2U Server Platform, SCSI, DDR2 400, w/North America Power Cord

II. Summary Tables

The following tables provide a summary of known errata and planned documentation changes for each of the following Intel products: Intel® Server Board SE7520JR2, Intel® Server Chassis SR1400, Intel® Server Chassis SR1450, and Intel® Server Chassis SR2400. Where possible, Intel will correct existing product errata with future product updates. Documentation changes will be made in future updates to the given document. Please refer to the following notations as legend.

Table 3. Document Notation

Doc:	Intel intends to update the appropriate document in a future revision.
Investigating	Intel is investigating the issue.
Fix:	Intel intends to fix this erratum in a future product update
Fixed:	This erratum has been addressed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or has been modified from the previous specification update.

Table 4. Summary of Known Product Errata

No.	Plans	Description of Errata
1.	Fixed	Memory Mirroring Not Supported by the System BIOS
2.	No Fix	Microsoft Windows* 2003 operating system shows 2 monitors in Device Manager.
3.	Fixed	Some RAID controllers fail to recognize their Option ROM access hot-key sequence needed to configure the card during POST
4.	Fixed	Platform Confidence Test (PCT) reports SIO error when no floppy drive is present
5.	Fixed	Unknown Interrupt Error Message During POST
6.	Fixed	COM Port B Ring Indicator not terminated correctly.
7.	Fixed	BMC SEL Timestamp Incorrect Information
8.	No Fix	Current BIOS does not support Legacy Mode for the on-board Serial ATA (SATA) ports
9.	No Fix	Non-threshold base sensors mBMC responds threshold value
10.	Fixed	LM93 sensor monitoring issue
11.	No Fix	The silk screen identifying the PCI Slot numbers on the Low Profile PCI Riser card for the SR2400 is not consistent with the silk screen of the full height PCI-X riser card.
12.	Fix	CPU 2 Processor Fault LED illuminated when no processor is installed
13.	No Fix	Silk screen for onboard SCSI Channels denote the internal SCSI connector as Channel A and the external SCSI connector as Channel B. However, LSI firmware recognizes them in opposite order.
14.	Fixed	Blinking Green Status LED Associated with FRUSDR 6.6.8 and Earlier on S7520JR2ATAD2 Server Boards

Table 5. Summary of Planned Documentation Changes

No.	Plans	Description of Documentation Change
1.	Doc	SATA drive activity LED is driven by both the backplane controller and the Hard Drives
2.	Doc	Incorrect description of 50-pin front panel connector as J1J2
3.	Doc	Incorrect pin assignment for table 90 "OEM RMC Connector Pinout (J3B2)" on TPS
4.	Doc	Incorrect measurement for table 1 "Chassis Dimentions" in TPS
5.	Doc	Power module must be inserted into the top slot of the power module enclosure in single power module configuration
6.	Doc	Memory error handling mechanism in BIOS is changed
7.	Doc	3-pin cable in SR1450 SATA Backplane Kit is not used with the onboard SATA controller

The following sections will provide expanded descriptions for each of the listed erratum / documentation changes indicated in the previous tables. The reference number specified for each listed item in the previous tables will match the expanded descriptions on the following pages.

III. Errata

1 Memory Mirroring Not Supported by the System BIOS

Problem The Memory Mirroring RASUM feature enabled by the Intel® E7520 Chipset is not currently supported by the Intel Server Board SE7520JR2 BIOS.

Implication Customers will not be able to use the Memory Mirroring capability.

Workaround None.

Status Fixed. Intel has enabled this feature with system BIOS P07 and later

2 Microsoft Windows* 2003 operating system shows 2 monitors in Device Manager.

Problem Microsoft Windows* 2003 operating system shows 2 monitors in Device Manager.

Implication Under Windows* 2003, in Device Manager, 2 monitors will be shown as below:

1. Default monitor
2. Plug & play Monitor.

Workaround At this moment there is no workaround or fix for this. The reason two monitors are showing up under Windows* is because the video BIOS used enables both the CRT and DVI outputs of the ATI RageXL*. This is necessary to support the Intel Management Module (IMM). Due to some architectural limitations with ATI RageXL*, the DVI output cannot be turned off even when the IMM is not installed.

Status No Fix.

3 Some RAID controllers fail to recognize their Option ROM access hot-key sequence needed to configure the card during POST

Problem Intel has determined a BIOS issue where some RAID controllers may fail to recognize their Option ROM access hot-key sequence needed to configure the card during POST.

Implication Configuring a RAID Array may not be possible

Workaround None

Status Fixed. Intel has corrected this issue starting with BIOS P07

4 Platform Confidence Test (PCT) reports SIO error when no floppy drive is present

Problem With no floppy drive connected to the onboard floppy controller, the Comprehensive Test option of PCT revs 1.03 and 1.04 when run from either a CDROM or a Hard Drive (HDD) will report a Super IO error as follow:

“ERROR: SIO308.Verify_ESCD
Resource mismatch between ECSD structure and SIO Registers”

Implication The PCT utility was developed to run from a floppy disk only. It was designed to automatically detect the presence of an onboard floppy drive during the Comprehensive Test option. However, with no floppy drive present the system BIOS keeps the onboard floppy controller enabled. During the HW detection process the PCT checks for the status of the floppy controller only assuming a floppy drive is present. This causes the SIO test module to fail. Until the new PCT is available, Intel recommends customers to disregard this error.

Workaround Add a floppy drive to the system configuration to clear error.

Status Fixed. Intel has corrected this issue starting with PCT Release 1.05.

5 Unknown Interrupt Error Message during POST

Problem When there are no bootable media or devices present i.e. no bootable floppy disk, cdrom disk or hard drive, the following error message may appear during POST:

"INT 0000006F Unknown Interrupt - HALT !!! (00000010 : XXXXXXXX) "

After posting the error, the machine boots to the EFI shell.

Implication This anomaly is due to the BIOS not masking an interrupt from the ICH5 correctly with MCH <= C2 stepping. The system will boot to EFI-32 after this error message posted. An EFI fix has been done in the P05 BIOS and later.

Workaround Add a bootable media device to system configuration.

Status Fixed. Intel has corrected this issue starting with production BIOS P05.

6 COM Port B Ring Indicator not terminated correctly.

Problem On first board productions of the Intel® Server Board SE7520JR2, the RI (ring indication) pin of the external serial port B, commonly used for modem applications, was incorrectly terminated. This may result with RI signal not functioning reliably.

Implication Modem not supported.

Workaround None.

Status Fixed. Intel has corrected this issue with a change to the basedboard, which was implemented in October of 2004. For details, please reference Product Change Notification #104462.

7 BMC SEL Timestamp Incorrect Information

Problem The Intel® Server Board SE7520JR2 has been found to have a BIOS erratum which causes the BMC SEL timestamp information to be incorrect. Beginning on January 1, 2005, the BMC date will lag the system date by 1 day. The system date January 1, 2005 will appear as December 31, 2004 in the BMC, and the BMC will be one day behind thereafter. Another day will be lost on January 1 of each succeeding year that follows a leapyear, i.e. 2009, 2013, etc

Implication The effect of this erratum is that the BMC will use this incorrect date for all entries in the System Event Log (SEL) maintained by the BMC. This includes informational events as well as error events, e.g. memory error events. Other BMC functions are unaffected..

Workaround None.

Status Fixed. This issue is corrected in produciton BIOS P07.10 and later.

8 Current BIOS does not support Legacy Mode for the on-board Serial ATA (SATA) ports

Problem The Intel® Server Boards SE7520JR2 (all SKUs) ship with the SATA ports from the Intel® ICH5-R I/O controller configured in Enhance Mode as the default. The current BIOS does not provide the user the capability to change the on-board SATA ports to Legacy Mode.

Implication Current BIOS limitation prevents users from installing and booting legacy operating systems from the on-board SATA ports when not configured in SATA RAID mode. Data access to SATA drives by Legacy operating systems installed on on-board SCSI controller or alternate HBAs is supported.

Workaround None.

Status No Fix.

9 Non-threshold base sensors mBMC responds threshold value.

Problem When a *Get Sensor Thresholds* command is sent to the mBMC for a non-threshold based sensor, the mBMC responds to the command as though the sensor was a threshold based sensor. The command should return an error code indicating that the request was not valid for that sensor, which it doesn't.

Implication A misleading threshold sensor information will be sent to any applications using the *Get Sensor Thresholds* command when issued to a non-threshold based sensor.

Workaround None.

Status No Fix.

10 LM93 sensor monitoring issue

Problem The Intel® Server Board SE7520JR2 has been found to have an issue where the LM93 monitoring chip is masking events generated by specific system sensors. This is happening because the LM93 part is operating in an S4/S5 sleep mode. Masked events are not passed to the system Baseboard Management Controller (BMC) for sensor readings, event logging or event processing. The following sensors attached to the LM93 are masked by this issue: IERR, Therm Trip, SCSI Term Error, VRD Therm Mon, Proc Hot & Throttling.

Implication Sensors that are masked by this issue will not have current readings available from the BMC, these events may not be logged in the BMC's System Event Log and BMC functions that require current readings for these sensors may not operate. This includes the automatic NMI that the BMC generates when it detects an IERR.

Workaround IERR, Therm Trip, SCSI Term Error, VRD Therm Mon, Proc Hot & Throttling are hardware based and this issue does not impact the functionality of these features. This is primarily an issue with the ability of server management software to monitor and report the status of these sensors.

Status Fixed. This issue has been corrected by a baseboard change, which was implemented in September of 2005. For details, please reference Product Change Notification #105053-03.

11 The silk screen identifying the PCI Slot numbers on the Low Profile PCI riser card for the SR2400 is not consistent with silk screen of the Full Height PCI-X (passive) riser card.

Problem Not having the PCI slot number silk screen of the two PCI-X risers cards match may cause confusion when populating add-in cards into these two risers.

Implication This issue may lead someone to populate add-in cards incorrectly. Not following the add-in card population rules for these two risers will result in a error message to be reported during system boot and halt the POST process.

Workaround If an error message is reported during POST for an add-in card population violation, verify that add-in cards are populated starting with the top slot first, followed by the middle, and finally the bottom slot closest to the baseboard.

Status No Fix. At this time, there is no plan to correct the silk screen on the riser card.

12 CPU 2 Processor Fault LED illuminated when no processor is installed

Problem	In a system configured with an Intel Management Module (IMM) Professional or Advanced Editions, the CPU-2 Fault LED will be illuminated when no second processor is installed.
Implication	When a fault LED is illuminated, it typically means that there is a failed component that needs to be replaced. In this case, there is no second CPU installed in the system. This fault indicator may lead to someone believing there is a fault somewhere on the board that needs correcting, when in fact there is not.
Workaround	None. With no CPU-2 installed, this fault indicator should be ignored. There is no SEL event generated for this fault indicator condition.
Status	Fix. Intel plans to correct this issue with a IMM BMC Firmware Update. All IMM BMC firmware release prior to and including rel 47 will have this issue.

13 Silk screen for onboard SCSI Channels denote the internal SCSI connector as Channel A and the external SCSI connector as Channel B. However, LSI firmware recognizes them in opposite order

Problem	The SE7520JR2 Technical Product Specification (TPS) and onboard silk screen identify the internal SCSI connector as SCSI Channel A and the external SCSI connector as SCSI Channel B. However, during system boot, the onboard LSI SCSI Controller firmware identifies these channels in opposite order.
Implication	With SCSI devices present on both connectors, the device boot order may not be what is expected.
Workaround	Manually enter the LSI Setup Utility and force the controller to recognize the channels in opposite order.
Status	No Fix. At this time LSI does not plan to correct this condition.

14 Blinking Green Status LED Associated with FRUSDR 6.6.8 and Earlier on S7520JR2ATAD2 Server Boards

Problem	SE7520JR2ATAD2 (PBA versions C53659-402 or later) server boards utilizing the Intel [®] Management Module (IMM) Advanced Edition or Professional Edition in a SR1400, SR1450 or SR2400 chassis may exhibit a blinking green system status LED. The System Event Log does not indicate a degraded system condition.
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As stated in the Intel[®] Technical Product Specification (TPS) for the SE7520JR2 server board, a blinking green light indicates the system is ready but in a degraded condition due to CPU, memory or power supply issues.

In addition, a blinking green LED may also indicate a degraded SCSI channel condition.

Implication	The system status LED may be blinking green indicating a degraded system configuration that does not exist.
Workaround	None.
Status	Fixed. This issue has been corrected in FRUSDR 6.6.A and later.

IV. Documentation Changes

1 SATA drive activity LED is driven by both the backplane controller and the Hard Drives

Problem In section 4.4.3 of Intel Server Chassis SR2400 Technical Product Specification (TPS) and section 4.4.2.1.6 of Intel Server Chassis SR1400 Technical Product Specification (TPS), the second sentence of the first paragraph will be updated as “The LED on the SATA backplane is driven by both the backplane GEM424 controller and SATA drives themselves using pin 11 on the connector. Therefore systems with newer SATA drives supporting pin 11 can support drive activity regardless of what SATA controller is used.”

Implication If using the onboard SATA controller of the baseboard, the Hard Drive will determine if Activity LED is supported. Only newer SATA drives will have Pin 11 enabled to support drive activity monitoring. No drive activity will be displayed on the Activity LED if using older SATA drives.

Status Doc. This will be added in a future release of Intel® Server Board SE7520JR2 TPS.

2 Incorrect description of 50-pin front panel connector as J1J2

Problem Table 92, page 190 of Intel® Server Board SE7520JR2 Technilcal Product Specification (TPS) 1.0 labels the 50-pin front panel connector as J1J2. It should state J1J1 as the proper reference.

Implication Misleading reference.

Status Doc. This will be corrected in a future release of Intel® Server Board SE7520JR2 TPS.

3 Incorrect pin assignment for table 90 “OEM RMC Connector Pinout (J3B2)”

Problem Table 89, page 187 of Server Board SE7520JR2 Technilcal Product Specification (TPS) 1.0 shows an inaccurate pin assignment for the J3B2 connector. The table should be as follow:

Table 90: OEM RMC Connector Pinout (J3B2)

Pin	Signal Name	Description
1	PERIPH_I2C_3VSB_SDA	
2	GROUND	
3	PERIPH_I2C_3VSB_SCL	
4	5V_STBY	
5	POST_STATUS	
6	ICH5_SYS_RST_L	
7	+5V	
8	FP_PWR_BTN_RMC	

Implication Misleading reference.

Status Doc. This will be corrected in a future release of Intel® Server Board SE7520JR2 TPS.

4 Incorrect measurement for table 1 “Chassis Dimentions” on TPS

Problem Table 1, page XX of Intel® Server Chassis SR2400 Technilcal Product Specification (TPS) 1.1 shows inaccurate measurements for the chassis dimensions table. The table should be as follow:

Table 6. Chassis Dimensions

Height	87.5 mm	3.445”
Width	430 mm	16.930”
Depth	672 mm	26.457”
Max. Weight	27.22 kg	60 Lbs

Implication Misleading reference.

Status Doc. This will be corrected in a future release of Intel® Server Chassis SR2400 TPS.

5 Power module must be inserted into the top slot of the power module enclosure in single power module configuration

Problem Section 2.2 of Intel® Server Chassis SR2400 Technilcal Product Specification (TPS) 1.0 states the wrong power module population rule in single power module configuration. In single power module configuration, the power module must be inserted into the top slot of the power module enclosure. The section 2.2 will be updated as “In single power module configurations, the power module must be inserted into the top slot of the power module enclosure. System and Power Supply thermals are not affected, however the nonoperating slot must have the power supply blank installed.”

Implication If the power module is inserted into the bottom slot in single power module configuration, the system status LED may be blinking green indicating a degraded system configuration that does not exist.

Status Doc. This will be corrected in a future release of Intel® Server Chassis SR2400 TPS.

6 Memory error handling mechanism in BIOS is changed

Problem The implementation of the memory error handling mechanism has been changed since production BIOS P07. So the section 6.2.2 of Intel® Server Board SE7520JR2 Technilcal Product Specification (TPS) 1.0 will be updated as below.

The expected error rates for DIMMs come from three sources: Intel experimental measurements, data from a memory component vendor, and the results from a 10 year study by a major computer manufacturer. The three respective error rates are all stated per GB of memory: 1.5 errors per year, about 1 error per month, and 4 per month. Since the lowest error rate was gathered over a relatively short time, and the highest error rate was gathered over a relatively long time, these two numbers are being thrown out. The middle error number, which is perceived as being a more accurate conservative estimate, will be used for purposes of programming the threshold registers for single bit correctable memory errors or SECs. This number must be adjusted for geographical areas of increased occurrence of alpha particles, which will increase error rates; such as high altitude or radioactive mineral deposits. Past studies have shown that single bit error rates at altitudes as low as 10,000 feet are 14 times higher than at sea level due to increased cosmic ray exposure. The highest of the three quoted error rates included various geographical locations.

Table 4-24 shows suggested settings for different DIMM sizes. The values shown are with minimal error residue at 1X the expected average error rate. Halving the time or threshold would result in loss of error count resolution. One register is programmed for each DIMM slot.

Table 4-24. Suggested Prescale Settings

DIMM Size	SPARECTL SEC Prescale Value	SPARECTL SEC Prescale Unit	Thresh_SEC Count on a per DIMM Basis
128 MB	128	7h = week	4
256 MB	64	7h = week	4
512 MB	32	7h = week	4
1 GB	16	7h = week	4
2 GB	8	7h = week	4
4 GB	4	7h = week	4

So even in non-RAS mode the chipset counter is still used to define how many SBEs can occur on each individual DIMM and the counter for that DIMM is also dependant on the DIMM size.

Here are the resulting threshold values based on the DIMM size...

DIMM Size	Threshold value
64M	4
128M	4
256M	4 x 2
512M	4 x 4
1G	4 x 8
2G	4 x 16
4G	4 x 32

If the SBE count that occurs on a DIMM is over the corresponding threshold, then the DIMM Faulty LED will be lit, and the SBE logging and detection will be disabled, and the DIMM will be taken off-line by BIOS.

Setting the “Memory Retest” option to “Enabled” in BIOS Setup will bring all DIMM(s) back on-line regardless of current states.

Implication Misleading reference.

Status Doc. This will be corrected in a future release of Intel® Server Board SE7520JR2 TPS.

7 3-pin cable in SR1450 SATA Backplane Kit is not used with the onboard SATA controller

Problem In page 63 – 65 of Intel® Server Chassis SR1450 User Guide, there is lack of documentation of the usage of a 3-pin cable in the SR1450 SATA Backplane Kit.

The following paragraph will be added to clarify its usage. “The SR1450 SATA Backplane Kit (Product Code: A1450SATAKIT, MM#: 869353) contains a 3-pin cable (Intel Part#: C37205-001) that is used to connect to the SATA Backplane at header location (J7A1) and a 3rd party add-in SATA card. This cable provides hard drive LED activity indication to the hard drive carriers. This cable is not used with the SE7520JR2 onboard SATA controller. “

Implication	The cable may be mis-used to connect the baseboard and the SATA backplane.
Status	Doc. This will be corrected in a future release of Intel® Server Chassis SR1450 User Guide.

V. FYI – Useful Information

This section is included to provide users with answers to commonly asked questions/issues with the specified products. Additional entries can be viewed at the “Known Issues and Solutions” area at the following Intel web site: <http://support.intel.com/support/motherboards/server/se7520jr2/>

1 Onboard CTRL <C> RAID 0, 1 creation appears to be slow and appears to limit the number of RAID configurations.

Description Initializing a RAID 1(mirror) using the BIOS (CTRL-C) utility will take approximately 1 hour per 5GB of drive space. There is also a limitation of one logical drive per controller.

Implication For optimal performance the mirror must finish initialization before rebooting the system or attempting to install the operating system on the mirror (though this is not required). Typically, 1 hour for each 5Gigabytes of hard drive capacity is required to complete initializing the mirror when using the onboard CTRL <C> application. For example, for two 70Gigabyte drives configured in a RAID 1 mirror, 12-14 hours should be allowed for the initialization to complete. Adding a 3rd drive configured as a “hot spare” will increase the time required to complete the mirror initialization.

Workaround For mirrored drives that will not hold the bootable operating system, create the RAID 1 configuration at the operating system level or use an Intel based RAID card for better performance. For mirrored drives that will hold the bootable operating system, configure the mirror using the CTRL-<C> bios utility and allow enough time for the mirror to complete initialization before rebooting the system. You will be limited to one RAID configuration per controller and you can not create a RAID configuration across controller channels (cables). In other words, if you have two onboard SCSI channels (cables) as with the I Intel® server Board SE7520JR2 SCSI you will only be able to create one RAID (0 or 1) configuration on one of the channels. For more details on the onboard controller please refer to the “LSI Integrated RAID User’s Guide” posted at <http://support.intel.com>

2 BIOS will display a warning message when the mBMC System Event Log (SEL) is full

Description During boot, the BIOS may briefly display a red warning message indicating that the System Event Log (SEL) is full. This message appears after multiple reboots, due to the limited SEL storage space of the On-Board Platform Instrumentation. The SEL storage space of the mBMC allows for the storage of 92 SEL entries. A typical reboot adds several informational event messages to the SEL as part of the normal boot process.

Implication The red warning message displayed by the BIOS is not an error. It is a warning message that the SEL is full and that no more system event messages can be logged until the SEL is cleared.

Workaround The System Event Log (SEL) of the On-Board Platform Instrumentation should be cleared regularly. There are several methods of clearing the SEL, including:

BIOS Setup (F2), SEL Viewer (included on the Intel Server Deployment Toolkit + the Software Update Package), and Intel Server Management 8.x (ISM) which includes the capability to manually manage the SEL as well as the capability to configure ISM to automatically clear the SEL when it reaches a user defined threshold. Mirrored

3 ID Button/LED functionality with no Intel Management Module (IMM)

Description With no IMM present, the ID LED will blink 15 times and turn off when the ID Button on the Control Panel is pressed.

Implication If the system is not identified within 30 seconds of pressing the ID Button, the ID LED will turn off

Workaround None

4 mBMC doesn't log the "AC Lost" event when AC power is lost.

Description mBMC does not record an "AC lost" event to the System Event Log (SEL) when AC power is lost.

Implication IPMI defines that the AC power lost event should be logged to SEL. But the mBMC used on Intel® Server Board SE7520JR2 -- NS87413C doesn't support this event logging.

Workaround None

5 Changing BIOS Setup options "Adjacent Cache Line Prefetch" and "Hardware Prefetch" from factory defaults may alter system performance.

Description Starting in system BIOS P07, the <F2> BIOS Setup Utility included options to Enable/Disable "Adjacent Cache Line Prefetch" and "Hardware Prefetch" features.

Implication Depending on the application software and OS installed on the system, changing these options from their factory default may enhance or degrade system performance.

Workaround If measured system performance is not meeting expectations, one option would be to go into <F2> BIOS setup and change one or both of these settings. These options should only be changed by persons with system performance tuning knowledge. Having these options set incorrectly may noticeably degrade the performance of the system. Intel's default settings for these two options may or may not be optimized for a given system operating environment.

6 SR2400 PCI-X Riser Card Add-in Card Population Rules

Description	In order to maintain signal integrity of the PCI-X buses on the Intel Server Board SE7520JR2, add-in card population rules must be followed when using the Low Profile PCI-X Riser card and the Full Height PCI-X (Passive) Riser card for the Intel Server Chassis SR2400. When using either of these two riser cards, add-in cards must be populated starting with the top PCI slot for a single add-in card. Additional cards should then be populated using the next open slot down from the top.
Implication	If the add-in card population rules for the Low Profile PCI-X and Full Height PCI-X (passive) riser card are not followed, the system BIOS will display an error message during boot up, and will halt POST until the add-in cards are configured properly.
Workaround	There is no workaround for the add-in card population rules when using the Low Profile PCI-X and Full Height PCI-X (passive) riser cards of the Server Chassis SR2400 with the Server Board SE7520JR2. However, the other two full height riser cards available for this platform, PCI-X (Active) and PCI-E, do not require specific population rules.

7 Required Steps When Installing an Intel Management Module (IMM) into a server

Description	When installing an Intel Management Module (IMM) Professional or Advanced Editions, into a server, the following two steps should be performed before installing any Server Management Software: <ol style="list-style-type: none">1. Upgrade the IMM BMC firmware to the latest available version (Recommended)2. Run the latest FRUSDR Utility (Required)
Implication	Failure to perform the two steps listed can cause the management features of the system to operate erratically and/or report false management errors to the System Event Log (SEL).