SE7320VP2 and SE7320VP2D2 Server Board

SR1435VP2 and SR1435VP2D2 Server Platform

SR1400LC Server Chassis

Specification Update

Intel Order Number C98464-005

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Enterprise Platforms and Services Marketing

Revision History

Date	Modifications
December 2004	Initial release based on the “Intel® Server Board SE7320VP2 Technical Product Specification”, “Intel® Server Platform SR1435VP2 Technical Product Specification” and “Intel® Server Chassis SR1400LC Technical Product Specification”.
January 2005	Added “BIOS will report warning message when SEL is full” issue.
February 2005	Added “BMC Timestamp Erratum” issue.
March 2005	Added “Marvell NIC LED is off under S5” issue.
May 2005	Removed document changes, as they were corrected in the *Intel Server Board SE7320VP2 Technical Product Specification Revision 2.0.* Added “Processor Hot & Throttling event are not logged in SEL” issue.
July 2005	Updated “Processor Hot & Throttling event are not logged in SEL” issue. Added SE7320VP2D2 and SE1435VP2D2 product.
August 2005	Added “Upper Non-Critical (UNC) event is triggered on some SR1435VP2 systems” issue
October 2005	Updated “Processor Hot & Throttling event are not logged in SEL” issue and “Upper Non-Critical (UNC) event is triggered on some SR1435VP2 systems” issue
February 2006	Added SE7320VP2 DDR2 RoHS compliant board and RoHS compliant statement

Disclaimers

The Server Board SE7320VP2 and SE7320VP2D2, Server Platform SR1435VP2 and SR1435VP2D2, and Server Chassis SR1400LC may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

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Preface

This document is an update to the product definition specified in the *Intel Server Board SE7320VP2 Technical Product Specification, and Server Platform SR1435VP2, Server Chassis SR1400LC Technical Product Specifications* (Order Number C91056-002, and C86755-001). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain specification changes, specification clarifications, errata, and document changes.

Refer to the *Intel® Xeon™ Processor with 800MHz System Bus Specification Update* (Document Number 302402-012) for specification updates concerning the Xeon™ processor with 800MHz System Bus. Items contained in the *Xeon™ Processor with 800MHz System Bus Specification Update* that either do not apply to the Server Board SE7320VP2, SE7320VP2D2 or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

- **Specification Changes** are modifications to the current published specifications for the Server Board SE7320VP2 and SE7320VP2D2, Server Platform SR1435VP2 and SR1435VP2D2, Server Chassis SR1400LC. These changes will be incorporated in a future release of the given document.

- **Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in a future release of the given document.

- **Documentation Changes** include typos, errors, or omissions from documents that are currently published. These documents may include Product Specs and Users Guides. These changes will be incorporated in a future release of the given document.

- **Errata** are design defects or errors. Errata may cause the Server Board SE7320VP2 and SE7320VP2D2, Server Platform SR1435VP2 and SR1435VP2D2, Server Chassis SR1400LC's behavior to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

Product Scope

Below are the specific boards, BIOS and components covered by this.

Baseboard Fab #	Baseboard PBA #	BIOS Revision / Build #	Mbmc Revision	FRU/SDR
FAB 6	C63184-603	P01	2.40	1.10
FAB 6	C63184-604	P02	2.40	1.30
FAB 6	C63184-605	P03	2.40	1.50
FAB 7	C63184-701	P05	2.40	6.6.H(1.70)
FAB 2	D10582-202	P04	2.40	6.6.H(1.70)
FAB 3	D10582-250	P07	2.40	6.6.K(2.00)

Summary Tables of Changes

The following tables indicate the errata and the document changes that apply to the Intel Server Board SE7320VP2 and SE7320VP2D2, Server Platform SR1435VP2 and SR1435VP2D2, Server Chassis SR1400LC. Intel intends to fix some of the specified errata in future updates to the server board and chassis. Documentation changes will be made in future updates to the given document. The tables use the following notations:

Doc:	Intel intends to update the appropriate document in a future revision.
Investigating	Intel is investigating the issue.
Fix:	Intel intends to fix this erratum in a future update of the board or chassis.
Fixed:	This erratum has been addressed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or has been modified from the previous specification update.

Table 1. Errata Summary

No.	Plans	Description of Errata
1.	NoFix	Front panel switch inhibit
2.	NoFix	Unable to boot from Maxtor USB hard drive
3.	NoFix	Reading FRUSDR information in BIOS setup menu takes about 7 seconds
4.	Investigating	WOL(Wake On LAN) function does not operate with the Marvell* Onboard NIC
5.	NoFix	The Activity/Fault LED's on the Drive Carriers do not operate using the Onboard SATA Controller and the SATA backplane
6.	NoFix	BIOS will display a warning message when the mBMC System Event Log (SEL) is full
7.	Fix	BMC Timestamp Erratum
8.	NoFix	Marvell NIC LED is off under S5 state
9	Fixed	Processor Hot & Throttling event are not logged in SEL
10	Fixed	Upper Non-Critical (UNC) event is triggered on some SR1435VP2 systems

Table 2. Documentation Changes

No.	Plans	Description of Documentation Change
1.		Add RoHS compliant statement to Product Regulatory and Certification Chapter

Following are in-depth descriptions of each erratum / documentation change indicated in the tables above. The errata and documentation change numbers below correspond to the numbers in the tables.

Errata

1. Front panel switch inhibit

Problem System can't shutdown or reset using the front panel Power and Reset switches in secure mode when "Front Panel Switch Inhibit" set to disabled.

Implication Power and reset switches on front panel are disabled in secure mode.

Workaround None.

Status No Fix. When Secure mode is activated, the front panel Power and Reset switches will be locked out. The Power Switch and the Reset Switch will both be disabled.

2. Unable to boot from Maxtor USB hard drive

Problem The system is unable to detect Maxtor USB hard drives in Windows* 2003 Server* Operating System. The Hard Drive is detected by the system during the Power On Self Test, and the user is able to format the drive with system files, but unable to boot to it.

Implication The Operating System that installed on the USB hard drive can not be set as the primary boot device.

Workaround None.

Status No Fix. As of April 2003, the official Microsoft* policy was as follows: "Recommendations for Booting Windows* from USB Storage Devices. Current versions of Windows* should not be installed to USB hard disk drives because Windows* does not support USB hard disk drives as the primary boot device." (from Microsoft* White Paper)

3. Reading FRUSDR information in BIOS setup menu takes about 7 seconds

Problem It will take approximately 7 seconds to read the FRUSDR Data from the mBMC in the BIOS Setup Utility. This option is available in the “Server→ System Management” section in BIOS Setup.

Implication The system may appear to be hung during the period of time when the mBMC is providing FRUSDR information.

Workaround None.

Status NoFix. The SE7320VP2 uses the SMBus to communicate with the mBMC to obtain FRUSDR information. Because the mBMC provides a low-speed interface, the user will need to wait for approximately 7 seconds to obtain FRUSDR information from the mBMC.

4. WOL(Wake On LAN) function does not operate with the Onboard Marvell* NIC

Problem If the “Wake from Standby” option is set to enabled for the onboard Marvell* Network Interface Controller (NIC) in Windows* 2003 or 2000 “Device Manager”, the system will not wake when it receives LAN activities.

Implication The WOL (Wake On LAN) function will fail to operate on the Marvell* PCI-E based NIC.

Workaround None.

Status This issue is under Investigation.

5. The Activity/Fault LED’s on the Drive Carriers do not operate using the Onboard SATA Controller and the SATA backplane

Problem The Activity/Fault LED’s on the Chassis Hard Drive Carriers will not function using the Server Board SE7320VP2 Onboard SATA Controller with the SR1400LC SATA Backplane. The Front Panel Hard Drive Activity LED will funtion as expected.

Implication The Hard Drive activity/fault status LED’s do not function and provide status indication.

Workaround None.

Status No Fix. To light the LED’s on the Hard Drive Carriers, the SATA controller must support the SAF-TE protocol over an I2C bus. The 6300ESB ICH SATA RAID controller on the Server Board SE7320VP2 does not support this function. For more information, please refer to *Intel Server Chassis SR1400LC / Intel Server Platform SR1435VP2 TPS V1.0* (Order number 86755-001) on page 35.

6. BIOS will display a warning message when the mBMC System Even Log (SEL) is full

Problem During boot, the BIOS may briefly display a red warning message indicating that the System Event Log (SEL) is full. This message appears after multiple reboots, due to the limited SEL storage space of the On-Board Platform Instrumentation. The SEL storage space of the mBMC allows for the storage of 92 SEL entries. A typical reboot adds several informational event messages to the SEL as part of the normal boot process.

Implication The red warning message displayed by the BIOS is not an error. It is a warning message that the SEL is full and that no more system event messages can be logged until the SEL is cleared.

Workaround The System Event Log (SEL) of the On-Board Platform Instrumentation should be cleared regularly. There are several methods of clearing the SEL, including: BIOS Setup (F2), SEL Viewer (included on the Intel Server Deployment Toolkit + the Software Update Package), and Intel Server Management 8.x (ISM) which includes the capability to manually manage the SEL as well as the capability configure ISM to automatically clear the SEL when it reaches a user defined threshold.

Status No Fix. Intel has no plans to increase the SEL capacity of the On-Board Platform Instrumentation beyond the current 92 entries.

7. BMC Timestamp Erratum

Problem The Intel® Server Board SE7320VP2 has been found to have a BIOS erratum which causes the BMC timestamp information to be incorrect. Beginning on January 1, 2005, the BMC date will lag the system date by 1 day throughout 2005. It will return to the correct date in 2006. This will recur for each year that follows a leap year, i.e. 2009, 2013, etc.

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Implication The effect of this erratum is that the BMC will use this incorrect date for all entries in the System Event Log (SEL) maintained by the BMC. This includes informational events as well as error events, e.g. memory error events. Other BMC functions are unaffected.

Workaround None.

Status This issue will be fixed in the next revision of the Intel Server board SE7320VP2 quarterly BIOS release, version P03.

8. Marvell NIC LED is off under S5 state

Problem When system is power down, there will be no LED lighting on Marvell NIC port.

Implication Although a standby power is added to Marvell NIC, the port LED will not be lit.

Workaround None.

Status There will be no fix for it. SE7320VP2 does not support WOL under S5 state. If the system runs Microsoft* Windows Server 2003, together with Marvell driver v7.24 or later, then Marvell LED is off under S5 state as default.

9. Processor Hot & Throttling event are not logged in SEL

Problem The Intel® Server Board SE7320VP2 has been found to have an issue where the VRD Thermal Monitor, Processor Hot & Throttling events are masked and not passed to the system Baseboard Management Controller (BMC) for event monitoring and logging.

Implication Even though the processors will throttle in the event of a high temperature condition, this will not be recorded in the system event log or monitored via Intel Server Management. In the unlikely event, the processor temperature increases and exceeds the thermal trip point of the processors, the system will perform a shutdown operation and generate the appropriate system event log entry.

Workaround None.

Status This issue has been fixed in the SE7320VP2 PBA# C63184-701 SKU board.

10. Upper Non-Critical (UNC) event is triggered on some SR1435VP2 systems

Problem The “Voltage #0x0E Upper Non-critical – going high” event is logged in SEL of some SR1435VP2 systems.

Implication This implies the baseboard +5V input Upper Non-Crtical threshold has been reached. When this event is triggered, the system status LED will blink.

Workaround None

Status This issue has been fixed in FRUSDR 6.6.I (1.80)

Documentation changes

1. Add RoHS compliant statement to Product Regulatory and Certification Chapter

Problem: SE7320VP2 DDR2 SKU board will be RoHS compliant. Add below statement to Product Regulatory and Certification Chapter

> "Restriction of Hazardous Substances (RoHS) Compliance: Intel has a system in place to restrict use of banned substances per in accordance to the European Directive 2002/95/EC. Compliance is based on materials banned in the RoHS Directive are either (1) below all applicable substance threshold limits or (2) an approved/pending RoHS exemption applies. (Note: RoHS implementing details are not fully defined and may change.) Threshold limits and banned substances are noted as follows:
> Quantity limit of 0.1% by mass (1000 PPM) for: Lead; Mercury; Hexavalent Chromium; Polybrominated Biphenyls Diphenyl Ethers (PBDE); and Quantity limit of 0.01% by mass (100 PPM) for Cadmium"

Implication: None

Status: This will be corrected in a future Server Board SE7320VP2 TPS release.