Intel® Server System SR1690WB

Technical Product Specification

Intel order number: E72797-008

Revision 1.6

January, 2011

Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
July 4, 2009	1.0	Initial release.
August 8, 2009	1.1	Changes on PSU cables and onboard SATA port numbering.
September 22, 2009	1.2	HDD LED status updated and added optional chassis rail kit.
March 15, 2010	1.3	Updated the supported processor list.
March 18, 2010	1.4	Removed CCC certificates.
November 10, 2010	1.5	Updated iBMC memory size.
December 30, 2010	1.6	Updated LAN IOAT2 support.

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Table of Contents

List of Figures

List of Tables

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1. Introduction

This Technical Product Specification (TPS) provides system specific information detailing the features, functionality, and high-level architecture of the Intel® Server System SR1690WB. You should also reference the *Intel® Server Board S5500WB Technical Product Specification* to obtain greater detail of functionality and architecture of the server board integrated in this server system.

In addition, you can obtain design-level information for specific sub-systems by ordering the External Product Specifications (EPS) or External Design Specifications (EDS) for a given sub-system. EPS and EDS documents are not publicly available. They are only made available under NDA with Intel and must be ordered through your local Intel representative. For a complete list of available documents, refer to the *Reference Documents* section at the end of this document.

The Intel® Server System SR1690WB may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Refer to the *Intel® Server Board S5500WB/Intel® Server System SR1690WB Specification Update* for published errata.

1.1 Chapter Outline

This document is divided into the following chapters:

- Chapter 1 – Introduction
- Chapter 2 – Product Overview
- Chapter 3 – Power Sub-System
- Chapter 4 – Cooling Sub-System
- Chapter 5 – Peripheral Driver Support
- Chapter 6 – Hard Disk Driver Support
- Chapter 7 – Front Panel Control and Indicators
- Chapter 8 – Configuration Jumpers
- Chapter 9 – PCI Riser Card and Assembly
- Chapter 10 – Environmental and Regulatory Specifications
- Appendix A – Integration and Usage Tips
- Appendix B – POST code LED Decoder
- Appendix C – Video POST Code Errors
- Appendix D – Jumper Block Settings and Usage
- Glossary
- Reference Documents

1.2 Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Overview

The *Intel® Server System SR1690WB* is a rack mount 1U server system, purpose-built for high-energy efficiency and lowest total cost of ownership in dense computing applications. The system is integrated with an *Intel® Server Board S5500WB* and supports up to four hot-swap SAS or SATA hard drives.

This chapter provides a high-level overview of the system features. The following chapters provide greater detail for each major system component or feature.

Table 1. System Feature Set

Feature	Description
Raw Storage Capacity	System raw storage capacity is based on the HDD capacity and number of HDDs used in the system. Raw storage capacity is the sum of single HDD capacity used in system. For example: if four 1 TB HDDs are used in system, the system raw storage capacity is 4.0 TB
External Drive Bays	Four hot-pluggable external drive bays
Hard Disk Drive Supported	3.5-inch SATA, SAS HDD. 2.5-inch SATA, SAS HDD.
Processor	Support for one or two Intel® Xeon® Processor 5500 series and Intel® Xeon® Processor 5600 series processors in FC-LGA 1366 Socket B package with up to 95 W Thermal Design Power (TDP) . Supports future processor compatibility guidelines 4.8 GT/s, 5.86 GT/s, and 6.4 GT/s Intel® Quick Path Interconnect (Intel® QPI). Meets EVRD11.1
Memory Capacity	Expandable to 64 GB maximum.
Memory Type	240-pin keyed support for 800/166/1333 MT/s ECC Registered (RDIMM) or Unbuffered (UDIMM) DDR3 memory. 8 DIMMs total across six memory channels (three channels per processor in a 2:1:1 configuration). No support for Quad-Rank x4 DIMMs.
DIMM Slots	Eight
Chipset	Intel® Chipset which includes the following components: Intel® 5500 chipset IOH（IOH24D） Intel® 82801Jx I/O Controller Hub (ICH10R)
System Connectors /Headers	External I/O connectors: • DB-15 Video connectors • RJ-45 serial Port A connector • RJ-45 connector for 10/100/1000 LAN • One 2x USB 2.0 connectors • One RJ-45 over USB for 10/100/1000 LAN Internal connectors/headers: • Two USB 2x5 pin header, supporting up to four USB 2.0 ports • One low-profile USB 2x5 pin • One DH-10 Serial Port B header • One 2x8 pin VGA header with presence detection to switch from rear I/O video connector • Six SATA II connectors • Dual Connectors for Intel® I/O Expansion Module • One RMM3 connector to support optional Intel® Remote Management

Feature	Description
	Module 3 • SATA SW RAID 5 Activation Key Connector • One SSI-EEB compliant front panel header
System Fan Support	Two sets of CPU fans Two sets of DIMM fans
Add-in Adapter Support	Intel® Server Board S5500WB SSI-compliant One riser slot supporting full-height or low-profile 1U and 1U MD2 PCI Express* x16 riser cards. Two connectors supporting double- and single-wide Intel® I/O Expansion Modules.
On-board Video	On-board Server Engines* LLC Pilot II Controller Matrox* G200 2D Video Graphics controller Uses 8 MB of the BMC 64 MB DDR2 Memory
LAN Support	Two 10/100/1000 ports provided by Intel® 82576 with Intel® I/O Acceleration Technology 2(I/OAT)
System Power	Single 650-W power supply, 80 plus silver with PFC
System Management	On-board Server Engines* LLC Pilot II Controller. Integrated Baseboard Management Controller (Integrated BMC), IPMI 2.0 compliant Basic • BMC Controller: ARC 926E-S microcontroller • Super IO: Serial Port logic, legacy interfaces, LPC interface, Port80 • Hardware Monitoring: Fan speed control and voltage monitoring Advanced • Video and USB compression and redirection • NC-SI port, a high-speed sideband management interface • Integrated Super I/O on LPC interface

The Intel® Server System SR1690WB system is supporting all Intel® Xeon® 5500 series and 5600 series processors with TDP 95 W and below. You can find a full list of supported processors at the Intel Support Website http://www.intel.com/support/motherboards/server/S5500WB/sb/CS-030205.htm.

2.1 System Views

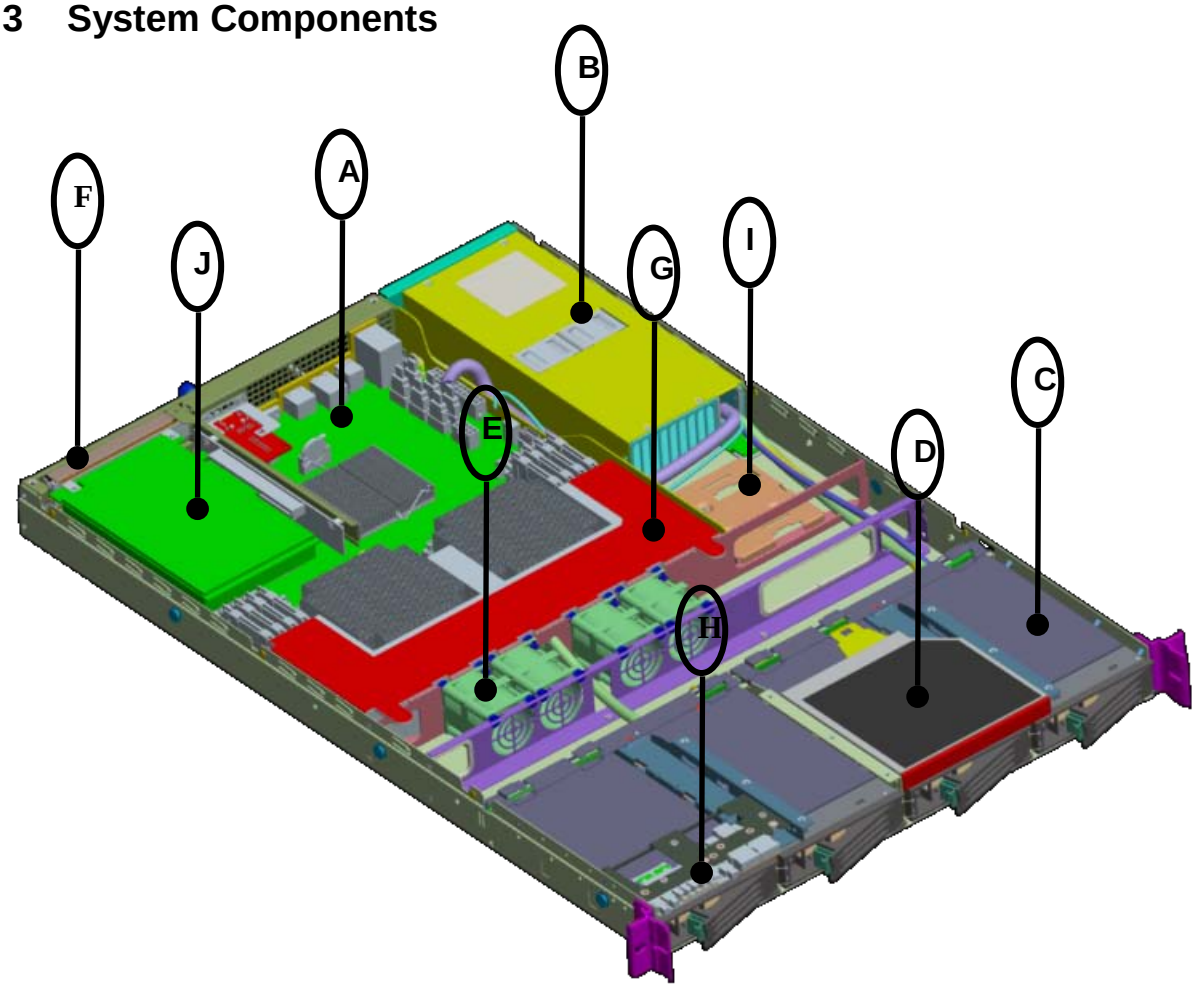
Figure 1. System Overview (HDD and Memory DIMMs are not included in package)

2.2 System Dimensions

Table 2. Chassis Dimensions

Height	43 mm	1.69 inches
Width without rails	451.17 mm	17.76 inches
Width with rails	482 mm	18.97 inches
Depth without CMA	671.08 mm	26.42 inches
Weight Chassis – basic configured (0 drives) Chassis – fully configured (4 drives)	 11.15 kg 13.32 kg	 24.58 lbs 29.27 lbs

2.3 System Components



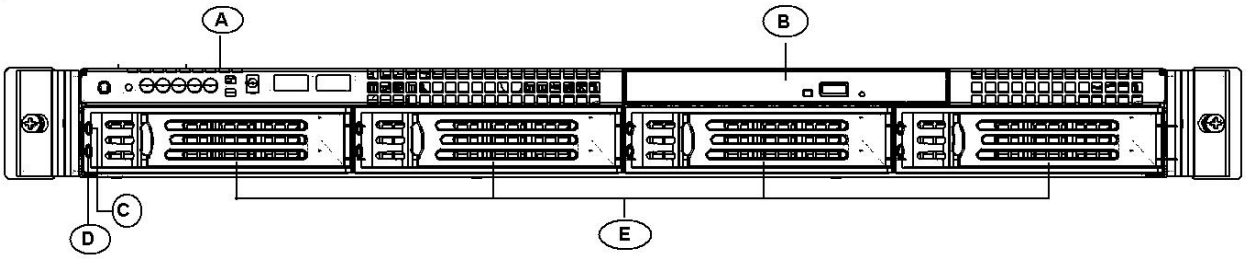
A	Mother Board	F	1U Chassis
B	Power Supply Module	G	Air Duct
C	External hot-swap HDD Carriers	H	Front Panel and Front USB module
D	Slim-line Optical Drive	I	Optional BBU3 Assembly Position
E	System Fans Module	J	Optional PCI Express* Add-in Card

Not shown: Rack slide rail, front bezel, and top cover.

Figure 2. Major Chassis Components

2.4 Hard Drive and Peripheral Bays

Device	Intel® Server System SR1690WB
Slim-line SATA Optical Drive	Supported
Slim-line USB Floppy Drive	No Support
SATA Drives (3.5-inch or 2.5-inch)	Up to four
SAS Drives (3.5-inch or 2.5-inch)	Up to four



A	System Control Panel
B	Slim-line drive bay
C	HDD Power LED
D	HDD Activity/Fault LED
E	Hard drive bays 0~3

Figure 3. Drive Bay Overview

2.5 Server Board Overview

The chassis is mechanically and functionally designed to support the Intel® Server Board S5500WB SSI-compliant. The following sections provide an overview of the server board feature sets.

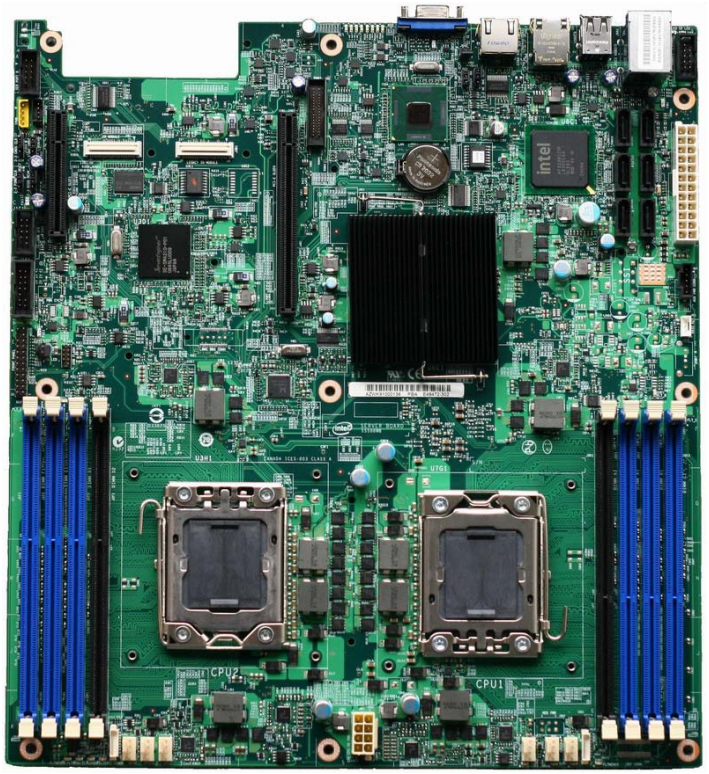


Figure 4. Intel® Server Board S5500WB SSI-compliant

The following figure shows the layout of the server board. Each connector and major component is identified by a number or letter, and a description is given below the figure.

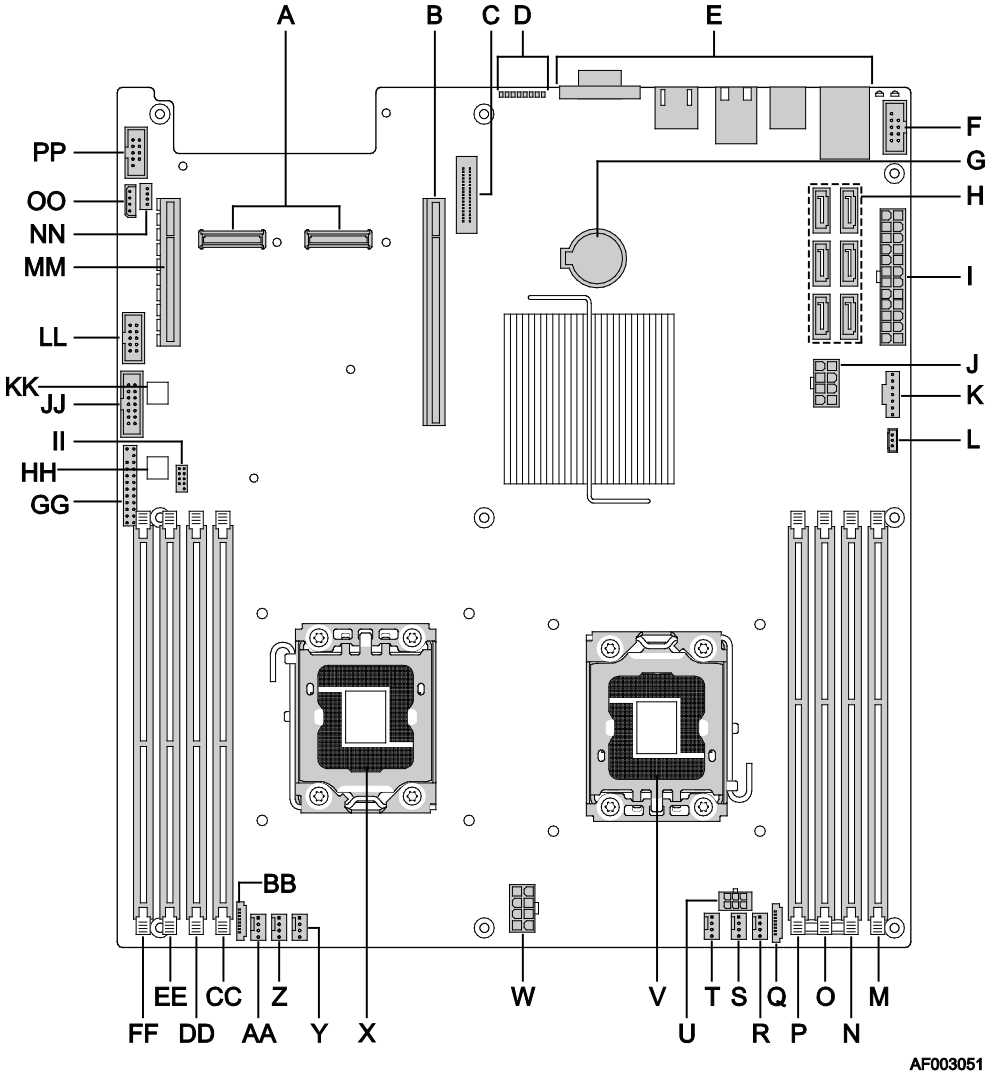
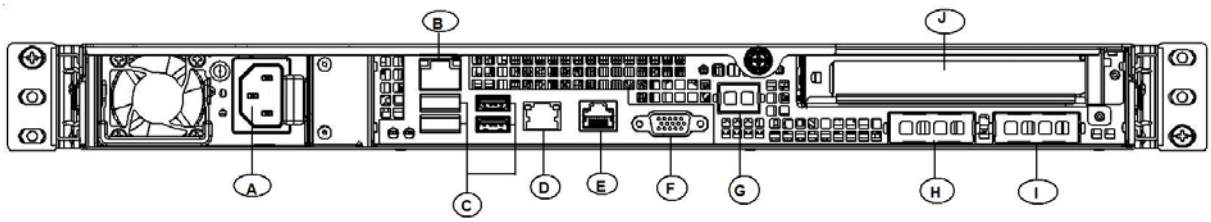


Figure 5. Intel® Server Board S5500WB SSI Components

	Description		Description
A	Dual Intel® I/O Expansion Module Connectors	V	Processor Socket 1
B	PCI Express* x16 Gen2	W	8-pin CPU Connector
C	Remote Management Module 3	X	Processor Socket 2
D	POST Code LEDs	Y	4-pin Fan Connector (CPU2)
E	External I/O	Z	4-pin Fan Connector (CPU2A)
F	USB Connector	AA	4-pin Fan Connector (MEM2)
G	Battery	BB	8-pin Fan Connector (MEM2R)
H	SATA Connectors 0~5	CC	DIMM Slot D2
I	24-pin Power Connector	DD	DIMM Slot D1
J	N/A	EE	DIMM Slot E1
K	Aux Power (5-pin or 7-pin)	FF	DIMM Slot F1
L	RAID Key	GG	Front Panel Connector
M	DIMM Slot C1	HH	HDD LED Header
N	DIMM Slot B1	II	Low-Profile USB Connector
O	DIMM Slot A1	JJ	Internal VGA Connector
P	DIMM Slot A2	KK	N/A
Q	8-pin Fan Connector (MEM1R)	LL	USB Connector
R	4-pin Fan Connector (MEM1)	MM	Slot 1 PCI Express* x8 Gen2

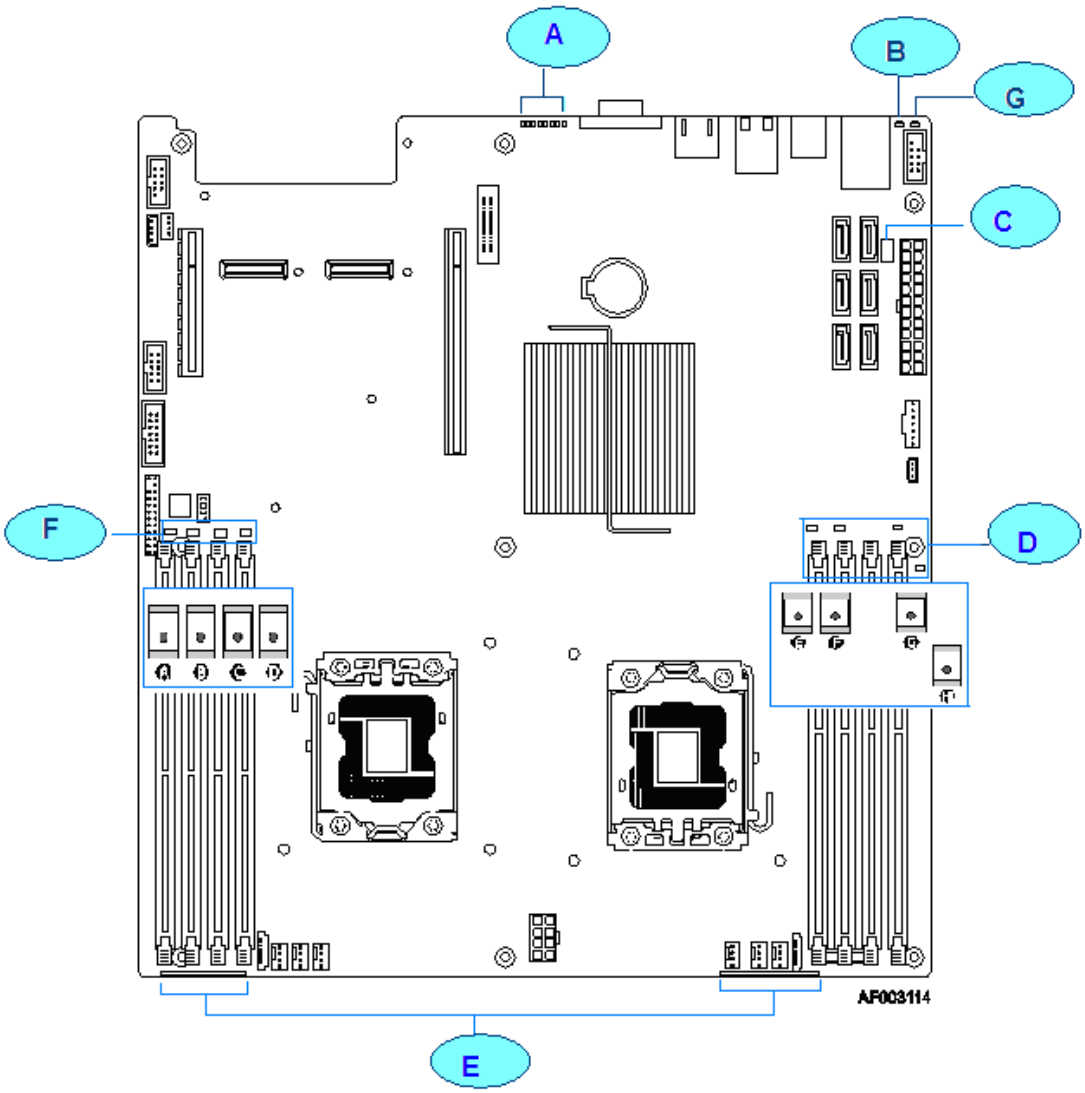
	Description		Description
S	4-pin Fan Connector (CPU1A)	NN	SGPIO Connector
T	4-pin Fan Connector (CPU1)	OO	IMPB Connector
U	N/A	PP	Serial Port B

Figure 6. Connector and Component Definitions



A	AC Power Receptacle	F	Video connector
B	NIC 1 connector	G	Management Network Interface (optional)
C	USB port 2, 5, 8, 9	H	IO module external connector 1 (optional)
D	NIC 2 connector	I	IO module external connector 2 (optional)
E	RJ-45 serial B port	J	Add-in card bracket (full height)

Figure 7. Back Panel Feature Overview



	Description		Description
A	Diagnostic LED	E	Fan Fault LED
B	System Status LED	F	CPU2 DIMM fault LED
C	5V Standby LED	G	System ID LED
D	CPU1 DIMM fault LED		

Figure 8. Light-Guided Diagnostic LED Locations

2.6 Rack and Cabinet Mounting Options

The chassis was designed to support 19 inches wide by up to 30 inches deep server cabinets. The system supports the following Intel rack mount options:

- A fixed mount relay rack/cabinet mount kit which you can configure to mount the system into either a 2-post rack or 4-post cabinet.
- A basic slide rail kit is designed to mount the chassis into a standard (19 inches by up to 30 inches deep) EIA-310D compatible server cabinet.
- A tool-less slide rail kit is designed to mount the chassis into a standard (19 inches by up to 30 inches deep) EIA-310D compatible server cabinet.

3. Power Sub-System

The system includes a 650-W power supply unit, which is 80 plus energy efficiency, demonstrating climate saver with silver rating.

3.1 Mechanism overview

The power supply will have a simple retention mechanism to retain the power supply once it is inserted. This mechanism shall withstand the specified mechanical shock and vibration requirements. The power supply module will be fixed on the chassis with screws.

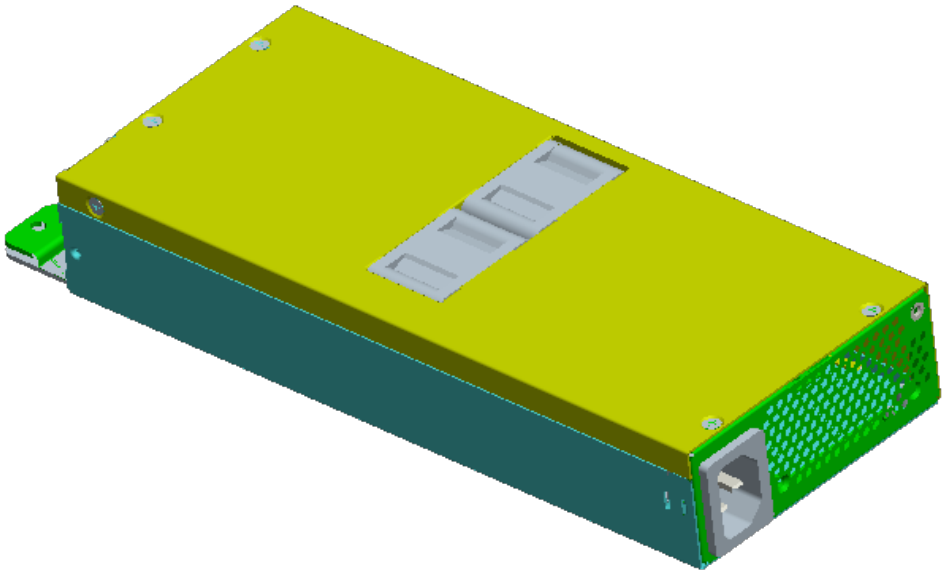


Figure 9. Power Supply Module Overview

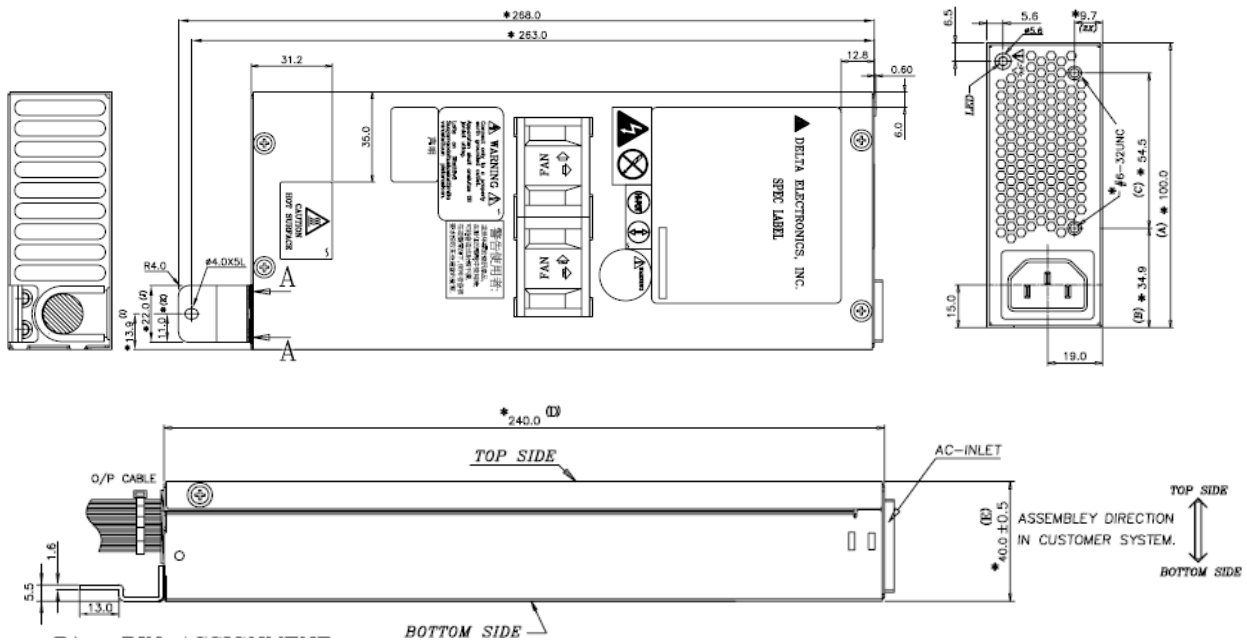


Figure 10. Power Supply Mechanical Drawing

3.2 Output connectors and Cable Harness

The power distribution board provides a cable harness for connectors to the various system boards. You can find the harness size, connectors (explained in the following table), and connectors' pin definitions in the power supply specification. Listed or recognized component appliance wiring material (AVL V2), CN, rated 105°C min, 300Vdc min shall be used for all output wiring.

Table 3. Cable Harness Definition

From	Length mm	To connector #	Number of pins	Description
Backplane cover exit hole	350	P1	2x12	Main power connector
Backplane cover exit hole	630	P2	2x4	Processor and memory power connector
Backplane cover exit hole	480	P3	2x2	Cable for Backplane power1
Backplane cover exit hole	270	P4	2x2	Cable for Backplane power2
Backplane cover exit hole	300	P5	1x5	Cable for PMBUS
Backplane cover exit hole	25	P6	1x4	CD/DVD drive SATA Power Connector

P1 – Main Power Connector

Connector housing: 24-Pin Molex* Mini-Fit Jr. 39-01-2245 or equivalent.

Table 4. P1 – Main Power Connector Pin-out

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	+3.3 VDC	Orange	13	+3.3 VDC	Orange
2	+3.3 VDC	Orange	14	-12 VDC	Blue
3	GND	Black	15	GND	Black
4	+5 VDC*	Red	16	PSON#	Green
5	GND	Black	17	GND	Black
6	+5 VDC	Red	18	GND	Black
7	GND	Black	19	GND	Black
8	PWR OK	Gray	20	Reserved	N.C.
9	5VSB	Purple	21	+5 VDC	Red
10	+12V3	Yellow/Blue Stripe	22	+5 VDC	Red
11	+12V3	Yellow/Blue Stripe	23	+5 VDC	Red
12	+3.3 VDC	Orange	24	GND	Black

Notes:

1. 5V Remote Sense Double Crimped into pin 4.
2. 3.3V Locate Sense Double Crimped into pin 2.

P2 – Processor and Memory Power Connector

Connector housing: 8-Pin Molex 39-01-2085 or equivalent

Table 5. P2 – Processor and Memory Connector Pin-out

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	GND	Black	5	+12V1	Yellow
2	GND	Black	6	+12V1	Yellow
3	GND	Black	7	+12V1	Yellow/Black Stripe
4	GND	Black	8	+12V1	Yellow/Black Stripe

P3 and P4 – Cable for Backplane Power connector 1&2

Connector housing: 4-Pin Molex 39-01-2040 or equivalent

Table 6. P3 and P4 – Backplane Power Connector Pin-out

Pin	Signal	18AWG Color
1	GND	Black
2	+12V2	Yellow/Black Strip
3	+5VDC	Red
4	+3.3VDC	Red

P5 – PMBus Connector

Connector housing: 5-pin Molex 50-57-9705 or equivalent

Table 7. P5 – PMBus/Power Signal Connector Pin-out

Pin	Signal	24 AWG Color
1	I2C Clock	White/Yellow Stripe
2	I2C Data	White/Yellow Stripe
3	I2C Alert	White
4	Return	Black
5	N.C.	

P6 – CD/DVD Drive SATA Power connector

Connector housing: 4-Pin Molex 43640-0400 or equivalent

Table 8. P6 – CD/DVD Drive SATA Power Connector Pin-out

Pin	Signal	18AWG Color
1	+5VDC	Red
2	+5VDC	Red
3	GND	Black
4	GND	Black

3.3 Efficiency

The following table provides the required minimum efficiency level at various loading conditions. These are provided at three different load levels; 100%, 50%, and 20%. Efficiency was tested over an AC input voltage range of 115 VAC to 220 VAC.

Table 9. Power Supply Efficiency

Loading	100% of maximum	50% of maximum	20% of maximum
Minimum Efficiency	>85%	>88%	>85%

3.4 AC Input Voltage Specification

The power supply operates within all specified limits over input voltage range shown in the following table. Harmonic distortion of up to 10% THD will not cause the power supply to go out of specified limits. The power supply shall power off if the AC input is less than 75VAC +/-5VAC range. The power supply shall start up if the AC input is greater than 85 VAC +/-4 VAC. Application of an input voltage below 85 VAC will not cause damage to the power supply, including a fuse blow.

Table 10. AC Input Rating

Parameter	Min.	Rated	Max.	Max. input current at Min. Vrms
Voltage (100)	90 V_{rms}	100 V_{rms}	110 V_{rms}	6.7 A_{rms}
Voltage (120)	108 V_{rms}	120 V_{rms}	132 V_{rms}	5.6 A_{rms}
Voltage (240)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}	3.4 A_{rms}
Frequency	47 Hz		63 Hz	

3.4.1 AC Line Transient Specification

AC line transient conditions are defined as “sag” and “surge” conditions. Sag conditions are also commonly referred to as a “brown-out”. These conditions are defined as the AC line voltage dropping below nominal voltage conditions. Surge refers to conditions when the AC line voltage rises above nominal voltage.

The power supply meets the requirements under the following AC line sag and surge conditions.

Table 11. AC Line Sag Transient Performance

AC Line Sag				
Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltage ranges	50/60 Hz	No loss of function or performance
0 to 1 AC cycle	100%	Nominal AC Voltage ranges	50/60 Hz	No loss of function or performance
> 1 AC cycle	>10%	Nominal AC Voltage ranges	50/60 Hz	Loss of function acceptable, self recoverable

Table 12. AC Line Surge Transient Performance

AC Line Surge				
Duration	Surge	Operating AC Voltage	Line Frequency	Performance Criteria
Continuous	10%	Nominal AC Voltages	50/60 Hz	No loss of function or performance
0 to ½ AC cycle	30%	Mid-point of nominal AC Voltages	50/60 Hz	No loss of function or performance

3.4.2 Susceptibility Requirements

The power supply meets the following electrical immunity requirements:

Table 13. Performance Criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.4.2.1 Electrostatic Discharge Susceptibility

The power supply complies with the limits defined in EN 55024: 1998 using the IEC 61000-4-2:1995 test standard and performance criteria B defined in Annex B of CISPR 24.Tested to meet the level 3 requirement.

3.4.2.2 Fast Transient/Burst

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-4:1995 test standard and performance criteria B defined in Annex B of CISPR 24. Test to meet the level 3 requirement.

3.4.2.3 Radiated Immunity

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-3:1995 test standard and performance criteria A defined in Annex B of CISPR 24.

3.4.2.4 Surge Immunity

The power supply was tested with the system for immunity to AC Ringwave and AC Unidirectional wave, both up to 2kV, per EN 55024:1998, EN 61000-4-5:1995 and ANSI C62.45: 1992.

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-5:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

3.4.3 AC Line Fast Transient (EFT) Specification

The power supply meets the *EN61000-4-5* directive and any additional requirements in *IEC1000-4-5:1995* and the Level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.

The supply meets surge-withstand test conditions under maximum and minimum DC-output load conditions.

3.4.4 AC Line Dropout/Holdup

Loading	Holdup time
80%	20msec
100%	12msec

An AC line **dropout** is defined to be when the AC input drops to 0VAC at any phase of the AC line for any length of time. During an AC dropout, the power supply must meet dynamic voltage regulation requirements. An AC line dropout of any duration shall not cause tripping of control signals or protection circuits. If the AC dropout lasts longer than the hold up time, the power supply should recover and meet all turn on requirements. The power supply shall meet the AC dropout requirement over rated AC voltages and frequencies. A dropout of the AC line for any duration shall not cause damage to the power supply.

3.4.4.1 AC Line 5V$_{SB}$ Holdup

The 5 V_{SB} output voltage will stay in regulation under its full load (static or dynamic) during an AC dropout of **70 ms** min (=5V_{SB} holdup time) whether the power supply is in an ON or OFF state (PSON asserted or de-asserted).

3.4.5 Power Recovery

The power supply will recover automatically after an AC power failure. AC power failure is defined as any loss of AC power that exceeds the dropout criteria.

3.4.5.1 Voltage Brown Out

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

In addition, the power supply meets the following Intel Requirements:

A continuous input voltage below the nominal input range shall not damage the power supply or cause overstress to any power supply component. The power supply must be able to return to normal power up state after a brownout condition. Maximum input current under a continuous brownout shall not blow the fuse. The power supply will tolerate a 3min ramp from 90VAC voltage to 0VAC after the components have reached a steady state condition.

3.4.5.2 Voltage Interruptions

The power supply complies with the limits defined in EN55024: 1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

3.4.6 AC Line Inrush

Cold Start (25 Deg C): Any additional inrush current surges or spikes in the form of AC cycles or multiple AC must not exceed **40A peak** for 1ms. You can ignore the in-rush spike (<100us) due to the EMI filter capacitors.

Warm Start: Power supply shall not damage and the peak current shall be less than the rating of its critical components including input fuse, bulk rectifier, and surge limits devices.

3.4.7 AC Line Leakage Current

The maximum leakage current to ground for each power supply is 1.0 mA when tested at 240 V_{AC} 60 Hz.

3.4.8 AC Line Fuse

The power supply has a single line fuse, on the Line (Hot) wire of the AC input. The line fusing is acceptable for all safety agency requirements. The input fuse is a slow blow type. AC inrush current will not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply will not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.4.9 Power Factor Correction

The power supply incorporates a Power Factor Correction circuit.

- The PFC must be 0.95 or greater for all specified AC input voltages with output loads greater than 90%.
- The PFC must be 0.85 or greater for all specified AC input voltages with output loads greater than 50%.

3.5 Protection Circuits

Protection circuits inside the power supply will cause only the power supply's main outputs to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle OFF for 15 sec and a PSON# cycle HIGH for 1 sec shall be able to reset the power supply.

3.5.1 Over-Current Protection (OCP)

The power supply will have current limits to prevent the +3.3V, +5V, and +12V outputs from exceeding the values shown in the following table. If the current limits are exceeded, the power supply will shut down and latch off. You can clear the latch by toggling the PSON# signal or by an AC power interruption. The power supply will not be damaged from repeated power cycling in this condition. -12V and 5VSB will be protected under over-current or shorted conditions so that no damage can occur to the power supply. Auto-recovery feature is a requirement on 5 VSB rail.

Table 14. Over-current Protection (OCP)

Voltage	Over Current Limit (Iout limit)
+3.3 V	110% minimum (= 22A) ; 150% maximum (= 30A)
+5 V	110% min (= 33A); 150% max (= 40A)
+12 V1	25A min; 30A max
+12 V2	25A min; 30A max
+12 V3	18A min; 20A max
+12 V4	18A min; 20A max
-12 V	0.625A min; 2.0A max
5 V_{SB}	6.0A max

3.5.2 Over-voltage Protection (OVP)

The power supply over-voltage protection is locally sensed. The power supply will shut down and latch off after an over-voltage condition occurs. You can clear this latch by toggling the PSON# signal or by an AC power interruption. The following table contains the over-voltage limits. The values are measured at the output of the power supply's connectors. The voltage will never exceed the maximum levels when measured at the power pins of the power supply connector during any single point of fail. The voltage will never trip any lower than the minimum levels when measured at the power pins of the power supply connector.

Exception: +5V_{SB} rail should be able to recover after an over-voltage condition occurs.

Table 15. Over-Voltage Protection (OVP) Limits

Output Voltage	MIN (V)	MAX (V)
+3.3V	+3.9	+4.5
+5V	+5.7	+6.2
+12V1,2, 3, 4	+13.3	+14.5
-12V	-13.3	-14.5
+5V_{SB}	+5.7	+6.5

3.5.3 Over-temperature Protection (OTP)

The power supply is protected against over-temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an OTP condition, the PSU will shut down. When the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the $5V_{SB}$ remains always on. The OTP circuit has built-in hysteresis such that the power supply will not oscillate on and off due to a temperature recovering condition. The OTP trip level has a minimum of 4°C of ambient temperature hysteresis.

3.5.4 Output Short Circuit Protection

A short circuit placed to ground shall cause no damage and the power supply shall shutdown. A short circuit between each output shall cause no damage to the power supply.

3.6 Maximum power supply dissipation test conditions

Maximum power supply dissipation test conditions at 115/230 VAC.

Table 16. Maximum Power Supply Dissipation Test Conditions

	Condition 1	Condition 2	Condition 3
	5 Vsb off	5 Vsb on, 0A	5 Vsb on, 0A
	12 V main off	12 V main off	12 V main on, 0A
	Fan off	Fan at Minimum RPM	Fan at Minimum RPM
115 VAC	1.0 W	5.0 W	7.0 W
230 VAC	2.0 W	5.0 W	7.0 W

Notes:

- **Condition 1 defined as standby power supply shutdown mode.**
- **Condition 2 defined as standby mode, no load.**
- **Condition 3 defined as output enabled, no load.**

3.7 FRU specification

The FRU device will implement the same protocols as the commonly used AT24C02 device, including the Byte Read, Sequential Read, Byte Write, and Page Read protocols. EEPROM follows standard FRU device address location: A0h. (The SMBus should have 3.3V logic level). The FRU data format shall be compliant with the *IPMI ver.1.0 (per rev.1.1 from Sept.25, 1999)* specification. The current version of this specification is available at: http://developer.intel.com/design/servers/ipmi/spec.htm.

3.8 PMBus

The PMBus features are requirements for AC/DC silver box power supply for use in server systems. It is also required to enable Intel® Intelligent Power Node Manager.
This specification is based on the *PMBus™ specifications parts I and II, revision 1.1X3*.
The power supply device address locations are shown:

PDB addressing Address0/1	0/0	0/1	1/0	1/1
Power supply PMBus™ device	B0h	B2h	B4h	B6h

Notes: Power supplies unit in the Intel® Server System SR1690WB are using the 0/0 address locations.

3.8.1 Hardware

The device in the power supply is compatible with both the SMBus 2.0 “high power” specification for I^2C Vdd based power and drive (for Vdd = 3.3V). This bus operates at 3.3 V but is tolerant of 5 V signaling. It also operates at full 100 kbps SMBus speed without using clock stretching to slow down the bus.

3.8.2 Data Format

The data format for current, voltage, power, temperature, and fan speed are using the PMBus Literal format.

Literal data format: $X = Y \cdot 2^N$
X = the sensor value in volts, amps, watts, degrees C, or RPM
Y = mantissa. The mantissa is the variable components that changes as the sensor value changes. Y is a 16-bit unsigned value for the READ_VOUT command. For all other READ commands, Y is an 11-bit signed 2’s compliment value. N = exponent. The exponents are fixed for each power supply and define the resolution for each sensor.

3.8.3 Monitoring power/current/voltage

The following PMBus commands are supported for the purpose of monitoring currents, voltages, and power

Table 17. PMBus Commands

PMBus command	Description
READ_IIN	RMS input current in amps
READ_VIN	RMS input voltage in volts
READ PIN	AC input power in watts

3.8.4 Accuracy

The sensor commands meet the following accuracy requirements.

	Required Accuracy (+/-x% of reading)		
Output Loading	10% - 20%	>20% - 50%	>50% - 100%
READ_IIN	+/-15%	+/-5%	+/-5%
READ_PIN	+/-15%	+/-5%	+/-5%
READ_VIN	+/-5% over full range		
READ_TEMPERATURE	+/-3 ºC		

3.8.5 Thermal Management

The following commands are supported for monitoring temperature, monitor fan speed, and controlling the power supply fan. The fan monitoring is configured to provide a value in RPM. The fan control is in RPM too. All temperature sensors and fans in the power supply are accessible via PMBus.

Table 18. Thermal Management Commands

Command	Description
READ_FAN_SPEED_1	Returns the fan speed in RPM of fan sensor 1.
READ_FAN_SPEED_2	Returns the fan speed in RPM of fan sensor 2.
READ_TEMPERATURE_1, _2, _3	Returns the temperature in degrees C of temp sensors 1, 2, and 3.
FAN_CONFIG_1_2	Returns the configuration of Fan 1 and Fan 2 in the power supply.
FAN_COMMAND_1,_2	Allows the system to request fans in the power supply to be set to the defined RPM. The system cannot cause the power supply to run slower than the power supply needs for cooling.

3.8.6 Capability and inventory reporting

The follow commands are supported for discovery of the power supplies capabilities:

Table 19. Power Supply Commands

Command	Meaning
CAPABILITY	Defines the power supplies PEC support, bus speed, and support of SMBAlert.
QUERY	Defines the power supplies PEC support, bus speed, and support of SMBAlert.
PAGE	The PAGE command is used to QUERY a specific output of a multi-output power supply.

Revision and inventory information

- PMBUS_REVISION
- MFR_ID
- MFR_MODEL
- Power supply ratings
- MFR_VIN_MIN
- MFR_VIN_MAX
- MFR_IIN_MAX
- MFR_PIN_MAX
- MFR_TAMBIENT_MAX
- MFR_EFFICIENCY_LOW
- MFR_EFFICIENCY_HIGH

3.9 Power Supply Status LED

There is a single color LED to indicate power supply status. The following table defines the LED operation.

Table 20. LED Operation

Power Supply Condition	LED
No AC power to power supply	OFF
Power supply critical events causing a shutdown: failure, OCP, OVP, Fan Failure	6.7 Hz Blink GREEN
AC present/Only $5V_{SB}$ on (PS off)	1Hz Blink GREEN
Output ON and OK	Solid GREEN

3.10 AC Inlet Connector

The AC input connector is an *IEC 320 C-14* power inlet. This inlet is rated for 15 A/250 VAC.

3.11 AC Power Cord Specification Requirements

The AC power cord used must meet the following specification requirements:

Table 21. AC Power Cord Specification Requirements

Cable Type	SJT
Wire Size	16 AWG
Temperature Rating	105º C
Amperage Rating	13A
Voltage Rating	125V

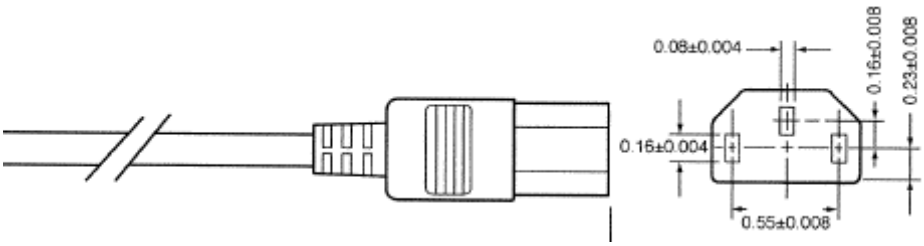


Figure 11. AC Power Cord Specifications

4. Cooling Sub-System

Several components and configuration requirements make up the cooling sub-system of the chassis. These include processors, chipsets, VR heatsinks, system fan module, power supply fans, CPU air duct, and drive bay population. All are necessary to provide and regulate the air flow and air pressure needed to maintain the system's thermals when operating at or below the maximum specified thermal limits.

In order to maintain the necessary airflow within the system, you must properly install the air duct and the top cover.

The chassis uses a variable fan speed control engine to provide adequate cooling for the system at various ambient temperature conditions, under various server workloads, and with the least amount of acoustic noise possible. The fans operate at the lowest speed for any given condition to minimize acoustics.

Note: The server system does not support redundant cooling fans. If any of the fans fail, you must power down the system as soon as possible to replace the fan.

4.1 CPU Heatsink

Two heatsinks are included in the system package. These heatsinks are designed for optimal cooling and performance. Each processor is cooled by a passive heatsink. To achieve better cooling performance, you must properly attach the heatsink bottom base with TIM (thermal interface material). ShinEtsu* G-751 or 7783D or Honeywell* PCM45F TIM is recommended. The mechanical performance of the heatsink must satisfy mechanical requirement of Intel® Xeon® processors. To keep chipsets and VR temperature at or below maximum temperature limit, the heatsink is required if necessary.

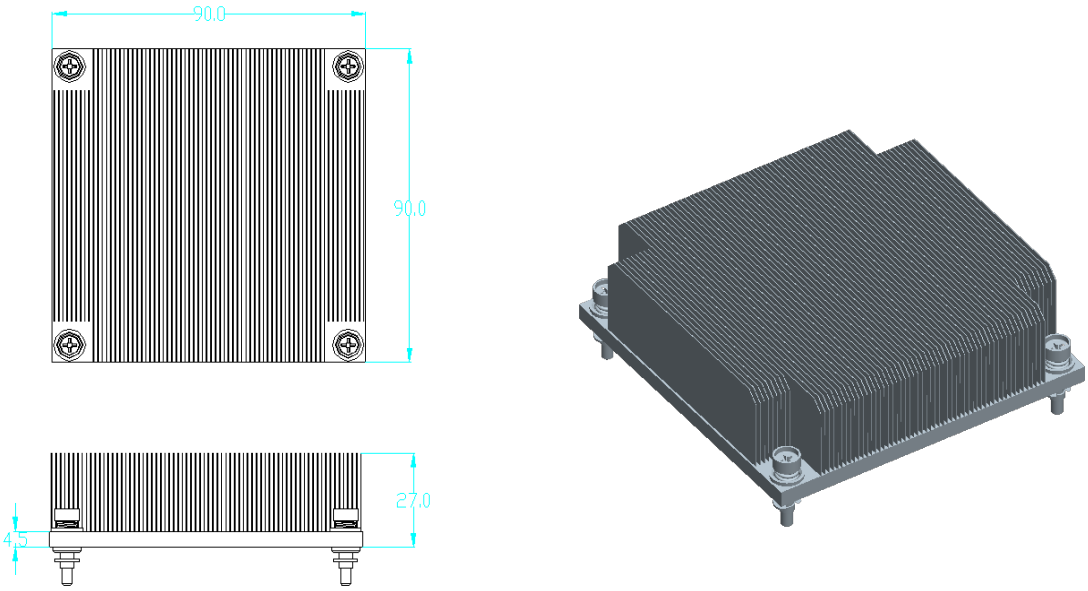


Figure 12. CPU Heatsink Overview

Note: The passive heatsink is Intel® standard thermal solution for 1U/2U rack chassis.

4.2 Four-Fan Module

The system includes a fan assembly consisting of four managed 40x40x56 mm dual-rotor, multi-speed fans. Four fans are separated into two types with different fan connectors.

The center two fans use two 4-pin connectors; each matches the processor fan header on the server board. The outer two fans use one 8-pin connector; each matches the memory fan header on the server board.

They provide the primary cooling for the processors, memory, and the hard drive bays on the front panel. Each fan is designed for tool-less insertion to or removal from the fan module housing.

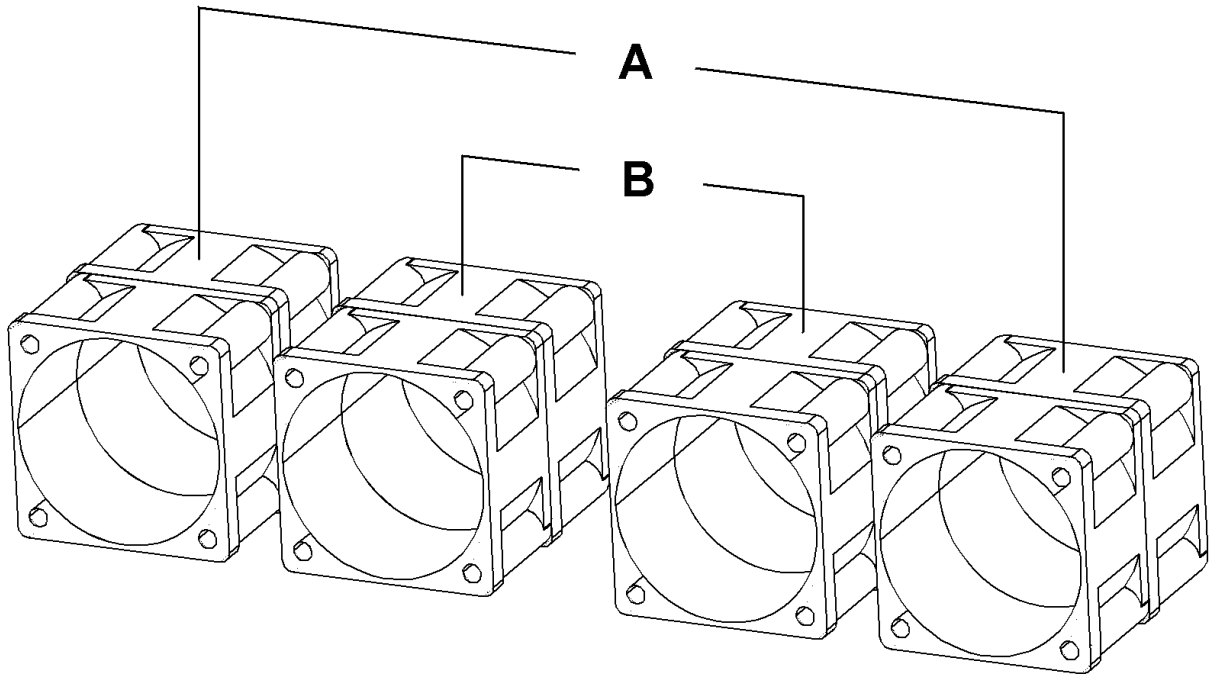
The system fan module is designed for ease of use and supports several management features that the server board management system can use.

Note: The fans are NOT hot-swappable. You must turn off the system to replace a failed fan.

Each fan within the module is capable of supporting multiple speeds. Fan speed changes automatically when internal ambient temperature of the system or processor temperature changes. The fan speed control algorithm is programmed into the server board's BIOS.

Each fan connector within the module supplies a tachometer signal that allows the BMC to monitor the status of each fan. If one of the fans should fail, the system fault LED on front panel will light.

Note: There is a spare fan kit that contains one CPU cooling fan and one memory cooling fan.



A	Memory Cooling Fans
B	Processor Cooling Fans

Figure 13. Fan Module Assembly

Each memory fan (Group A) uses 8-pin connector, which is connected to fan connector on mother board (Connector BB and Q in Figure 5).

Each processor fan (Group B) uses 4-pin connector, which is connected to processor fan connector on mother board (Connector S, T and Y, Z in Figure 5).

The fan connector pin-out definition is as follows:

Table 22. 4-pin Connector Pin-Out for Processor Cooling Fan

Pin	Signal Name	Description
1	GND	Ground
2	12V	Power Supply +12 V
3	Tach Out	FAN_TACH signal output
4	PWM In	PWM signal input

Table 23. 8-pin Connector Pin-Out for Memory Cooling Fan

Pin	Signal Name	Description
1	GND	Ground
2	12V	Power Supply 12 V
3	Tack0	Tach signal output from FAN0
4	PMW0	PWM control signal input for FAN0
5	GND	Ground
6	12V	Power Supply 12 V
7	Tach1	Tach signal output from FAN1
8	PWM1	PWM control signal input for FAN1

4.3 Power Supply Fan

Each power supply module supports one non-redundant 40 mm fan. The fans control the cooling of the power supply and some drive bays. These fans are not replaceable. Therefore, if a power supply fan fails, you must replace the power supply module.

4.4 Air Duct Module

The chassis requires the use of an air duct module to direct airflow over critical areas within the system. The following provides a summary and description of Air Duct Module.

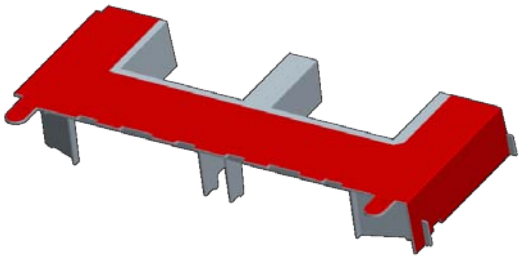


Figure 14. Air Duct Module

The following provides a description for Air Duct module assembling process.

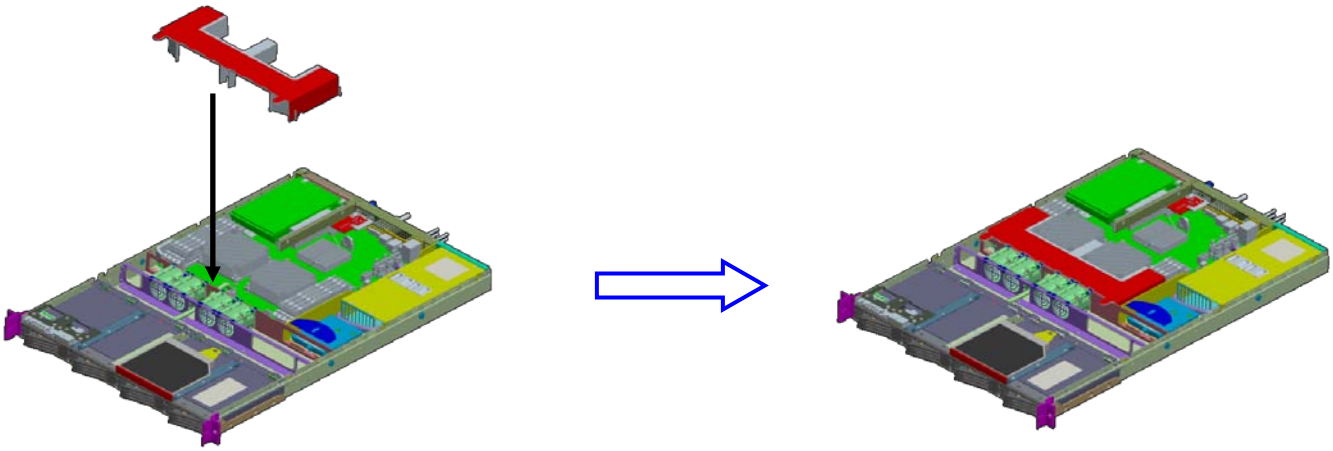


Figure 15. Air Duct Module assembly process

4.5 Drive Bay Population Requirement

In order to maintain system thermal requirements, you must fully populate all hard drive bays. Hard drive trays used for hot-swap drives must either have a hard drive installed or not have a hard drive installed.

IMPORTANT: If the drive bay is missing or not fully populated, the system will not meet the thermal cooling requirements of the processor, which will most likely result in degraded performance as a result of throttling or thermal shutdown of the system. It is recommended to apply the air block on the blank HDD carrier if the installed HDD quantity is less than four pieces.

Figure 16. Hot-swap HDD Tray with SAS/SATA HDD Installed

5. Peripheral Drive Support

The system provides a slim-line drive bay that can populate with a SATA optical drive (CD-ROM, DVD, and DVD/CD-R). The drive is mounted on a tool-less tray, which allows for easy installation into and removal from the system. The slim-line device is not hot-swappable. Recommended to use Intel® validated optical drive.

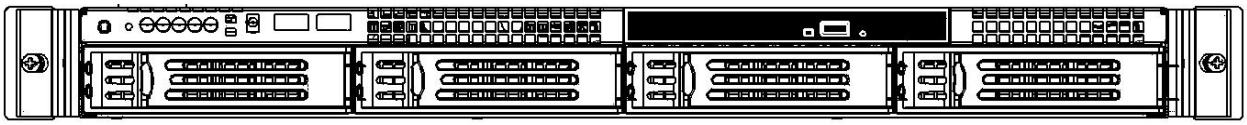


Figure 17. View of Slim-line Drive Bay (in Deep Black)

The drive is directly connected to a SATA cable and a SATA power cable. The other end of the SATA cable is connected to one SATA port on the server board.

Table 24. Optical Drive SATA Connector Pin-out

Pin	Signal Name	Description
1	GND	Ground
2	SATA_TX_P	Positive side of transmit differential pair
3	SATA_TX_N	Negative side of transmit differential pair
4	GND	Ground
5	SATA_RX_N	Negative side of receive differential pair
6	SATA_RX_P	Positive side of receive differential pair
7	GND	Ground

Table 25. Optical Drive SATA Power Connector Pin-out

Pin	Signal Name	Description
P1	Not Used	-
P2	Not Used	-
P3	Not Used	-
P4	GND	Ground
P5	GND	Ground
P6	GND	Ground
P7	P5V	Power supply 5V
P8	P5V	Power supply 5V
P9	P5V	Power supply 5V
P10	GND	Ground
P11	Reserved	-
P12	GND	Ground
P13	P12V	Power supply 12V
P14	P12V	Power supply 12V
P15	P12V	Power supply 12V

6. Hard Disk Drive Support

The server system provides four hard drive bays at the front of the chassis. You can populate all hard drive bays with a carrier-mounted 3.5-inch or 2.5-inch SATA or SAS hard disk drives.

6.1 Hard Disk Drive Bays

The server system 1U chassis can support up to four carrier-mounted SATA or SAS 3.5-inch or 2.5-inch hard disk drives. The drives may be “electrically” hot-swapped while the system power is applied, but you must take caution before hot-swapping while the system is functioning under operating system/application control or data may be lost.

Note: All drive bays (0 through 3) are controlled by the server board or the RAID controller card.

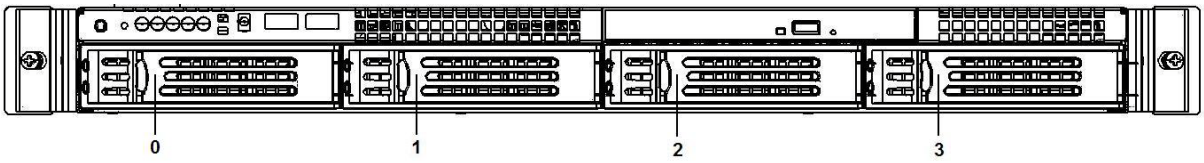


Figure 18. HDD Bays and Numbering

If a failed drive needs replacing, it is recommended you replace it with the same manufacturer, model, and capacity.

6.2 Hard Drive Trays

You can use hard drive trays for 3.5-inch or 2.5-inch hot-swap hard drive configurations.

Hot-swap drive trays make insertion and extraction of the drive from the system very simple. Each drive tray has its own latching mechanism, which is used to both insert and extract drives from the chassis and lock the tray in place. Each drive tray supports two light pipes to direct light from the drive status LEDs on the backplane to the tray’s face allowing it to be viewable from the front of the system.

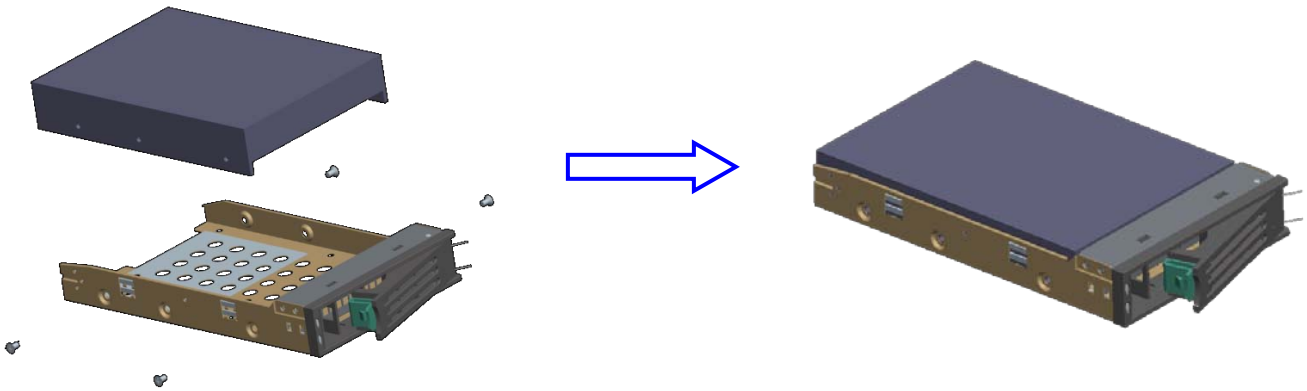


Figure 19. 3.5-inch HDD Assembly Overview

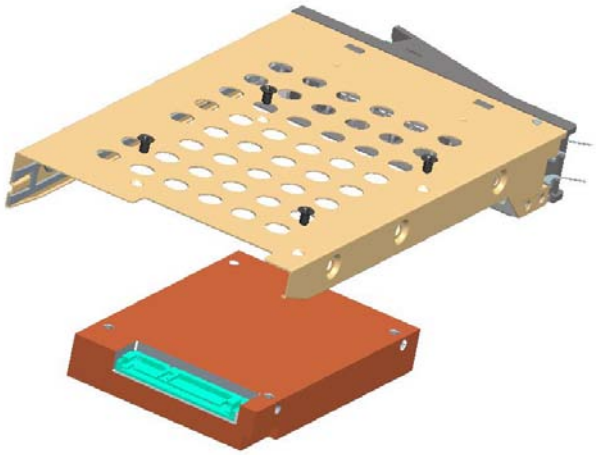


Figure 20. 2.5-inch HDD Assembly Overview

6.3 Hot-Swap Hard Drive Support

The Intel® Server System SR1690WB can support up to four hot-swap SATA or SAS hard drives. Hard drives interface with the passive backplane through a blind mate connection when drives are installed into a hard drive bay using hot-swap drive trays.

The passive backplane acts as an intermediate pass-through interface board where SATA ports of the server board or add-in SAS/SATA controller are cabled to the backplane. The on board Intel® 82801Jx I/O Controller Hub provides the necessary drive interface. You can also connect the passive backplane to an add-in PCI Express* based SAS/SATA RAID card.

The following sections describe the feature and connections between the backplane and server board.

6.3.1 Backplane Feature set:

- Vitesse* VSC410 enclosure management controller
  - Integrated v3000 32 bit RISC microprocessor core
  - External non-volatile Flash ROM
  - Four I^2C interfaces
  - 44 GPIO pins
- Four drive control connectors supporting either SATA ports from the server board or SAS/SATA ports from an add-in RAID card
- Support for up to four hot-swap SAS/SATA drives
- 4x2 hard drive activity/fault LEDs
- 2x4 pin power connector
- One 4-pin IPMB connector
- One 4-pin SMBus connector
- One 4-pin SGPIO connector
- One 3-pin SES connector
- Four internal SAS/SATA connectors

6.3.2 Backplane Block Diagram:

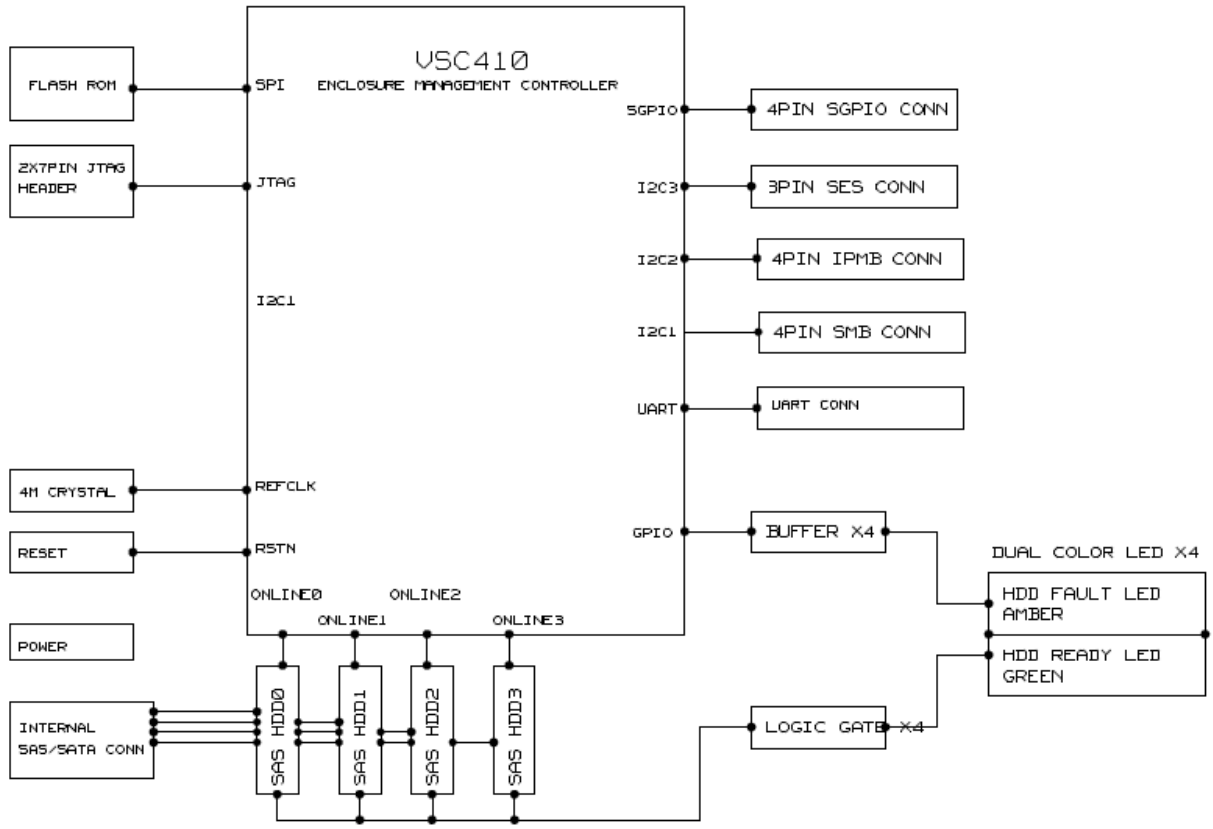
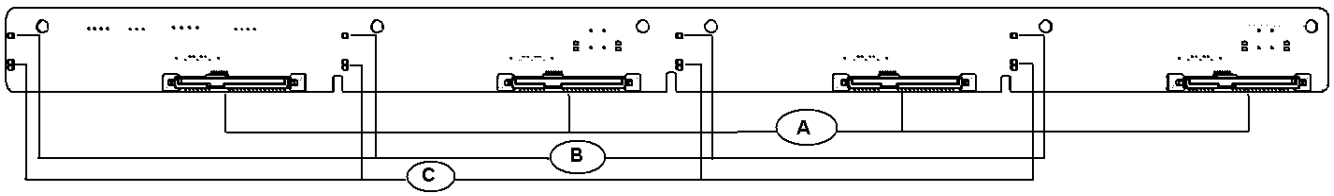


Figure 21. Passive Backplane Block Diagram

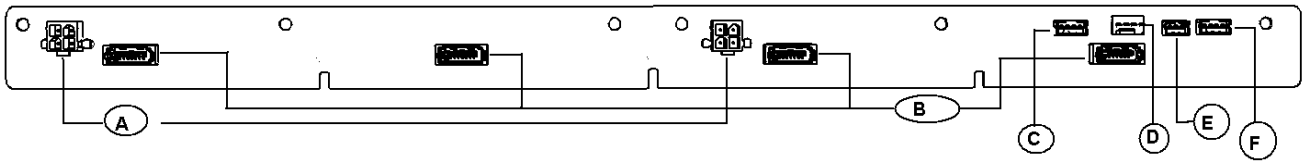
6.3.3 Backplane Connector Definition

The following diagrams show the layout of major components and connectors for backplane.



A	HDD Connectors 0~3 (left to right)
B	HDD On-line LEDs 0~3 (left to right)
C	HDD Act/Fault LEDs 0~3 (left to right)

Figure 22. Backplane Component and Connectors (Front View)



A	4-pin power connectors 1~2 for backplane
B	SATA/SAS connectors 0~3 (right to left)
C	4-pin SGPIO connector
D	4-pin SMBus connector
E	3-pin SES connector

A	4-pin power connectors 1~2 for backplane
F	4-pin IPMB connector

Figure 23. Backplane Component and Connectors (Back View)

6.3.4 Backplane LED Support

The backplanes support both HDD online and activity/fault LEDs for each of the hard drive connectors. A light duct in HDD tray is used to conduct LED light to front panel. The following lists LED functionality.

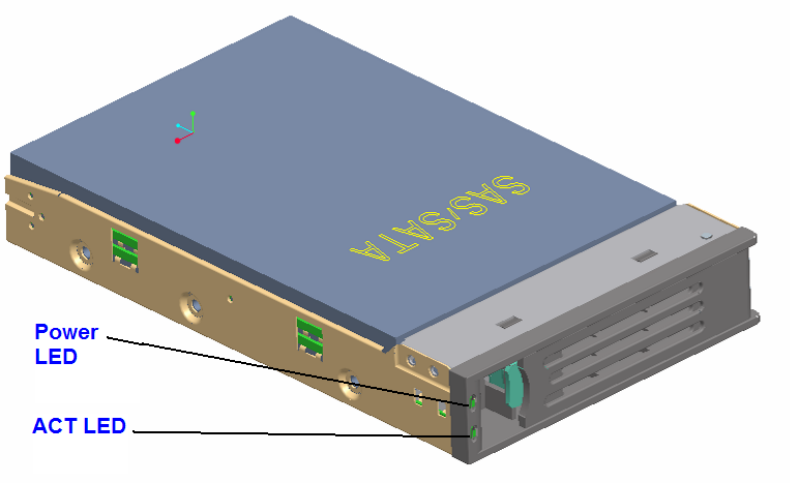


Table 26. Hard Drive Tray LED Functions

	LED color	Condition	Description
Power LED	Blue	ON	HDD On-line
		OFF	HDD Not On-line
Activity LED	Green	OFF	Standby/Stopped
		Flashing(on 0.5s off 0.5s)	Spin-Up/Spin-Down
		ON	Active/Idle power
		Flashing(on 1s off 1s)	Formatting
	Amber	ON	Fault
		Flashing(on 0.5s off 0.5s)	Rebuild

6.3.5 Backplane Connector Definition

The backplanes include several different connectors. This section defines the purpose and pinout associated with each.

6.3.5.1 Power Connector(J1A1, J5A1)

The backplane provides power to the three hard drive bays and the slim-line drive bay. An 8-pin power cable is routed from the power supply and plugs into two 4-pin shrouded plastic PC power connector on the backplane. The following table shows the power connector pin-out.

Table 27. Backplane Power Connector Pin-out

Pin	Signal	Pin	Signal
1	COM	3	+5VDC
2	+12VDC	4	+3V3DC

6.3.5.2 Hot-Swap SATA/SAS Drive Connectors(JC2L1, JC4L1, JC6L1, JC9L1)

The backplanes provide four hot-swap SATA/SAS connectors, which provide power and signals using a single docking connector. Each drive attaches to the backplane using one of these connectors.

Table 28. Hot-Swap SATA/SAS Connector Pin-out

Pin#	Signal Description
SI	Ground
S2	SAS#_TX_DP (# = 0…2)
S3	SAS#_TX_DN (# = 0…2)
S4	Ground
S5	SAS#_RX_DN (# = 0…2)
S6	SAS#_RX_DP (# = 0…2)
S7	Ground
S8	Not Used
S9	Not Used
S10	Not Used
S11	Not Used
S12	Not Used
S13	Not Used
S14	Not Used
P1	Not Used
P2	Not Used
P3	Not Used
P4	Ground
P5	Ground
P6	P3V3
P7	P5V
P8	P5V
P9	P5V
P10	Ground
P11	LED_SAS#_ACT_L (# = 0…2)
P12	Ground
P13	P12V
P14	P12V
P15	P12V
PTH0	Ground
PTY1	Ground

6.3.5.3 SATA/SAS Drive Control Connectors (J1A2, J4A1, J6A2, and J8A2)

The passive backplane includes four drive control connectors. These are used to attach SATA/SAS cables from the backplane to either the SATA ports on the server board, or to SAS/SATA ports from an add-in card. Each drive control connector has the following pin-out.

Table 29. SATA/SAS Drive Control Connector Pin-out

Pin#	Description
1	GROUND
2	SATA # TX_DP (# = 0,1,2)
3	SATA # TX_DN (# = 0,1,2)
4	GROUND
5	SATA # RX_DN (# = 0,1,2)
6	SATA # RX_DP (# = 0,1,2)
7	GROUND

6.3.5.4 System Management(IPMB) Connector(J9A1)

The backplanes provide connectors to interface with system management buses. The following tables define the pin-out for each of these connectors.

Table 30. IPMB Connector Pin-out

Pin #	Description
1	SMB_5VSB_IPMB_DAT
2	GND
3	SMB_5VSB_IPMB_CLK
4	SMB_PWR_IPMB_CONN

6.3.5.5 System Management Bus (SMBus) Connector (J8A1)

The backplanes provide connectors to interface with System Management Bus. The following tables define the pin-out for each of this connector.

Table 31. SMBus Connector Pin-out

Pin #	Description
1	SMB_5V_DAT
2	GND
3	SMB_5V_CLK
4	GND

6.3.5.6 System General Purpose IO (SGPIO) Connector (J4A2)

The backplanes provide connectors to interface with System General Purpose IO control. The following tables define the pin-out for each of this connector.

Table 32. SGPIO Connector Pin-out

Pin #	Description
1	Data In
2	Data Out
3	End Control
4	Clock

6.3.5.7 SCSI Enclosure Services (SES) Connector (J9A2)

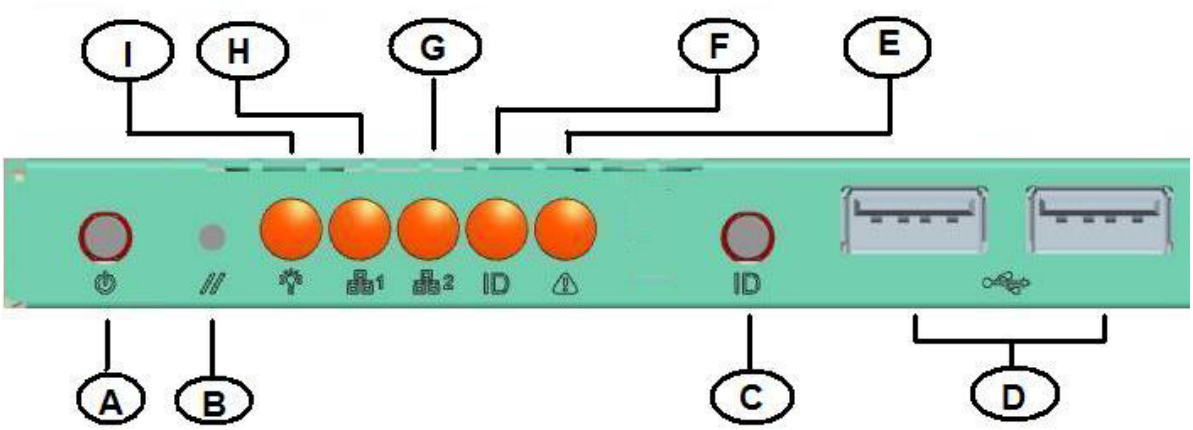
The backplanes provide connectors to interface with SCSI Enclosure Services (SES) signals. The following tables define the pin-out for each of this connector.

Table 33. SES Connector Pin-out

Pin #	Description
1	SMB_HBA_I2C_DAT
2	GND
3	SMB_HBA_I2C_CLK

7. Front Panel Control and Indicators

The Intel® Server System SR1690WB Front Control Panel integrates control buttons, LEDs, and USB ports. The control panel assembly is pre-assembled and fixed to the chassis.



A	Power/Sleep Button
B	System Reset Button
C	System Identification Button
D	USB 2.0 connectors – Port 0 & 1
E	System Status LED
F	System Identification LED
G	System NIC 2 Activity LED
H	System NIC 1 Activity LED
I	Power/Sleep LED

Figure 24. Front Control Panel

7.1 Control Panel Button

The following table lists the control panel features and functions. The control panels features a system power button.

Table 34. Front Control Button Function

Feature	Function
Power/Sleep Button	Toggles the system power on/off. This button also functions as a Sleep Button if enabled by an ACPI-compliant operating system.
System Reset Button	Reset system to reboot
System ID Button	Turn On/turn off ID LED

7.2 Control Panel LED Indicators

The control panel houses five LEDs, which are viewable to display the system's operating status.

The following table identifies each LED and describes their functionality.

Table 35. Front LED Indicator Functions

LED Indicator	Color	Condition	What it describes
Power/Sleep	Green	On	Power On/ACPI S0 state
	Green	Blink	Sleep /ACPI S1 state
	-	Off	Power Off /ACPI S5 state
LAN 1 and LAN 2	Green	On	LAN Link no Access
	Green	Blink	LAN Activity
	-	Off	No Link
System ID	Blue	On	Identify Active via command or button
	-	Off	No Identification
System Status	Green	On	System Ready/No Alarm
	Green	Blink	System ready, but degraded: redundancy lost such as the power supply or fan failure; non-critical temp/voltage threshold; battery failure; or predictive power supply failure.
	Amber	On	Critical Alarm: Critical power modules failure, critical fans failure, voltage (power supply), critical temperature and voltage
	Amber	Blink	Non-Critical Alarm: Redundant fan failure, redundant power module failure, non-critical temperature and voltage
	-	Off	AC power off: System unplugged AC power on: System powered off and in standby, no prior degraded\non-critical\critical state

Notes:

Blink rate is ~1 Hz at 50% duty cycle.

It is also off when the system is powered off (S5) or in a sleep state (S1).

The power LED sleep indication is maintained on standby by the chipset. If the system is powered down without going through the BIOS, the LED state in effect at the time of power off is restored when the system is powered on until the BIOS clear it.

If the system is not powered down normally, it is possible the Power LED will blink at the same time the system status LED is off due to a failure or configuration change that prevents the BIOS from running.

7.2.1 Power/Sleep LED

Table 36. SSI Power LED Operation

State	Power Mode	LED	Description
Power Off	Non-ACPI	Off	System power is off and the BIOS has not initialized the chipset.
Power On	Non-ACPI	Solid On	System power is on but the BIOS has not yet initialized the chipset.
S5	ACPI	Off	Mechanical is off and the operating system has not saved any context to the hard disk.
S1 Sleep	ACPI	Blink	DC power is still on. The operating system has saved context and gone into a level of low-power state.
S0	ACPI	Solid On	System and the operating system are up and running.

Notes: Blink rate is ~ 1Hz at 50% duty cycle.

7.2.2 System Status LED

Table 37. System Status LED Operation

Color	State	Criticality	Description
Off	N/A	Not ready	AC power off or BMC initialization completes if no degraded, non-critical, critical, or non-recoverable conditions exist after AC plug in

Color	State	Criticality	Description
Green/ Amber	Both Solid On	Not ready	Pre DC Power On – 15-20 second BMC Initialization when AC is applied to the server. The system will not POST until BMC initialization completes.
Green	Solid on	Ok	System ready
Green	Blink	Degraded	BIOS detected 1. Unable to use all of the installed memory (more than one DIMM installed).[1] 2. In a mirrored configuration, when memory mirroring takes place and system loses memory redundancy. This is not covered by (2). [1] 3. PCI Express* correctable link errors. Integrated BMC detected 1. Redundancy loss such as a power supply or fan. Applies only if the associated platform subsystem has redundancy capabilities. 2. CPU disabled – if there are two CPUs and one CPU is disabled. 3. Fan alarm – Fan failure. Number of operational fans should be more than minimum number needed to cool the system. 4. Non-critical threshold crossed – Temperature, voltage, power nozzle, power gauge, and PROCHOT2 (Therm Ctrl) sensors. 5. Battery failure. 6. Predictive failure when the system has redundant power supplies.
Amber	Blink	Non-critical	Non-fatal alarm – system is likely to fail **BIOS Detected** 1. In non-mirroring mode, if the threshold of ten correctable errors is crossed within the window.[1] 2. PCI Express* uncorrectable link errors. **Integrated BMC Detected** 1. Critical threshold crossed – Voltage, temperature, power nozzle, power gauge, and PROCHOT (Therm Ctrl) sensors. 2. VRD Hot asserted. 3. Minimum number of fans to cool the system are not present or have failed.
Amber	Solid on	Critical, non-recoverable	Fatal alarm – system has failed or shutdown **BIOS Detected** 1. DIMM failure when there is one DIMM present and no good memory is present.[1] 2. Run-time memory uncorrectable error in non-redundant mode.[1] 3. CPU configuration error (for instance, processor stepping mismatch). **Integrated BMC Detected** 1. CPU CATERR signal asserted. 2. CPU 1 is missing. 3. CPU THERMTRIP. 4. No power good – power fault. • Power Unit Redundancy sensor – Insufficient resources offset (indicates not enough power supplies are present).

Notes:

1. The BIOS detects these conditions and sends a Set Fault Indication command to the Integrated BMC to provide the contribution to the system status LED

2. Blink rate is ~ 1Hz at 50% duty cycle.

7.2.2.1 System Status LED – BMC Initialization

When AC power is first applied to the system and 5V-STBY is present, the BMC controller on the server board requires 15-20 seconds to initialize. During this time, the system status LED will be solid on, both amber and green. Once BMC initialization has completed, the

status LED will stay green solid on. If power button is pressed before BMC initialization completes, the system will not boot to POST.

7.2.3 System Identification LED

The system ID LED provides a visual indication of a system being serviced. The state of the system ID LED is affected by the following:

- Toggled by the system ID button
- Controlled by *the Chassis Identify command* (IPMI)
- Controlled by *the Chassis Identify LED command* (OEM)

Table 38. System ID LED Indicator States

State	LED State
Identify active via button	Solid on
Identify active via command	~1 Hz blink
Off	Off

There is no precedence or lock-out mechanism for the control sources. When a new request arrives, all previous requests are terminated. For example, if the system ID LED is blinking and the system ID button is pressed, then the system ID LED changes to solid on. If the button is pressed again with no intervening commands, the system ID LED turns off.

7.3 Front Panel Connectors

Front Panel uses 2 cables to connect with motherboard, one is 24-pin SSI control panel cable to J1D3 on motherboard, another is 10-pin 2 ports USB cable to J9A2 (USB port 0/1) on motherboard.

The pin-out for SSI control cable is as below:

Table 39. Front Panel SSI connector pin-out

Pin	Signal Name	Pin	Signal Name
1	P3V3_STBY (Power LED Anode)	2	P3V3_STBY (Front Panel Power)
3	Key	4	P5V_STBY (ID LED Anode)
5	FP_PWR_LED_N	6	FP_ID_LED_BUF_N
7	P3V3 (HDD Activity LED Anode)	8	FP_LED_STATUS_GREEN_N
9	LED_HDD_ACTIVITY_N	10	FP_LED_STATUS_A MBER_N
11	FP_PWR_BTN_N	12	NIC1_ACT_LED_N
13	GND (Power Button GND)	14	NIC1_LINK_LED_N
15	BMC_RST_BTN_N	16	SMB_SENSOR_3V3STB_DATA
17	GND (Reset GND)	18	SMB_SENSOR_3V3STB_CLK
19	FP_ID_BTN_N	20	FP_CHASSIS_INTRU
21	NC	22	NIC2_ACT_LED_N
23	FP_NMI_BTN_N	24	NIC2_LINK_LED_N

Front panel USB connector pin-out is as follows:

Table 40. Front Panel USB connector pin-out

Pin	Signal Name	Pin	Signal Name
1	NC	2	Key Pin
3	GND	4	GND
5	USB_P	6	USB_P
7	USB_N	8	USB_N
9	+5V	10	+5V

8. Configuration Jumpers

The following table provides a summary and description of configuration, test, and debug jumpers on the Intel® Server Board S5500WB, which is used in Intel® Server System SR1690WB.

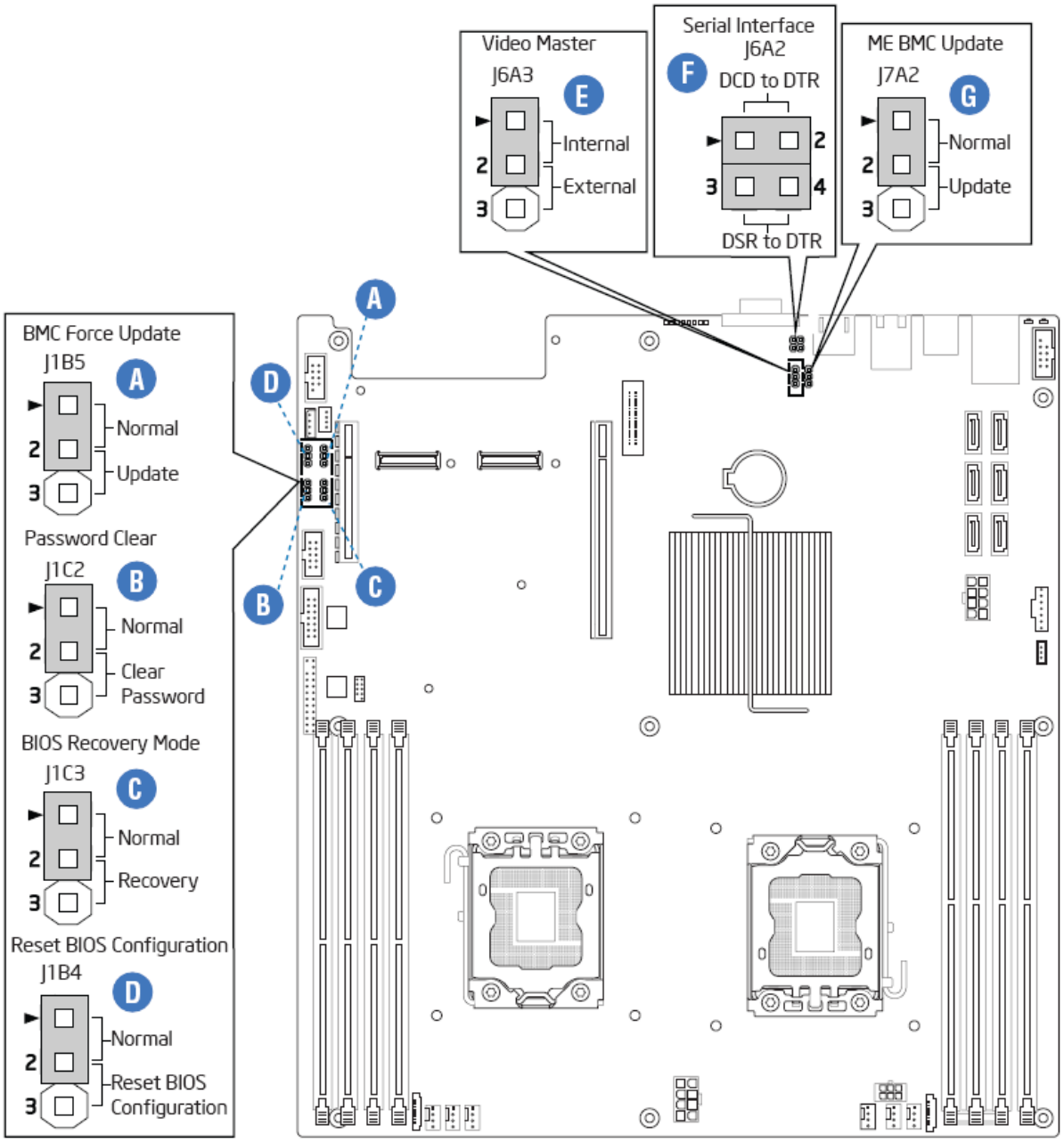


Figure 25.Jumper Locations and Functions

8.1 Force IBMC Update (J1B5)

When performing a standard BMC firmware update procedure, the update utility places the BMC into an update mode, allowing the firmware to load safely onto the flash device. In the unlikely event the BMC firmware update process fails due to the BMC not being in the proper update state, the server board provides a BMC Force Update jumper (J1B5) that forces the BMC into the proper update state. You must complete the following procedure in the event the standard BMC firmware update process fails.

Table 41. Force IBMC Update Jumper

Jumper Position	Mode of Operation	Note
1-2	Normal	IBMC GPIO [1] is pulled HIGH. Default position.
2-3	Update	IBMC GPIO [1] is pulled LOW.

1. Power down and remove the AC power cord.
2. Open the server chassis. Refer to your server chassis documentation for instructions.
3. Move the jumper from the default operating position, covering pins 1 and 2, to the enabled position, covering pins 2 and 3.
4. Close the server chassis.
5. Reconnect the AC cord and power up the server.
6. Perform the BMC firmware update procedure as documented in the README.TXT file included in the given BMC firmware update package. After the successful completion of the firmware update process, the firmware update utility may generate an error stating the BMC is still in update mode.
7. Power down and remove the AC power cord.
8. Open the server chassis.
9. Move the jumper from the enabled position, covering pins 2 and 3 to the disabled position, covering pins 1 and 2.
10. Close the server chassis.
11. Reconnect the AC cord and power up the server.

Note: Normal BMC functionality is disabled when the Force BMC Update jumper is set to the enabled position. You should never run the server with the BMC Force Update jumper set in this position. You should only use this jumper setting when the standard firmware update process fails. This jumper should remain in the default/disabled position when the server is running normally.

8.2 Password Clear (J1C2)

This 3-pin jumper is used to clear the BIOS password.

Table 42. BIOS Password Clear Jumper

Jumper Position	Mode of Operation	Note
1-2	Normal	ICH10R INTRUDER# pin is pulled HIGH. Default position.
2-3	Clear Password	ICH10R INTRUDER# pin is pulled LOW.

8.2.1 Clearing the BIOS Password

1. Power down server. Do not unplug the power cord.
2. Open the chassis. For instructions, refer to your server chassis documentation.
3. Move the jumper (J1B6) from the default operating position, covering pins 1 and 2, to the password clear position, covering pins 2 and 3.
4. Close the server chassis.
5. Power up the server, wait 10 seconds or until POST completes.
6. Power down the server.
7. Open the chassis and move the jumper back to default position, covering pins 1 and 2.
8. Close the server chassis.
9. Power up the server. The password is now cleared and you can reset it by going into the BIOS setup. The BIOS password is now cleared.

8.3 BIOS Recovery Mode (J1C3)

The Intel® Server Board S5500WB uses the BIOS recovery to repair the system BIOS from flash corruption in the main BIOS and Boot Block. This 3-pin jumper is used to reload the BIOS when the image is suspected to be corrupted. For instructions on how to recover the BIOS, refer to the specific BIOS release notes.

Table 43. BIOS Recovery Mode Jumper

Jumper Position	Mode of Operation	Note
1-2	Normal	ICH10R GPIO [55] is pulled HIGH. Default position.
2-3	Recovery	ICH10R GPIO [55] is pulled LOW.

8.4 Reset BIOS Configuration (J1B4)

This jumper used to be the CMOS Clear jumper. The BIOS has moved CMOS data to the NVRAM region of the BIOS flash since the previous generation. The BIOS checks during boot to determine if the data in the NVRAM must be set to default.

Table 44. Reset BIOS Jumper

Jumper Position	Mode of Operation	Note
1-2	Normal	ICH10R RTCRST# pin is pulled HIGH. Default position.
2-3	Reset BIOS Configuration	ICH10R RTCRST# pin is pulled LOW.

Clearing the CMOS

1. Power down server. Do not unplug the power cord.
2. Open the server chassis. For instructions, refer to your server chassis documentation.
3. Move the jumper (J1B4) from the default operating position, covering pins 1 and 2, to the reset/clear position, covering pins 2 and 3.
4. Wait five seconds.
5. Remove AC power.
6. Move the jumper back to default position, covering pins 1 and 2.
7. Close the server chassis.
8. Power up the server.

The CMOS settings are now cleared.

Note: Removing AC Power before performing the CMOS Clear operation causes the system to automatically power up and immediately power down, after the procedure is followed and AC power is re-applied. If this happens, remove the AC power cord again, wait 30 seconds, and re-install the AC power cord. Power up system and proceed to the <F2> BIOS Setup Utility to reset the preferred settings.

8.5 Video Master (J6A3)

This jumper is used to set the video output port if both internal and external add-in video card are used.

Table 45. Video Master Jumper

Jumper Position	Mode of Operation	Note
1-2	Internal	Internal connector overrides if both connectors are used.
2-3	External	External connector overrides if both connectors are used.

8.6 Serial Interface (J6A2)

This jumper is used to set the communication mode of serial port.

Table 46. Serial Interface Jumper

Pins	Mode	Description
1 – 2	DTR	Data Terminal Ready
2 – 3	DCD	Data Carrier Detect
None	DSR	Data Set Ready

9. PCI Riser Card and Assembly

Each Intel® Server System SR1690WB includes one PCI Express* riser slot that accepts one PCI Express* x16 full height or low profile adapter card. The riser also accommodates PCI Express x8, x4, and x1 adapters.

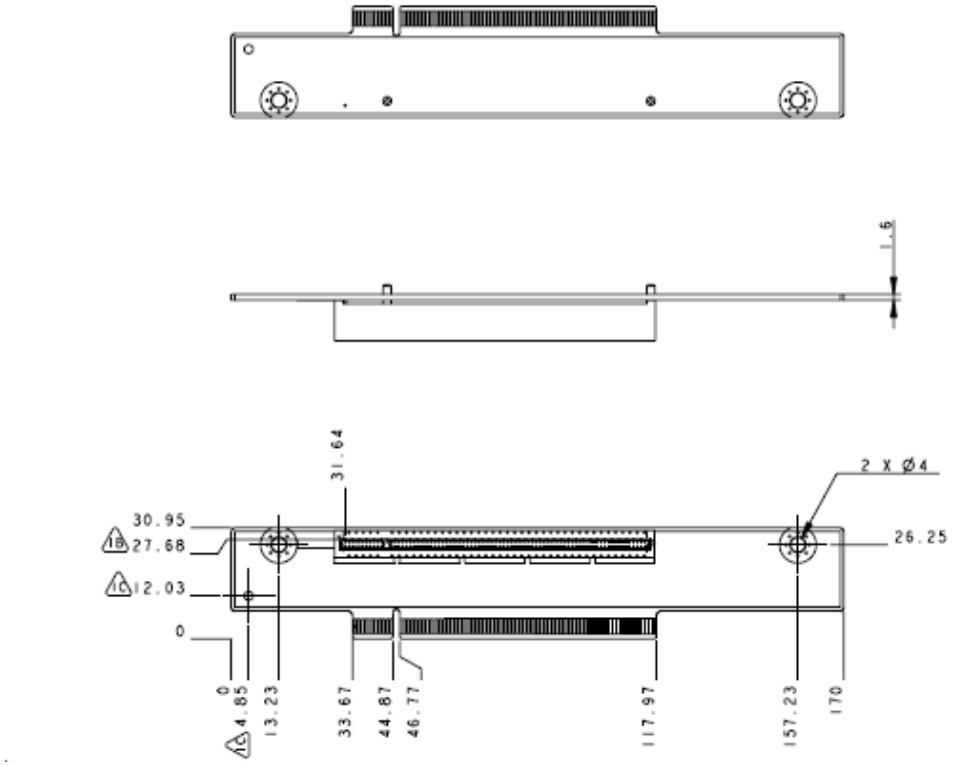


Figure 26. 1U PCI Express* Riser Card Mechanical Drawing

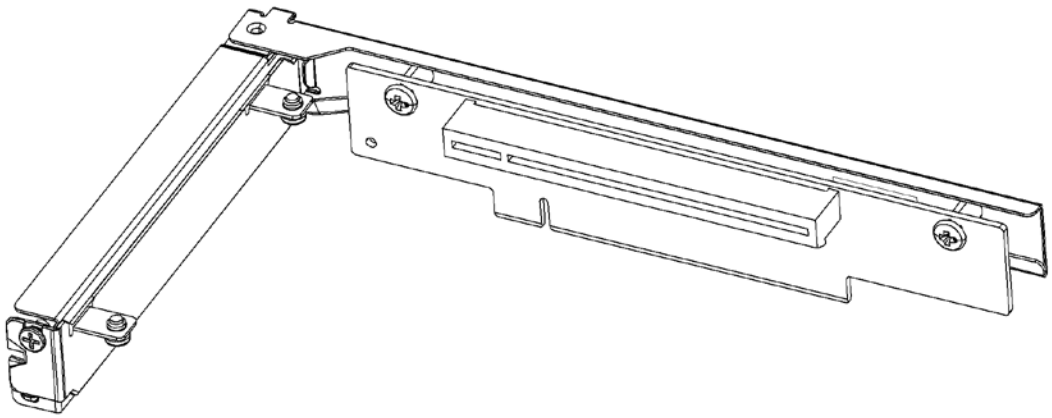


Figure 27. Intel® Server System SR1690WB PCI Express* Riser Assembly

Note: The PCI Express* riser card is separately orderable as spare.

10. Environmental and Regulatory Specifications

10.1 System Level Environmental Limits

The following table defines the system level operating and non-operating environmental limits.

Table 47. System Office Environmental Summary

Parameter	Limits
Operating Temperature	+10°C to +35°C with the maximum rate of change not to exceed 10°C per hour
Non-Operating Temperature	-40°C to +70°C
Non-Operating Humidity	50%- 90%, non-condensing with a maximum wet bulb of 28°C
Acoustic noise	Sound Pressure: 55 dBA (Rackmount) in an idle state at typical office ambient temperature. (23°C +/- 2°C) Sound Power: 7.0 BA in an idle state at typical office ambient temperature. (23 +/- 2 degrees C)
Shock, operating	Half sine, 2 g peak, 11 mSec
Shock, unpackaged	Trapezoidal, 25 g, velocity change 136 inches/sec (≧40 lbs to > 80 lbs)
Shock, packaged	Non-palletized free fall in height 24 inches (≧40 lbs to > 80 lbs)
Vibration, unpackaged	5 Hz to 500 Hz, 2.20 g RMS random
Shock, operating	Half sine, 2 g peak, 11 mSec
ESD	+/-15kV except I/O port +/-8KV per Intel® Environmental test specification
System Cooling Requirement in BTU/Hr	2050 BTU/hour
EMI operating	Required to meet EMI emission requirements, tested as part of system

10.2 Serviceability and Availability

The system is designed to be serviced by qualified technical personnel only.

The desired Mean Time To Repair (MTTR) the system is 30 minutes, which includes diagnosing the system's problem. To meet this goal, the system enclosure and hardware was designed to minimize the MTTR.

The following are the maximum times a trained field service technician should take to perform the listed system maintenance procedures after diagnosing the system and identifying the failed component(s).

Table 48. Serviceability and Availability

Activity	Time Estimate
Remove and replace top cover	26 sec
Remove and replace hard disk drive	1 min
Remove and replace power supply module(include cable routing)	4 min 3sec
Remove and replace system fan(each)	1 min 10sec
Remove and replace backplane board(include cable routing)	8 min 20 sec
Remove and replace server board(include cable routing)	15 min 40 sec

10.3 Replacing the Backup Battery

The lithium battery on the server board powers the real time clock (RTC) for up to 10 years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

ADVARSEL!

Lithiumbatteri - Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

ADVARSEL

Lithiumbatteri - Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

10.4 Product Regulatory Compliance

The server chassis product, when correctly integrated per this guide, complies with the following safety and electromagnetic compatibility (EMC) regulations.

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation.

Notifications to Users on Product Regulatory Compliance and Maintaining Compliance – To ensure regulatory compliance, you must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products/components will void the UL listing and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in the region(s) in which the product is sold.

To help ensure EMC compliance with your local regional rules and regulations, before computer integration, make sure that the chassis, power supply, and other modules have passed EMC testing using a server board with a microprocessor from the same family (or higher) and operating at the same (or higher) speed as the microprocessor used on this server board. The final configuration of your end system product may require additional EMC

compliance testing. For more information please contact your local Intel Representative. This is an FCC Class A device and its use is intended for a commercial type market place.

10.5 Use of Specified Regulated Components

To maintain the UL listing and compliance to other regulatory certifications and/or declarations, the following regulated components must be used and conditions adhered to. Interchanging or use of other component will void the UL listing and other product certifications and approvals.

Updated product information for configurations can be found on the Intel Server Builder Web site at the following URL:
http://channel.intel.com/go/serverbuilder

If you do not have access to Intel's Web address, please contact your local Intel representative.

Server chassis (base chassis is provided with power supply and fans) – NRTL listed.
Server board – you must use an Intel server board – UL recognized.
Add-in boards – must have a printed wiring board flammability rating of minimum UL94V-1. Add-in boards containing external power connectors and/or lithium batteries must be UL recognized or UL listed. Any add-in board containing modem telecommunication circuitry must be UL listed. In addition, the modem must have the appropriate telecommunications, safety, and EMC approvals for the region in which it is sold.
Peripheral Storage Devices – must be UL recognized or UL listed accessory and TUV or VDE licensed. Maximum power rating of any one device or combination of devices can not exceed manufacturer's specifications. Total server configuration is not to exceed the maximum loading conditions of the power supply.

The following table references Server Chassis Compliance and markings that may appear on the product. Markings below are typical markings however, may vary or be different based on how certification is obtained.

Note: Certifications Emissions requirements are to Class A.

Table 49. Product Safety and Electromagnetic (EMC) Compliance

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
Australia/New Zealand	AS/NZS CISPR22 (Emissions)	 N232
Argentina	IRAM Certification (Safety)	
Canada/USA	CSA 60950 – UL 60950-1 (Safety) Listing	 3178574
	Industry Canada ICES-003 (Emissions)	CANADA ICES-003 CLASS A CANADA NMB-003 CLASSE A

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
	FCC CFR 47, Part 15 (Emissions)	This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept interference receive, including interference that may cause undesired operation.
CENELEC Europe Germany	Low Voltage Directive 2206/95/EC(Europe – EN60950-1); EMC Directive 2004/108/EEC EN55022 (Emissions) EN55024 (Immunity) EN61000-3-2 (Harmonics) EN61000-3-3 (Voltage Flicker) CE Declaration of Conformity GS Certification – EN60950-1	CE Intertek GS
International	CB Certification – IEC60950-1 CISPR 22/CISPR 24	None Required.
Japan	VCCI Certification	この装置は、クラス A 情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。VCCI-A
Korea	KCC Certification MIC Notice No. 1997-41 (EMC) & 1997-42 (EMI)	인증번호: CPU-SR1690(A)
Russia	GOST-R 50377-92 Certification GOST R 29216-91 (Emissions) GOST R 50628-95 (Immunity)	MO04
Ukraine	Ukraine Certification	None Required.
Taiwan	BSMI CNS13438	R33025 警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策

10.6 Electromagnetic Compatibility Notices

10.6.1 FCC Verification Statement (USA)

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etc.) that comply with FCC Class B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

10.6.2 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur : "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

(English translation of the notice above) This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications.

10.6.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

10.6.4 Japan EMC Compatibility

Electromagnetic Compatibility Notices (International)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:

This is a Class A product based on the standard of the Voluntary Control Council For Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

10.6.5 BSMI (Taiwan)

The BSMI Certification number and the following warning is located on the product safety label which is located on the bottom side (pedestal orientation) or side (rack mount configuration).

警告使用者：

這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策。

10.6.6 KCC (Korea)

Following is the KCC certification information for Korea.

인증번호 : CPU-SR1690 (A)

10.7 Rack Mount Installation Guidelines

Anchor the equipment rack: The equipment rack must be anchored to an unmovable support to prevent it from falling over when one or more servers are extended in front of the rack on slides. You must also consider the weight of any other device installed in the rack. A crush hazard exists should the rack tilt forward which could cause serious injury.
Temperature: The temperature, in which the server operates when installed in an equipment rack, must not go below 5 °C (41 °F) or rise above 40 °C (104 °F). Extreme fluctuations in temperature can cause a variety of problems in your server.
Ventilation: The equipment rack must provide sufficient airflow to the front of the server to maintain proper cooling. The rack must also include ventilation sufficient to exhaust a maximum of 1023 BTUs (British Thermal Units) per hour for the server. The rack selected and the ventilation provided must be suitable to the environment in which the server will be used.

10.7.1 If AC power supplies are installed:

Mains AC power disconnection: The AC power cord(s) is considered the mains disconnect for the server and must be readily accessible when installed. If the individual server power cord(s) will not be readily accessible for disconnection then you are responsible for installing an AC power disconnect for the entire rack unit. This main disconnect must be readily accessible, and it must be labeled as controlling power to the entire rack, not just to the server(s).
Grounding the rack installation: To avoid the potential for an electrical shock hazard, you must include a third wire safety ground conductor with the rack installation. If the server power cord is plugged into an AC outlet that is part of the rack, then you must provide proper grounding for the rack itself. If the server power cord is plugged into a wall AC outlet, the safety ground conductor in the power cord provides proper grounding only for the server. You must provide additional, proper grounding for the rack and other devices installed in it.
Overcurrent protection: The server is designed for an AC line voltage source with up to 20 amperes of overcurrent protection per cord feed. If the power system for the equipment rack is installed on a branch circuit with more than 20 amperes of protection, you must provide supplemental protection for the server.

10.7.2 If DC power supplies are installed:

Connection with a DC (Direct Current) source should only be performed by trained service personnel. The server with DC input is to be installed in a Restricted Access Location in accordance with articles 110-16, 110-17, and 110-18 of the National Electric Code, ANSI/NFPA 70. The DC source must be electrically isolated by double or reinforced insulation from any hazardous AC source.
Main DC power disconnect: You are responsible for installing a properly rated DC power disconnect for the server system. This mains disconnect must be readily accessible, and it must be labeled as controlling power to the server. The circuit breaker of a centralized DC power system may be used as a disconnect device when easily accessible and should be rated no more than 10 amps.
Grounding the server: To avoid the potential for an electrical shock hazard, you must reliably connect an earth grounding conductor to the server. The earth grounding conductor must be a minimum 18AWG connected to the earth ground stud(s) on the rear of the server. The safety ground conductor should be connected to the chassis stud with a Listed closed two-hole crimp terminal having 5/8 inch pitch. The nuts on the chassis earth ground studs should be installed with a 10 in/lbs torque. The safety ground conductor provides proper grounding only for the server. You must provide additional, proper grounding for the rack and other devices installed in it.
Overcurrent protection: Overcurrent protection circuit breakers must be provided as part of each host equipment rack and must be incorporated in the field wiring between the DC source and the server. The branch circuit protection shall be rated minimum 75Vdc, 10 A maximum per feed pair. If the DC power system for the equipment rack is installed with more than 10 amperes of protection, you must provide supplemental protection for the server.

10.8 Power Cord Usage Guidelines

Warning: *Do not attempt to modify or use an AC power cord set that is not the exact type required. You must use a power cord set that meets the following criteria:*
• *Rating: In the U.S. and Canada, cords must be UL (Underwriters Laboratories, Inc.) Listed/CSA (Canadian Standards Organization) Certified type SJT, 18-3 AWG (American Wire Gauge). Outside of the U.S. and Canada, cords must be flexible harmonized (<HAR>) or VDE (Verband Deutscher Electrotechniker, German Institute of Electrical Engineers) certified cord with 3 x 0.75 mm conductors rated 250 VAC (Volts Alternating Current).*

• Connector, wall outlet end: Cords must be terminated in grounding-type male plug designed for use in your region. The connector must have certification marks showing certification by an agency acceptable in your region and for U.S. must be Listed and rated 125% of overall current rating of the server.
• Connector, server end: The connectors that plug into the AC receptacle on the server must be an approved IEC (International Electrotechnical Commission) 320, sheet C13, type female connector.
• Cord length and flexibility: Cords must be less than 4.5 meters (14.76 feet) long.

10.9 Product Ecology Compliance

Intel has a system in place to restrict the use of banned substances in accordance with world wide product ecology regulatory requirements. The following is Intel's product ecology compliance criteria.

Table 50. Product Ecology Compliance

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
California	**CA. Lithium Perchlorate insert** California Code of Regulations, Title 22, Division 4.5; Chapter 33: Best Management Practices for Perchlorate Materials.	Special handling may apply. See www.dtsc.ca.gov/hazardouswaste/perchlorate This notice is required by California Code of Regulations, Title 22, Division 4.5; Chapter 33: Best Management Practices for Perchlorate Materials. This product/part includes a battery which contains Perchlorate material.
China	**China RoHS** China RoHS (MII Measure 39) Product marked with the Environmental Friendly Usage Period (EFUP) label of 20yrs, substance table in Simplified Chinese either placed with the product documentation or separate insert. **China Recycling (GB18455-2001)** Mark requires to be applied to be retail product only. Marking applied to bulk packaging and single packages. Not applied to internal packaging such as plastics, foams, etc.	 
Intel Internal Specification	All materials, parts and subassemblies must not contain restricted materials as defined in Intel's ***Environmental Product Content Specification*** of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm	None Required.
Europe	**Waste Electrical and Electronic Equipment (WEEE) Directive 2002/96/EC** – Mark applied to system level products only.	

Compliance Regional Description	Compliance Reference	Compliance Reference Marking Example
	European Directive 2002/95/EC - Restriction of Hazardous Substances (RoHS) Threshold limits and banned substances are noted below. Quantity limit of 0.1% by mass (1000 PPM) for: Lead, Mercury, Hexavalent Chromium, Polybrominated Biphenyls Diphenyl Ethers (PBB/PBDE) Quantity limit of 0.01% by mass (100 PPM) for: Cadmium	None Required.
Intel Internal Specification	All materials, parts and subassemblies must not contain restricted materials as defined in Intel's ***Environmental Product Content Specification*** of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm	None Required.
International	**ISO11469** – Plastic parts weighing >25gm are intended to be marked with per ISO11469.	>PC/ABS<
	Recycling Markings – Fiberboard (FB) and Cardboard (CB) are marked with international recycling marks. Applied to outer bulk packaging and single package.	 

10.10 Other Markings

Table 51. Other Markings

Compliance Description	Compliance Reference	Compliance Reference Marking Example
Stand-by Power	60950 Safety Requirement Applied to product is stand-by power switch is used.	
Multiple Power Cords	60950 Safety Requirement Applied to product if more than one power cord is used.	English: This unit has more than one power supply cord. To reduce the risk of electrical shock, disconnect (2) two power supply cords before servicing.
		Simplified Chinese: 注意： 本设备包括多条电源系统电缆。为避免遭受电击，在进行维修之前应断开两（2）条电源系统电缆。
		Traditional Chinese: 注意： 本設備包括多條電源系統電纜。爲避免遭受電擊，在進行維修之前應斷開兩（2）條電源系統電纜。
		German: Dieses Geräte hat mehr als ein Stromkabel. Um eine Gefahr des elektrischen Schlages zu verringern trennen sie beide (2) Stromkabeln bevor Instandhaltung.

Compliance Description	Compliance Reference	Compliance Reference Marking Example
Ground Connection	60950 Deviation for Nordic Countries	Line1 : "WARNING:" Swedish on line2: "Apparaten skall anslutas till jordat uttag, när den ansluts till ett nätverk." Finnish on line 3: "Laite on liitettävä suojamaadoituskoskettimilla varustettuun pistorasiaan." English on line 4: "Connect only to a properly earth grounded outlet."
Country of Origin	Logistic Requirements. Applied to products to indicate where product was made.	Made in China.

Appendix A: Integration and Usage Tips

Before attempting to integrate and configure your system, you should reference this section, which provides a list of useful information.

- After the system is integrated with processors, memory, and peripheral devices, the FRUSDR utility **must** be run to load the proper Sensor Data Record data to the integrated Server Management subsystem. Failure to run this utility may prevent Server Management from accurately monitoring system health and may affect system performance. The FRUSDR utility for this server system can either be run from the Intel Deployment CDROM that came with your system, or can be downloaded from the Intel website referenced at the bottom of this page.

- To ensure the highest system reliability, make sure the latest system software is loaded on the server before deploying the system onto a live networking environment. This includes system BIOS, FRUSDR, BMC firmware, and hot-swap controller firmware. The system software can be updated using the Intel Deployment CDROM that came with your system or can be downloaded from the Intel website referenced at the bottom of this page.

- System fans are not hot-swappable.

- Only supported memory validated by Intel should be used in this server system. A list of supported memory can be found in the Intel® Server System SR1690WB Tested Memory List which can be downloaded from the Intel website referenced at the bottom of this page.

- This system supports the Intel® Xeon® processor 5500 and 5600 sequence. Table 2 in this document provides a list of supported processors. You cannot use Intel® Xeon® processors not referenced on the supported processor list in this server system.

- You must use the CPU/memory air duct to maintain system thermals.

- To maintain system thermals, you must populate all hard drive bays with either a hard drive or drive blank.

- You must remove power from the system prior to opening the chassis for service

You can download the latest system documentation, drivers, and system software from the Intel Support website http://www.intel.com/p/en_US/support/highlights/server/s5500wb.

Appendix B: POST Code LED Decoder

During the system boot process, the BIOS executes a number of platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the POST code to the POST Code Diagnostic LEDs on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, you can use the diagnostic LEDs to identify the last POST process executed.

Each POST code is represented by the eight amber diagnostic LEDs. The POST codes are divided into two nibbles, an upper nibble and a lower nibble. The upper nibble bits are represented by diagnostic LEDs #4, #5, #6, and #7. The lower nibble bits are represented by diagnostics LEDs #0, #1, #2, and #3. If the bit is set in the upper and lower nibbles, then the corresponding LED is lit. If the bit is clear, then the corresponding LED is off.

The diagnostic LED #7 is labeled as “MSB” (Most Significant Bit), and the diagnostic LED #0 is labeled as “LSB” (Least Significant Bit).

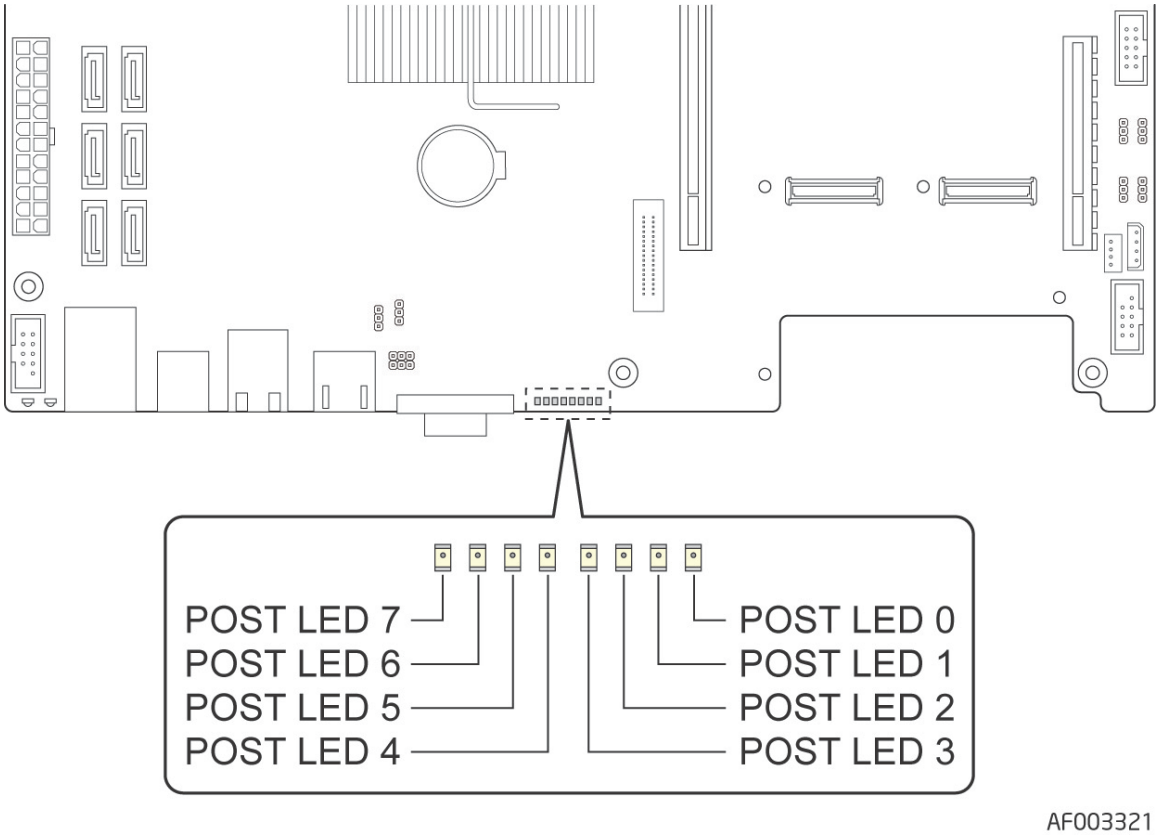


Figure 28. Diagnostic LED Placement Diagram

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

Table 52. POST Progress Code LED Example

LEDs	Upper Nibble LEDs				Lower Nibble LEDs			
	MSB							LSB
	LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
	8h	4h	2h	1h	8h	4h	2h	1h
Status	ON	OFF	ON	OFF	ON	ON	OFF	OFF
Results	**1**	0	**1**	0	**1**	**1**	0	0
	Ah				**Ch**			

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh.

Table 53. POST Progress Code LED Example

Checkpoint	Diagnostic LED Decoder 1 = On, 0=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
Host Processor									
0x10h	0	0	0	1	0	0	0	0	Power-on initialization of the host processor (bootstrap processor)
0x11h	0	0	0	1	0	0	0	1	Host processor cache initialization (including AP)
0x12h	0	0	0	1	0	0	1	0	Starting application processor initialization
0x13h	0	0	0	1	0	0	1	1	SMM initialization
0x14h	0	0	0	1	0	1	0	0	Selection of Processor with least features to be used as Boot Strap Processor
0x15h	0	0	0	1	0	1	0	1	Switch an AP processor to become the new Boot Strap Processor
Chipset									
0x21h	0	0	1	0	0	0	0	1	Initializing a chipset component
Memory									
0x22h	0	0	1	0	0	0	1	0	Reading configuration data from memory (SPD on FBDIMM)
0x23h	0	0	1	0	0	0	1	1	Detecting presence of memory
0x24h	0	0	1	0	0	1	0	0	Programming timing parameters in the memory controller
0x25h	0	0	1	0	0	1	0	1	Configuring memory parameters in the memory controller
0x26h	0	0	1	0	0	1	1	0	Optimizing memory controller settings
0x27h	0	0	1	0	0	1	1	1	Initializing memory, such as ECC init
0x28h	0	0	1	0	1	0	0	0	Testing memory
0xE4h	1	1	1	0	0	1	0	0	BIOS cannot communicate with DIMM (serial channel hardware failure)
0xE6h	1	1	1	0	0	1	1	0	DIMM(s) failed Memory iBIST or Memory Link Training failure
0xE8h	1	1	1	0	1	0	0	0	No memory available (system halted)
0xE9h	1	1	1	0	1	0	0	1	Unsupported or invalid DIMM configuration (system halted)
0xEAh	1	1	1	0	1	0	1	0	DIMM training sequence failed (system halted)
0xEBh	1	1	1	0	1	0	1	1	Memory test failed (system halted)
0xECh	1	1	1	0	1	1	0	0	Unsupported or invalid DIMM configuration (system halted)
0xEDh	1	1	1	0	1	1	0	1	Unsupported or invalid DIMM configuration (system halted)
0xEBh	1	1	1	0	1	0	1	1	DIMM with corrupted SPD data detected (system halted)
QuickPath Interconnect (QPI)									
0xA0h	1	0	1	0	0	0	0	0	QPI Initialization
0xA1h	1	0	1	0	0	0	0	1	QPI Initialization
0xA2h	1	0	1	0	0	0	1	0	QPI Initialization
0xA3h	1	0	1	0	0	0	1	1	QPI Initialization
0xA4h	1	0	1	0	0	1	0	0	QPI Initialization
0xA5h	1	0	1	0	0	1	0	1	QPI Initialization
0xA6h	1	0	1	0	0	1	1	0	QPI Initialization
0xA7h	1	0	1	0	0	1	1	1	QPI Initialization
0xA8h	1	0	1	0	1	0	0	0	QPI Initialization
0xA9h	1	0	1	0	1	0	0	1	QPI Initialization
0xAAh	1	0	1	0	1	0	1	0	QPI Initialization
0xABh	1	0	1	0	1	0	1	1	QPI Initialization
0xACh	1	0	1	0	1	1	0	0	QPI Initialization
0xADh	1	0	1	0	1	1	0	1	QPI Initialization
0xAEh	1	0	1	0	1	1	1	0	QPI Initialization
0xAFh	1	0	1	0	1	1	1	1	QPI Initialization
Integrated Memory Controller (IMC)									
0xB0h	1	0	1	1	0	0	0	0	Memory Initialization of Integrated Memory Controller
0xB1h	1	0	1	1	0	0	0	1	Memory Initialization of Integrated Memory Controller
0xB2h	1	0	1	1	0	0	1	0	Memory Initialization of Integrated Memory Controller
0xB3h	1	0	1	1	0	0	1	1	Memory Initialization of Integrated Memory Controller
0xB4h	1	0	1	1	0	1	0	0	Memory Initialization of Integrated Memory Controller

Checkpoint	Diagnostic LED Decoder 1 = On, 0=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
0xB5h	1	0	1	1	0	1	0	1	Memory Initialization of Integrated Memory Controller
0xB6h	1	0	1	1	0	1	1	0	Memory Initialization of Integrated Memory Controller
0xB7h	1	0	1	1	0	1	1	1	Memory Initialization of Integrated Memory Controller
0xB8h	1	0	1	1	1	0	0	0	Memory Initialization of Integrated Memory Controller
0xB9h	1	0	1	1	1	0	0	1	Memory Initialization of Integrated Memory Controller
0xBAh	1	0	1	1	1	0	1	0	Memory Initialization of Integrated Memory Controller
0xBBh	1	0	1	1	1	0	1	1	Memory Initialization of Integrated Memory Controller
0xBCh	1	0	1	1	1	1	0	0	Memory Initialization of Integrated Memory Controller
0xBDh	1	0	1	1	1	1	0	1	Memory Initialization of Integrated Memory Controller
0xBEh	1	0	1	1	1	1	1	0	Memory Initialization of Integrated Memory Controller
0xBFh	1	0	1	1	1	1	1	1	Memory Initialization of Integrated Memory Controller
PCI Bus									
0x50h	0	1	0	1	0	0	0	0	Enumerating PCI buses
0x51h	0	1	0	1	0	0	0	1	Allocating resources to PCI buses
0x52h	0	1	0	1	0	0	1	0	Hot Plug PCI controller initialization
0x53h	0	1	0	1	0	0	1	1	Reserved for PCI bus
0x54h	0	1	0	1	0	1	0	0	Reserved for PCI bus
0x55h	0	1	0	1	0	1	0	1	Reserved for PCI bus
USB									
0x56h	0	1	0	1	0	1	1	0	Initializing USB host controllers
0x57h	0	1	0	1	0	1	1	1	Detecting USB devices
0x58h	0	1	0	1	1	0	0	0	Resetting USB bus
0x59h	0	1	0	1	1	0	0	1	Reserved for USB devices
ATA/ATAPI/SATA									
0x5Ah	0	1	0	1	1	0	1	0	Resetting SATA bus and all devices
0x5Bh	0	1	0	1	1	0	1	1	Detecting the presence of ATA device
0x5Ch	0	1	0	1	1	1	0	0	Enable SMART if supported by ATA device
0x5Dh	0	1	0	1	1	1	0	1	Reserved for ATA
SMBUS									
0x5Eh	0	1	0	1	1	1	1	0	Resetting SMBUS
0x5Fh	0	1	0	1	1	1	1	1	Reserved for SMBUS
I/O Controller Hub									
0x61h	0	1	1	0	0	0	0	1	Initializing I/O Controller Hub
Super I/O									
0x63h	0	1	1	0	0	0	1	1	Initializing Super I/O
Local Console									
0x70h	0	1	1	1	0	0	0	0	Resetting the video controller (VGA)
0x71h	0	1	1	1	0	0	0	1	Disabling the video controller (VGA)
0x72h	0	1	1	1	0	0	1	0	Enabling the video controller (VGA)
0x73h	0	1	1	1	0	0	1	1	Reserved for video controller (VGA)
Remote Console									
0x78h	0	1	1	1	1	0	0	0	Resetting the console controller
0x79h	0	1	1	1	1	0	0	1	Disabling the console controller
0x7Ah	0	1	1	1	1	0	1	0	Enabling the console controller
0x7Bh	0	1	1	1	1	0	1	1	Reserved for console controller
Keyboard (only USB)									
0x90h	1	0	0	1	0	0	0	0	Resetting the keyboard
0x91h	1	0	0	1	0	0	0	1	Disabling the keyboard
0x92h	1	0	0	1	0	0	1	0	Detecting the presence of the keyboard
0x93h	1	0	0	1	0	0	1	1	Enabling the keyboard
0x94h	1	0	0	1	0	1	0	0	Clearing keyboard input buffer
0x96h	1	0	0	1	0	1	1	0	Reserved for keyboard
Mouse (only USB)									
0x98h	1	0	0	1	0	0	1	0	Resetting the mouse
0x99h	1	0	0	1	0	0	1	1	Detecting the mouse
0x9Ah	1	0	0	1	0	1	1	0	Detecting the presence of mouse

Checkpoint	Diagnostic LED Decoder 1 = On, 0=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
0x9Bh	1	0	0	1	0	1	1	1	Enabling the mouse
0x9Ch	1	0	0	1	0	0	1	0	Reserved for mouse
Serial Port									
0xA8h	1	0	1	0	1	0	0	0	Resetting the serial port
0xA9h	1	0	1	0	1	0	0	1	Disabling the serial port
0xAAh	1	0	1	0	1	0	1	0	Detecting the presence of the serial port
0xABh	1	0	1	0	1	0	1	1	Clearing serial port buffer
0xACh	1	0	1	0	1	1	0	0	Enabling serial port
0xADh	1	0	1	0	1	1	0	1	Reserved for serial port
Fixed Media									
0xB0h	1	0	1	1	0	0	0	0	Resetting fixed media device
0xB1h	1	0	1	1	0	0	0	1	Disabling fixed media device
0xB2h	1	0	1	1	0	0	1	0	Detecting presence of a fixed media device (SATA hard drive detection, and so forth)
0xB3h	1	0	1	1	0	0	1	1	Enabling/configuring a fixed media device
0xB4h	1	0	1	1	0	1	0	0	Reserved for fixed media
Removable Media									
0xB8h	1	0	1	1	1	0	0	0	Resetting removable media device
0xB9h	1	0	1	1	1	0	0	1	Disabling removable media device
0xBAh	1	0	1	1	1	0	1	0	Detecting presence of a removable media device (SATA CDROM detection, and so forth)
0xBCh	1	0	1	1	1	1	0	0	Enabling/configuring a removable media device
0xBDh	1	0	1	1	1	1	0	1	Reserved for removable media device
Boot Device Selection (BDS)									
0xD0	1	1	0	1	0	0	0	0	Entered the Boot Device Selection phase (BDS)
0xD1	1	1	0	1	0	0	0	1	Return to last good boot device
0xD2	1	1	0	1	0	0	1	0	Setup boot device selection policy
0xD3	1	1	0	1	0	0	1	1	Connect boot device controller
0xD4	1	1	0	1	0	1	0	0	Attempt flash update boot mode
0xD5	1	1	0	1	0	1	0	1	Transfer control to EFI boot
0xD6	1	1	0	1	0	1	1	0	Trying to boot device selection
0xDF	1	1	0	1	1	1	1	1	Reserved for boot device selection
Pre-EFI Initialization (PEI) Core									
0xE0h	1	1	1	0	0	0	0	0	Entered Pre-EFI Initialization phase (PEI)
0xE1h	1	1	1	0	0	0	0	1	Started dispatching early initialization modules (PEIM)
0xE2h	1	1	1	0	0	0	1	0	Initial memory found, configured, and installed correctly
0xE3h	1	1	1	0	0	0	1	1	Transfer control to the DXE Core
PEI Modules									
0xF0h	1	1	1	1	0	0	0	0	Install PEIM for Platform Status Codes
0xF1h	1	1	1	1	0	0	0	1	Detecting Platform Type
0xF2h	1	1	1	1	0	0	1	0	Early Platform Initialization
0xF3h	1	1	1	1	0	0	1	1	PEI Modules initialized
Driver eXecution Environment (DXE) Core									
0xE4h	1	1	1	0	0	1	0	0	Entered EFI driver execution phase (DXE)
0xE5h	1	1	1	0	0	1	0	1	Started dispatching drivers
0xE6h	1	1	1	0	0	1	1	0	Started connecting drivers
DXE Drivers									
0xE7h	1	1	1	0	1	1	0	1	Waiting for user input
0xE8h	1	1	1	0	1	0	0	0	Checking password
0xE9h	1	1	1	0	1	0	0	1	Entering BIOS setup
0xEAh	1	1	1	0	1	1	0	0	Flash Update
0xEBh	1	1	1	0	1	1	0	1	Legacy Option ROM initialization
0xECh	1	1	1	0	1	0	0	0	DXE Drivers initialized
0xEDh	1	1	1	0	1	0	0	1	Transfer control to Boot Device Selection (BDS)
0xEEh	1	1	1	0	1	1	0	0	Calling Int 19. One beep unless silent boot is enabled.
0xEFh	1	1	1	0	1	1	0	1	Unrecoverable boot failure
Pre-EFI Initialization Module (PEIM)/Recovery									

Checkpoint	Diagnostic LED Decoder 1 = On, 0=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
0x30h	0	0	**1**	**1**	0	0	0	0	Crisis recovery initiated because of a user request
0x31h	0	0	**1**	**1**	0	0	0	**1**	Crisis recovery initiated by software (corrupt flash)
0x34h	0	0	**1**	**1**	0	**1**	0	0	Loading crisis recovery capsule
0x35h	0	0	**1**	**1**	0	**1**	0	1	Handing off control to the crisis recovery capsule
0x36h	0	0	**1**	**1**	0	**1**	**1**	0	Begin crisis recovery
0x3Eh	0	0	**1**	**1**	**1**	**1**	**1**	0	No crisis recovery capsule detected
0x3Fh	0	0	**1**	**1**	**1**	**1**	**1**	**1**	Crisis recovery capsule failed integrity check of capsule descriptors

Appendix C: Video POST Code Errors

Whenever possible, the BIOS outputs the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The Response section in the following table is divided into three types:

No Pause: The message is displayed on the local Video screen during POST or in the Error Manager. The system continues booting with a degraded state. The user may want to replace the erroneous unit. The setup POST error Pause setting does not have any effect with this error.

Pause: The message is displayed on the Error Manager screen, and an error is logged to the SEL. The setup POST error Pause setting determines whether the system pauses to the Error Manager for this type of error, where the user can take immediate corrective action or choose to continue booting.

Halt: The message is displayed on the Error Manager screen, an error is logged to the SEL, and the system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system. The setup POST error Pause setting does not have any effect with this error.

Table 54. POST Error Message and Handling

Error Code	Error Message	Response
0012	CMOS date/time not set	Pause
0048	Password check failed	Halt
0108	Keyboard component encountered a locked error	No Pause
0109	Keyboard component encountered a stuck key error	No Pause
0113	Fixed Media The SAS RAID firmware can not run properly. The user should attempt to re-flash the firmware.	Pause
0140	PCI component encountered a PERR error	Pause
0141	PCI resource conflict	Pause
0146	PCI out of resources error	Pause
0192	L3 cache size mismatch	Halt
0194	CPUID, processor family are different	Halt
0195	Front side bus mismatch	Pause
0196	Processor model mismatch	Pause
0197	Processor speed mismatch	Pause
0198	Processor family is unsupported	Pause
019F	Processor and chipset stepping configuration is unsupported	Pause
5220	CMOS/NVRAM configuration cleared	Pause
5221	Password cleared by jumper	Pause
5224	Password clear jumper is set	Pause
8110	Processor 01 internal error (IERR) on last boot	Pause
8111	Processor 02 internal error (IERR) on last boot	Pause
8120	Processor 01 thermal trip error on last boot	Pause
8121	Processor 02 thermal trip error on last boot	Pause
8130	Processor 01 disabled	Pause
8131	Processor 02 disabled	Pause
8140	Processor 01 Failed FRB-3 Timer.	No Pause
8141	Processor 02 Failed FRB-3 Timer.	No Pause
8160	Processor 01 unable to apply BIOS update	Pause
8161	Processor 02 unable to apply BIOS update	Pause
8170	Processor 01 failed Self Test (BIST).	Pause

Error Code	Error Message	Response
8171	Processor 02 failed Self Test (BIST).	Pause
8180	Processor 01 BIOS does not support the current stepping for processor	No Pause
8181	Processor 02 BIOS does not support the current stepping for processor	No Pause
8190	Watchdog timer failed on last boot	Pause
8198	Operating system boot watchdog timer expired on last boot	Pause
8300	Integrated Baseboard Management Controller failed self-test	Pause
84F2	Integrated Baseboard Management Controller failed to respond	Pause
84F3	Integrated Baseboard Management Controller in update mode	Pause
84F4	Sensor data record empty	Pause
84FF	System event log full	No Pause
8500	Memory component could not be configured in the selected RAS mode.	Pause
8520	DIMM_A1 failed Self Test (BIST).	Pause
8521	DIMM_A2 failed Self Test (BIST).	Pause
8522	DIMM_A3 failed Self Test (BIST).	Pause
8523	DIMM_A4 failed Self Test (BIST).	Pause
8524	DIMM_B1 failed Self Test (BIST).	Pause
8525	DIMM_B2 failed Self Test (BIST).	Pause
8526	DIMM_B3 failed Self Test (BIST).	Pause
8527	DIMM_B4 failed Self Test (BIST).	Pause
8528	DIMM_C1 failed Self Test (BIST).	Pause
8529	DIMM_C2 failed Self Test (BIST).	Pause
852A	DIMM_C3 failed Self Test (BIST).	Pause
852B	DIMM_C4 failed Self Test (BIST).	Pause
852C	DIMM_D1 failed Self Test (BIST).	Pause
852D	DIMM_D2 failed Self Test (BIST).	Pause
852E	DIMM_D3 failed Self Test (BIST).	Pause
852F	DIMM_D4 failed Self Test (BIST).	Pause
8540	DIMM_A1 Disabled.	Pause
8541	DIMM_A2 Disabled.	Pause
8542	DIMM_A3 Disabled.	Pause
8543	DIMM_A4 Disabled.	Pause
8544	DIMM_B1 Disabled.	Pause
8545	DIMM_B2 Disabled.	Pause
8546	DIMM_B3 Disabled.	Pause
8547	DIMM_B4 Disabled.	Pause
8548	DIMM_C1 Disabled.	Pause
8549	DIMM_C2 Disabled.	Pause
854A	DIMM_C3 Disabled.	Pause
854B	DIMM_C4 Disabled.	Pause
854C	DIMM_D1 Disabled.	Pause
854D	DIMM_D2 Disabled.	Pause
854E	DIMM_D3 Disabled.	Pause
854F	DIMM_D4 Disabled.	Pause
8560	DIMM_A1 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8561	DIMM_A2 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8562	DIMM_A3 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8563	DIMM_A4 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8564	DIMM_B1 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8565	DIMM_B2 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8566	DIMM_B3 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8567	DIMM_B4 Component encountered a Serial Presence Detection (SPD) fail error.	Pause

Error Code	Error Message	Response
8568	DIMM_C1 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8569	DIMM_C2 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856A	DIMM_C3 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856B	DIMM_C4 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856C	DIMM_D1 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856D	DIMM_D2 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856E	DIMM_D3 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
856F	DIMM_D4 Component encountered a Serial Presence Detection (SPD) fail error.	Pause
8580	DIMM_A1 Correctable ECC error encountered.	Pause after 10 Occurrence
8581	DIMM_A2 Correctable ECC error encountered.	Pause after 10 Occurrence
8582	DIMM_A3 Correctable ECC error encountered.	Pause after 10 Occurrence
8583	DIMM_A4 Correctable ECC error encountered.	Pause after 10 Occurrence
8584	DIMM_B1 Correctable ECC error encountered.	Pause after 10 Occurrence
8585	DIMM_B2 Correctable ECC error encountered.	Pause after 10 Occurrence
8586	DIMM_B3 Correctable ECC error encountered.	Pause after 10 Occurrence
8587	DIMM_B4 Correctable ECC error encountered.	Pause after 10 Occurrence
8588	DIMM_C1 Correctable ECC error encountered.	Pause after 10 Occurrence
8589	DIMM_C2 Correctable ECC error encountered.	Pause after 10 Occurrence
858A	DIMM_C3 Correctable ECC error encountered.	Pause after 10 Occurrence
858B	DIMM_C4 Correctable ECC error encountered.	Pause after 10 Occurrence
858C	DIMM_D1 Correctable ECC error encountered.	Pause after 10 Occurrence
858D	DIMM_D2 Correctable ECC error encountered.	Pause after 10 Occurrence
858E	DIMM_D3 Correctable ECC error encountered.	Pause after 10 Occurrence
858F	DIMM_D4 Correctable ECC error encountered.	Pause after 10 Occurrence
85A0	DIMM_A1 Uncorrectable ECC error encountered.	Pause
85A1	DIMM_A2 Uncorrectable ECC error encountered.	Pause
85A2	DIMM_A3 Uncorrectable ECC error encountered.	Pause
85A3	DIMM_A4 Uncorrectable ECC error encountered.	Pause
85A4	DIMM_B1 Uncorrectable ECC error encountered.	Pause
85A5	DIMM_B2 Uncorrectable ECC error encountered.	Pause
85A6	DIMM_B3 Uncorrectable ECC error encountered.	Pause
85A7	DIMM_B4 Uncorrectable ECC error encountered.	Pause
85A8	DIMM_C1 Uncorrectable ECC error encountered.	Pause
85A9	DIMM_C2 Uncorrectable ECC error encountered.	Pause
85AA	DIMM_C3 Uncorrectable ECC error encountered.	Pause
85AB	DIMM_C4 Uncorrectable ECC error encountered.	Pause
85AC	DIMM_D1 Uncorrectable ECC error encountered.	Pause

Error Code	Error Message	Response
85AD	DIMM_D2 Uncorrectable ECC error encountered.	Pause
85AE	DIMM_D3 Uncorrectable ECC error encountered.	Pause
85AF	DIMM_D4 Uncorrectable ECC error encountered.	Pause
8601	Override jumper is set to force boot from lower alternate BIOS bank of flash ROM	No Pause
8602	WatchDog timer expired (secondary BIOS may be bad!)	No Pause
8603	Secondary BIOS checksum fail	No Pause
8604	Chipset Reclaim of non critical variables complete.	No Pause
9000	Unspecified processor component has encountered a non specific error.	Pause
9223	Keyboard component was not detected.	No Pause
9226	Keyboard component encountered a controller error.	No Pause
9243	Mouse component was not detected.	No Pause
9246	Mouse component encountered a controller error.	No Pause
9266	Local Console component encountered a controller error.	No Pause
9268	Local Console component encountered an output error.	No Pause
9269	Local Console component encountered a resource conflict error.	No Pause
9286	Remote Console component encountered a controller error.	No Pause
9287	Remote Console component encountered an input error.	No Pause
9288	Remote Console component encountered an output error.	No Pause
92A3	Serial port component was not detected	Pause
92A9	Serial port component encountered a resource conflict error	Pause
92C6	Serial Port controller error	No Pause
92C7	Serial Port component encountered an input error.	No Pause
92C8	Serial Port component encountered an output error.	No Pause
94C6	LPC component encountered a controller error.	No Pause
94C9	LPC component encountered a resource conflict error.	Pause
9506	ATA/ATPI component encountered a controller error.	No Pause
95A6	PCI component encountered a controller error.	No Pause
95A7	PCI component encountered a read error.	No Pause
95A8	PCI component encountered a write error.	No Pause
9609	Unspecified software component encountered a start error.	No Pause
9641	PEI Core component encountered a load error.	No Pause
9667	PEI module component encountered an illegal software state error.	Halt
9687	DXE core component encountered an illegal software state error.	Halt
96A7	DXE boot services driver component encountered an illegal software state error.	Halt
96AB	DXE boot services driver component encountered invalid configuration.	No Pause
96E7	SMM driver component encountered an illegal software state error.	Halt
0xA022	Processor component encountered a mismatch error.	Pause
0xA027	Processor component encountered a low voltage error.	No Pause
0xA028	Processor component encountered a high voltage error.	No Pause
0xA421	PCI component encountered a SERR error.	Halt
0xA500	ATA/ATPI ATA bus SMART not supported.	No Pause
0xA501	ATA/ATPI ATA SMART is disabled.	No Pause
0xA5A0	PCI Express* component encountered a PERR error.	No Pause
0xA5A1	PCI Express* component encountered a SERR error.	Halt
0xA5A4	PCI Express* IBIST error.	Pause
0xA6A0	DXE boot services driver Not enough memory available to shadow a legacy option ROM.	No Pause

Appendix D: Jumper Block Settings and Usage

The server board has several 2-pin and 3-pin jumper blocks that can be used to configure, protect, or recover specific features of the server board. Pin 1 on each jumper block is denoted by an "*" or "▼".

Force IBMC Update (J1B5)

When performing a standard BMC firmware update procedure, the update utility places the BMC into an update mode, allowing the firmware to load safely onto the flash device. In the unlikely event the BMC firmware update process fails due to the BMC not being in the proper update state, the server board provides a BMC Force Update jumper (J1B5) which will force the BMC into the proper update state. The following procedure should be followed in the event the standard BMC firmware update process fails.

Table 55. Force IBMC Update (J1B5)

Jumper Position	Mode of Operation	Note
1-2	Normal	IBMC GPIO [1] is pulled HIGH. Default position.
2-3	Update	IBMC GPIO [1] is pulled LOW.

1. Power down and remove the AC power cord.
2. Open the server chassis. See your server chassis documentation for instructions.
3. Move jumper from the default operating position, covering pins1 and 2, to the enabled position, covering pins 2 and 3.
4. Close the server chassis.
5. Reconnect the AC cord and power up the server.
6. Perform the BMC firmware update procedure as documented in the README.TXT file included in the given BMC firmware update package. After successful completion of the firmware update process, the firmware update utility may generate an error stating the BMC is still in update mode.
7. Power down and remove the AC power cord.
8. Open the server chassis.
9. Move the jumper from the enabled position, covering pins 2 and 3 to the disabled position, covering pins 1 and 2.
10. Close the server chassis.
11. Reconnect the AC cord and power up the server.

Note: Normal BMC functionality is disabled with the Force BMC Update jumper is set to the enabled position. You should never run the server with the BMC Force Update jumper set in this position. You should only use this jumper setting when the standard firmware update process fails. This jumper should remain in the default/disabled position when the server is running normally.

Password Clear (J1C2)

The user sets this 3-pin jumper to clear the password.

Table 56. Password Clear (J1C2)

Jumper Position	Mode of Operation	Note
1-2	Normal	ICH10R INTRUDER# pin is pulled HIGH. Default position.
2-3	Clear Password	ICH10R INTRUDER# pin is pulled LOW.

1. Power down server. Do not unplug the power cord.
2. Open the chassis. For instructions, see your server chassis documentation.
3. Move jumper (J1B6) from the default operating position, covering pins 1 and 2, to the password clear position, covering pins 2 and 3.
4. Close the server chassis.
5. Power up the server, wait 10 seconds or POST completes.
6. Power down the server.
7. Open the chassis and move the jumper back to default position, covering pins 1 and 2.
8. Close the server chassis.
9. Power up the server.

BIOS Recovery Mode (J1C3)

The Intel® Server Board S5500WB uses BIOS recovery to repair the system BIOS from flash corruption in the main BIOS and Boot Block. This 3-pin jumper is used to reload the BIOS when the image is suspected to be corrupted. For directions on how to recover the BIOS, refer to the specific BIOS release notes.

Table 57. BIOS Recovery Mode (J1C3)

Jumper Position	Mode of Operation	Note
1-2	Normal	ICH10R GPIO [55] is pulled HIGH. Default position.
2-3	Recovery	ICH10R GPIO [55] is pulled LOW.

You can accomplish a BIOS recovery from the SATA CD and USB Mass Storage device. Please note that this platform does not support recovery from a USB floppy.

The recovery media must contain the following files under the root directory:

1. FVMAIN.FV
2. UEFI iFlash32 2.6 Build 9
3. *Rec.CAP
4. Startup.nsh (update accordingly to use proper *Rec.CAP file)

The BIOS starts the recovery process by first loading and booting to the recovery image file (FVMAIN.FV) on the root directory of the recovery media (SATA CD or USB disk).

This process takes place before any video or console is available. Once the system boots to this recovery image file (FVMAIN.FV), it boots automatically into the EFI Shell to invoke the Startup.nsh script and start the flash update application (IFlash32.efi).

IFlash32.efi requires the supporting BIOS Capsule image file (*Rec.CAP).

After the update is complete, a message displays, stating the "BIOS has been updated successfully". This indicates the recovery process is finished.

The user should then switch the recovery jumper back to normal operation and restart the system by performing a power cycle.

The following steps demonstrate this recovery process:

1. Power OFF the system.
2. Insert recovery media.
3. Switch the recovery jumper. Details regarding the jumper ID and location can be obtained from the Board EPS for that Platform.
4. Power ON the system.

5. The BIOS POST screen will appear displaying the progress, and the system automatically boots to the EFI SHELL.
6. The Startup.nsh file executes, and initiates the flash update (IFlash32.efi) with a new capsule file (*Rec.CAP). The regular IFlash message displays at the end of the process—once the flash update succeeds.
7. Power OFF the system, and revert the recovery jumper position to "normal operation".
8. Power ON the system.
9. Do NOT interrupt the BIOS POST during the first boot.

Reset BIOS Configuration (J1B4)

This jumper used to be the CMOS Clear jumper. Since the previous generation, the BIOS has moved CMOS data to the NVRAM region of the BIOS flash. The BIOS checks during boot to determine if the data in the NVRAM needs to be set to default.

Table 58. Reset BIOS Configuration (J1B4)

Jumper Position	Mode of Operation	Note
1-2	Normal	ICH10R RTCRST# pin is pulled HIGH. Default position.
2-3	Reset BIOS Configuration	ICH10R RTCRST# pin is pulled LOW.

1. Power down server. Do not unplug the power cord.
2. Open the server chassis. For instructions, see your server chassis documentation.
3. Move jumper (J1B4) from the default operating position, covering pins 1 and 2, to the reset/clear position, covering pins 2 and 3.
4. Wait five seconds.
5. Remove AC power.
6. Move the jumper back to default position, covering pins 1 and 2.
7. Close the server chassis.
8. Power up the server.

The CMOS is now cleared and you can reset it by going into the BIOS setup.

Note: Removing AC Power before performing the CMOS Clear operation causes the system to automatically power up and immediately power down, after the procedure is followed and AC power is re-applied. If this happens, remove the AC power cord again, wait 30 seconds, and re-install the AC power cord. Power-up the system and proceed to the <F2> BIOS Setup Utility to reset the desired settings.

Video Master (J6A3)

This jumper determines which video is the primary.

Table 59. Video Master (J6A3)

Jumper Position	Mode of Operation	Notes
1-2	Internal	Internal connector will override if both connectors are used.
2-3	External	External connector will override if both connectors are used.

J6A3, 1-2 jumpered: Internal video connector is primary, but video can come out of external video connector if you connect to it.

J6A3, 2-3 jumpered: External video connector is primary, but video can come out of internal video connector if you connect to it.

Serials Interface Setting (J6A2)

Table 60. Serials Interface Setting (J6A2)

Pins	Mode	Description
1 – 2	DCD to DTR	Data Carrier Detect
3 – 4	DSR to DTR	Data Set Ready

Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ASIC	Application Specific Integrated Circuit
ASMI	Advanced Server Management Interface
BIOS	Basic Input/Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
Byte	8-bit quantity.
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.)
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMP	Emergency Management Port
EPS	External Product Specification
ESB2-E	Enterprise South Bridge 2
FBD	Fully Buffered DIMM
FMB	Flexible Mother Board
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GB	1024MB
GPIO	General Purpose I/O
GTL	Gunning Transceiver Logic
HSC	Hot-Swap Controller
Hz	Hertz (1 cycle/second)
I^2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture
IBF	Input Buffer
ICH	I/O Controller Hub
ICMB	Intelligent Chassis Management Bus
IERR	Internal Error
IFB	I/O and Firmware Bridge
INTR	Interrupt
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
ITP	In-Target Probe
KB	1024 bytes
KCS	Keyboard Controller Style

Term	Definition
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB	1024KB
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
ms	milliseconds
MTTR	Memory Type Range Register
Mux	Multiplexor
NIC	Network Interface Controller
NMI	Nonmaskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm	Unit of electrical resistance
PEF	Platform Event Filtering
PEP	Platform Event Paging
PIA	Platform Information Area (This feature configures the firmware for the platform hardware)
PLD	Programmable Logic Device
PMI	Platform Management Interrupt
POST	Power-On Self Test
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
RMM2	Remote Management Module – 2nd generation
RMM2 NIC	Remote Management Module – 2nd generation dedicated management NIC
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board)
SDR	Sensor Data Record
SECC	Single Edge Connector Cartridge
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory
SEL	System Event Log
SIO	Server Input/Output
SMI	Server Management Interrupt (SMI is the highest priority nonmaskable interrupt)
SMM	Server Management Mode
SMS	Server Management Software
SNMP	Simple Network Management Protocol
TBD	To Be Determined
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
UTC	Universal time coordinate
VID	Voltage Identification
VRD	Voltage Regulator Down

Term	Definition
Word	16-bit quantity
ZIF	Zero Insertion Force

Reference Documents

Refer to the following documents for additional information:

- *Intel® Server Board S5500WB Technical Product Specification*
- *Intel® Dynamic PowerTechnology Node Manager 1.5 External Interface Specification using IPMI, 2007. Intel Corporation.*
- *Intel® Dynamic PowerTechnology Node Manager 1.5 External Interface Specification using IPMI, 2007*. Intel Corporation.
- *Node Power and Thermal Management Architecture Specification v1.5, rev.0.79. 2007*, Intel Corporation.
- *Intel® Server System Integrated Baseboard Management Controller Core External Product Specification, 2007 Intel* Corporation.
- *Intel® Thurley Server Platform Services IPMI Commands Specification, 2007.* Intel Corporation.
- *Intelligent Platform Management Bus Communications Protocol Specification, Version 1.0, 1998*. Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation.
- *Platform Environmental Control Interface (PECI) Specification, Version 2.0*. Intel Corporation
- *Platform Management FRU Information Storage Definition, Version 1.0, Revision 1.2, 2002.* Intel Corporation, Hewlett-Packard Company, NEC Corporation, Dell Computer Corporation. http://developer.intel.com/design/servers/ipmi/spec.htm
- ACPI 3.0: http://www.acpi.info/spec.htm
- IPMI 2.0
- *Data Center Management Interface Specification v1.0*, May 1, 2008.: www.intel.com/go/dcmi
- *PCI Bus Power Management Interface Specification 1.1*: http://www.pcisig.com/
- *PCI Express* Base Specification Rev 2.0* Dec06: http://www.pcisig.com/
- *PCI Express* Card Electromechanical Specification Rev 2.0*: http://www.pcisig.com/
- PMBus*: http://pmbus.org
- SATA 2.6: http://www.sata-io.org/
- SMBIOS 2.4
- SSI-EEB 3.0: http://www.ssiforum.org
- USB 1.1: http://www.usb.org
- USB 2.0: http://www.usb.org
- Microsoft Windows* Logo/SDG 3.0