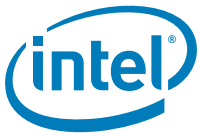

Intel® Server Board S5500BC

Technical Product Specification

Intel order number: E42249-003

Revision 1.0

January, 2009

Enterprise Platforms and Services Division - Marketing

Revision History

Date	Revision Number	Modifications
January 2009	1.0	Production Release

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Intel Corporation server baseboards support peripheral components and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel's own chassis are designed and tested to meet the intended thermal requirements of these components when the fully integrated system is used together. It is the responsibility of the system integrator that chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation can not be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

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1. Introduction

This Technical Product Specification (TPS) provides board-specific information about the features, functionality, and high-level architecture of the Intel® Server Board S5500BC.

The Intel® Server Board S5500BC may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Refer to the Intel® Server Board S5500BC Specification Update for published errata.

1.1 Server Board Use Disclaimer

Intel® Server Boards support add-in peripherals and contain high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2. Product Overview

The Intel® Server Board S5500BC is a monolithic printed circuit board (PCB) that supports the high-density 1U rack-mount server and 5U pedestal server market.

2.1 Feature Set

Feature	Description
Processors	LGA 1366 sockets supporting up to two Intel® Xeon® processor 5500 series with Intel® QuickPath Interconnect (QPI) and Integrated Memory controllers.
Memory	Eight DDR3 DIMM slots supporting DDR3 800/1066/1333 MT/s ECC Registered DIMM and ECC or Non-ECC unbuffered DIMM. Four slots support CPU_1 and four slots support CPU_2.
Chipset	• Intel® I/O Hub (IOH) 5500 chipset • Intel® 82801Jx I/O Controller Hub 10 Raid (ICH10R) • ServerEngines* LLC Pilot II BMC controller (Integrated BMC)
On-board Connectors / Headers	• Eight 240-Pin DDR3 DIMM connectors • Three PCI Express* Gen2 x8 connectors • One PCI Express* Gen1 x4 connector • One 5-V PCI 32-bit/33MHz connector • Two stacked RJ-45 connectors with Magnetics and LEDs and two USB combo connectors • One external Serial Port Header (9 pin) • Two internal USB 2x5 pin headers, each supports two USB 2.0 ports • One 24-pin main power connector • One 8-pin CPU power connector • One 5-pin auxiliary power connector • One DB-15 VGA connector • One DB-9 serial port connector • Six 7-pin SATA II connectors • One 4-pin SGPIO connector • Five 4-pin, 0.10” pitch fan headers • One 24-pin Front Panel connector • One 2-pin Chassis Intrusion header • One Intel® Remote Management Module 3 (RMM3)connector
Add-in PCI, PCI Express* Cards	Slot6: One half-length (6.6 inches) PCI Express* Gen2 x8 connector with X8 link width (support riser card) Slot7 : One half-length (6.6 inches) PCI Express* Gen2 x8 connector with x8 link width Slot5 : One half-length (6.6 inches) PCI Express* Gen2 x8 connector with x4 link width Slot3 : One half-length (6.6 inches) PCI Express* x4 connector with x4 link width Slot4 : One half-length (6.6 inches) 5V PCI 32 bit / 33 MHz connector
On-board Video	On-board ServerEngines* LLC Pilot II BMC controller ▪ Integrated 2D video controller ▪ 64 MB DDR2 667 MHz memory
Feature	**Description**

On-board Hard Drive Controller	Support up to six Serial ATA II hard drives through six on-board SATA II connectors
LAN	Two 10/100/1000 NICs ▪ One 82574LGbE PCI Express* Network Controller connects to the Gen2 x1 interface on the Intel® IOH 5500 chipset. ▪ One 82567 Gigabit Network Connection that connects to the Gigabit LAN Connect Interface / LAN Connect Interface on the Intel® ICH10R ▪ Two 10/100/1000 Base-TX Interfaces through RJ-45 connectors with integrated magnetics. ▪ Link and Speed LEDs on the RJ-45 Connector.
Fans	Five 4-pin fan headers supporting two processor fans and three system fans
USB	• Four USB 2.0 Ports connected to the Server Rear Panel • Four USB 2.0 Ports connected to Headers on the motherboard • One USB 1.1 Port connected to the Integrated BMC for KB/MS function • One USB 2.0 Port connected to the Integrated BMC for remote storage function
Power Supply	• One main power connector • On-board Power generation • VRD 11.1 processor Core Voltage • 1.2 V Regulator for Processor VTT • 1.1 V Regulator for IOH Core and I/O • 1.05 V Regulator for Intel® ICH10R Core • 1.5 V Regulator for the Intel® ICH10R • 1.5 V for DDR3 and 0.75V for DDR3 Termination • 3.3 V SB Voltage regulator • 1.8 V AUX, 1.2V AUX, and 0.9V AUX for the Integrated BMC and the DDR2 memory in it
System Management	• Processor on die temperature monitoring from the PECI interface • Board temperature measurement • Fan speed monitoring and control • Voltage monitoring • IPMI based server management

2.2 Server Board Layout

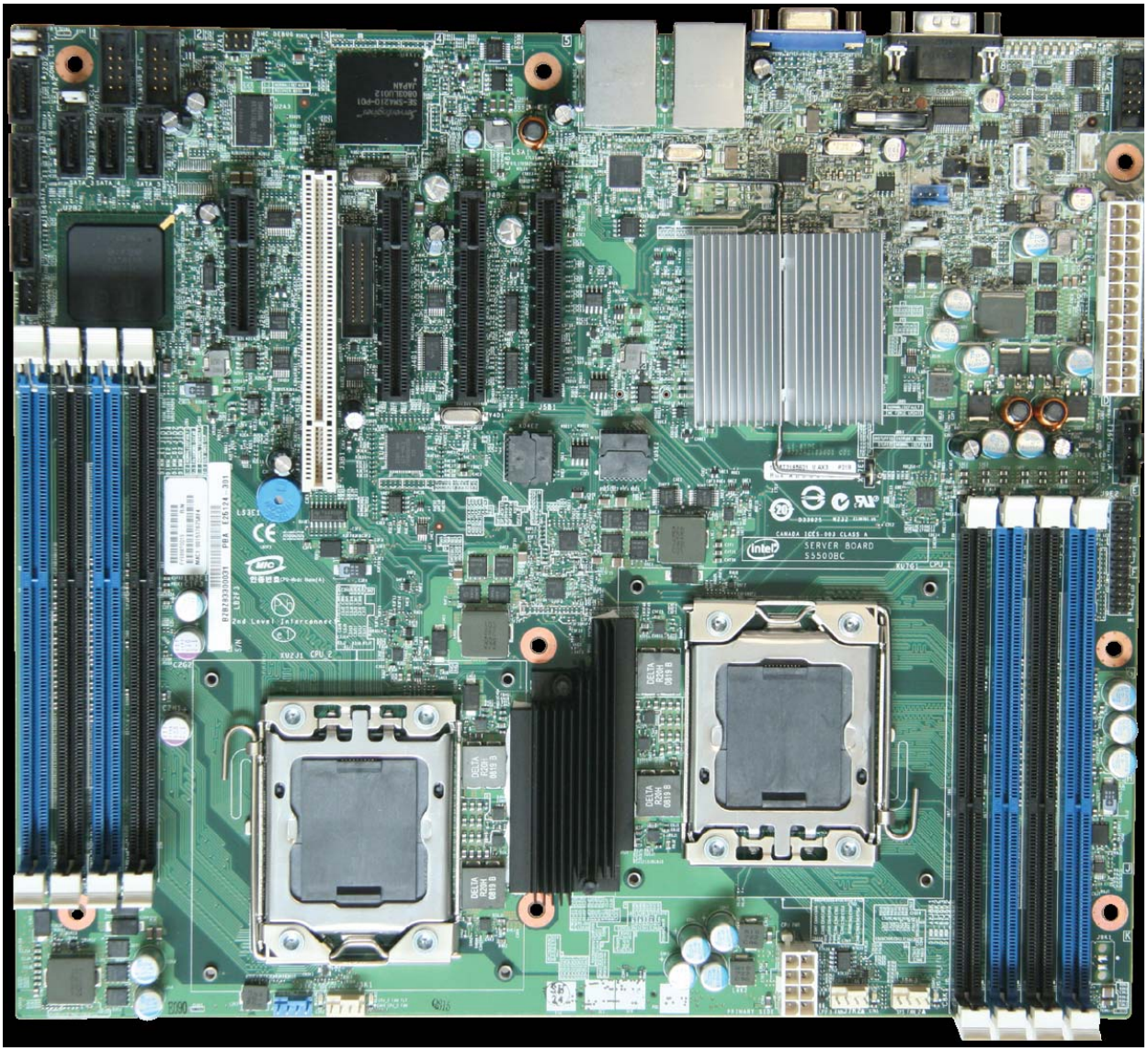


Figure 1. Intel® Server Board S5500BC picture

2.2.1 Server Board Connector and Component Layout

Figure 2 shows the board layout of the server board. Each connector and major component is identified by a number or letter, and a description is below the figure.

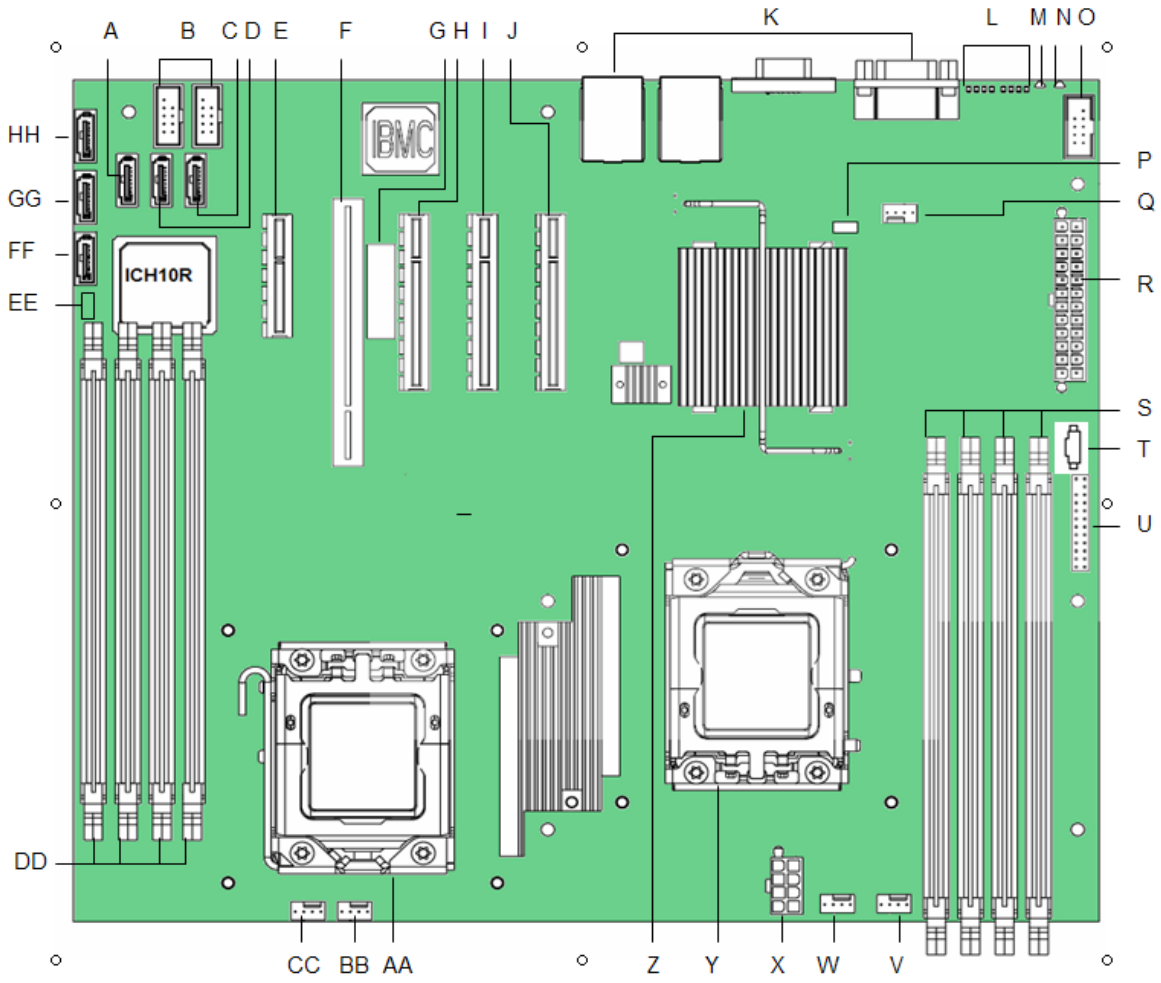


Figure 2. Intel® Server Board S5500BC Layout

Table 1. Board Layout reference

	Description		Description
A	SATA 3	B	Internal dual port USB2.0 header
C	SATA 5	D	SATA 4
E	Slot 3, PCI Express* x4	F	Slot 4, PCI 32 bit/33 MHz
G	Intel® RMM3 slot	H	Slot 5, PCI Express* x8
I	Slot 6, PCI Express* x8 (Riser card)	J	Slot 7, PCI Express* x8
K	Back panel I/O ports	L	Diagnostic LEDs
M	Status LED	N	ID LED
O	External Serial B header	P	SATA Key
Q	System fan 3 header	R	Main power connector
S	DIMM sockets for Channel A & B (Supports CPU_1)	T	Power Supply Auxiliary Connector
U	SSI 24 pin Front Panel connector	V	System fan 2 header
W	CPU_1 fan header	X	CPU Power Connector
Y	CPU_1 Socket	Z	Intel® IOH 5500 chipset

AA	CPU Socket 2	BB	CPU 2 fan header
CC	System fan 1 header	DD	DIMM sockets for Channel D and E (Supports CPU_2)
EE	SATA SGPIO	FF	SATA 0
GG	SATA 1	HH	SATA 2

2.2.2 Server Board Mechanical Drawing

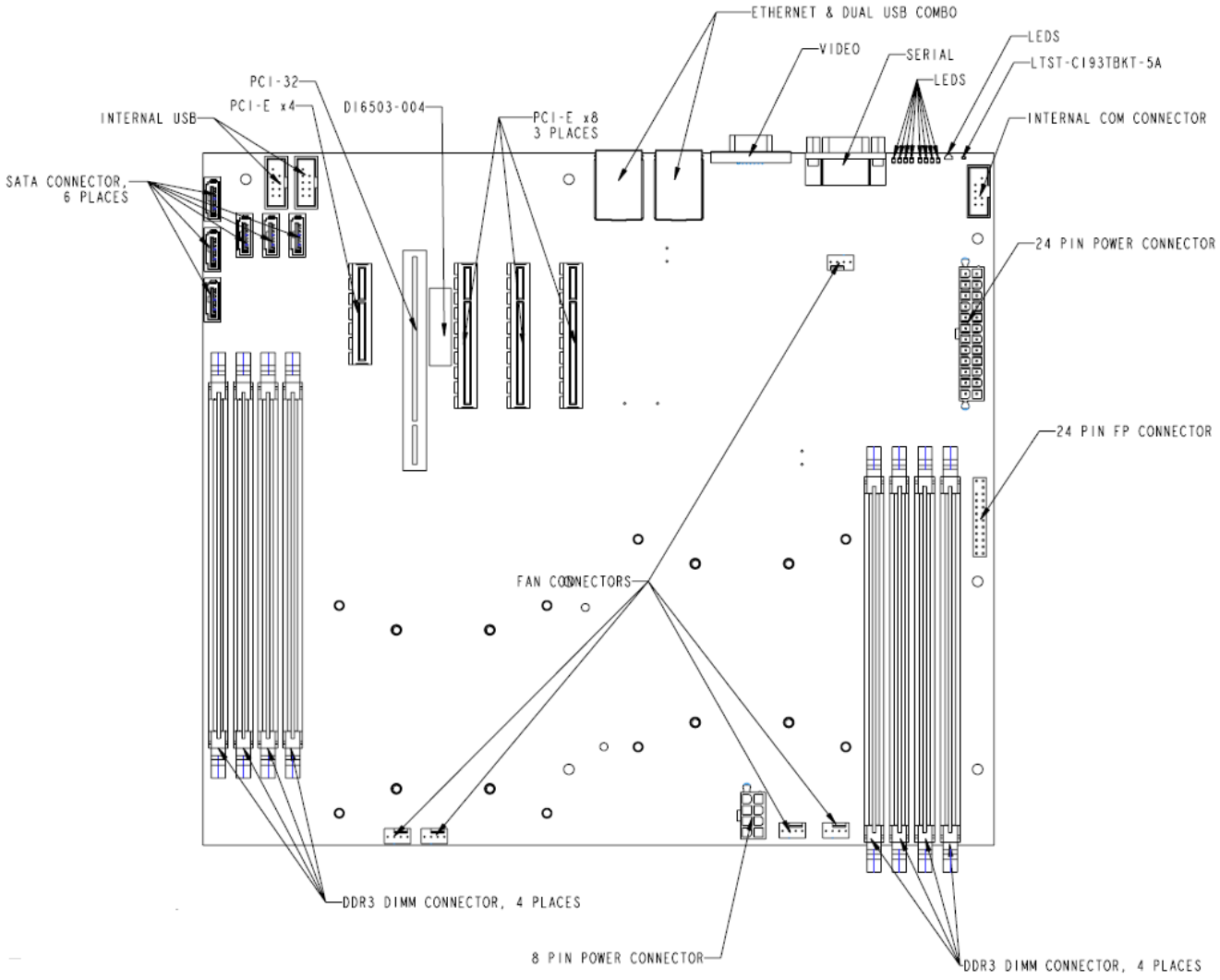


Figure 3. Key Connector and LED Indicator Identification

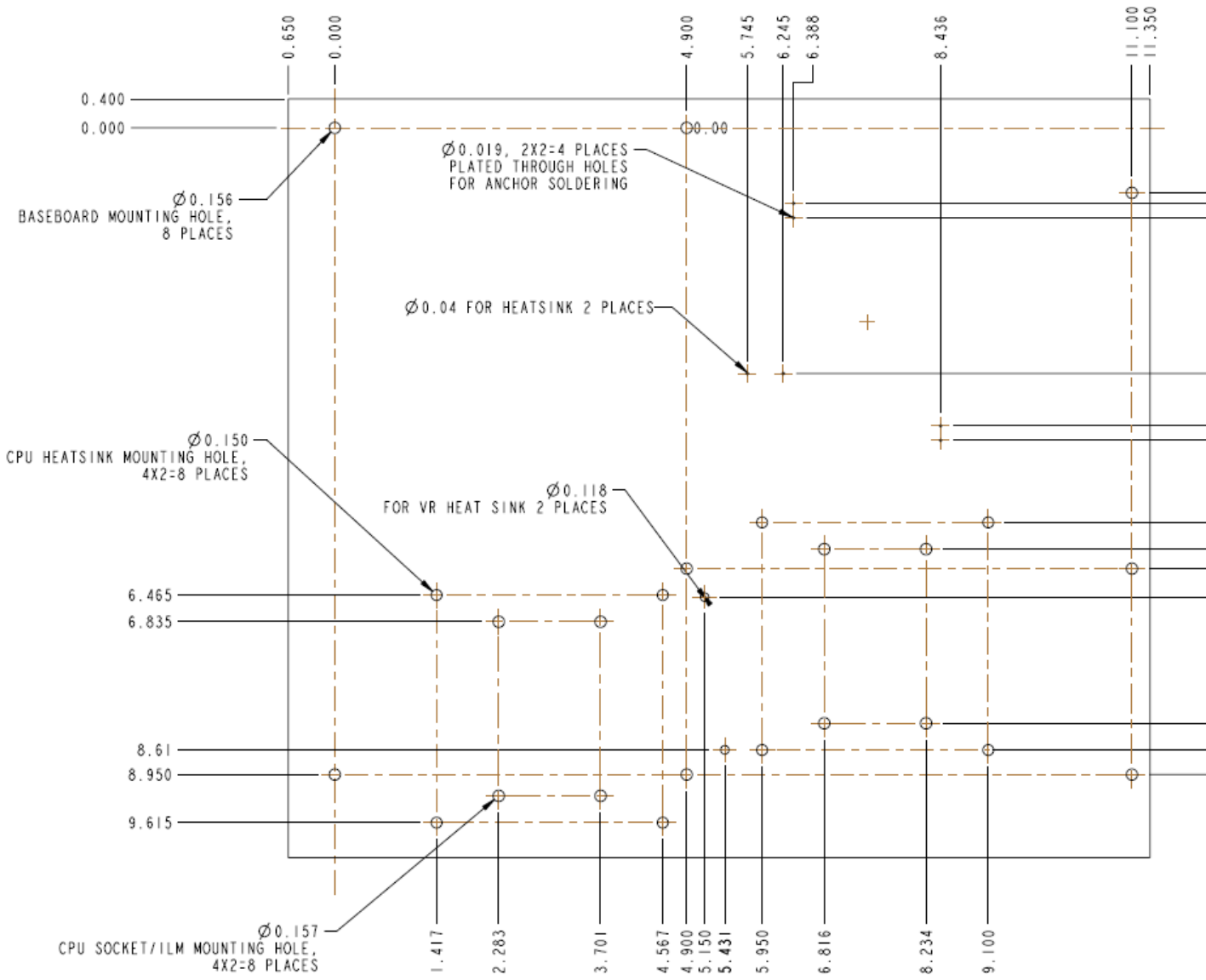


Figure 4. Mounting hole location

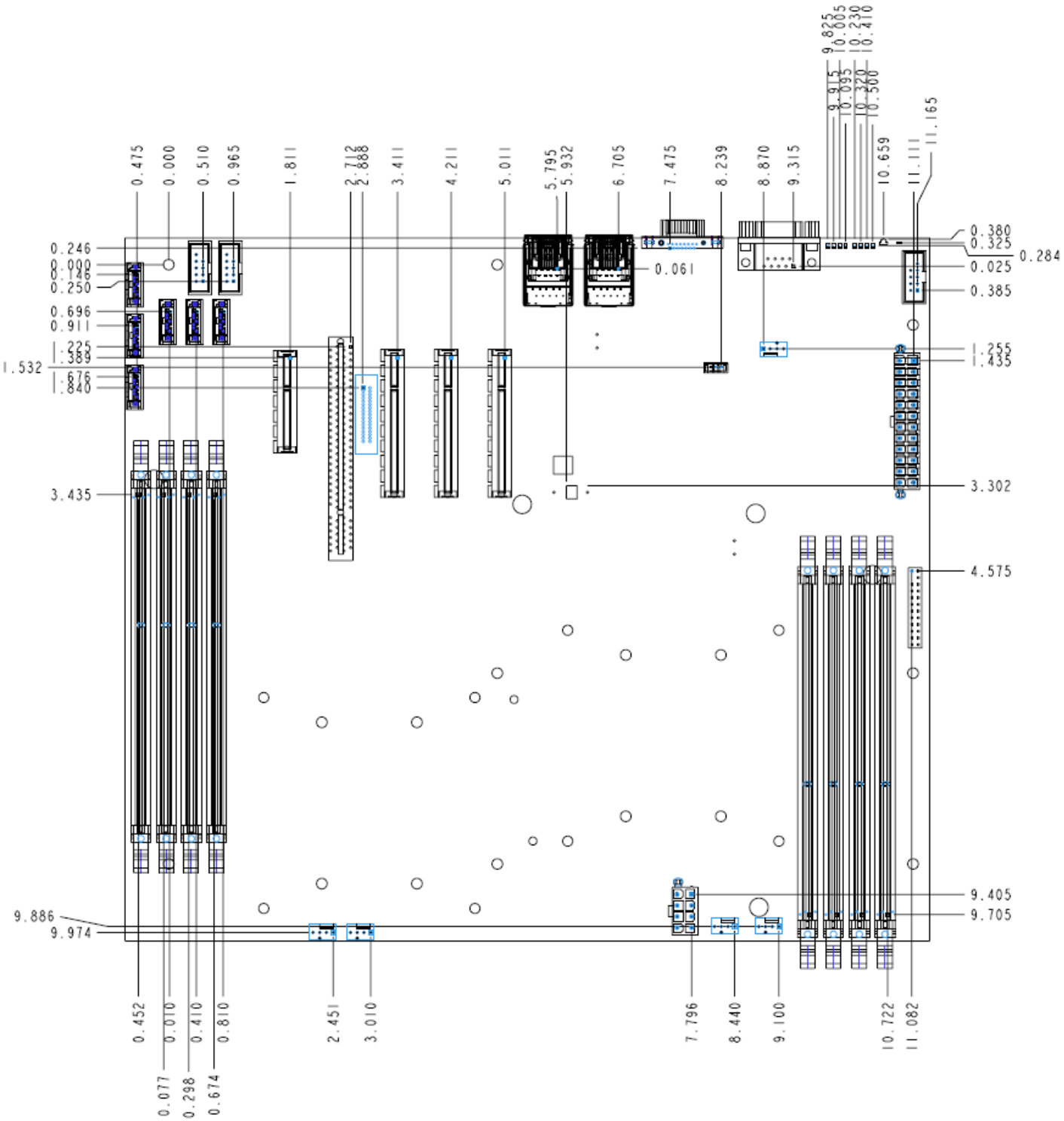


Figure 5. Major connector pin-1 locations

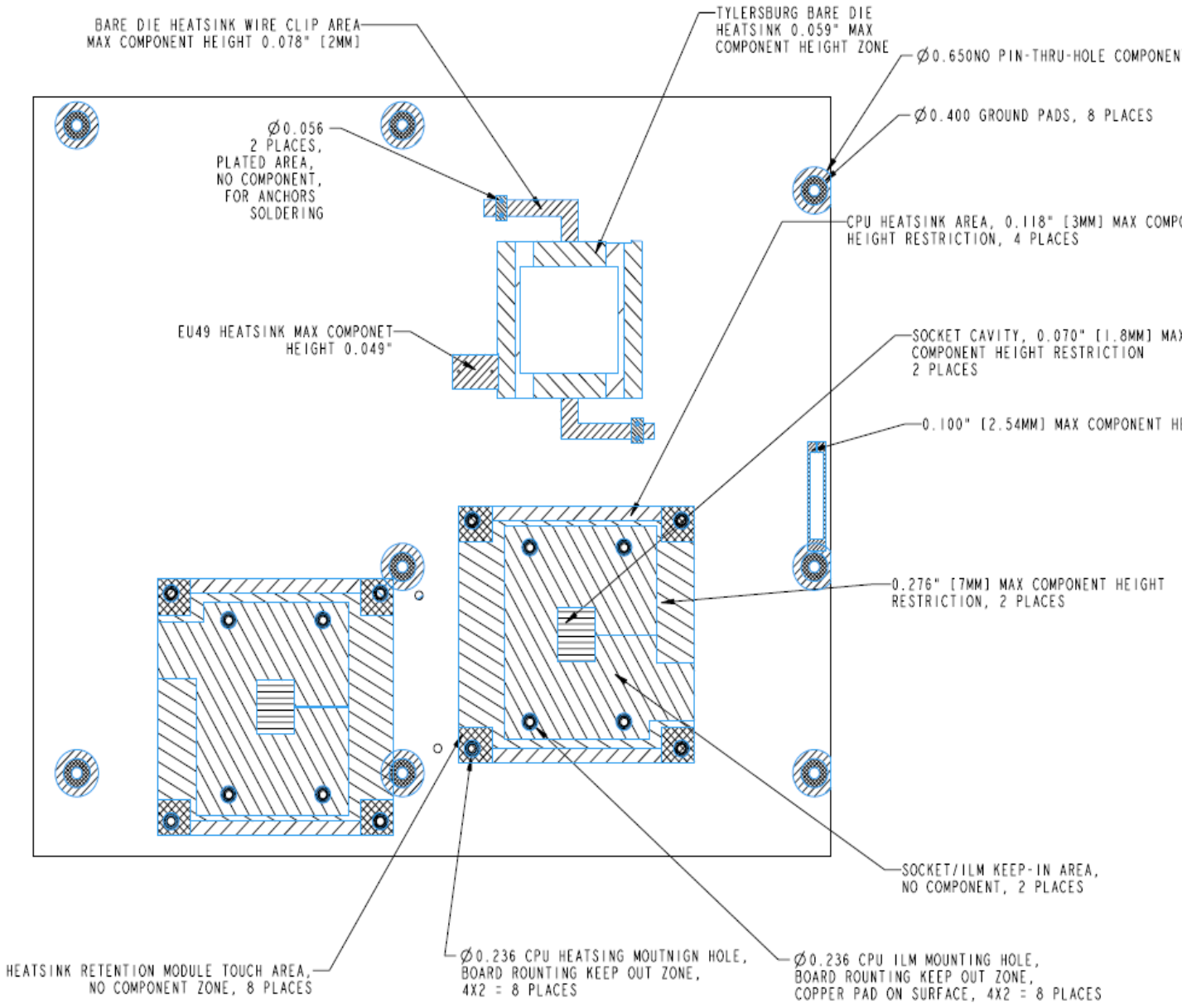


Figure 6. S5500BC Board Primary Side Keepouts

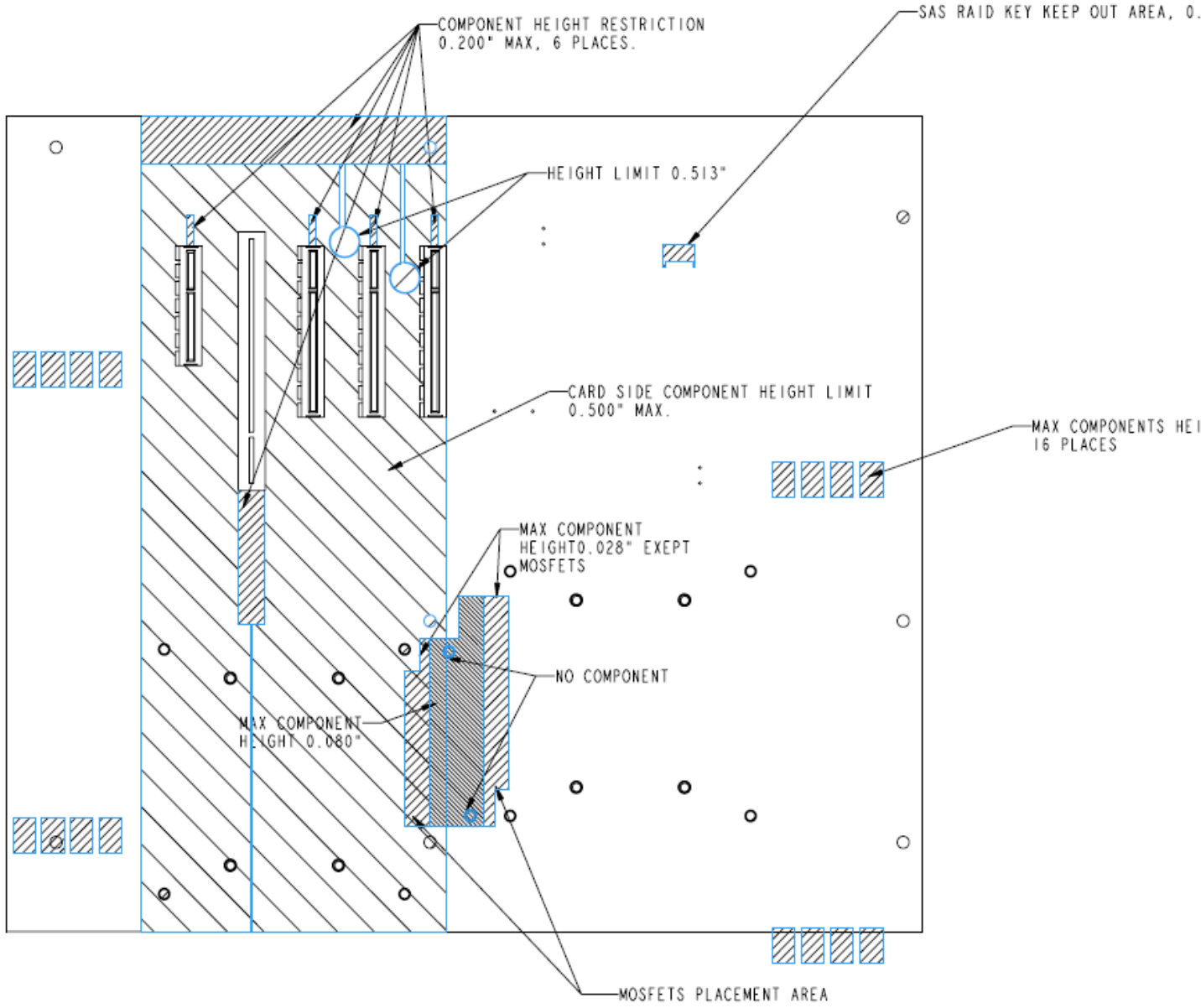


Figure 7. S5500BC Board PRIMARY SIDE CARD-SIDE KEEPOUT ZONE

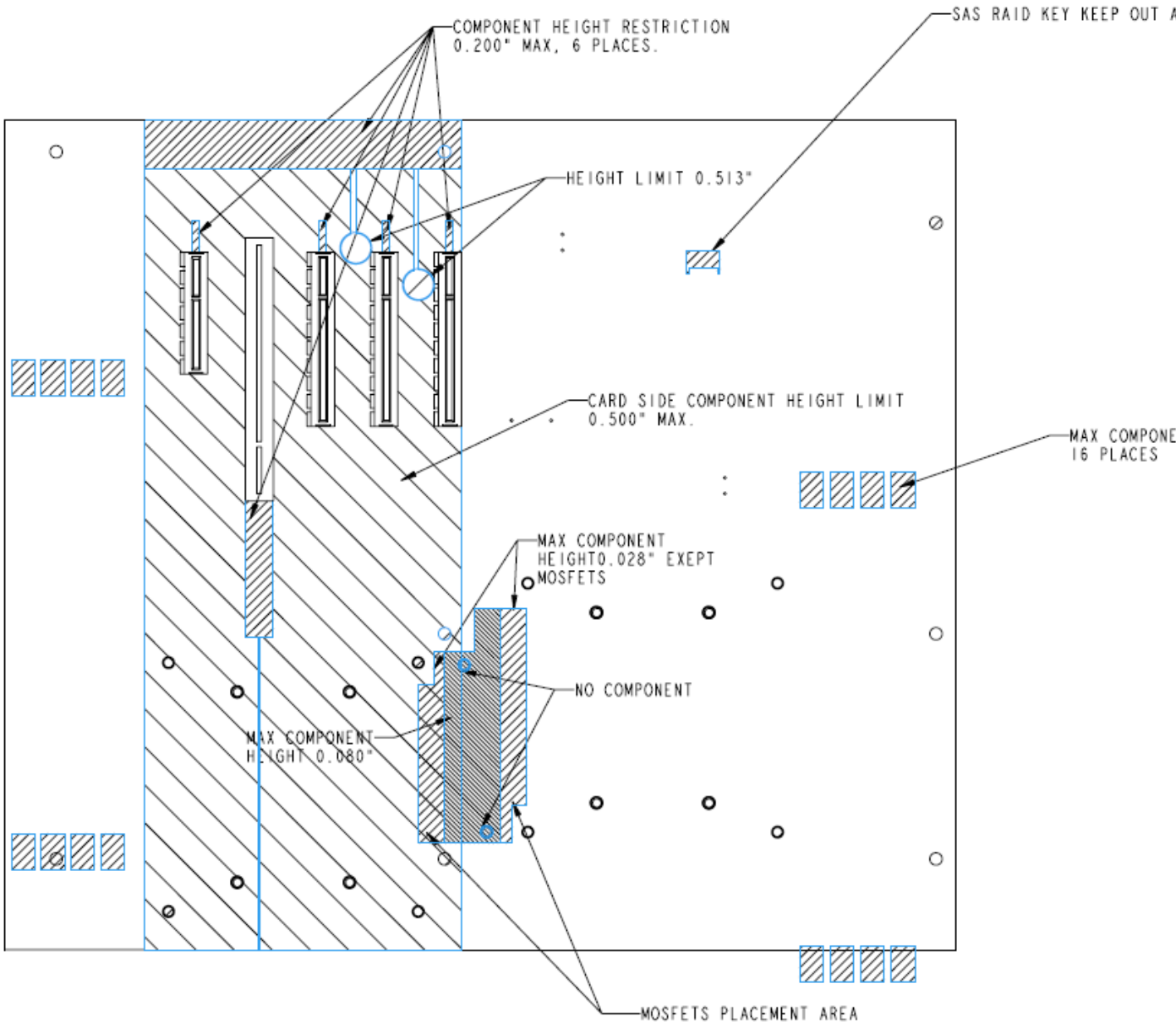


Figure 8. Secondary Side Keepout -- Mounting Hole Keepout

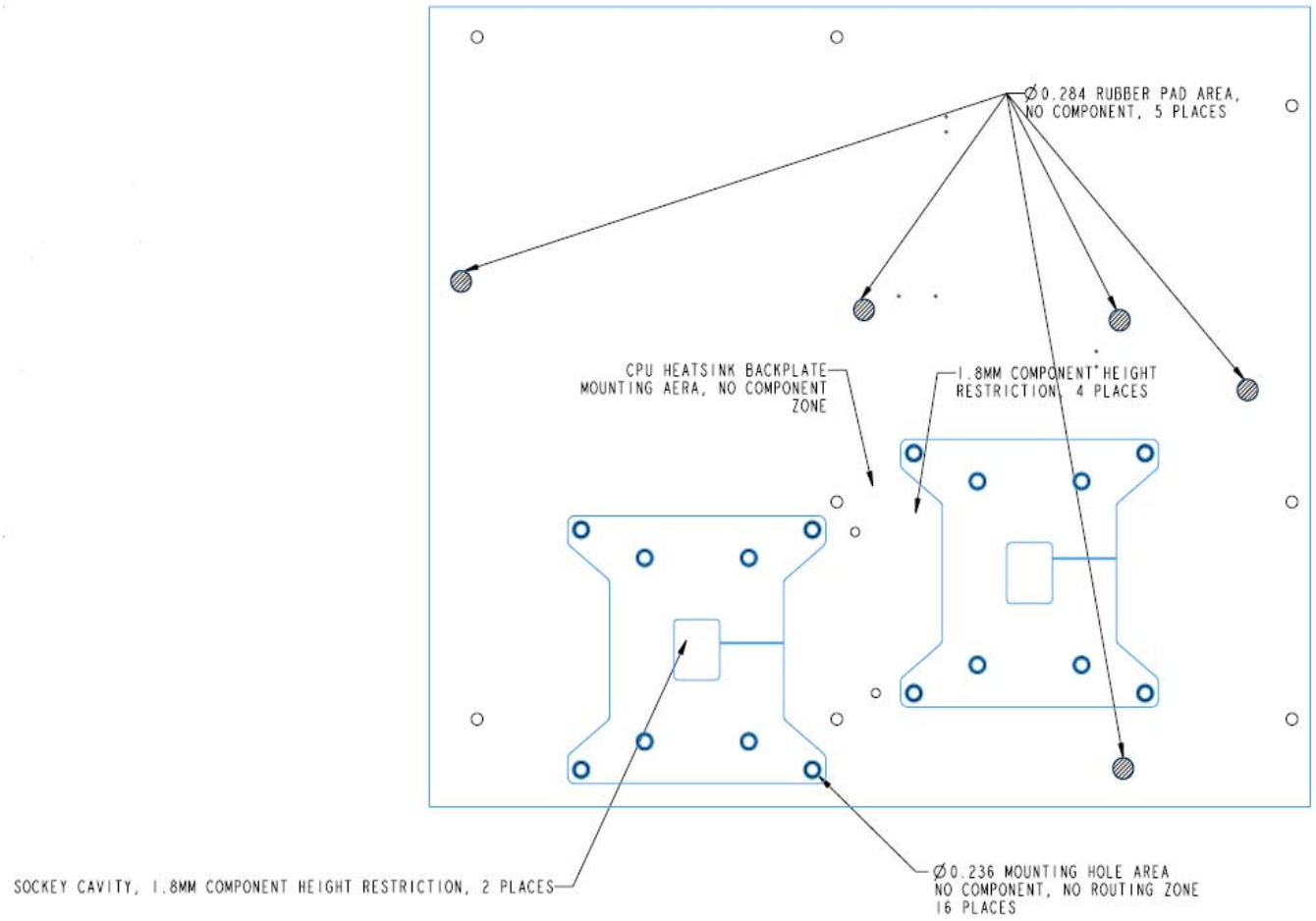


Figure 9. Secondary Side Keepout - CPU Socket and Rubber Pad Keepout

2.2.3 Intel® Light-Guided Diagnostic LED Locations

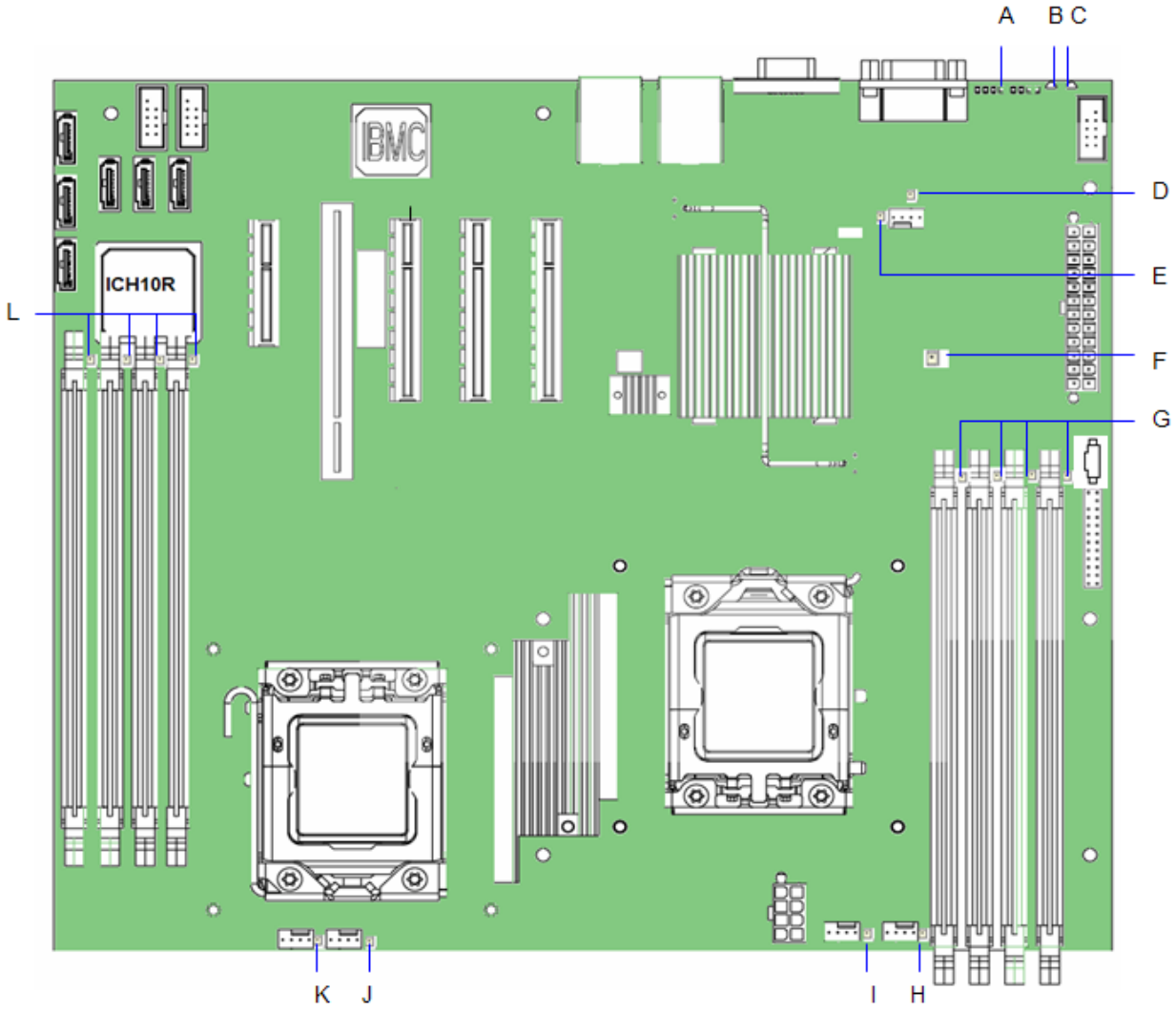


Figure 10. Intel® Light-Guided Diagnostic LED Locations

Table 2. Intel® Light-Guided Diagnostic LED reference

	Description		Description
A	Post-Code Diagnostic LEDs	B	Status LED
C	System ID LED	D	HDD LED
E	System Fan 3 Fault LED	F	5 VSB LED
G	DIMM Fault LED	H	System Fan 2 Fault LED
I	CPU 1 Fan Fault LED	J	CPU 2 Fan Fault LED
K	System Fan 1 Fault LED	L	DIMM Fault LED

2.2.4 External I/O Connector Locations

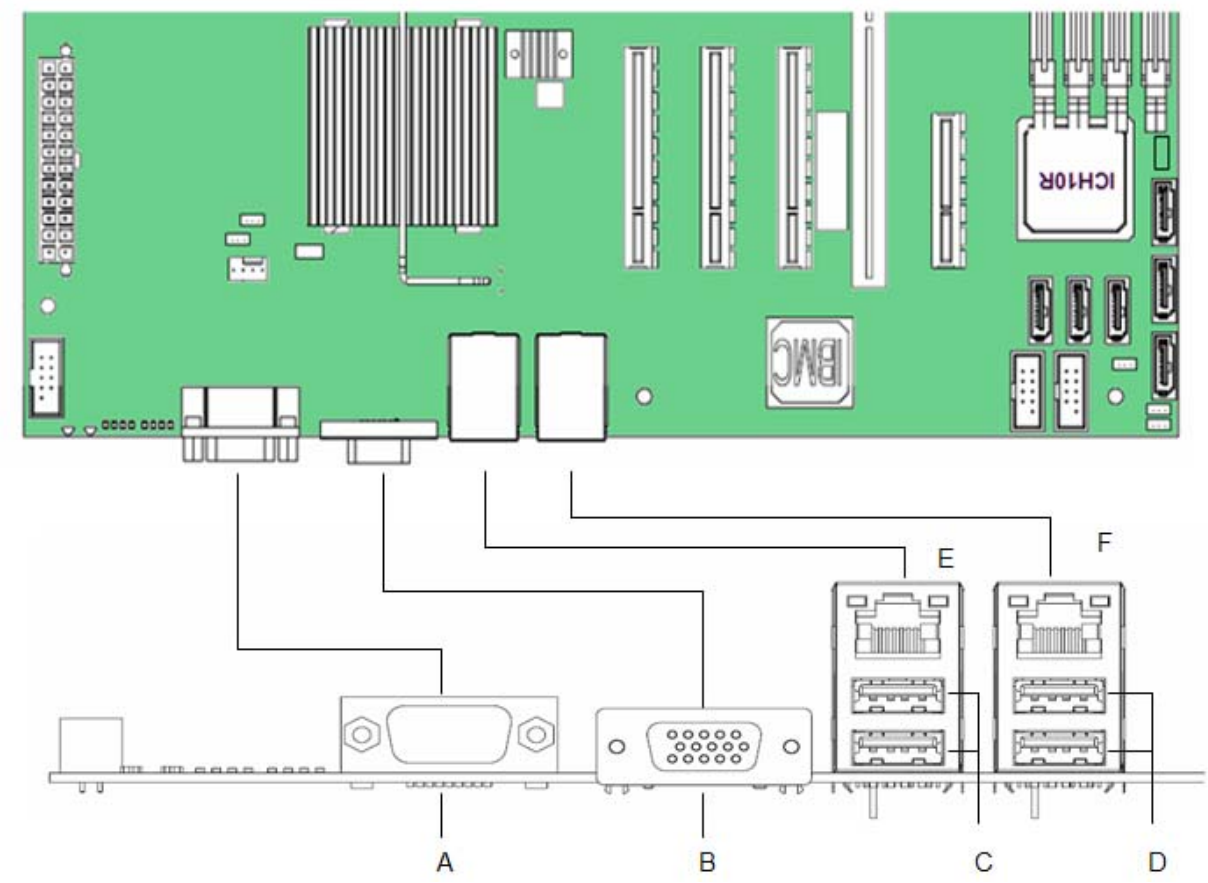


Figure 11. External I/O Layout

Table 3. External I/O Layout Reference

	Description		Description
A	Serial Port A	B	Video
C	USB Port 6-7	D	USB Port 8-9
E	NIC Port 1	F	NIC Port 2 (management port)

3. Functional Architecture

The architecture and design of the Intel® Server Board S5500BC is based on the Intel® 5500 chipset and the Intel® Xeon® processor 5500 family series. This chapter provides a high-level description of the functionality associated with each chipset component and the architectural blocks that make up this server board.

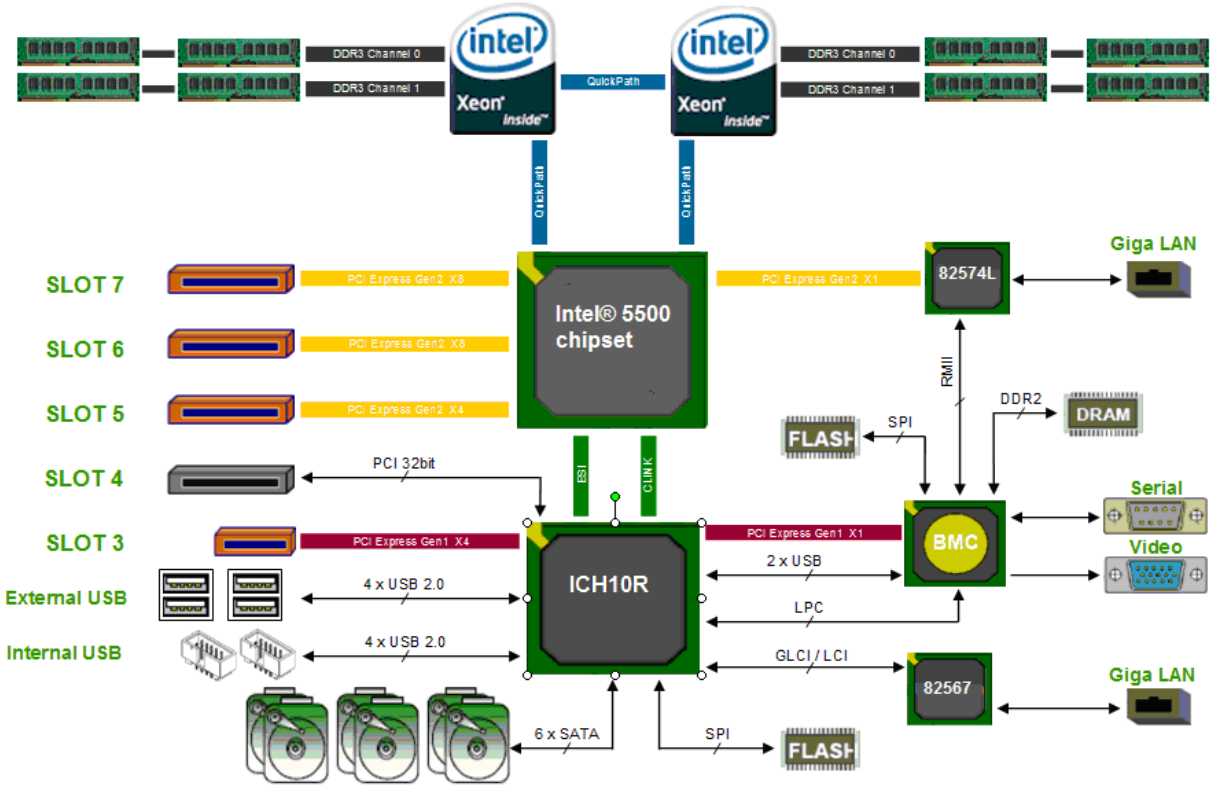


Figure 12. Functional Block Diagram

3.1 Processor Sub-system

The Intel® Xeon® processor 5500 series is the first generation server/workstation multi-core processor to implement the following key technologies:

- Integrated Memory Controller
- Point-to-point link interface based on Intel® QuickPath Interconnect (QPI)—formerly known as Common System Interface.

The processor is optimized for performance with the power efficiencies of a low-power micro architecture to produce smaller, quieter systems.

Table 4. Intel® Xeon® Processor 5500 Series Feature Set Overview

Feature	Intel® Xeon® Processor 5500 Series
Cache Sizes	Instruction Cache = 32 KB Data Cache = 32 KB 8 MB shared among cores (up to 4)
Data Transfer Rate	Two full-width Intel® QuickPath Interconnect links, up to 6.4 GT/s in each direction.
Multi-Core Support	Up to four cores per processor.
Dual Processor Support	Up to two processors per platform.
Package	1366-land FCLGA

The Intel® Server Board S5500BC supports Intel® Xeon® processor 5500 series with 95 W Thermal Design Power (TDP) or less and with a maximum data transfer rate of 6.4 GT/s.

3.1.1 Intel® QuickPath Interconnect (QPI)

Intel® QuickPath Interconnect (QPI) is a cache-coherent, link-based interconnect specification developed by Intel to connect processor, chipset and I/O bridge components. The Intel® IOH 5500 chipset is the first dual-processor server/workstation platform to implement Intel® QuickPath Interconnect links. Figure 6 provides a platform overview of the Intel® IOH 5500 chipset with Intel® QuickPath Interconnect implementation.

The Intel® IOH 5500 chipset supports up to two processor sockets, with up to four cores per socket. With Intel® QuickPath Interconnect, caching agents are responsible for participating in the cache coherence protocol, and home agents are responsible for managing access to the memory regions they control. Since the Intel® Xeon® processor 5500 series contains an integrated memory controller, the home agents and caching agents reside within the processor sockets. The Intel® QuickPath Interconnect link blocks include the Intel® QuickPath Interconnect Physical through Protocol layers, which are implemented in hardware. No special software or drivers are required, other than firmware to initialize the Intel® QuickPath Interconnect links and load routing information.

Each the Intel® Xeon® processor 5500 series is connected to the other processor and the Intel® I/O Hub (IOH) chipset through dedicated Intel® QuickPath Interconnect links. Each Intel® QuickPath Interconnect link is a serial point-to-point connection, with 20 lanes per link under full width operation. These links are the only mode of data exchange between the processors and Intel® IOH chipset. There are no sideband signals. The Intel® QuickPath Interconnect communication fabric is glueless and does not require special hardware to interface to the processors to maintain cache coherency.

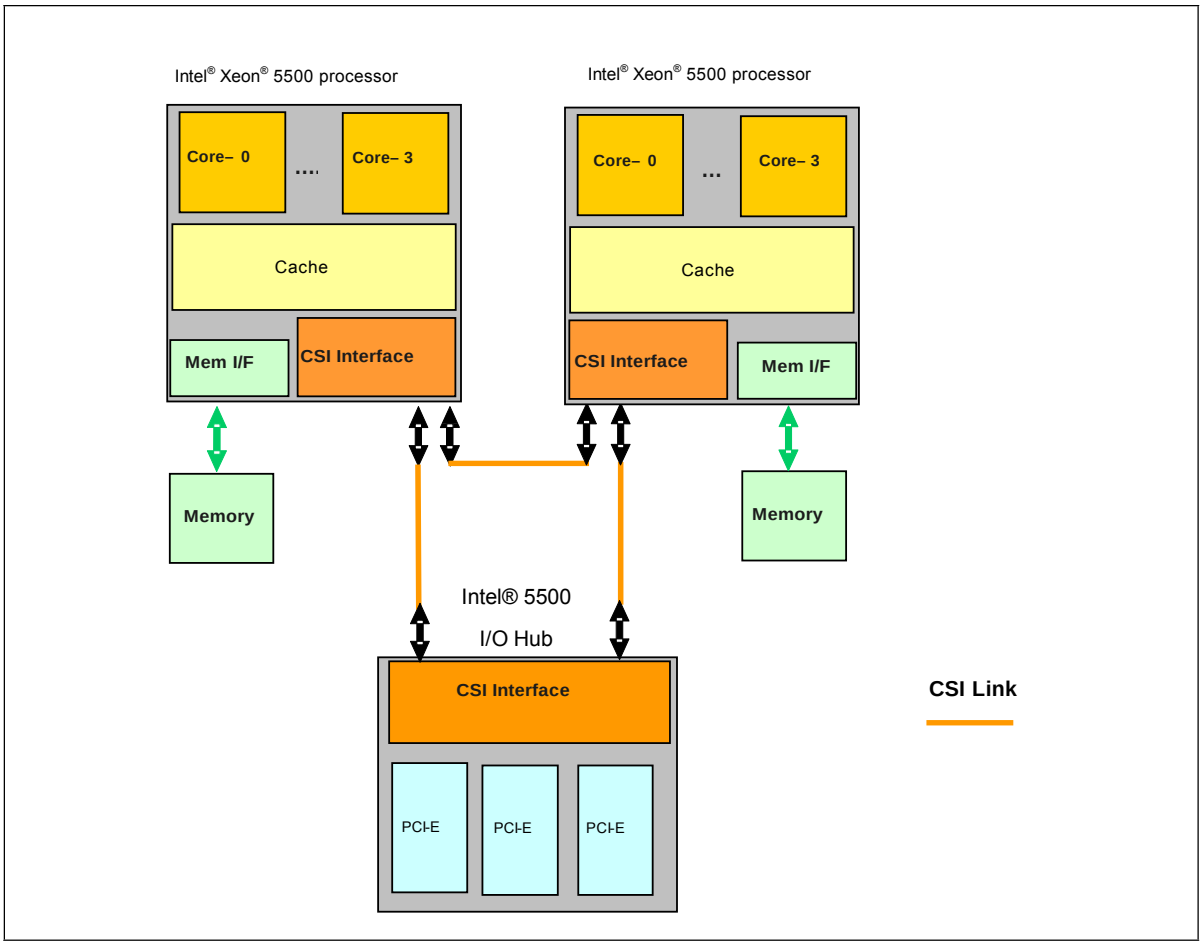


Figure 13. Intel® IOH 5500 Chipset with Intel® QuickPath Interconnect Block Diagram

3.1.2 Processor Population Rules

When using a single processor configuration, you must install the processor into the processor socket labeled CPU_1. A terminator is not required in the second processor socket when a single processor is used.

When two processors are installed, the following population rules apply:

- Both processors must be from the same processor family.
- Both processors must have the same Intel® QuickPath Interconnect speed.
- Both processors must have the same cache size.
- Processors with different speeds can be mixed in a system, given the prior rules are met. If this condition is detected, all processor speeds are set to the lowest common denominator (highest common speed) and an error is reported.
- Processor stepping within a common processor family can be mixed as long as it is listed in the processor specification updates published by Intel Corporation.

The following table describes mixed processor conditions and recommended actions for all Intel® server boards and systems that use the Intel® IOH chipset. Errors fall into one of two categories:

- Fatal: If the system can boot, it goes directly to the error manager, regardless of the "Post Error Pause" set-up option.
- Major: If the "Post Error Pause" set-up option is enabled, the system goes directly to the error manager; otherwise, the system continues to boot and no prompt is given for the error. The error is logged to the error manager.

Table 5. Mixed Processor Configurations

Error	Severity	System Action
Processor family not Identical	Fatal	The BIOS detects the error condition and responds as follows: • Logs the error into the system event log (SEL). • Alerts the BMC of the configuration error with an IPMI command. • Does not disable the processor. • Displays "0194: Processor family mismatch detected" message in the error manager. • Halts the system.
Processor cache not identical	Fatal	The BIOS detects the error condition and responds as follows: • Logs the error into the SEL. • Alerts the BMC of the configuration error with an IPMI command. • Does not disable the processor. • Displays "0192: Cache size mismatch detected" message in the error manager. • Halts the system.

Error	Severity	System Action
Processor frequency (speed) not identical	Major	The BIOS detects the error condition and responds as follows: • Adjusts all processor frequencies to lowest common denominator. • Continues to boot the system successfully. If the frequencies for all processors cannot all be adjusted to be the same, then the BIOS: • Logs the error into the SEL. • Displays “0197: Processor speeds mismatched” message in the error manager. • Halts the system.
Processor microcode missing	Fatal	The BIOS detects the error condition and responds as follows: • Logs the error into the SEL. • Alerts the BMC of the configuration error with an IPMI command. • Does not disable the processor. • Displays “816x: Processor 0x unable to apply microcode update” message in the error manager. • Pauses the system for user intervention.
Processor Intel® QuickPath Interconnect speeds not identical	Fatal	The BIOS detects the error condition and responds as follows: • Logs the error into the system event log (SEL). • Alerts the BMC of the configuration error with an IPMI command. • Does not disable processor. • Displays “0195: Processor Front Side Bus speed mismatch detected” message in the error manager. • Halts the system.

3.1.3 Multiple Processor Initialization

Intel® IA-32 processors have a microcode-based bootstrap processor (BSP) arbitration protocol. The BSP starts executing from the reset vector (F000:FFF0h). A processor that does not perform the role of BSP is referred to as an application processor (AP).

The Intel® Server Board S5500BC is a dual-socket server platform based on Intel® QuickPath Interconnect replacing Front Side Bus architecture. At reset, one BSP per processor socket is selected. However, the BIOS POST Power On Self Test (POST) code requires only one processor for execution. This requires the BIOS to elect a single system BSP using registers in

the chipset. The BIOS cannot guarantee which processor will be the system BSP, only that a system BSP is selected. In the remainder of this document, system BSP is referred to as BSP.

The BSP is responsible for executing the BIOS POST and preparing the server to boot the operating system. At boot time, the server is in virtual wire mode and the BSP alone is programmed to accept local interrupts (INTR driven by programmable interrupt controller (PIC) and non-maskable interrupt (NMI)).

As a part of the boot process, the BSP wakes each AP. When awakened, an AP programs its memory type range registers (MTRRs) to be identical to those of the BSP. All APs execute a halt instruction with their local interrupts disabled. If the BSP determines that an AP exists that is a lower-featured processor or that has a lower value returned by the CPUID function, the BSP switches to the lowest-featured processor in the server. The system management mode (SMM) handler expects all processors to respond to an SMI.

3.1.4 Turbo Mode

The Turbo Mode feature opportunistically and automatically allows the CPU to run faster than the TDP frequency if the processor is operating below specifications. Processor must be below the power, temperature, and current specification limits. Turbo Mode increases performance of both multi-threaded and single-threaded workloads. Turbo Mode operates under operating system control - only entered when the operating system requests higher performance, such as a transition from a P1 state to a P0 state. Ability to enter Turbo Mode is independent of the number of active cores. Achievable processor turbo frequency is limited by the most constraining of processor temperature, power, core Icc, and core ratio limits. Maximum Turbo Mode frequency is dependent on the number of active cores. Each processor has a fixed number of —turbo bins that may have up to 3 bins above marked —max freq bin. When fewer cores are active, more turbo bins are available. Example: 1 Core 3 Turbo bins, 2 Cores 2 Turbo bins, 4 Cores 1 Turbo bin. If the processor supports this feature (it is not available in all SKUs), the BIOS setup provides an option to enable or disable this feature. The default is disabled.

3.1.5 Simultaneous Multi-Threading

The Intel® Xeon® processors 5500 series supports Simultaneous Multi-Threading (SMT). The BIOS detects processors that support this feature and enables SMT during POST.

If the processor supports this feature, the BIOS setup provides an option to enable or disable this feature. The default is enabled.

The BIOS creates additional entries in the ACPI MP tables to describe the virtual processors. The SMBIOS Type 4 structure shows only the physical processors installed. It does not describe the virtual processors.

3.1.6 Enhanced Intel® SpeedStep® Technology

Enhanced Intel® SpeedStep® Technology helps reduce average system power consumption and potentially improves system acoustics by allowing the system to dynamically adjust processor voltage and core frequency

3.1.7 Multi-Core Processor Support

The BIOS does the following:

- Initializes all processor cores.
- Installs all NMI handlers for all Intel® Xeon® processor 5500 series.
- Leaves initialized AP in CLI/HLT loop.
- Initializes stack for all APs.

BIOS Setup provides an option to selectively enable or disable multi-core processor support. The default behavior is enabled.

3.1.8 Independent Loading Mechanism (ILM) Back Plate Design Support

The Intel® Server board S5500BC complies with Intel's Independent Loading Mechanism (ILM) processor mounting and Unified Retention System (URS) heat sink retention solution. The ILM design allows a bottoms-up assembly of the components to the board. The unified back plate for dual processor server products consists of a flat steel back plate with threaded studs for ILM attachment, and internally threaded nuts for attaching the heat sink. The threaded studs have a knurled feature that attaches the back plate to the motherboard when assembled.

The following diagram illustrates the URS and the Unified Backplate Assembly. The URS is designed to extend air-cooling capability through the use of larger heat sinks with minimal airflow blockage and bypass. URS retention transfers load to the baseboard via the Unified Backplate Assembly. The URS spring, captive in the heat sink, provides the necessary compressive load for the thermal interface material.

***Note**: The processor heat sink and ILM backplate shown in the following diagram is for reference purposes only. The actual processor heat sink and ILM backplate solutions compatible with this generation of server boards may have a different design.*

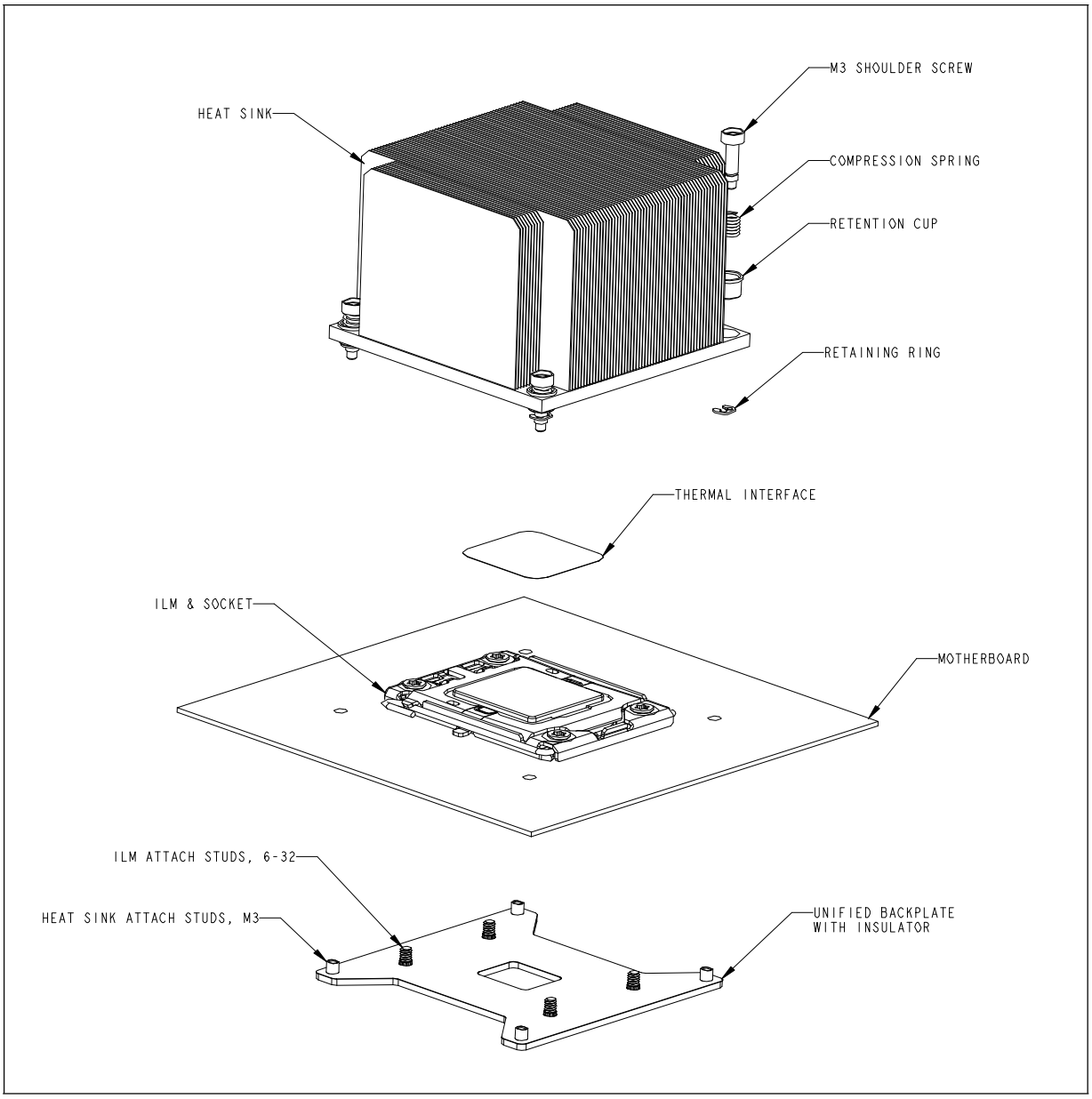


Figure 14. ILM backplate and URS

3.2 Memory Sub-system

3.2.1 Integrated Memory Controller

The Intel® Xeon® processors 5500 series has an Integrated Memory Controller (IMC). The Intel® Server Board S5500BC memory interface supports up to three DDR3 channels. Each channel consists of 64 data and 8 ECC bits. The IMC provides DDR3 channels and groups DIMMs on

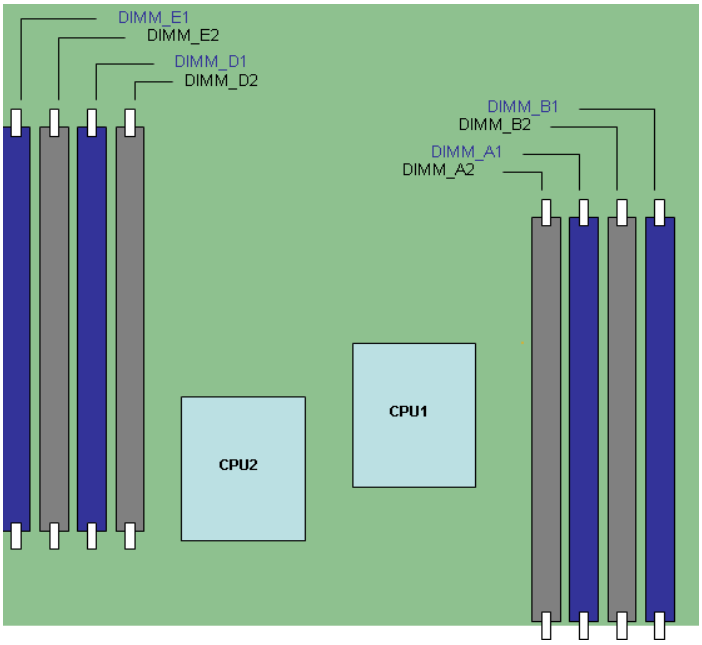
the board into an autonomous RAS memory. The server board is designed to support a DDR3-based memory subsystem with eight DIMM slots.

- 1 GB and 2 GB DRAM technology/density support.
- DDR3 800/1066/1333 MT/s support with up to 16 GB capacity.
- Single-rank and dual-rank support.

The BIOS can configure the memory controller dynamically in accordance with the available DDR3 DIMM population and the selected RAS (reliability, availability, and serviceability) mode of operation.

3.2.2 DIMM Population Requirements

DIMMs on this board are organized into physical slots on the DDR3 memory channels divided between two processor sockets. For more information, refer to the following figure.



Processor Socket 1				Processor Socket 2			
Channel A		Channel B		Channel D		Channel E	
A1	A2	B1	B2	D1	D2	E1	E2

Figure 15. DIMM Organization

- DIMMs are organized into physical slots on DDR3 memory channels that belong to the processor sockets.
- The memory channels for processor socket 1 are identified as channels A and B. The memory channels for processor socket 2 are identified as channels D and E.
- Each node supports four DIMM sockets (two DIMM sockets per channel).

- The DIMM identifiers on the silkscreen on the board provide information about which channel and therefore which node they belong to. For example, DIMM_A1 is the first slot on channel A of node 1. DIMM_D1 is the first DIMM socket on channel D of node 2.
- The memory slots for each DDR3 channel from the Intel® Xeon® 5500 processor series must be populated on a farthest first fashion. This also holds true for Independent Channel mode. Therefore, DIMM_A2 cannot be populated/used if DIMM_A1 is empty.
- When CPU socket 1 is empty, any DIMM memory in channel A and B is unavailable.
- When CPU socket 2 is empty, any DIMM memory in channel D and E is unavailable.
- If channel A and channel B are empty, CPU socket 1 can still function if memory is available from channel D and channel E. However, platform performance will suffer latency due to remote memory.
- Sockets are self-contained and autonomous. However, all RAS Error Management configurations in the BIOS setup will be applied commonly across sockets.

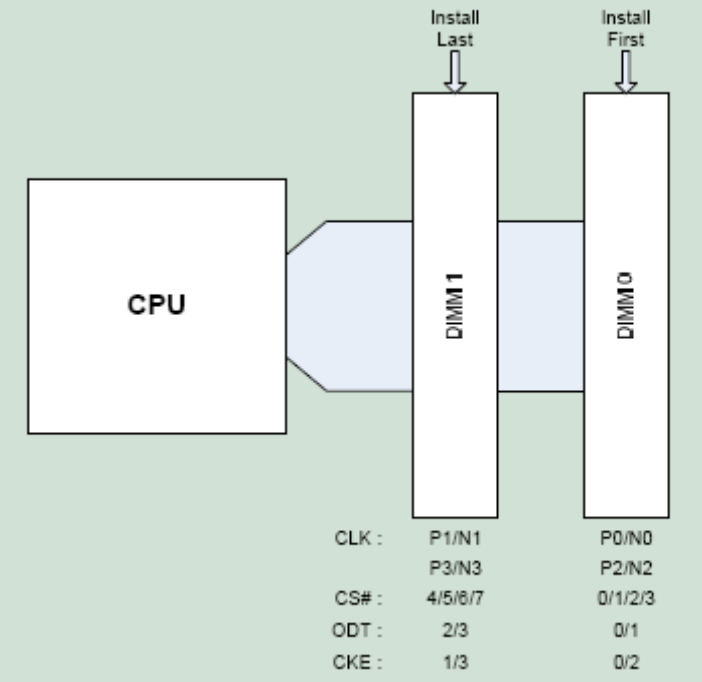


Figure 16. Channel slots Configuration

The DIMM population configurations (UDIMMs or RDIMMs) for two slots per channel are reviewed in the following table.

Table 6. DIMM Population configurations

S#	Speed	DIMM1	DIMM0
1	DDR3-800/1066/1333	Empty	Single rank
2	DDR3-800/1066/1333	Empty	Dual rank
3	DDR3-800/1066/1333	Single rank	Single rank
4	DDR3-800/1066/1333	Single rank	Dual rank
5	DDR3-800/1066/1333	Dual rank	Single rank
6	DDR3-800/1066/1333	Dual rank	Dual rank

3.2.3 Memory Upgrade Guidelines

Upgrading the system memory requires careful positioning of the DDR3 DIMMs based on the following factors:

- The current RAS mode of operation.
- The existing DDR3 DIMM population.
- The DDR3 DIMM characteristics.
- The optimization techniques used by the Intel® Xeon® processor 5500 series to maximize memory bandwidth.

In Independent Channel Mode all DDR3 channels operate independently. Slot-to-slot DIMM matching is not required across channels. For example, DIMM_A1 and DIMM_B1 do not have to match in terms of size, organization, and timing. DIMMs in a channel can be a different size and organization, but they will operate at the maximum common frequency. You can use Independent Channel Mode to support a single DIMM configuration in channel A and Single Channel Mode.

You should observe the following general rules when selecting and configuring memory to obtain the best performance from the system.

- The Independent Channel Mode is the default maximum performance mode preferred for Intel® Xeon® processor 5500 series based platforms.
- Socket1 usually has precedence over socket 2 in determining the possible RAS modes.
- The sockets are autonomous and capable of being independently initialized. However, the minimal upgrade for socket 2 is DIMM_D1 in Independent Channel Mode.
- Minimal upgrade for Channel Mirror mode is {D1, E1}. If this mode fails, then the Independent channel mode is used across the sockets.
- If an installed DDR3 DIMM has faulty or incompatible SPD data, it is ignored during the memory initialization and therefore essentially disabled by the BIOS. If the DDR3 DIMM has no or missing SPD information, the BIOS ignores the DIMM and the slot is marked as empty.
- The DDR3 DIMM populated in slot DIMM_B1 of socket1 determines the RAS mode of the system. If the DIMM_A1 and DIMM_B1 are not identical, then the system falls back to Independent Channel Mode.

- The minimal memory population possible is DIMM_A1. In this configuration, the system operates in Independent Channel Mode. No RAS is possible.
- The minimal memory population for Channel Mirroring Mode is {A1, B1}.
- Memory population on channel A and channel B of socket 1 should be identical to enable Channel Mirroring Mode. channel D and channel E of socket 2 should also be identical.
- If the DDR3 DIMMs on adjacent channels of a socket are not identical in mirroring, the DIMMs on the higher slots are disabled.
- DIMM parameters and matching requirements for memory RAS are specific to each socket.
- When one socket fails the DIMM matching on the adjacent channels for the RAS configuration selected in Setup, the BIOS configures all DDR3 Channels to Independent mode.
- DDR3 DIMMs on the same channel but adjacent slots do not need to be identical.

3.2.4 Support for Mixed-speed Memory Modules

The BIOS supports memory modules of mixed speed by automatically selecting the highest common frequency of all DDR3 DIMMs.

3.2.5 CPU Cores, QPI Links and DDR3 Channels Frequency Configuration

The Intel® Xeon® processor 5500 series connects to each other and to the Intel® IOH 5500 chipset through Intel® Quick Path Interconnect technology. The frequencies of the processor cores and the links to the Intel® Xeon® processor 5500 series are independent from each other. Unlike the front side bus (FSB) of earlier products, there are no gear-ratio requirements for the Intel® Xeon® processor 5500 series.

Intel® IOH 5500 chipset will support 4.8 GT/s, 5.86 GT/s, and 6.4 GT/s frequencies for the Intel® Quick Path Interconnect links on this server board. During Initialization, the BIOS will configure both end points of each link to the same speeds for correct operation.

During memory initialization, the BIOS keeps track of the latency requirements of each installed DDR3 DIMM by recording the requirements from each DIMMs SPD data. The BIOS then reviews the requirements of all components and configures the memory system and DDR3 DIMMs for a common frequency.

3.2.6 Memory RAS Features

The Intel® server boards S5500BC supports the following memory RAS features:

- Channel Independent Mode
- Channel Mirroring Mode
- Demand and Patrol Scrub
- Lockstep Channel Mode

The Intel® Xeon® processor 5500 series offer memory RAS at the channel level. Mirroring occurs at the channel level. Channel B mirrors channel A. All DIMM matching requirements are on a slot-to-slot basis on adjacent channels. To enable Mirroring, the corresponding slots on channel A and channel B must have DIMMs with identical parameters. DIMMs on adjacent slots on the same channel are not required to have identical parameters.

When installing memory, you must populate first the memory slot that is the farthest away in the channel for each processor (See “Channel Slots Configuration” figure), even for Independent Channel mode. Therefore, you cannot populate/use DIMM_A2 if DIMM_A1 is empty.

The Intel® Xeon® processor 5500 series on socket 1 and socket 2 in a dual processor configuration is completely autonomous. DIMMs routed to sockets are isolated and can be initialized locally, including RAS configurations. The Intel® Server Board S5500BC provides one set of RAS questions in the BIOS Setup and can configure common RAS features across the sockets. If one socket fails the RAS population requirements, the BIOS sets all channels to Independent Channel mode. The rules on channel population and channel matching vary by the RAS mode used. Note that support of RAS modes require matching DIMM population between channels (sparing, mirroring, and lockstep) require that ECC DIMMs be populated. Independent Mode is the only mode that supports non-ECC DIMMs in addition to ECC DIMMs.

3.2.7 Independent Channel Mode

You can populate channels in any order in Independent Channel Mode. You can populate both channels in any order and have no matching requirements. All channels must run at the same interface frequency, but individual channels may run at different DIMM timings (RAS latency, CAS latency, and so forth).

3.2.8 Channel Mirroring Mode

The Intel® Xeon® processor 5500 series supports channel mirroring to configure the available channels of DDR3 DIMMs in a mirrored configuration. Unlike channel sparing, the mirrored configuration is a redundant image of the memory and can continue to operate when sporadic uncorrectable errors occur.

3.2.9 Lockstep Channel Mode

In Lockstep Channel Mode, each memory access is a 128-bit data access that spans the first channel and the second channel. The same address is used on both channels such that an address error on any channel is detectable by bad ECC. Lockstep channel mode requires that you populate the first channel and the second channel identically. That is, each DIMM in one channel must have a corresponding DIMM of identical organization such as the number of ranks, banks, rows, and/or columns. DIMMs may be of different speed grades, but the Intel® QuickPath Memory Controller is configured to operate all DIMMs according to the slowest parameters present. DIMM slot populations within a channel do not have to be identical, but the same DIMM slot location across the first channel and the second channel must be populated the same. The third channel is unused in lockstep channel mode.

3.2.10 Demand and Patrol Scrub

The Intel® Integrated Memory Controller supports demand and patrol scrubbing. A scrub fixes a correctable error in memory. A 4-byte ECC is attached to each 32-byte "payload". An error is detected when the ECC calculated from the payload does not match the ECC read from memory. The error is corrected by modifying the ECC, payload, or both, and then writing both the ECC and payload back to memory. Only one demand or patrol scrub can be completed at a time. Patrol scrubs are intended to ensure that data with a correctable error does not remain in DRAM long enough to cause further corruption and an uncorrectable particle error. The Intel® QuickPath Memory Controller issues a Patrol Scrub at a rate sufficient to write every line once a day. The maximum is one scrub every 82 ms with 64 GB of memory.

3.3 Intel® I/O Hub (IOH) 5500 chipset

The Intel® I/O Hub (IOH) 5500 chipset component provides a connection point between various I/O components and Intel® QuickPath Interconnect based processors. The following table shows the features supported by the chipset.

Table 7. Intel® IOH 5500 Chipset Features

Chipset	Intel® QuickPath Interconnect Ports	Processor	PCI Express* Lanes	Manageability
Intel® IOH 5500 chipset	2	Intel® Xeon® processor 5500 series	24	Node Manager

The Intel® IOH 5500 chipset on the Intel® Server Board S5500BC has the following features:

- Two Intel® QuickPath Interconnect interfaces with full-width links (20 lanes in each direction).
- Two x16 PCI Express* Gen2 ports are also configurable as x8 and x4 links compliant to the PCI Express* Base Specification, Revision 2.0. Each port supports up to 8 GB/s/direction peak bandwidth.
- One x4 Enterprise South Bridge Interface (ESI) link interface.
- Support Controller Link interface between the IOH and ICH portions of the Manageability Engine subsystem.
- Manageability Integrated support: Manageability Engine (ME) and external memory controller for manageability firmware; ME network access; and System Defense Feature support enabled by firmware.
- Reduced Media Independent Interface (RMII) support.
- Supports an SMBus Specification Revision 2.0 slave interface for server management with Packet Error Checking.
- Power Management Support
- Intel® Virtualization Technology for Directed I/O (Intel® VT-d), Second Revision for server security.
- Integrated IOxAPIC

3.3.1 PCI Express* Gen 2

PCI Express* generation 1 and 2 are dual simplex, point-to-point serial differential low voltage interconnect. The signaling bit rate is 2.5 Gbit/sec/lane/direction for Generation 1 and 5.0 Gbit/sec/lane/direction for Generation 2.

The Intel® S5500 chipset on the Intel® Server Board S5500BC provides PCI Express* Gen2 interface. The key features are the following:

- Connected to three PCI Express* Gen2 x8 connectors (one with x4 link).
- Connected to 82574L GbE with a PCI Express Gen2 x1 link.
- Compliant with the PCI Express* 2.0 specification.

3.3.2 Enterprise South Bridge Interface (ESI) Features

The interface between the Intel® IOH 5500 chipset and Intel® ICH10R is called the Enterprise South Bridge Interface or simply ESI. ESI is electrically equivalent to the PCI Express* Generation 1 interface and the routing guidelines are similar.

3.3.3 Controller Link (M-Link)

The Controller Link is the interconnect that connects the north bridge (IOH) to the LAN Controller in the ICH. The Management Engine (ME) resides in the IOH and communicates with the ICH LAN Controller through this interface.

3.3.4 Management Engine (ME)

The Management Engine (ME) is an embedded ARC controller within the IOH. The IOH ME performs manageability functions called Intel® Server Platform Services (SPS) for the discrete Baseboard Management Controller (BMC).

Server Platform Services are value-added platform management options that enhance the value of Intel platforms and their component ingredients (CPUs, chipsets and I/O components). Each service is designed to function independently wherever possible, or grouped together with one or more features in flexible combinations to allow OEMs (Original Equipment Manufacturers) to differentiate platforms. The following is a high-level view of the Intel® Server Board S5500BC SPS functions.

- **Node Management Features:**
  - NPTM Policy Manager
  - Power Supply Monitoring Service
  - Inlet Temperature Monitoring Service (support for this feature on Intel servers is platform-specific)
  - CPU Power Limiting Service
- **Provide Access to ICH10 Devices:**

  The ME has control of ICH10 platform instrumentation. SPS provides a mechanism for the BMC to access this instrumentation through IPMI OEM commands. Use of this capability on Intel servers is platform-/SKU-specific.

- Fan monitoring and fan control
- ICH10 temperature monitoring

- **PECI 2.0 Proxy:**

  SPS offers a means for a BMC without a PECI 2.0 interface to use the ME as a PECI proxy. The BMC on Intel servers already has a PECI 2.0 interface, so this SPS capability is not used.

No external IOH memory is required to support the ME SPS functions.

3.3.4.1 ME Firmware Update

The ME FW provides a set of IPMI OEM commands for performing the firmware update. An update utility running on the host uses IPMI bridging functionality to send these commands to the ME through the BMC over the BMC/IPMB link.

On Intel server platforms, the ME FW uses a single operational image with a recovery image. In order to upgrade an operational image, a boot to recovery image must be performed. The recovery image only provides the basic functionality that is required to perform the update; therefore, other SPS features are not functional when the update is in progress.

3.3.4.2 Management Engine Interaction

ME-BMC interactions include the following:

- BMC stores sensor data records for ME-owned sensors.
- BMC participates in ME firmware update.
- BMC initializes ME-owned sensors based on SDRs.
- BMC receives platform event messages sent by the ME.
- BMC notifies ME of POST completion.
- BMC may be queried by the ME for inlet temperature readings.

BMC uses the ICH10R fan tachs through the ME.

3.3.5 Intel® Virtualization Technology for Directed I/O (Intel® VT-d) (rev. 2)

Intel® Virtualization Technology (Intel® VT) is the technology that makes a single system appear as multiple independent systems to software loaded on the system. This allows for multiple independent operating systems to be running simultaneously on a single system. The first revision of this technology (Intel® Virtualization Technology for Intel® IA-32 Architecture or Intel® VT-x) adds hardware support in the processor to improve the virtualization performance and robustness. The second revision of this specification (Intel® VT-d) adds a chipset hardware implementation to improve I/O performance and robustness.

You can enable the Intel® VT in the BIOS Setup. The default setting is disabled.

Note: *If the setup options are changed to enable or disable the Virtualization Technology setting in the processor, the user must perform an AC power cycle before the changes take effect.*

The Intel® IOH 5500 chipset on the Intel® Server Board S5500BC supports Intel® VT-d2 features as outlined:

- Builds on the first generation of Intel® VT-d features
- Improves performance through better invalidation architecture
- Supports end-point Address Translation Caching (ATC) compliant with the PCISIG IOV Address Translation Services (ATS), Revision 1.0 specification
- Provides interrupt remapping
- Optimizes translation of sequential accesses
- Supports IOV (ARI)

Note*: For more information on VT-d2, refer to: http://download.intel.com/technology/computing/vptech/Intel(r)_VT_for_Direct_IO.pdf.*

3.4 Intel® 82801Jx I/O Controller Hub (ICH10R)

The Intel® ICH10R I/O Controller Hub provides extensive I/O support. Functions and capabilities include:

- PCI Express* Base Specification, Revision 1.1 support
- PCI Local Bus Specification, Revision 2.3 for 33 MHz PCI operations (supports up to four REQ#/GNT# pairs)
- ACPI Power Management Logic Support, Revision 3.0a
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial ATA host controllers with independent DMA operation on up to six ports and AHCI support
- USB host interface supports up to 12 USB ports; six UHCI host controllers; and two EHCI high-speed USB 2.0 host controllers
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, Version 2.0, with additional support for I^2C devices
- Low Pin Count (LPC) interface support
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support

3.4.1 PCI and PCI Express* Interfaces

The Intel® ICH10R provides a 33MHz, 3.3 V PCI interface implementation. All PCI signals are 5 V tolerant except PME#. The Intel® Server Board S5500BC provides one slot for legacy PCI devices. This 5-V keyed slot can support Universal or legacy 5-V keyed PCI 32-bit / 33MHz add-in cards.

The Intel® ICH10R provides six PCI Express* Root Ports which are compliant with the PCI Express Base Specification, Revision 1.1. You can statically configure the PCI Express* root ports 1-4 as four x 1 ports, or group them together to form two x2 ports, one x2 with two x1 ports, or one x4 port. You can only use ports 5 and 6 as two x1 ports or one x2. Port 6 is multiplexed with a Gigabit LAN Connect Interface. The x4 configuration supports lane reversal. Each root port supports 2.5 Gb/s bandwidth in each direction.

Ports 1-4 on the Intel® Server Board S5500BC are grouped together to form a single x4 link connecting to an x4 PCI Express* Slot. Port 5 connects to the Integrated BMC for 2D video function. Port 6 is used as Gigabit LAN Connect Interface and connected to the Ethernet device PHY.

3.4.2 Serial ATA II Interface

The ICH10R has an integrated Serial ATA (SATA) controller that supports independent DMA operation on six ports and data transfer rates of up to 3.0 Gb/s. The six SATA ports on the server board are numbered SATA-0 through SATA-5. You can enable or disable the SATA ports and/or configure them by accessing the BIOS setup utility during POST.

The BIOS Setup utility provides multiple drive configuration options on the Advanced | Mass Storage Controller Configuration setup page, some of which affect the ability to configure RAID. The “Onboard SATA Controller” option is enabled by default. When this option is enabled, you can set the “SATA Mode” option to ENHANCED mode, COMPATIBILITY mode, AHCI mode, or SW RAID mode. The modes affect the configuration as follows:

- **ENHANCED mode** supports up to 6 SATA ports with IDE Native Mode.

- **COMPATIBILITY mode** supports up to 4 SATA ports [0/1/2/3] with IDE Legacy mode and 2 SATA ports[4/5] with IDE Native Mode.

- **AHCI mode** supports all SATA ports using the Advanced Host Controller Interface when the option is enabled. Note: For AHCI capability in EFI, you should set the AHCI legacy Option ROM to “disabled”.

- **SW RAID mode** supports configuration of SATA ports for RAID via RAID configuration software.

For RAID 0, 1, and 10, enclosure management is provided through the SATA_SGPIO connector on the server board when a cable is attached between this connector on the server board and to the backplane or I^2C interface.

3.4.3 Software RAID Support

The Intel® Server Board provides six SATA ports (3 Gb/ps) using ICH10R with Intel® Embedded Server RAID Technology, with SW RAID levels 0/1/10; with optional support for SW RAID 5 with activation key.

If RAID 5 is needed, you can install the optional Intel® RAID Activation Key AXXRAKSW5. To enable RAID 5, this activation key is placed on the SATA Key connector located on the right side of the server board. For information on how to install the Intel® RAID Activation Key

AXXRAKSW5 accessory to enable RAID 5, see the documentation included with the accessory kit.

3.4.4 Low Pin Count Interface (LPC)

The Intel® ICH10R implements an LPC Interface. The Low Pin Count (LPC) bridge function of the Intel® ICH10R resides in PCI Device 31: Function 0. In addition to the LPC bridge interface function, D31:F0 contains other functional units including DMA, interrupt controllers, timers, power management, system management, GPIO, and RTC.

The LPC bus supports the Integrated BMC, which contains Server Class Super I/O functionality in an integrated subsystem on the Intel® Server Board S5500BC.

3.4.5 Serial Bus (USB) Controller

The Intel® ICH10R contains up to two Enhance Host Controller Interface (EHCI) host controllers that support USB high-speed signaling. High-speed USB2.0 allows data transfers up to 480 Mb/s, which is 40 times faster than full-speed USB. The Intel® ICH10R also contains up to six Universal Host Controller Interface (UHCI) controllers that support USB full-speed and low-speed signaling.

The Intel® ICH10R supports up to 12 USB 2.0 ports. All 12 ports are high-speed, full-speed, and low-speed capable. Intel® ICH10R's port-routing logic determines whether a USB port is controller by one of the UHCI or EHCI controllers. Ten ports are used on the Intel® server board S5500BC as outlined:

- Four ports are connected to dual USB + RJ-45 stacked external connectors on the rear panel.
- Four ports are connected to internal headers.
- Two ports are connected to the Integrated BMC for remote storage and remote KB/MS function.

3.4.6 Serial Peripheral Interface (SPI)

The Intel® ICH10R implements an SPI Interface as an alternative interface for the BIOS flash device. You can use an SPI flash device as a replacement for the FWH, which is required to support Gigabit Ethernet. The Intel® ICH10R supports up to two SPI flash devices with speeds up to 33 MHz using two chip select pins.

3.4.7 General Purpose Input/Output (GPIO)

Various general purpose inputs and outputs are provided for custom system design. The number of inputs and outputs varies depending on Intel® ICH10R configuration.

3.4.8 Enhanced Power Management

The Intel® ICH10R supports the Advanced Configuration and Power Interface, Version 2.0 (ACPI) that provides power and thermal management. The Intel® ICH10R also supports the

Manageability Engine Power Management Support for new wake events from the IOH Management Engine.

The Intel® Server Board S5500BC server is fully compliant with the Advanced Configuration and Power Interface (ACPI) specifications, Revision 2.0.

3.4.9 System Management Interface

Intel® ICH10R on the Intel® Server board S5500BC functions as a SMBus Host Controller that allows the processor to communicate with SMBus slaves. This interface is compatible with most I^2C devices. Intel® ICH10R also supports slave functionality.

3.4.10 Real Time Clock (RTC)

Intel® ICH10R contains a Motorola MS146818A* functionally compatible Real Time Clock (RTC) with two 128-byte banks of battery-backed RAM. The RTC performs two key functions on the Intel® Server Board S5500BC:

- Keeps track of the time of day
- Stores System configuration data even when the system is powered down.

The RTC operates on a 32.768 KHz crystal and a 3-V lithium battery.

3.4.11 Manageability

Intel® ICH10R integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

The management engine includes:

- TCO Timer: Detects system locks
- Process Present Indicator: Determines the processor fetches the first instruction after reset.
- ECC Error Reporting: Reports ECC errors from the host controller.
- Function Disable: Prevents a disabled function from generating interrupts and power management events.
- Intruder Detect Input: Determines system cases.

3.4.12 Unsupported Intel® ICH10R Interfaces

The Intel® Server Board S5500BC does not support the following interfaces on the Intel® ICH10R:

- An Audio Codec (AC) ’97 Component Specification, Version 2.3 controller that can be used to attach an AC, Modem Codec (MC), Audio/Modem Codec (AMC), or a combination of ACs and a single MC.
- Intel® High Definition Audio
- SST, Fan tach and PWM, and PEC controller

3.5 Network Interface Controller (NIC)

The Intel® 82574L GbE PCI-E Network Controller is a single, compact component with integrated Gigabit Ethernet Media Access Controller (MAC) and Physical Layer (PHY) function. This device is connected to the Intel® ICH10R. The Intel® Server Board S5500BC uses this device along with the integrated Intel® ICH10R MAC and external Intel® 82567 Gigabit Network connector to provide two Gigabit Ethernet Ports designed for 10/100/1000 Mbps operation.

The Intel® 82574L GbE PCI-E Network Controller correlates to the NIC2 connector on the back edge of the board; the external Intel® 82567 Gigabit Network correlates to the NIC1 connector on the back edge of the board. When looking at the I/O panel, the NIC 1 should be wired to the left-most RJ-45 connector. The Intel® 82574L GbE Ethernet Controller and the external Intel® 82567 Gigabit Network connector drive two LEDs located on each network interface connector. The normal RJ45 link/activity LED at the right of the connector indicates network connection when on and Transmit/Receive activity when blinking. These LEDs are be powered from a Standby voltage rail. The speed LED at the left indicates 1000 Mbps operation when amber; 100 Mbps operation when green; and 10 Mbps when off.

Table 8. NIC Status LED

Led Name	Voltage resources	Color	Status	Description
LAN#1-Link/Act	3V3Aux	Amber	On	Link
		Amber	Blink	LAN Access (off when there is traffic)
		Off		Disconnect
LAN#1-Speed	3V3Aux	Green	On	Green, link speed is 100 Mbits/sec
		Amber	On	Amber, link speed is 1000 Mbits/sec
		Off		OFF, link speed is 10 Mbits/sec
LAN#2-Link/Act	3V3Aux	Amber	On	Link
		Amber	Blink	LAN Access (off when there is traffic)
		Off		Disconnect
LAN#2 Speed	3V3Aux	Green	On	Green, link speed is 100 Mbits/sec
		Amber	On	Amber, link speed is 1000 Mbits/sec
		Off		Off, link speed is 10 Mbits/sec

3.5.1 Intel® 82574L GbE PCI-E Network Controller

The Intel® 82574L GbE PCI-E Network controller is a single, compact, low-power component that offers a fully-integrated PCI-Express* x1 10/100/1000 GbE controller with Media Access Control (MAC) and Physical Layer (PHY) port. The device is compliant with PCI Express* Base Specification, Revision 2.0. The 82574L GbE PCI-E Network controller enables a single-port implementation in a relatively small area, so it can be used for server and client configurations as a LAN-on-Motherboard (LOM) design. You can also use the 82574L GbE PCI-E Network controller in embedded applications such as switch add-on cards and network appliances. The 82574L GbE PCI-E Network controller provides one PCI Express* lane operating at 2.5 GHz with sufficient bandwidth to support a 100 Mb/s transfer rate. 32 KB of on-chip buffering mitigates instantaneous receive bandwidth demands and eliminates transmit under-runs by buffering the entire outgoing packet prior to transmission. The Intel® 82574L GbE PCI-E Network controller supports the following features:

- Standard IEEE 802.3 Ethernet interface for 10BASE-T, 100BASE-TX, and 1000BASE-T (802.3, 802.3u, and 802.3ab) applications
- NC-SI or SMBus connection to a Manageability Controller (MC)
- IEEE 1149.1 JTAG
- Support for PCI 3.0 Vital Product Data (VPD)
- IPMI MC pass-through; multi-drop NC-SI
- TimeSync offload compliant with 802.1AS specification

3.5.2 Intel® 82567 Gigabit Network Connection Physical Layer Transceiver (PHY)

The Intel® 82567 Gigabit Network Transceiver is a single-port Gigabit Network Layer Transceiver (PHY) that connects to the Media Access Controller (MAC) through a dedicated interconnect. The 82567 Gigabit Network Transceiver is based on Intel's Gigabit Network PHY technology, and supports operation at data rates of 10/100/1000 Mb/s. The Intel® 82567 Gigabit Network Transceiver works with ICH9/ICH10 that incorporates and integrates the MAC, which is referred to as the ICH10 LAN. The Intel® 82567 Gigabit Network Transceiver interfaces with the MAC through two interfaces:

- Gigabit LAN Connect Interface (GLCI): A high-speed serial interface based on 802.3 serializer deserializer
- LAND Connect Interface (LCI): A low-speed proprietary parallel bus.

The 82567 Gigabit Network Transceiver operates using both interfaces—the GLCI for 1000Mb/s traffic and the LC for all other traffic types.

3.5.3 MAC Address Definition

Each Intel® Server Board S5500BC has the following four MAC addresses assigned to it at the Intel factory.

- NIC 1 MAC address
- NIC 2 MAC address – Assign the NIC 1 MAC address +1

- BMC LAN Channel MAC address – Assign the NIC 1 MAC address +2
- Intel® Remote Management Module 3 (Intel® RMM3) MAC address – Assign the NIC 1 MAC address +3

During the manufacturing process, each server board will have a white MAC address sticker placed on the top of the NIC 1 port. The sticker displays the NIC 1 MAC address in both bar code and alphanumeric formats, and displays the Intel® RMM3 MAC address in alphanumeric format. The NIC2 will work as a management port on the board.

3.6 Integrated Baseboard Management Controller

The ServerEngines* LLC Pilot II Integrated BMC is provided by an embedded ARM9 controller and associated peripheral functionality that is required for IPMI-based server management. Firmware usage of these hardware features is platform-dependant. The Integrated BMC on the Intel® Server Board S5500BC contains the following integrated functionality:

Server Class Super I/O functionality includes:

- Keyboard Style/BT interface for BMC support
- One Fully Functional Serial Ports, compatible with the 16C550
- Serial IRQ Support
- SMI/SCI/PME Support
- ACPI Compliant
- Up to 16 Shared GPIO ports
- Programmable Wake-up Event Support
- Plug and Play Register Set
- Power Supply Control
- Watchdog timer compliant with Microsoft SHDG*
- LPC to SPI bridge for system BIOS support
- Real Time Clock (RTC) module with the external RTC interface

Baseboard Management Controller

- IPMI 2.0 Compliant
- Integrated 250 MHz, 32-bit ARM9 processor
- Six I2C SMBus Modules with Master-Slave support
- Two independent 10/100 Ethernet Controllers with RMII support
- LPC Master interface for non-volatile code storage
- SPI Flash interface
- Three UART for ICMB support
- DDR2 16-bit up to 667 MHz memory interface
- 16 Mailbox Registers for communication between the host and the BMC
- Watchdog timer
- Three General Purpose Timers

- Dedicated Real Time Clock (RTC) for BMC
- Up to 16 direct and 64 Serial GPIO ports
- Ability to maintain text and graphics controller history
- 12 10-bit Analog to Digital Converters
- Three Diode Inputs for Temperature measurements
- Eight Fan Tach Inputs
- Four Pulse Width Modulators (PWM)
- Chassis Intrusion Logic with battery-backed general purpose register
- LED support with programmable blink rate control
- Programmable IO Port snooping, which can be used to snoop on Port 80h
- Unique Chip ID for each part (burned at the time production testing)
- Hardware 32-bit Random Number generator
- JTAG Master interface
- On-Chip Test Infrastructure for testing BMC firmware

Remote KVMS Features

- USB 2.0 interface for Keyboard, Mouse, and Remote storage, such as a CD/DVD-ROM and floppy
- USB 1.1 interface for PS/2 to USB bridging and remote Keyboard and Mouse
- Hardware-based Video Compression and Redirection Logic
- Supports both text and graphics redirection
- Hardware-assisted video redirection using the Frame Processing Engine
- Direct interface to the Integrated Graphics Controller registers and Frame buffer
- Hardware-based encryption engine

Graphics Controller Subsystem

- Integrated Matrix Graphics Core
- 2D Hardware Graphics Acceleration
- DDR2 memory interface supports up to 128 MB of memory
- Supports all display resolutions up to 1600 x 1200 16bpp @ 75Hz
- High-speed Integrated 24-bit RAMDAC
- Single lane PCI-Express* host interface

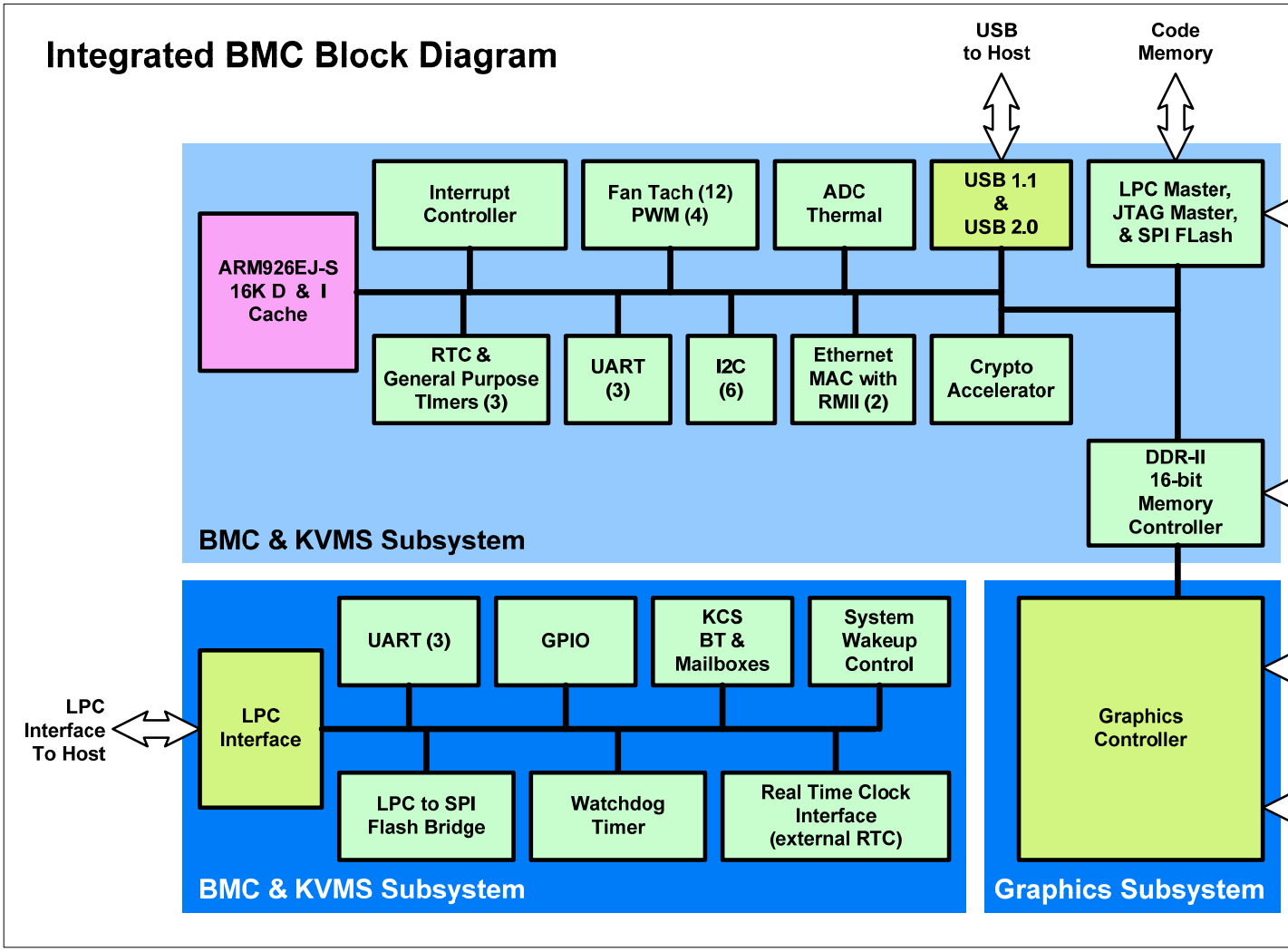


Figure 17. Integrated BMC Block Diagram

3.6.1 Integrated BMC Embedded LAN Channel

The Integrated BMC hardware includes two dedicated 10/100 network interfaces.

- Interface 1: This interface is available from either of available NIC ports in system which can be shared with the host. Only one NIC may be enabled for management traffic at any time. The active interface is NIC2 on this board.
- Interface 2: This interface is available from RMM3 which is dedicated management NIC and not shared with host.

For these channels, you can enable support for IPMI-over-LAN and DHCP. For security reasons, embedded LAN channels have the following default settings:

- IP Address: Static.
- All users disabled.

For more information about BMC IP address configuration, refer to the *Intel® S5500 Chipset Server Board Baseboard Management Controller Core External Product Specification*.

3.7 Video Support

The Intel® server board S5500BC includes a video controller in the on-board ServerEngines* LLC Pilot II BMC and 64 MB of video DDR2 SDRAM. The SVGA sub-system supports a variety of modes—up to 1600 x 1200 resolution in 8/16/32 bpp under 2D. It also supports both CRT and LCD monitors up to a 100-Hz vertical refresh rate. Video is accessed using a standard 15-pin VGA connector on the back edge of the server board.

3.7.1 Video modes

The integrated video controller supports all standard IBM VGA modes. The following table shows the 2D modes supported for both CRT and LCD.

Table 9. Video Modes

2D Mode	Refresh Rate (Hz)	2D Video Mode Support		
		8 bpp	16 bpp	32 bpp
640x480	60, 72, 75, 85, 90, 100, 120, 160, 200	Supported	Supported	Supported
800x600	60, 70, 72, 75, 85, 90, 100, 120,160	Supported	Supported	Supported
1024x768	60, 70, 72, 75,85,90,100	Supported	Supported	Supported
1152x864	43,47,60,70,75,80,85	Supported	Supported	Supported
1280x1024	60,70,74,75	Supported	Supported	Supported
1600x1200	52	Supported	Supported	Supported

3.8 Serial Ports

The Intel® Server Board S5500BC provides an external serial port and an internal serial header. The primary serial port, serial port A is connected from the Integrated BMC to a rear panel, industry-standard DB-9 male connector for pedestal products and RJ-45 for rack products. The secondary serial port, serial port B, is connected from the Integrated BMC to an on-board, internal 2x5 header.

3.9 Floppy Disk Controller

The Intel® Server Board S5500BC does not support a floppy disk controller (FDC) interface, but the system BIOS recognizes USB floppy devices.

3.10 Keyboard and Mouse Support

The server board does not support PS/2 interface keyboards and mice. However, the system BIOS recognizes USB specification-compliant keyboard and mice.

3.11 Wake-up Control

The BMC allows events to power-on and power-off the system. Wake from S1 is supported on LAN, USB, Serial port, and PCI Express* slots Wake from S4 are supported on LAN, Serial Port, Front panel Power button, and potentially RTC. To save power consumption during Standby, standby power is not being provided to the PCI Express* slots, so no Wake from S4 is supported on PCI Express* slots.

3.12 System Health Support

The BMC provides an interface from the GPIOs (General Purpose Input/Output) for BIOS and system management firmware to activate the diagnostic LEDs, FRU fault indicator LEDs for DIMMs, fans, and system status LED.

4. Platform Management

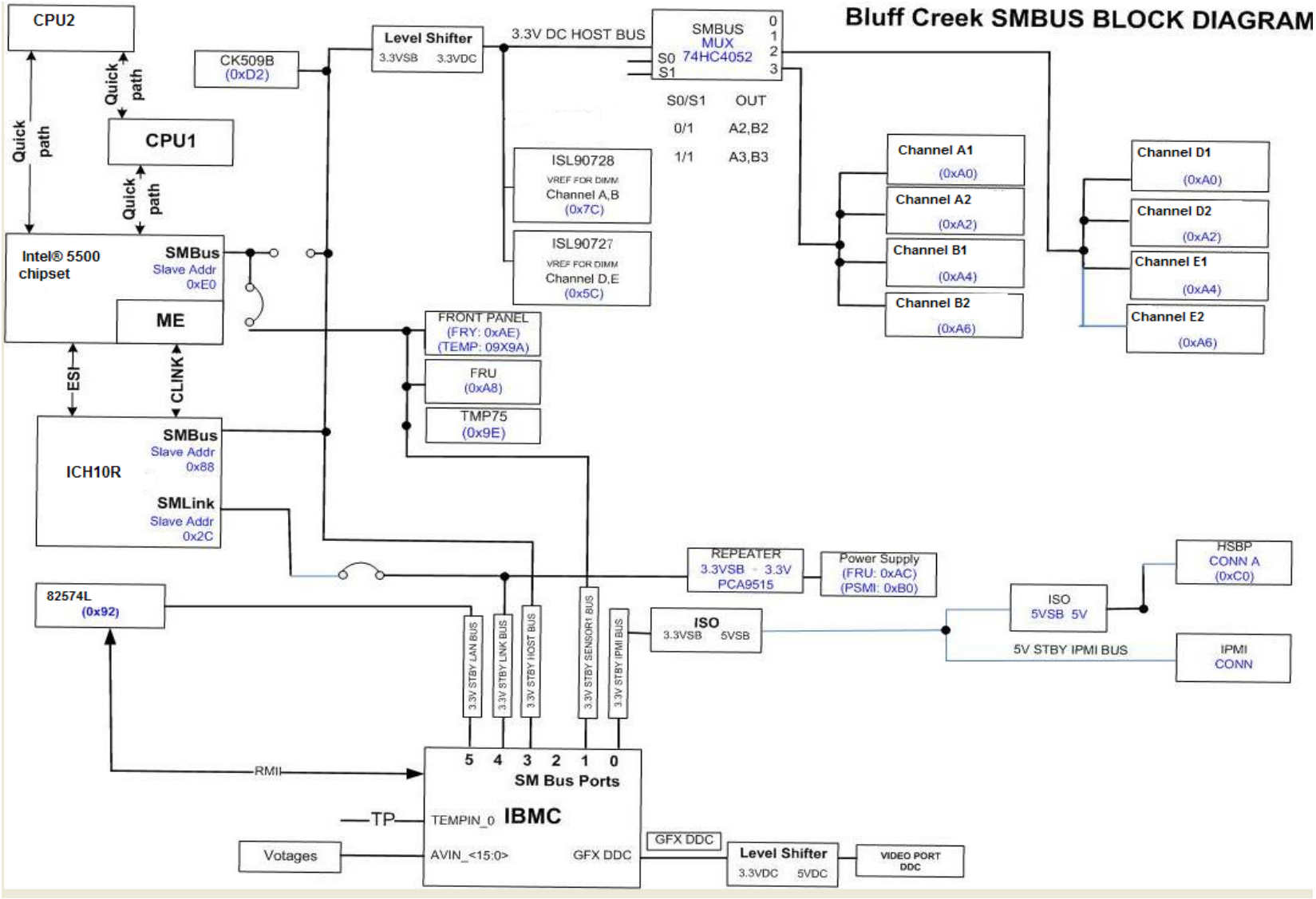
The Platform Management sub-system on the Intel® Server Board S5500BC consists of a Baseboard Management Controller (BMC), server management buses, sensors, server management firmware, and system BIOS. The BMC on the Intel® Server Board S5500BC is provided by ServerEngines* Pilot II integrated Baseboard Management Controller (Integrated BMC). The platform management sub-system is responsible for error management and reporting, system power control, thermal monitoring, and management including system fan control. The BMC provides system interface and monitoring features based on the IPMI 2.0 specification.

This section provides a high level overview of the server management architecture. For more information, refer to the following documents:

- *Intel® S5500 Chipset Server Board BIOS External Product Specification*
- *Intel® S5500 Chipset Server Board Baseboard Management Controller Core External Product Specification*
- *Intel® Remote Management Module 3 Technical Product Specification*
- *Intelligent Platform Management Interface (IPMI) 2.0 Specification*

The following diagram provides an overview of the Server Management Bus (SMBUS) architecture used on this server board.

Figure 18. SMBUS Block Diagram



4.1 Feature Support

4.1.1 IPMI 2.0 Features

- Baseboard management controller (BMC).
- IPMI Watchdog timer.
- Messaging support, including command bridging and user/session support.
- Chassis device functionality, including power/reset control and BIOS boot flags support.
- Event receiver device: The BMC receives and processes events from other platform subsystems.
- Field replaceable unit (FRU) inventory device functionality: The BMC supports access to system FRU devices using IPMI FRU commands.
- System event log (SEL) device functionality: The BMC supports and provides access to a SEL.
- Sensor device record (SDR) repository device functionality: The BMC supports storage and access of system SDRs.
- Sensor device and sensor scanning/monitoring: The BMC provides IPMI management of sensors. It polls sensors to monitor and report system health.
- IPMI interfaces.
- Host interfaces include system management software (SMS) with receive message queue support, and server management mode (SMM).
- Terminal mode serial interface.
- IPMB interface.
- LAN interface that supports the IPMI-over-LAN protocol (RMCP, RMCP+).
- Serial-over-LAN (SOL).
- ACPI state synchronization: The BMC tracks ACPI state changes that are provided by the BIOS.
- BMC self test: The BMC performs initialization and run-time self-tests, and makes results available to external entities.

4.1.2 Non-IPMI Features

The BMC supports the following non-IPMI features. This list does not preclude support for future enhancements or additions.

- In-circuit BMC firmware update.
- Fault resilient booting (FRB): FRB2 is supported by the watchdog timer functionality
- Chassis intrusion detection and chassis intrusion cable presence detection.
- Basic fan control using T-Control version 2 SDRs.

- Fan redundancy monitoring and support.
- Power supply redundancy monitoring and support.
- Hot-swap fan support.
- Acoustic management: Support for multiple fan profiles.
- Signal testing support: The BMC provides test commands for setting and getting platform signal states.
- The BMC generates diagnostic beep codes for fault conditions.
- System GUID storage and retrieval.
- Front panel management: The BMC controls the system status LED and chassis ID LED. It supports secure lockout of certain front panel functionality and monitors button presses. The chassis ID LED is turned on using a front panel button or a command.
- Power state retention.
- Power fault analysis.
- Intel® Light-Guided Diagnostics.
- Power unit management: Support for power unit sensor. The BMC handles power-good dropout conditions.
- DIMM temperature monitoring: New sensors and improved acoustic management using closed-loop fan control algorithm taking into account DIMM temperature readings.
- Address Resolution Protocol (ARP): The BMC sends and responds to ARPs (supported on embedded NICs).
- Dynamic Host Configuration Protocol (DHCP): The BMC performs DHCP (supported on embedded NICs).
- Chassis intrusion fan interactions.
- Platform environment control interface (PECI) thermal management support.

4.2 Advanced Management Feature Support

This section explains the advanced management features supported by BMC firmware.

4.2.1 Enabling Advanced Management Features

Advanced management features will only be enabled by the BMC when it detects the presence of the Intel® Remote Management Module 3 (Intel® RMM3) card. Without the Intel® RMM3, the advanced features will be dormant.

4.2.1.1 RMM3

The Intel® RMM3 provides the BMC with an additional dedicated network interface. The dedicated interface will consume its own LAN channel. Additionally, the Intel® RMM3 will provide additional flash storage for advanced features like WS-MAN.

4.2.2 Keyboard, Video, Mouse (KVM) Redirection

The BMC firmware supports keyboard, video, and mouse redirection over LAN. This feature is available remotely from the embedded web server as a Java applet. This feature is only enabled when the RMM3 is present.

- **Keyboard and Mouse**
  The keyboard and mouse are emulated by the BMC as USB human interface devices.

- **Video**
  Video output from the KVM subsystem is equivalent to the video output on the local console. Video redirection is available from the point video is initialized by the system BIOS.

- **Availability**
  Up to two remote KVM sessions are supported.

  The default inactivity timeout is 30 minutes, but may be changed through the embedded web server. Remote KVM activation does not disable the local system keyboard, video, or mouse. Remote KVM is not deactivated by local system input, unless the feature is disabled locally.

  KVM sessions will persist across system reset, but not across an AC power loss.

4.2.3 Media Redirection

The embedded web server provides a Java applet to enable remote media redirection. This may be used in conjunction with the remote KVM feature, or as a standalone applet. This feature is only enabled when the RMM3 is present.

The media redirection feature is intended to allow system administrators or users to mount a remote IDE or USB CD-ROM, floppy drive, or a USB flash disk as a USB device to the server. Once mounted, the remote device appears just like a local device to the server, allowing system administrators or users to install software (including operating systems, copy files, update BIOS, and so forth) or boot the server from this device. USB2.0 needs to be supported for better performance.

The following capabilities are supported:

- The operation of remotely mounted devices is independent of the local devices on the server. Both remote and local devices are useable in parallel.
- Either IDE (CD-ROM, floppy) or USB devices can be mounted as a remote device to the server.
- It is possible to boot all supported (P1) Microsoft Windows and Linux operating systems from the remotely mounted device and to boot from disk IMAGE (*.IMG) files.
- It is possible to mount at least two devices concurrently.

- The mounted device is visible to (and useable by) the managed system's operating system and BIOS in both pre-boot and post-boot states.
- The mounted device shows up in the BIOS boot order and it is possible to change the BIOS boot order to boot from this remote device.
- It is possible to install an operating system on a bare metal (no operating system present) server using the remotely mounted device. This may also require the use of KVM-r to configure the operating system during install.

4.2.4 Availability

The default inactivity timeout is 30 minutes, but may be changed through the embedded web server.

Media redirection sessions will persist across system reset but not across an AC power loss.

4.2.5 Web Services for Management (WS-MAN)

The BMC firmware supports the Web Services for Management (WS-MAN) specification.

4.2.6 Local Directory Authentication Protocol (LDAP)

The BMC firmware supports the Local Directory Authentication Protocol (LDAP) protocol for user authentication. Note that IPMI users/passwords and sessions are not supported over LDAP.

4.2.7 Embedded Web server

The BMC provides an embedded web server for out of band management. User authentication is handled by IPMI user names and passwords. Base functionality for the embedded web server includes:

- Power Control – Limited control based on IPMI user privilege.
- Sensor Reading – Limited access based on IPMI user privilege.
- SEL Reading – Limited access based on IPMI user privilege.
- KVM/Media Redirection – Limited access based on IPMI user privilege. Only available when the RMM3 is present.
- IPMI User Management – Limited access based on IPMI user privilege.

The web server is available on all enabled LAN channels. See Appendix B for Integrated BMC core sensors.

4.3 Console Redirection

The BIOS supports redirection of both video and keyboard via a serial link (serial port). When console redirection is enabled, the local (host server) keyboard input and video output are passed both to the local keyboard and video connections, and to the remote console through the serial link. Keyboard inputs from both sources are considered valid and video is displayed to both outputs.

As an option, the system can be operated without a host keyboard or monitor attached to the system and run entirely via the remote console. Utilities that can be executed remotely include the BIOS setup.

4.3.1 Serial Configuration Settings

For optimal configuration of Serial Over LAN (SOL) or EMP, see *Intel® Server System Integrated Baseboard Management Controller Core External Product Specification*.

The BIOS does not require that the splash logo be turned off for console redirection to function. The BIOS supports multiple consoles, some of which are in graphics mode and some in text mode. The graphics consoles can display the logo and the text consoles receive the redirected text.

Console redirection normally ends at the beginning of the legacy OS boot (INT 19h). The operating system is responsible for continuing the redirection from that point, unless the legacy operating system redirection is selected through the BIOS setup.

Serial-over-LAN (SOL 2.0)

The BMC supports IPMI 2.0 SOL. IPMI 2.0 introduced a standard serial-over-LAN feature. Activating a SOL session requires an existing IPMI-over-LAN session. If encryption is used, it should be negotiated when the IOL session is established. SOL sessions are only supported on serial port 1 (COM1).

4.3.2 SOL, EMP and Console Redirection Use Case Model

The IBMC's integrated Super I/O is used for serial port sharing. SOL and Console Redirection on the Serial B port are mutually exclusive features. At any moment of time, only one of them works. SOL has the highest priority followed by Console Redirection.

Console Redirection is available via the Serial A or Serial B port.

Console Redirection on Serial A and Serial B are mutually exclusive features. The end user can configure only one of them at any moment of time.

Case I:

Console Redirection is enabled on Serial B with Baud = 115200, Flow Control=CTS-RTS, Terminal Type =VT100

SOL Not Active: BIOS sends data on Serial B port with 115200 Baud, flow control CTS-RTS enabled and emulates the terminal Type as VT100. In summary, the BIOS uses the setup settings and performs Console Redirection on Serial B.

SOL Found Active: The BIOS prioritizes SOL over Serial B Console Redirection. The BIOS queries the BMC for SOL Baud Rate and overrides the setup Serial B Console Redirection Baud with SOL Baud Rate.

The BIOS also enables Hardware Flow control between the BIOS and BMC and forces terminal emulation type as PC-ANSI.

Since Serial B is a shared port between the BIOS and BMC, if SOL is found active, the user sees no data on Serial B port.

Note: *The SOL override settings are only valid for the current BIOS boot. On the next boot, if SOL is not found active, the BIOS uses the Console Redirection settings set by the user and performs Console Redirection either on Serial A or Serial B port.*

Case II:

Console Redirection is enabled on Serial A with Baud = 115200, Flow Control=CTS-RTS, Terminal Type =VT100.

The BIOS sends data on Serial A port with 115200 Baud, flow control CTS-RTS enabled and emulates the terminal Type as VT100. In summary, the BIOS uses the setup settings and performs Console Redirection on Serial A.

Legacy Console Redirection:

The BIOS enables Legacy OS redirection on Serial A or Serial B, depending upon the BIOS settings. Legacy OS redirection happens at the same Baud, Flow Control and Terminal Type set by the user.

SOL Found Active: If SOL is found active, then the BIOS overrides the BIOS settings and **AUTO** enables Legacy Operating System redirection on the SOL console.

4.4 Node Manager

4.4.1 Overview

Node Management (NM) provides the system with a method of monitoring power consumption and thermal output, and adjusting system variables to control those factors. As opposed to component-level power/thermal solutions (such as Demand Based Switching), Node Management functions at the platform level.

NM is only available on platforms that support PMBus-compliant power supplies. The BMC supports NM specification version 1.5. Additionally, the platform chipset must have an NM-capable Management Engine (ME).

4.4.2 Command Bridging

The majority of BMC functionality to support the NM is handled by bridging commands and alerts. The ME participating in Node Management acts as a satellite controller on the BMC's secondary IPMB. The BMC does not own any platform event filters or traps for NM-related events. You should configure these events in the NM by server management software.

4.4.3 External Communications Link

The BMC bridges commands between external software agents and the system's ME using standard IPMI *Send Message* commands. See the command bridging section in the *Intelligent Platform Management Interface Specification Second Generation v2.0* for more information.

All NM-related IPMB transactions utilize the secondary IPMB. This is a private I^2C bus that is only accessible by the BMC and ME. Please see the appropriate platform appendix for channel and bus number information.

4.4.4 Alerting

The ME's Node Manager may need to send alerts to external software agents. The NM uses two different methods to send an alert. Each method is outlined in the following sections.

- **Fault Events**

  Alerts that signify fault conditions and should be recorded in the system SEL will be sent to the BMC by the ME using the IPMI *Platform Event Message* command. The BMC deposits these events into the SEL. The external SW must configure the BMC's PEF and alerting features to send that event out as an IPMI LAN alert, directed to the SW application over the LAN link.

- **Informational Events**

  Alerts that provide useful notification to the external SW for NPTM management but do not represent significant fault conditions and do not need to be entered in the SEL are sent to the BMC using the IPMI *Alert Immediate* command. This requires the external SW application provide the NM on the ME with the alert destination and alert string information needed to properly form and send the alert. The external SW must first properly configure the alert destination and string in the BMC LAN configuration using standard IPMI commands, then provide the associated selectors to the BMC using the *Set Node Manager Alert Destination* OEM command.

4.4.5 System Information Passed to ME and POST Complete Notification

The BIOS sends the BMC the following information during POST:

- Number of supported P-states
- Number of supported T-states
- Platform Info (data from processor MSR 0CEh)
- TDP value per CPU

When the BMC detects that POST has completed, the BMC passes on the BIOS-provided system information to the ME. As part of this command transaction to the ME, the BMC also provides the total number of installed CPUs, the Icc_TDC value for each CPU (retrieved by the BMC via PECI), and a notification that POST has completed.

At system startup the ME may query the BMC for the following information using IPMI OEM commands:

- Inlet air temperature reading – This corresponds to the temperature reading from the Front Panel Ambient Temperature sensor. Some platforms may not support this feature. Refer to the applicable platform appendix.

4.4.6 ACPI Mode Notification

The BIOS notifies the BMC when the system enters and exits ACPI mode. The BMC, in turn, notifies the ME. The NM power-limiting functionality is only available when the system is operating in ACPI mode (an ACPI-compliant operating system is running).

4.4.7 Persistence Across Boots

Data passed to the ME will persist across boots, but will not persist across AC power loss.

4.5 Power Management Bus (PMBUS)

The BMC firmware implements power-management features based on the Power Management Bus (PMBus) 1.1 Specification. The following sensor types are supported for systems that contain PMBus-compliant power supplies and a PMBus-compliant power distribution board.

- Power Supply Input Power Sensor
- Power Supply Output Current Sensor
- Power Supply Temperature Sensor

5. Connector / Header Locations and Pin-outs

5.1 Board Connectors

Table 10. Board Connector Matrix

Connector	Quantity	Reference Designators	Connector Type	Pin Count
Memory	8	J1D1,J1D2,J1D3,J1D4,J8K2,J8K1,J9K2,J9K3	DDR3 DIMM Sockets	240x8
PCI Express* x8	3	J4B1,J4B2,J5B1	Card Edge	98x3
PCI Express* x4	1	J2B2	Card Edge	64
PCI 32/33	1	J3B1	Card Edge	120
SATA	6	J1B4,J1B3,J1A2,J1B1,J1B2,J2B1	App-specific Plug	7x6
SGPIO	1	J1C1	Header	4
IPMB	2	J8B1	Header	4
HSBP	1	J9B1	Header	4
Fans	5	J3K1,J7K2,J3K2,J8K3,J8B4	Header	4x5
RMM3	1	J3C1	RMM3 connector	34
Power Supply	3	J9B3 J7K1 J9E1	Header	24 8 5
USB	4	J1A3 J2A2 J5A1 J6A1	Dual USB/LAN Connector on the rear panel; dual USB headers on the board	10 10 22 22
VGA	1	J7A1	Connector	15
Serial Port	2	J8A1 J9A1	DB-9 rear connector 2x5 Header	9 10
GigE	2	J5A1 J6A1	USB/LAN combo connector	22 22
Front Panel	1	J9E2	Header	24
SATA Key	1	J7B1	Header	3
Intrusion Detect	1	J8B3	Header	2
Battery	1		Battery Holder	2

5.2 Power Connectors

The main power supply connection has an SSI-compliant 2x12 pin connector (J9B3) and two additional power-related connectors: one SSI-compliant 2x4 pin power connector (J7K1) that

supports an additional 12 V and one SSI-compliant 1x5 pin connector (J9C1) that provides I^2C monitors the power supply.

Table 11. EPS12V 2x12 Connector (J9B3)

Pin	Signal Name	Color	Pin	Signal Name	Color
1	+3.3V	Orange	13	+3.3V	Orange
2	+3.3V	Orange	14	-12V	Blue
3	GND	Black	15	GND	Black
4	+5V	Red	16	PS_ON	Green
5	GND	Black	17	GND	Black
6	+5V	Red	18	GND	Black
7	GND	Black	19	GND	Black
8	PWR_GD	Gray	20	NC	N/A
9	5VSB	Purple	21	+5V	Red
10	+12V	Yellow	22	+5V	Red
11	+12V	Yellow	23	+5V	Red
12	+3.3V	Orange	24	GND	Black

Table 12. EPS12V 2x4 Connector (J7K1)

Pin	Signal Name	Color	Pin	Signal Name	Color
1	GND	Black	5	+12V	Yellow
2	GND	Black	6	+12V	Yellow
3	GND	Black	7	+12V	Yellow
4	GND	Black	8	+12V	Yellow

Table 13. EPS12V 1x5 Connector (J9E1)

Pin	Signal Name	Signal Name
1	SMB_PWR_3V3SB_CLK	White
2	SMB_PWR_3V3SB_DAT	Yellow
3	NC	N/A
4	GND	Black
5	3.3V SENSE+	Orange

5.3 Riser Card Slot

The Intel® Sever Board S5500BC has one riser card slot (J4B2). The riser card slot supports one low-profile half-length PCI Express* 2.0 x8 add-in card.

Table 14. Low-profile PCI Riser Card Pin-out (J3C1)

Pin	Name	Slot	Name	Pin
B1	12V		PRSNT1#	A1
B2	12V		12V	A2
B3	12V		12V	A3
B4	GND		GND	A4
B5	SMCLK		JTAG2	A5
B6	SMDATA		JTAG3	A6
B7	GND		INTRU#	A7
B8	3.3V		JTAG5	A8
B9	JTAG1		3.3V	A9
B10	3.3VAux		3.3V	A10
B11	WAKE#		PERST#	A11
Key				
B12	3.3V		GND	A12
B13	GND		REFCLK1+	A13
B14	PETxP0		REFCLK1-	A14
B15	PETxN0		GND	A15
B16	GND		PERxP0	A16
B17	PRSNT2#		PERxN0	A17
B18	GND		GND	A18
B19	PETxP1		3.3V	A19
B20	PETxN1		GND	A20
B21	GND		PERxP1	A21
B22	GND		PERxN1	A22
B23	PETxP2		GND	A23
B24	PETxN2		GND	A24
B25	GND		PERxP2	A25
B26	GND		PERxN2	A26
B27	PETxP3		GND	A27
B28	PETxN3		GND	A28
B29	GND		PERxP3	A29
B30	3.3V		PERxN3	A30
B31	PRSNT2#		GND	A31
B32	GND			A32
B33	PETxP4			A33

Pin	Name	Slot	Name	Pin
B34	PETxN4		GND	A34
B35	GND		PERxP4	A35
B36	GND		PERxN4	A36
B37	PETxP5		GND	A37
B38	PETxN5		GND	A38
B39	GND		PERxP5	A39
B40	GND		PERxN5	A40
B41	PETxP6		GND	A41
B42	PETxN6		GND	A42
B43	GND		PERxP6	A43
B44	GND		PERxN6	A44
B45	PETxP7		GND	A45
B46	PETxN7		GND	A46
B47	GND		PERxP7	A47
B48	PRSNT2#		PERxN7	A48
B49	PE Strap		GND	A49

5.4 RMM3 Connector

The Intel® Sever Board S5500BC provides a connector (J3C1) to support a RMM3 card. The RMM3 card provides the Integrated BMC with an additional dedicated network interface. The dedicated interface uses a separate LAN channel. The RMM3 provides additional flash storage for advanced features such as the WS-MAN. The following table shows the pin-out settings for this connector.

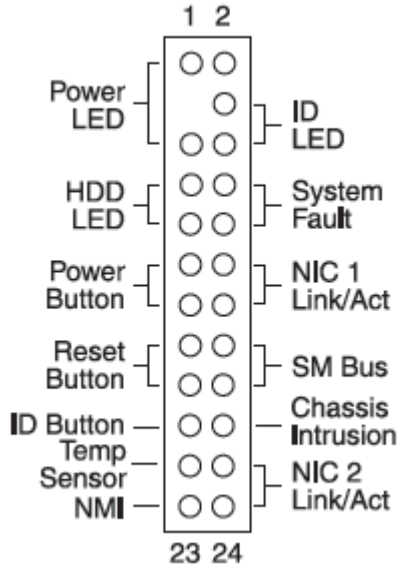
Table 15. RMM3 Connector Pin-out (J3C1)

Pin	Signal Name	Pin	Signal Name
1	P3V3	2	RMI_IBMC_MAC_MDIO
3	P3V3	4	RMII_IBMC_MAC_MDC
5	GND	6	RMII_IBMC_GCM4_RXD<1>
7	GND	8	RMII_IBMC_GCM4_RXD<0>
9	GND	10	RMII_IBMC_GCM4_CRS_DV
11	GND	12	CLK_50M_GCM4
13	GND	14	RMII_IBMC_GCM4_RX_ER
15	GND	16	RMII_IBMC_GCM4_TX_EN
17	GND	18	Key
19	GND	20	RMII_IBMC_GCM4_TXD<0>
21	GND	22	RMII_IBMC_GCM4_TXD<1>
23	P3V3	24	SPI_IBMC_BK_CS_N
25	P3V3	26	TP_GCM4_P26
27	P3V3	28	SPI_IBMC_BK_DO
29	GND	30	SPI_IBMC_BK_CLK
31	GND	32	SPI_IBMC_BK_DI
33	GND	34	FM_GCM4_PRSNT_N

5.5 SSI Front Panel Connector

The Intel® Server Board S5500BC provides a 24-pin SSI control panel connector (J9E2) for use with a non-Intel chassis. Several LEDs, such as the power status LED, HDD LED, and LAN status LED, are provided on the front panel to provide a visual status. The following table provides the pin-out information for this connector.

Table 16. Front Panel SSI Standard 24-pin Connector Pin-out (J9E2)

Pin	Signal Name	Control Panel Pin-out	Pin	Signal Name
1	P3V3_STBY		2	P3V3_STBY
3	Key		4	P5V_STBY
5	FP_PWR_LED_N_R		6	FP_ID_LED_R1_N
7	P3V3（(HDD Activity LED Anode）		8	LED_STATUS_GREEN_R_N
9	LED_HDD_ACTIVITY_R_N		10	LED_STATUS_AMBER_R_N
11	FP_PWR_BTN_R_N		12	P3V3_STBY
13	GND(Power Button GND)		14	LED_NIC1_LINK_ACT_BUF_R_N
15	RST_IBMC_RST_BTN_N		16	SMB_SEN_3V3SB_DAT
17	GND (Reset GND)		18	SMB_SEN_3V3SB_DAT
19	FP_ID_BTN_R_N		20	FM_IBMC_INTRUDER_HDR
21	PU_FM_SIO_TEMP_SENSOR		22	P3V3_STBY
23	FP_NMI_BTN_R_N		24	LED_NIC0_LINK_ACT_BUF_R_N

5.6 I/O Connector Pin-out Definition

5.6.1 VGA Connector

The following table details the pin-out of the VGA connector (J7A1).

Table 17. VGA Connector Pin-out (J7A1)

Pin	Signal Name
1	VGA_RED
2	VGA_GREEN
3	VGA_BLUE
4	RESERVED
5	GND
6	GND
7	GND
8	GND
9	5V
10	GND
11	RESERVED
12	DDCDAT
13	HSYNC
14	VSYNC
15	DDCCLK

5.6.2 SATA II Connectors

The Intel® Server Board S5500BC provides six Serial ATA connectors (J1B4, J1B3, J1A2, J1B1, J1B2, and J2B1).

Table 18. SATA Connector Pin-out (J1B4, J1B3, J1A2, J1B1, J1B2, and J2B1)

Pin	Signal Name	Description
1	GND	GND1
2	SATA#_TX_P_C	Positive side of transmit differential pair
3	SATA#_TX_N_C	Negative side of transmit differential pair
4	GND	GND2
5	SATA#_RX_N_C	Negative side of Receive differential pair
6	SATA#_RX_P_C	Positive side of Receive differential pair
7	GND	GND3

5.6.3 Serial Port Connectors

The Intel® Server Board S5500BC provides one external 9-pin Serial 'A' port (J8A1) and one internal 9-pin Serial B port header (J9A1). Serial A is a standard DB-9 interface for pedestal products and RJ-45 for rack products and is located on the rear I/O panel of the server board. The following tables define the pin-outs for each:

Table 19. 9-pin External Serial A Port Header Pin-out (J8A1)

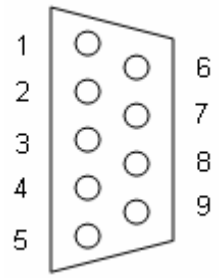
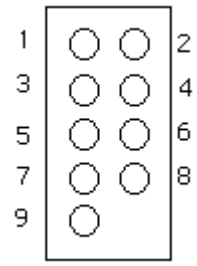
Pin	Signal Name	Description
1	SPA_DCD	
2	SPA_SIN_N	
3	SPA_SOUT_N	
4	SPA_DTR	
5	GND	
6	SPA_DSR	
7	SPA_RTS	
8	SPA_CTS	
9	SPA_RI	

Table 20. Internal Serial B Port Header Pin-out (J9A1)

Pin	Signal Name	Serial Port A Header Pin-out
1	DCD	
2	DSR	
3	RXD	
4	RTS	
5	TXD	
6	CTS	
7	DTR	
8	RI	
9	GND	

5.6.4 USB and GigE Connector

The Intel® ICH10R I/O Controller Hub on the Intel® Server Board S5500BC supports eleven USB ports. Four ports are connected to two USB+RJ-45 NIC stacked connectors on the rear panel of the server board. The following table lists the pin-out information for the external USB connectors (J5A1, J6A1).

Table 21. External USB and GbE connector Pin-out (J5A1, J6A1)

Pin	Signal Name
1	USB PWR
2	USBP_1N
3	USBP_1P
4	GND
5	USB PWR
6	USB_0N
7	USB_0P
8	GND
9	TERM
10	MDI0P
11	MDI0N
12	MDI1P
13	MDI1N
14	MDI2P
15	MDI2N
16	MDI3P
17	MDI3N
18	GND
19	GRN_C
20	GRN_A
21	GRN_C/YEL_A
22	GRN_A/YEL_C

Four ports are connected to the two 2x5 headers (J1A3, J2A2) on the Intel® Server Board S5500BC. The following table provides the pin-out information for the header. The two headers are identical.

Table 22. Internal USB Header Pin-out (J1A3, J2A2)

Pin	Signal Name	Description
1	USB PWR	USB Power
2	USB PWR	USB Power
3	USB_5N	USB Port 5 Negative Signal
4	USB_6N	USB Port 6 Negative Signal
5	USB_5P	USB Port 5 Positive Signal
6	USB_6P	USB Port 6 Positive Signal
7	Ground	Ground
8	Ground	Ground
9	Key	N/A
10	NC	No Connection

5.7 Fan Headers

The Intel® Server Board S5500BC incorporates a system fan circuit that supports five SSI compliant 4-pin fan connectors. The two 4-pin fan connectors are for processor cooling fans: CPU_1 fan (J3K1) and CPU_2 fan (J7K2). The three 4-pin fan connectors are for system fans system fan 1, system fan 2, and system fan 3 (J3K2, J8K3, and J8B4). The pin configuration for each fan connector is identical. The following table provides pin-out information.

Table 23. CPU and System Fan Connector Pin-out (J3K1, J7K2, J3K2, J8K3, J8B4)

Pin	Signal Name	Type	Description
1	Ground	GND	GROUND is the power supply ground.
2	12V	Power	Power supply 12 V.
3	Fan Tach	Out	FAN_TACH signal is connected to the BMC to monitor the fan speed.
4	Fan PWM	In	FAN_PWM signal to control the fan speed.

Note: *The Intel® Server Board S5500BC supports peripheral components and contains a number of high-density VLSI and power delivery components that require adequate air flow to cool. Intel designs the chassis to meet the intended thermal requirements of these components when the fully integrated system is used together. If Intel server building blocks are not used in the system, it is the responsibility of the system integrator to consult vendor datasheets and operating parameters for the air flow requirements for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the Intel® Server Board S5500BC does not operate correctly when used outside of the published operating parameters.*

5.8 SGPIO Header

One 4-Pin SGPIO Connector (J1C1).

Table 24. SGPIO connector Pin-out (J1C1)

Pin	Signal Name
1	SCLK
2	SLOAD
3	SDATAOUT0
4	SDATEOUT1

5.9 Chassis Intrusion Header

A 2-pin Chassis intrusion header (J8B3) is provided. This is intended to support micro switches that close, making a connection to ground when the chassis is opened or removed. The intrusion signal is routed to the Integrated BMC internal intrusion circuit, which resides in the RTC well.

Table 25. Chassis Intrusion connector Pin-out (J8B3)

Output	Signal Name
To BMC	FM_IBMC_INTRUDER_HDR_N
To FP	FM_IBMC_INTRUDER_HDR

5.10 SMB Hot-Swap Backplane (HSBP) Header

Table 26. SMB HSBP connector Pin-out (J9B1)

Pin	Signal Name
1	SMB_HSBP_5V_DAT
2	GND
3	SMB_HS BP_5V_CLK
4	P5V Pull-up

5.11 SATA RAID Key Header

Table 27. SATA connector Pin-out (J7B1)

Pin	Signal Name
1	GND
2	FM_ICH_RAID_KEY
3	GND

5.12 IPMB Header

Table 28. IPMB Connector Pin-out (J8B1)

Pin	Signal Name
1	SMB_IPMB_5VSB_DAT
2	GND
3	SMB_IPMB_5VSB_CLK
4	P5V_STBY

6. Jumper Block Settings

The Intel® Server Board S5500BC has several jumper blocks that can be used to configure, recover, or enable /disable specific features of the server board. Pin 1 on each jumper block is denoted by "▼".

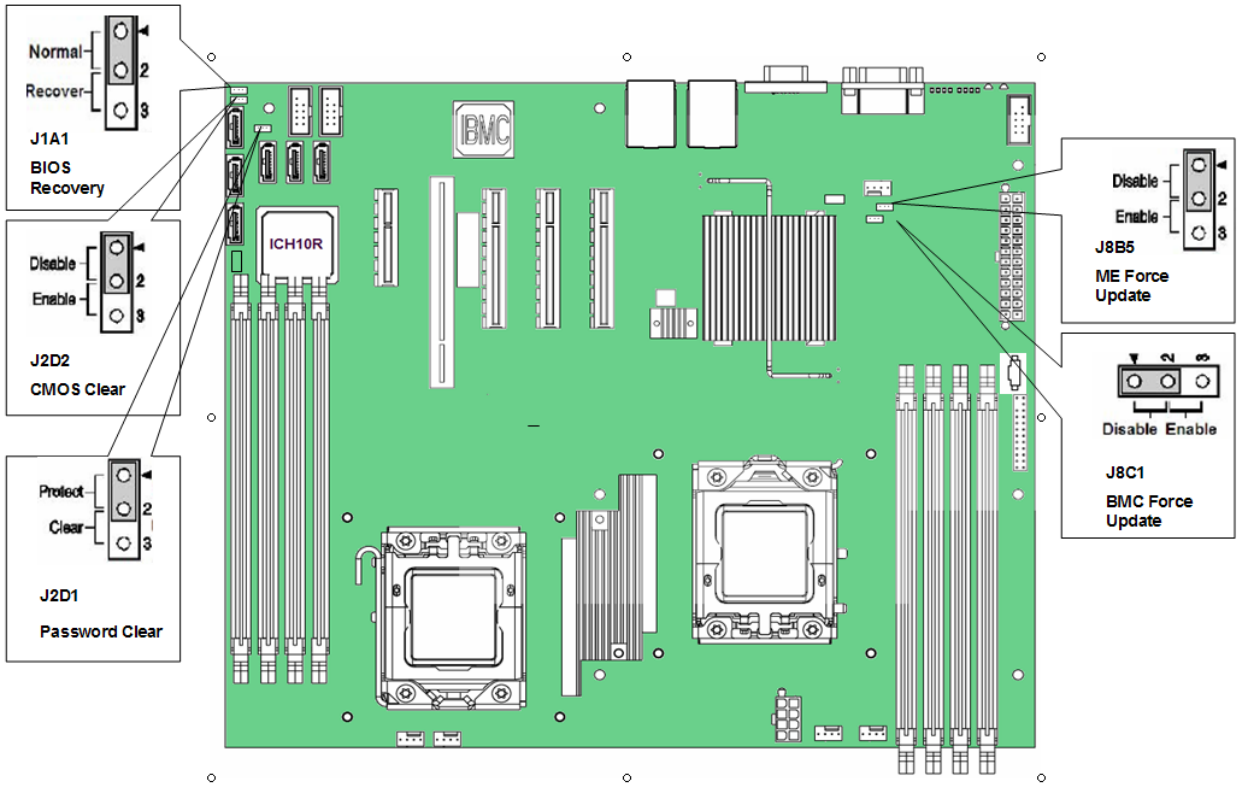


Figure 19. Jumper Blocks

Table 29. Jumper Block Matrix

Jumper Name	Pins	What happens at system reset…
J8C1: BMC Force Update	**1-2**	BMC Firmware Force Update Mode – Disabled (**Default**)
	2-3	BMC Firmware Force Update Mode – Enabled
J2D1: Password Clear	**1-2**	These pins should have a jumper in place for normal system operation. (**Default**)
	2-3	If these pins are jumpered, administrator and user passwords will be cleared on the next reset. **Note**: These pins should not be jumpered for normal operation.
J2D2: CMOS Clear	**1-2**	These pins should have a jumper in place for normal system operation. (**Default**)
	2-3	If these pins are jumpered, the CMOS settings will be cleared on the next reset **Note**: These pins should **not** be jumpered for normal operation.

Jumper Name	Pins	What happens at system reset…
J1A1: BIOS Recovery	1-2	These pins should have a jumper in place for normal system operation.(**Default**)
	2-3	The main system BIOS will not boot with these pins jumpered. **Note**: The system will boot from EFI-bootable recovery media with a recovery BIOS image.
J8B5: ME Force Update	1-2	These pins should have a jumper in place for normal system operation. **(Default)**
	2-3	ME force update model.

7. Intel® Light-Guided Diagnostics

The Intel® Server Board S5500BC has several on-board diagnostic LEDs to assist in troubleshooting board-level issues. Functionality of the on-board LEDs is owned by the BMC and system BIOS. This section provides an overview of each LED including the location and a high level-usage description.

7.1 5-Volt Standby LED

Several server management features on the Intel® Server Board S5500BC require a 5-volt stand-by from the power supply. The features and components that require this voltage be present when the system is "Off" include the Integrated BMC, onboard NICs, and optional Intel® Remote Management Module 3 connector with Intel® RMM3 installed. (Refer to Figure 10: Intel® Server Board S5500BC Layout for the location.)

7.2 System ID and Status LED

The Intel® Server Board S5500BC provides a System ID LED and a Status LED. Refer to Figure 10 for the location. The blue system identification LED helps identify a system for servicing. This is especially useful when the system is installed in a high-density rack or cabinet populated with several similar systems. The blue "System ID" LED can be illuminated using either of two mechanisms.

- By pressing the system ID button on the system control panel, the ID LED displays a solid blue color until the button is pressed again.
- By issuing the appropriate hex IPMI "Chassis Identify" value, the ID LED either blinks blue for 15 seconds and turns off or blinks indefinitely until the appropriate hex IPMI Chassis Identify value is issued to turn it off.

Note: *The system status LED shows the state for the current, most severe fault. For example, if there was a critical fault due to one source and a non-critical fault due to another source, the system status LED would be solid, which is the state for a critical fault.*

The system status / fault LED is a bi-color LED. Green (status) indicates normal (solid-on) or degraded (blink) operation. Amber (fault) indicates a failure state and overrides the green status. The system status LED is controlled by the BMC, but includes non-BMC owned sensors in a fault determination such as BIOS-owned sensors.

When the Intel® Server Board S5500BC is powered down (transitions to the DC-off state or S5), the BMC is still on standby power and retains the sensor and front panel status LED state established before the power-down event. If the system status is OK (LED in solid green state), then the system status LED is off when the system is powered down.

The LED state information in the following table is dependent on the underlying sensor support.

Table 30. System Status LED Indicator States

Color	State	System Status	Description
Green	Solid on	OK	System booted and ready
Green	blink	Degraded	System degraded: ▪ Non-critical temperature threshold asserted. ▪ Non-critical voltage threshold asserted. ▪ Non-critical fan threshold asserted. ▪ Fan redundancy lost, sufficient system cooling maintained. This does not apply to non-redundant systems. ▪ Power supply predictive failure. ▪ Power supply redundancy lost. This does not apply to non-redundant systems. Correctable errors over a threshold of 10 and migrating to a spare DIMM (memory sparing). This indicates the user no longer has spared DIMMs indicating a redundancy lost condition. Corresponding DIMM LED should light up.
Amber	blink	Non-fatal	Non-fatal alarm – system is likely to fail: ▪ CATERR asserted. ▪ Critical temperature threshold asserted. ▪ Critical voltage threshold asserted. ▪ Critical fan threshold asserted. ▪ VRD hot asserted. ▪ SMI Timeout asserted.
Amber	Solid on	Fatal	Fatal alarm – system has failed or shutdown: ▪ CPU Missing. ▪ Thermtrip asserted. ▪ Non-recoverable temperature threshold asserted. ▪ Non-recoverable voltage threshold asserted. ▪ Power fault / Power Control Failure. ▪ Fan redundancy lost, insufficient system cooling. This does not apply to non-redundant systems. ▪ Power supply redundancy lost; insufficient system power. This does not apply to non-redundant systems.
Off	N/A	Not ready	AC power off, if no degraded, non-critical, critical, or non-recoverable conditions exist.

7.3 DIMM Fault LEDs

The Intel® Server Board S5500BC provides a memory fault LED for each DIMM slot. Refer to Figure 10 for the LEDs' location. The DIMM fault LED is illuminated when the system BIOS disables a DIMM when it reaches a specified number of failures or if specific critical DIMM failures are detected.

Table 31. DIMM LEDs Indicator States

LED Name	Voltage resources	Color	Status	Description
DIMM#A1-E1 fault (7 total)	5V Aux	Amber	On	Corresponding DIMM Fault
		N/A	Off	Normal

7.4 Fan Fault LEDs

The Intel® Server Board S5500BC has a fan fault LED associated with each fan header. In the event of a critical threshold event status, the BMC will light a fan fault LED. The fan LED sensor remains on until the system is reset either by a DC power-on or a system reset. Refer to Figure 10 for the location of the LEDs.

Table 32. Fan LED Indicator States

LED Name	Voltage resources	Color	Status	Description
FAN fault (5 total)	5V Aux	Amber	On	Corresponding Fan fault
		N/A	Off	Normal

7.5 Post Code Diagnostic LEDs

During the boot process, the BIOS executes several platform configuration processes with specific hex POST code numbers. As each configuration routine is started, the BIOS displays the POST code on the POST code diagnostic LEDs on the back edge of the Intel® Server Board S5500BC. The diagnostic LEDs can identify the last POST process executed to help troubleshoot a system hang during POST.

Each POST code is represented by a combination of colors from the four LEDs. The LEDs can display three colors: green, red, and amber. The POST codes are divided into an upper nibble and a lower nibble. Each bit in the upper nibble is represented by a red LED and each bit in the lower nibble is represented by a green LED. If both bits are set in the upper and lower nibbles, then both red and green LEDs are lit and an amber color appears. If both bits are clear, then the LED is off.

Refer to Appendix D for a complete overview of how the LEDs are read and for a list of all supported POST codes. For more information on the location of the LEDs, refer to Figure 10 for the location of the LEDs.

8. Power and Environmental Specifications

8.1 Intel® Server Board S5500BC Design Specifications

Operating the server board at conditions beyond the specifications outlined in the following table may cause permanent damage to the system. Exposure to maximum conditions for extended periods may impact system reliability.

Table 33. Server Board Design Specifications

Parameter	Limit
Operating Temperature	0º C to 55º C (32º F to 131º F), at product airflow specification
Non-Operating Temperature	-40º C to 70º C (-40º F to 158º F)
DC Voltage	± 5% of all nominal voltages
Shock (unpackaged)	50 G trapezoidal waveform. Velocity change of 170 inches/sec
Shock (packaged): < 20 lbs ≥ 20 to < 40 ≥ 40 to < 80 ≥ 80 to < 100 ≥100 to < 120 ≥120	 36 inches 30 inches 24 inches 18 inches 12 inches 9 inches
Vibration (unpackaged)	5 Hz to 500 Hz 3.13 G_{rms} random.

***Note**: Intel® Server Boards support add-in peripherals and contain a number of high-density VLSI and power delivery components require proper airflow for cooling. Intel develops and tests chassis so when they are used with Intel® server building blocks, the integrated system will meet component thermal requirements. If Intel components are not installed, it is the responsibility of the system integrator to consult vendor datasheets and operating parameters to determine the air flow requirements for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside of the published operating parameters.*

8.2 Baseboard Power Requirements

This section reviews the power supply design guidelines for a system with an Intel® Server Board S5500BC. The voltage and current specifications and power supply on/off sequencing characteristics are provided.

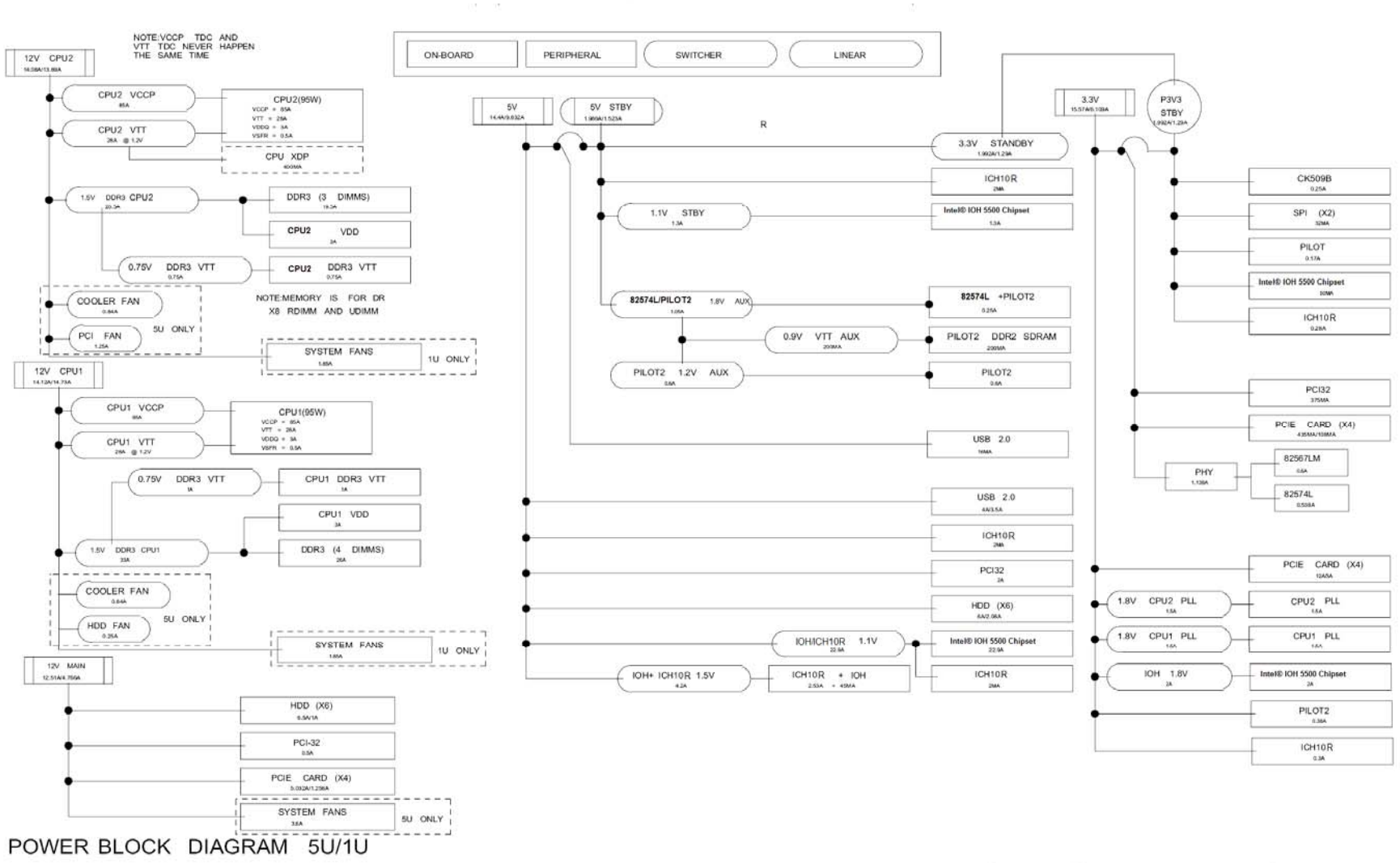


Figure 20. Power Distribution Block Diagram

8.2.1 Power Requirements

The power supply generates power at +5 V, +3.3 V, +12 V, -12 V, and +5 VSB (standby). The other required voltages on the Intel® Server Board S5500BC Server are generated using the linear and switching regulators. An external potentiometer is used to margin the critical voltages by +/- ±5%. The following table summarizes the maximum power requirements for all on-board and peripheral devices, as well as the system, for proper operation. The total power requirement for the board is calculated as follows. The main power supply connector provides +12 V, -12 V, +3.3 V, and +5.0 V. Other voltages are derived using switching regulators. In order to select the power supply, it is important to know the current rating requirement for each of the voltage rails. The maximum power required to operate the server board under normal conditions with peripherals is about 80% of the total worst case power dissipation or 503 W. This includes a 15% regulator efficiency.

8.2.2 Turn On No Load Operation

At power on, the system should present a no load condition to the power supply. In this state, the voltage regulation limits for the 3.3 V and 5 V are relaxed to +/-10%, and the +12 V rail limits are relaxed to +10/-8%. When operating loads are applied, the voltages must regulate within normal limits.

Table 34. No load Operating Range

Voltage	Minimum Continuous	Maximum Continuous	Peak
+3.3 V	0 A	7 A	
+5 V	0 A	5 A	
+12 V [1]	0 A	5 A	7 A
+12 V [2]	0 A	5 A	7 A
+12 V [3]	0 A	6 A	
+12 V [4]	0 A	5 A	
-12 V	0 A	0.5 A	
+5 VSB	0.1 A	3.0 A	3.5 A

Notes:

1. Maximum continuous total DC output power should not exceed 400 W.
2. Peak load on the combined 12 V output should not exceed 49 A.
3. Maximum continuous load on the combined 12 V output should not exceed 44 A.
4. Peak total DC output power should not exceed 650 W.

8.2.3 Grounding

The grounds of the pins of the power supply output connector provide the power return path. The output connector ground pins should be connected to safety ground (power supply enclosure).

Note: *The grounding should be well designed to ensure passing the maximum allowed common mode noise levels.*

The power supply should be provided with a reliable protective earth ground. All secondary circuits should be connected to protective earth ground. Resistance of the ground returns to the chassis should not exceed 1.0 mΩ. This path can be used to carry the DC current.

8.2.4 Standby Outputs

The 5 VSB output should be present when an AC input greater than the power supply turn on voltage is applied.

8.2.5 Remote Sense

The power supply has remote sense return (ReturnS) to regulate out ground drops for all output voltages: +3.3 V, +5 V, +12 V1, +12 V2, +12 V3, -12 V, and 5 VSB. The power supply uses remote sense (3.3 VS) to regulate out drops in the system for the +3.3 V output. The +5 V, +12 V1, +12 V2, +12 V3, –12 V, and 5 VSB outputs only use remote sense referenced to the ReturnS signal.

The remote sense input impedance to the power supply must be greater than 200 Ω on 3.3 VS and 5 VS; this is the value of the resistor connecting the remote sense to the output voltage internal to the power supply. Remote sense must be able to regulate out a minimum of a 200 mV drop on the +3.3 V output.

The remote sense return (ReturnS) must be able to regulate out a minimum of a 200 mV drop in the power ground return. The current in any remote sense line should be less than 5 mA to prevent voltage sensing errors. The power supply must operate within the specification over the full range of voltage drops from the power supply output connector to the remote sense points.

8.2.6 Voltage Regulation

The power supply output voltages must remain within the following limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise.

Table 35. Voltage Regulation Limits

Parameter	Tolerance	Minimum	Nominal	Maximum	Units
+ 3.3V	- 5% / +5%	+3.14	+3.30	+3.46	V_{rms}
+ 5V	- 5% / +5%	+4.75	+5.00	+5.25	V_{rms}
+ 12V	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
- 12V	- 5% / +9%	-11.40	-12.00	-13.08	V_{rms}
+ 5VSB	- 5% / +5%	+4.75	+5.00	+5.25	V_{rms}

8.2.7 Dynamic Loading

The output voltages should remain within the limits for the step loading and capacitive loading specified in the following table. The load transient repetition rate should be tested between 50 Hz and 5 kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 36. Transient Load Requirements

Output	Δ Step Load Size[1]	Load Slew Rate	Test Capacitive Load
+3.3 V	6.0 A	0.25 A/μsec	250 μF
+5 V	4.0 A	0.25 A/μsec	400 μF
12 V	18.0 A	0.25 A/μsec	2200 μF 1, 2
+5 VSB	0.5 A	0.25 A/μsec	20 μF

Notes:

1. The +12 V should be tested with 2200 μF evenly divided between the four +12 V rails.
2. Step loads on each 12 V output may occur simultaneously.

8.2.8 Capacitive Loading

The power supply should be stable and meet all capacitive loading requirements. The following table outlines these conditions.

Table 37. Capacitive Loading Conditions

Output	Minimum	Maximum	Units
+3.3 V	250	6,800	μF
+5 V	400	4,700	μF
+12 V	500 each	11,000	μF
-12 V	1	350	μF
+5 VSB	20	350	μF

8.2.9 Closed-Loop Stability

The power supply should be unconditionally stable under all line/load/transient load conditions, including capacitive load ranges. A minimum of 45° phase margin and -10 dB gain margin is

required. The power supply manufacturer should provide proof of the unit's closed-loop stability with local sensing through the submission of bode plots. Closed-loop stability must be maintained at the maximum and minimum loads as applicable.

8.2.10 Common Mode Noise

The common mode noise on any output should not exceed 350 mV peak-peak over the frequency band of 10 Hz to 30 MHz.

- The measurement should be made across a 100 Ω resistor between each of the DC outputs, including ground, at the DC power connector and chassis ground (power subsystem enclosure).
- The test set-up should use an FET probe such as a Tektronix P6046* model or equivalent.

8.2.11 Ripple / Noise

The maximum allowed ripple/noise output of the power supply is defined in the following table. This is measured over a bandwidth of 0 Hz to 20 MHz at the power supply output connectors. A 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor are placed at the point of measurement.

Table 38. Ripple and Noise

+3.3 V	+5 V	+12 V	-12 V	+5 VSB
50mVp-p	50mVp-p	120mVp-p	120mVp-p	50mVp-p

8.2.12 Soft Starting

The power supply should contain a control circuit which provides a monotonic soft start for the outputs without overstressing the AC line or any power supply components at any specified AC line or load conditions. There is no requirement for rise time on the 5 V standby but the turn on/off should be monotonic.

8.2.13 Timing Requirements

The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70 ms, except for 5 VSB; it is allowed to rise from 1.0 to 25 ms. All outputs must rise monotonically. Each output voltage should reach regulation within 50 ms (T_{vout_on}) of each other during power on. Each output voltage should fall out of regulation within 400 msec (T_{vout_off}) of each other during turn off. The following tables show the timing requirements to turn the power supply on and off via the AC input with PSOn held low, and the PSOn signal with the AC input applied.

Table 39. Output Voltage Timing

Item	Description	Minimum	Maximum	Units
T_{vout_rise}	Output voltage rise time from each main output.	5.0 *	70 *	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	msec
T_{vout_off}	All main outputs must leave regulation within this time.		400	msec

*The 5 VSB output voltage rise time shall be from 1.0 ms to 25.0 ms

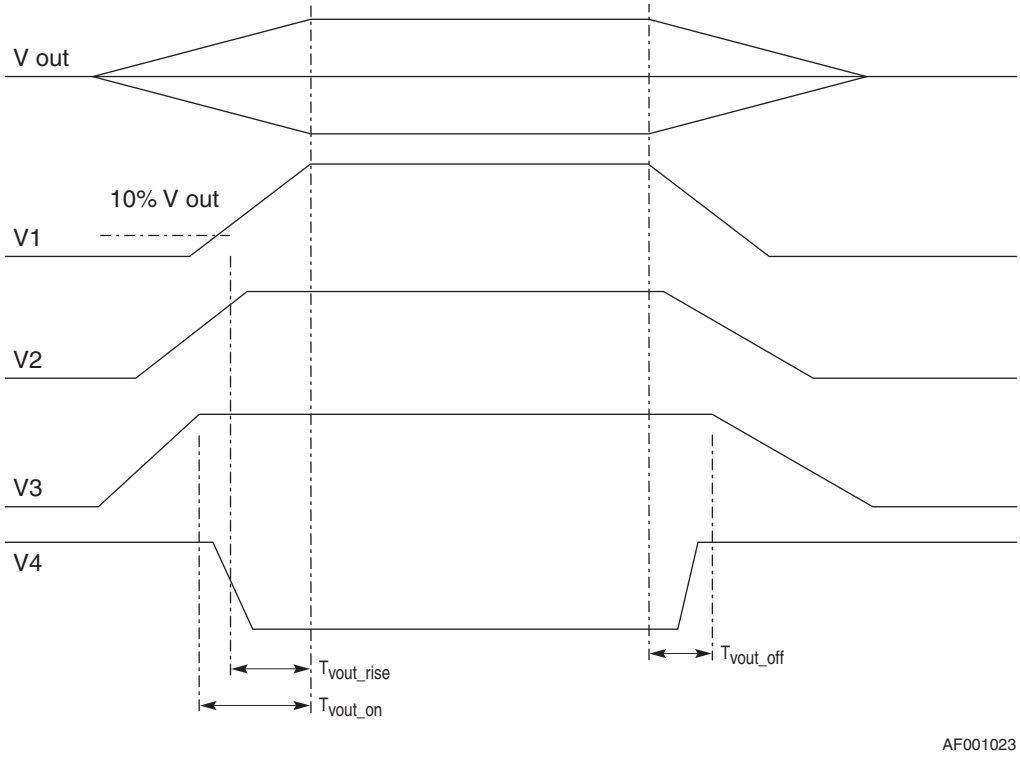


Figure 21. Output Voltage Timing

Table 40. Turn On/Off Timing

Item	Description	Minimum	Maximum	Units
$T_{sb\_on\_delay}$	Delay from AC applied to 5VSB within regulation.		1500	msec
$T_{ac\_on\_delay}$	Delay from AC applied to all output voltages within regulation.		2500	msec
T_{vout_holdup}	Time all output voltages stay within regulation after loss of AC. Measured at 75% of maximum load.	21		msec
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK. Measured at 75% of maximum load.	20		msec
$T_{pson\_on\_delay}$	Delay from PSOn# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSOn# deactive to PWOK being de-asserted.		50	msec

Item	Description	Minimum	Maximum	Units
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	msec
T_{pwok_off}	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		msec
T_{pwok_low}	Duration of PWOK in the de-asserted state during an off/on cycle using AC or the PSOn signal.	100		msec
T_{sb_vout}	Delay from 5VSB in regulation to O/Ps in regulation at AC turn on.	50	1000	msec
T_{5VSB_holdup}	Time the 5VSB output voltage stays within regulation after loss of AC.	70		msec

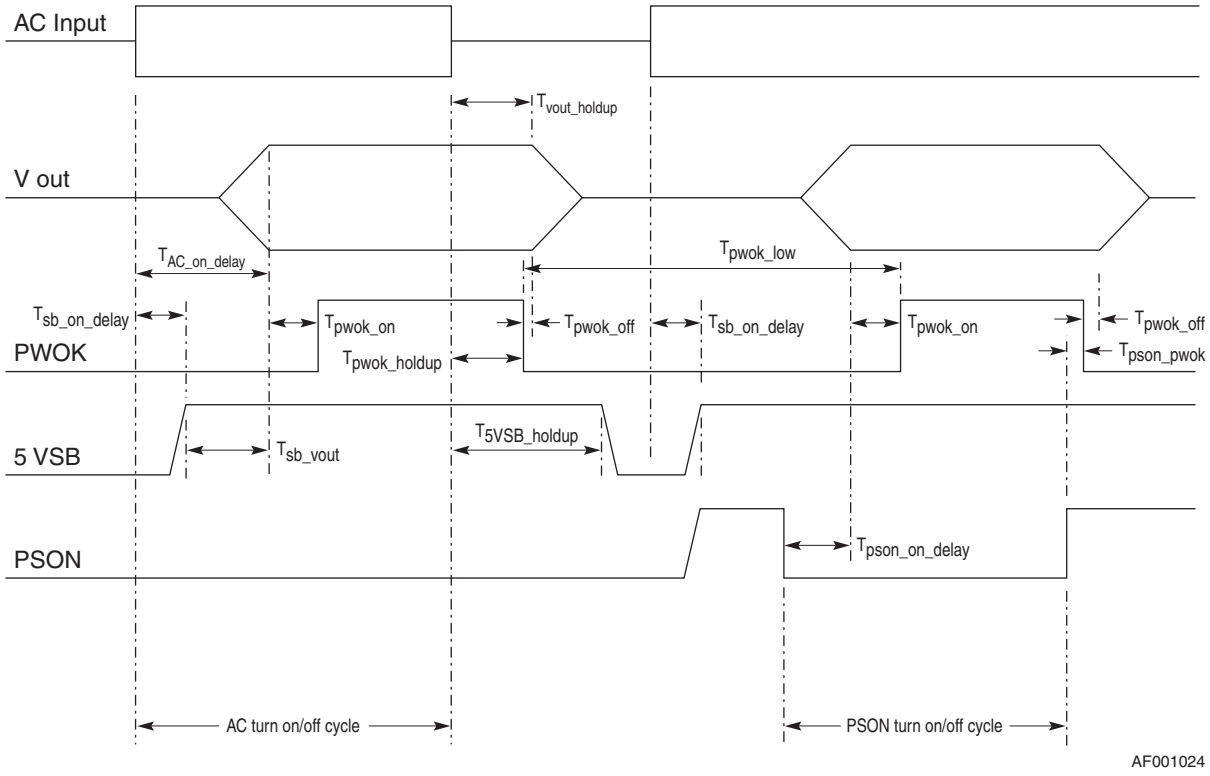


Figure 22. Turn On/Off Timing (Power Supply Signals)

8.2.14 Residual Voltage Immunity in Standby Mode

The power supply should be immune to any residual voltage placed on the outputs (typically a leakage voltage through the system from standby output) up to 500 mV. There should be no additional heat generated, or stress of any internal components with this voltage applied to any individual output or all outputs simultaneously. It should not trip the power supply protection circuits during turn on.

Residual voltage at the power supply outputs for a no load condition should not exceed 100 mV when AC voltage is applied and the PSOn# signal is de-asserted.

9. Regulatory and Certification Information

⚠ WARNING
To ensure regulatory compliance, you must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products / components will void the UL listing and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in the region(s) in which the product is sold.

To help ensure EMC compliance with your local regional rules and regulations, before computer integration, make sure that the chassis, power supply, and other modules have passed EMC testing using a server board with a microprocessor from the same family (or higher) and operating at the same (or higher) speed as the microprocessor used on this server board. The final configuration of your end system product may require additional EMC compliance testing. For more information please contact your local Intel Representative.

This is an FCC Class A device. Integration of it into a Class B chassis does not result in a Class B device.

9.1 Product Regulatory Compliance

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation. This is an FCC Class A device. Integration of it into a Class B chassis does not result in a Class B device.

Note: The use and/or integration of telecommunication devices such as modems and/or wireless devices have not been planned for with respect to these systems. If there is any change of plan to use such devices, then telecommunication type certifications will require additional planning. If NEBS compliance is required for system level products, additional certification planning and design will be required.

9.1.1 Product Safety Compliance

- UL60950 – CSA 60950 (USA / Canada)
- EN60950 (Europe)
- IEC60950 (International)
- CB Certificate & Report, IEC60950 (report to include all country national deviations)
- BSMI Declaration of Conformity (Taiwan)
- Belarus License – Listed on System License (Belarus)
- UL 60950 Recognition (USA)

9.1.2 Product EMC Compliance – Class A Compliance

Note: *This product requires complying with Class A EMC requirements. However, Intel targets a 10 db margin to support customer enablement.*

- CISPR 22 – Emissions (International)
- EN55022 - Emissions (Europe)
- EN55024 - Immunity (Europe)
- CE – EMC Directive 89/336/EEC (Europe)
- FCC – Part 15 Emissions (USA) Verification
- AS/NZS 3548 Emissions (Australia / New Zealand)
- BSMI CNS13438 Emissions (Taiwan)
- RRL MIC Notice No. 1997-41 (EMC) & 1997-42 (EMI) (Korea)

IMPORTANT NOTE:

The host system with the Server Board S5500BC requires the use of shielded LAN cable to comply with Immunity regulatory requirements. Use of non-shield cables may result in the product having insufficient protection against electromagnetic effects, which may cause improper operation of the product.

9.1.3 Certifications / Registrations / Declarations

- UL Certification (US/Canada)
- CE Declaration of Conformity (CENELEC Europe)
- FCC/ICES-003 Class A Attestation (USA/Canada)
- C-Tick Declaration of Conformity (Australia)
- MED Declaration of Conformity (New Zealand)
- BSMI Declaration (Taiwan)
- RRL Certification (Korea)
- GOST – Listed on one System License (Russia)
- Belarus – Listed on one System License (Belarus)
- Ecology Declaration (International)

9.1.4 Product Ecology Requirements

Intel restricts the use of banned substances in accordance with world wide product ecology regulatory requirements. Suppliers Declarations of Conformity to the banned substances must be obtained from all suppliers; and a Material Declaration Data Sheet (MDDS) must be produced to illustrate compliance. Due verification of random materials is required as a screening / audit to verify suppliers declarations.

The server board complies with the following ecology regulatory requirements:

- All materials, parts, and subassemblies must not contain restricted materials as defined in Intel's Environmental Product Content Specification of Suppliers and Outsourced Manufacturers – http://supplier.intel.com/ehs/environmental.htm.
- Europe - European Directive 2002/95/EC - Restriction of Hazardous Substances (RoHS) Threshold limits and banned substances are noted below.

  Quantity limit of 0.1% by mass (1000 PPM) for Lead, Mercury, Hexavalent Chromium, Polybrominated Biphenyls Diphenyl Ethers (PBB/PBDE)

  Quantity limit of 0.01% by mass (100 PPM) for Cadmium
- China RoHS
- All plastic parts that weigh >25gm shall be marked with the ISO11469 requirements for recycling. Example >PC/ABS<
- EU Packaging Directive
- CA. Lithium Perchlorate insert Perchlorate Material – Special handling may apply. Refer to http://www.dtsc.ca.gov/hazardouswaste/perchlorate.
  This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product / part includes a battery which contains Perchlorate material.
- German Green Dot
- Japan Recycling

9.2 Product Regulatory Compliance Markings

The server board is provided with the following regulatory marks.

Regulatory Compliance	Region	Marking
UL Mark	USA/Canada	c UL us E139761
CE Mark	Europe	CE
EMC Marking (Class A)	Canada	CANADA ICES-003 CLASS A
BSMI Marking (Class A)	Taiwan	D33025 警告使用者： 這是甲類的資訊產品，在居住的環境中使用時，可能會造成射頻干擾，在這種情況下，使用者會被要求採取某些適當的對策
C-tick Marking	Australia / New Zealand	N232
RRL MIC Mark	Korea	MIC 인증번호: CPU-Model Name (A)
Country of Origin	Exporting Requirements	MADE IN xxxxx (Provided by label, not silk screen)
Model Designation	Regulatory Identification	Examples (Intel® Server Board S5500BC) for boxed type boards; or Board PB number for non-boxed boards (typically high-end boards)
PB Free Marking?	Environmental Requirements	Pb 2nd lvl intct e1 *Refer to the spec* *http://prodregs.intel.com/ProductCertifications/Servers/GG-1035%20spec%20Rev%2002.pdf*
China RoHS Marking	China	20

Regulatory Compliance	Region	Marking
China Recycling Package Marking (Marked on packaging label)	China	
Other Recycling Package Marking (Marked on packaging label)	Other Recycling Package Marks	
Other Recycling Package Marking (Marked on packaging label)	CA. Lithium Perchlorate insert	Perchlorate Material – Special handling may apply. See www.dtsc.ca.gov/hazardouswaste/perchlorate This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product / part includes a battery which contains Perchlorate material.

9.3 Electromagnetic Compatibility Notices

9.3.1 FCC Verification Statement (USA)

This device complies with Part 15 of the FCC Rules. Operation is subject to two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124-6497
Phone: 1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of these measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded may result in interference to radio and TV reception.

9.3.2 ICES-003 (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe B prescrites dans la norme sur le matériel brouilleur: “Appareils Numériques”, NMB-003 édictée par le Ministre Canadian des Communications.

English translation of the notice above:
This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled “Digital Apparatus,” ICES-003 of the Canadian Department of Communications.

9.3.3 Europe (CE Declaration of Conformity)

This product has been tested in accordance too, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

9.3.4 VCCI (Japan)

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＢ情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
取扱説明書に従って正しい取り扱いをして下さい。

English translation of the notice above:
This is a Class B product based on the standard of the Voluntary Control Council for Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

9.3.5 BSMI (Taiwan)

The BSMI Certification Marking and EMC warning is located on the outside rear area of the product.

警告使用者：
這是甲類的資訊產品，在居住的環境中使用時，
可能會造成射頻干擾，在這種情況下，使用者會
被要求採取某些適當的對策

9.3.6 RRL (Korea)

Following is the RRL certification information for Korea.

1. 기기의 명칭(모델명) :
2. 인증번호 :
3. 인증받은 자의 상호 :
4. 제조년월일:
5. 제조자/제조국가 :

English translation of the notice above:

1. Type of Equipment (Model Name): On License and Product
2. Certification No.: On RRL certificate. Obtain certificate from local Intel representative
3. Name of Certification Recipient: Intel Corporation
4. Date of Manufacturer: Refer to date code on product
5. Manufacturer/Nation: Intel Corporation/Refer to country of origin marked on product

9.3.7 CNCA (CCC-China)

The CCC Certification Marking and EMC warning is located on the outside rear area of the product.

声明

此为A级产品，在生活环境中，该产品可能会造成无线电干扰。在这种情况下，可能需要用户对其干扰采取可行的措施。

Appendix A: Integration and Usage Tips

- When adding or removing components or peripherals from the server board, you must remove AC power. With AC power plugged into the server board, 5-volt standby is still present even though the server board is powered off.
- Only " Intel® Xeon® processor 5500 series" with 95 W and less Thermal Design Power (TDP) are supported on this server board. Previous generation Intel® Xeon® processors are not supported. "Intel® Xeon® processor 5500 series" with TDP higher than 95 W are not supported.
- Processors must be installed in order. CPU 1 is located near the edge of the server board and must be populated to operate the board.
- On the back edge of the server board are eight diagnostic LEDs that display a sequence of amber POST codes during the boot process. If the server board hangs during POST, the LEDs display the last POST event run before the hang.
- Only registered DDR3 DIMMs (RDIMMs) and unbuffered DDR3 DIMMs (UDIMMs) are supported on this server board. Mixing of RDIMMs and UDIMMs is not supported.
- For the best performance, the number of DDR3 DIMMs installed should be balanced across both processor sockets and memory channels. For example: a Two-DIMM configuration will perform better than a One-DIMM configuration. In a Two-DIMM configuration, DIMMs should be installed in DIMM sockets A1 and D1. An Eight-DIMM configuration (DIMM sockets A1, B1, A2, B2, D1, D2, E1, and E2) will perform better than a Four-DIMM configuration (DIMM Sockets A1, B1, A2, and B2).
- The Intel® RMM3 connector is not compatible with the Intel® Remote Management Module (Product Code AXXRMM3) or with the Intel® Remote Management Module 2 (Product Code AXXRMM2).
- Clear COMS with AC power cord plugged. Removing AC power before performing the CMOS clear operation will cause the system to automatically power up and immediately power down after the CMOS clear procedure is followed and AC power is re-applied. If this happens, remove the AC power cord, wait 30 seconds, and then re-connect the AC power cord. Power up the system and proceed to the <F2> BIOS setup utility to reset the desired settings.
- Normal BMC functionality is disabled with the force BMC update jumper (J8C1) set to the "enabled" position (pins 2-3). The server should never be run with the BMC force update jumper set in this position and should only be used when the standard firmware update process fails. This jumper should remain in the default (disabled) position (pins 1-2) when the server is running normally.
- This server board no longer supports rolling BIOS (two BIOS banks) and implements a BIOS recovery mechanism instead.
- When performing normal a BIOS update procedure, the BIOS recovery jumper (J1A1) must be set to its default position (pins 1-2).

Appendix B: Sensor Tables

This appendix lists the sensor identification numbers and information regarding the sensor type, name, supported thresholds, assertion and de-assertion information, and a brief description of the sensor purpose. See the *Intelligent Platform Management Interface Specification, Version 2.0*, for sensor and event/reading-type table information.

- **Sensor Type**

  The sensor type references the values in the sensor type codes table in the Intelligent Platform Management Interface Specification Second Generation v2.0. It provides the context to interpret the sensor.

- **Event / Reading Type**

  The event / reading type references values from the event / reading type code ranges and the generic event / reading type code tables in the Intelligent Platform Management Interface Specification Second Generation v2.0. Digital sensors are a specific type of discrete sensors that only have two states.

- **Event Thresholds / Triggers**

  The following event thresholds are supported for threshold type sensors.

[u,l][nr,c,nc]	upper non-recoverable, upper critical, upper non-critical, lower non-recoverable, lower critical, lower non-critical
uc, lc	upper critical, lower critical

  Event triggers are supported, event-generating offsets for discrete type sensors. You can find the offsets in the generic event / reading type code or sensor type code tables in the Intelligent Platform Management Interface Specification Second Generation v2.0, depending on whether the sensor event / reading type is generic or a sensor-specific response.

- **Assertion / De-assertion Enables**

  Assertion and de-assertion indicators reveal the type of events the sensor can generate:

  As: Assertions

  De: De-assertion

- **Readable Value / Offsets**

  Readable Value indicates the type of value returned for threshold and other non-discrete type sensors.

  Readable Offsets indicate the offsets for discrete sensors that are readable via the Get Sensor Reading command. Unless otherwise indicated, all event triggers are readable (for example, Readable Offsets consists of the reading type offsets that do not generate events).

- **Event Data**

  This is the data included in an event message generated by the associated sensor. For threshold-based sensors, these abbreviations are used:

  R: Reading value

  T: Threshold value

- **Rearm Sensors**

  The rearm is a request for the event status for a sensor to be rechecked and updated upon a transition between good and bad states. Rearming the sensors can be done manually or automatically. This column indicates the type supported by the sensor. The following abbreviations are used in the comment column to describe a sensor:

  A: Auto-rearm

  M: Manual rearm

  I: Rearm by init agent

- **Default Hysteresis**

  Hysteresis setting applies to all thresholds of the sensor. This column provides the count of hysteresis for the sensor, which can be 1 or 2 (positive or negative hysteresis).

- **Criticality**

  Criticality is a classification of the severity and nature of the condition. It also controls the behavior of the Control Panel Status LED.

- **Standby**

  Some sensors operate on standby power. These sensors may be accessed and / or generate events when the main (system) power is off, but AC power is present.

Table 41. Integrated BMC Core Sensors

Full Sensor Name *(Sensor name in SDR)*	Sensor #	Platform Applicability	Sensor Type	Event / Reading Type	Event Offset Triggers	Contrib. To System Status	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Stand-by
Power Unit Status *(Pwr Unit Status)*	01h	All	Power Unit 09h	Sensor Specific 6Fh	00 - Power down 04 - A/C lost	OK	As and De	–	Trig Offset	A	X
					05 - Soft power control failure 06 - Power unit failure	Fatal					
Power Unit Redundancy[1] *(Pwr Unit Redund)*	02h	Chassis-specific	Power Unit 09h	Generic 0Bh	00 - Fully Redundant	OK	As and De	–	Trig Offset	A	X
					01 - Redundancy lost	Degraded					
					02 - Redundancy degraded	Degraded					
					03 - Non-redundant: sufficient resources. Transition from full redundant state.	Degraded					
					04 – Non-redundant: sufficient resources. Transition from insufficient state.	Degraded					
					05 - Non-redundant: insufficient resources	Fatal					
					06 – Redundant: degraded from fully redundant state.	Degraded					

Full Sensor Name *(Sensor name in SDR)*	Sensor #	Platform Applicability	Sensor Type	Event / Reading Type	Event Offset Triggers	Contrib. To System Status	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Stand-by
					07 – Redundant: Transition from non-redundant state.	Degraded					
IPMI Watchdog *(IPMI Watchdog)*	03h	All	Watchdog 2 23h	Sensor Specific 6Fh	00 - Timer expired, status only 01 - Hard reset 02 - Power down 03 - Power cycle 08 - Timer interrupt	OK	As	–	Trig Offset	A	X
Physical Security *(Physical Scrty)*	04h	Chassis Intrusion is chassis-specific	Physical Security 05h	Sensor Specific 6Fh	00 - Chassis intrusion	OK	As and De	–	Trig Offset	A	X
					04 - LAN leash lost	OK					
FP Interrupt *(FP NMI Diag Int)*	05h	Chassis - specific	Critical Interrupt 13h	Sensor Specific 6Fh	00 - Front panel NMI / diagnostic interrupt	OK	As	–	Trig Offset	A	–
SMI Timeout *(SMI Timeout)*	06h	All	SMI Timeout F3h	Digital Discrete 03h	01 – State asserted	Fatal	As and De	–	Trig Offset	A	–
System Event Log *(System Event Log)*	07h	All	Event Logging Disabled 10h	Sensor Specific 6Fh	02 - Log area reset / cleared	OK	As	–	Trig Offset	A	X
System Event *(System Event)*	08h	All	System Event 12h	Sensor Specific 6Fh	04 – PEF action	OK	As	-	Trig Offset	A,I	X
BB +1.1V IOH *(BB +1.1V IOH)*	10h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–

Full Sensor Name *(Sensor name in SDR)*	Sensor #	Platform Applicability	Sensor Type	Event / Reading Type	Event Offset Triggers	Contrib. To System Status	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Stand-by
BB +1.1V P1 Vccp *(BB +1.1V P1 Vccp)*	11h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
BB +1.1V P2 Vccp *(BB +1.1V P2 Vccp)*	12h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
BB +1.5V P1 DDR3 *(BB +1.5V P1 DDR3)*	13h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
BB +1.5V P2 DDR3 *(BB +1.5V P2 DDR3)*	14h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
BB +1.8V AUX *(BB +1.8V AUX)*	15h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
BB +3.3V *(BB +3.3V)*	16h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
BB +3.3V STBY *(BB +3.3V STBY)*	17h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
BB +3.3V Vbat *(BB +3.3V Vbat)*	18h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
BB +5.0V *(BB +5.0V)*	19h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
BB +5.0V STBY *(BB +5.0V STBY)*	1Ah	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
BB +12.0V *(BB +12.0V)*	1Bh	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
BB -12.0V *(BB -12.0V)*	1Ch	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Baseboard Temperature *(Baseboard Temp)*	20h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X

Full Sensor Name *(Sensor name in SDR)*	Sensor #	Platform Applicability	Sensor Type	Event / Reading Type	Event Offset Triggers	Contrib. To System Status	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Stand-by
Front Panel Temperature *(Front Panel Temp)*	21h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
IOH Thermal Margin *(IOH Therm Margin)*	22h	All	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Processor 1 Memory Thermal Margin (Mem P1 Thrm Mrgn)	23h	All	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Processor 2 Memory Thermal Margin (Mem P2 Thrm Mrgn)	24h	Dual processor only	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	–
Fan Tachometer Sensors (Chassis specific sensor names)	30h–39h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	nc = Degraded c = Non-fatal[2]	As and De	Analog	R, T	M	–
Fan Present Sensors *(Fan x Present)*	40h–45h	Chassis-specific	Fan 04h	Generic 08h	01 - Device inserted	OK	As and De	-	Triggered Offset	Auto	–
Fan Redundancy [1] *(Fan Redundancy)*	46h	Chassis-specific	Fan 04h	Generic 0Bh	00 - Fully redundant	OK	As and De	–	Trig Offset	A	
					01 - Redundancy lost	Degraded					
					02 - Redundancy degraded	Degraded					
					03 - Non-redundant: Sufficient resources. Transition from redundant	Degraded					

Full Sensor Name *(Sensor name in SDR)*	Sensor #	Platform Applicability	Sensor Type	Event / Reading Type	Event Offset Triggers	Contrib. To System Status	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Stand-by
					04 - Non-redundant: Sufficient resources. Transition from insufficient.	Degraded					–
					05 - Non-redundant: insufficient resources.	Non-fatal					
					06 – Non-Redundant: degraded from fully redundant.	Degraded					
					07 - Redundant degraded from non-redundant	Degraded					
					07 - Redundant degrade from non-redundant	Degraded					
Power Supply 1 Status *(PS/1 Status)*	50h	Chassis-specific	Power Supply 08h	Sensor Specific 6Fh	00 - Presence	OK	As and De	–	Trig Offset	A	X
					01 - Failure	Degraded					
					02 – Predictive Failure	Degraded					
					03 - A/C lost	Degraded					
					06 – Configuration error	OK					
Power Supply 2 Status *(PS/2 Status)*	51h	Chassis-specific	Power Supply 08h	Sensor Specific 6Fh	00 - Presence	OK	As and De	–	Trig Offset	A	X
					01 - Failure	Degraded					

Full Sensor Name *(Sensor name in SDR)*	Sensor #	Platform Applicability	Sensor Type	Event / Reading Type	Event Offset Triggers	Contrib. To System Status	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Stand-by
					02 – Predictive Failure	Degraded					
					03 - A/C lost	Degraded					
					06 – Configuration error	OK					
Power Supply 1 AC Power Input (PS/1 Power In)	52h	Chassis-specific	Other Units 0Bh	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 2 AC Power Input (PS/2 Power In)	53h	Chassis-specific	Other Units 0Bh	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 1 +12V % of Maximum Current Output (*PS/1 Curr Out %*)	54h	Chassis-specific	Current 03h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 2 +12V % of Maximum Current Output (*PS/2 Curr Out %*)	55h	Chassis-specific	Current 03h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 1 Temperature (*PS/1 Temperature*)	56h	Chassis-specific	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Power Supply 2 Temperature (*PS/2 Temperature*)	57h	Chassis-specific	Temperature	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	R, T	A	X
Processor 1 Status *(P1 Status)*	60h	All	Processor 07h	Sensor Specific 6Fh	01 - Thermal trip	Fatal	As and De	–	Trig Offset	M	X
					07 - Presence	OK					
Processor 2 Status *(P2 Status)*	61h	Dual processor only	Processor 07h	Sensor Specific 6Fh	01- Thermal trip	Fatal	As and De	–	Trig Offset	M	X
					07 - Presence	OK					
Processor 1 Thermal Margin (*P1 Therm Margin*)	62h	All	Temperature 01h	Threshold 01h	–	–	–	Analog	–	–	–

Full Sensor Name *(Sensor name in SDR)*	Sensor #	Platform Applicability	Sensor Type	Event / Reading Type	Event Offset Triggers	Contrib. To System Status	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Stand-by
Processor 2 Thermal Margin (*P2 Therm Margin*)	63h	Dual processor only	Temperature 01h	Threshold 01h	–	–	–	Analog	–	–	–
Processor 1 Thermal Control % (*P1 Therm Ctrl %*)	64h	All	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	Trig Offset	A	–
Processor 2 Thermal Control % (*P2 Therm Ctrl %*)	65h	Dual processor only	Temperature 01h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-fatal	As and De	Analog	Trig Offset	A	–
Processor 1 VRD Temp (*P1 VRD Hot*)	66h	All	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Fatal	As and De	–	Trig Offset	M	–
Processor 2 VRD Temp (*P2 VRD Hot*)	67h	Dual processor only	Temperature 01h	Digital Discrete 05h	01 - Limit exceeded	Fatal	As and De	–	Trig Offset	M	–
Catastrophic Error *(CATERR)*	68h	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	Non-fatal	As and De	–	Trig Offset	M	–
CPU Missing *(CPU Missing)*	69h	All	Processor 07h	Digital Discrete 03h	01 – State Asserted	Fatal	As and De	–	Trig Offset	M	–
IOH Thermal Trip *(IOH Thermal Trip)*	6Ah	All	Temperature 01h	Digital Discrete 03h	01 – State Asserted	Fatal	As and De	–	Trig Offset	M	–

Appendix C: POST Error Messages and Handling

Whenever possible, the BIOS outputs the current boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware that is being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The Response section in the following table is divided into three types:

- **Minor:** The message displays on the screen or in the Error Manager screen. The system continues booting with a degraded state. The user may want to replace the erroneous unit. The setup POST error Pause setting does not have any effect with this error.
- **Major:** The message is displayed in the Error Manager screen and an error is logged to the SEL. The setup POST error Pause setting determines whether the system pauses to the Error Manager for this type of error where the user can take immediate corrective action or choose to continue booting.
- **Fatal:** The message is displayed in the Error Manager screen, an error is logged to the SEL, and the system cannot boot unless the error is resolved. The user must replace the faulty part and restart the system. The setup POST error Pause setting does not have any effect with this error.

Table 42. POST Error Messages and Handling

Error Code	Error Message	Response
0012	CMOS date / time not set	Major
0048	Password check failed	Major
0108	Keyboard component encountered a locked error.	Minor
0109	Keyboard component encountered a stuck key error.	Minor
0113	Fixed Media The SAS RAID firmware can not run properly. The user should attempt to reflash the firmware.	Major
0140	PCI component encountered a PERR error.	Major
0141	PCI resource conflict	Major
0146	PCI out of resources error	Major
0192	L3 cache size mismatch	Fatal
0194	CPUID, processor family are different	Fatal
0195	Front side bus mismatch	Major
0196	Processor Model mismatch	Major
0197	Processor speeds mismatched	Major
0198	Processor family is unsupported.	Major
019F	Processor and chipset stepping configuration is unsupported.	Major
5220	CMOS/NVRAM Configuration Cleared	Major
5221	Passwords cleared by jumper	Major
5224	Password clear Jumper is Set.	Major

Error Code	Error Message	Response
8180	Processor 01 BIOS does not support the current stepping for processor	Minor
8181	Processor 02 BIOS does not support the current stepping for processor	Minor
8190	Watchdog timer failed on last boot	Major
8198	Operating system boot watchdog timer expired on last boot	Major
8300	Baseboard management controller failed self-test	Major
84F2	Baseboard management controller failed to respond	Major
84F3	Baseboard management controller in update mode	Major
84F4	Sensor data record empty	Major
84FF	System event log full	Minor
8500	Memory component could not be configured in the selected RAS mode.	Major
8520	DIMM_A1 failed Self Test (BIST).	Major
8521	DIMM_A2 failed Self Test (BIST).	Major
8522	DIMM_A3 failed Self Test (BIST).	Major
8524	DIMM_B1 failed Self Test (BIST).	Major
8525	DIMM_B2 failed Self Test (BIST).	Major
8526	DIMM_B3 failed Self Test (BIST).	Major
8528	DIMM_C1 failed Self Test (BIST).	Major
8529	DIMM_C2 failed Self Test (BIST).	Major
852A	DIMM_C3 failed Self Test (BIST).	Major
852C	DIMM_D1 failed Self Test (BIST).	Major
852D	DIMM_D2 failed Self Test (BIST).	Major
852E	DIMM_D3 failed Self Test (BIST).	Major
8540	DIMM_A1 Disabled.	Major
8541	DIMM_A2 Disabled.	Major
8542	DIMM_A3 Disabled.	Major
8544	DIMM_B1 Disabled.	Major
8545	DIMM_B2 Disabled.	Major
8546	DIMM_B3 Disabled.	Major
8548	DIMM_C1 Disabled.	Major
8549	DIMM_C2 Disabled.	Major
854A	DIMM_C3 Disabled.	Major
854C	DIMM_D1 Disabled.	Major
854D	DIMM_D2 Disabled.	Major
854E	DIMM_D3 Disabled.	Major
8560	DIMM_A1 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8561	DIMM_A2 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8562	DIMM_A3 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8564	DIMM_B1 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8565	DIMM_B2 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8566	DIMM_B3 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8568	DIMM_C1 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8569	DIMM_C2 Component encountered a Serial Presence Detection (SPD) fail error.	Major
856A	DIMM_C3 Component encountered a Serial Presence Detection (SPD) fail error.	Major
856C	DIMM_D1 Component encountered a Serial Presence Detection (SPD) fail error.	Major

Error Code	Error Message	Response
856D	DIMM_D2 Component encountered a Serial Presence Detection (SPD) fail error.	Major
856E	DIMM_D3 Component encountered a Serial Presence Detection (SPD) fail error.	Major
8580	DIMM_A1 Correctable ECC error encountered.	Minor/Major after 10
8581	DIMM_A2 Correctable ECC error encountered.	Minor/Major after 10
8582	DIMM_A3 Correctable ECC error encountered.	Minor/Major after 10
8584	DIMM_B1 Correctable ECC error encountered.	Minor/Major after 10
8585	DIMM_B2 Correctable ECC error encountered.	Minor/Major after 10
8586	DIMM_B3 Correctable ECC error encountered.	Minor/Major after 10
8588	DIMM_C1 Correctable ECC error encountered.	Minor/Major after 10
8589	DIMM_C2 Correctable ECC error encountered.	Minor/Major after 10
858A	DIMM_C3 Correctable ECC error encountered.	Minor/Major after 10
858C	DIMM_D1 Correctable ECC error encountered.	Minor/Major after 10
858D	DIMM_D2 Correctable ECC error encountered.	Minor/Major after 10
858E	DIMM_D3 Correctable ECC error encountered.	Minor/Major after 10
85A0	DIMM_A1 Uncorrectable ECC error encountered.	Major
85A1	DIMM_A2 Uncorrectable ECC error encountered.	Major
85A2	DIMM_A3 Uncorrectable ECC error encountered.	Major
85A4	DIMM_B1 Uncorrectable ECC error encountered.	Major
85A5	DIMM_B2 Uncorrectable ECC error encountered.	Major
85A6	DIMM_B3 Uncorrectable ECC error encountered.	Major
85A8	DIMM_C1 Uncorrectable ECC error encountered.	Major
85A9	DIMM_C2 Uncorrectable ECC error encountered.	Major
85AA	DIMM_C3 Uncorrectable ECC error encountered.	Major
85AC	DIMM_D1 Uncorrectable ECC error encountered.	Major
85AD	DIMM_D2 Uncorrectable ECC error encountered.	Major
85AE	DIMM_D3 Uncorrectable ECC error encountered.	Major
8604	Chipset Reclaim of non critical variables complete.	Minor
9000	Unspecified processor component has encountered a non specific error.	Major
9223	Keyboard component was not detected.	Minor
9226	Keyboard component encountered a controller error.	Minor
9243	Mouse component was not detected.	Minor
9246	Mouse component encountered a controller error.	Minor
9266	Local Console component encountered a controller error.	Minor
9268	Local Console component encountered an output error.	Minor
9269	Local Console component encountered a resource conflict error.	Minor
9286	Remote Console component encountered a controller error.	Minor
9287	Remote Console component encountered an input error.	Minor
9288	Remote Console component encountered an output error.	Minor
92A3	Serial port component was not detected	Major
92A9	Serial port component encountered a resource conflict error	Major
92C6	Serial Port controller error	Minor
92C7	Serial Port component encountered an input error.	Minor
92C8	Serial Port component encountered an output error.	Minor
94C6	LPC component encountered a controller error.	Minor

Error Code	Error Message	Response
94C9	LPC component encountered a resource conflict error.	Major
9506	ATA/ATPI component encountered a controller error.	Minor
95A6	PCI component encountered a controller error.	Minor
95A7	PCI component encountered a read error.	Minor
95A8	PCI component encountered a write error.	Minor
9609	Unspecified software component encountered a start error.	Minor
9641	PEI Core component encountered a load error.	Minor
9667	PEI module component encountered a illegal software state error.	Fatal
9687	DXE core component encountered a illegal software state error.	Fatal
96A7	DXE boot services driver component encountered a illegal software state error.	Fatal
96AB	DXE boot services driver component encountered invalid configuration.	Minor
96E7	SMM driver component encountered a illegal software state error.	Fatal
0xA000	TPM device not detected.	Minor
0xA001	TPM device missing or not responding.	Minor
0xA002	TPM device failure.	Minor
0xA003	TPM device failed self test.	Minor
0xA022	Processor component encountered a mismatch error.	Major
0xA027	Processor component encountered a low voltage error.	Minor
0xA028	Processor component encountered a high voltage error.	Minor
0xA421	PCI component encountered a SERR error.	Fatal
0xA500	ATA/ATPI ATA bus SMART not supported.	Minor
0xA501	ATA/ATPI ATA SMART is disabled.	Minor
0xA5A0	PCI Express component encountered a PERR error.	Minor
0xA5A1	PCI Express component encountered a SERR error.	Fatal
0xA5A4	PCI Express IBIST error.	Major
0xA6A0	DXE boot services driver Not enough memory available to shadow a legacy option ROM.	Minor

The following table lists POST error beep codes. Prior to system Video initialization, the BIOS uses these beep codes to inform users of error conditions. The beep code is followed by a user-visible code on POST Progress LEDs.

Table 43. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
3	Memory error		System halted because a fatal error related to the memory was detected

In the case of POST error(s) listed as Major, the BIOS enters the error manager and waits for the user to press an appropriate key before booting the operating system or entering the BIOS Setup.

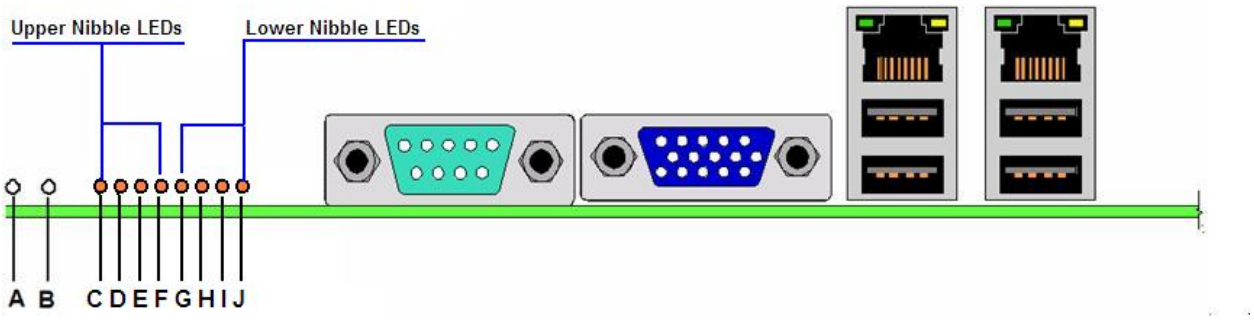
The user can override this option by setting the POST Error Pause option as disabled on the BIOS setup Main screen. If this option is disabled, the system boots the operating system without user intervention. The default is disabled.

Appendix D: POST Code Diagnostic LED Decoder

The BIOS executes platform configuration processes during the system boot. Each process is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the POST code on the POST Code Diagnostic LEDs on the back edge of the server board. The Diagnostic LEDs identify the last POST process to be executed.

Each POST code is represented by the eight amber Diagnostic LEDs. The POST codes are divided into two nibbles, an upper nibble and a lower nibble. The upper nibble bits are represented by Diagnostic LEDs #4, #5, #6, #7. The lower nibble bits are represented by Diagnostics LEDs #0, #1, #2 and #3. Given the bit is set in the upper and lower nibbles, and then the corresponding LED is lit. If the bit is clear, corresponding LED is off.

Diagnostic LED #7 is labeled as “MSB”, and the Diagnostic LED #0 is labeled as “LSB”.



A. ID LED	F. Diagnostic LED #4
B. Status LED	G. Diagnostic LED #3
C. Diagnostic LED #7 (MSB LED)	H. Diagnostic LED #2
D. Diagnostic LED #6	I. Diagnostic LED #1
E. Diagnostic LED #5	J. Diagnostic LED #0 (LSB LED)

Figure 23. Diagnostic LED Placement Diagram

In the following example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

Table 44. POST Progress Code LED Example

	Upper Nibble LEDs				Lower Nibble LEDs			
	MSB							LSB
	LED #7	LED #6	LED #5	LED #4	LED #3	LED #2	LED #1	LED #0
	8h	4h	2h	1h	8h	4h	2h	1h
Status	ON	OFF	ON	OFF	ON	ON	OFF	OFF
	1	0	1	0	1	1	0	0
	Ah				Ch			

Upper nibble bits = 1010b = Ah; Lower nibble bits = 1100b = Ch; the two are concatenated as ACh.

Table 45. Diagnostic LED POST Code Decoder

Checkpoint	Diagnostic LED Decoder O = On, X=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
Host Processor									
0x10h	X	X	X	O	X	X	X	X	Power-on initialization of the host processor (bootstrap processor)
0x11h	X	X	X	O	X	X	X	O	Host processor cache initialization (including AP)
0x12h	X	X	X	O	X	X	O	X	Starting application processor initialization
0x13h	X	X	X	O	X	X	O	O	SMM initialization
Chipset									
0x21h	X	X	O	X	X	X	X	O	Initializing a chipset component
Memory									
0x22h	X	X	O	X	X	X	O	X	Reading configuration data from memory (SPD on DIMM)
0x23h	X	X	O	X	X	X	O	O	Detecting presence of memory
0x24h	X	X	O	X	X	O	X	X	Programming timing parameters in the memory controller
0x25h	X	X	O	X	X	O	X	O	Configuring memory parameters in the memory controller
0x26h	X	X	O	X	X	O	O	X	Optimizing memory controller settings
0x27h	X	X	O	X	X	O	O	O	Initializing memory, such as ECC init
0x28h	X	X	O	X	O	X	X	X	Testing memory
PCI Bus									
0x50h	X	O	X	O	X	X	X	X	Enumerating PCI buses
0x51h	X	O	X	O	X	X	X	O	Allocating resources to PCI buses
0x52h	X	O	X	O	X	X	O	X	Hot Plug PCI controller initialization
0x53h	X	O	X	O	X	X	O	O	Reserved for PCI bus
0x54h	X	O	X	O	X	O	X	X	Reserved for PCI bus
0x55h	X	O	X	O	X	O	X	O	Reserved for PCI bus
0X56h	X	O	X	O	X	O	O	X	Reserved for PCI bus
0x57h	X	O	X	O	X	O	O	O	Reserved for PCI bus
USB									
0x58h	X	O	X	O	O	X	X	X	Resetting USB bus
0x59h	X	O	X	O	O	X	X	O	Reserved for USB devices
ATA/ATAPI/SATA									
0x5Ah	X	O	X	O	O	X	O	X	Resetting SATA bus and all devices
0x5Bh	X	O	X	O	O	X	O	O	Reserved for ATA
SMBUS									
0x5Ch	X	O	X	O	O	O	X	X	Resetting SMBUS
0x5Dh	X	O	X	O	O	O	X	O	Reserved for SMBUS
Local Console									
0x70h	X	O	O	O	X	X	X	X	Resetting the video controller (VGA)
0x71h	X	O	O	O	X	X	X	O	Disabling the video controller (VGA)
0x72h	X	O	O	O	X	X	O	X	Enabling the video controller (VGA)
Remote Console									
0x78h	X	O	O	O	O	X	X	X	Resetting the console controller
0x79h	X	O	O	O	O	X	X	O	Disabling the console controller
0x7Ah	X	O	O	O	O	X	O	X	Enabling the console controller
Keyboard (only USB)									
0x90h	O	X	X	O	X	X	X	X	Resetting the keyboard
0x91h	O	X	X	O	X	X	X	O	Disabling the keyboard
0x92h	O	X	X	O	X	X	O	X	Detecting the presence of the keyboard
0x93h	O	X	X	O	X	X	O	O	Enabling the keyboard
0x94h	O	X	X	O	X	O	X	X	Clearing keyboard input buffer
0x95h	O	X	X	O	X	O	X	O	Instructing keyboard controller to run Self Test(PS/2 only)
Mouse (only USB)									
0x98h	O	X	X	O	O	X	X	X	Resetting the mouse

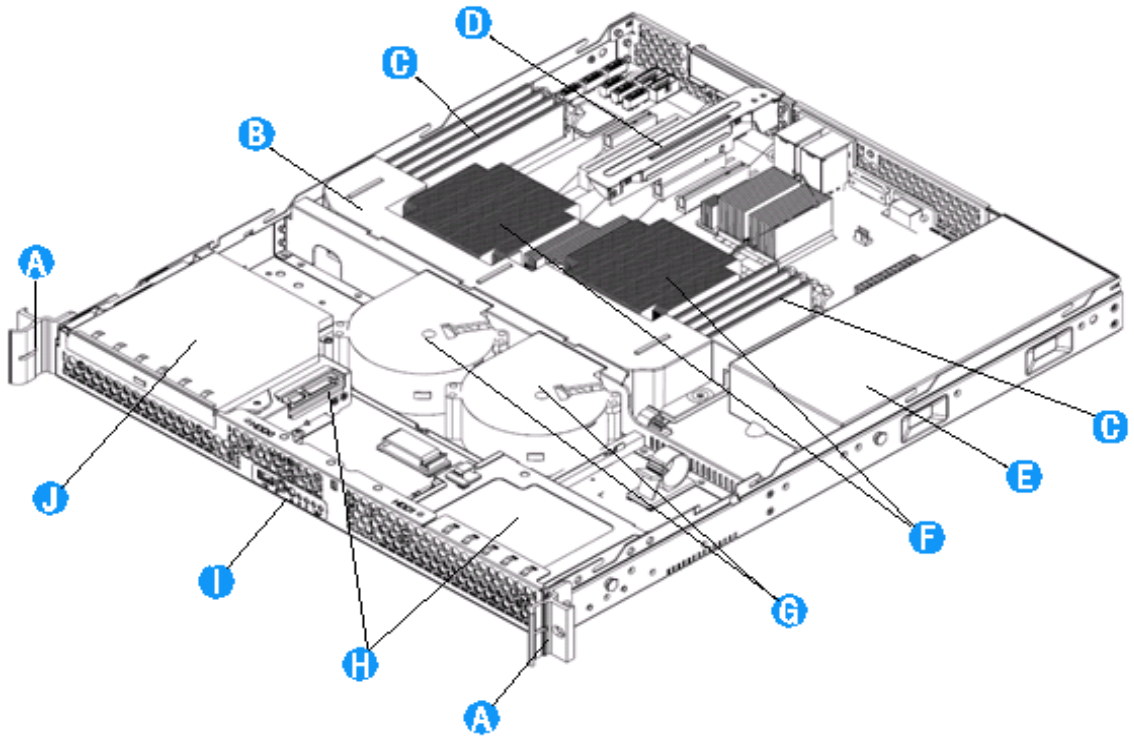
Checkpoint	Diagnostic LED Decoder O = On, X=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
0x99h	O	X	X	O	O	X	X	O	Detecting the mouse
0x9Ah	O	X	X	O	O	X	O	X	Detecting the presence of mouse
0x9Bh	O	X	X	O	O	X	O	O	Enabling the mouse
Fixed Media									
0xB0h	O	X	O	O	X	X	X	X	Resetting fixed media device
0xB1h	O	X	O	O	X	X	X	O	Disabling fixed media device
0xB2h	O	X	O	O	X	X	O	X	Detecting presence of a fixed media device (hard drive detection, and so forth.)
0xB3h	O	X	O	O	X	X	O	O	Enabling / configuring a fixed media device
Removable Media									
0xB8h	O	X	O	O	O	X	X	X	Resetting removable media device
0xB9h	O	X	O	O	O	X	X	O	Disabling removable media device
0xBAh	O	X	O	O	O	X	O	X	Detecting presence of a removable media device (CDROM detection, and so forth.)
0xBCh	O	X	O	O	O	O	X	X	Enabling / configuring a removable media device
Boot Device Selection (BDS)									
0xD0	O	O	X	O	X	X	X	X	Trying to boot device selection 0
0xD1	O	O	X	O	X	X	X	O	Trying to boot device selection 1
0xD2	O	O	X	O	X	X	O	X	Trying to boot device selection 2
0xD3	O	O	X	O	X	X	O	O	Trying to boot device selection 3
0xD4	O	O	X	O	X	O	X	X	Trying to boot device selection 4
0xD5	O	O	X	O	X	O	X	O	Trying to boot device selection 5
0xD6	O	O	X	O	X	O	O	X	Trying to boot device selection 6
0Xd7	O	O	X	O	X	O	O	O	Trying to boot device selection 7
0xD8	O	O	X	O	O	X	X	X	Trying to boot device selection 8
0xD9	O	O	X	O	O	X	X	O	Trying to boot device selection 9
0xDA	O	O	X	O	O	X	O	X	Trying to boot device selection A
0xDB	O	O	X	O	O	X	O	O	Trying to boot device selection B
0xDC	O	O	X	O	O	O	X	X	Trying to boot device selection C
0xDD	O	O	X	O	O	O	X	O	Trying to boot device selection D
0xDE	O	O	X	O	O	O	O	X	Trying to boot device selection E
0xDF	O	O	X	O	O	O	O	O	Trying to boot device selection F
Pre-EFI Initialization (PEI) Core									
0xE0h	O	O	O	X	X	X	X	X	Started dispatching early initialization modules (PEIM)
0xE1h	O	O	O	X	X	X	X	O	Reserved for Initializaiton module use (PEIM)
0xE2h	O	O	O	X	X	X	O	X	Initial memory found, configured, and installed correctly
0xE3h	O	O	O	X	X	X	O	O	Reserved for Initializaiton module use (PEIM)
Driver eXecution Environment (DXE) Core (not accompanied by a beep code)									
0xE4h	O	O	O	X	X	O	X	X	Entered EFI driver execution phase (DXE)
0xE5h	O	O	O	X	X	O	X	O	Started dispatching drivers
0xE6h	O	O	O	X	X	O	O	X	Started connecting drivers
DXE Drivers									
0xE7h	O	O	O	X	O	O	X	O	Waiting for user input
0xE8h	O	O	O	X	O	X	X	X	Checking password
0xE9h	O	O	O	X	O	X	X	O	Entering BIOS setup
0xEAh	O	O	O	X	O	X	O	X	Flash Update
0xEEh	O	O	O	X	O	O	O	X	Calling Int 19. One beep unless silent boot is enabled.
0xEFh	O	O	O	X	O	O	O	O	Unrecoverable boot failure
Runtime Phase / EFI Operating System Boot									
0xF4h	O	O	O	O	X	O	X	X	Entering Sleep state

Checkpoint	Diagnostic LED Decoder O = On, X=Off								Description
	Upper Nibble				Lower Nibble				
	MSB							LSB	
	8h	4h	2h	1h	8h	4h	2h	1h	
LED	#7	#6	#5	#4	#3	#2	#1	#0	
0xF5h	O	O	O	O	X	O	X	O	Exiting Sleep state
0xF8h	O	O	O	O	O	X	X	X	Operating system has requested EFI to close boot services (ExitBootServices ( ) Has been called)
0xF9h	O	O	O	O	O	X	X	O	Operating system has switched to virtual address mode (SetVirtualAddressMap ( ) Has been called)
0xFAh	O	O	O	O	O	X	O	X	Operating system has requested the system to reset (ResetSystem ( ) has been called)
Pre-EFI Initialization Module (PEIM) / Recovery									
0x30h	X	X	O	O	X	X	X	X	Crisis recovery has been initiated because of a user request
0x31h	X	X	O	O	X	X	X	O	Crisis recovery has been initiated by software (corrupt flash)
0x34h	X	X	O	O	X	O	X	X	Loading crisis recovery capsule
0x35h	X	X	O	O	X	O	X	O	Handing off control to the crisis recovery capsule
0x3Fh	X	X	O	O	O	O	O	O	Unable to complete crisis recovery capsule
Memory Error Codes (Accompanied by a beep code)									
0xE8h	O	O	O	X	O	X	X	X	No Usable Memory Error: No memory in the system, or SPD bad so no memory could be detected
0xEBh	O	O	O	X	O	X	O	O	Memory Test Error: memory failed Hardware BIST.
0xEDh	O	O	O	X	O	O	X	O	Population Error: RDIMMs and UDIMMs cannot be mixed in the system
0xEEh	O	O	O	X	O	O	O	X	Mismatch Error: more than 2 Quad Ranked DIMMS in a channel.

Appendix E: Intel® Server System SR1630BC

The Intel® Server System SR1630BC is a 1U server system designed to support the Intel® Server Board S5500BC. The server board and the system have features designed to support the high-density server market.

For more information, refer to the Intel® Server System SR1630BC Technical Product Specification (TPS).



A	Rack handles (two)	F	CPU Heat sink (two)
B	Processor air duct	G	System blower fans (two)
C	System memory DIMM sockets	H	Hard drives (two)
D	PCI add-in card bracket	I	Control panel
E	Power supply	J	Slimline optical drive

Figure 24. 1U Intel® Server System SR1630BC Overview

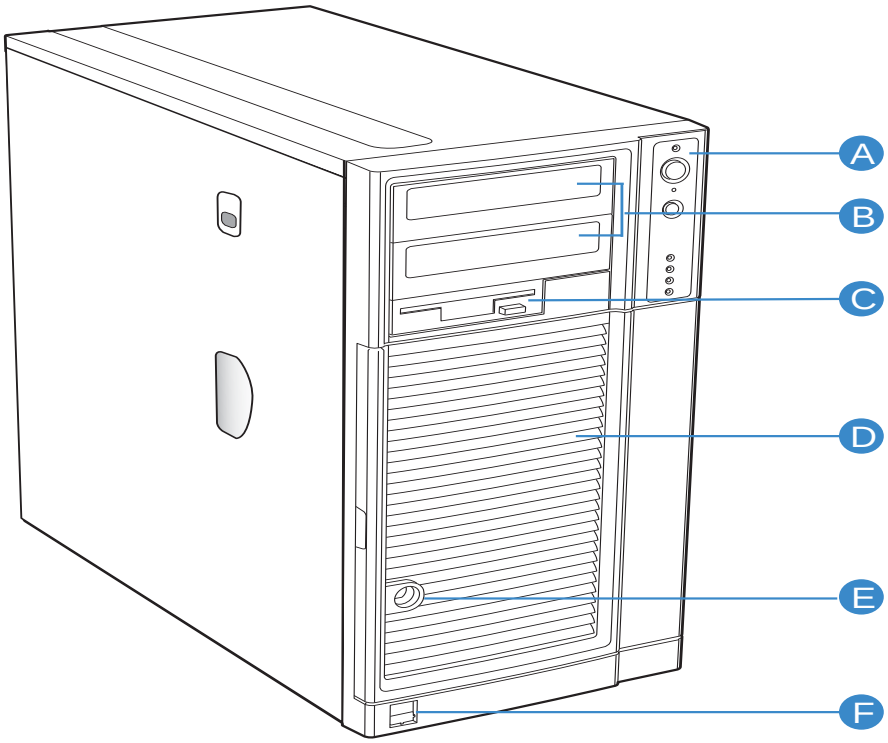
Appendix F: Supported Intel® Server Chassis SC5650

The Intel® Entry Server Chassis SC5650 is a 5.2U pedestal chassis designed to support the Intel® Server Boards S5500BC.

The Intel® Entry Server Chassis SC5650 addresses the value server market with two power factor correction (PFC) power supply unit (PSU) configurations:

- SC5650DP – 600-W fixed PSU for dual-processor server boards
- SC5650BRP – 600-W 1+1 redundant PSU for dual-processor server boards

For more information, see the Intel® Server Chassis SC5650 Technical Product Specification (TPS).



A. Control panel controls and indicators
B. Two half-height 5.25-inch peripheral drive bays
C. 3.5-inch removable media drive bay
D. Internal hard drive bay cage (behind door)
E. Security lock
F. USB ports

Figure 25. 5U Intel® Entry Server Chassis SC5650 Overview

Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ASIC	Application Specific Integrated Circuit
ASMI	Advanced Server Management Interface
BIOS	Basic Input/Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
byte	8-bit quantity
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs, together they bridge the IPMB buses of multiple chassis.
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHCI	Enhanced Host Controller Interface
EMP	Emergency Management Port
EPS	External Product Specification
ESB2	Enterprise South Bridge 2
FBD	Fully Buffered DIMM
FMB	Flexible Mother Board
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GB	1024 MB
GPIO	General Purpose I/O
GTL	Gunning Transceiver Logic
HSC	Hot-Swap Controller
Hz	Hertz (1 cycle/second)
I2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture
IBF	Input Buffer
ICH	I/O Controller Hub
ICMB	Intelligent Chassis Management Bus
IERR	Internal Error
IFB	I/O and Firmware Bridge
INTR	Interrupt
IP	Internet Protocol

Term	Definition
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
ITP	In-Target Probe
KB	1024 bytes
KCS	Keyboard Controller Style
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB	1024 KB
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
ms	Milliseconds
MTTR	Memory Type Range Register
Mux	Multiplexor
NIC	Network Interface Controller
NMI	Nonmaskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm	Unit of electrical resistance
PEF	Platform Event Filtering
PEP	Platform Event Paging
PIA	Platform Information Area (This feature configures the firmware for the platform hardware)
PLD	Programmable Logic Device
PMI	Platform Management Interrupt
POST	Power-On Self Test
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
RAM	Random Access Memory
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board)
SDR	Sensor Data Record
SECC	Single Edge Connector Cartridge
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory
SEL	System Event Log
SIO	Server Input/Output
SMI	Server Management Interrupt (SMI is the highest priority nonmaskable interrupt)
SMM	Server Management Mode

Term	Definition
SNMP	Simple Network Management Protocol
TBD	To Be Determined
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
UTC	Coordinated Universal Time
VID	Voltage Identification
VRD	Voltage Regulator Down
Word	16-bit quantity
ZIF	Zero Insertion Force

Reference Documents

- Intel® S5500 Chipsets Server Board BIOS External Product Specification
- Intel® S5500 Chipsets Server Board Baseboard Management Controller Core External Product Specification
- Intel® Remote Management Module 2 Technical Product Specification
- Intelligent Platform Management Interface (IPMI) 2.0 Specification
- Intel® S5500 Chipset I/O Hub (IOH) 36D/24D External Design Specification
- Intel® Xeon® Processor 5500 Series and LGA1366 Socket Thermal/Mechanical Design Guide
- Intel® Xeon® Processor 5500 Series External Design Specification
- Intel® Xeon® Processor 5500 Series Electrical, Mechanical, and Thermal Specifications
- Intel® Virtualization Technology for Directed I/O Architecture Specification
- Intel® I/O Controller Hub 9 (ICH9) Family Datasheet
- Intel® I/O Controller Hub 10 (ICH10) Family EDS Specification Update
- Intel® Server Chassis SC5650 Technical Product Specification
- Intel® Server System SR1630BC Technical Product Specification