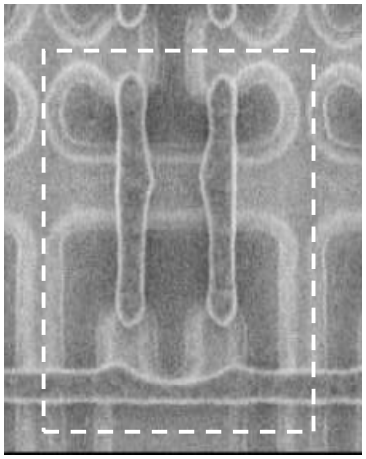
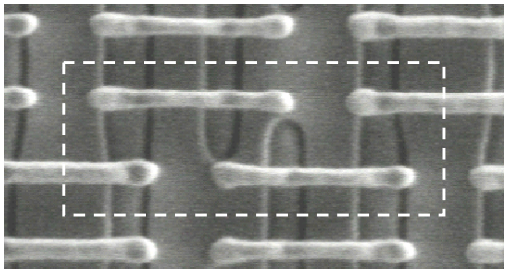
Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond

Kelin J. Kuhn
Intel Fellow
Director of Advanced Device Technology
Portland Technology Development
Intel Corporation

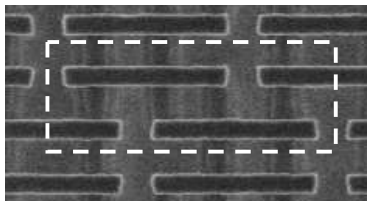
Consistent 2-year scaling



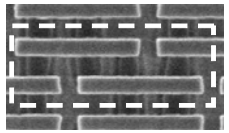
90nm – TALL
1.0 μm²



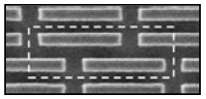
65nm – WIDE - 0.57 μm²



45nm – WIDE
0.346 μm²

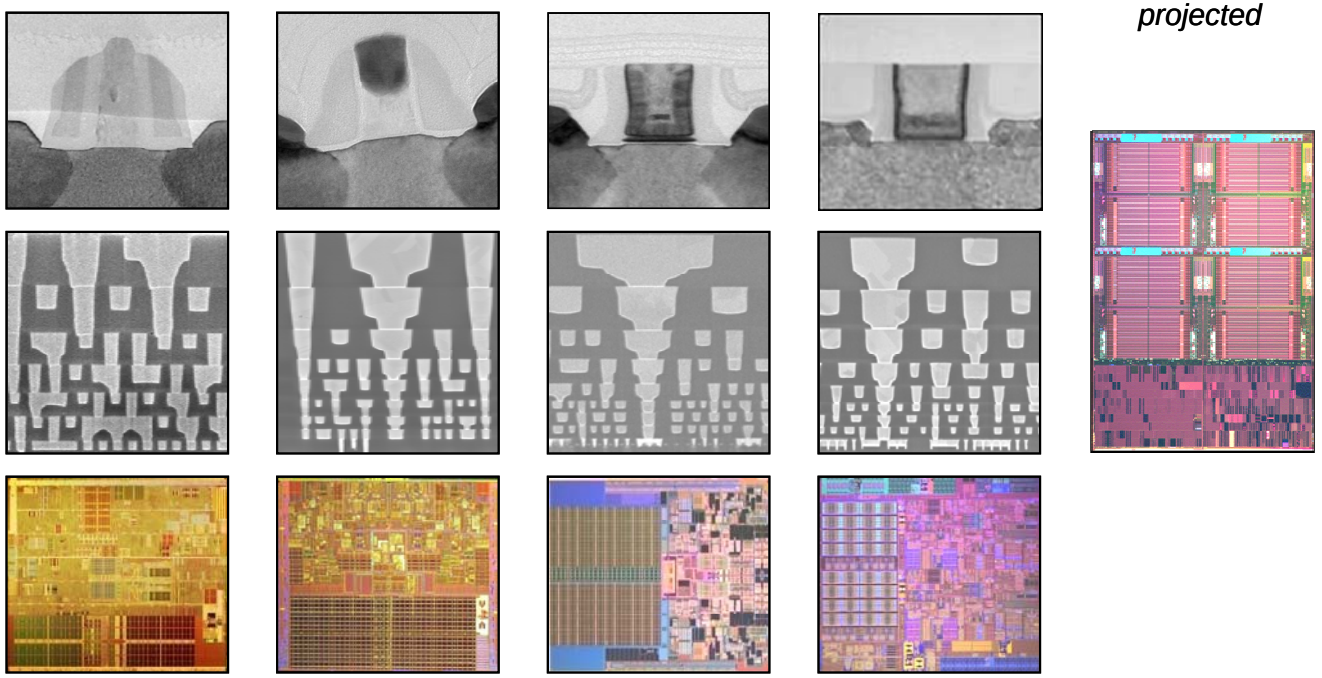


32nm – WIDE
0.171 μm²



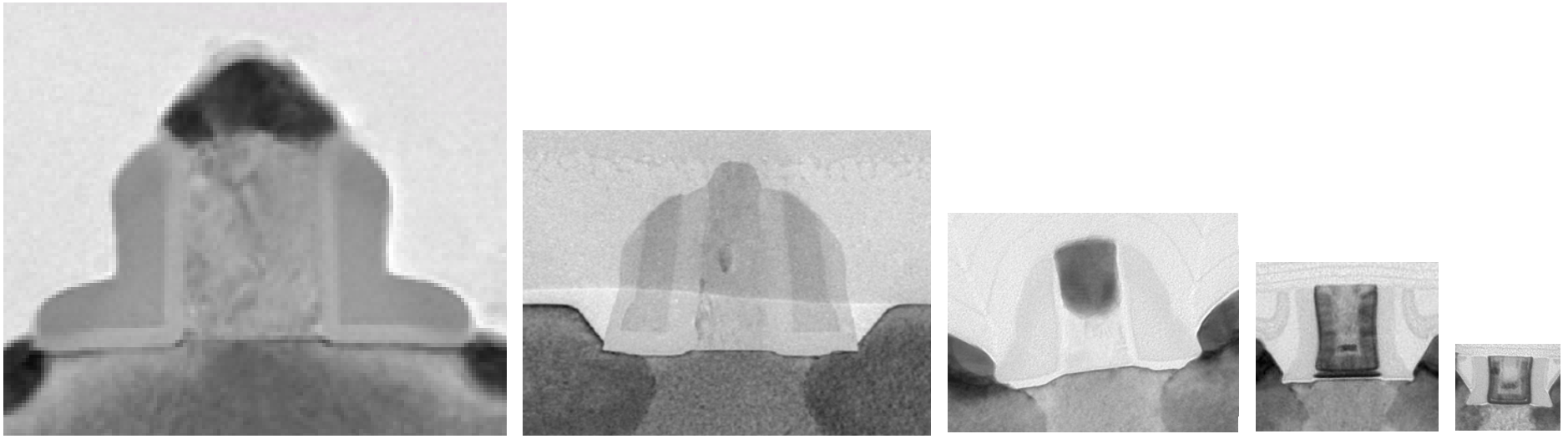
22nm – WIDE
0.092 μm²

90 nm	65 nm	45 nm	32 nm	22 nm
2003	2005	2007	2009	2011 *projected*



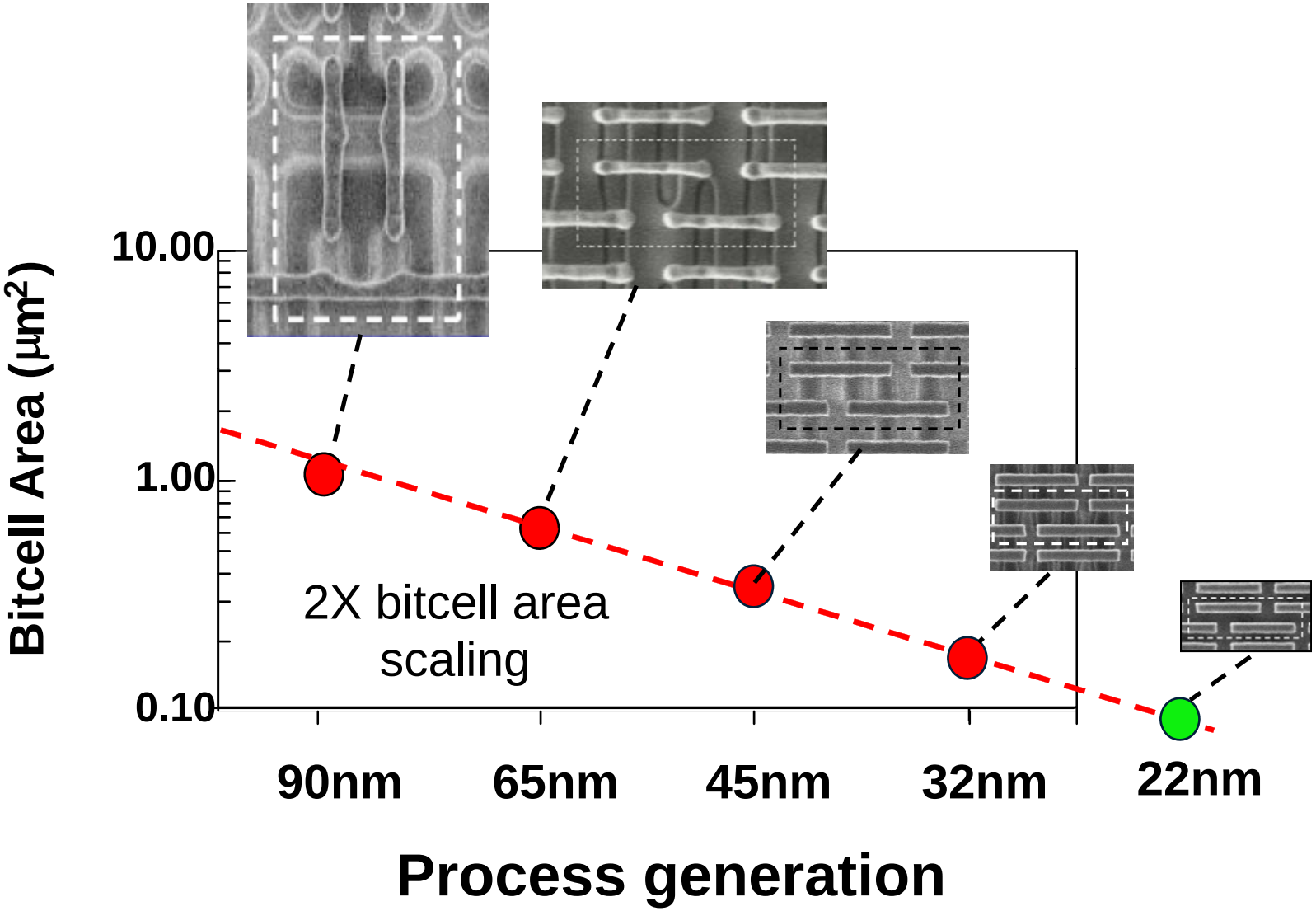
Changes in Scaling

THEN	NOW
• Scaling drove down cost	• Scaling drives down cost
• Scaling drove performance	• Materials drive performance
• Performance constrained	• Power constrained
• Active power dominates	• Standby power dominates
• Independent design-process	• Collaborative design-process



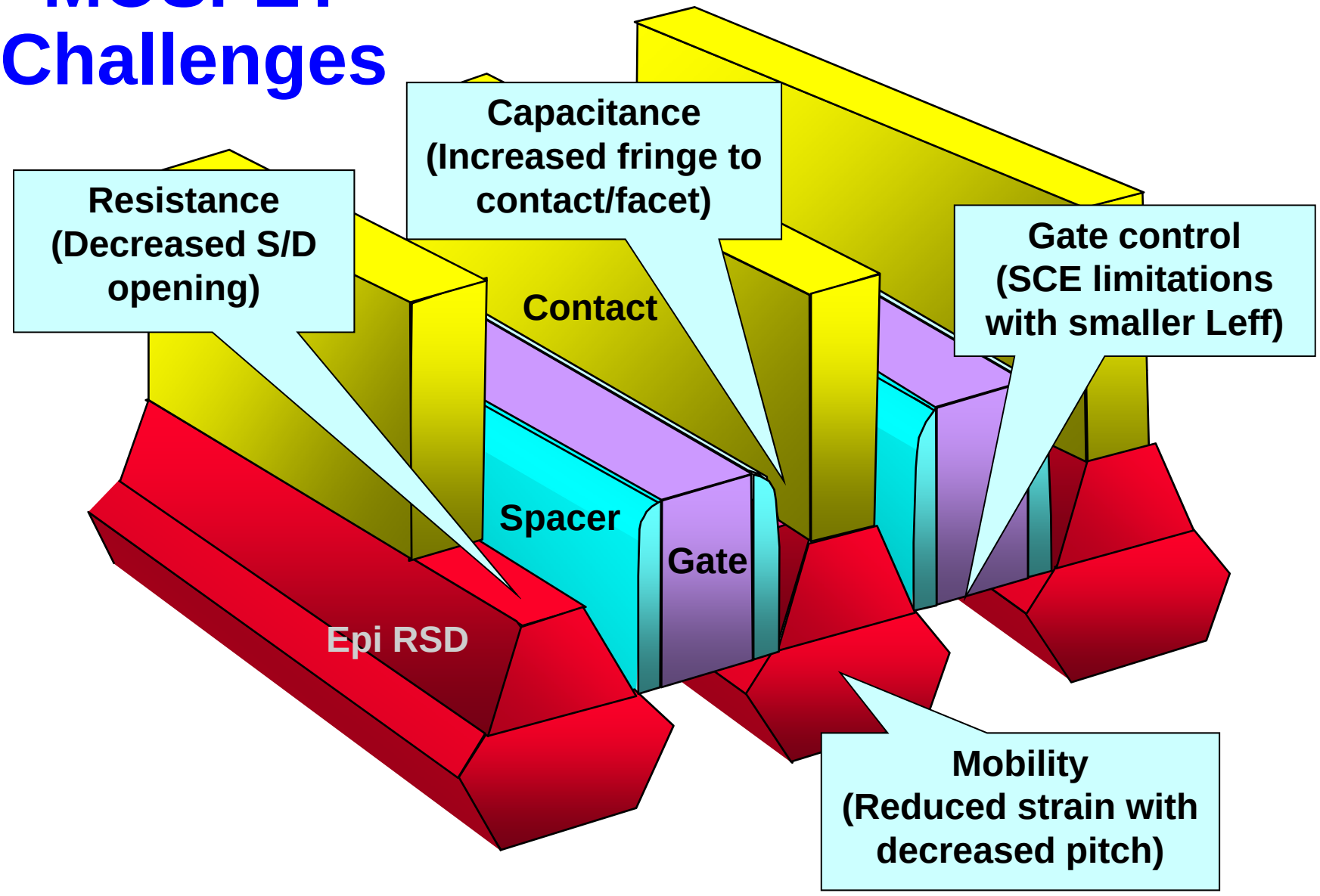
130nm 90nm 65nm 45nm 32nm

Consistent SRAM Density Scaling



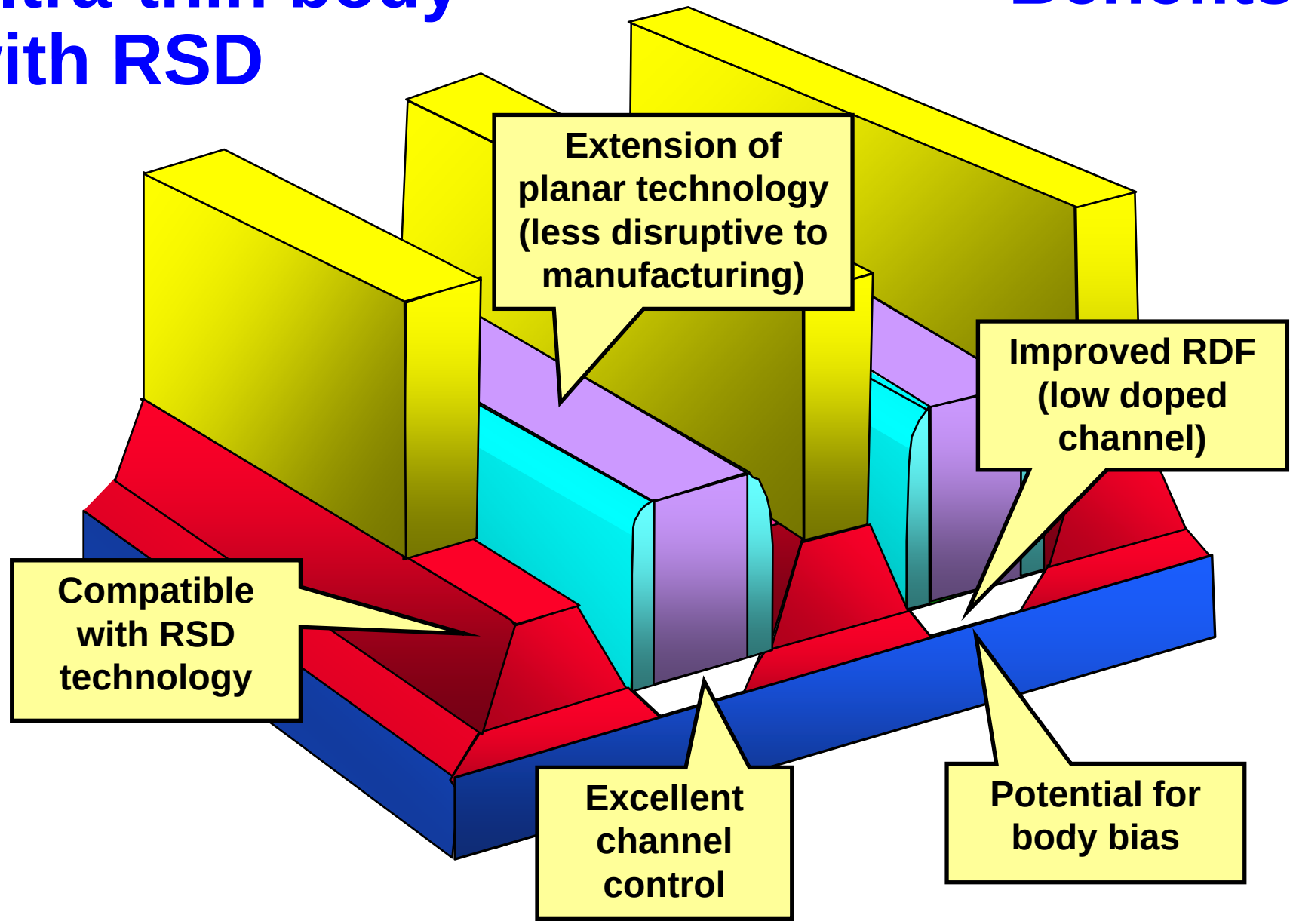
K. Zhang, ISCC, 2009; M. Bohr IDF 2010

MOSFET Challenges



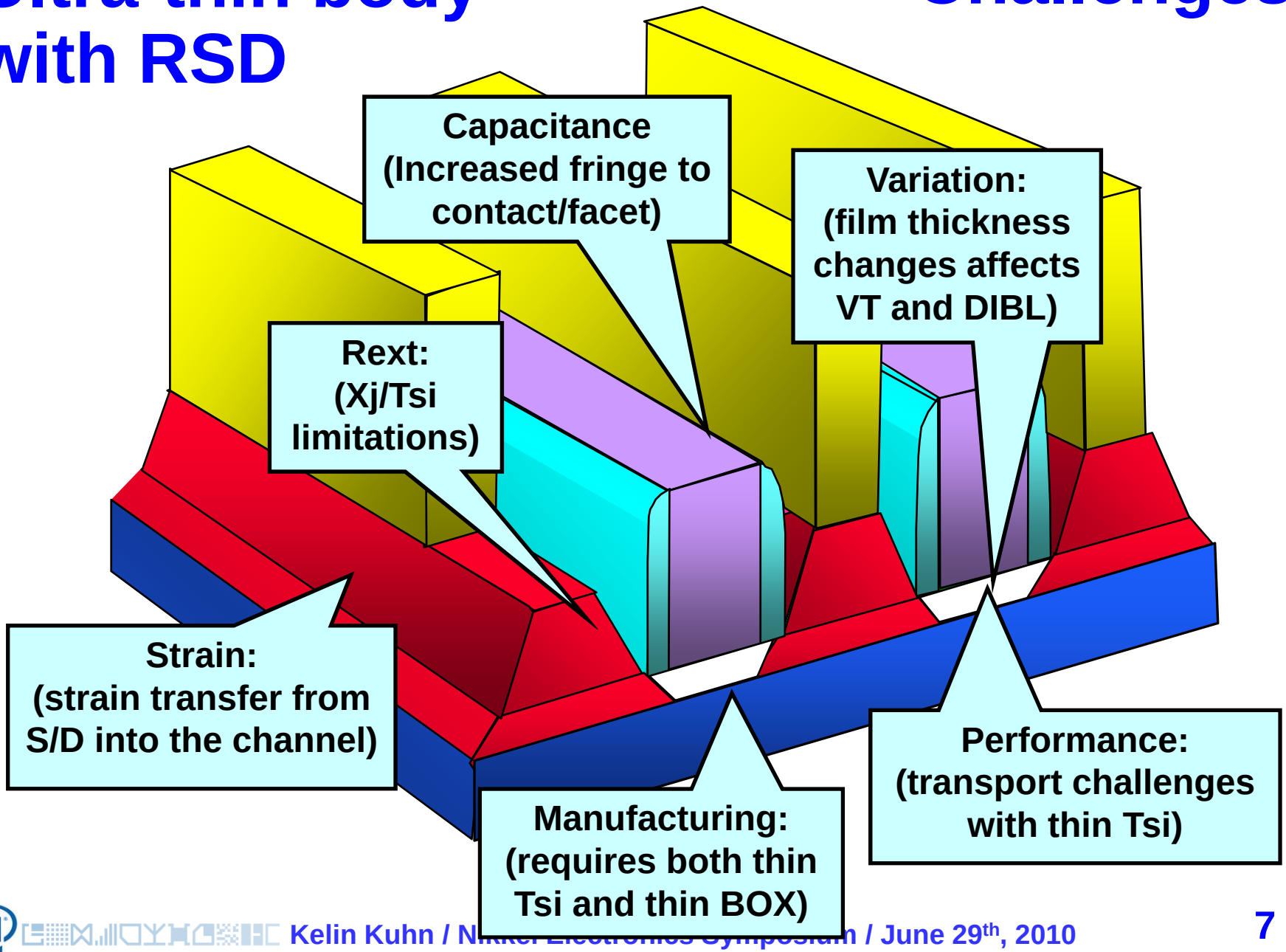
Ultra-thin body with RSD

Benefits



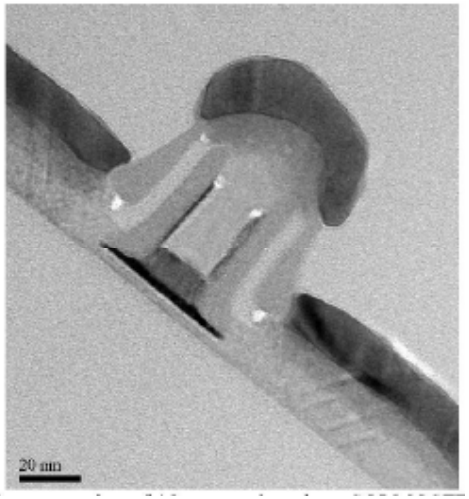
Ultra-thin body with RSD

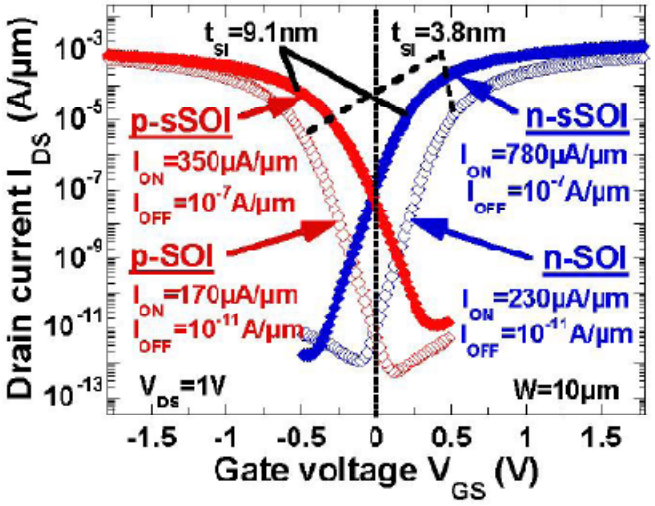
Challenges

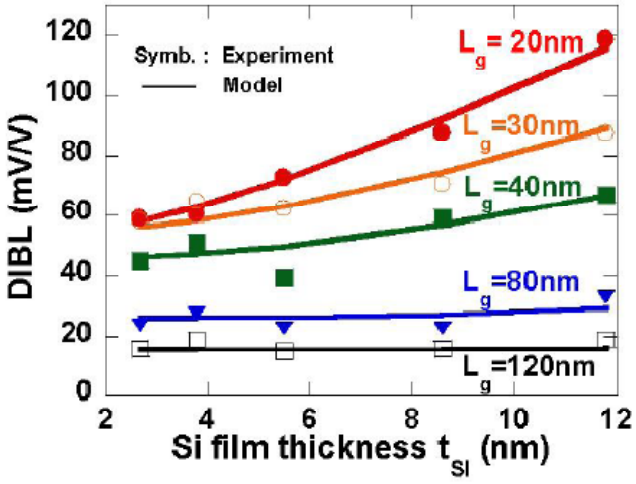


Ultra-thin body

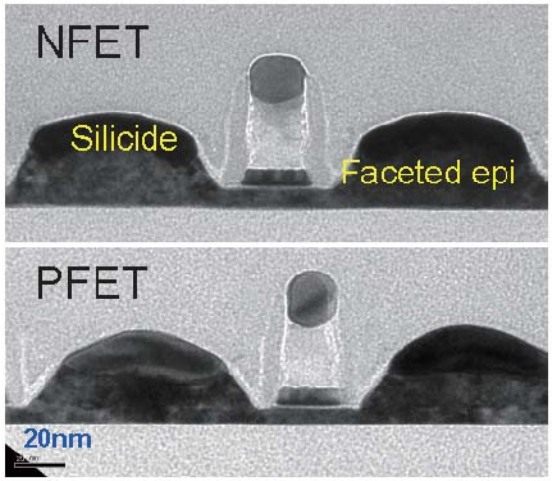
Barral – CEA-LETI– IEDM 2007

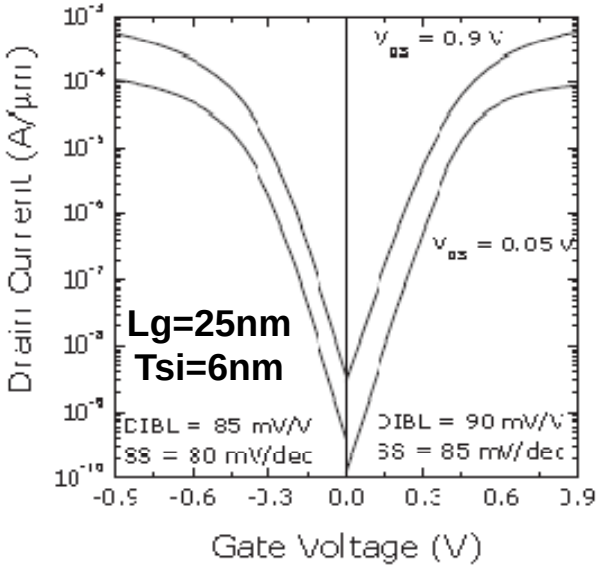


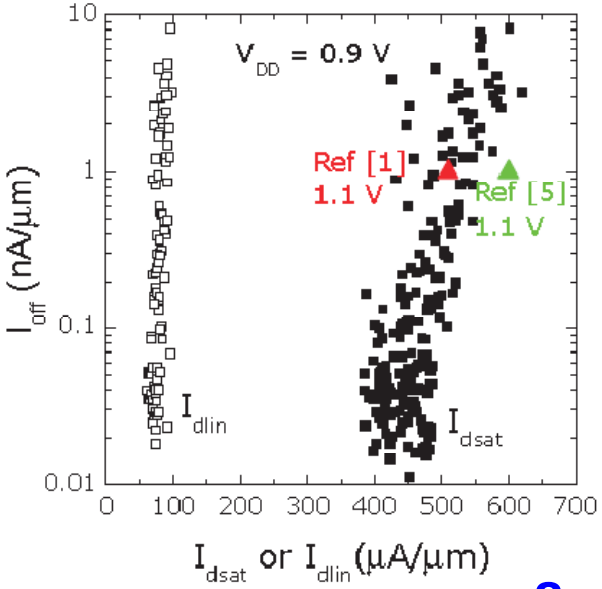




Cheng – IBM – VLSI 2009

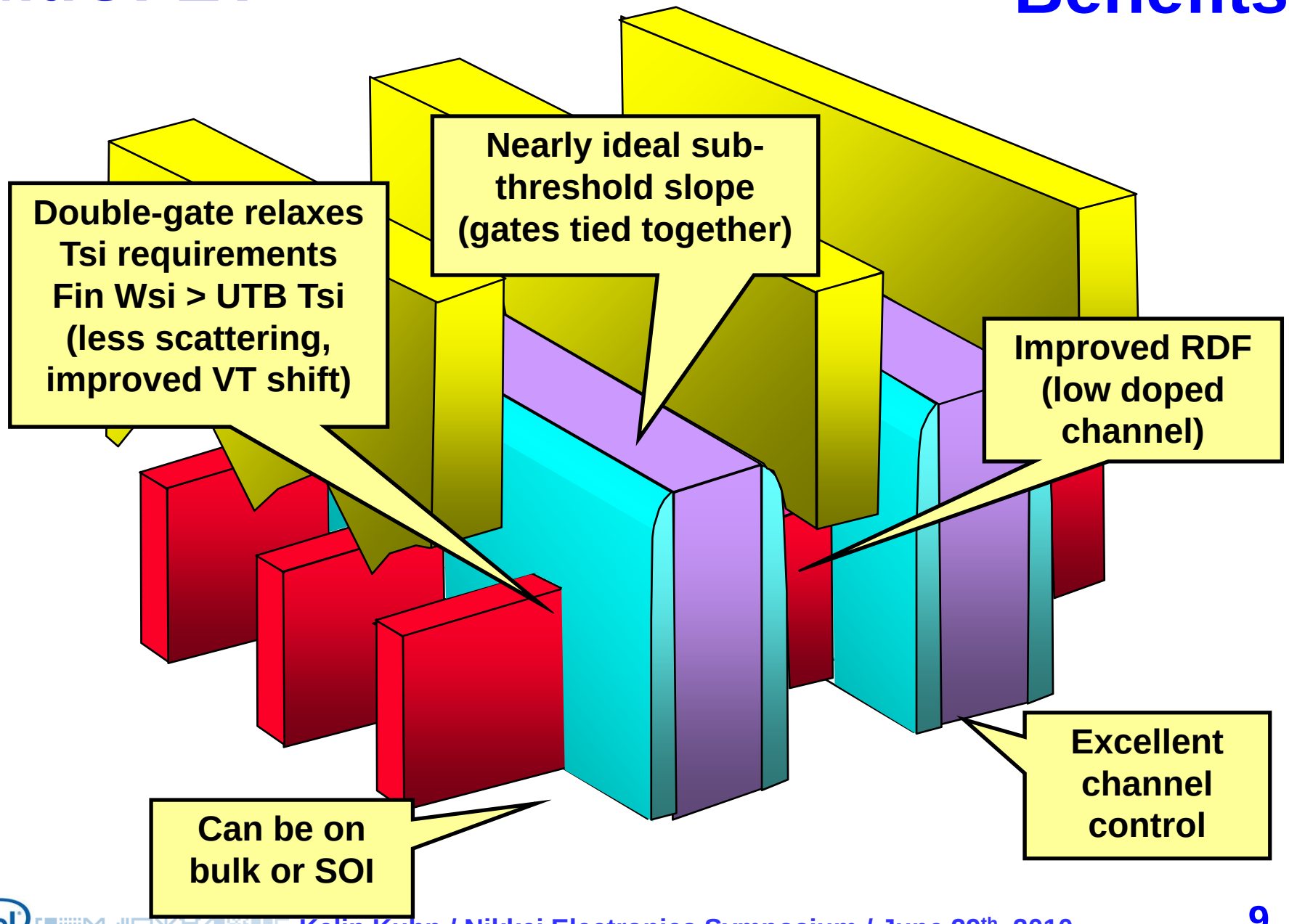






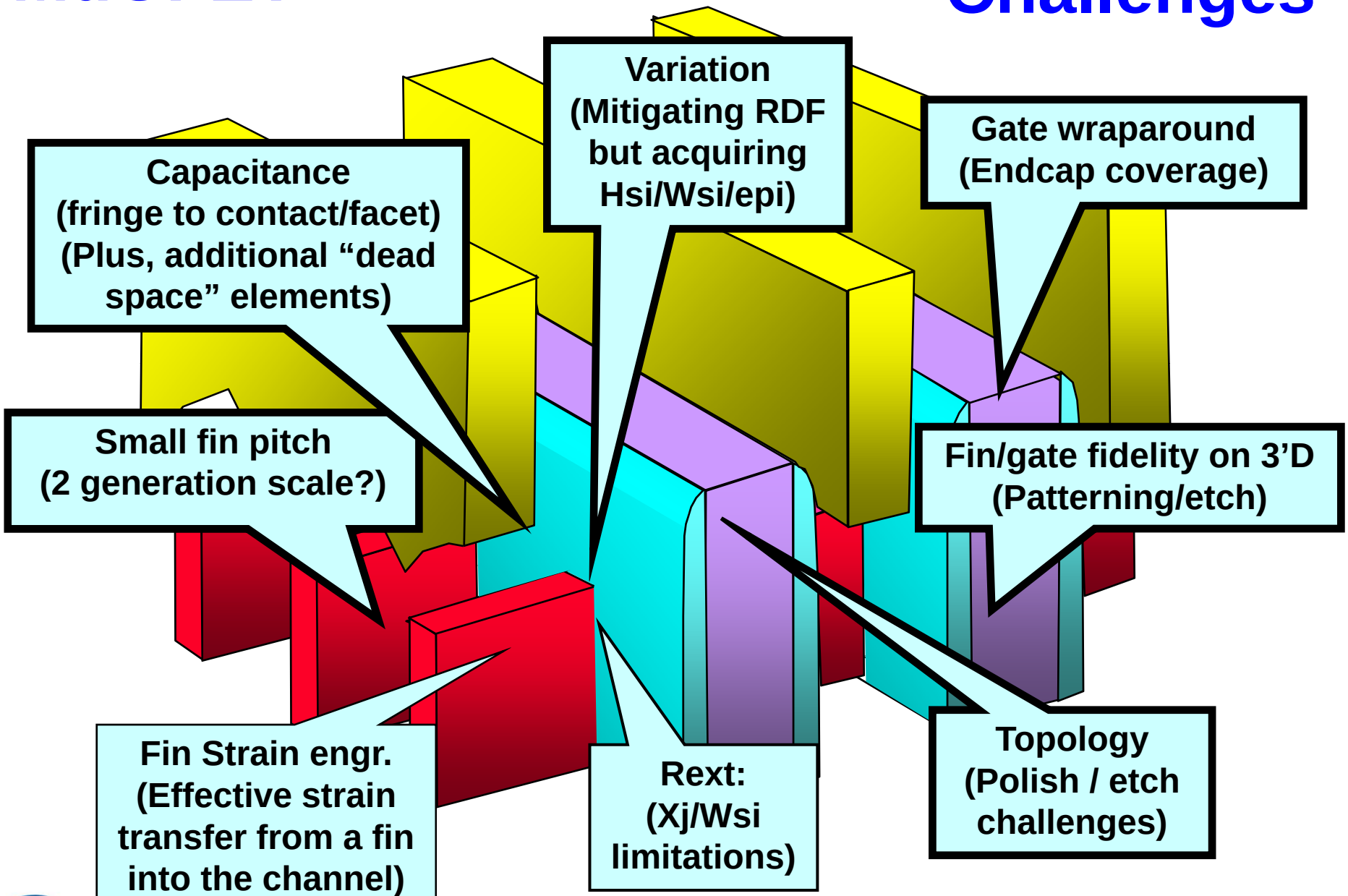
MuGFET

Benefits



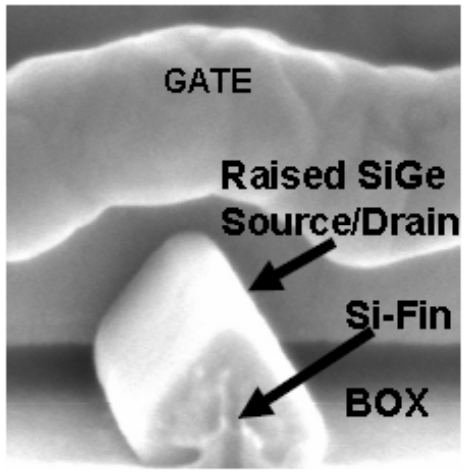
MuGFET

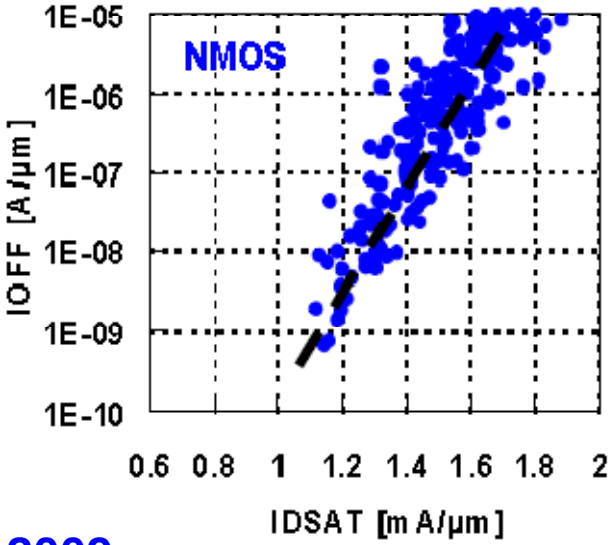
Challenges

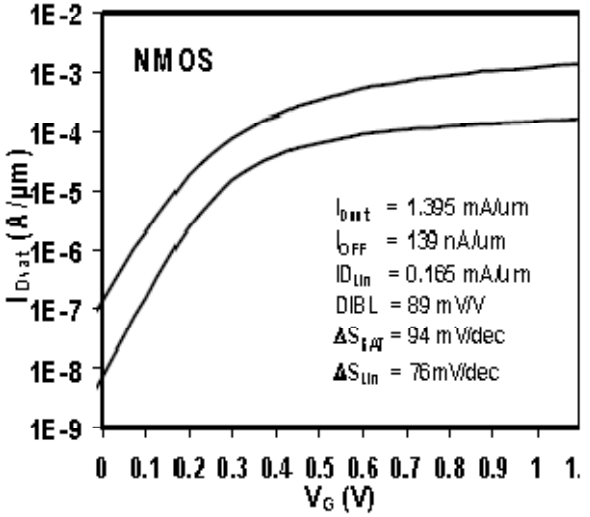


MuGFET

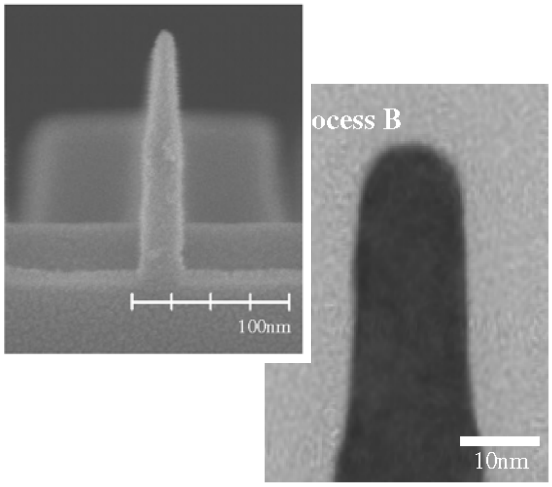
Kavalieros – Intel – IEDM 2006

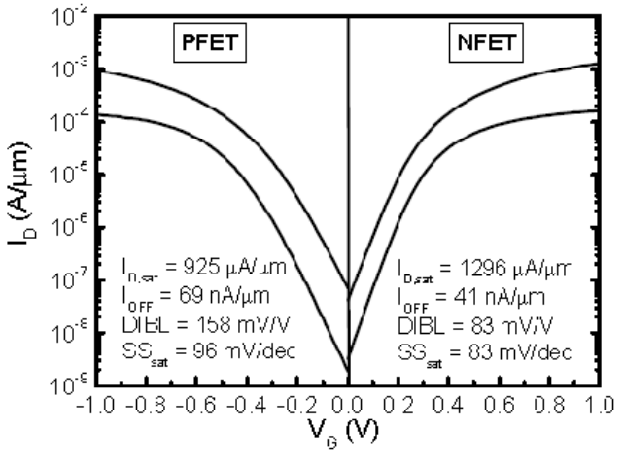


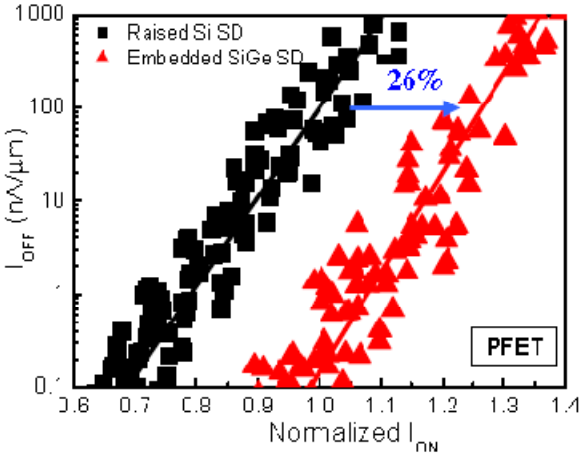




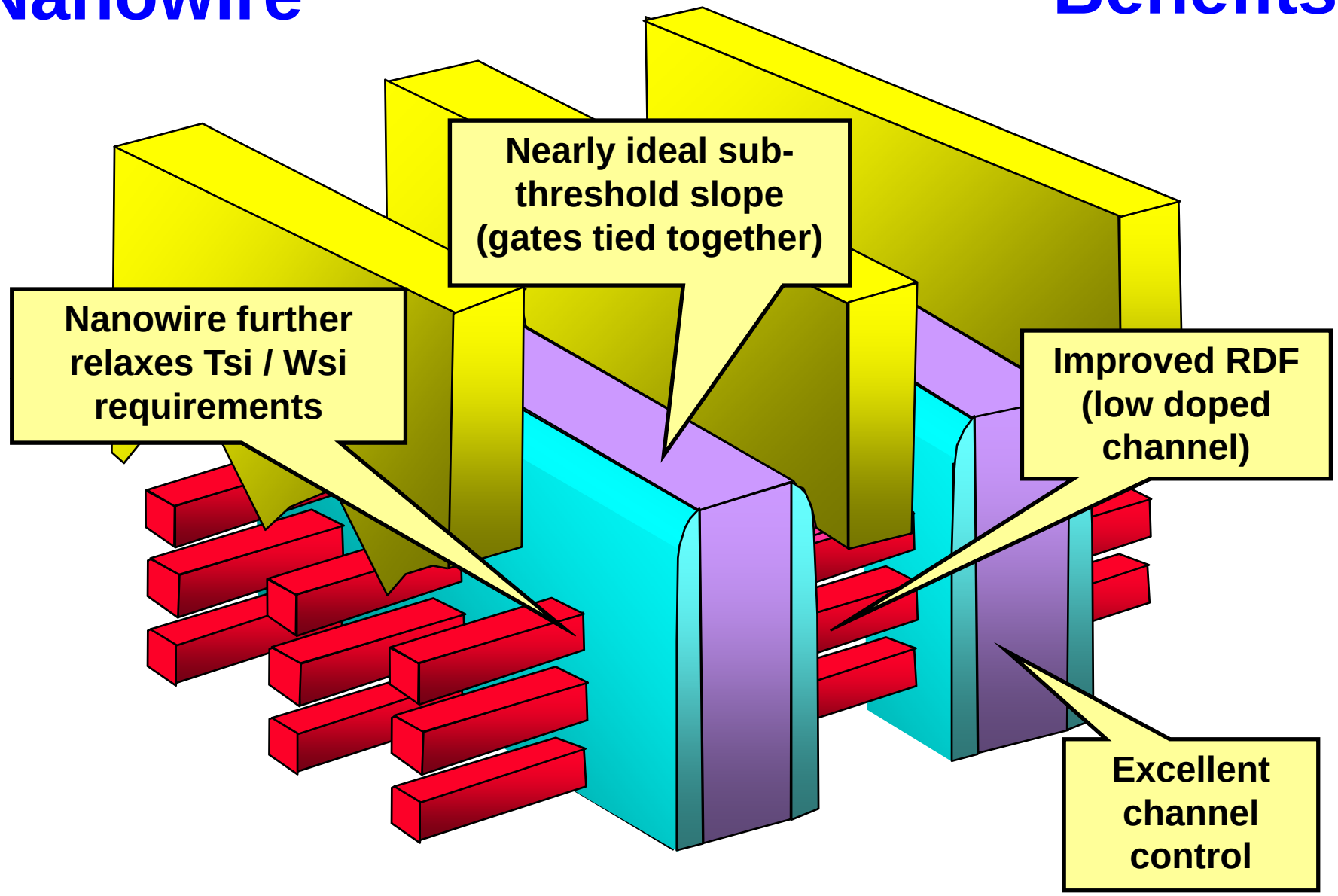
Chang – TSMC – IEDM 2009



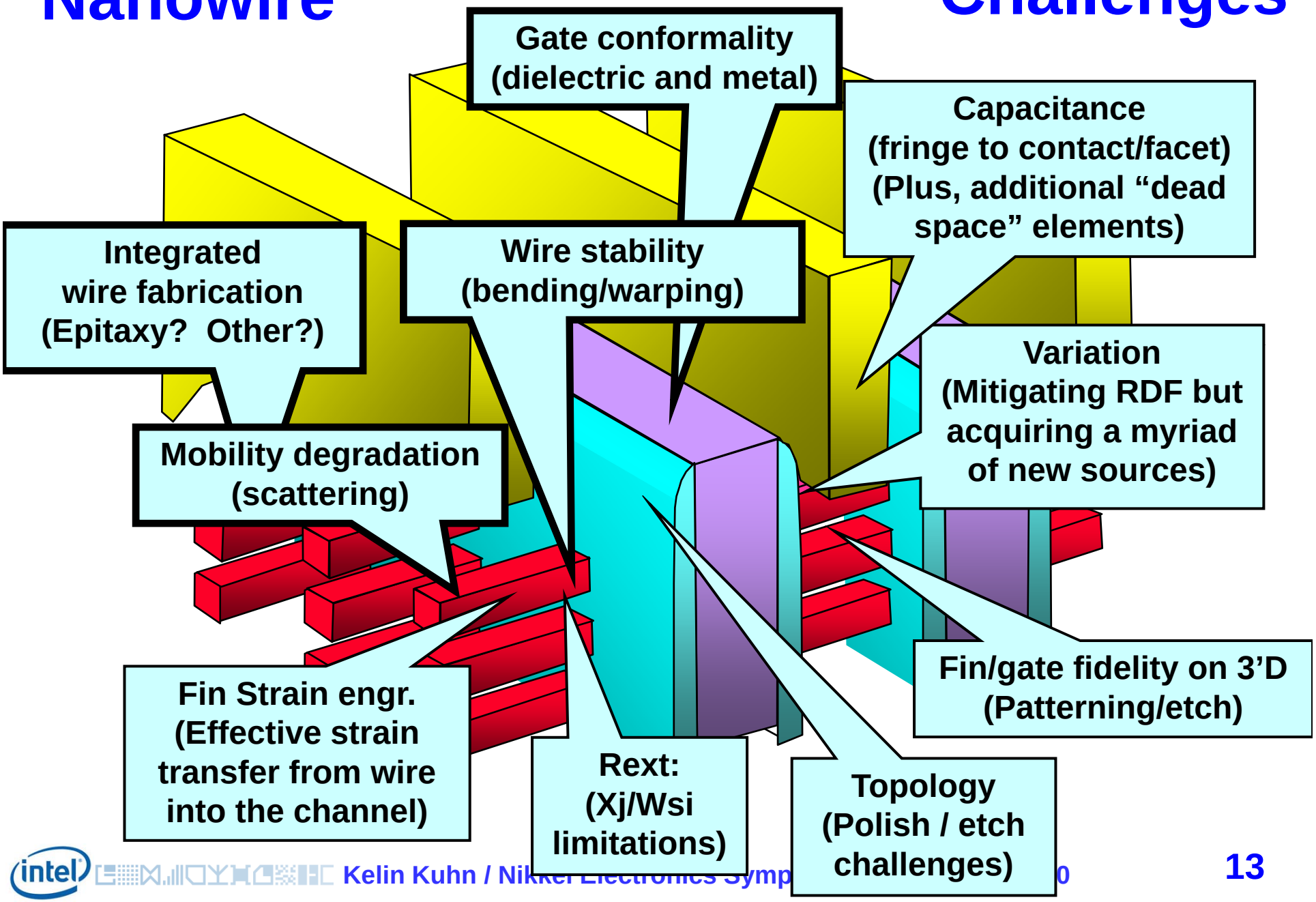




Nanowire Benefits

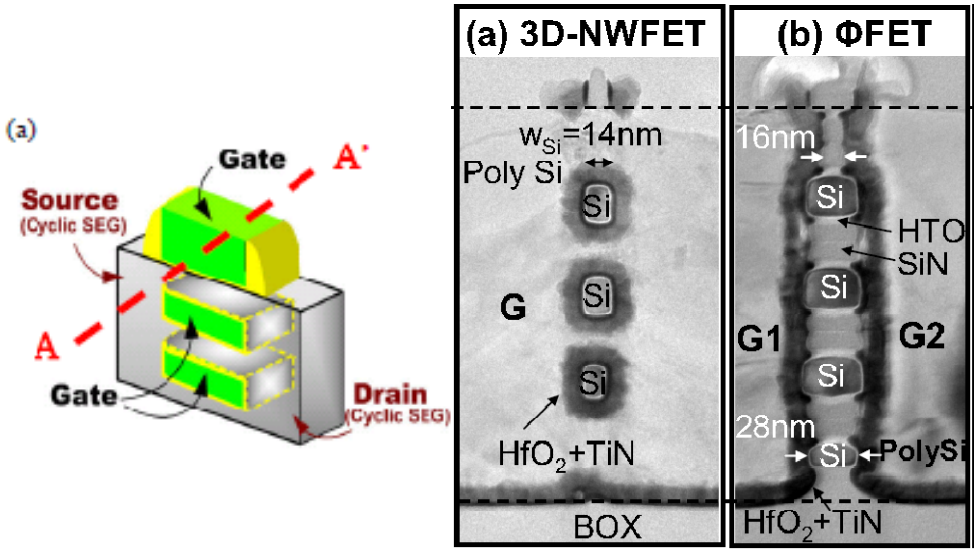


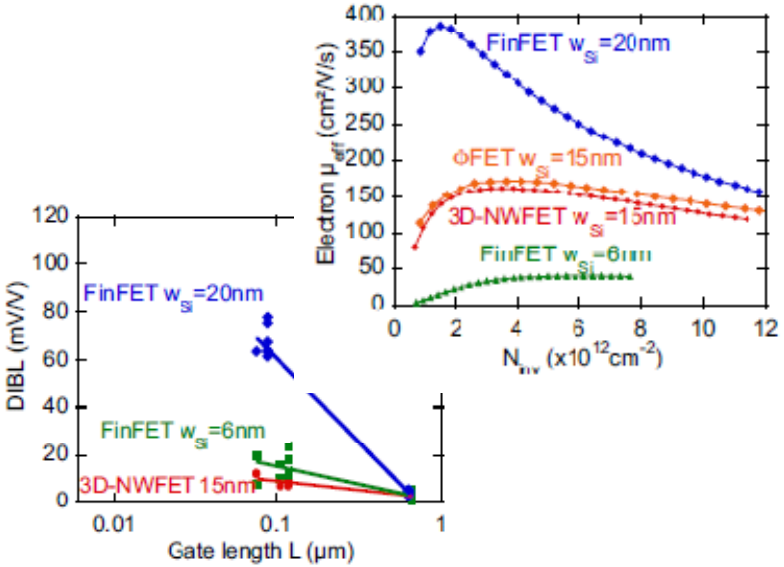
Nanowire Challenges



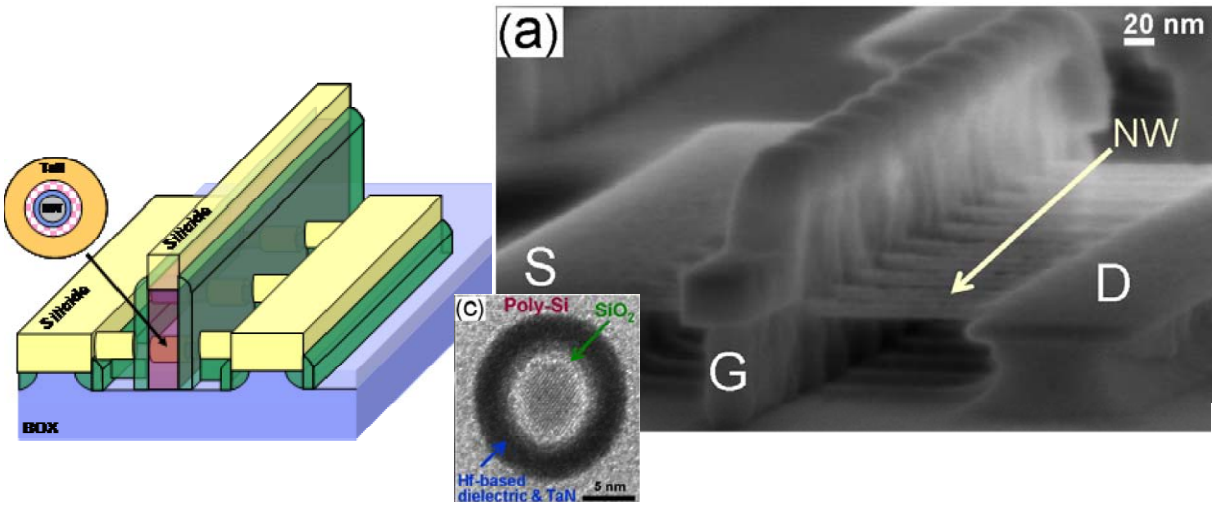
Nanowire FETs

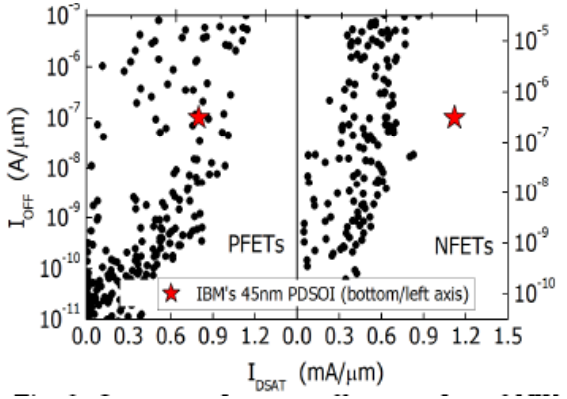
Dupre – CEA-LETI – IEDM 2008





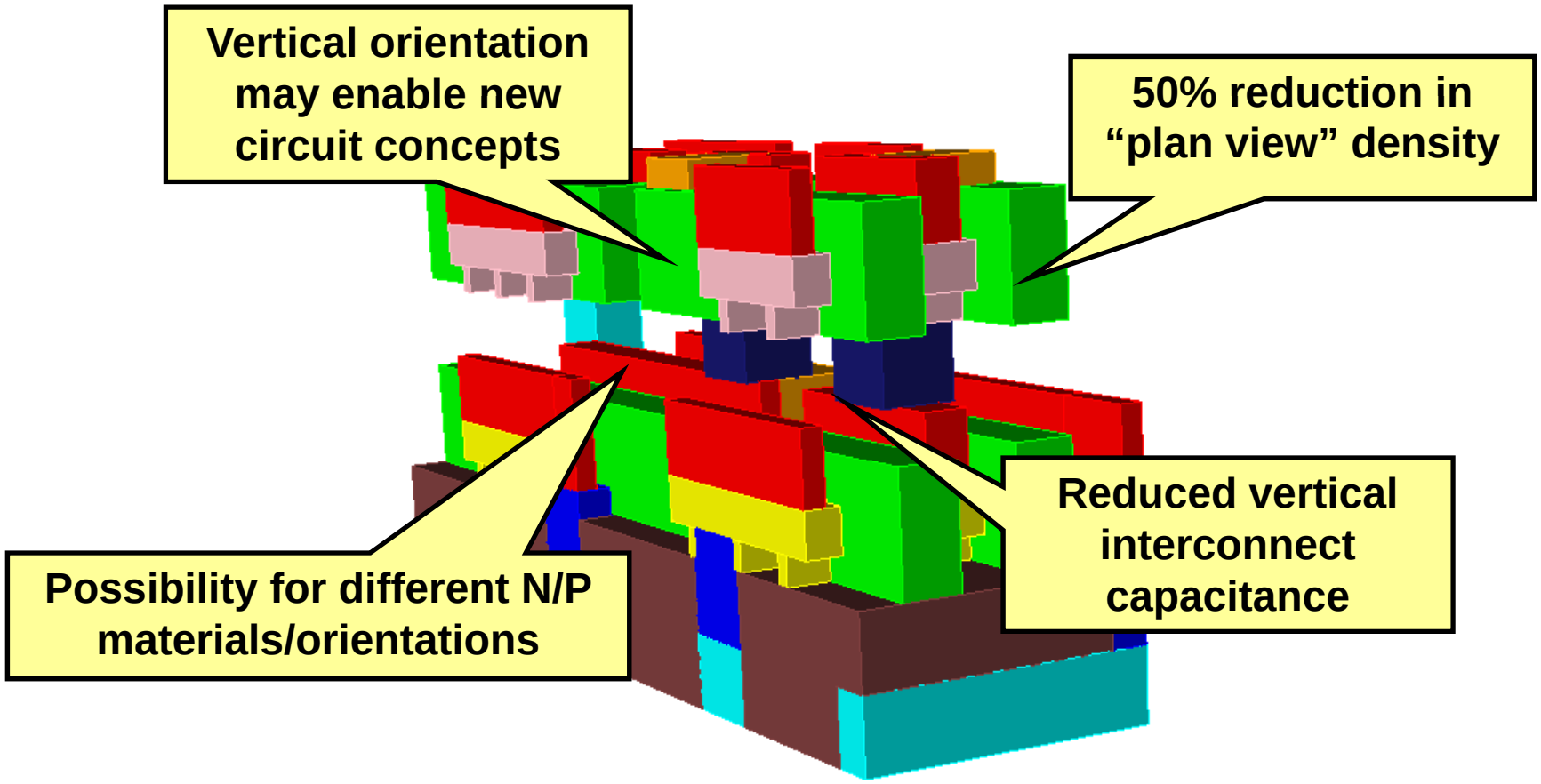
Bangsaruntip – IBM – IEDM 2009





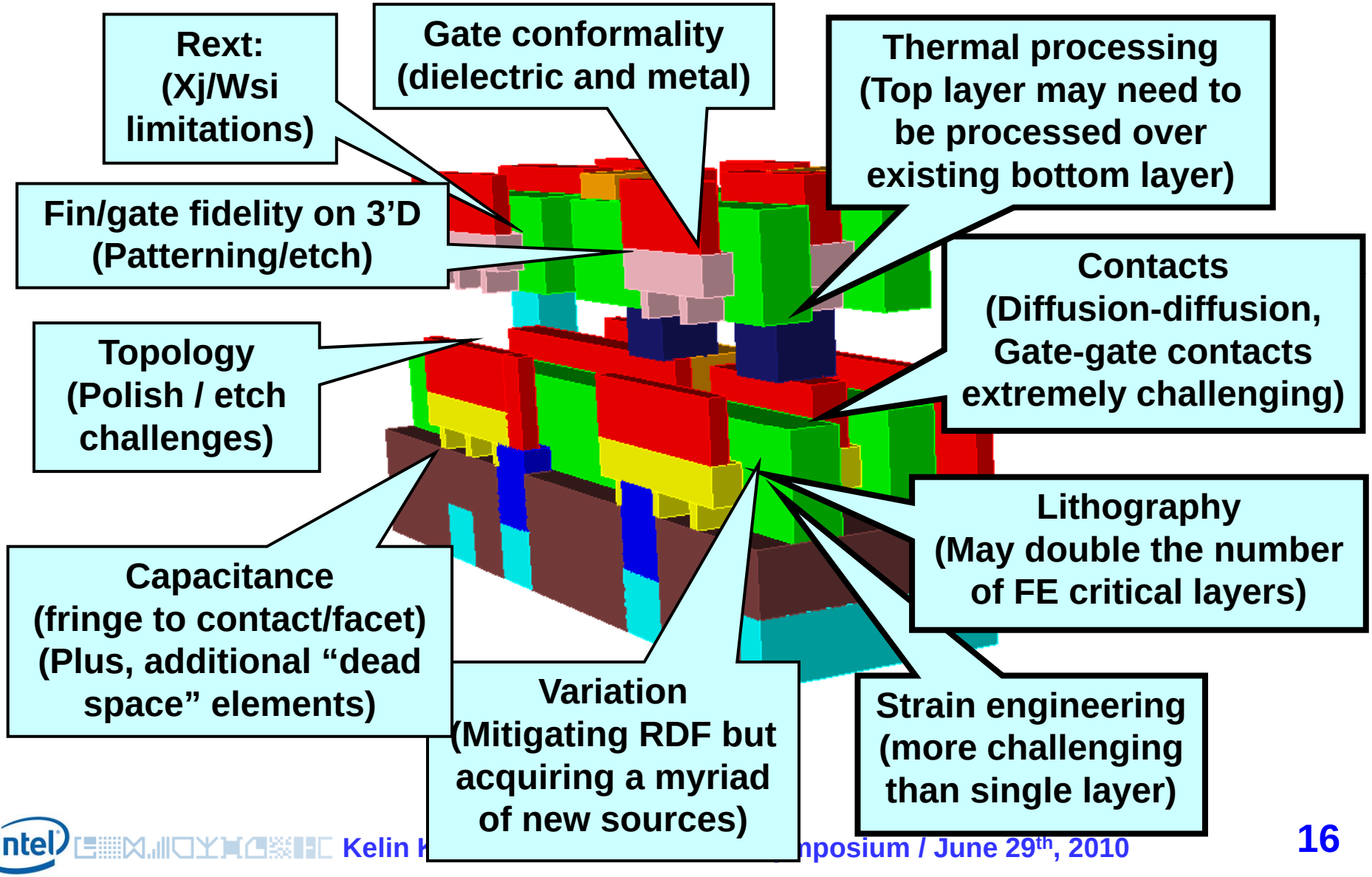
Vertical Architectures

Benefits



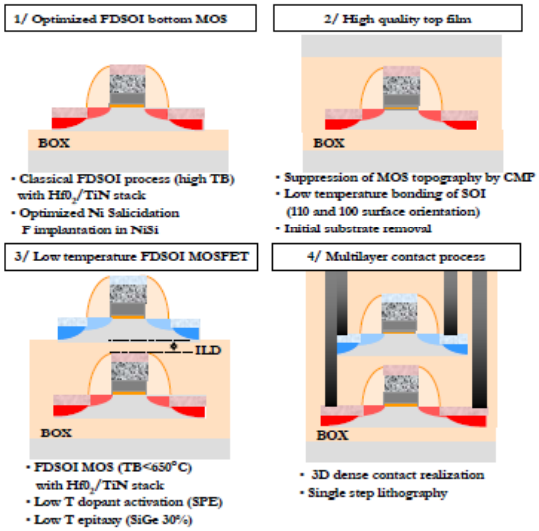
Vertical Architectures

Challenges



Vertical

Batude – CEA LETI - IEDM 2009 – stacked 110/100



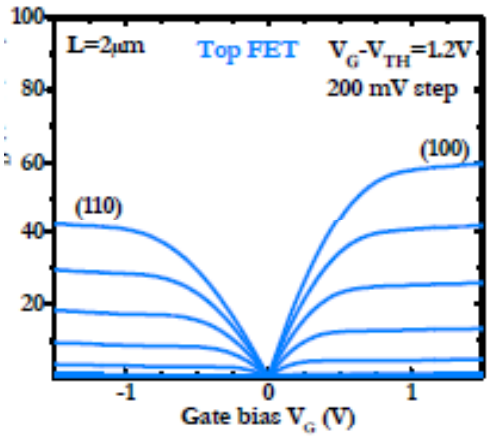


Fig.15: I_D-V_D characteristics of top FET

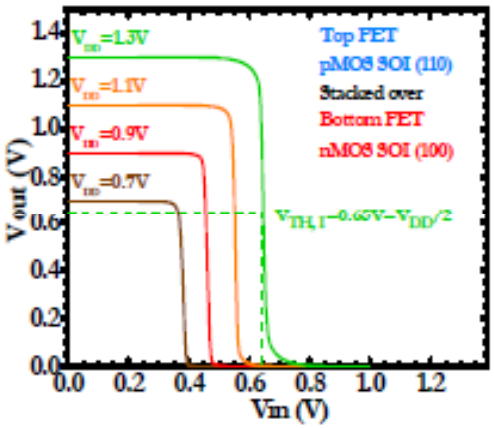
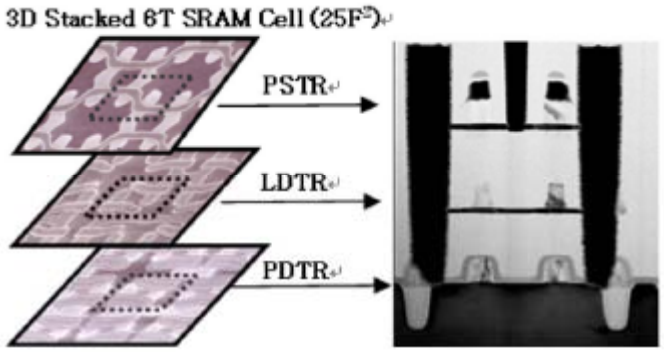
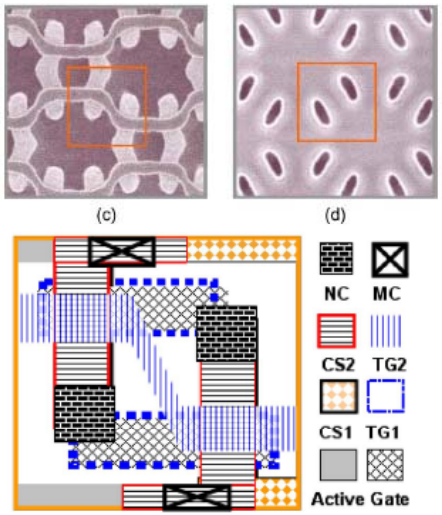
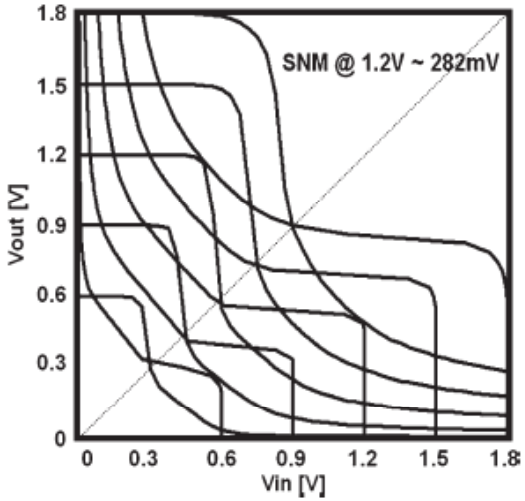


Fig.16:Transfer Voltage characteristic of an inverter: top SOI (110) pFET and bottom SOI (100) nFET

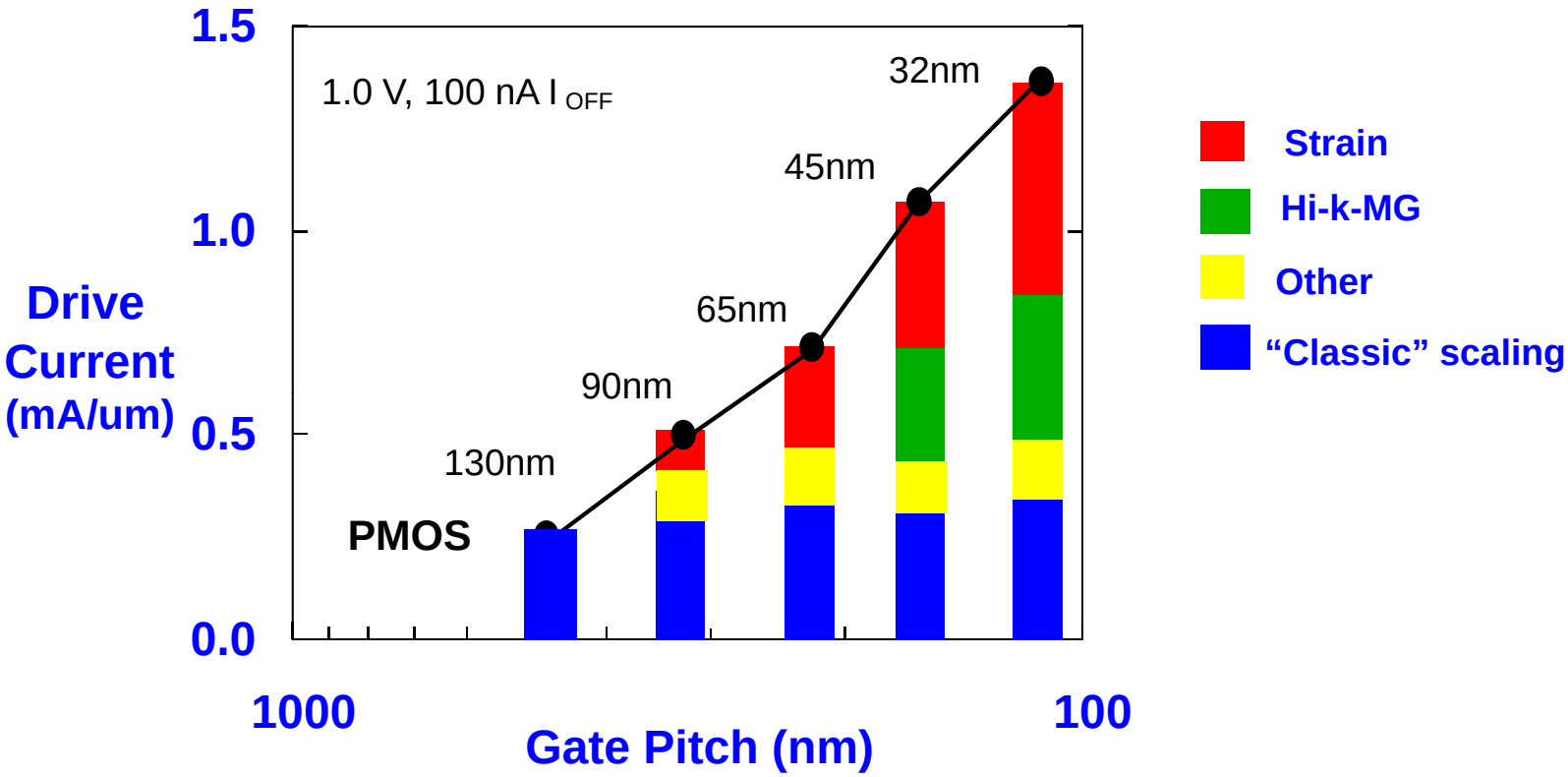
Jung – Samsung - IEEE TED 2010 – 3'D stacked 6T







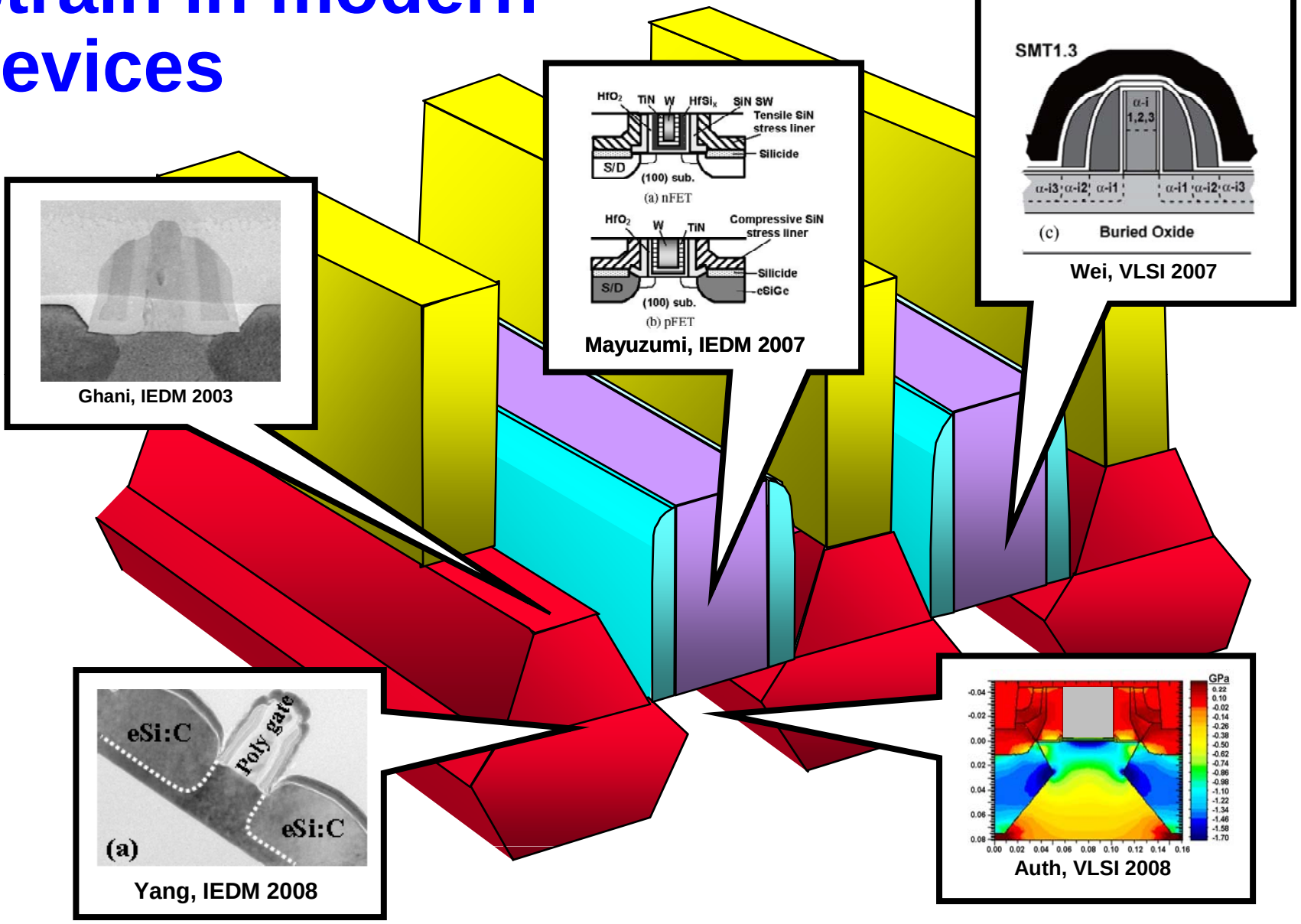
Transistor Performance Trend



Strain is a critical ingredient in modern transistor scaling

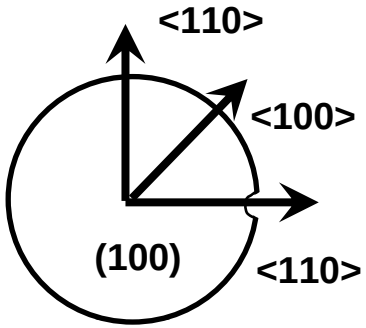
Strain was first introduced at 90nm, and its contribution has increased in each subsequent generation

Strain in modern devices



ORIENTATION

(100) surface – top down

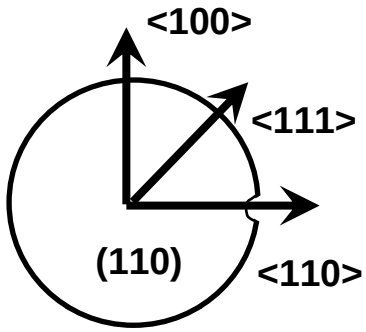


Standard wafer / direction
(100) Surface / <110> channel

(100) Surface / <100>
(a "45 degree" wafer)

Both <110> directions are the same.

(110) surface – top down

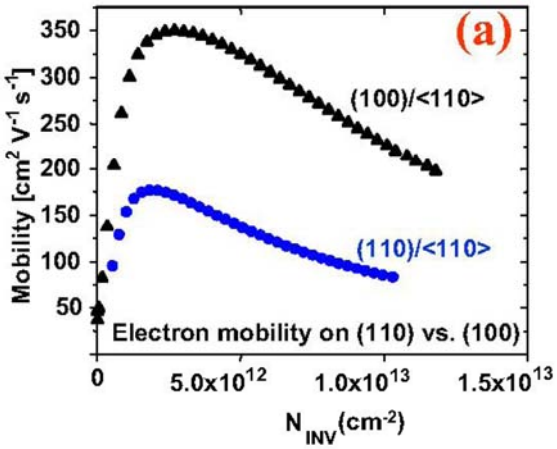


Non-standard

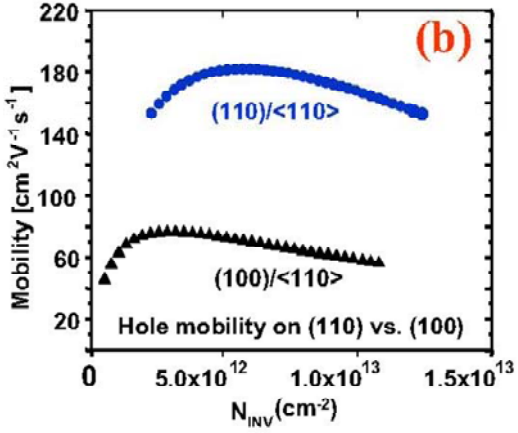
(110) Surface

Three possible channel directions
<110> <111> and <100>

(100) BEST NMOS



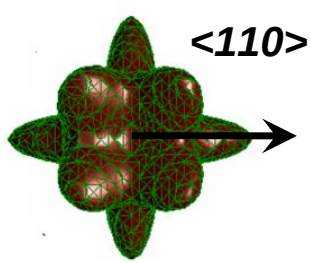
(110) <110> BEST PMOS



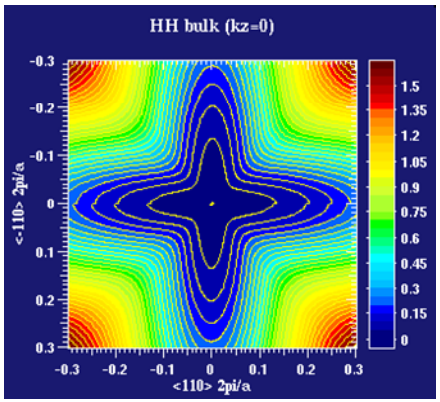
Yang
AMD/IBM
EDST 2007

Orientation and Strain: More complex for non-(100) orientations

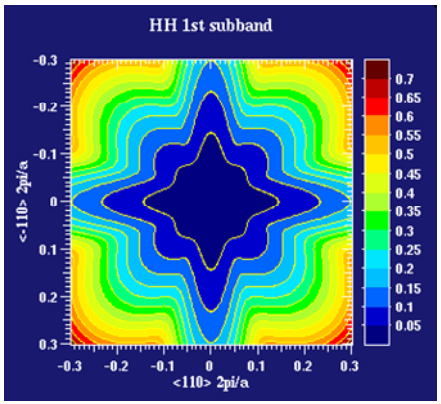
(100)



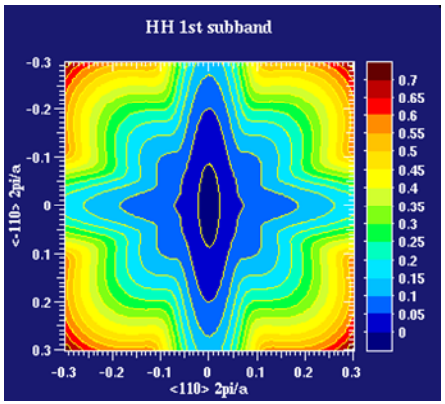
(001) Surface (k⊥=0)



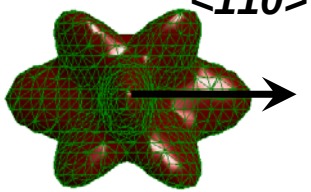
(001) Surface Vg=-1V



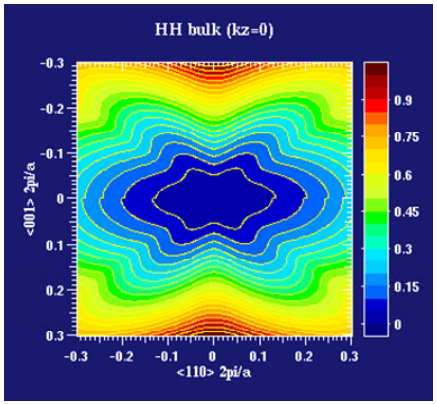
(001) Surface Vg=-1V, Sxx=-1GPa



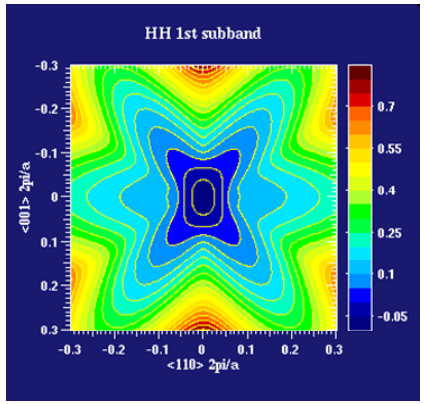
(110)



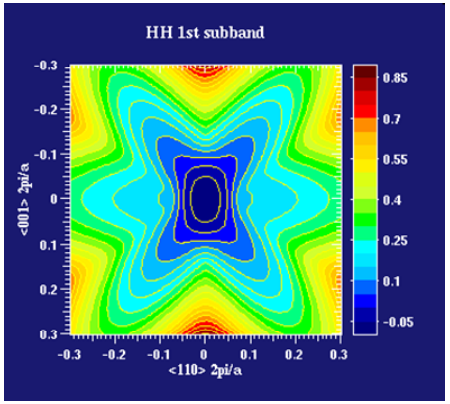
(110) Surface (k⊥=0)



(110) Surface Vg=-1V

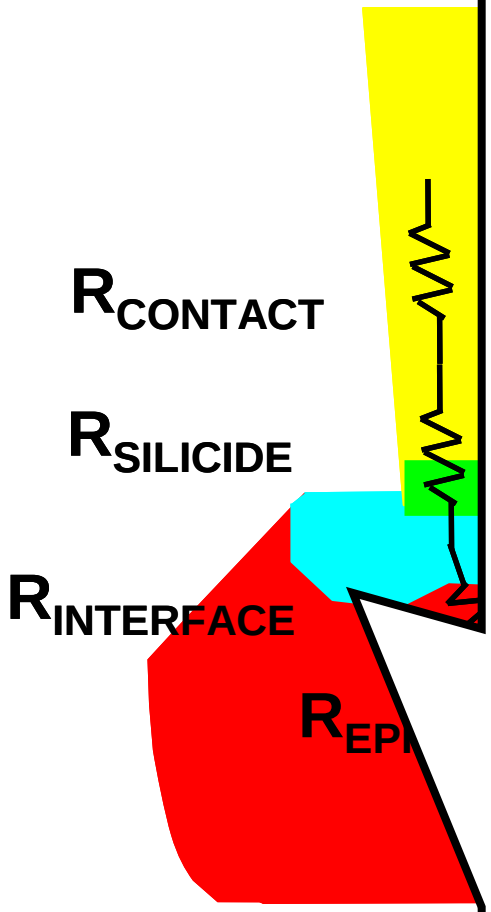


(110) Surface Vg=-1V, Sxx=-1GPa



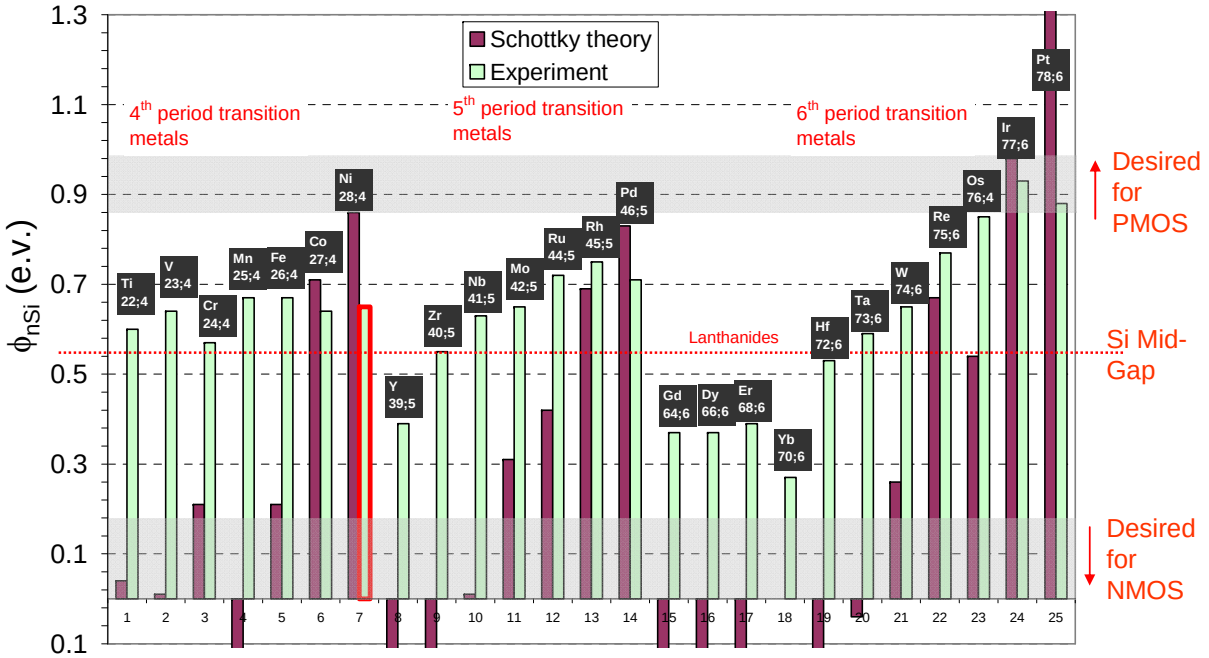
BULK **1'D CONFINED** **1'D CONFINED STRAINED**

Planar Resistive Elements



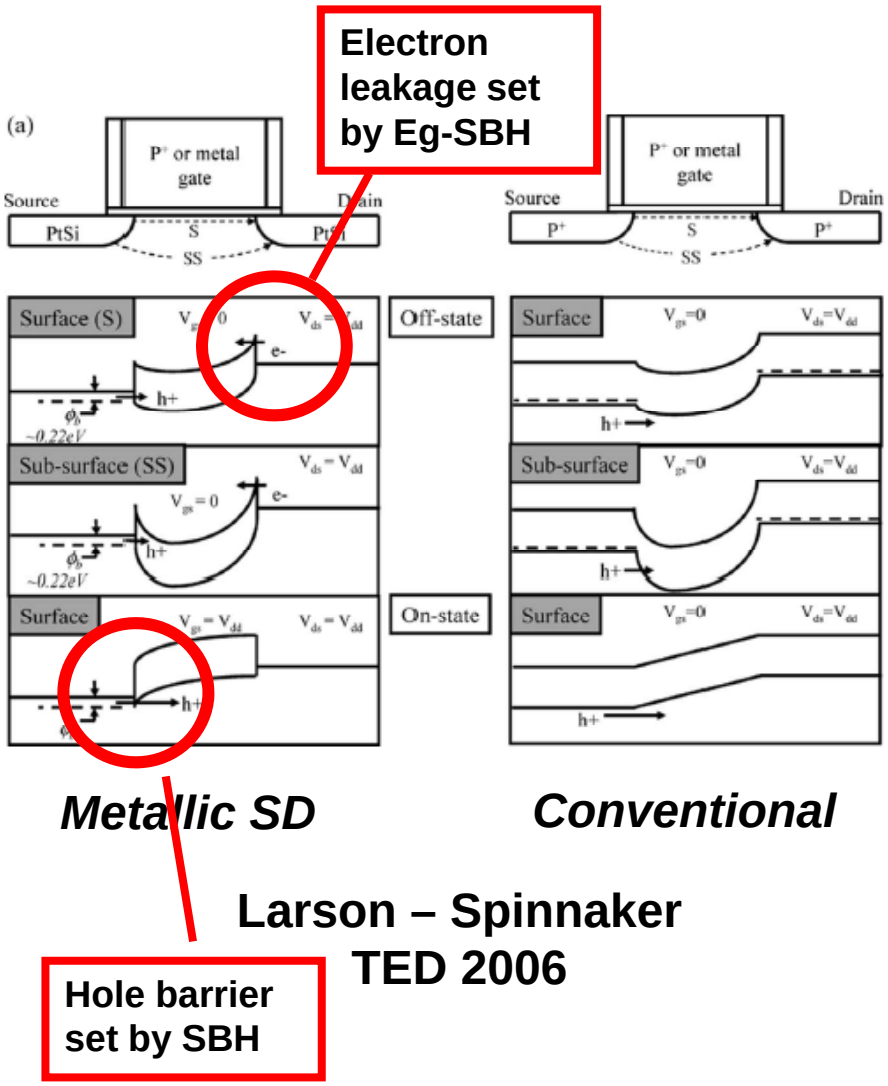
Rinterface: Reduction in Schottky Barrier Height

$$R_{\text{interface}} \propto \exp\left(\frac{q\phi_B}{\sqrt{N_D}}\right)$$



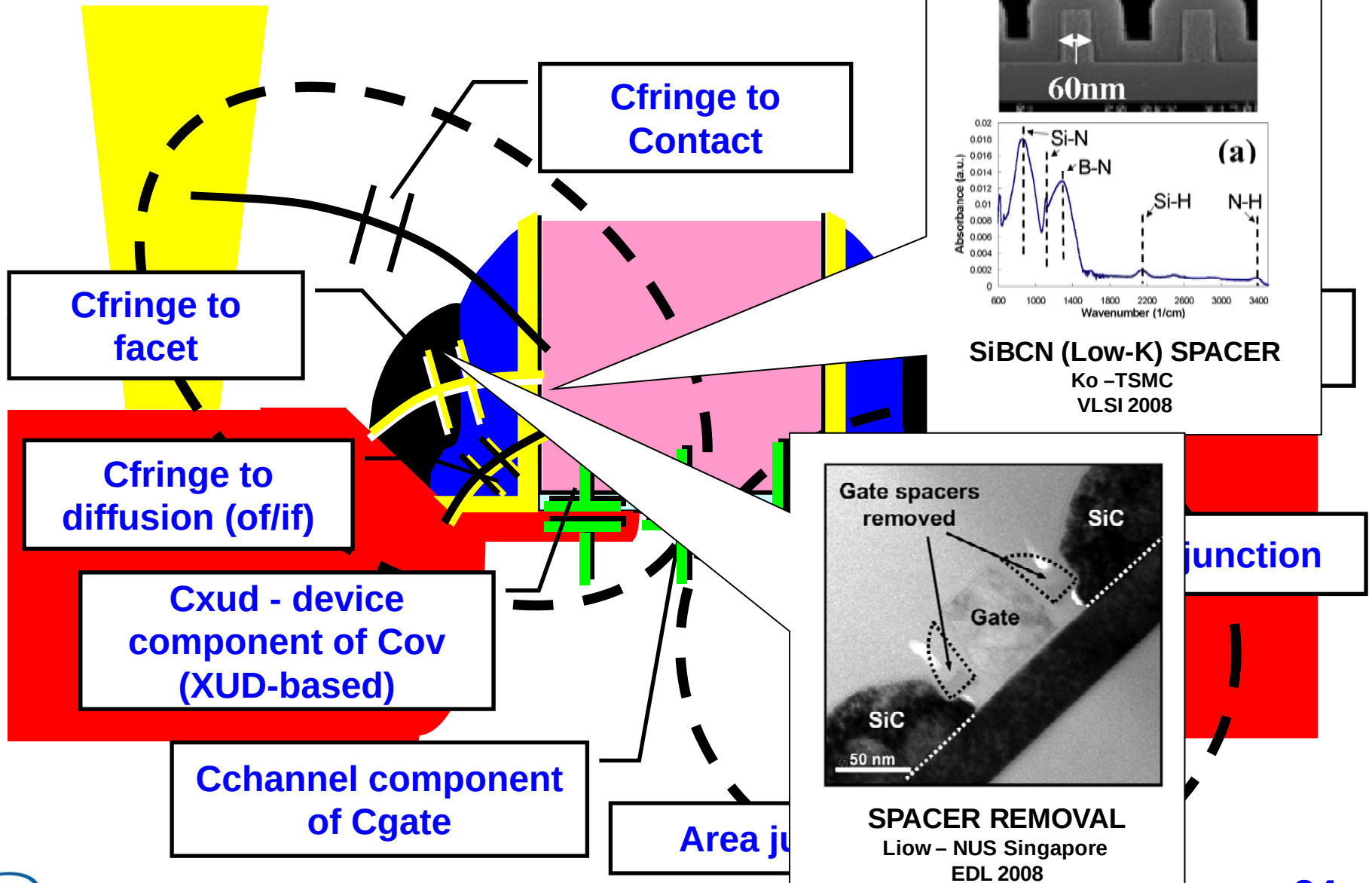
Schottky Barrier Height Reduction is a critical area for development. Techniques under investigation include exotic alloys, implants, and Fermi-unpinning layers

Schottky barrier S/D – an option?



- In a metal SB-MOS, S/D forms an atomically abrupt Schottky-barrier having the height ϕb.
- The extreme limit for metal in the S/D regions (with associated improvements in Rext)
- Unconventional operation (field emission device in the ON state)
- Needs complementary devices (midgap silicide or two silicides)

Planar Capacitive Elements



Looking Forward

Low risk

Enhancements in strain technology
Enhancements in annealing/implant technology

Medium Risk

Optimized substrate and channel orientation
Reduction in MOS parasitic resistance
Reduction in MOS parasitic capacitance

High risk

UTB devices
MuGFETS
Nanowires
Vertical Devices