Technology Research to Drive Innovation

Mike Mayberry
Components Research
VP, Technology and Manufacturing Group
Intel Corporation

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Optimize Collaboration and Investing in R&D Pipeline

External
Consortia
Universities
Investment
Suppliers
Nat'l Labs
Internal

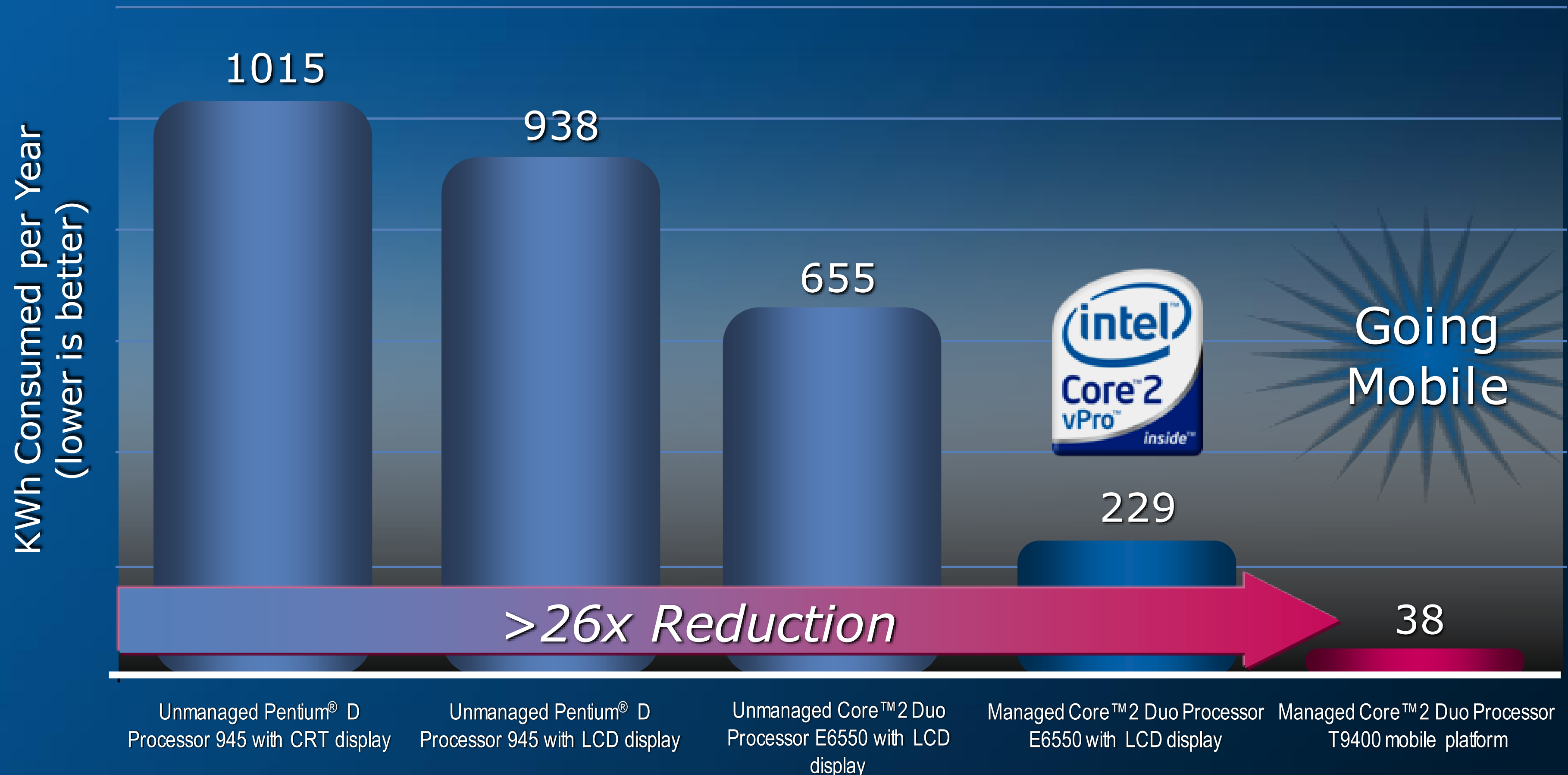
RESEARCH

Components Research
- How can we build it ?
- How can we integrate it ?

Intel Labs
- What should we build ?
- How will people use it ?

Identify Ideas/Options → Select Features/ Make it Work for HVM → High Volume Manufacturing

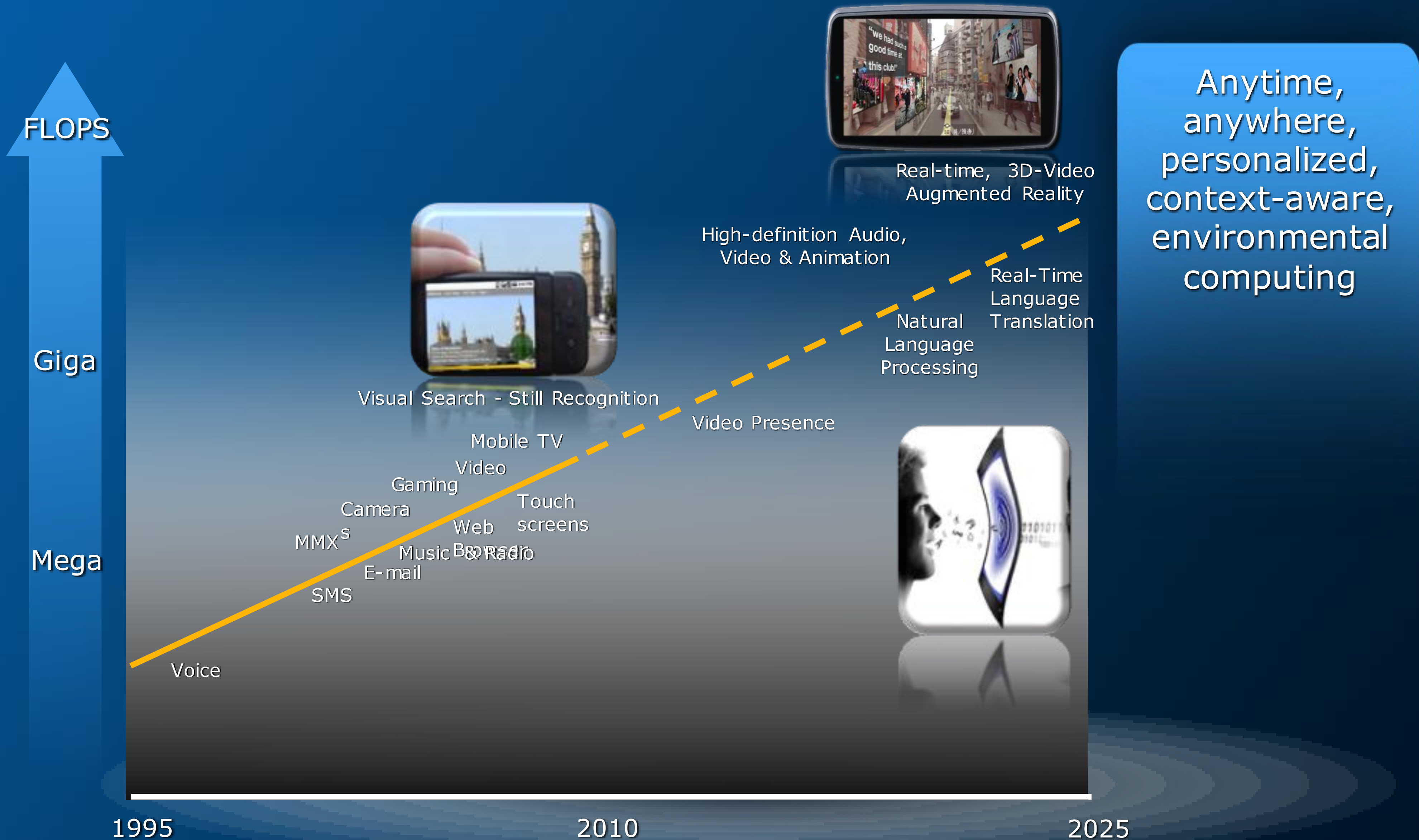
Potential Energy Savings Enabled by Moore's Law



Energy savings comes from combination of transistor scaling and architectural innovations

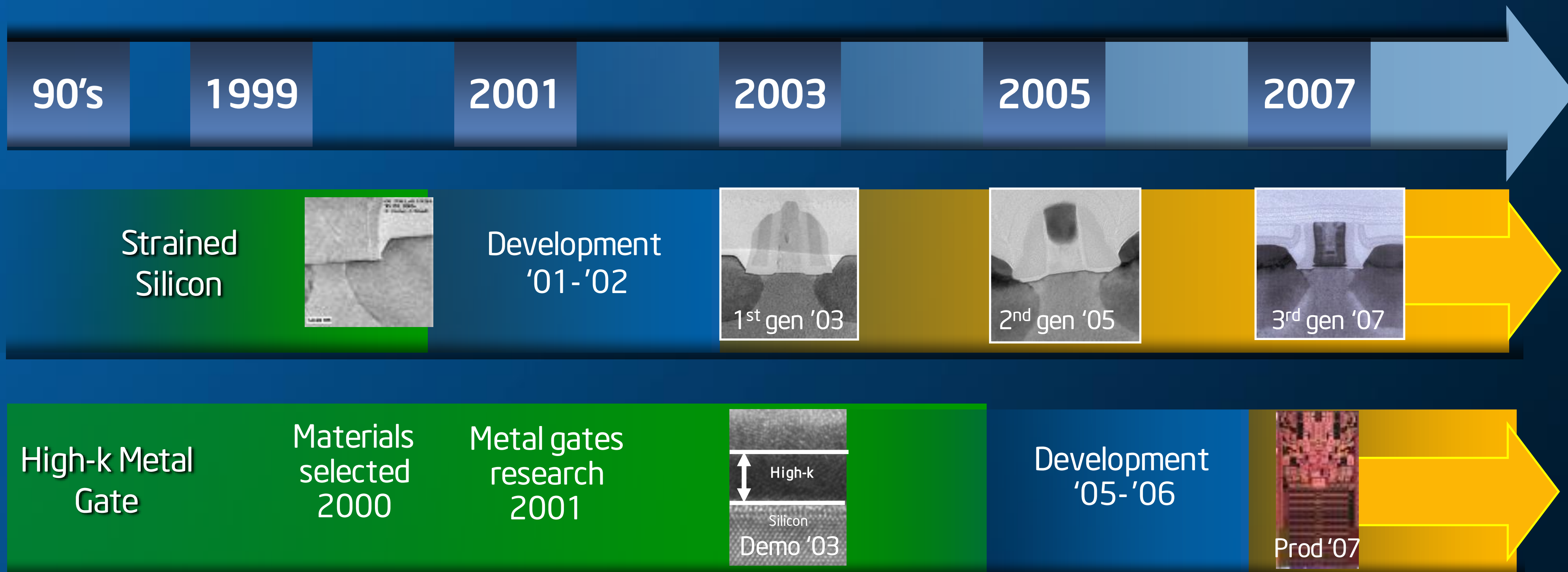
Performance tests/ratings are provided assuming specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. This data may vary from other material generated for specific marketing requests.

Small Computing Segment Needs More and More Performance At Low Power



Source: Intel Investor Meeting 2009

The Timing of Research Is Not Always Predictable



But a Commitment to Research is Required

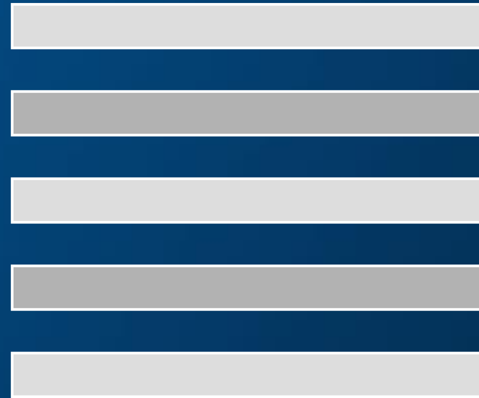
Source: Intel

Lithography Options for Beyond 32 nm

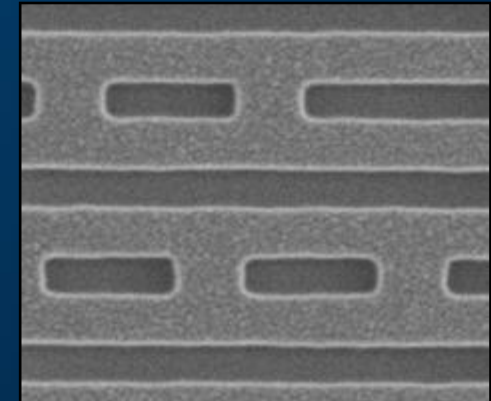
Double Patterning

- Pitch doubling
- Improved 2-D features

Pitch Doubling



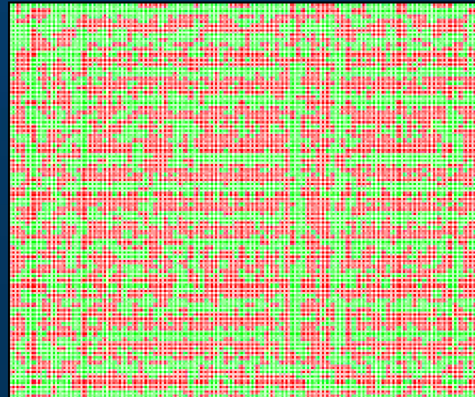
2-D Features



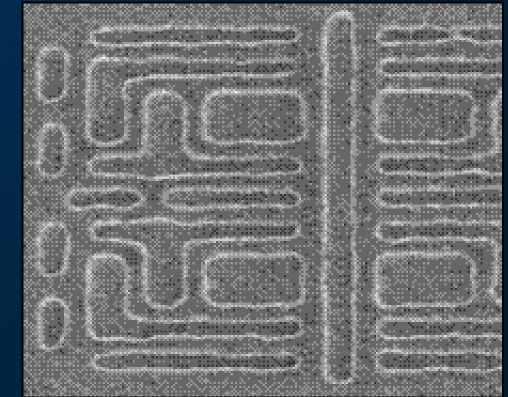
Computational Lithography

- Pixilated mask
- Existing 193 nm litho tools

Pixilated Mask



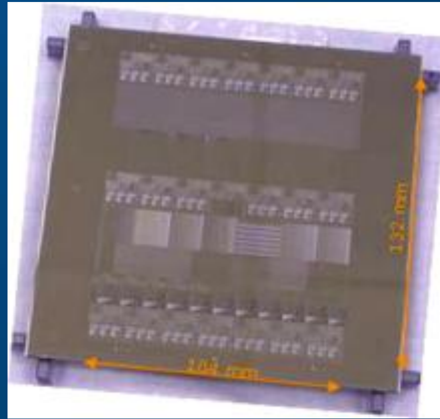
Printed Image

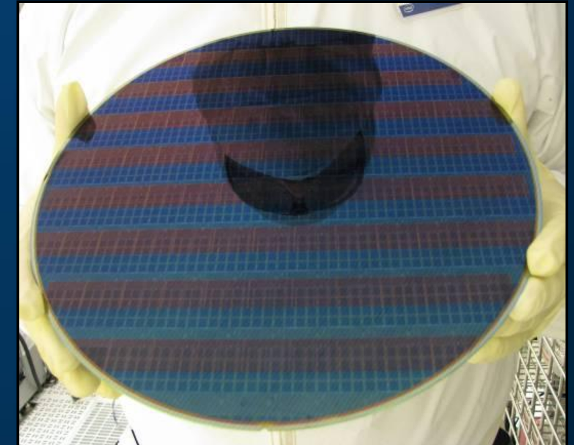


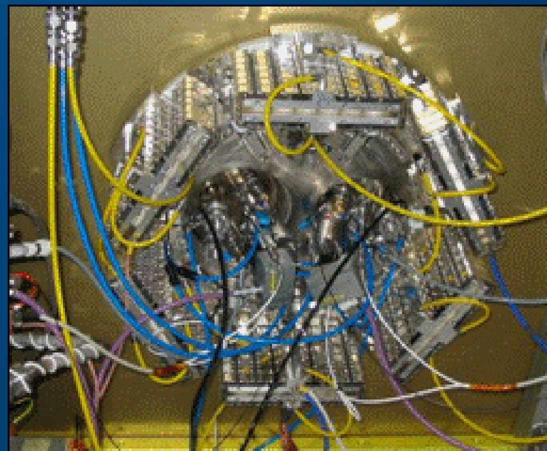
Source: M. Bohr, paper 1.3, ISSCC'09

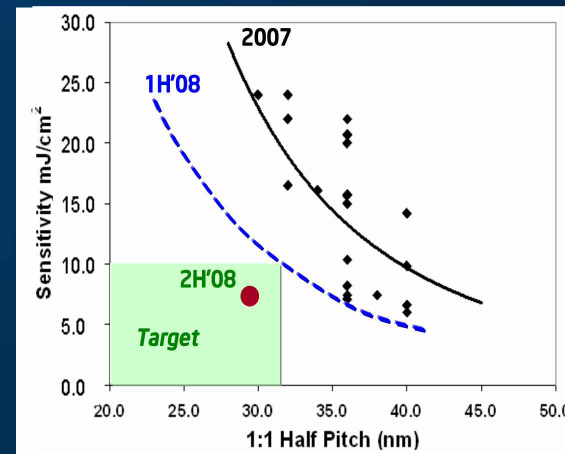
Extreme Ultraviolet Lithography

Cymer beta source


Intel EUV Mask


ASML ADT printed wafer


Philips beta source

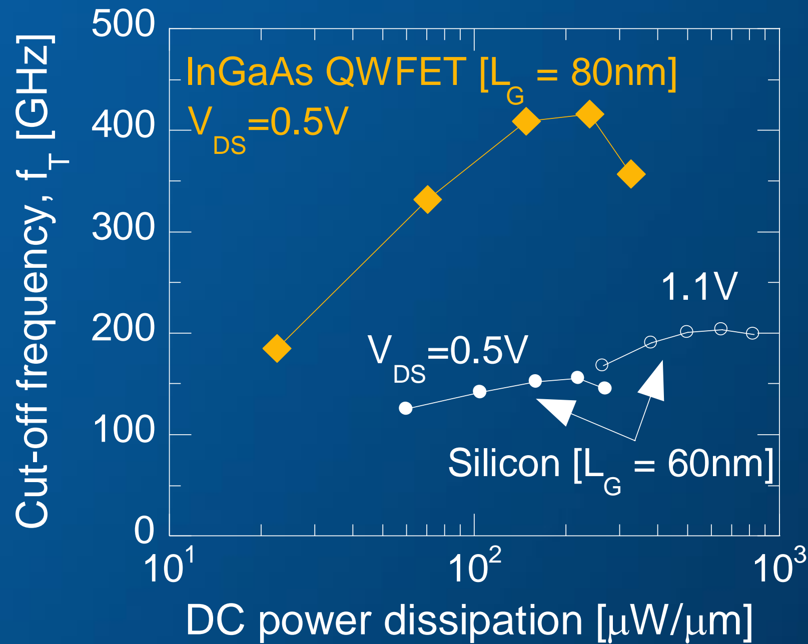


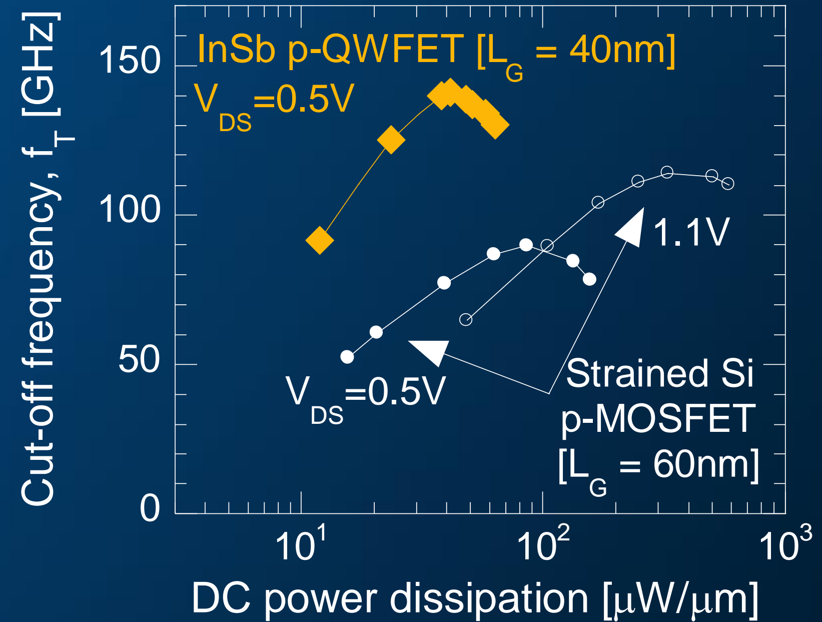
Photoresist Development

Continued progress towards EUV implementation

Source: M. Bohr, paper 1.3, ISSCC'09

III-V Transistor Options





InGaAs NMOS QWFET

Peak f_T > 400GHz at Vcc = 0.5V

InSb PMOS QWFET

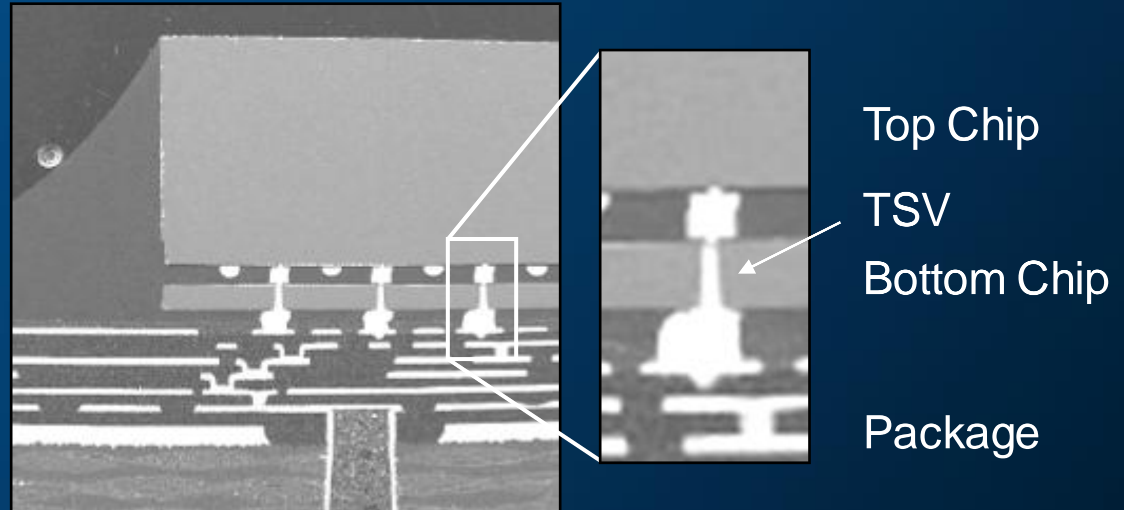
Peak f_T > 140 GHz at Vcc = -0.5V

III-V materials for improved performance at low voltage

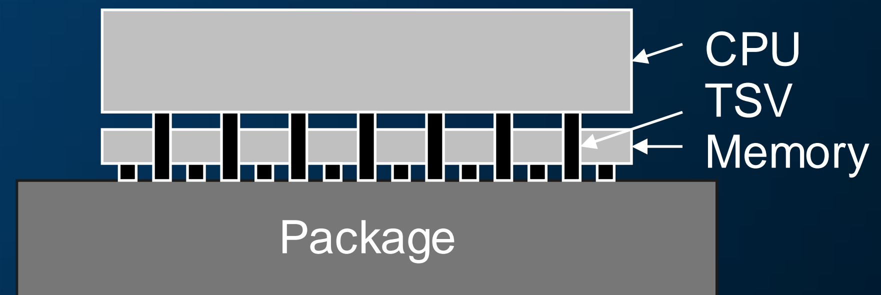
Source: M. Bohr, paper 1.3, ISSCC'09

3-D Chip Stacking

+ High density chip-chip connections
+ Small form factor
+ Combine dissimilar technologies



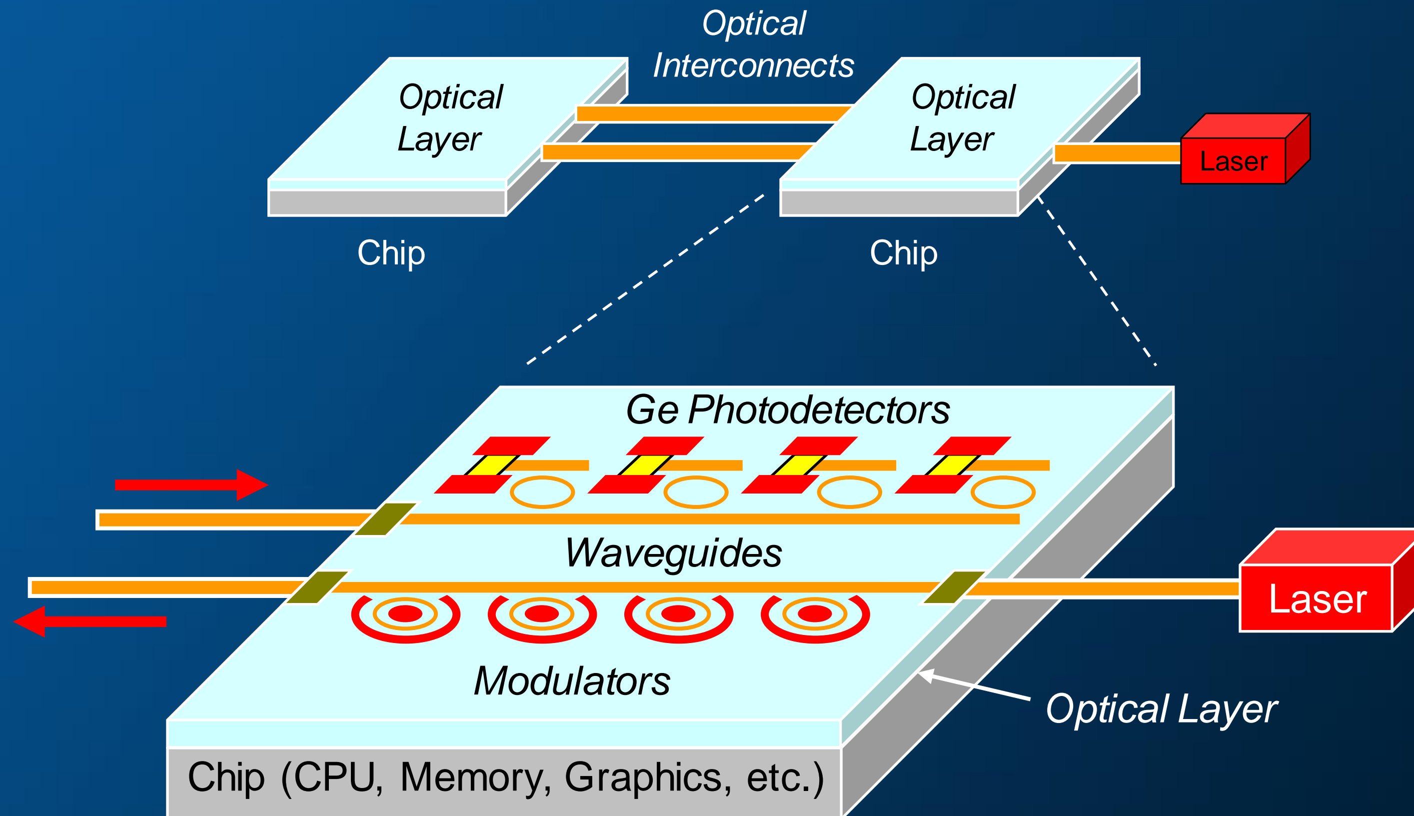
? Added cost
? Degraded power delivery, heat sinking
? Area impact on lower chip



3-D chip stacking using through-silicon vias

Source: M. Bohr, paper 1.3, ISSCC'09

Optical Interconnects

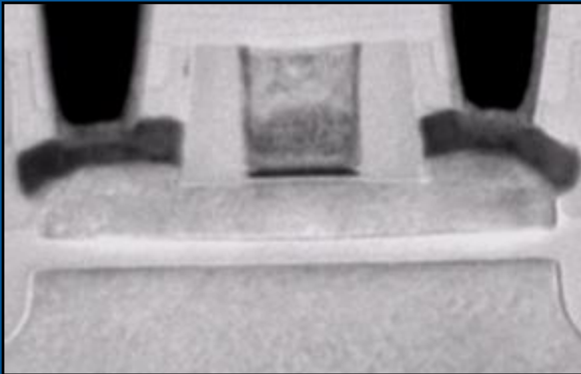


Nearer term: High bandwidth chip-chip interconnects

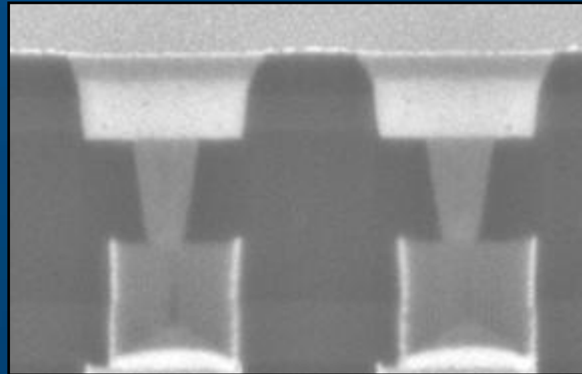
Longer term: On-chip interconnects

Ref. I. Young, paper 28.1, ISSCC '09

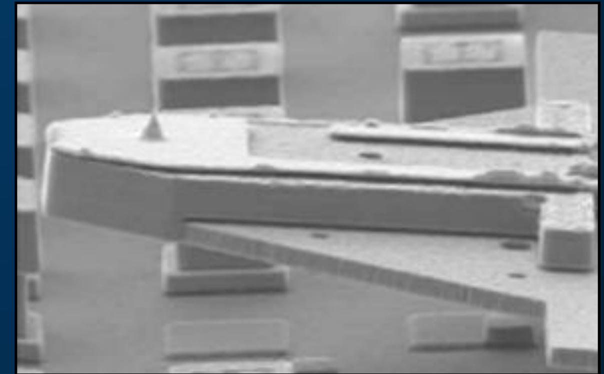
High Density Memory



Floating Body Cell



Phase Change Memory



Seek and Scan Probe

Dense memory increasingly important

Several novel directions being explored

Source: M. Bohr, paper 1.3, ISSCC'09

Discussion