A Guide to Help You Explore Intel's Eco-Technology Related Research Projects

Intel is researching a collection of technologies to help improve the environment. The first set of technologies improve how we monitor, analyze and track ongoing changes in our environment with the belief that better information will help communities consume less energy and lead to more effective environmental policies. Intel's second area of research is in advancements that significantly improve the energy efficiency of Intel-based products and systems. The result will be continuing improvements in performance but at dramatically reduced levels of energy consumption, thereby lessening the impact Intel platforms will have on our future environment.

New Research To Better Monitor Changes to Our Environment

Common Sense Environmental Sensing
Map location: H
Citizens are often motivated to seek information. The Common Sense team is developing prototypes of mobile environmental sensing platforms that empower individuals and communities to gather, analyze, and share information in order to influence environmental policy. We will present our prototype and the results of our current deployment on street sweepers in San Francisco.

Cascaded Silicon Raman Laser
Map location: H
In this exploratory research project, Intel achieved continuous lasing in silicon using the Raman effect. This breakthrough was recently published in the journal Nature Photonics. The cascaded silicon Raman laser's new sensing capabilities are demonstrated by measuring greenhouse gasses, methane gas and water vapor, to identify their molecular fingerprints. This demonstration establishes pathway to extending the laser wavelength into the mid-IR region for gas sensing and other important spectroscopy applications that are possible today only with complicated bulky, expensive or cryogenically cooled lasers. This research achievement could lead to silicon-based lasers that offer compactness and lower cost compared to current lasers used in a wide range of spectroscopy, sensing and medical applications.

Intel Product Enhancements to Make Technology More Energy Efficient:

Bredlow: Platform Power Management (PPM)
Map location: D
Platform power management is an area of research that redefines the behavior and power management of Intel platforms with the goal of significantly reducing power consumption. A key mechanism underpinning PPM is the continual monitoring of changes in platform operation and aggressively powering down portions of the system that are not in use. As an example, with straightforward changes to existing platforms we can demonstrate reductions in power of more

than 30%. In re-designed platforms of the future, we expect to reduce power consumption by 50% or more. PPM will benefit the full range of Intel products including ultra mobile, laptop, desktop, servers, and Tera-scale.

Ultra low voltage special-purpose video accelerator silicon demonstration
Map location: F
In order to improve performance/watt in future tera-scale as well as mobile architectures, Intel researchers are exploring circuits to accelerate key algorithms. We present Intel's first ultra-low voltage special-purpose video encoding accelerator implemented in 65nm CMOS. We show operation down to 0.22V, an energy-efficiency improvement up to 9.6X, and industry-leading performance/watt of 411 GOPS/W.

Energy Efficient Communication
Map location: D
This demo shows how our work on Energy Efficient Communication enables energy saving for both the wireless communication device as well as the overall platform. It demonstrates how the Wireless NIC converges very quickly to find an optimum on/off pattern for the current workload saving significant energy for the device, between 4 to 6 times for workloads like VoIP or video streaming, as well as the overall platform. Intel innovation: Firmware level algorithms selecting the optimum on/off time for the wireless device. 4-6x reduction of the communication device power without impacting the quality of service

Intel's 32nm Logic Process
Map location: J
As Intel ramps its 45nm logic process, future processes are under development. We will show progress on the 32nm process, which is due for initial production in 2009. The 32nm process continues Moore's Law by doubling transistor density compared to that at 45nm (as measured by SRAM cell size). It incorporates the 2nd generation of high-k/metal gate to further improve performance and performance per watt. And, it makes use of immersion lithography for patterning critical layers, a first for Intel. A functional 291 Mbit SRAM wafer will be part of the demo.

Increased data center density using power clamping
Map location: G
Today's servers in data centers are often constrained by power, resulting in limited rack density. However, individual servers are mostly underutilized. Taking advantage of hooks in Intel silicon, this technology provides a governor mechanism that clamps power consumption, allowing additional servers to be added to the rack while minimizing performance impact during normal operation. Additional benefits include continued operation during brown-out conditions.

DEMO ZONES

- A Intel Technology Journal and Press
- I Intel Library
- C Health
- D Mobility
- E Tech for Dev.Regions
- F Tera-Scale Computing
- G Enterprise
- H Exploratory
- J Silicon Research
- Energy Efficient and Green Demos

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