

The Invention of Uniaxial Strained Silicon Transistors at Intel

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All engineers are familiar with Murphy's Law, namely that if something can go wrong it will go wrong. All of us are familiar with experiments and projects that didn't work quite as expected, at least not the first time. Sometimes that's a good thing. Sometimes serendipity trumps Murphy's Law. Intel's invention of uniaxial strained silicon transistors had a serendipitous beginning after some early experiments didn't work quite as expected.

First some background on how Intel organizes research and development for our silicon process technologies. Portland Technology Development is the organization within Intel that is responsible for developing logic technologies for microprocessor products. PTD is located in Hillsboro, Oregon. PTD is responsible for deciding what process features go into any new logic generation, then putting the technology elements together to make a working process flow, and then finally running the process in a medium-volume manufacturing mode before transferring to high volume manufacturing fabs. Also located at the same Hillsboro site is Intel's Components Research group. CR is responsible for exploring novel technology options several years before they might be used in manufacturing. Some of CR's ideas are adopted by the PTD organization as they decide the features to be used in a new generation of process technology. To ensure that there is an effective handoff of new technology options from CR to PTD, members of each group work together in a temporary organization for a given technology generation called Pathfinding. This whole cycle of Research-Pathfinding-Development-Manufacturing is referred to as Intel's Silicon R&D pipeline and has been a successful model for introducing new generations of process technology on regular two year intervals since the mid-1990's.

The history behind Intel's invention of uniaxial strained silicon transistors starts in the 1990s when Robert Chau's transistor research team in CR was exploring the use of selectively deposited SiGe films in PMOS source-drains as a means to reduce parasitic source-drain resistance. Anand Murthy from our thin films group worked for Robert and he was responsible for developing SiGe deposition techniques. They expected that lower source-drain resistance could be achieved with SiGe because boron can have higher dopant activation levels in SiGe than in Si. By 1999 their SiGe PMOS transistors were demonstrating increased drive current and they knew they were on to something.

In 1999 engineers from PTD joined together with CR engineers and formed a Pathfinding group chartered to identify promising transistor features for Intel's 90 nm generation logic technology. Tahir Ghani and Kaizad Mistry joined me in that combined CR + PTD Pathfinding group to explore transistor options. SiGe source-drain experiments were continued and refined. Like all good transistor engineers we attempted to do careful modeling of these SiGe PMOS transistors, but our early models did not

match the experimental results. Drive currents were higher than what models predicted, at least for models that comprehended improvements in boron activation in source-drain regions. Something about these PMOS transistors was not quite as expected, and our device and TCAD engineers wouldn't rest until we had an explanation. After considerable discussion and experimentation, we concluded that the SiGe source-drains create uniaxial compressive strain in channel regions, which would improve hole mobility and increase drive current.

But what about NMOS transistors? Selective SiGe was a great idea for PMOS because it provided two performance benefits: increased boron dopant activation and uniaxial compressive strain. But SiGe does not help N+ dopant activation the way it helps P+ activation, and uniaxial compressive strain does not improve electron mobility for NMOS transistors, which want uniaxial tensile strain. Intel's 0.13 um logic technology uses a Si₃N₄ etch stop layer, essentially a capping layer deposited on top of transistors before contacts are formed, which induces some strain in the channel of NMOS transistors. By 1999, however, we had learned that increasing the thickness of the Si₃N₄ etch stop layer creates more tensile strain which increases NMOS drive current by ~10%. Again our modeling work proved to us that the effect was due to uniaxial tensile strain being formed in transistor channels, which increased electron mobility and increased NMOS drive current. Although this discovery was felt to be too late to implement in our 0.13 um technology by increasing the thickness of the Si₃N₄ etch stop layer used in the process, the Pathfinding group realized it was a great option for the 90 nm NMOS transistors.

The general effects of strain on electron and hole mobility in silicon have been known for decades, but no practical process had yet been identified for implementing strain on modern CMOS technologies. During the late 1990's a form of strain known as biaxial strain was being explored by several groups in the industry. Biaxial strain stretches silicon atoms in the transistor channel in both X and Y dimensions, while uniaxial strain stretches the atoms only in the X direction, the direction orthogonal to the gate layout direction. Biaxial strain can be created by depositing a relatively thick blanket layer of SiGe on an unpatterned wafer, followed by depositing a thin layer of Si, which is then biaxially strained due to the lattice mismatch between Si and SiGe. The difference between biaxial and uniaxial strain techniques is illustrated in Figure 1. The biaxial and uniaxial forms of strain have also been referred to as global and local strain respectively. The biaxial approach does not provide much PMOS drive current increase and suffers from several process problems that have prevented it from being adopted in a high volume manufacturing process. Intel's 90 nm Pathfinding group considered the biaxial strain approach, but the uniaxial strain process was appearing to be both more effective for improving performance and easier to manufacture.

2001 was the year we had to make commitments on key features to be used on our 90 nm transistors. During the first half of that year we were performing experiments that combined SiGe strained PMOS transistors with Si₃N₄ strained NMOS transistors. Our experiments were demonstrating impressive transistor performance and SRAM test chips were demonstrating the first yield results. By the middle of 2001 we were convinced that

uniaxial strained silicon transistors would work in volume manufacturing and we committed our 90 nm process to that approach. Around this point Scott Thompson joined the team after wrapping up his 0.13 μm transistor development responsibilities. By early 2002 he became the 90 nm program manager and was responsible for getting strained silicon transistors along with copper plus low-k interconnects to meet performance, yield and reliability requirements in time for the first product shipments in 2003.

The next year entailed demonstrating transistors and interconnects at the final 90 nm design rules. The process was in its full development mode and the team's focus was on improving performance, yield and reliability on 52 Mb SRAM test chips in preparation for the microprocessor products that would come in 2003. The first paper on our 90 nm process was presented by Scott Thompson at the International Electron Devices Meeting in December of 2002 [1]. This paper described many aspects of our 90 nm transistors and interconnects and showed industry-leading transistor drive currents, but although the paper mentioned the use of strained silicon transistors, we did not describe the unique uniaxial process technique for competitive reasons. That disclosure was saved for December of 2003 when Tahir Ghani presented a late paper at the International Electron Devices Meeting [2], and again by Kaizad Mistry at the Symposium on VLSI Technology in June of 2004 [3]. Pictures of Intel's 90 nm strained silicon transistors are shown in Figure 2. Uniaxial strain increased NMOS performance by >10% and PMOS performance by >25% on our 90 nm technology, or provided >4x leakage power reduction. Intel enhanced the uniaxial strain technique on our subsequent 65 nm technology in 2004 for even more performance gain [4]. Solving all the integration, yield and manufacturing issues with a new material like SiGe was quite a challenge, but is something that Intel's Portland Technology Development group excels at. SiGe + Si₃N₄ uniaxial strained silicon transistors proved to not only be very successful for Intel, but now virtually every major semiconductor company has published a paper showing plans to copy this technique on their future logic technologies.

REFERENCES

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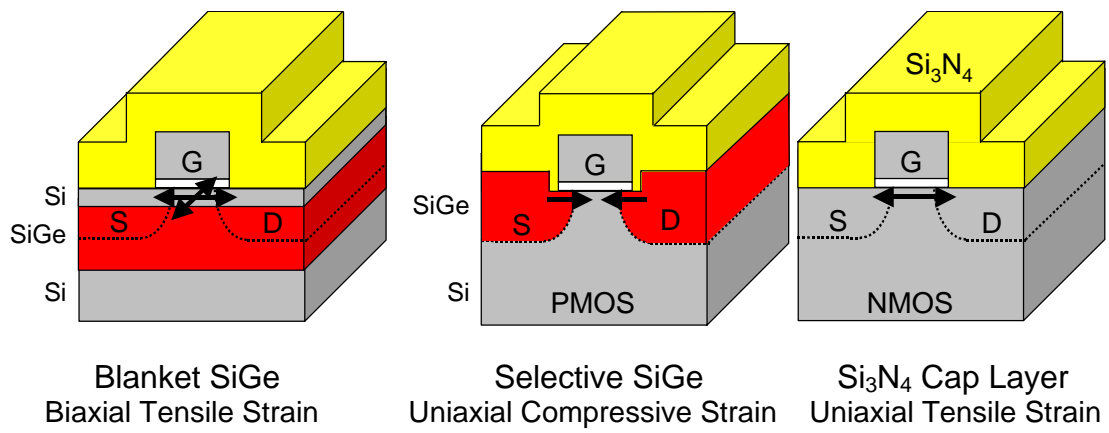


Figure 1 - Biaxial (left) vs. Uniaxial (right) Strain Techniques

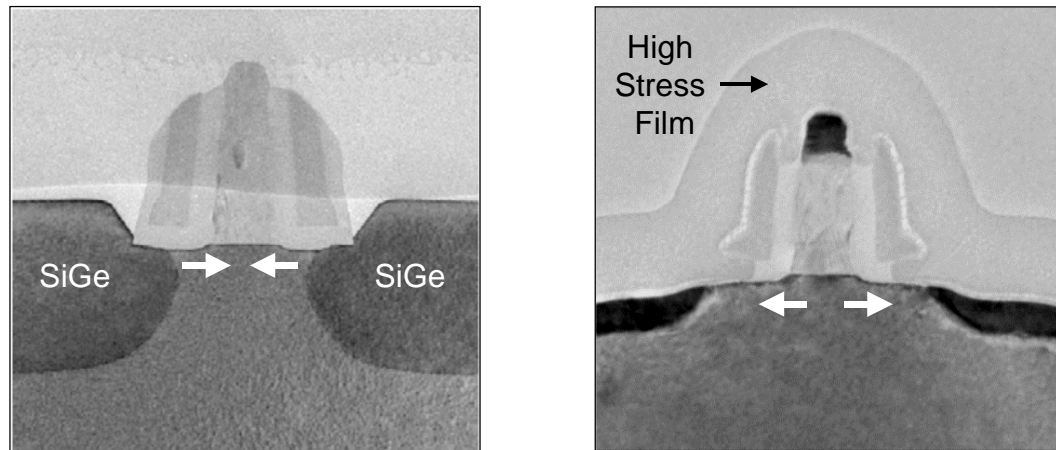


Figure 2 - Intel 90 nm PMOS (left) and NMOS (right) Strained Silicon Transistors