



## Intel® Xeon Phi™ coprocessors What Software Partners are Saying

Quotes as of November 2012

*"TACC is excited about providing Stampede to the open science community as one of the most powerful computing systems in the world. We are especially proud to debut the new Intel® MIC Architecture at large scale, and look forward to working with researchers to harness its capabilities. With its underlying x86 architecture and support of common parallel programming standards, we expect users to be able to achieve tremendous performance using Stampede's Intel® Xeon® Processors and Intel® Xeon Phi™ coprocessors using a variety of programming approaches. This familiarity and flexibility will accelerate porting and optimization for Intel MIC Architecture, enabling users to take advantage of Stampede's tremendous performance potential relatively quickly. We expect many new scientific discoveries early in 2013 from our talented users, made possible by Stampede."*

**Jay Boisseau, director, Texas Advanced Computing Center at The University of Texas at Austin**

*"Sandia's pre-production Intel® Xeon Phi™ coprocessor testbeds have explored architectural features that could impact exascale computing for our mission-critical programming models and algorithmic configurations. The programming models available for the Intel MIC Architecture are open-standard and portable between traditional processors and Intel Xeon Phi coprocessors. This should allow us to leverage code development across multiple platforms. Although further work remains to fully exploit the raw performance of the architecture throughout our broad application portfolio, we expect Intel's comprehensive software development environment — including compilers, libraries, profilers and debuggers — to help."*

**James A. Ang, Ph.D., Extreme-scale Computing, Sandia National Laboratories**

*"Having ported a variety of important scientific codes to Intel® Xeon Phi™ coprocessors, NICS can attest to the relative ease in exploiting these computational resources without resorting to redevelopment. The potential to easily port applications to Intel Xeon Phi coprocessors represents a significant leap ahead in developer productivity and performance. The Intel Xeon Phi coprocessor architecture provides truly impressive performance through familiar programming models and tools. Its energy efficiency demonstrates that high performance operation can be obtained even with power constraints."*

**Greg Peterson, Director, National Institute for Computational Sciences**

*"The Intel® Xeon Phi™ coprocessor seems so painless compared to GPUs. I would also say that this chip seems the most promising in terms of technology for the next generation of supercomputers."*

**Homa Karimabadi, Space Physics Group Leader, University of California, San Diego**

*"We have really enjoyed exploring and testing the performance capabilities of the Intel® Xeon Phi™ coprocessor. The integrated Intel tool chain allowed us to take code written for Intel® Xeon® processors and execute on the coprocessors with minimal to no changes — this Intel Xeon Phi coprocessor capability is extremely important to integrating alternative compute devices in our environment. We have seen impressive results on large matrix tests and it's clear that the compute capabilities have jumped. We look forward to working with Intel and exploring this technology further."*

**John Shafae, Director - HPC R&D, UBS CTO Innovation Team**



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*“We are very encouraged by the up to 2.53x performance gains on prestack depth migration using Intel® Xeon Phi™ coprocessors. We accomplished this using the same programming models, Intel® MKL DFT routines, and source code as runs on Intel® Xeon® processors. Using MPI, we also demonstrated the ability to scale up performance with two nodes that each have two coprocessors, to 10x compared to a host node without coprocessors. This will provide an amazing boost for the performance of the Sinopec iCluster\* seismic imaging system.”*

**Zhao Gaishan, VP of Sinopec Geophysical Research Institute**

*“With the amazing capabilities of the latest supercomputing coprocessors such as the Intel® Xeon Phi™ coprocessor, it’s vital to make it as simple as possible to integrate them into existing supercomputers. The latest iteration of Moab was designed to maximize the investment being made by today’s HPC providers.”*

**Robert Clyde, CEO of Adaptive Computing**

*“As part of our commitment to providing the high performance computing (HPC) market with software tools and components for the most advanced hardware, Rogue Wave has invested significant R&D resources to include the Intel® Xeon Phi™ coprocessor support in our strategic software development products. Thanks to our close relationship with Intel and participation in the early testing program, Rogue Wave has been able to quickly advance our portfolio of products to support the Intel Xeon Phi coprocessor, which will give developers the tools and components they need to fully leverage its computational power in their applications.”*

**Scott Lasica, VP of Products & Alliances at Rogue Wave**

*“ScaleMP has been working with Intel for many years. We are very excited to be able to offer our customers support for the Intel True Scale Fabric Host Adapter which will enable the high performance they expect. In addition, by allowing developers and customers the ability to run their existing applications on the Intel® Xeon Phi™ coprocessor transparently through virtualization, we are enabling ISV’s to develop and optimize extremely powerful applications.”*

**Shai Fultheim, CEO and founder of ScaleMP**

*“Hybrid architectures such as those built with Intel Xeon Phi coprocessors are clearly at the forefront of creating High Performance Computing (HPC) systems. They allow for responding to challenges such as scalability, energy consumption and cost effectiveness. Customers will, however, only be able to take full advantage of the benefits offered by Intel® Xeon Phi™ coprocessors if access to these critical resources is well managed and seamlessly integrated with the workload and resource management software orchestrating the workflow through the HPC system. This is exactly what we are able to provide with our integration of Intel Xeon Phi coprocessors with Univa Grid Engine and why it will be a key differentiator for Intel Xeon Phi coprocessor users.”*

**Fritz Ferstl, CTO of Univa Corporation.**

*“With the ongoing standardization effort in the directive-based programming such as OpenMP for accelerators, we believe our customers will be able to keep their legacy codes portable across those architectures. By using these tools, our customers can easily accelerate their use of manycore architectures.”*

**François Bodin, CAPS CTO**



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*“Accelrys, in partnership with Intel is investigating the high performance that the new Intel® Xeon Phi™ coprocessor provides for computing intensive codes like CASTEP. What has impressed us is not only the raw power this system provides for increasing scale and scope of computation, but how quickly and easily our engineers can adapt existing codes like CASTEP to take advantage of this system. This was possible because of the common architecture, programming language and tools with Intel® Xeon® processors. We look forward to using this approach and advanced architecture, in a number of our technical and scientific applications for both Life and Materials Science and Engineering applications.”*

**Michael Doyle, Ph.D., Director of Product Marketing & Principal Scientist, Accelrys**

*“ETI's SWARM technology is a parallel computing framework for multi-core/multi-node systems. SWARM is a dynamic adaptive runtime system that minimizes user exposure to physical parallelism and system complexity. It is designed to improve scalability, efficiency, and programmability on many-core architectures by utilizing a dynamic, event-driven model of execution instead of the fork-join or bulk-synchronous methods of conventional programming models. We are pleased to announce that Intel® Xeon Phi™ coprocessors will be supported utilizing the SWARM technology adding to the breath of our solution for multi-core/multi-node systems. Intel Xeon Phi coprocessors enable many exciting applications; in one early example, we are seeing a noticeable boost in the performance of computationally-intensive kernels of wave migration solutions that are vital to our partners in the energy field to develop highly complex structural imaging.”*

**Rishi Khan, Vice President of Research and Development, ET International**

*“We are extremely pleased to have achieved a significant 3.46x speedup in only a matter of 3 days. The programmability of the Intel® Xeon Phi™ coprocessor helps us to accelerate our developer's work in designing building blocks for applications, and the performance benefits the research of our customers in studying the properties of novel materials and complex atomic systems.”*

**Dr. Thomas Steinke, Konrad-Zuse-Zentrum für Informationstechnik Berlin**

*“With the improved processing made possible with Intel® Xeon Phi™ and PBS Professional, users of applications like RADIOSS can explore complex simulations and real-world design scenarios.”*

**Sam Mahalingam, Senior VP of Software Development at Altair**

*“Altair PBS Professional is one of the first workload management products to support Intel® Xeon Phi™ coprocessors out of the box. At the Intel Xeon Phi coprocessor launch, we will offer a new toolkit that automates the configuration for the coprocessor within PBS Professional. With our support for Intel Xeon Phi coprocessors, including the simplified configuration toolkit, we are ensuring our users can run some of the most compute-intensive portions of their work on the most cutting-edge, high-performance architecture available.”*

**Bill Nitzberg, CTO for PBS Works at Altair**

*“This is the first time we have been able to port the entire RADIOSS explicit code on a coprocessor or accelerator, and we are excited about the performance potential. The porting process was easy, since we were able to use tools we were already familiar with from Intel® Xeon® processor development.”*

**Eric Lequiniou, Director of High Performance Computing at Altair**



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*“HPC users adopting Intel® Xeon Phi™ coprocessors will have a clear eye on the performance ball, and to get the most out of the hardware they have to know where to parallelize and where to offload computation. The Allinea MAP profiler is a scalable tool that drills down to the source to shows instantly where real bottlenecks are. The level of integration between Allinea DDT and Allinea MAP - with one consistent development environment - will be a unique and powerful enabler for HPC software developers.*

*“In releasing the Allinea DDT debugger with support for the Intel® Xeon Phi™ coprocessor today, users adapting their code will be able to fix software problems quickly - essential to any effective software project. Allinea DDT is ready to debug on this platform from the very start – from one node through to Petascale and beyond.”*

**Dr David Lecomber, CTO of Allinea Software**

*"At AccelerEyes, we've found that porting the ArrayFire library to OpenCL on the Intel® Xeon Phi™ coprocessor was refreshingly simple. We are very pleased with the new opportunity afforded by the Intel Xeon Phi coprocessor and anticipate ArrayFire as a software companion for many defense, energy, life sciences, financial computing, and traditional HPC codes."*

**John Melonakos, CEO, AccelerEyes**

*“We package everything that's necessary to get the Intel® Xeon Phi™ coprocessor to work. Getting your software environment completely right is normally a tedious challenge. With Bright it will work out of the box. We have also introduced a 'MICHost' role which can be assigned to nodes that are hosting one or multiple coprocessors. It allows some features to be configured, and it will control the services that need to be running on the machine that hosts the coprocessor. Bright users will be able to make the most of their Intel Xeon Phi coprocessor investment.”*

**Martijn de Vries, CTO at Bright Computing**

*"The computational demands of large scale lattice QCD simulations can only be satisfied by massively parallel machines. This is why we looked into the Intel® Many Integrated Core (MIC) architecture and selected Intel® Xeon Phi™ coprocessors for our next generation QPACE supercomputer. One of our most important application codes - BQCD - compiled out of the box, and we were delighted to see an immediate speed-up of over 1.5x when a single Intel Xeon Phi coprocessor card was added to every node of a cluster containing 2 sockets of the Intel® Xeon® processor E5-2670 per node. We are confident that larger speed-ups will be obtained in the future with modest modifications of the code. The Intel Xeon Phi coprocessor will greatly reduce our time to solution on QPACE II."*

**Prof. Dr. Tilo Wettig, Principal Investigator of the QPACE project**



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*“Dense linear algebra is a cornerstone for many HPC applications and MAGMA. Optimized algorithms and frameworks are what we focus on and we are excited about the ease of programming and performance of the Intel® Xeon Phi™ family as we move forward in our development efforts to support it within MAGMA.”*

**Jack Dongarra, University Distinguished Professor, Director – Innovative Computing Laboratory, Director – Center for Information Technology Research, University of Tennessee**

*“Interest in Intel® Xeon Phi™ within our customer base is strong and growing. Our work to develop a version of our numerical libraries for it is on track, and we look forward to making a beta version available shortly.”*

**Mike Dewar, CTO, NAG**

*“With the advancement of manycore processor architectures and their realization in next-generation products comes the key need for tools that can identify areas for tuning for maximum performance. ParaTools, Inc. (in association with the TAU Project at the University of Oregon) is pleased to announce support for the Intel® Xeon Phi™ coprocessors in the TAU Performance System®.”*

**ParaTools, Inc., Prof. Allen D. Malony, Professor, Dept. of CIS and Director, NIC, U. Oregon, CEO and Director, ParaTools, Inc.**

*“IBM is continuing our relationship with Intel through the integration of IBM Platform Computing management software and the Intel Xeon Phi architecture. IBM Platform LSF and IBM Platform HPC users will be able to intelligently allocate application workload to Intel® Xeon Phi™ coprocessors, leveraging its many core capabilities to accelerate performance.”*

**Dr. William Lu, Global Product Manager, IBM Platform Computing.**