Enabling Breakthroughs In Technology

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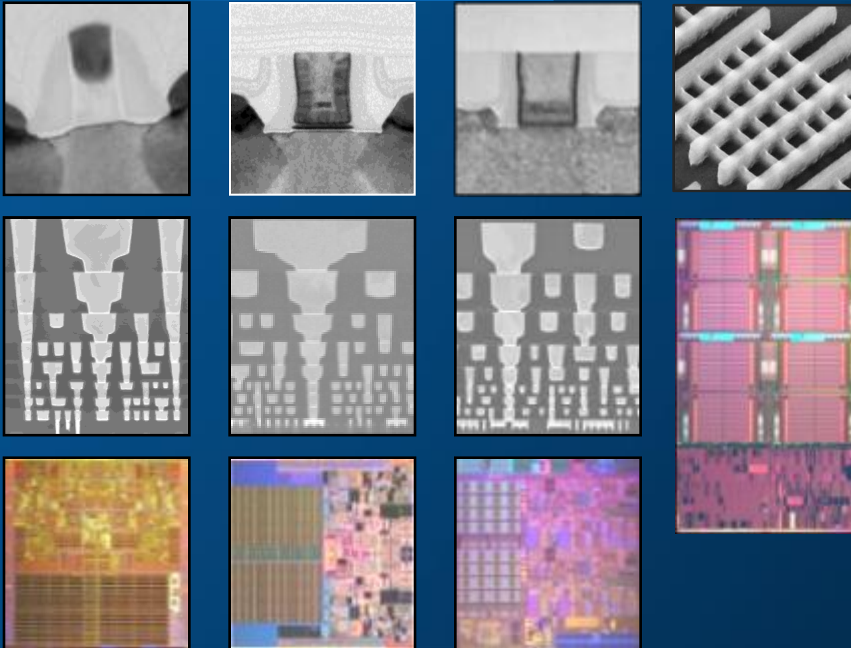
Enabling a Steady Technology Cadence

TECHNOLOGY GENERATION

65nm	45nm	32nm	22nm	14nm	10nm	7nm	Beyond
2005	2007	2009	2011	2013	2015	2017	2020

MANUFACTURING — DEVELOPMENT — RESEARCH



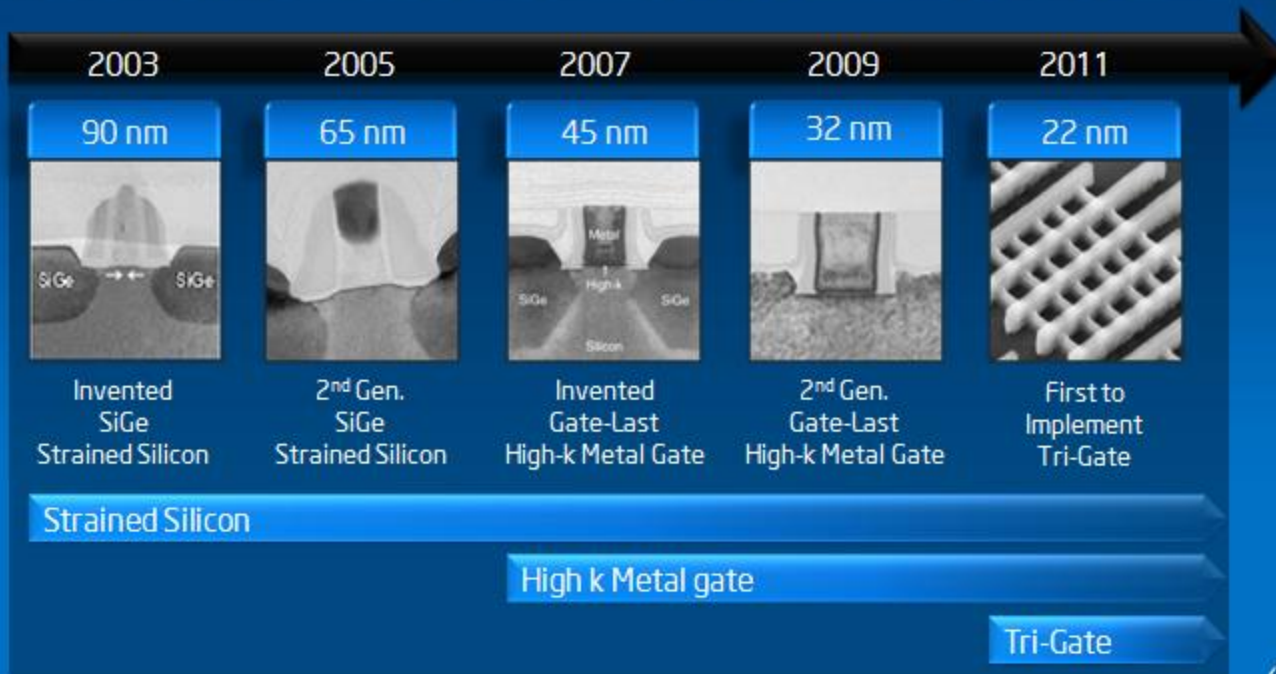
Defined | To be defined

What to do now to enable these future generations ?

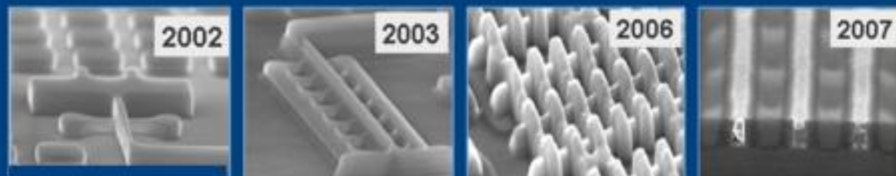
Not to scale

But first
some old technology …

Transistor Innovations Enable Technology Cadence



Tri-Gate Invented



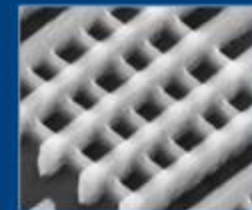
Single-fin transistor demonstrated

Multi-fin transistor demonstrated

Tri-gate SRAM cells demonstrated

Tri-gate RMG process flow developed

Tri-Gate Selected for 22nm node



Tri-gate optimized for HVM

Tri-Gate Mfg

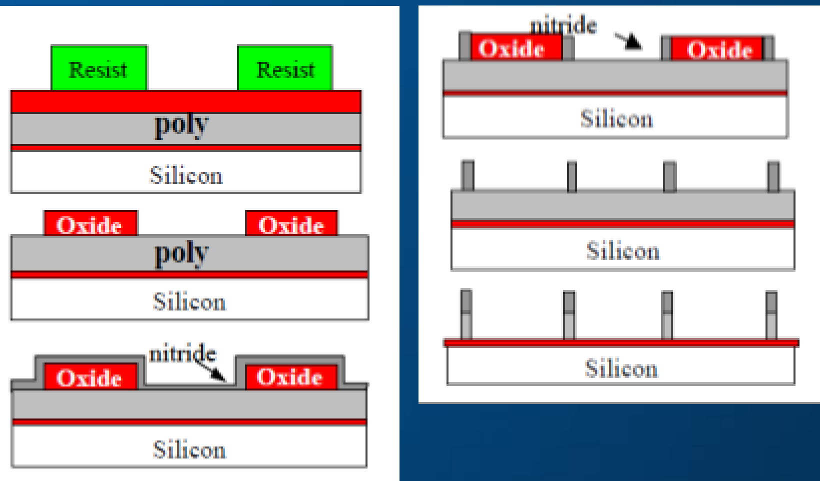
Exploration – late 90's

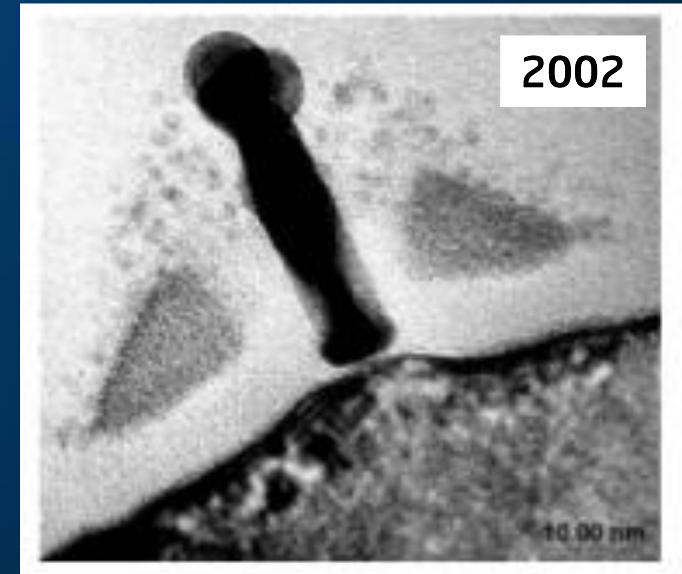
- Talk of 0.1um as the end due to leakage power
- 248nm lithography limited device exploration

Then enabled

- Creation of sub-resolution features
- Study of dense patterns (later)

1997 Intel Invention
Spacer based pattern





Intel: 10nm planar transistor

Exploration was not limited by lithography

Exploration – late 90's

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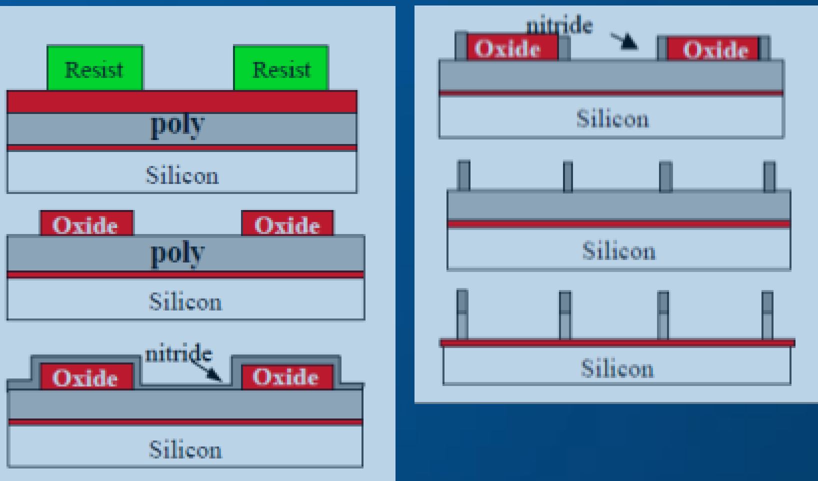
- 248nm lithography limited device exploration

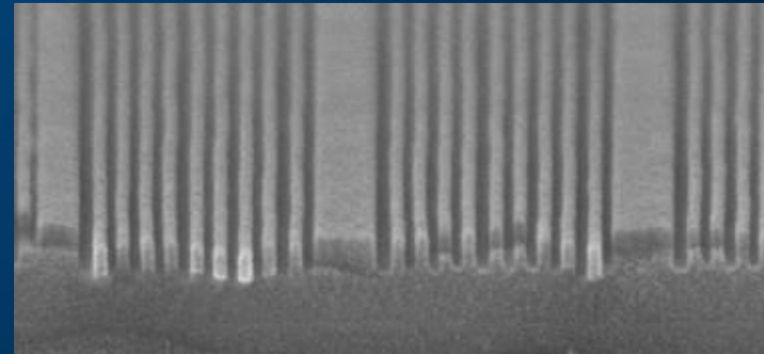
1997 Intel Invention
Spacer based pattern

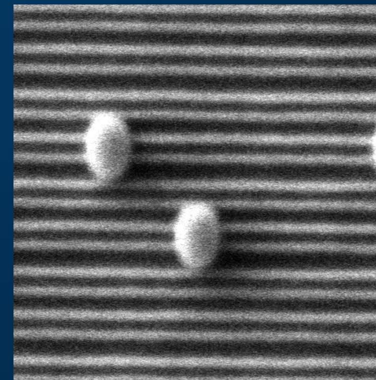


Exploration today

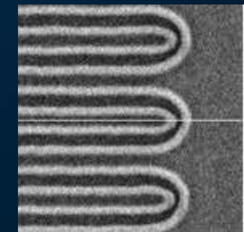
193 immersion lithography
+ Spacer based pattern twice

Pitch Quartering with
193i, 16nm features





Scalable to
Sub 10nm features



Exploration (still) not limited by lithography

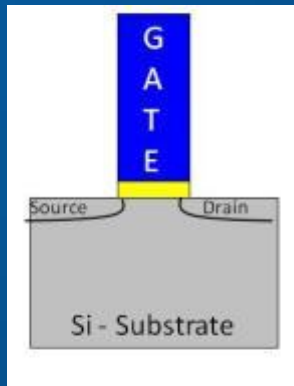
Evaluation – early 00's

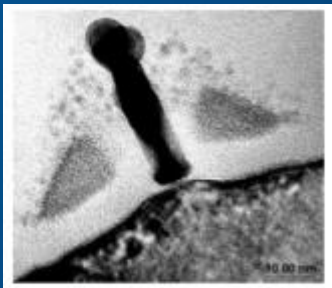
- 15 yrs discussion of possible non-planar device concepts
- No systematic scaling studies

Then enabled

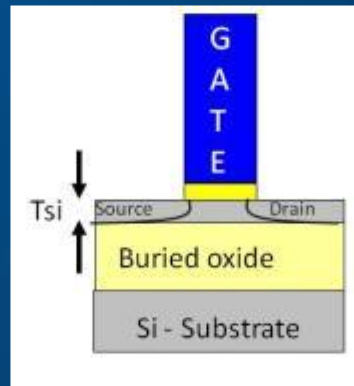
- Assessment of scaling challenges and critical parameters
- Focus for optimization

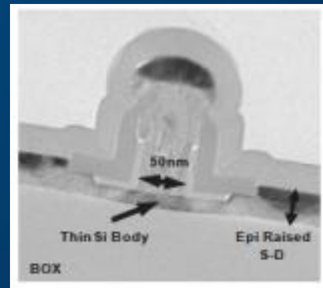
Planar



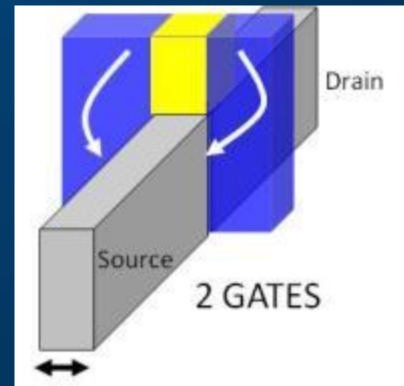


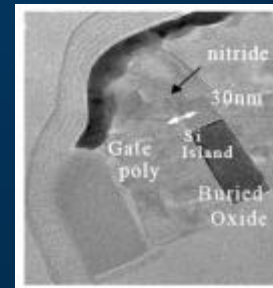
Thin body SOI



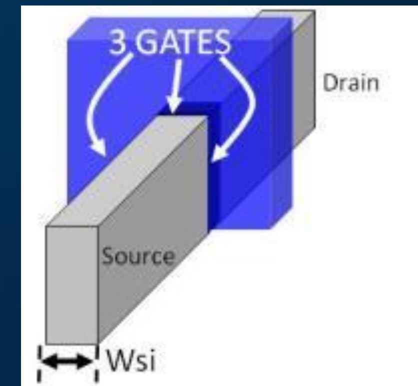


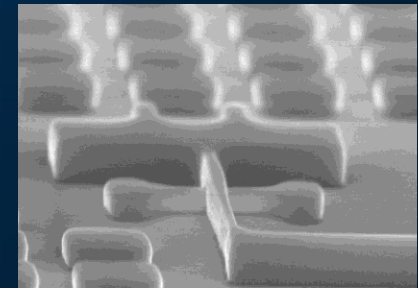
FinFET on SOI





Trigate on SOI





Build all variations and compare

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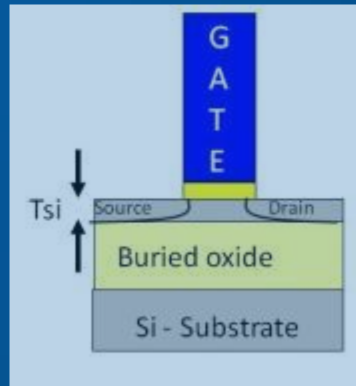
Evaluation – early 00's

- 15 yrs discussion of possible non-planar device concepts
- No systematic scaling studies

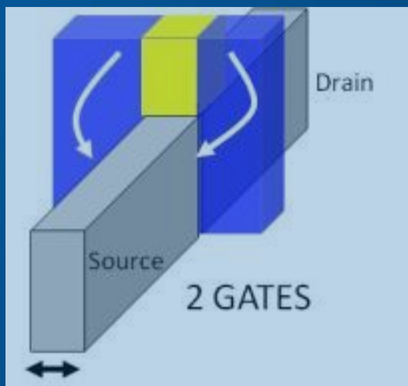
Evaluation today

- Assessment of scaling challenges and critical parameters for III-V

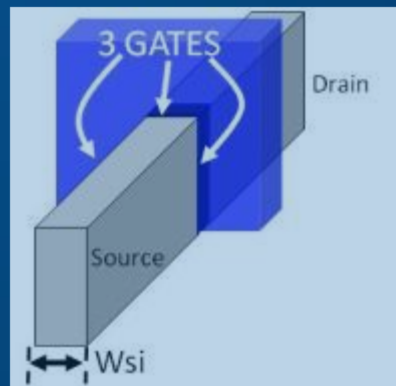
Thin body SOI



FinFET on SOI



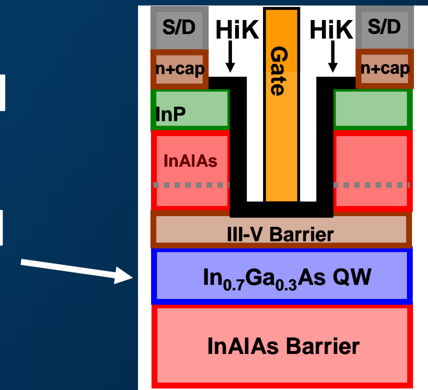
Trigate on SOI



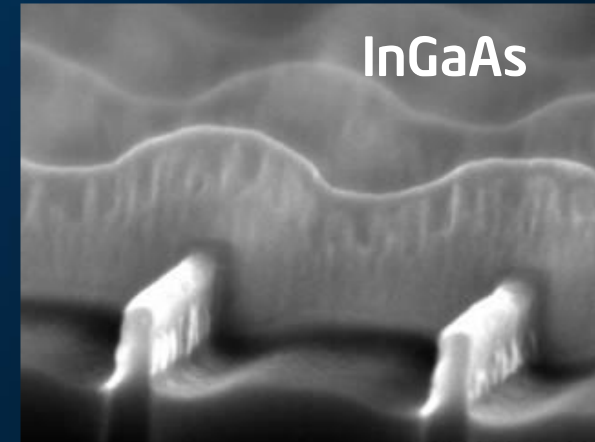
Quantum Well

equivalent to

Thin body SOI



3D devices



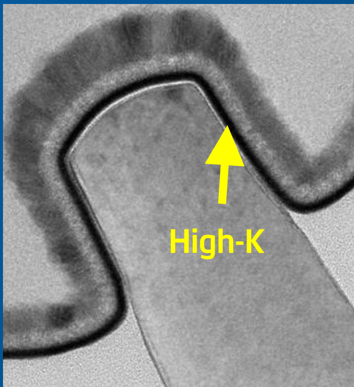
intel

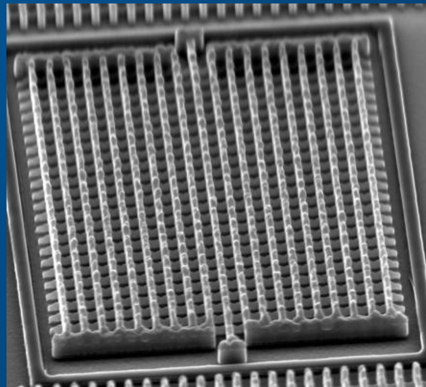
Integration – mid 00's

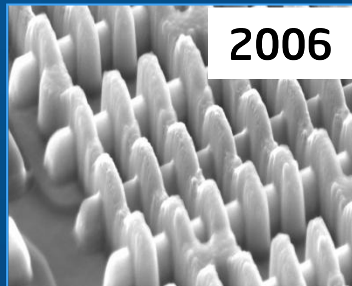
- Move to bulk silicon (cost)
- Catch up to planar for high k/metal gate + strain
- Create working CMOS

Then enabled

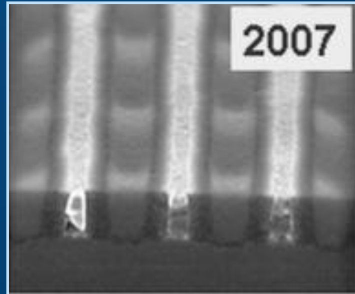
- Quality decision to adopt
- Development roadmap
- Lots more work !!!!



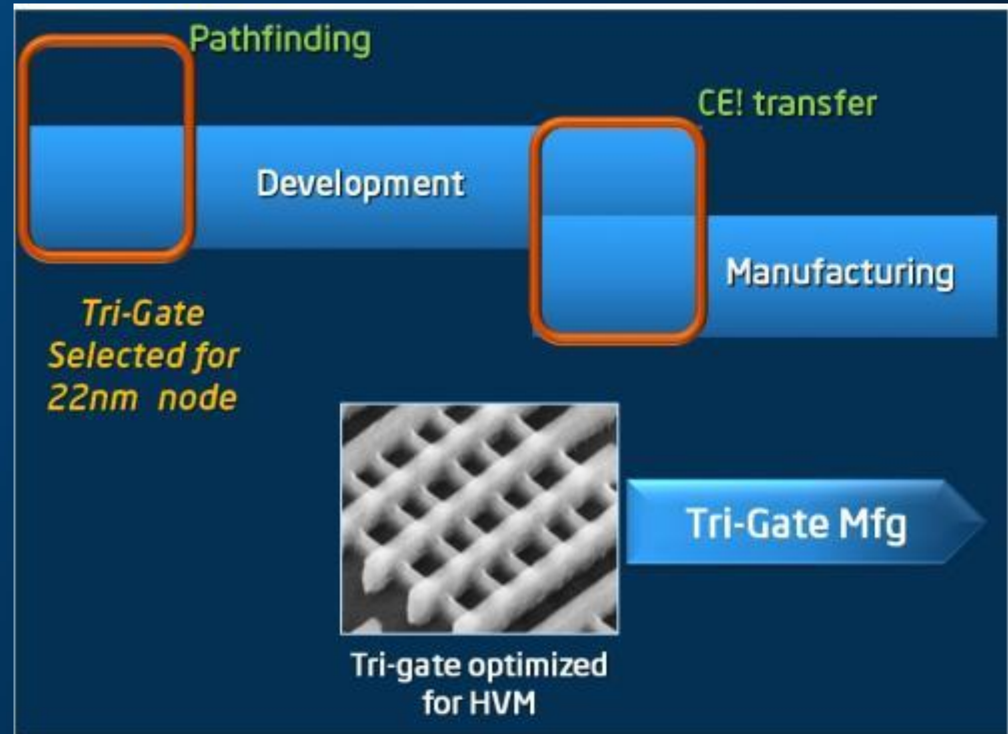




Tri-gate SRAM cells demonstrated



Tri-gate RMG process flow developed



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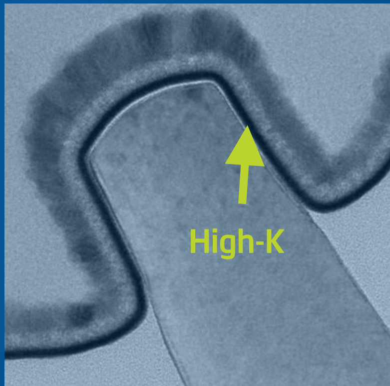

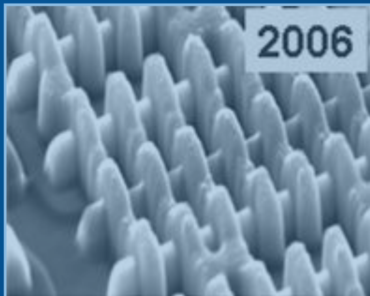

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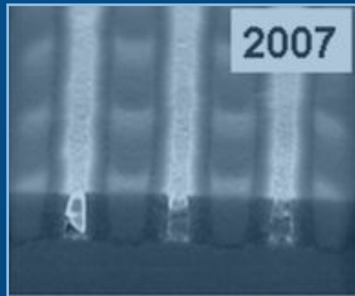
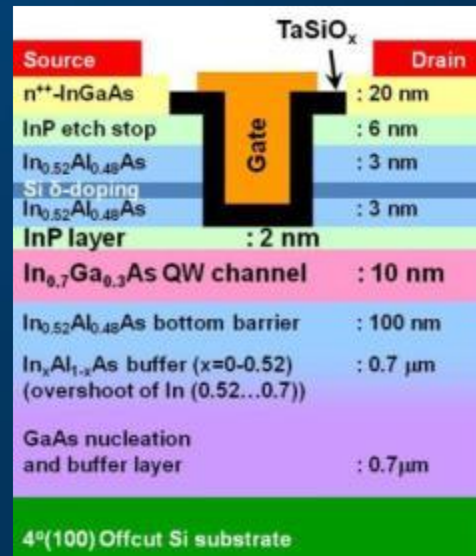
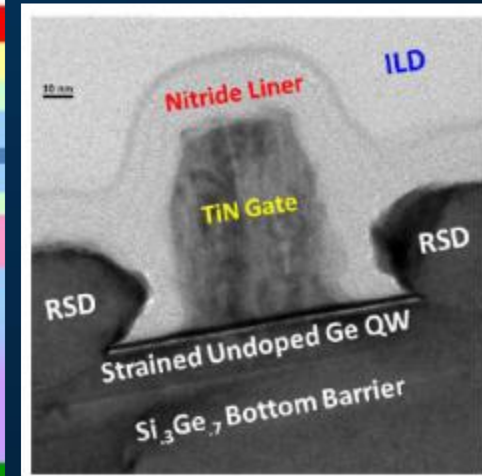


Tri-gate RMG process flow developed

Integration Today

- III-V grown on bulk silicon
- High k integration done
- Strain engineering – not needed
- 3D devices – partially done
- N and P on same wafer – NOT DONE





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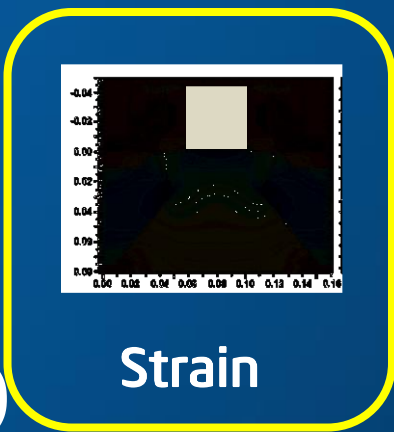
THEN

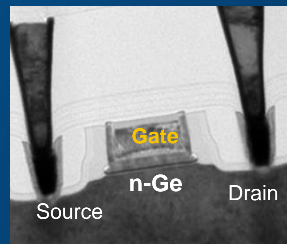
Optimizing Choices for Transistors on Multiple Fronts

Increasing MOBILITY

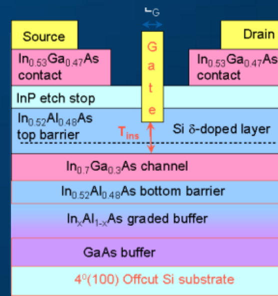
(better ON)



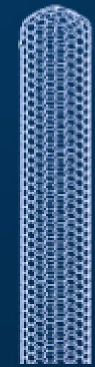
Strain



Ge



III-V

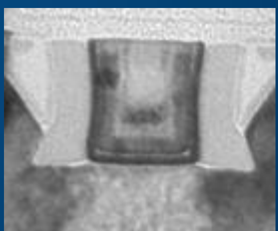


CNT

Graphene

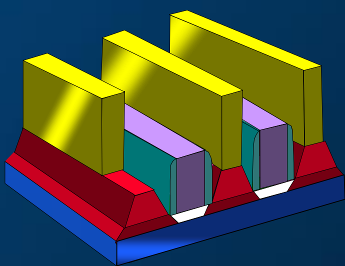
Increasing COUPLING

(better OFF)



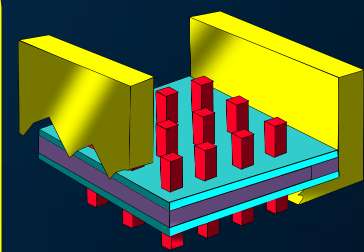
Planar

With High K



UTB SOI (or QW)

Fins



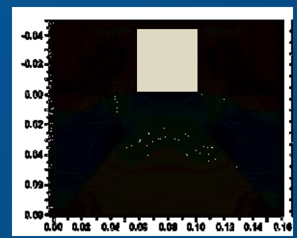
Wires/Dots

NOW

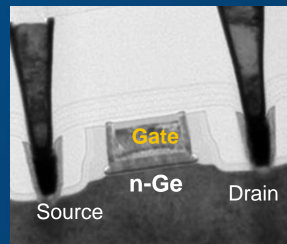
Optimizing Choices for Transistors on Multiple Fronts

Increasing MOBILITY

(better ON)



Strain



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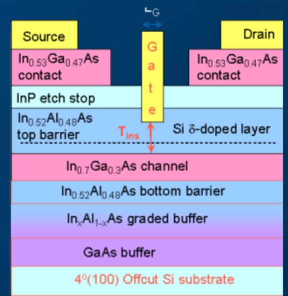
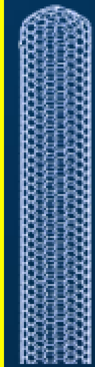


III-V

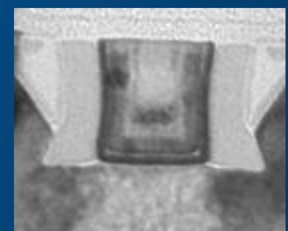


CNT

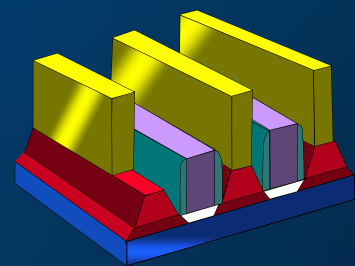
Graphene

Increasing COUPLING

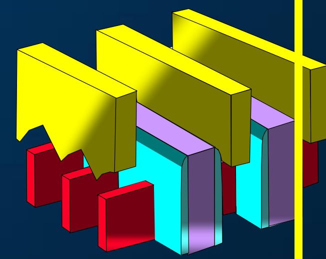
(better OFF)



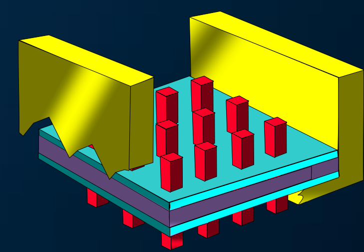
Planar With High K



UTB SOI (or QW)

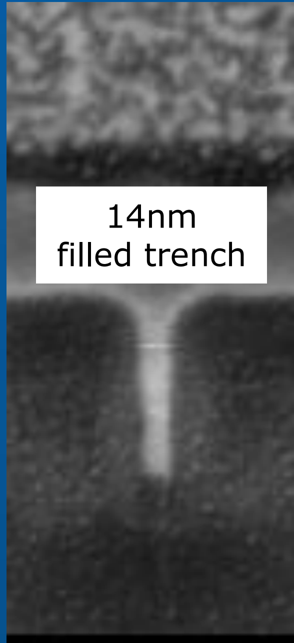


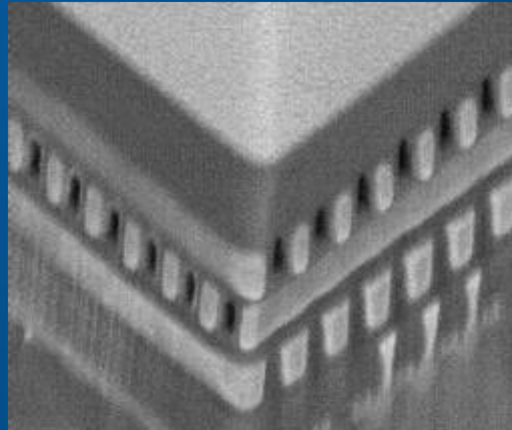
Fins

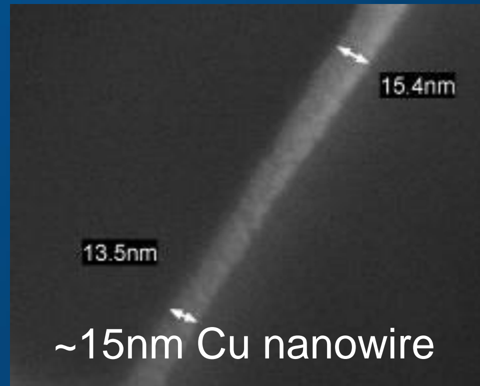


Wires/Dots

Interconnects Need to Scale

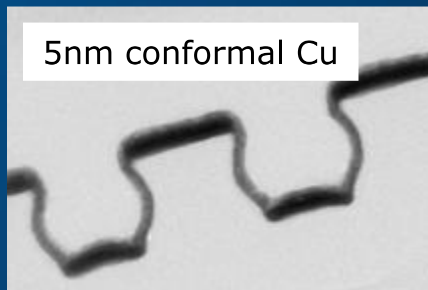


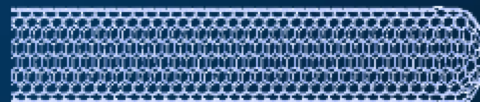




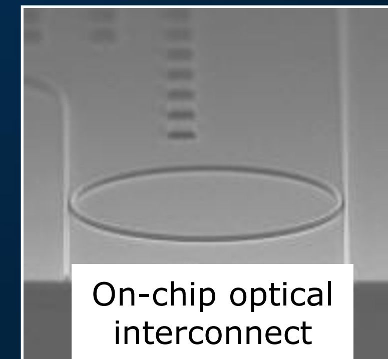
Needed Focus

- Thin conformal plateable barrier
  ... or self forming barrier
- Tall vias might use non-Cu
- Non-SiO2 dielectrics
- Exotic long interconnects: CNT (10's um), optical (>mm)
- 3D stacking





CNT



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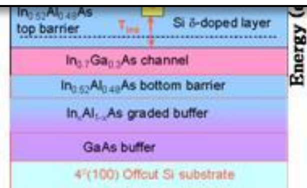
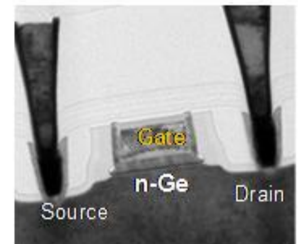
Broad Range of Options

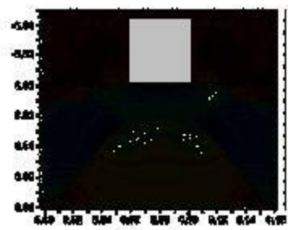
MOBILITY



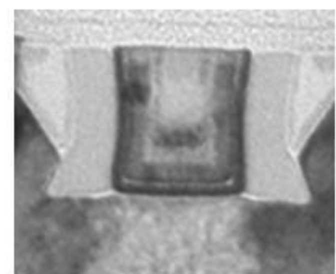
III-V



Ge

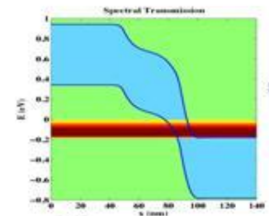


Strain



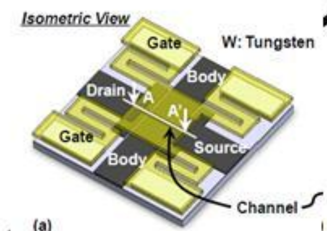
32nm

STRUCTURE



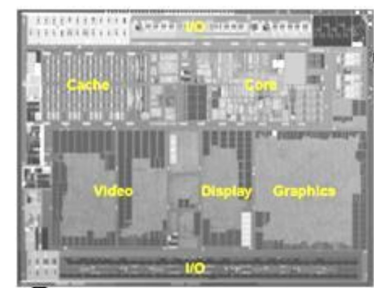
TFET

M. Luisier (Purdue) EDL 2009

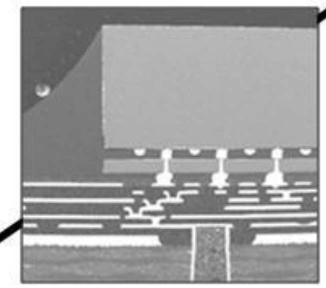


RELAY

Liu IEDM 2010

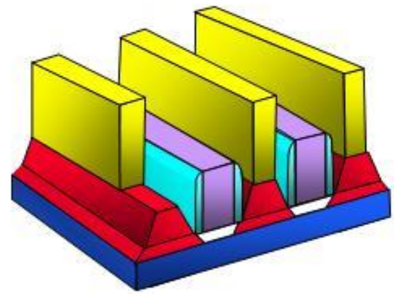


System-on-chip

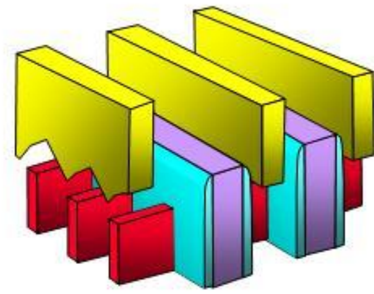


System-in-package

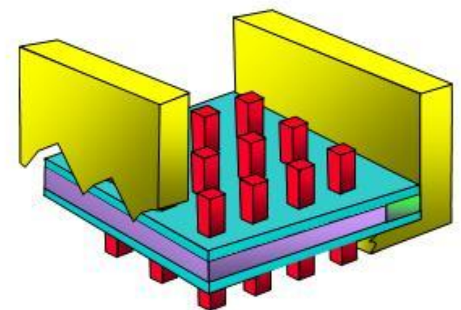
INTEGRATION



UTB SOI



Fins



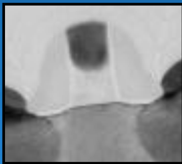
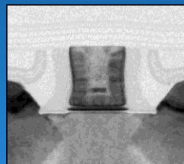
Wires/Dots

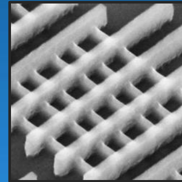
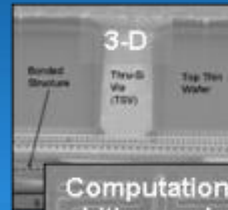
COUPLING

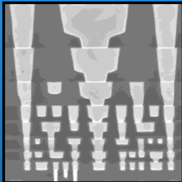
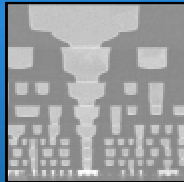
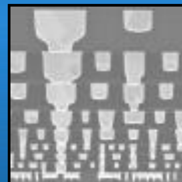
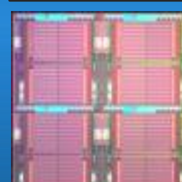
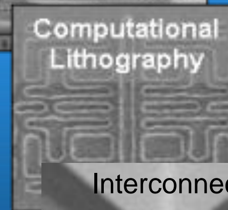
We Expect Technology Innovation to Continue

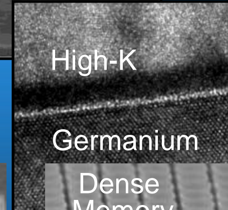
65nm	45nm	32nm	22nm	14nm	10nm	7nm	Beyond
2005	2007	2009	2011*	2013*	2015*	2017*	2019+

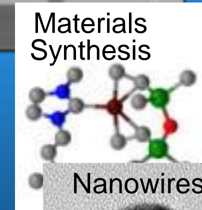
MANUFACTURING → DEVELOPMENT → RESEARCH

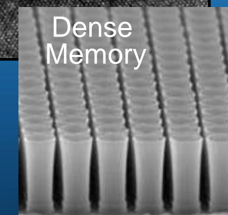



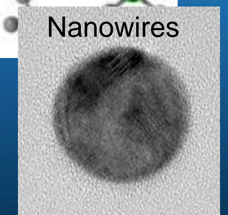











*projected

Conclusions

- Moore's Law is not a law of nature, it is an expectation of continued innovation
- We expect to continue through focused research, rapid development, investment in production

- Scaling research is increasingly about materials research, solving problems brings opportunities
- New product opportunities will arise from continued advances in integration, connectivity

Discussion