

CMOS Transistor Scaling Past 32nm and Implications on Variation

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Abstract - This paper explores CMOS transistor scaling past the 32nm generation and its implications on variation. Front-end variation sources are reviewed, with detailed discussion on lithography and polish variation sources past 32nm. New transistor architectures are discussed, with emphasis on benefits and challenges relative to variation. Detailed variation measurement techniques are reviewed, with supporting multi-generational trend results, including data from the 32nm node.

I. INTRODUCTION

For the past 40 years, relentless focus on Moore's Law transistor scaling has delivered ever-increasing transistor density. For much of that time, Moore's Law transistor scaling meant "classic" Dennard scaling [1] where oxide thickness (T_{ox}), transistor length (L_g) and transistor width (W) were scaled by a constant factor ($1/k$) in order to provide a delay improvement of $1/k$ at constant power density. In recent years, Dennard scaling has become less influential, and performance enhancers have been added to continue the density scaling roadmap (e-SiGe and strained SiN for strain in the 90nm and 65nm nodes [2,3], and high-k metal-gate (HiK-MG) in the 45nm and 32nm nodes [4,5]). As a consequence of continued density scaling, features are moving ever closer to fundamental dimensions (such as atomic dimensions and light wavelengths) meaning that management of variation will play a major role in future technology scaling [6].

II. VARIATION SOURCES

Variation sources in the CMOS front-end [7, and references therein] can be categorized into two groups. The first group consists of historical variation sources which will continue to offer challenges moving forward. This group includes patterning proximity effects (both classical, and optical proximity correction (OPC) [8]), line-edge and line-width roughness (LER and LWR, respectively [9]), polish variations (shallow trench isolation (STI) [10] and gate [11]), and variations in the gate dielectric (oxide thickness variations [12], fixed charge [13], and defects and traps [14]). The second group includes variation sources which were historically of minor impact, but have emerged as significant challenges in recent years. This group includes random dopant fluctuation (RDF) [15-17], variation associated with implants and anneals (tool-based [18], pocket implants [19], rapid-thermal anneal (RTA) [20]), variation associated with strain (wafer-level biaxial [21], high-stress capping layers [22], and embedded silicon-germanium (SiGe) [23]) and variation associated with granularity in the gate material (for poly gates, [24], for metal gates, [25]).

A. Patterning past 32nm

The last four technology generations have used 193nm optical lithography, with OPC, aperture improvement, advanced lens designs, and immersion lithography bridging the resolution gap (see Fig. 1).

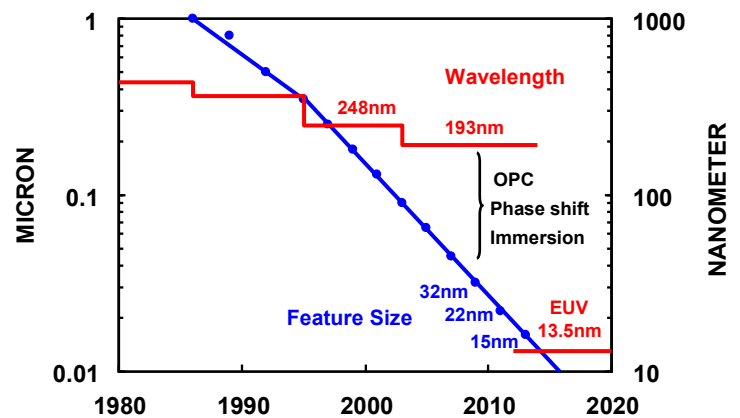


Fig. 1. Recent technology generations have used 193nm optical lithography, with OPC, aperture improvement, advanced lens designs, and immersion lithography bridging the resolution gap.

The effectiveness of these advanced lithography techniques can be seen in the steady improvement in gate critical dimension (CD) variation (see Fig. 2) as well as the steady reduction in SRAM cell area (see Fig. 3).

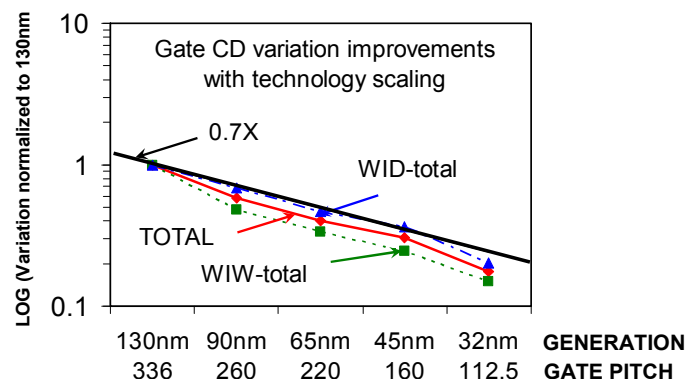


Fig. 2. Critical to management of variation is the ability to deliver a 0.7X gate CD variation improvement in each generation enabled by continuous process technology improvements [26].

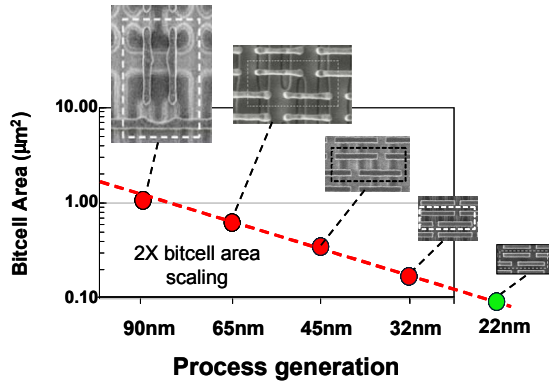


Fig. 3. Consistent 2X bitcell area scaling for the last five generations [27].

While there is certainly much discussion and anticipation on the generational intercept point for EUV lithography, perhaps of more interest to the variation community are the non-EUV pitch-reduction technologies. These technologies (such as double-patterning, or spacer-patterning) are likely to alter historical variation trends (and will undoubtedly be paired with EUV in advanced technology nodes.)

Double patterning technologies decrease the pitch by patterning twice, either through a resist freeze technique, or a double pattern transfer. These techniques allow for pitch-doubling without EUV technology. However, double patterning techniques still require resolution of a very small space (with associated LER and LWR issues), are very sensitive to misalignment between the two exposures (see Fig. 4-left), and eliminate the close correlation between adjacent transistor pairs (with significant implications for memory cells and other circuits that rely on CD matching between adjacent devices, see Fig. 4-right).

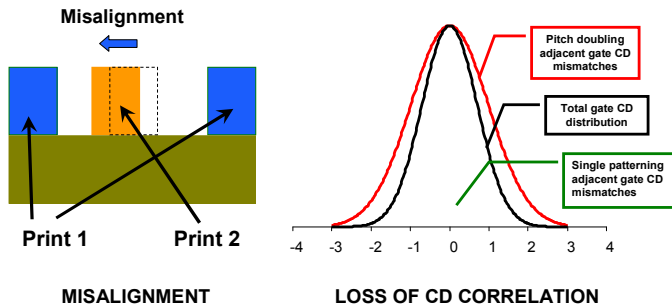


Fig. 4. Challenges of double patterning [26].

Spacer patterning technologies decrease the pitch by patterning a dummy structure at 2X the desired pitch, depositing spacers on the dummy structure, and then removing the dummy to leave the spacers at the desired pitch. Spacer patterning allows for significant pitch reduction without EUV technology, and does not suffer from misalignment or correlation issues. However, spacer patterning poses significant integration challenges and likely requires a “trim” mask (Fig. 5).

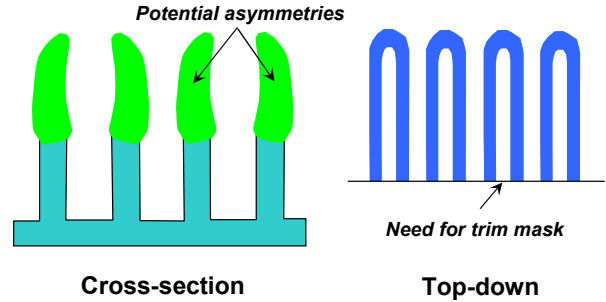


Fig. 5. Spacer patterning will have variation and integration challenges.

B. Polish past 32nm

Of particular interest are historical variation sources whose impact has been altered by advanced processing. An excellent example is the polish operations associated with the replacement gate high-k metal gate process.

Recall that there are two primary competing architectures for high-k metal gate (Fig. 6). These are gate first (where the metal is laid down before gate definition) and replacement gate (where a sacrificial gate is fabricated and later replaced by the metal gate material) [4, 28-29].

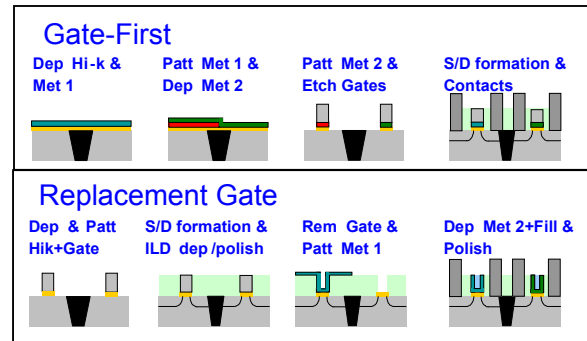


Fig. 6. HiK-MG flows, gate first vs. replacement gate [28]

The replacement gate process has several benefits over the gate-first process. One benefit is that replacement gate permits higher temperature anneals prior to the metal deposition (for better activation of implants). Another benefit is that the replacement gate flow enables an elegant PMOS strain enhancement mechanism (Fig. 7) through first straining the PMOS with e-SiGe and then removing the gate [28,30].

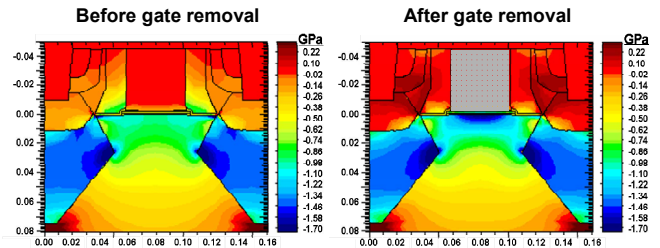


Fig. 7. Removal of poly gate increases channel stress by 50% [28].

However, the replacement gate process also poses challenges, as it requires two new polishing steps and interacts with STI polish (see Fig. 8).

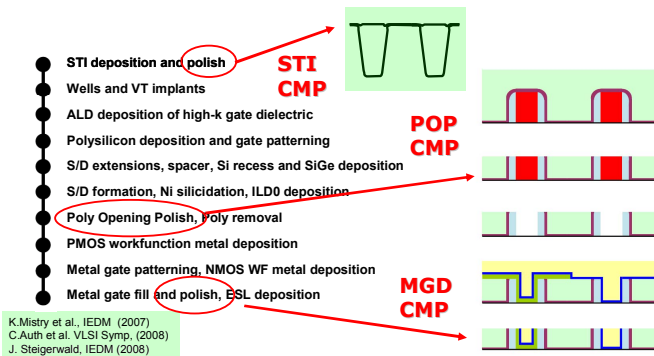


Fig. 8. Replacement metal gate: three critical CMP operations [11].

Gate height control is essential in a replacement gate process (see Fig. 9). If the gate is over-polished, the raised source-drain is exposed to the polish, resulting in R_{ext} and mobility variation. If the gate is under-polished, the contact taper causes R_{ext} variation (the extreme case resulting in an open-contact yield issue).

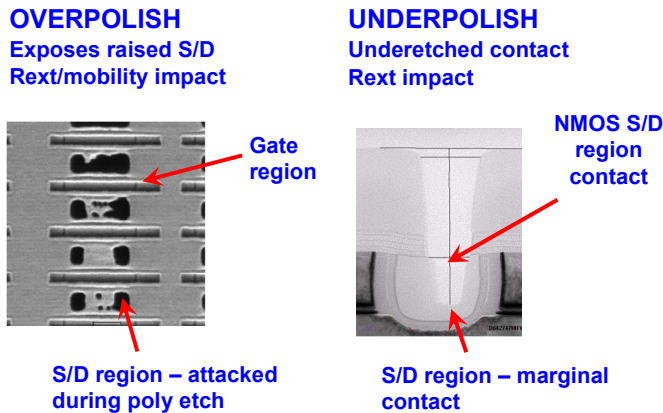


Fig. 9. Criticality of gate-height control in a replacement gate process [11].

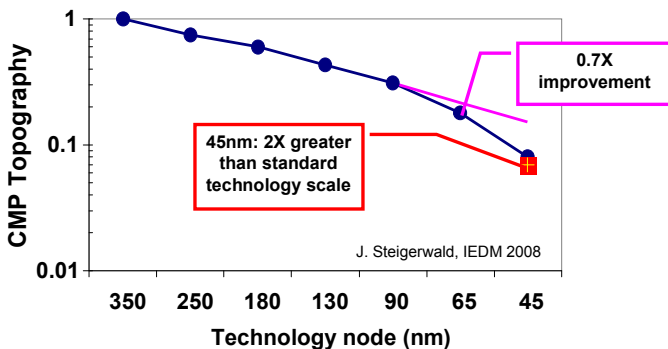


Fig. 10. 2X improvement in the topography roadmap associated with the introduction of the replacement gate process [11].

To avoid an increase in variation, the developmental roadmap for gate polish improvement needs to exceed 0.7X technology scaling in the generation where the replacement gate process is introduced. This is illustrated in Fig. 10, where the 45nm generation (the first introduction of replacement metal gate in manufacturing) shows almost a 2X improvement over the standard 0.7X generational scaling.

III. FUTURE TRANSISTOR ARCHITECTURES

A variety of device architectures are being investigated for advanced technology nodes. These architectures can be broadly categorized by the method of electrostatic confinement. There are architectures which provide additional electrostatic confinement with a planar architecture (ultra-thin body (UTB), fully-depleted SOI (FDSOI), etc.), those which use 1'D electrostatic confinement (double gate, FinFET, etc.), those with more than 1'D, but less than 2'D (Trigate, Omega-FET, etc.) and those with full 2'D confinement (gate-all-around (GAA), nanowire etc.) [31].

A. Additional electrostatic confinement in planar

The potential value of fully-depleted UTB SOI for planar electrostatic confinement (as well as the requirements for extremely Si thin layers to achieve well-designed fully-depleted devices) has been recognized since the mid-1980s [32-33]. There has been a steady reduction in the minimum demonstrated body thicknesses (T_{si}) moving from ~100nm in the 1980s and early 90s [34-35], down to the 15-20nm range in early 2000 [36-38], and more recently to values significantly below 10nm [39-41].

UTB SOI devices benefit from using similar manufacturing to planar SOI technology, but with improved SCE, potential for improved RDF (due to lower channel doping) and the possibility for body bias (with thin BOX).

Challenges of UTB SOI include thin T_{si} effects (external resistance, R_{ext} , scattering, and quantum confinement changes in V_T), difficulties in inducing strain and variation manufacturing challenges with the thin T_{si} .

B. 1'D and 1'D+ confinement

There is a tradeoff between the electrostatic improvement of a GAA device and the fabrication complexity of making gates on all sides of a channel. A number of intermediate architectures (sometimes called multiple gate FET devices or MuGFETs) have been developed in an attempt to get the best SCE with the minimum process complexity [42-59].

Double-gate devices first appeared in the literature in the mid-1980s [42], and a variety of different geometries were explored in the next two decades [43-58]. Categories (see Fig. 11) include:

FinFET: Combines double-gate and vertical device concepts for a more manufacturable version of a double gate device [44-55].

Trigate: Differs from FinFETs in the absence of a gate-blocking layer on the top of the gate. Tri-gate devices have gates around three sides of the device, providing improved SCE with reduced vertical topography requirements [56-57].

Pi-gates: Differs from Tri-gates in having the gate extend below the channel. This creates a virtual back gate which shields the back of the channel from electric field lines from the drain, providing improved SCE [58].

Omega-FETS: Differ from Tri-gates in that the gate not only wraps around three sides, but underlaps part of the fourth. This has an effect similar to Pi-gate in shielding the back of the channel from field lines, resulting in improved SCE [59].

All of these multiple-gate devices have similar RDF and SCE advantages over planar as UTB SOI. In addition, the increased confinement in comparison with UTB devices relaxes the manufacturing constraints ($W_{si} \sim 2T_{si}$). Furthermore, tying the gates together provides nearly ideal sub-threshold slope. Note also that independent gate operation is possible in some of these architectures.

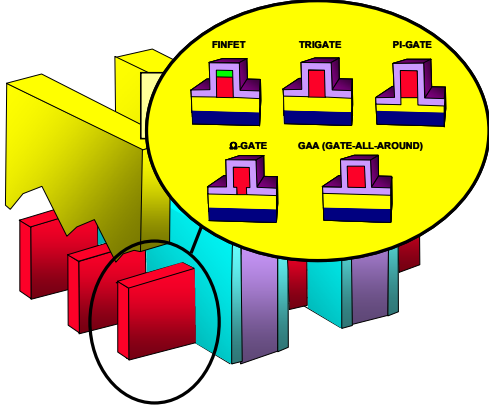


Fig. 11. Type of multiple gate architectures.

MuGFETs share the strain and R_{ext} challenges of UTB devices. In addition, these devices face significant variation challenges posed by the vertical topography, tight diffusion pitches and complex gate patterning.

C. 2D confinement

GAA devices were first reported in the late 1990s [60-61]. GAA devices differ from Omega-FETs in that the gate wraps entirely around the device. Note that both lateral [60,62,64], and vertical [61,63], devices are possible with this architecture. Both types provide full two dimensional confinement with the associated RDF and SCE benefits.

GAA devices offer the best potential solution to electrostatic confinement challenges of future devices, as well as offering the possibility for significant RDF reduction. However, these devices face significant challenges. Not only do they have the strain, R_{ext} , vertical topography, tight pitch, and complex gate patterning challenges of the MuGFET devices, they also face new challenges with gate conformality and excess parasitic capacitance.

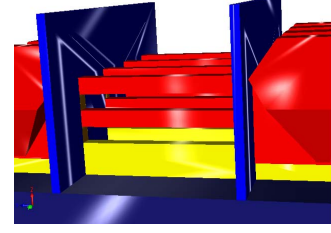


Fig. 12. Nanowires are an extreme case of GAA devices.

Nanowires are an extreme case of GAA devices, having height and width dimensions roughly the same (or even cylindrical) and small (<10nm) dimensions [Fig. 12, 65-69]. Nanowires add the challenges of phonon scattering [70], (along with possible benefits due to reduction in interface scattering [71-72]).

III. VARIATION DEFINITIONS AND MEASUREMENT STRATEGIES

Unfortunately, the terms “random variation” and “systematic variation” do not have a unified definition in the semiconductor variation community. Experimentally, random variation can be defined as the variation measured between a pair of two closely-spaced objects. Systematic variation can be defined as the variation measured from a number of widely separated objects, after the random variation has been removed by a root-mean-square (RMS) analysis (eq. 1).

$$\sigma X_{systematic} = \sqrt{(\sigma X_{pop})^2 - (\sigma X_{random})^2} \quad (1)$$

Using V_T as an example, the most common way to measure random variation (σV_T) is to measure the difference in V_T (DV_T) between paired closely spaced devices, obtain the standard deviation of DV_T (σDV_T) over a large population of pairs (for example, all the pairs on a wafer), divide σDV_T by $\sqrt{2}$ to obtain the random σV_T for the individual device as,

$$\sigma V_{T_{one-device(random)}} = \frac{\sigma(VT_A - VT_B)}{\sqrt{2}} = \frac{\sigma(DVT)}{\sqrt{2}} \quad (2)$$

then, compute the systematic σV_T from the RMS as,

$$\sigma V_{T_{systematic}} = \sqrt{(\sigma V_{T_{pop}})^2 - \left(\frac{\sigma(DVT)}{\sqrt{2}}\right)^2} \quad (3)$$

One significant difficulty with the paired-device method is that there may be systematic variation of the random variation. (As one common example, the random variation measured from matched pairs may be systematically higher at the edge of the wafer than in the center) Unfortunately, the obvious mitigation (filtering the data) carries the associated risk of

dropping the sample size below good statistical sampling criteria as defined by the central limit theorem (CLT). (As a common example of this problem, if statistical data is evaluated on a per-wafer basis, under-sampling can result in the measured σ varying from wafer to wafer solely due to the under-sampling – not the underlying process.)

One way to address under-sampling issues with paired devices is to use measurement arrays (see Fig. 13 and 14). A measurement array consists of a large number of devices, each individually addressable, so all parametric measurements (V_T , I_D , SS , $DIBL$, etc.) can be done on a large set of closely-spaced devices. The size of the array is chosen so as to be large enough to avoid CLT sampling issues, but smaller than all known systematic effects (typically $100 < \text{array size} < 1000$). The clear value of these arrays is they provide σX values for a single physical test structure (essentially a single physical location on the wafer). The disadvantage is that arrays have systematic layout debiasing (see Fig. 13) and significant testing analysis and effort is required to accurately measure arrays.

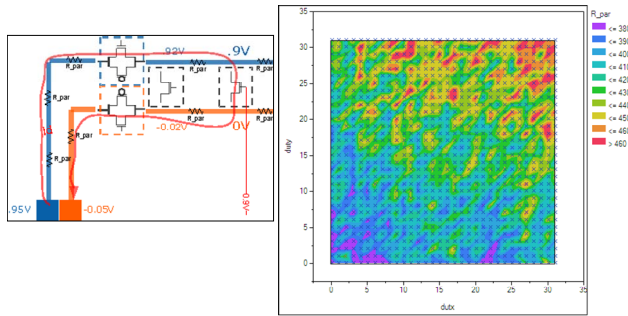


Fig. 13. Systematic parasitic resistance variation across an array structure

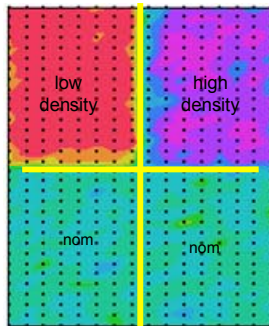


Fig. 14. Use of a bias-compensated array to measure variation in precision resistors as a function of pattern density.

Another approach for variation measurement is to use ring oscillators (see Fig. 15). By analogy with individual devices (eq. 1), closely spaced ring oscillators (or ring oscillators with interlaced transistors) are used to obtain random variation data, and large populations of oscillators (with random variation removed via RMS) are used to obtain systematic variation data.

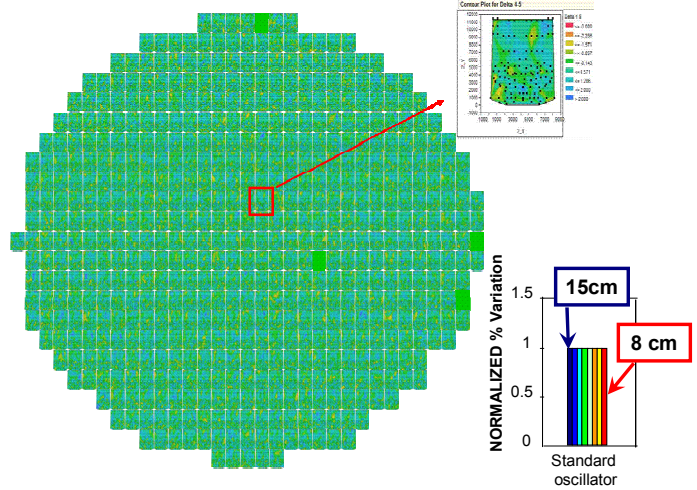


Fig. 15. Use of a ring-oscillators to measure random variation across a 45nm product wafer [7]

The positive features of ring oscillators are that they can be implemented on product die rather than test chip die (frequency data can be easily multiplexed out with other end-of-line tests on product material). The value of product implementation is a dramatic increase in the sample size.

The major negative feature of ring oscillators is the difficulty in correlating the measured frequency variation back to simple parametric terms (such as V_T , I_D , SS , $DIBL$, etc.), or individual process mechanisms (such as L_e , mobility, R_{sd} etc). In spite of these difficulties, product ring oscillators remain an excellent way to benchmark overall product variation between technologies, as they represent a simple circuit design than can be implemented generation after generation (see Fig. 16)

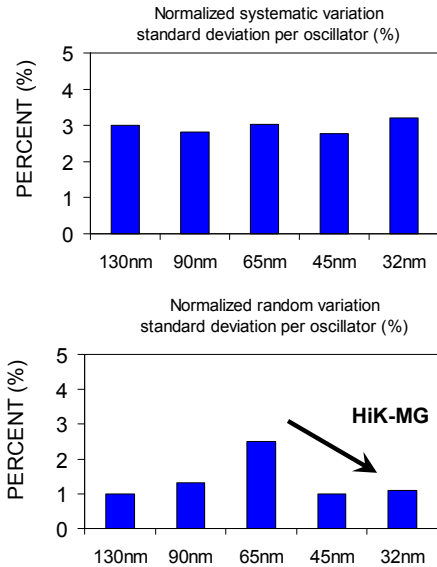


Fig. 16. Systematic variation (top) and random variation (bottom). Technology trends for the last five generations [7].

IV. CONCLUSION

While significant variation challenges exist for technologies past 32nm, numerous solutions are being explored to drive Moore's Law forward. Process variation is not an insurmountable barrier to Moore's law, but is simply another challenge to be overcome.

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