EECS 579   *Exam 2*

Name (print) _____

ID number _____

Grades: 1. _____

2. _____

3. _____

4. _____

5. _____

6. _____

Total Grade   _____ %

Instructions

1.   The exam is ***closed book***, meaning no books, notes, or the like may be used.
2.   Attempt ***any five*** of the six problems. Each problem is worth 20 points, for a maximum grade of 100 points. Mark with an X in the above grade list the problem you do ***not*** want graded.
3.   Write your answers after the questions in this booklet. If you need more space, use the backs of the sheets with a pointer like "Go to back of p. 4". There is an extra blank page at the end.
4.   When in doubt, state any assumptions you make.
5.   Show all your work. You get partial credit for partial answers.

Problem 1 (*Combinational faults and tests*)

Answer the following 10 questions, each of which is worth 2 points.

1. How many test vectors are needed to detect all single-stuck line (SSL) faults in a 7-input NAND gate? **Answer 1**: _____

2. How many test vectors are needed to detect all SSL faults in a 7-input XOR (exclusive-or) gate?

A**nswer 2**: _____

3. How many test vectors are needed to detect all SSL faults in an n-input XOR gate, where $n \geq 2$?

Answer 3: _____

4. How many classes of equivalent SSL faults are present in a 4-input NAND gate?

Answer 4: _____

5. How many classes of equivalent multiple-stuck line (MSL) faults are present in a 4-input NAND gate? **Answer 5**: _____

6. How many SSL faults in an n-input NAND gate are dominated by some SSL fault that is not equivalent to the dominated fault? **Answer 6**: _____

7. In an n-input NAND gate, is it true that no two SSL faults affecting input lines can be equivalent to each other? **Answer 7**: _____

8. Is it true that every fanout-free circuit with n inputs requires at least $n + 1$ test vectors to detect all its SSL faults? **Answer 8**: _____

9. An n-bit adder is to be tested for pin faults (PFs) only, that is, for single stuck-at-0 and stuck-at-1 faults affecting the adder's primary input and output lines. The internal logic design of the adder is unknown. How many tests are needed to detect all the adder's PFs?

Answer 9: _____

10. An n-input, m-output combinational cell M is embedded inside a large circuit, and is to be tested under the cell-fault (CF) model. What is the maximum (worst-case) number of test vectors that must be applied to M? **Answer 10**: _____

Problem 2 (*C-testability*)

(**a**) Define concisely what it means to say that the iterative logic array *A* of Figure 1*a* below is C-testable with respect to any single-cell fault.
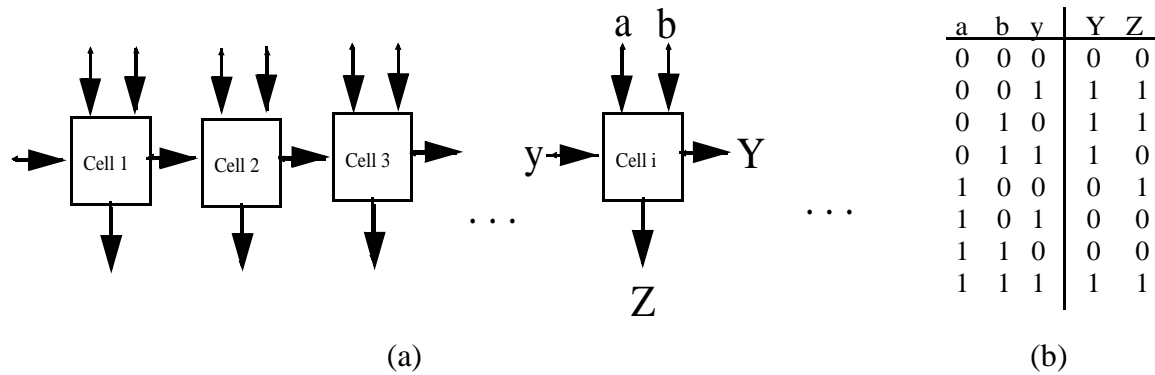

a	b	y	Y	Z
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

(a)   (b)

Figure 1

(**b**) Suppose that the cells of *A* have the behavior shown in Figure 1*b*. Prove that *A* is C-testable by constructing a complete (and preferably minimal) set of tests for it.

(**c**) Show how you can change just one row of the table of Figure 1*b* in order to make it non-C-testable. Explain clearly why the modified table is not C-testable.

Problem 3 (*Sequential Circuit Testing*)
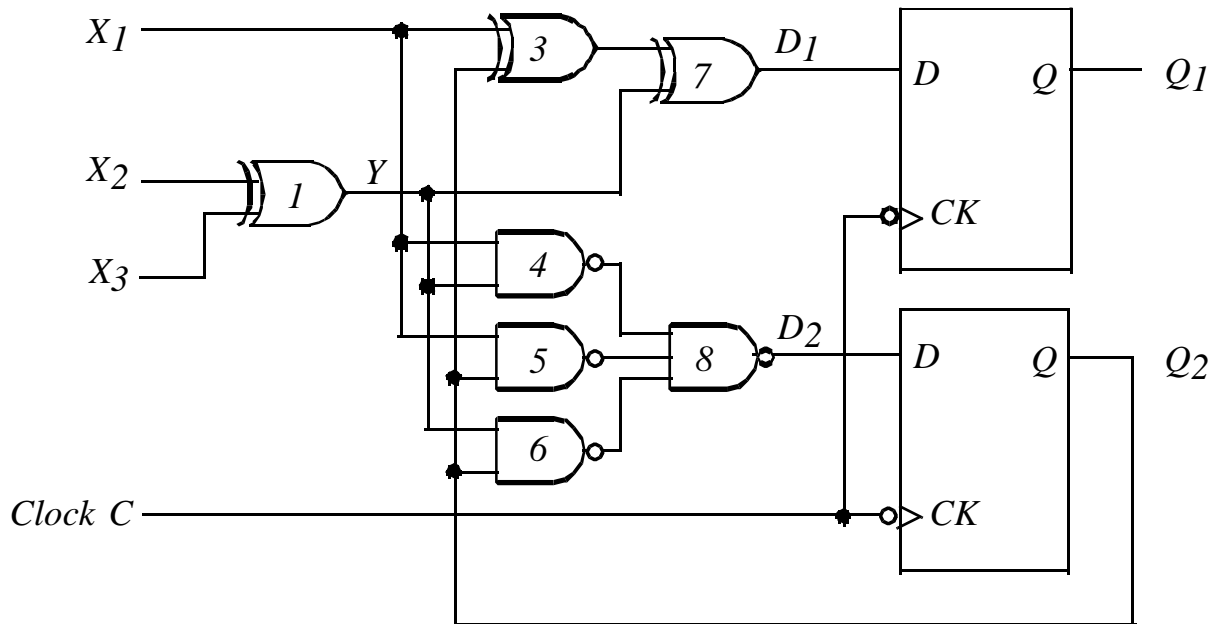
Consider the synchronous sequential circuit M_0 above, which is based on the 74F385. It has three primary inputs (plus a clock signal) and one primary output Q_1. Assume that all the XORs are primitive gates. The circuit has up to four internal states which you must label with the names A, B, C, and D corresponding to $Q_1Q_2 = 00, 01, 10$, and 11, respectively.

(**a**) The fault-free M_0 can be reset to a fixed initial state while operating in normal synchronous mode. Prove this by constructing a minimum-length synchronizing sequence for M_0.

(**b**) Suppose that flip-flop input D_2 is stuck-at-1, and that this fault $D_2/1$ changes M_0 to a faulty circuit M_1. Determine if there is a sequence that will synchronize the circuit whether or not this fault is present. Again find a minimum-length synchronizing sequence, or prove that none exists.

(**c**) Using any method, derive a test sequence that detects the fault $D_2/1$ when the initial state is unknown. Identify your method and use comments to clearly explain your calculations.

Problem 4 (*Compression methods*)

(**a**) A single-output combinational circuit has a complete and minimal test set of eight test vectors for some fault class. Seven of the test vectors $t_1^0, t_2^0, t_3^0, t_4^0, t_5^0, t_6^0, t_7^0$ produce output 0 and one test vector t_8^1 produces output 1. Assume the tests can be applied in any order. Construct as short a tests sequence as you can that guarantees complete fault detection when the output response is compressed using ones counting. Explain why your test sequence is complete.

Ans. Test length =_____

(**b**) [Text Problem 10.5] Prove that any two-level AND-OR irredundant circuit that realizes a unate function in all its variables is syndrome testable. [Recall that the syndrome for an n-input function with k minterms is $k/2^n$.]

Problem 5 (*Fault simulation*)
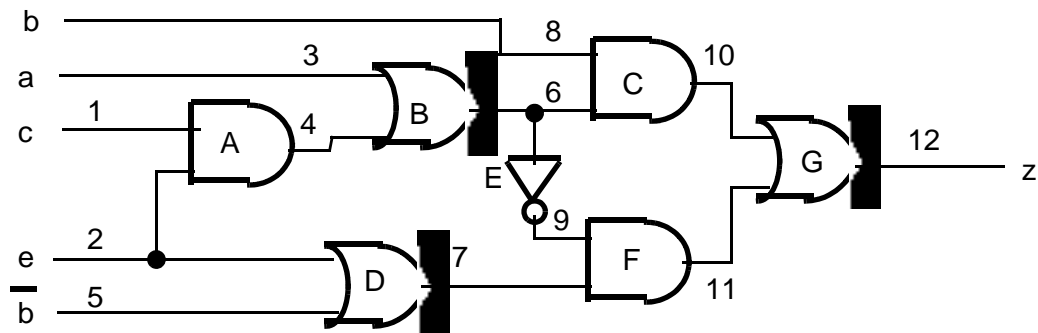
Consider the AND-OR-NOT circuit shown above. Use the deductive fault simulation method to identify all SSL faults detected by the input pattern $(a,b,c,e) = (1,1,1,0)$. (IGNORE THE THICK VERTICAL BLACK BARS - IT'S JUST A PRINTING PROBLEM)

Problem 6 (*BIST*)

A certain 20-input 2-output combinational circuit *K* requires exhaustive testing for complete fault detection. *K* is built from a technology which guarantees that the number of errors appearing on each of its output lines z_i will always be odd in response to exhaustive testing. It is required to design a low-cost BIST scheme for *K* consisting of a test generator TG, and a response monitor RM that can store reference signature(s) and produces a single output signal *ERROR*. The BIST design goals are: first, as little aliasing as possible, and second, as little hardware area overhead as possible. Test application time is not of concern here. Assume that hardware area cost can be estimated as follows: an *k*-input gate has cost *k*; a D-flip-flop or a RAM storage cell has cost 5; a ROM storage cell has cost 3; a *k*-bit register or counter has cost 5*k*; a *k*-bit magnitude comparator has cost 10*k*. Wiring costs can be ignored.

(**a**) Select suitable designs for TG and RM, and briefly justify your design decisions. Draw a block diagram showing the overall structure of your BIST configuration.

(**b**) Obtain a numerical estimate of the aliasing probability of your method and justify it.

>   **Ans**. Aliasing probability (percent): _____

(**c**) Obtain a numerical estimate of the hardware area overhead cost of your method, showing your calculations and assumptions,

.   **Ans**. Area overhead cost: _____