EECS 522 - Projects

1 Low phase noise quadrature voltage controlled oscillator
2.4GHz, power consumption 50mW, phase noise -100dBc at 100 KHz.
Supply voltage 1.8+/- 5% temp 25-100C
(many papers from Abidi, Razavi etc.)
Design a simple bias circuit.
1 degree phase accuracy – you must consider transistor mismatch
(consider only MOS Vt mismatch, used signma_Vt= Avt/sqrt(WL),
where AVt = 10mV um, W= width and L = Length)

2. Front end for GPS radio (low IF architecture)
RF @ 1.575GHz, LO@1.573GHz
Just implement the LNA and the mixer.
Design a simple bias circuit.
Supply voltage 1.8+/- 5% temp 25-100C
50 ohm input match +/- 10%. No output match requirement
Clock generator or quadrature generator not required, you can assume ideal clock signals
Total noise figure 2.5dB
Linearity Output IM3 -127dBm
No power spec – just make it work….
(see Tom Lee's 98 paper)

3. Clock generator for GPS radio
1.573GHz out, 1/16 of that in.
Capture range 5MHz
This is most likely implemented as a PLL with a fixed feedback divider.
(The divider is simply a 1 to 16 counter)
Supply voltage 1.8+/- 5% temp 25-100C
However other approaches (e.g. injection locking) are also fine.
This design should include a VCO of some sort, possibly an LC oscillator
Total Power < 50mW.
No noise specs.

4 For the brave (and/or foolish)
A super-regenerative receiver.
1GHz RF in.
Modulation on off keying (OOK) – low bandwidth.
No specs, just get something working.
Envelope detector for on off keying optional
(clock generator not required)
(see Joehl JSSC July 02 for bipolar implementation)