Lab 3:
Differential to Single Ended Amplifier

In this lab, you will design and simulate a differential input to single ended output amplifier.

For NMOS transistors:
V_{th} =.56 V, $\mu_n C_{ox}$ =190 uA/V^2, λ=0.035, and L (Length) =0.5 um
For PMOS transistors:
V_{th}=-.49 V, $\mu_p C_{ox}$= 0.25*$\mu_n C_{ox}$, λ=0.05, L (Length) =0.5 um

1. Schematic and Simulation

Start Cadence and draw the schematic shown in Figure 1 in a new cell. Use *pfetx* cells for the PMOS transistors and *nfet* cells for the NMOS transistors. The *nfet* cells are used so that the substrate contacts are made automatically.

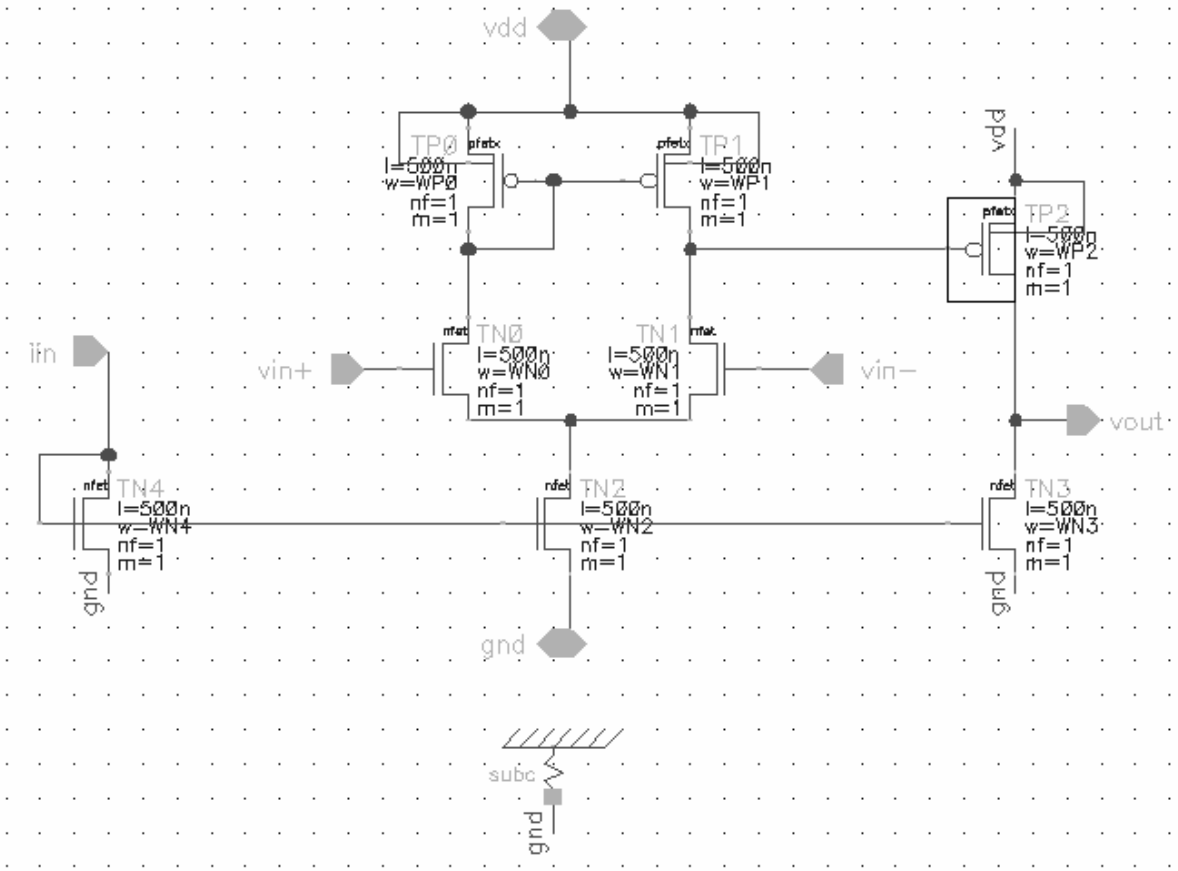

Figure 1. Differential to Single Ended Amplifier

Create a symbol for this circuit. It should have the same number and type of pins as the schematic in Figure 1.

Amplifier Design Conditions:

1) Id = 100uA for TN2, TN3, TN4 (Ideal current source of 100 uA connected to *iin* pin)
2) VDsat=400 mV for all transistors
3) When *vin*+ = *vin*- => current delivered by TP2 = current sunk by TN3
   (In technical terms, this means no systematic offset)
4) VD > VDsat + 200 mV for all transistors

1(a). Choose W for all of the transistors so that the design conditions are satisfied. Also choose the value of the common mode voltage (Vcm). Show work for all these calculations.

1(b). Simulate the DC operating point of this circuit using the symbol in a new cell. Refer to Figure 2. The capacitor of 1 fF (cell *cap*, AnalogLib) at the output will not affect the circuit (for our purposes), it is only placed there to satisfy Cadence connectivity rules. You will have to adjust the widths of the transistors and Vcm to satisfy the design conditions. Note all changes to the design and why they were made. Make a plot of your schematic (the amplifier) by going to

Design > Plot > Submit

and hand this in.

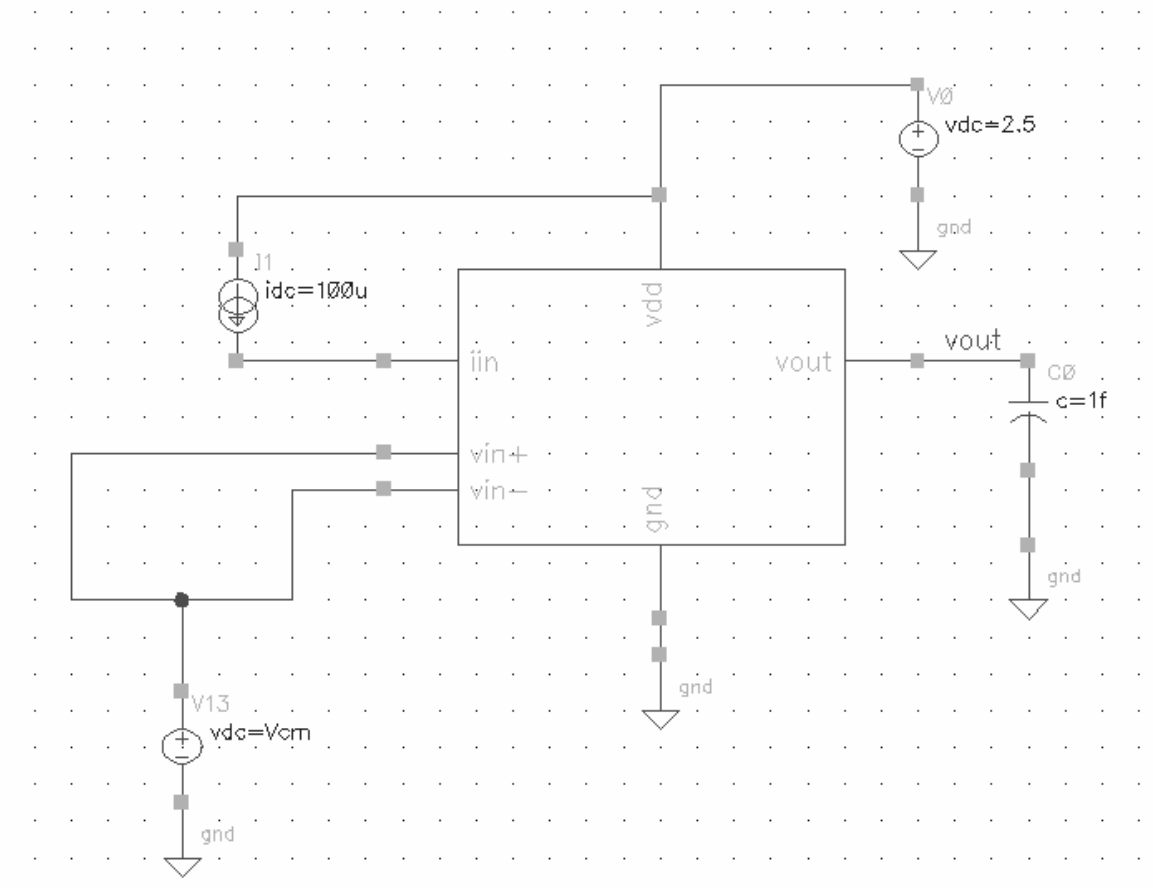

Figure 2. DC operating point simulation

1(c). Draw the schematic shown in Figure 3. There is a voltage-controlled voltage source (cell *vcvs*, AnalogLib) in the schematic. Set the Voltage gain of this device to -1. So, now vin- = - vin+. Sweep the dc voltage *Vpos* from -10mV to 10mV using a Sweep Type of linear (not automatic) with step size of 100u. Plot VS("/vout") using the calculator and hand in. Measure the input offset voltage. That is, when the output is ½ vdd (1.25V), what is the input Voltage? It may be of some use to use the horizontal markers

Markers > Horizontal Marker

It will give you the input for a specific output (1.25 V).

1(d). Measure the slope of this curve when the output is 1.25 V. Determine the gain of the circuit.

Note: For 1(c) and 1(d), remember that you are plotting vout vs. vin+, but the input offset voltage and gain are due to the differential input voltage (vin+ - vin-).

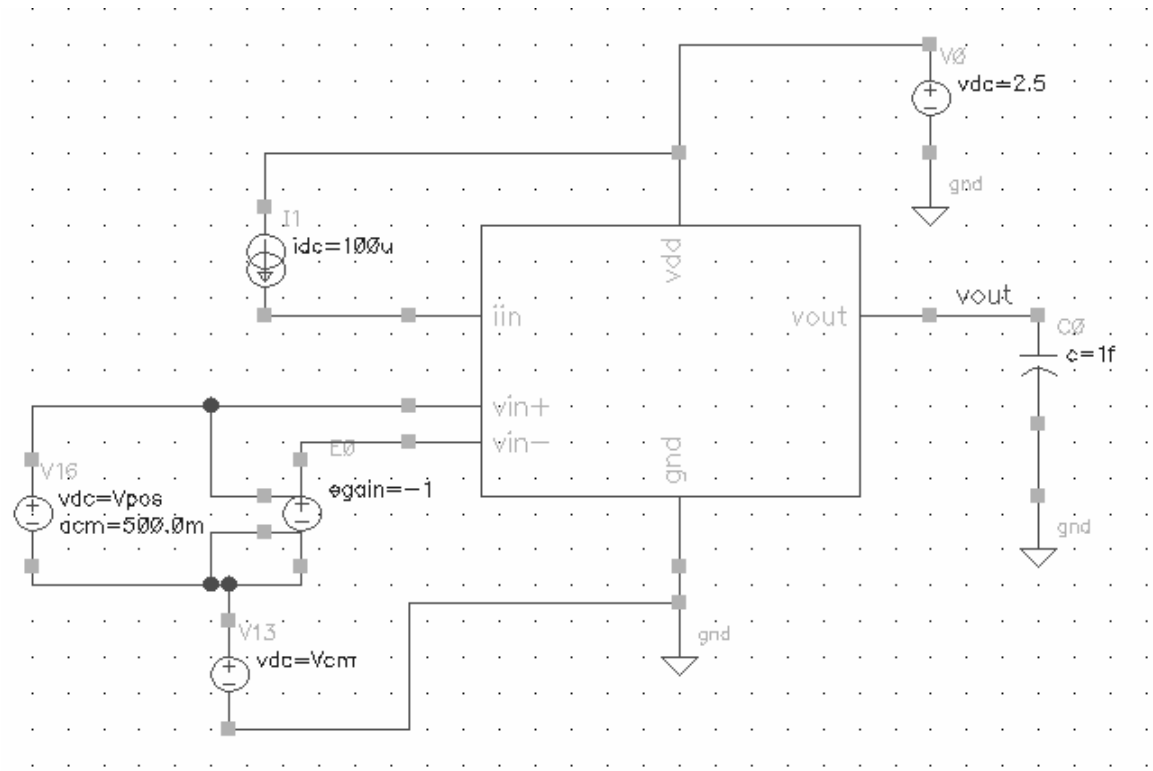

Figure 3. DC and AC Simulation Schematic

1(e). Determine an equation for the gain of this circuit in terms of the small signal parameters. Find the theoretical gain.

1(f). Simulate the gain using an AC analysis. To do this, enter 0.5 for AC Magnitude of the voltage source connected to vin+, as shown in Figure 3. Since the voltage controlled voltage source has a gain of -1, the AC Magnitude of vin- will be -0.5. Thus the AC magnitude of the differential input is 1. AC simulation is done for a range of frequencies. Set up an AC analysis from 10 kHz to 10 MHz in the simulation window and run the simulation. To view the gain of this circuit vs. frequency, plot the AC magnitude of vout by going to

Results > Direct Plot > AC Magnitude

Print and hand in. Since the AC magnitude at the input is 1, the AC magnitude at vout is equal to the gain.

So far in this course we have only looked at the low frequency gain (ignored all capacitance). As the frequency is increased the capacitance starts affecting the gain. Ignore this for now, and concentrate on the low frequency gain. Compare this value to hand calculations.

2. Layout and Verification

2(a) Layout your design. Keep these points in mind when doing layout:

1) The placement of devices in a good layout usually is the same in layout as in the schematic.
2) Make the gnd and vdd rails 5 μm thick.
3) In most cases, laying out the gates vertically works best (vdd and gnd run horizontally across the top and bottom of the circuit, as in the inverter layout).
4) If the width of one transistor (M1) is equal to 2 times the width of another transistor (M2), then the width of M2 should be made using 2 fingers. This means that M2 will consist of two gates, each being the width of the gate for M1. This will make the layout "fit" together better in between vdd and gnd. For more information, refer to Chapter 18 of Razavi. Also, more than one finger should be used if two transistors have a common source or drain. You can select the number of fingers within the properties box for each transistor.
5) Have the inputs enter from the bottom of your layout (below gnd rail) and the output leaving the top of the layout (above vdd rail). You can use M1_M2 contact (via) to go from Metal 1 layer to Metal 2 layer. The metal 2 layer can run over the Metal 1 layer (vdd and gnd rails). The inputs and outputs of your circuit should be on the Metal 1 layer.

2(b) Run the DRC

2(c) Do the extraction

2(d) Run LVS to compare the netlist of the schematic to the netlist of the extracted layout. Make sure the netlists match.

2(e) Print out a copy of your layout

Design > Plot > Submit

Be sure you fit the design to your window and select "Viewing Area" for plotting.

2(f) Provide the path to the library for lab 3 in which you have all your completed cells.