Lab 2:
Common Source Amplifiers

In this lab, you will design and simulate common source amplifiers having different types of loads. A comparison of hand calculations to actual simulation results will be done. The types of loads used will be

1) Ideal Current Source
2) Resistor
3) Diode Connected PMOS

An NMOS transistor will be used as the amplification device for all loads. This NMOS transistor will have the following characteristics for the entire lab:
Vth=.56 V, mCox=190 uA/V^2, λ=0.02, and L(Length)=1 um
Note: Vth, mCox, and λ are very approximate values.

1)   Start Cadence and create a new library for Lab 2 and a new cell for the first circuit. Start by drawing the schematic shown in *Figure 1*.   There are two DC sources at the input of the amplifier. One is to bias the circuit to the desired operating point. You will choose the value of VBIAS. The other DC source will be used as the small signal input to the transistor. We will sweep the voltage of this source, *vgs*. The load for part 1 will be an ideal current source. This can be found in the *analogLib* as cell *idc*. Also, names have been given to the nodes *Vin* and *Vout*, so we can refer to them in this lab.
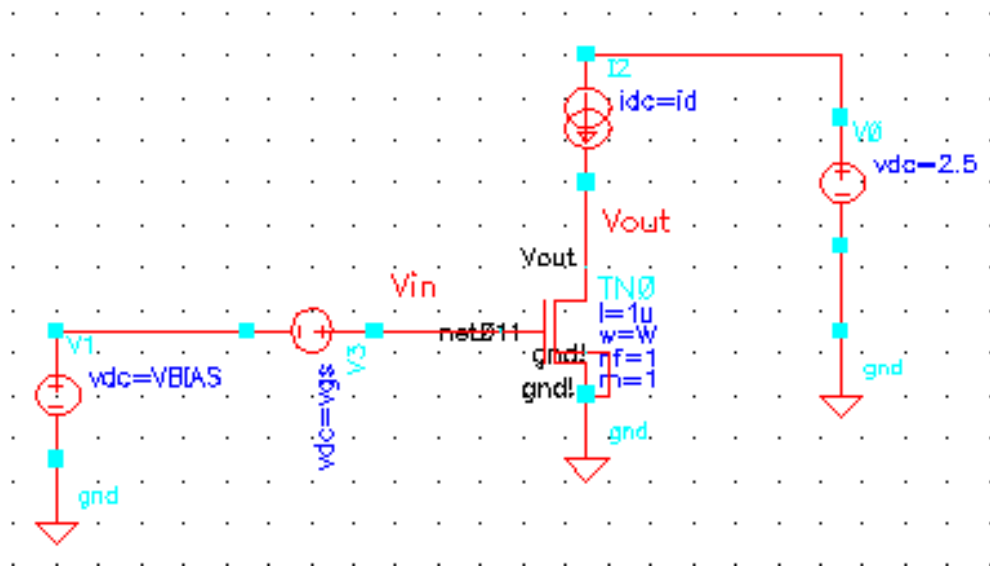

Fig 1. Schematic for Part 1

1(a)   If Id=100uA and Vdsat   .2 V, calculate the maximum theoretical gain using hand calculations. Determine *W* (the width of the transistor) and VBIAS (bias voltage) for maximum gain.

1(b)   Enter these values into your schematic. Save your design and go to the Analog Environment. Initialize the value of the variable *vgs* to 0. This is done so that when the DC operating point of the amplifier is found, only VBIAS will be present at the gate of the transistor. Set up a DC analysis to linearly sweep *vgs* from 0 to 10 uV. Also, check the checkbox to save the DC operating point. Run the simulation. To examine the DC operating point of the transistor, click on Results > DC Operating Point. Then click on the NMOS transistor in the schematic. A new window showing the DC operating point of the transistor should open. Examine the values of vgs, vds, vdsat, vth, etc. and make sure that they are appropriate for the design. The simulation values will often be quite different from hand calculations, so you have to "tweak" the design. Modify W and VBIAS to satisfy the design constraints in simulation. Note any of these changes.

1(c)   Find the value of λ around the chosen operating point by plotting Id vs. Vds at the chosen value of Vgs. You can revert to the Lab 1 Part 1 schematic, and fix vgs to your design value VBIAS. Sweep VDS from 0 to 2.5 V. Print this waveform. From your plot, you will see that in practice, the value of Vds must actually be somewhat greater than Vdsat to be in saturation. For our purposes, let's apply the additional constraint Vds   Vdsat + 200 mV. This will lower the value of λ, thus decreasing gds, and increasing the output resistance. In turn, we will get more gain. Now, make any additional modifications to your design to satisfy this additional requirement. Also, determine the new operating point of the transistor and print out a copy of this.

1(d)   We will use the calculator to determine the small signal input and output, and thus the gain. Enter the expression
        VS("/Vout")-VDC("/Vout")
into the calculator either by manually typing it in or using the calculator buttons and clicking on the nodes in the schematic. Plot this waveform. This is the small signal output voltage due to the small signal input voltage. The total voltage at the output is due to the large and small input signals. We subtract the VDC("/Vout") voltage (large signal) from the total output to get the small signal voltage. Now, plot
        VS("/Vin")-VDC("/Vin")
This is the small signal input voltage. Print these plots and hand in. You can print both on the same sheet on different axes by using the *switch axis mode* we used in the tutorial. Find the gain. Compare the simulated gain to theoretical gain.

2)   Now, replace the current source load with a resistor. Use an ideal resistor. This is located in the *analogLib* as the cell *res*. Your schematic should now look like *Figure. 2*. Determine the maximum gain for this configuration and the corresponding values of R (resistance), VBIAS, and *W* (Width). Remember, the transistor must be in saturation, with Vdsat   .2 V and Vds   Vdsat + 200mV. Again, do the same DC analysis that was done in Part 1. Change the design parameters after simulation if need be. Print out a copy of the DC operating point of the transistor. Find the gain, print the small signal input and output signals, and compare theoretical results to simulated results.

R0
r=R

V0
vdc=2.5

Vout

Vin

Vout

nfet TN0
l=1u
w=W
gnd! nf=1
gnd! m=1

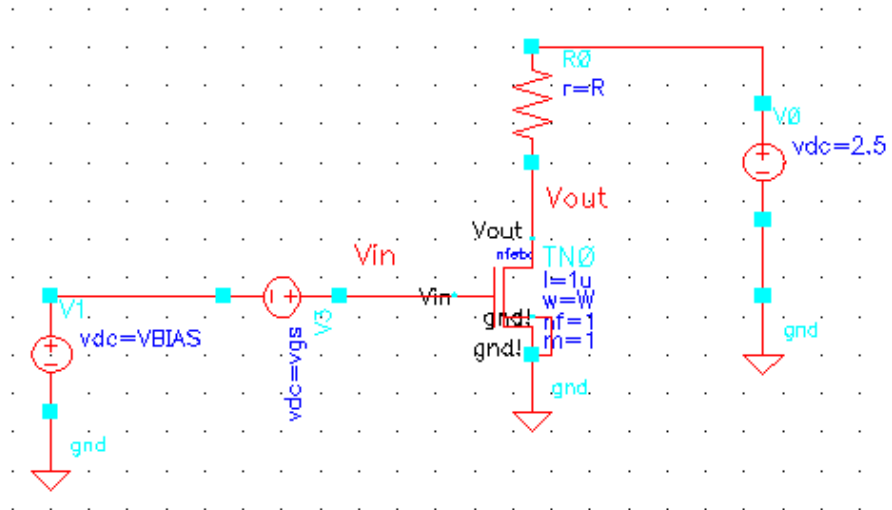V1.
vdc=VBIAS

V3
vdc=vgs

Vin

gnd

gnd

gnd

Fig 2. Schematic for Part 2

3)   Replace the resistor with a diode connected PMOS. This is the *pfetx* cell in the *cmrf6sf* library. The new schematic is shown in *Figure 3*. This PMOS will have the following characteristics:

V_{th}=-.49 V, unCox= 4.75 upCox, L(Length)=1 um
Note: These values are only approximations. As |VGS| is increased far beyond the minimum value, for instance, the mobility can decrease by even a factor of 2 or more.

The design constraints once again are Id=100uA, Vdsat   .2 V and Vd   Vdsat + 200mV Determine VBIAS, W for the NMOS, and W for the PMOS transistors that will give the maximum gain. Enter these values into the schematic and simulate. Make sure the design conditions are being met. Print out a copy of the DC operating point of both transistors. If not, tweak the values in your design so that the conditions are being met. Note these changes. Sweep vgs again from 0 to 10 uV, measure the gain, and compare to theoretical gain. Print your small signal input and output waveforms.

pfet TP0
l=1u
w=WP
nf=1
m=1

V0
vdc=2.5

Vout

Vout

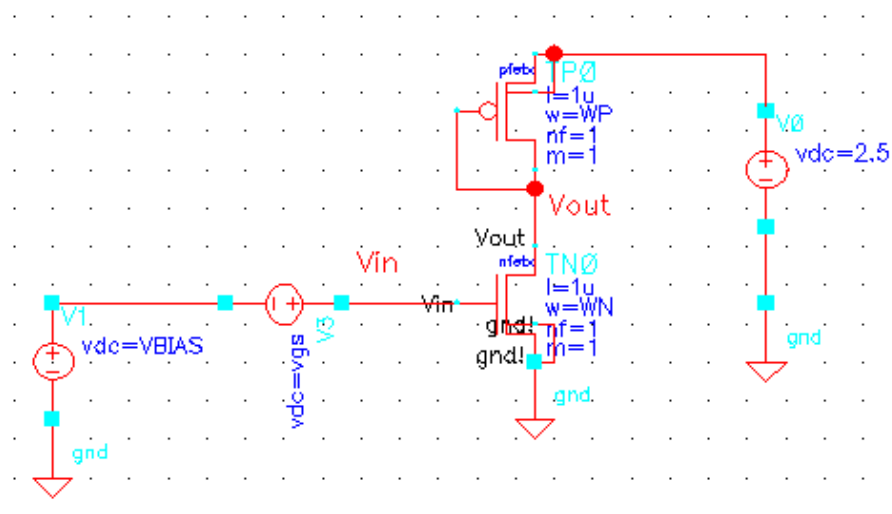Vin

nfet TN0
l=1u
w=WN
gnd! nf=1
gnd! m=1

V1.
vdc=VBIAS

V3
vdc=vgs

Vin

gnd

gnd

gnd

Fig 3. Schematic for Part 3