Lab 1:
MOSFET Characterization using Cadence

This lab is intended to familiarize you with the Cadence software and the MOSFET devices that we will be using throughout the semester in larger circuit simulations. We will simulate the voltage-current relationships of a NMOS transistor in Cadence and estimate some process parameters using the simulation results. Finally the body effect and its relation to the threshold voltage will be simulated.

Start Cadence and create a new library for Lab1. Create a new cell within this library and draw the schematic shown in *Figure 1*. This schematic will be used to simulate the relationship between Vgs, Vds, and Id for a single NMOS transistor.

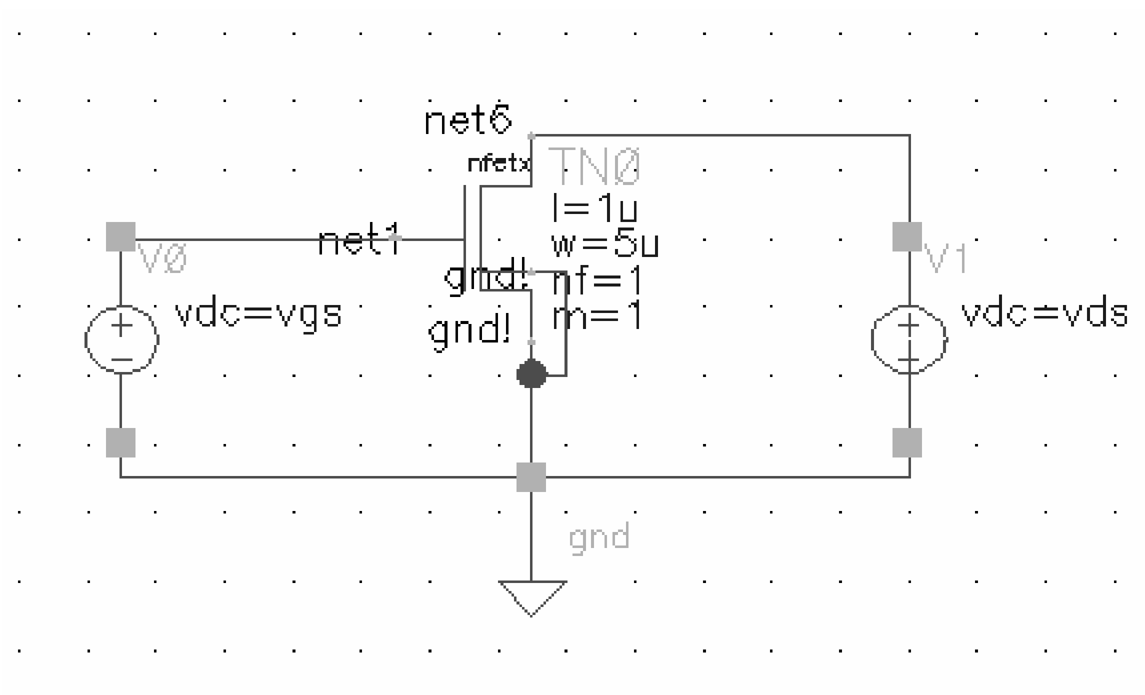

Fig 1. Schematic for Parts 1-4

1) The DC voltage of the two sources is set to the variable names *vgs* and *vds*. Later, we will sweep these variables. The transistor has length=1 um and width=5 um. Check and Save the design and enter the Analog Environment. Make sure the Model Libraries and Simulation Files are setup as was done in the inverter tutorial. Copy the variables from the cellview and set *vds* and *vgs* to 2.5 V. We would like to save the output current from the transistor. This must be done manually. Go to Outputs > To be Saved > Select on Schematic. Click on the drain pin (the square terminal, not the wire) of the transistor in the schematic. The output “TNO/D” should now appear in the Outputs list.

First we will simulate Id vs. *vds* for different values of *vgs*. This simulation requires the sweeping of two variables. We will sweep *vds* in the dc analysis, and *vgs* using the parametric sweep tool. First setup a dc analysis, sweeping the design variable *vds* from 0 to 2.5 V. The Sweep Type in this case can be set to Automatic. Click the *Netlist and Run* Icon. Now, go to Tools > Parametric Analysis. Enter *vgs* for the variable name, sweep it from 0 to 2.5 V using 6 total steps. Go to Analysis > Start. Go back to the Analog Environment window when this simulation is complete. We will view the output using the Calculator tool. This is found in Tools > Calculator. The calculator is a very powerful tool; it gives the user the ability to customize the plots and apply built in functions to data. To plot the current-voltage characteristics of this transistor, click on the *is* button on the calculator, and then click on the drain terminal of the nfetx in the schematic. Push the *plot* button in the calculator. Id vs. vds for different values of vgs should appear in a new window. Print this and hand it in. From this plot, determine λ.

2) Change the width of the transistor to 10 um and the length to 2 um. Plot the Id vs. *vds* curve for *vgs* from 0 to 2.5 V in 6 steps (like in part 1). Print this and hand it in. Determine λ at VGS=1 V and VGS=2.5 V. Explain the difference between 1) and 2).

3) Now, we will plot Id vs. *vgs* for a fixed value of *vds*. Change the size of the transistor back to its original size (length=1 um, width=5 um). Set up a new dc analysis, sweeping *vgs* from 0 to 2.5. An automatic sweep type will work fine here. If you remember, we already set the *vds* Design Variable to 2.5 V at the beginning of this lab. So, if this variable is not swept, it will remain at 2.5 V for this simulation. Click on *Netlist and Run*, and plot Id using the calculator, as we did in Part 1. You should now obtain the Id vs. *vgs* curve with *vds* at 2.5 V. We would also like to plot the square root of Id. Using this plot we can estimate the threshold voltage V_{th} for this transistor. Go back to the calculator and the expression IS("/TN0/D") should still appear in the window. We want to take the sqrt of this, so press the *sqrt* button on the calculator. The button pressed on the calculator operates on the expression that is already displayed (The calculator uses Reverse Polish Notation). Now, sqrt(IS("/TN0/D") should appear in the window. Push the *erplot* button. This will erase all previous plots and plot the expression in a new window. Print this curve and hand it in. Using this curve estimate the value for V_{th}. Hint. Use linear extrapolation.

4) Let's see how gm varies with *vgs*. In the calculator, make sure IS("/TN0/D") is displayed as the current expression. We would like to take the derivative of this curve to find how gm varies with *vgs*. Go to the Special Functions button on the calculator, then click on the *deriv* button. The new expression should be deriv(IS("/TN0/D")). Plot this waveform, print, and hand in. Using the equations from class, determine gm at *vgs*=1.5 V. Compare to the value on the plot.

5) Finally, we would like to see how the body effect changes V_{th}. Add a 1 V dc voltage source from the source of the transistor to ground. Now there is a difference in potential between source and bulk. The negative terminal of the *vgs* voltage source should now be connected to the source of the transistor, instead of ground. These changes are shown in *Figure 2*. Repeat part 4 with this new circuit. Determine V_{th} from the plot. Explain the how the body effect has changed V_{th}. There is no need to calculate V_{th} by hand.

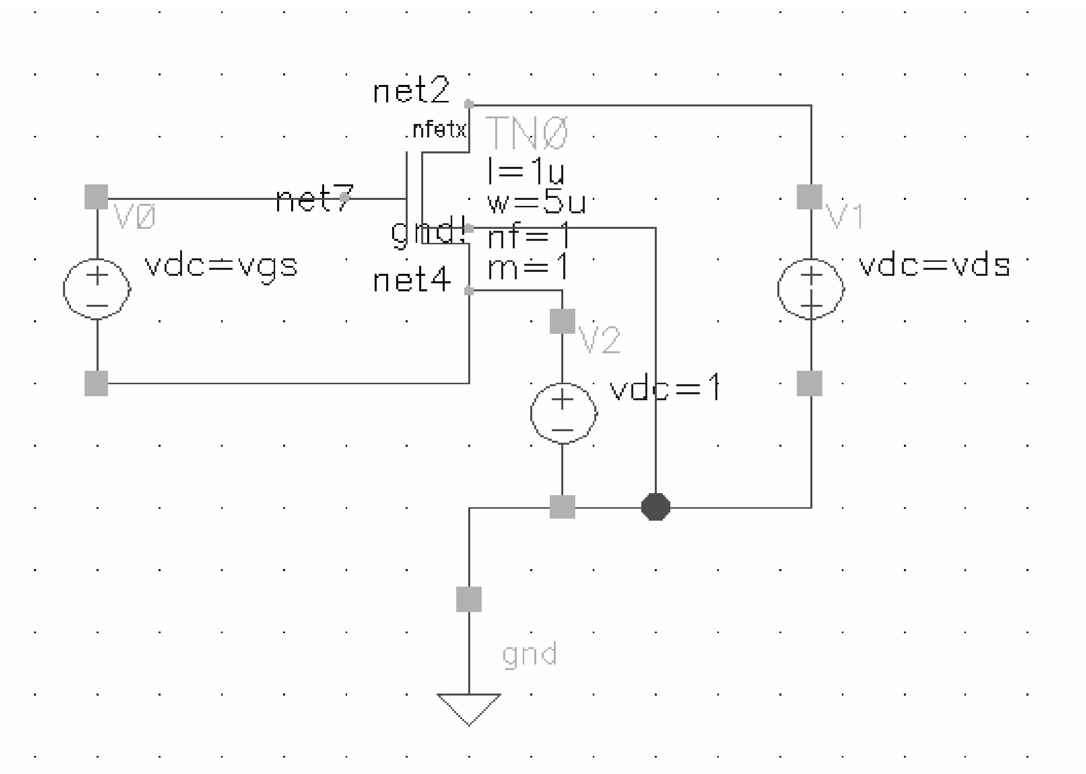

Fig. 2. Schematic for Part 5