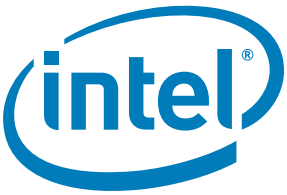

Intel® Core™2 Duo Processor and Intel® Core™2 Extreme Processor on 45-nm Process for Platforms Based on Mobile Intel® 965 Express Chipset Family

Datasheet

January 2008

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Revision History

Document Number	Revision Number	Description	Date
318914	-001	Initial release	January 2008

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1 Introduction

The Intel® Core™2 Duo processor and Intel® Core™2 Extreme processor built on 45-nanometer process technology are the next generation high-performance, low-power mobile processors based on the Intel® Core™ microarchitecture. The Intel Core 2 Duo processor and Intel Core 2 Extreme processor support the Mobile Intel® 965 Express Chipset and Intel® 82801HBM ICH8 Controller Hub-Based Systems. The document contains electrical, mechanical and thermal specifications for the following processors:

- Intel Core 2 Duo processor - Standard Voltage
- Intel Core 2 Extreme processor

Note: In this document, the Intel Core 2 Duo processor and Intel Core 2 Extreme mobile processor built on 45-nm process technology are referred to as the processor. The Mobile Intel® 965 Express Chipset family is referred to as the (G)MCH.

The following list provides some of the key features on this processor:

- Dual-core processor for mobile with enhanced performance.
- Supports Intel® architecture with Intel® Wide Dynamic Execution.
- Supports L1 cache-to-cache (C2C) transfer.
- Supports PSI2 functionality.
- Supports Enhanced Intel® Virtualization Technology.
- On-die, primary 32-KB instruction cache and 32-KB write-back data cache in each core.
- On-die, up to 6-MB second-level shared cache with Advanced Transfer Cache Architecture.
- Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3), Supplemental Streaming SIMD Extensions 3 (SSSE3) and SSE4.1 Instruction Sets.
- 800-MHz Source-Synchronous front side bus (FSB).
- Advanced power management features including Enhanced Intel SpeedStep® Technology and Dynamic FSB frequency switching.
- Digital Thermal Sensor (DTS).
- Intel® 64 architecture.
- Intel® Dynamic Acceleration Technology and Enhanced Multi-Threaded Thermal Management (EMTTM).
- Micro-FCPGA and Micro-FCBGA packaging technologies (Extreme Edition only available in Micro-FCPGA).
- Execute Disable Bit support for enhanced security.
- Deep Power-Down Technology with P_LVL6 I/O Support.
- Half-ratio support (N/2) for Core-to-Bus ratio.

1.1 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel® processors.
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to laptops.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® Architecture Software Developer's Manual* for more detailed information.
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the chipset components).
Half ratio support (N/2) for Core to Bus ratio	Penryn processor support the N/2 feature which allows having fractional core to bus ratios. This feature provides the flexibility of having more frequency options and be able to have products with smaller frequency steps.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
Intel® Virtualization Technology	Processor virtualization which, when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
Processor Core	Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.
Storage Conditions	Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TDP	Thermal Design Power.
V_{CC}	The processor core power supply.
V_{SS}	The processor ground.

1.2 References

Document	Document Number
Intel® Core™2 Duo Mobile Processor and Intel® Core™2 Extreme Processor on 45-nm Technology Specification Update	318915
Mobile Intel® 965 Express Chipset Family Datasheet	316273
Mobile Intel® 965 Express Chipset Family Specification Update	316274
Intel® I/O Controller Hub 8 (ICH8)/ I/O Controller Hub 8M (ICH8M) Datasheet	See http://www.intel.com/design/chipsets/datashts/313056.htm
Intel® I/O Controller Hub 8 (ICH8)/ I/O Controller Hub 8M (ICH8M) Specification Update	See http://www.intel.com/design/chipsets/specupdt/313057.htm
Intel® 64 and IA-32 Architectures Software Developer's Manual	See http://www.intel.com/design/pentium4/manuals/index_new.htm
Intel® 64 and IA-32 Architectures Software Developer's Manuals Documentation Change	See http://developer.intel.com/design/processor/specupdt/252046.htm
Volume 1: Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669

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2 Low Power Features

2.1 Clock Control and Low-Power States

The processor supports low-power states both at the individual core level and the package level for optimal power management.

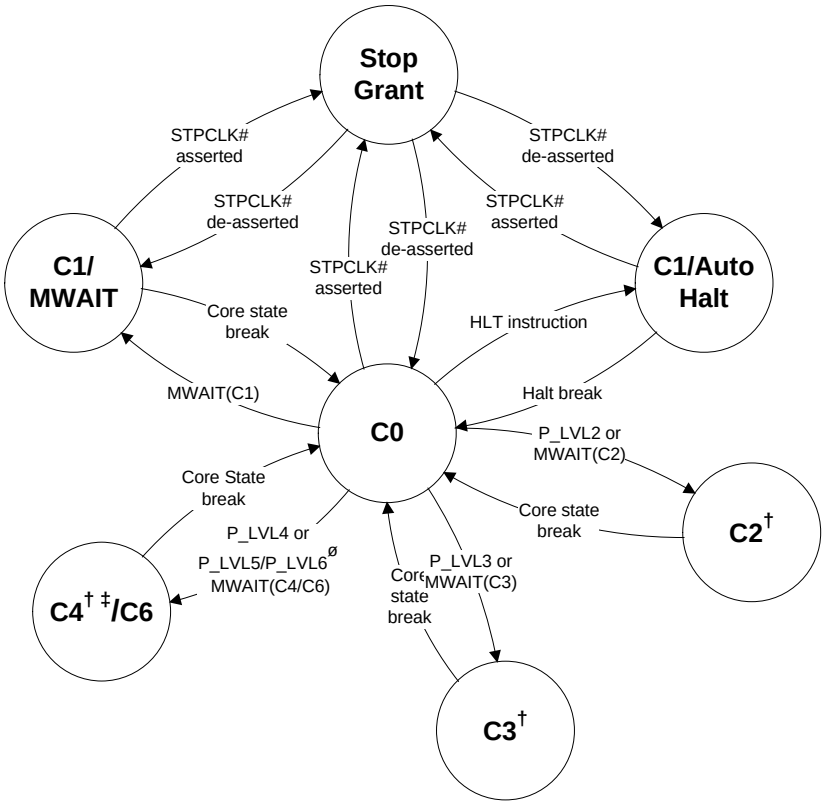
A core may independently enter the C1/AutoHALT, C1/MWAIT, C2, C3, C4, Intel® Enhanced Deeper Sleep, and Intel Deep Power-Down low-power states. When both cores coincide in a common core low-power state, the central power management logic ensures the entire processor enters the respective package low-power state by initiating a P_LVLx (P_LVL2, P_LVL3, P_LVL4, P_LVL5,P_LVL6) I/O read to the (G)MCH.

The processor implements two software interfaces for requesting low-power states: MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor and do not directly result in I/O reads on the processor FSB. The P_LVLx I/O Monitor address does not need to be set up before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured through the IA32_MISC_ENABLES model-specific register (MSR).

If a core encounters a chipset break event while STPCLK# is asserted, it then asserts the PBE# output signal. Assertion of PBE# when STPCLK# is asserted indicates to the system logic that individual cores should return to the C0 state and the processor should return to the Normal state.

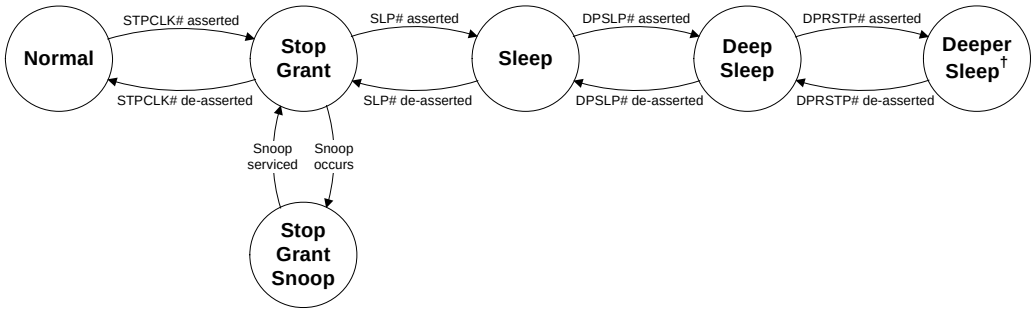
Figure 1 shows the core low-power states and Figure 2 shows the package low-power states for the processor. Table 1 maps the core low-power states to package low-power states.

Figure 1. Core Low-Power States



halt break = A20M# transition, INIT#, INTR, NMI, PREQ#, RESET#, SMI#, or APIC interrupt
core state break = (halt break OR Monitor event) AND STPCLK# high (not asserted)
† — STPCLK# assertion and de-assertion have no effect if a core is in C2, C3, or C4.
‡ — Core C4 state supports the package level Intel Enhanced Deeper Sleep state.
Ø — P_LVL5/P_LVL6 read is issued once the L2 cache is reduced to zero.

Figure 2. Package Low-Power States



† — Deeper Sleep includes the Deeper Sleep state, Intel Enhanced Deeper Sleep state, and C6 state

Table 1. Coordination of Core Low-Power States at the Package Level

Package State	Core 1 State				
Core 0 State	**C0**	**C1**	**C2**	**C3**	**C4/C6**
C0	Normal	Normal	Normal	Normal	Normal
C1[1]	Normal	Normal	Normal	Normal	Normal
C2	Normal	Normal	Stop-Grant	Stop-Grant	Stop-Grant
C3	Normal	Normal	Stop-Grant	Deep Sleep	Deep Sleep
C4/C6	Normal	Normal	Stop-Grant	Deep Sleep	Deeper Sleep/Intel® Enhanced Deeper Sleep/ Intel® Deep Power-Down

NOTES:
1. AutoHALT or MWAIT/C1.

2.1.1 Core Low-Power State Descriptions

2.1.1.1 Core C0 State

This is the normal operating state for cores in the processor.

2.1.1.2 Core C1/AutoHALT Power-Down State

C1/AutoHALT is a low-power state entered when a core executes the HALT instruction. The processor core will transition to the C0 state upon occurrence of SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt messages. RESET# will cause the processor to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT power-down state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 3A/3B: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT power-down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT power-down state, the dual-core processor will process bus snoops and snoops from the other core. The processor core will enter a snoopable sub-state (not shown in Figure 1) to process the snoop and then return to the AutoHALT power-down state.

2.1.1.3 Core C1/MWAIT Power-Down State

C1/MWAIT is a low-power state entered when the processor core executes the MWAIT(C1) instruction. Processor behavior in the MWAIT state is identical to the AutoHALT state except that Monitor events can cause the processor core to return to the C0 state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 2A: Instruction Set Reference, A-M* and *Volume 2B: Instruction Set Reference, N-Z*, for more information.

2.1.1.4 Core C2 State

Individual cores of the dual-core processor can enter the C2 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C2) instruction, but the processor will not issue a Stop-Grant Acknowledge special bus cycle unless the STPCLK# pin is also asserted.

While in the C2 state, the dual-core processor will process bus snoops and snoops from the other core. The processor core will enter a snoopable sub-state (not shown in Figure 1) to process the snoop and then return to the C2 state.

2.1.1.5 Core C3 State

Individual cores of the dual-core processor can enter the C3 state by initiating a P_LVL3 I/O read to the P_BLK or an MWAIT(C3) instruction. Before entering C3, the processor core flushes the contents of its L1 caches into the processor's L2 cache. Except for the caches, the processor core maintains all its architecture in the C3 state. The monitor remains armed if it is configured. All of the clocks in the processor core are stopped in the C3 state.

Because the core's caches are flushed the processor keeps the core in the C3 state when the processor detects a snoop on the FSB or when the other core of the dual-core processor accesses cacheable memory. The processor core will transition to the C0 state upon occurrence of a Monitor event, SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt message. RESET# will cause the processor core to immediately initialize itself.

2.1.1.6 Core C4 State

Individual cores of the dual-core processor can enter the C4 state by initiating a P_LVL4 or P_LVL5 I/O read to the P_BLK or an MWAIT(C4) instruction. The processor core behavior in the C4 state is nearly identical to the behavior in the C3 state. The only difference is that if both processor cores are in C4, the central power management logic will request that the entire processor enter the Deeper Sleep package low-power state (see Section 2.1.2.6).

To enable the package-level Intel Enhanced Deeper Sleep state, Dynamic Cache Sizing and Intel Enhanced Deeper Sleep state fields must be configured in the PMG_CST_CONFIG_CONTROL MSR. Refer to Section 2.1.2.6 for further details on Intel Enhanced Deeper Sleep state.

2.1.1.7 Core C6 State

C6 is a radical, new, power-saving state which is being implemented on this processor. In C6 the processor saves its entire architectural state onto an on-die SRAM, hence allowing it to run at a voltage V_{C6} that is lower than Enhanced Deeper Sleep voltage.

An individual core of the dual-core processor can enter the C6 state by initiating a P_LVL6 I/O read to the P_BLK or an MWAIT(C6) instruction. The primary method to enter C6 used by newer operating systems (that support MWAIT) will be through the MWAIT instruction.

When the core enters C6, it saves the processor state that is relevant to the processor context in an on-die SRAM that resides on a separate power plane V_{CCP} (I/O power supply). This allows the main core V_{CC} to be lowered to a very low-voltage V_{C6}. The on-die storage for saving the processor state is implemented as a per-core SRAM. The microcode performs the save and restore of the processor state on entry and exit from C6, respectively.

2.1.2 Package Low-Power State Descriptions

2.1.2.1 Normal State

This is the normal operating state for the processor. The processor remains in the Normal state when at least one of its cores is in the C0, C1/AutoHALT, or C1/MWAIT state.

2.1.2.2 Stop-Grant State

When the STPCLK# pin is asserted, each core of the dual-core processor enters the Stop-Grant state within 20 bus clocks after the response phase of the processor-issued Stop-Grant Acknowledge special bus cycle. Processor cores that are already in the C2, C3, or C4 state remain in their current low-power state. When the STPCLK# pin is deasserted, each core returns to its previous core low-power state.

Since the AGTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to V_{CCP}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.

RESET# causes the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. When RESET# is asserted by the system, the STPCLK#, SLP#, DPSLP#, and DPRSTP# pins must be deasserted prior to RESET# deassertion as per AC Specification T45. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be deasserted after the deassertion of SLP#, as per AC Specification T75.

While in Stop-Grant state, the processor will service snoops and latch interrupts delivered on the FSB. The processor will latch SMI#, INIT# and LINT[1:0] interrupts and will service only one of each upon return to the Normal state.

The PBE# signal may be driven when the processor is in the Stop-Grant state. PBE# will be asserted if there is any pending interrupt or Monitor event latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that the entire processor should return to the Normal state.

A transition to the Stop-Grant Snoop state occurs when the processor detects a snoop on the FSB (see Section 2.1.2.3). A transition to the Sleep state (see Section 2.1.2.4) occurs with the assertion of the SLP# signal.

2.1.2.3 Stop-Grant Snoop State

The processor responds to snoop or interrupt transactions on the FSB while in Stop-Grant state by entering the Stop-Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. The processor returns to the Stop-Grant state once the snoop has been serviced or the interrupt has been latched.

2.1.2.4 Sleep State

The Sleep state is a low-power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and stops all internal clocks. The Sleep state is entered through assertion of the SLP# signal while in the Stop-Grant state. The SLP# pin should only be asserted when the processor is in the Stop-Grant state. SLP# assertions while the processor is not in the Stop-Grant state is out of specification and may result in unapproved operation.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP# or RESET#) are allowed on the FSB while the processor is in Sleep state. Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior. Any transition on an input signal before the processor has returned to the Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through the Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state, by asserting the DPSLP# pin (See Section 2.1.2.5). While the processor is in the Sleep state, the SLP# pin must be deasserted if another asynchronous FSB event needs to occur.

2.1.2.5 Deep Sleep State

The Deep Sleep state is entered through assertion of the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform level power savings. BCLK stop/restart timings on appropriate chipset-based platforms are as follows:

- **Deep Sleep entry:** the system clock chip may stop/tristate BCLK within two BCLKs of DPSLP# assertion. It is permissible to leave BCLK running during Deep Sleep.
- **Deep Sleep exit:** the system clock chip must drive BCLK to differential DC levels within 2-3 ns of DPSLP# deassertion and start toggling BCLK within 10 BCLK periods.

To re-enter the Sleep state, the DPSLP# pin must be deasserted. BCLK can be re-started after DPSLP# deassertion as described above. A period of 15 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin must be deasserted to re-enter the Stop-Grant state.

While in the Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the FSB while the processor is in the Deep Sleep state. When the processor is in the Deep Sleep state it will not respond to interrupts or snoop transactions.

Warning: Any transition on an input signal before the processor has returned to the Stop-Grant state will result in unpredictable behavior.

2.1.2.6 Deeper Sleep State

The Deeper Sleep state is similar to the Deep Sleep state but further reduces core voltage levels. One of the potential lower core voltage levels is achieved by entering the base Deeper Sleep state. The Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep state. The following lower core voltage level is achieved by entering the Intel Enhanced Deeper Sleep state, which is a sub-state of the Deeper Sleep state. Intel Enhanced Deeper Sleep state is entered through assertion of the DPRSTP# pin while in the Deep Sleep only when the L2 cache has been completely shut down. Refer to Section 2.1.2.6.1 and Section 2.1.2.6.3 for further details on reducing the L2 cache and entering the Intel Enhanced Deeper Sleep state.

In response to entering Deeper Sleep, the processor drives the VID code corresponding to the Deeper Sleep core voltage on the VID[6:0] pins. Refer to the platform design guides for further details.

Exit from Deeper Sleep or the Intel Enhanced Deeper Sleep state is initiated by DPRSTP# deassertion when either core requests a core state other than C4 or either core requests a processor performance state other than the lowest operating point.

2.1.2.6.1 Intel® Enhanced Deeper Sleep State

Intel Enhanced Deeper Sleep state is a sub-state of Deeper Sleep that extends power saving capabilities by allowing the processor to further reduce core voltage once the L2 cache has been reduced to zero ways and completely shut down. The following events occur when the processor enters the Intel Enhanced Deeper Sleep state:

- The last core entering C4 issues a P_LVL4 or P_LVL5 I/O read or an MWAIT(C4) instruction and then progressively reduces the L2 cache to zero.
- Once the L2 cache has been reduced to zero, the processor triggers a special chipset sequence to notify the chipset to redirect all FSB traffic, except APIC messages, to memory. The snoops are replied as misses by the chipset and are directed to main memory instead of the L2 cache. This allows for higher residency of the processor's Intel Enhanced Deeper Sleep state.
- The processor drives the VID code corresponding to the Intel Enhanced Deeper Sleep state core voltage on the VID[6:0] pins.

2.1.2.6.2 Intel® Deep Power-Down State (Previously known as Package C6 State)

When both cores have entered the CC6 state and the L2 cache has been shrunk down to zero ways, the processor will enter the Intel Deep Power-Down state or C6 state. To do so both cores save their architectural states in the on-die SRAM that resides in the V_{CCP} domain. At this point, the core V_{CC} will be dropped to the lowest core voltage V_{C6}. The processor is now in an extremely low-power state.

In the Intel Deep Power-Down state, the processor does not need to be snooped, as all the caches are flushed before entering C6.

C6 exit is triggered by the chipset when it detects a break event. It deasserts the DPRSTP#, DPSLP#, SLP#, and STPCLK# pins to exit the processor out of the C6 state. At DPSLP# deassertion, the core V_{CC} ramps up to the LFM value and the processor starts up its internal PLLs. At SLP# deassertion the processor is reset and the architectural state is read back into the cores from an on-die SRAM. The restore will be done in both cores irrespective of the break event and which core it is directed to. The C6 exit event will put both cores in CC0.

Refer to Figure 3 and Figure 4 for C6 entry sequence and exit sequence.

Figure 3. C6 Entry Sequence

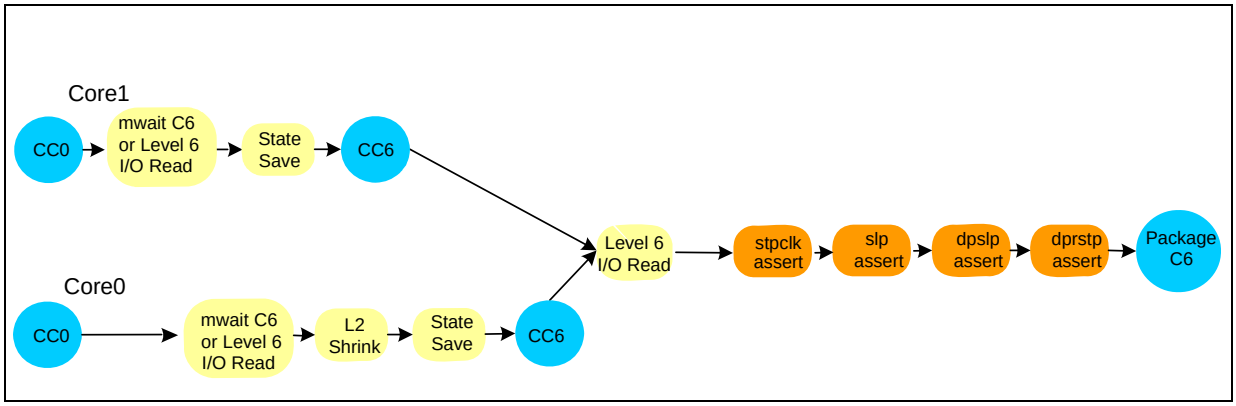
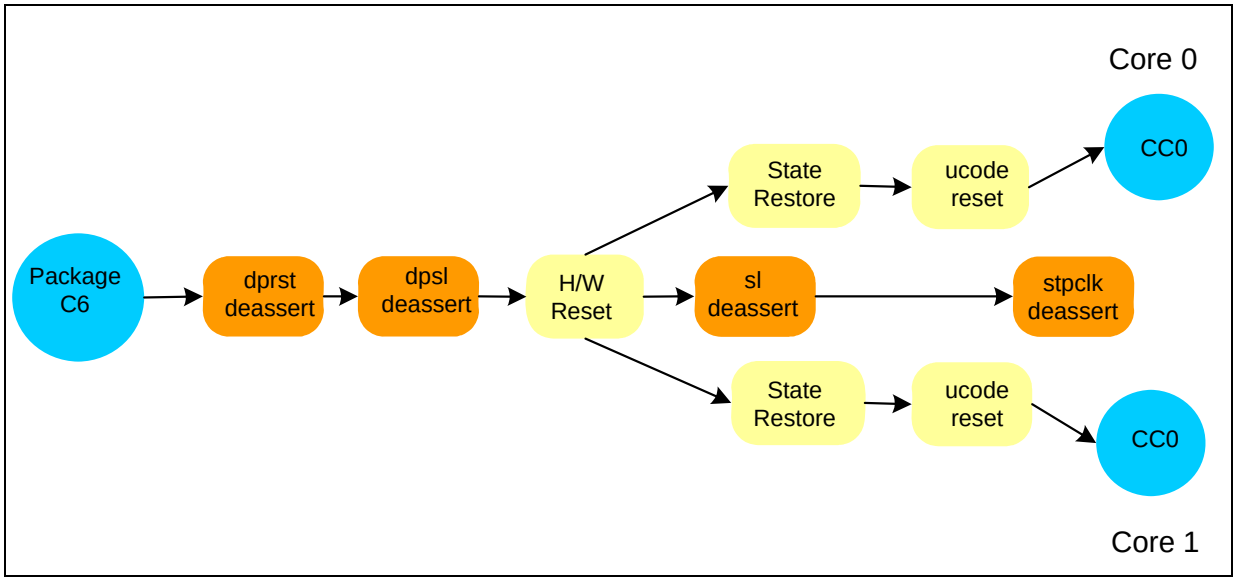


Figure 4. C6 Exit Sequence



2.1.2.6.3 Dynamic Cache Sizing

Dynamic Cache Sizing allows the processor to flush and disable a programmable number of L2 cache ways upon each Deeper Sleep entry under the following conditions:

- The second core is already in C4 and Intel Enhanced Deeper Sleep state or C6 state is enabled (as specified in Section 2.1.1.6).
- The C0 timer that tracks continuous residency in the Normal package state has not expired. This timer is cleared during the first entry into Deeper Sleep to allow consecutive Deeper Sleep entries to shrink the L2 cache as needed.
- The FSB speed to processor core speed ratio is below the predefined L2 shrink threshold.

If the FSB speed-to-processor core speed ratio is above the predefined L2 shrink threshold, then L2 cache expansion will be requested. If the ratio is zero, then the ratio will not be taken into account for Dynamic Cache Sizing decisions.

Upon STPCLK# deassertion, the first core exiting the Intel Enhanced Deeper Sleep state or C6 will expand the L2 cache to two ways and invalidate previously disabled cache ways. If the L2 cache reduction conditions stated above still exist when the last core returns to C4 and the package enters the Intel Enhanced Deeper Sleep state or C6, then the L2 will be shrunk to zero again. If a core requests a processor performance state resulting in a higher ratio than the predefined L2 shrink threshold, the C0 timer expires, or the second core (not the one currently entering the interrupt routine) requests the C1, C2, or C3 states, then the whole L2 will be expanded upon the next interrupt event.

In addition, the processor supports Full Shrink on L2 cache. When the MWAIT C6 instruction is executed with a hint=0x2 in ECX[3:0], the micro code will shrink all the active ways of the L2 cache in one step. This ensures that the package enters C6 immediately when both cores are in CC6 instead of iterating till the cache is reduced to zero. The operating system (OS) is expected to use this hint when it wants to enter the lowest power state and can tolerate the longer entry latency.

L2 cache shrink prevention may be enabled as needed on occasion through an MWAIT(C4) sub-state field. If shrink prevention is enabled, the processor does not enter Intel Enhanced Deeper Sleep state or C6 since the L2 cache remains valid and in full size.

2.2 Enhanced Intel SpeedStep® Technology

The processor features Enhanced Intel SpeedStep Technology. The key features of Enhanced Intel SpeedStep Technology follow:

- Multiple voltage and frequency operating points provide optimal performance at the lowest power.
- Voltage and frequency selection is software controlled by writing to processor MSRs:
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps by placing new values on the VID pins, and the PLL then locks to the new frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the new frequency, and the V_{CC} is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. If a previous transition is in progress the new transition is deferred until the previous transition completes.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Low transition latency and large number of transitions possible per second:
  - Processor core (including L2 cache) is unavailable for up to 10 µs during the frequency transition.
  - The bus protocol (BNR# mechanism) is used to block snooping.

- Improved Intel® Thermal Monitor mode:
  - When the on-die thermal sensor indicates that the die temperature is too high, the processor can automatically perform a transition to a lower frequency and voltage specified in a software-programmable MSR.
  - The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up-transition to the previous frequency and voltage point occurs.
  - An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system-level thermal management.
- Enhanced thermal management features:
  - Digital Thermal Sensor and Out of Specification detection
  - Intel® Thermal Monitor 1 (TM1) in addition to Intel Thermal Monitor 2 (TM2) in case of unsuccessful TM2 transition.
  - Dual-core thermal management synchronization.

Each core in the dual processor implements an independent MSR for controlling Enhanced Intel SpeedStep Technology, but both cores must operate at the same frequency and voltage. The processor has performance state coordination logic to resolve frequency and voltage requests from the two cores into a single frequency and voltage request for the package as a whole. If both cores request the same frequency and voltage, then the processor will transition to the requested common frequency and voltage. If the two cores have different frequency and voltage requests, then the processor will take the highest of the two frequencies and voltages as the resolved request and transition to that frequency and voltage.

The processor also supports Dynamic FSB Frequency Switching and Intel Dynamic Acceleration Technology mode on select SKUS. The operating system can take advantage of these features and request a lower operating point called SuperLFM (due to Dynamic FSB Frequency Switching) and a higher operating point Intel Dynamic Acceleration Technology mode.

2.3 Extended Low-Power States

Extended low-power states (C1E, C2E, C3E, C4E, C6E) optimize for power by forcibly reducing the performance state of the processor when it enters a package low-power state. Instead of directly transitioning into the package low-power state, the enhanced package low-power state first reduces the performance state of the processor by performing an Enhanced Intel SpeedStep Technology transition down to the lowest operating point. Upon receiving a break event from the package low-power state, control will be returned to software while an Enhanced Intel SpeedStep Technology transition up to the initial operating point occurs. The advantage of this feature is that it significantly reduces leakage while in low-power states.

C6 is always enabled in the extended low-power state, as described above.

Note: Long-term reliability cannot be assured unless all the extended low power states are enabled.

The processor implements two software interfaces for requesting extended package low-power states: MWAIT instruction extensions with sub-state hints and via BIOS by configuring IA32_MISC_ENABLES MSR bits to automatically promote package low-power states to extended package low-power states.

Extended Stop-Grant and Enhanced Deeper Sleep must be enabled via the BIOS for the processor to remain within specification. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor. As processor technology changes, enabling the extended low-power states becomes increasingly crucial when building computer systems. Maintaining the proper BIOS configuration is key to reliable, long-term system operation. Not complying to this guideline may affect the long-term reliability of the processor.

Caution: Enhanced Intel SpeedStep Technology transitions are multi-step processes that require clocked control. These transitions cannot occur when the processor is in the Sleep or Deep Sleep package low-power states since processor clocks are not active in these states. Extended Deeper Sleep is an exception to this rule when the Hard C4E configuration is enabled in the IA32_MISC_ENABLES MSR. This Extended Deeper Sleep state configuration will lower core voltage to the Deeper Sleep level while in Deeper Sleep and, upon exit, will automatically transition to the lowest operating voltage and frequency to reduce snoop service latency. The transition to the lowest operating point or back to the original software requested point may not be instantaneous. Furthermore, upon very frequent transitions between active and idle states, the transitions may lag behind the idle state entry resulting in the processor either executing for a longer time at the lowest operating point or running idle at a high operating point. Observations and analyses show this behavior should not significantly impact total power savings or performance score while providing power benefits in most other cases.

2.4 FSB Low-Power Enhancements

The processor incorporates FSB low-power enhancements:

- Dynamic FSB Power-Down
- BPRI# control for address and control input buffers
- Dynamic Bus Parking
- Dynamic On-Die Termination disabling
- Low V_{CCP} (I/O termination voltage)
- Dynamic FSB frequency switching

The processor incorporates the DPWR# signal that controls the data bus input buffers on the processor. The DPWR# signal disables the buffers when not used and activates them only when data bus activity occurs, resulting in significant power savings with no performance impact. BPRI# control also allows the processor address and control input buffers to be turned off when the BPRI# signal is inactive. Dynamic Bus Parking allows a reciprocal power reduction in chipset address and control input buffers when the processor deasserts its BR0# pin. The On-Die Termination on the processor FSB buffers is disabled when the signals are driven low, resulting in additional power savings. The low I/O termination voltage is on a dedicated voltage plane independent of the core voltage, enabling low I/O switching power at all times.

2.4.1 Dynamic FSB Frequency Switching

Dynamic FSB frequency switching effectively reduces the internal bus clock frequency in half to further decrease the minimum processor operating frequency from the Enhanced Intel SpeedStep Technology performance states and achieve the Super Low Frequency Mode (SuperLFM). This feature is supported at FSB frequencies of 800-MHz on the Santa Rosa platform and does not entail a change in the external bus signal (BCLK) frequency. Instead, both the processor and (G)MCH internally lower their BCLK reference frequency to 50% of the externally visible frequency. Both the processor and (G)MCH maintain a virtual BCLK signal (“VBCLK”) that is aligned to the external BCLK,

but at half the frequency. After a downward shift, it would appear externally as if the bus is running with a 100-MHz base clock in all aspects except that the actual external BCLK remains at 200 MHz. The transition into Super LFM, a “down-shift,” is done following a handshake between the processor and (G)MCH. A similar handshake is used to indicate an “up-shift,” a change back to normal operating mode. Ensure this feature is enabled and supported in the BIOS.

2.4.2 Intel® Dynamic Acceleration Technology

The processor supports the Intel Dynamic Acceleration Technology mode. The Intel Dynamic Acceleration Technology feature allows one core of the processor to operate at a higher frequency point when the other core is inactive and the operating system requests increased performance. This higher frequency is called the “opportunistic frequency” and the maximum rated operating frequency is the “guaranteed frequency.”

Note: Extreme Edition processors do not support Intel Dynamic Acceleration Technology.

Intel Dynamic Acceleration Technology mode enabling requires:

- Exposure, via BIOS, of the opportunistic frequency as the highest ACPI P state
- Enhanced Multi-Threaded Thermal Management (EMTTM)
- Intel Dynamic Acceleration Technology mode and EMTTM MSR configuration via BIOS.

When in Intel Dynamic Acceleration Technology mode, it is possible for both cores to be active under certain internal conditions. In such a scenario the processor may draw an Instantaneous current ($I_{CC\_CORE\_INST}$) for a short duration of t_{INST}; however, the average I_{CC} current will be “lesser then” or “equal” to I_{CCDES} current specification. Please refer to the Processor DC Specifications section for more details.

2.5 VID-x

The processor implements the VID-x feature for improved control of core voltage levels when the processor enters a reduced power consumption state. VID-x applies only when the processor is in the Intel Dynamic Acceleration Technology performance state and one or more cores are in low-power state (i.e., CC3/CC4/CC6). VID-x provides the ability for the processor to request core voltage level reductions greater than one VID tick. The amount of VID tick reduction is fixed and only occurs while the processor is in the Intel Dynamic Acceleration Technology mode. This improved voltage regulator efficiency, during periods of reduced power consumption, allows for leakage reduction that results in platform power savings and extended battery life.

2.6 Processor Power Status Indicator (PSI-2) Signal

The processor incorporates the PSI# signal that is asserted when the processor is in a reduced power consumption state. PSI# can be used to improve intermediate and light load efficiency of the voltage regulator, resulting in platform power savings and extended battery life. The algorithm that the processor uses for determining when to assert PSI# is different from the algorithm used in previous mobile processors. For details, refer to the platform design guide for PSI-2. Functionality is expanded further to support three processor states when:

- Both cores are in idle state.
- Only one core is in active state.
- Both cores are in active state.

3 Electrical Specifications

3.1 Power and Ground Pins

For clean, on-chip power distribution, the processor will have a large number of V_{CC} (power) and V_{SS} (ground) inputs. All power pins must be connected to V_{CC} power planes while all V_{SS} pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. Refer to the platform design guide for more details. The processor V_{CC} pins must be supplied the voltage determined by the VID (Voltage ID) pins.

3.2 FSB Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous-generation processors, the processor core frequency is a multiple of the BCLK[1:0] frequency. The processor uses a differential clocking implementation.

3.3 Voltage Identification

The processor uses seven voltage identification pins,VID[6:0], to support automatic selection of power supply voltages. The VID pins for processor are CMOS outputs driven by the processor VID circuitry. Table 2 specifies the voltage level corresponding to the state of VID[6:0]. A 1 refers to a high-voltage level and a 0 refers to low-voltage level.

Table 2. Voltage Identification Definition (Sheet 1 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875

Table 2. Voltage Identification Definition (Sheet 2 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875

Table 2. Voltage Identification Definition (Sheet 3 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875

Table 2. Voltage Identification Definition (Sheet 4 of 4)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

3.4 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125°C (maximum), or if the THERMTRIP# signal is asserted, the V_{CC} supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP# functionality is not ensured if the PWRGOOD signal is not asserted, and during package C6.

3.5 Reserved and Unused Pins

All RESERVED (RSVD) pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 4.2 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected.

The TEST1,TEST2,TEST3,TEST4,TEST5,TEST6,TEST7 pins are used for test purposes internally and can be left as “No Connects”.

3.6 FSB Frequency Select Signals (BSEL[2:0])

The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). These signals should be connected to the clock chip and the appropriate chipset on the platform. The BSEL encoding for BCLK[1:0] is shown in Table 3.

Table 3. BSEL[2:0] Encoding for BCLK Frequency

BSEL[2]	BSEL[1]	BSEL[0]	BCLK Frequency
L	L	L	RESERVED
L	L	H	RESERVED
L	H	H	166 MHz
L	H	L	200 MHz
H	H	L	RESERVED
H	H	H	RESERVED
H	L	H	RESERVED
H	L	L	RESERVED

3.7 FSB Signal Groups

The FSB signals have been combined into groups by buffer type in the following sections. AGTL+ input signals have differential input buffers that use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving. With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 4 identifies which signals are common clock, source synchronous, and asynchronous.

Table 4. FSB Pin Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, PREQ#[5], RESET#, RS[2:0]#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, BNR#, BPM[3:0]#[3], BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#[3], DPWR#
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr><tr><td>A[35:17]#</td><td>ADSTB[1]#</td></tr><tr><td>D[15:0]#, DINV0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DINV1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DINV2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DINV3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
CMOS Input	Asynchronous	A20M#, DPRSTP#, DPSLP#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#
Open Drain Output	Asynchronous	FERR#, IERR#, THERMTRIP#
Open Drain I/O	Asynchronous	PROCHOT#[4]
CMOS Output	Asynchronous	PSI#, VID[6:0], BSEL[2:0]
CMOS Input	Synchronous to TCK	TCK, TDI, TMS, TRST#
Open Drain Output	Synchronous to TCK	TDO
FSB Clock	Clock	BCLK[1:0]
Power/Other		COMP[3:0], DBR#[2], GTLREF, RSVD, TEST2, TEST1, THERMDA, THERMDC, V_{CC}, V_{CCA}, V_{CCP}, V_{CC_SENSE}, V_{SS}, V_{SS_SENSE}

NOTES:
1. Refer to Chapter 4 for signal descriptions and termination requirements.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no-connects.
3. BPM[2:1]# and PRDY# are AGTL+ output-only signals.
4. PROCHOT# signal type is open drain output and CMOS input.
5. On-die termination differs from other AGTL+ signals.

3.8 CMOS Signals

CMOS input signals are shown in Table 4. Legacy output FERR#, IERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) use Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the CMOS signals are required to be asserted for more than four BCLKs for the processor to recognize them. See Section 3.10 for the DC specifications for the CMOS signal groups.

3.9 Maximum Ratings

Table 5 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Caution: Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 5. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1]
$T_{STORAGE}$	Processor storage temperature	-40	85	°C	2, 3, 4
V_{CC}	Any processor supply voltage with respect to V_{SS}	-0.3	1.45	V	
$V_{inAGTL+}$	AGTL+ buffer DC input voltage with respect to V_{SS}	-0.1	1.45	V	
$V_{inAsynch\_CMOS}$	CMOS buffer DC input voltage with respect to V_{SS}	-0.1	1.45	V	

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be met.
2. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
3. This rating applies to the processor and does not include any tray or packaging.
4. Failure to adhere to this specification can affect the long term reliability of the processor.

3.10 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Table 4 for the pin signal definitions and signal pin assignments.

Table 6 through Table 11 list the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency Mode (HFM) and Lowest Frequency Mode (LFM) refer to the highest and lowest core operating frequencies supported on the processor. Active mode load line specifications apply in all states except in the Deep Sleep and Deeper Sleep states. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the processor are at T_J = 105°C. Read all notes associated with each parameter.

Table 6. Voltage and Current Specifications for the Extreme Edition Processors (Sheet 1 of 2)

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		1.0		1.275	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.85		1.10	V	1, 2
V_{CCSLFM}	V_{CC} at Super Low Frequency Mode (Super LFM)		0.8		1.0	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power-Up		—	1.200	—	V	2, 5, 6, 7
V_{CCP}	AGTL+ Termination Voltage		1.000	1.050	1.100	V	
V_{CCA}	PLL Supply Voltage		1.425	1.500	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep		0.65		0.85	V	1, 2
V_{DC4}	V_{CC} at Intel® Enhanced Deeper Sleep state		0.60		0.85	V	1, 2
V_{C6}	V_{CC} at Deep Power-Down Technology		0.35		0.70	V	1, 2
I_{CCDES}	I_{CC} for Processors Recommended Design Target		—	—	59	A	
I_{CC}	I_{CC} for Processors		—	—	—		
	Processor Number	Core Frequency/Voltage	—	—	—		
	X9000	2.8 GHz & V_{CCHFM} 1.2 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	—	—	57 34 26	A	3, 4, 10, 12
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM SuperLFM		—	—	 27.3 18.3	A	3, 4, 10
I_{SLP}	I_{CC} Sleep HFM SuperLFM		—	—	 26.5 18.1	A	3, 4, 10
I_{DSLP}	I_{CC} Deep Sleep HFM SuperLFM		—	—	 24.5 17.6	A	3, 4, 10
I_{DPRSLP}	I_{CC} Deeper Sleep		—	—	12.2	A	3, 4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep		—	—	11.7	A	3, 4
I_{C6}	I_{CC} Deep Power-Down Technology		—	—	11.0	A	3, 4

Table 6. Voltage and Current Specifications for the Extreme Edition Processors (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin	—	—	600	A/µs	5, 9
I_{CCA}	I_{CC} for V_{CCA} Supply	—	—	130	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} Supply after V_{CC} Stable	—	—	4.5 2.5	A A	8 9

NOTES:

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 105°C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 5 and Figure 6.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification, which is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state I_{CC} current specification, which is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. Processor I_{CC} requirements in Intel Dynamic Acceleration Technology mode is lesser than I_{CC} in HFM
11. The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor will be lesser than or equal to 300 mV.
12. Intel Dynamic Acceleration Technology is **not** supported.

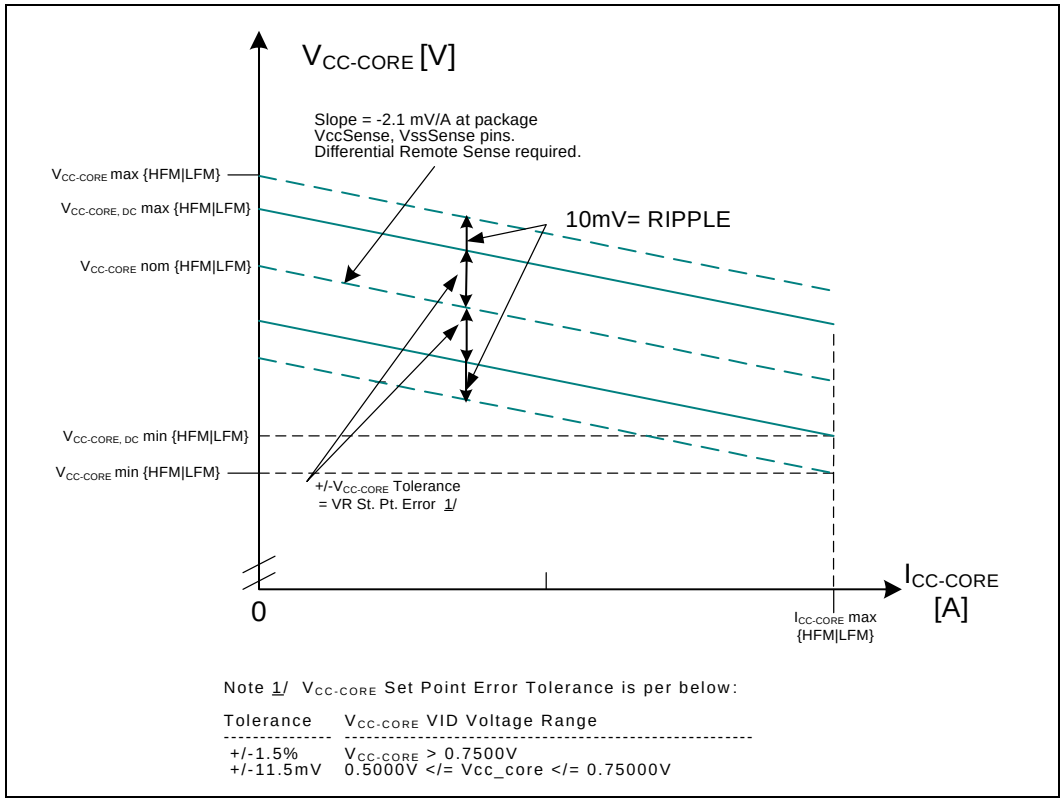
Table 7. Voltage and Current Specifications for the Dual-Core Standard Voltage Processors

Symbol	Parameter		Min	Typ	Max	Unit	Notes
V_{CCDAM}	V_{CC} in Intel Dynamic Acceleration Technology Mode		1.000		1.300	V	1, 2
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)		1.000		1.250	V	1, 2
V_{CCLFM}	V_{CC} at Lowest Frequency Mode (LFM)		0.850	—	1.025	V	1, 2
V_{CCSLFM}	V_{CC} at Super Low Frequency Mode (Super LFM)		0.750	—	0.95	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power-Up		—	1.200	—	V	2, 5, 7
V_{CCP}	AGTL+ Termination Voltage		1.000	1.050	1.100	V	
V_{CCA}	PLL Supply Voltage		1.425	1.500	1.575	V	
$V_{CCDPRSLP}$	V_{CC} at Deeper Sleep		0.650	—	0.850	V	1, 2
V_{DC4}	V_{CC} at Intel® Enhanced Deeper Sleep State		0.600	—	0.850	V	1, 2
V_{C6}	V_{CC} at Deep Power-Down Technology		0.35	—	0.70	V	1, 2
I_{CCDES}	I_{CC} for LV Processors Recommended Design Target		—	—	44	A	13
I_{CC}	I_{CC} for Processors		—	—	—		
	Processor Number	Core Frequency/Voltage	—	—	—		
	T9500 T9300 T8300 T8100	2.6 GHz & V_{CCHFM} 2.5 GHz & V_{CCHFM} 2.4 GHz & V_{CCHFM} 2.1 GHz & V_{CCHFM} 1.2 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	—	—	44 44 44 44 28.6 22.4	A	3, 4, 11
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant HFM SuperLFM		—	—	 23.3 13.7	A	3, 4, 11
I_{SLP}	I_{CC} Sleep HFM SuperLFM		—	—	 22.7 13.5	A	3, 4, 11
I_{DSLP}	I_{CC} Deep Sleep HFM SuperLFM		—	—	 21.0 13.0	A	3, 4, 11
I_{DPRSLP}	I_{CC} Deeper Sleep		—	—	11.7	A	3, 4
I_{DC4}	I_{CC} Intel Enhanced Deeper Sleep		—	—	10.5	A	3, 4
I_{C6}	I_{CC} Deep Power-Down Technology		—	—	5.7	A	3, 4
$dI_{CC/DT}$	V_{CC} Power Supply Current Slew Rate at Processor Package Pin		—	—	600	A/µs	6, 8
I_{CCA}	I_{CC} for V_{CCA} Supply		—	—	130	mA	
I_{CCP}	I_{CC} for V_{CCP} Supply before V_{CC} Stable I_{CC} for V_{CCP} Supply after V_{CC} Stable		—	—	4.5 2.5	A A	9 10

NOTES:(Begin on next page.)

1. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Intel Thermal Monitor 2, Enhanced Intel SpeedStep Technology, or Enhanced Halt State).
2. The voltage specifications are assumed to be measured across V_{CC_SENSE} and V_{SS_SENSE} pins at socket with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 105°C T_J.
4. Specified at the nominal V_{CC}.
5. Measured at the bulk capacitors on the motherboard.
6. $V_{CC,BOOT}$ tolerance shown in Figure 5 and Figure 6.
7. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
8. This is a power-up peak current specification that is applicable when V_{CCP} is high and V_{CC_CORE} is low.
9. This is a steady-state Icc current specification that is applicable when both V_{CCP} and V_{CC_CORE} are high.
10. Processor I_{CC} requirements in Intel Dynamic Acceleration Technology mode is lesser than I_{CC} in HFM
11. The maximum delta between Intel Enhanced Deeper Sleep and LFM on the processor will be lesser than or equal to 300 mV.
12. Instantaneous current $I_{CC\_CORE\_INST}$ of 55 A has to be sustained for short time (t_{INST}) of 10 µs. Average current will be less than maximum specified I_{CCDES}. VR OCP threshold should be high enough to support current levels described herein.

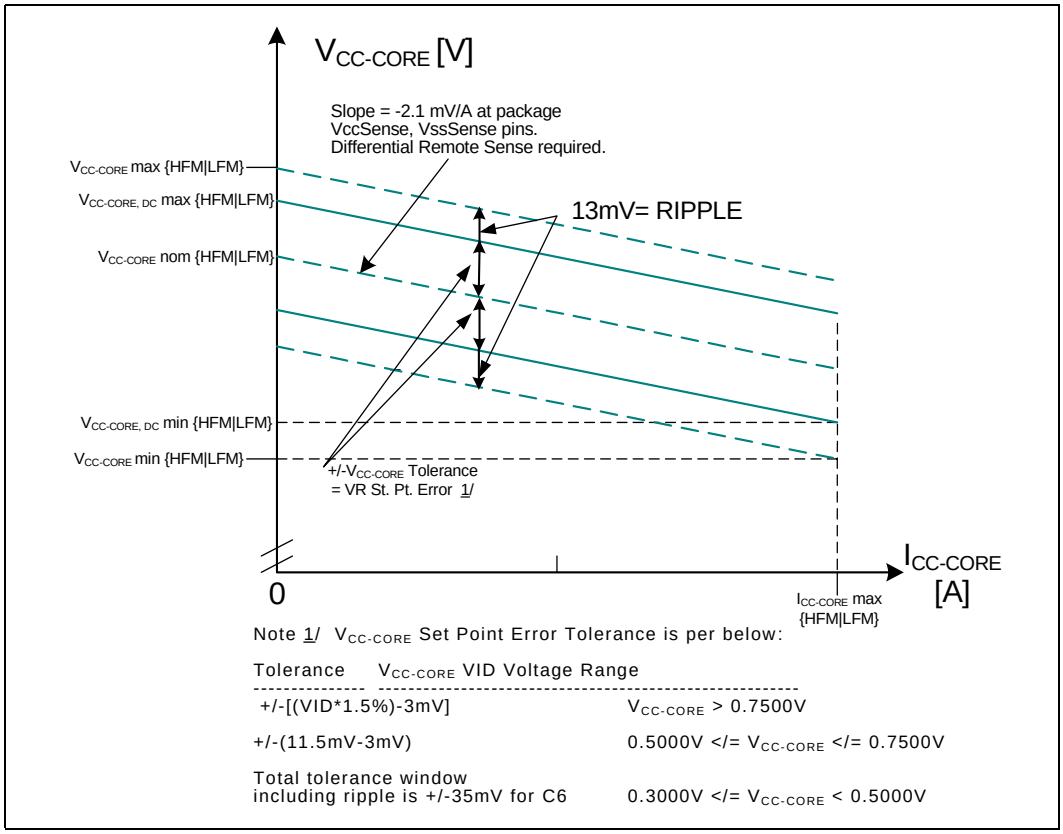
Figure 5. Active V_{CC} and I_{CC} Loadline Standard Voltage and Extreme Edition Processors



Note 1/ $V_{CC\text{-}CORE}$ Set Point Error Tolerance is per below:

Tolerance	$V_{CC\text{-}CORE}$ VID Voltage Range
+/-1.5%	$V_{CC\text{-}CORE}$ > 0.7500V
+/-11.5mV	0.5000V </= Vcc_core </= 0.75000V

Figure 6. Deeper Sleep V_{CC} and I_{CC} Loadline Standard Voltage and Extreme Edition Processors



NOTE: Deeper Sleep mode tolerance depends on VID value.

Table 8. FSB Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CROSS}	Crossing Voltage	0.3	—	0.55	V	2, 7, 8
ΔV_{CROSS}	Range of Crossing Points	—	—	140	mV	2, 7, 5
V_{SWING}	Differential Output Swing	300	—	—	mV	6
I_{LI}	Input Leakage Current	-5	—	+5	µA	3
Cpad	Pad Capacitance	0.95	1.2	1.45	pF	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. For V_{in} between 0 V and V_{IH}.
4. Cpad includes die capacitance only. No package parasitics are included.
5. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 2.
6. Measurement taken from differential waveform.
7. Measurement taken from single-ended waveform.
8. Only applies to the differential rising edge (Clock rising and Clock# falling).

Table 9. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	
GTLREF	Reference Voltage	0.65	0.70	0.72	V	6
R_{COMP}	Compensation Resistor	27.23	27.5	27.78	Ω	10
$R_{ODT/A}$	Termination Resistor Address	48	55	65	Ω	11, 12
$R_{ODT/D}$	Termination Resistor Data	48	55	64	Ω	11, 13
$R_{ODT/Cntrl}$	Termination Resistor Control	48	55	65	Ω	11, 14
V_{IH}	Input High Voltage	0.82	1.05	1.20	V	3, 6
V_{IL}	Input Low Voltage	-0.10	0	0.55	V	2, 4
V_{OH}	Output High Voltage	0.90	V_{CCP}	1.10	V	6
$R_{TT/A}$	Termination Resistance Address	48	55	65	Ω	7, 12
$R_{TT/D}$	Termination Resistance Data	48	55	64	Ω	7, 13
$R_{TT/Cntrl}$	Termination Resistance Control	48	55	65	Ω	7, 14
$R_{ON/A}$	Buffer On Resistance Address	22	25	30	Ω	5, 12
$R_{ON/D}$	Buffer On Resistance Data	22	25	29.5	Ω	5, 13
$R_{ON/Cntrl}$	Buffer On Resistance Control	22	25	30	Ω	5, 14
I_{LI}	Input Leakage Current	—	—	±100	µA	8
Cpad	Pad Capacitance	1.80	2.30	2.75	pF	9

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull-down driver resistance. Refer to processor I/O Buffer Models for I/V characteristics. Measured at 0.31*V_{CCP}. R_{ON} (min) = 0.4*R_{TT}, R_{ON} (typ) = 0.455*R_{TT}, R_{ON} (max) = 0.51*R_{TT}. R_{TT} typical value of 55 Ω is used for R_{ON} typ/min/max calculations.
6. GTLREF should be generated from V_{CCP} with a 1% tolerance resistor divider. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP}.
7. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Measured at 0.31*V_{CCP}. R_{TT} is connected to V_{CCP} on die. Refer to processor I/O buffer models for I/V characteristics.
8. Specified with on die R_{TT} and R_{ON} are turned off. V_{in} between 0 and V_{CCP}.
9. Cpad includes die capacitance only. No package parasitics are included.
10. This is the external resistor on the comp pins.
11. On-die termination resistance, measured at 0.33*V_{CCP}.
12. Applies to Signals A[35:3].
13. Applies to Signals D[63:0].
14. Applies to Signals BPRI#,DEFER#,PREQ#, RESET#, RS[2:0]#, TRDY#, ADS#, BNR#, BPM[3:0], BR0#, DBSY#, DRDY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#, DPWR#, ADSTB[1:0]#, DSTBP[3:0] and DSTBN[3:0]#.

Table 10. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	1.00	1.05	1.10	V	
V_{IH}	Input High Voltage	0.7 * V_{CCP}	V_{CCP}	V_{CCP}+0.1	V	2
V_{IL}	Input Low Voltage CMOS	-0.10	0.00	0.3 * V_{CCP}	V	2, 3
V_{OH}	Output High Voltage	0.9 * V_{CCP}	V_{CCP}	V_{CCP}+0.1	V	2
V_{OL}	Output Low Voltage	-0.10	0	0.1 * V_{CCP}	V	2
I_{OH}	Output High Current	1.5	—	4.1	mA	5
I_{OL}	Output Low Current	1.5	—	4.1	mA	4
I_{LI}	Input Leakage Current	—	—	±100	µA	6
Cpad1	Pad Capacitance	1.80	2.30	2.75	pF	7
Cpad2	Pad Capacitance for CMOS Input	0.95	1.2	1.45	pF	8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCP} referred to in these specifications refers to instantaneous V_{CCP}.
3. Refer to the processor I/O Buffer Models for I/V characteristics.
4. Measured at 0.1*V_{CCP}.
5. Measured at 0.9*V_{CCP}.
6. For V_{in} between 0 V and V_{CCP}. Measured when the driver is tristated.z
7. Cpad1 includes die capacitance only for DPRSTP#, DPSLP#, PWRGOOD. No package parasitics are included.
8. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.

Table 11. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{OH}	Output High Voltage	V_{CCP} – 5%	V_{CCP}	V_{CCP} + 5%	V	3
V_{OL}	Output Low Voltage	0	—	0.20	V	
I_{OL}	Output Low Current	16	—	50	mA	2
I_{LO}	Output Leakage Current	—	—	±200	µA	4
Cpad	Pad Capacitance	1.80	2.30	2.75	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2 V.
3. V_{OH} is determined by value of the external pull-up resistor to V_{CCP}. Refer to the appropriate platform design guide for details.
4. For V_{in} between 0 V and V_{OH}.
5. Cpad includes die capacitance only. No package parasitics are included.

§

4 Package Mechanical Specifications and Pin Information

4.1 Package Mechanical Specifications

The processor is available in 6-MB and 3-MB, 478-pin Micro-FCPGA packages as well as 6-MB and 3-MB, 479-ball Micro-FCBGA packages. The package mechanical dimensions are shown in Figure 7 through Figure 10.

The mechanical package pressure specifications are in a direction normal to the surface of the processor. This requirement is to protect the processor die from fracture risk due to uneven die pressure distribution under tilt, stack-up tolerances and other similar conditions. These specifications assume that a mechanical attach is designed specifically to load one type of processor.

Intel also specifies that 15-lbf load limit should not be exceeded on any of Intel's BGA packages so as to not impact solder joint reliability after reflow. This load limit ensures that impact to the package solder joints due to transient bend, shock, or tensile loading is minimized. The 15-lbf metric should be used **in parallel** with the 689 kPa (100 psi) pressure limit as long as neither limits are exceeded. In some cases, designing to 15-lbf will exceed the pressure specification of 689 kPa (100 psi) and therefore should be reduced to ensure both limits are maintained.

Moreover, the processor package substrate should not be used as a mechanical reference or load-bearing surface for the thermal or mechanical solution. Refer to the *Santa Rosa Platform Mechanical Design Guide* for details.

Caution: The Micro-FCBGA package incorporates land-side capacitors. The land-side capacitors are electrically conductive so care should be taken to avoid contacting the capacitors with other electrically conductive materials on the motherboard. Doing so may short the capacitors and possibly damage the device or render it inactive.

Figure 7. 6-MB and 3-MB on 6-MB Die Micro-FCPGA Processor Package Drawing (Sheet 1 of 2)

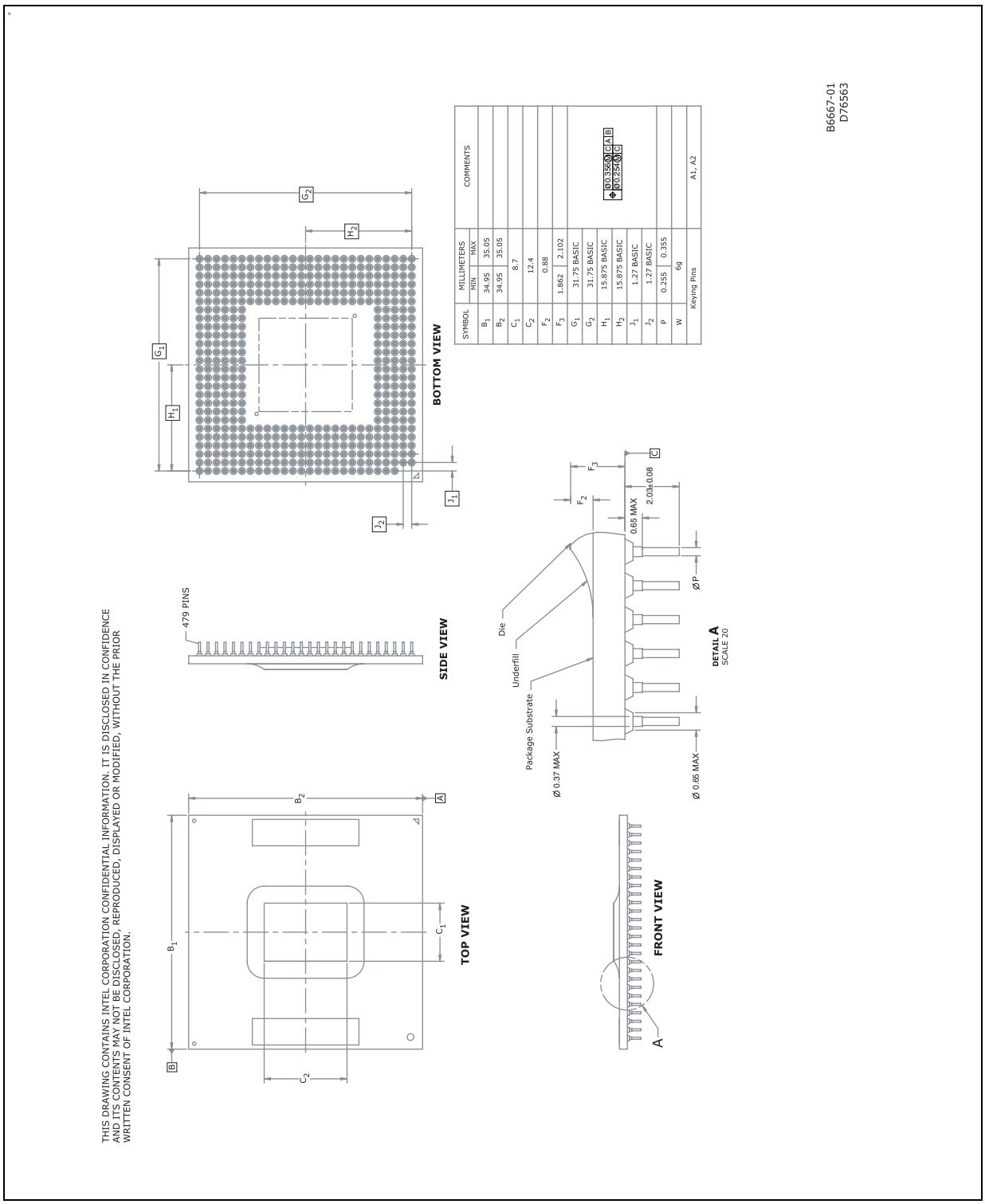


Figure 8. 6-MB and 3-MB on 6-MB Die Micro-FCPGA Processor Package Drawing (Sheet 2 of 2)

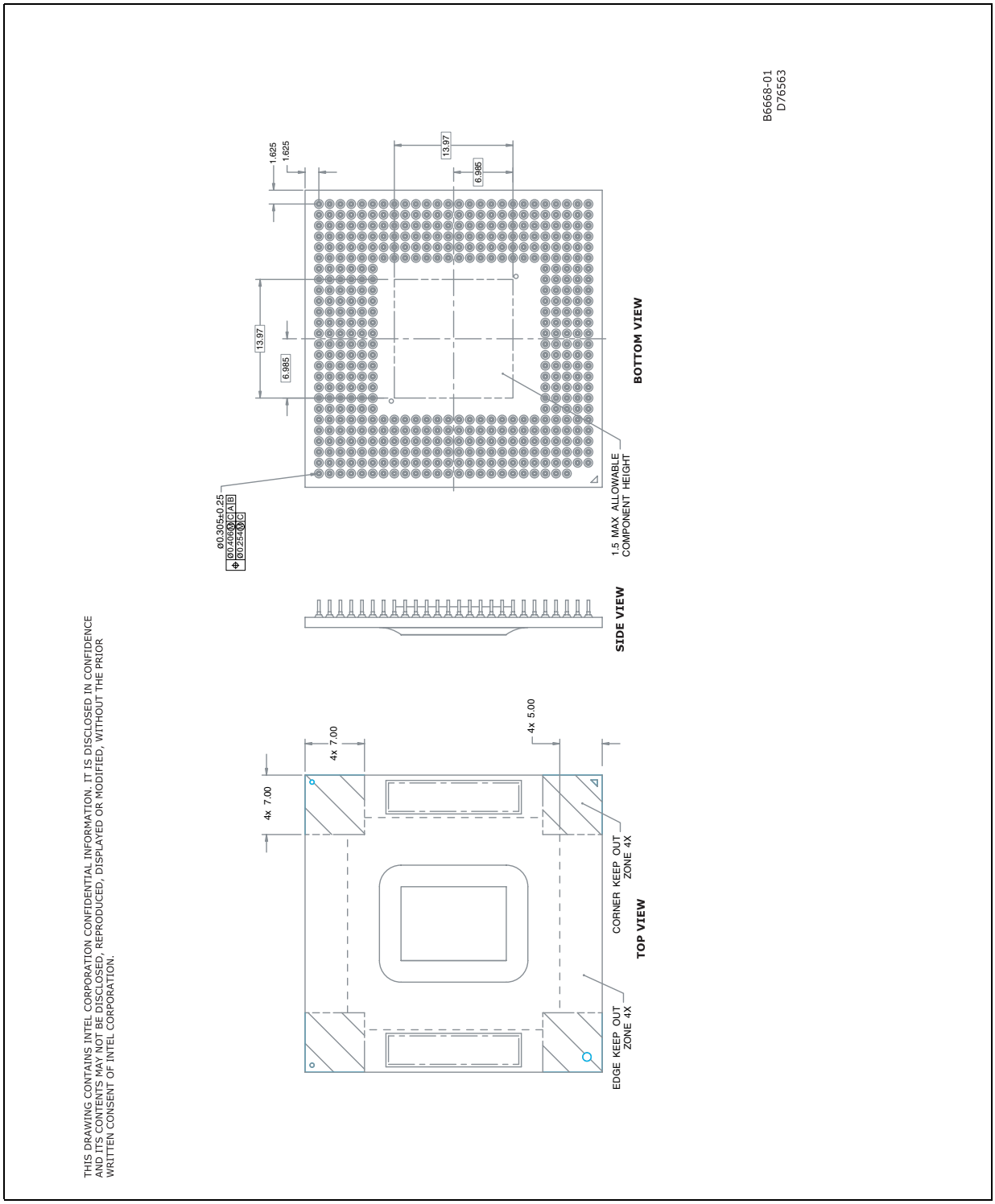


Figure 9. 6-MB and 3-MB on 6-MB Die Micro-FCBGA Processor Package Drawing (Sheet 1 of 2)

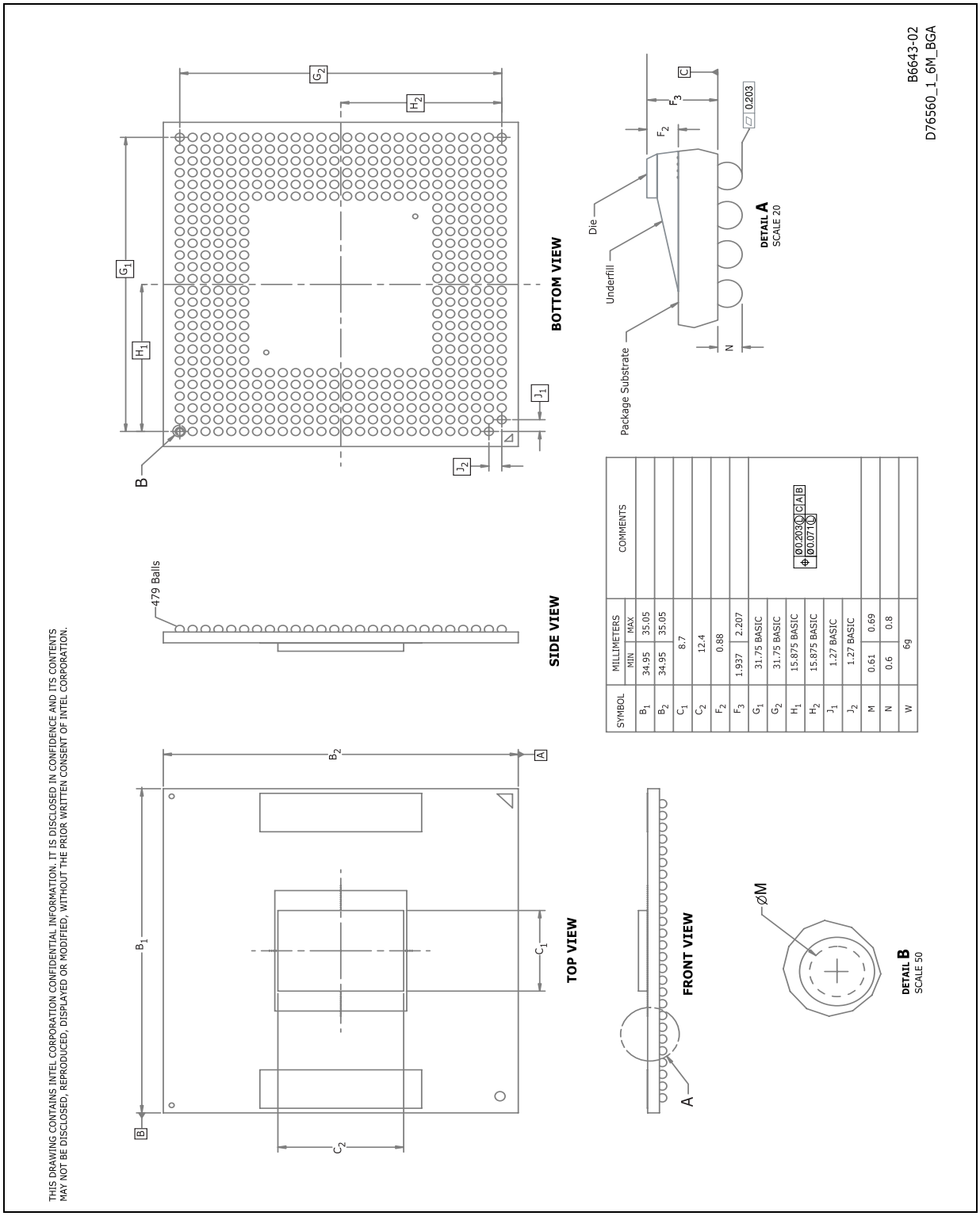


Figure 10. 6-MB and 3-MB on 6-MB die Micro-FCBGA Processor Package Drawing (Sheet 2 of 2)

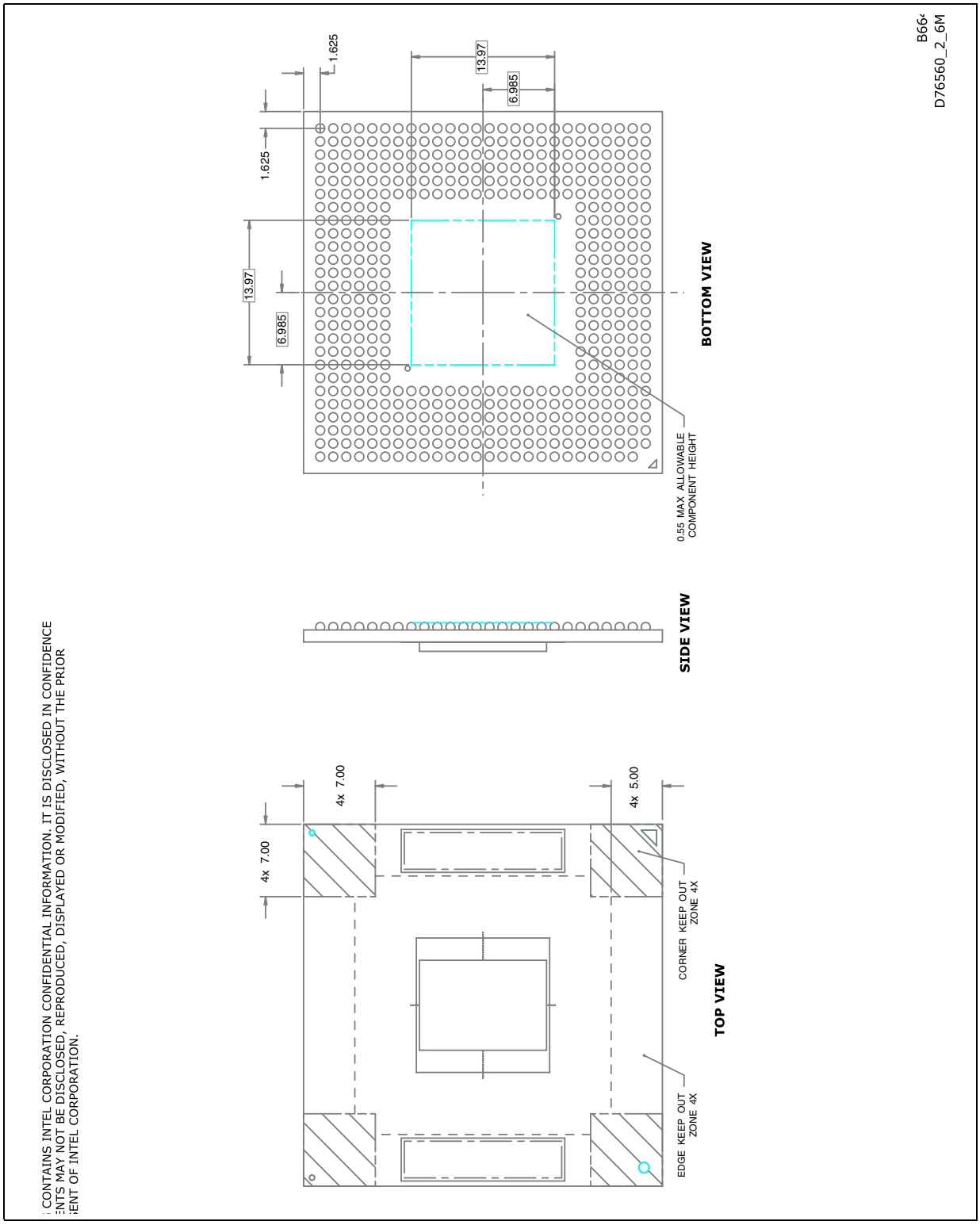


Figure 11. 3-MB Micro-FCPGA Processor Package Drawing (Sheet 1 of 2)

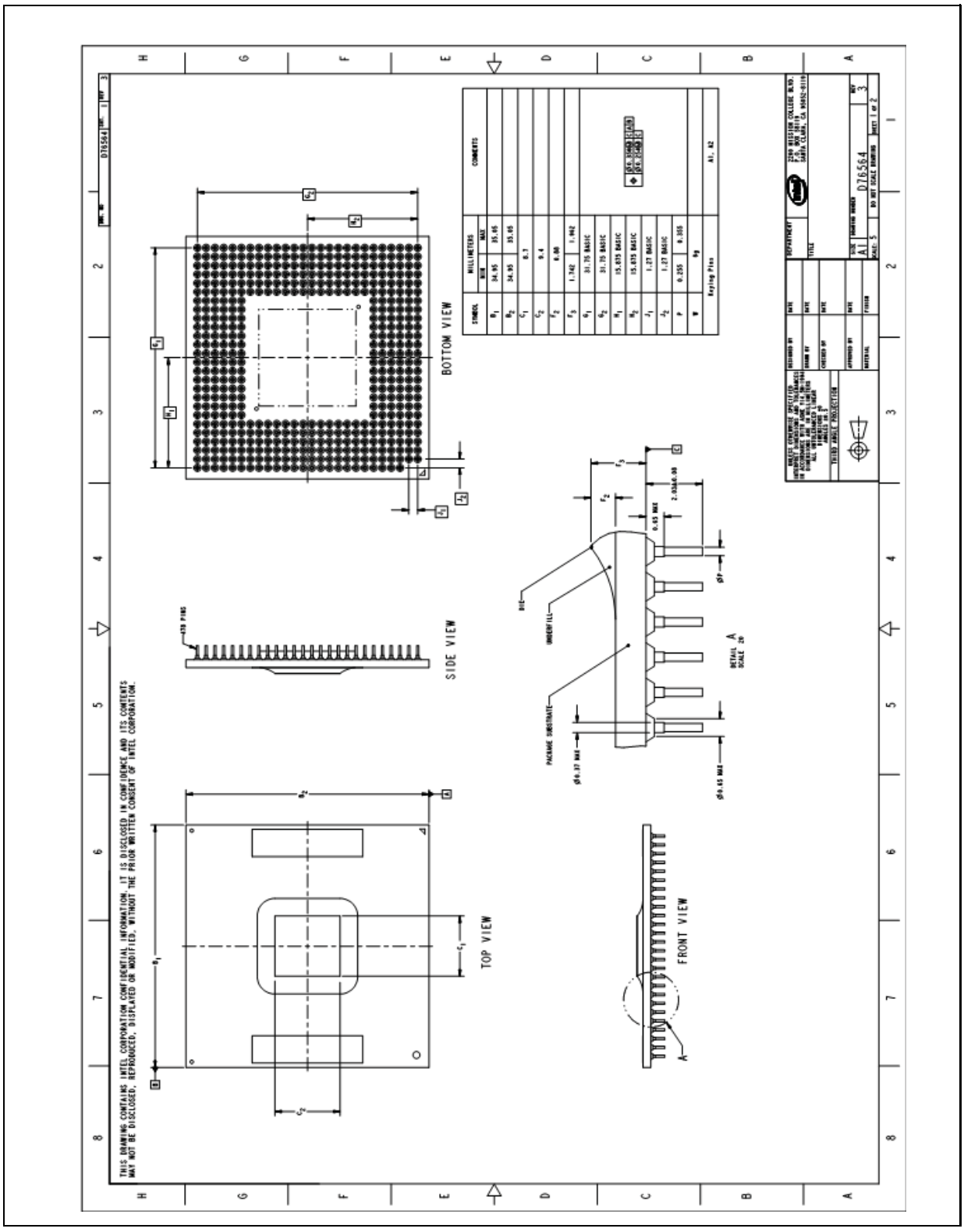


Figure 12. 3-MB Micro-FCPGA Processor Package Drawing (Sheet 2 of 2)

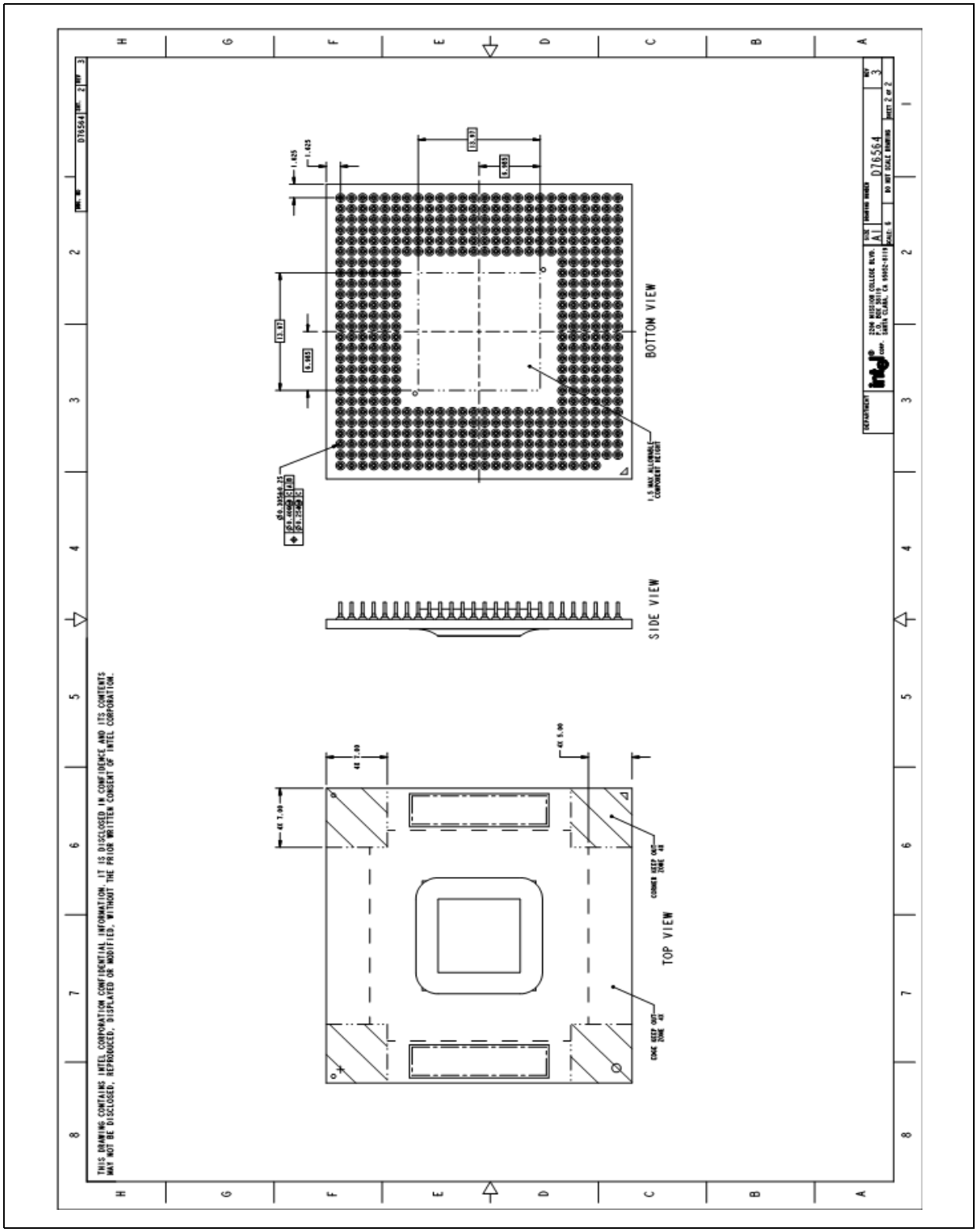


Figure 13. 3-MB Micro-FCBGA Processor Package Drawing (Sheet 1 of 2)

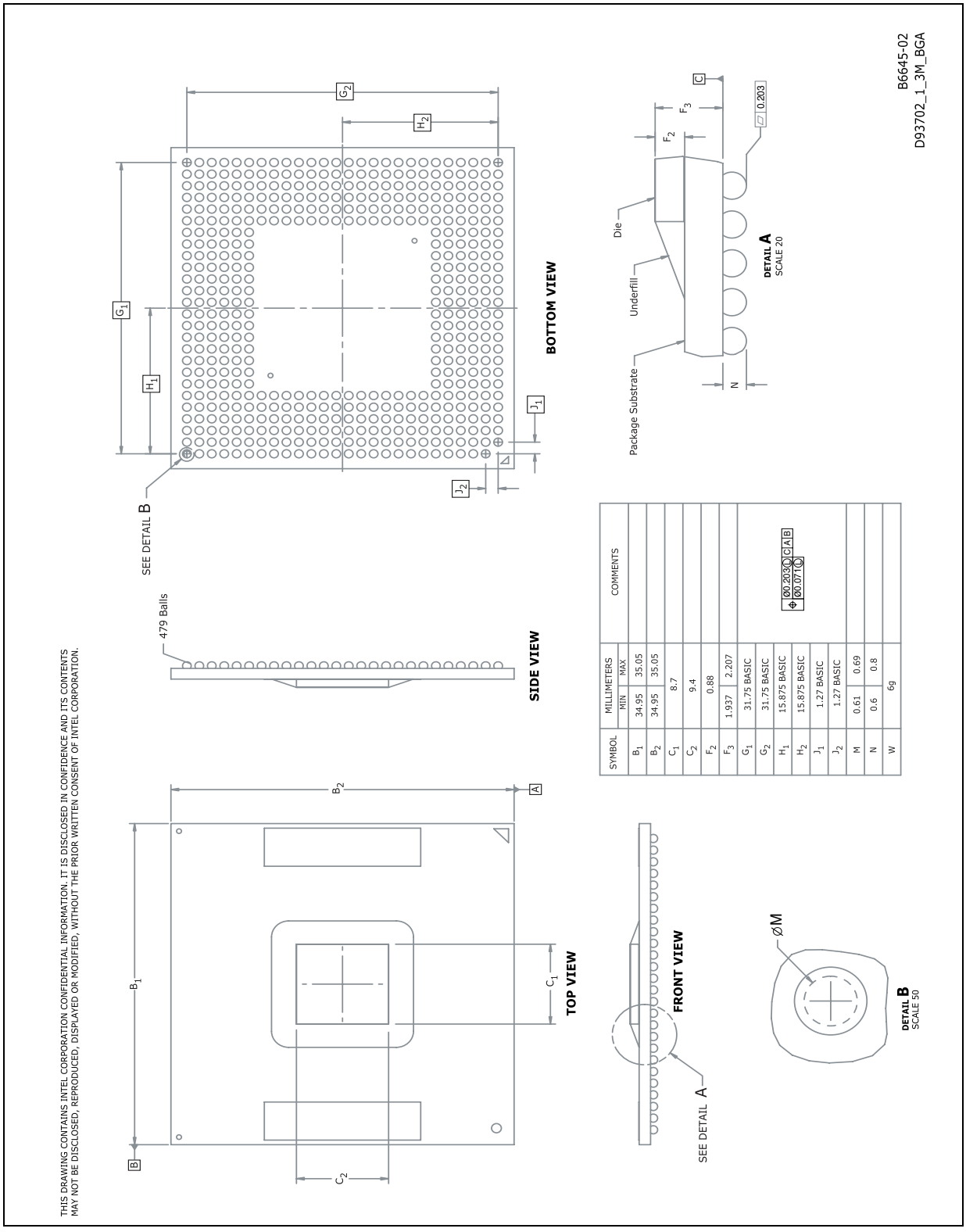
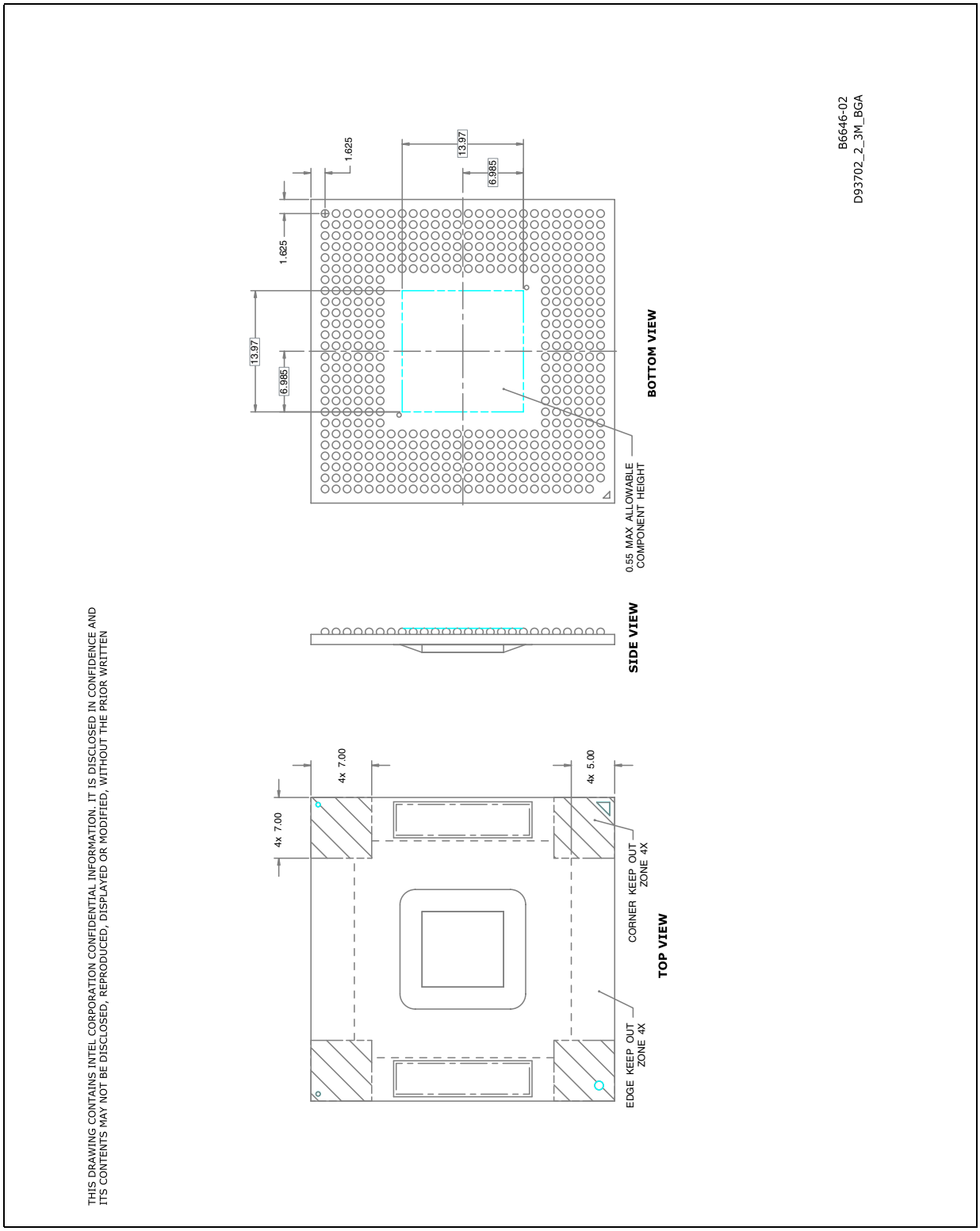


Figure 14. 3-MB Micro-FCBGA Processor Package Drawing (Sheet 2 of 2)



4.2 Processor Pinout and Pin List

Figure 15 and Figure 16 show the processor pinout as viewed from the top of the package. Table 12 provides the pin list, arranged numerically by pin number.

Figure 15. Processor Pinout (Top Package View, Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A[1]		VSS	SMI#	VSS	FERR#	A20M#	VCC	VSS	VCC	VCC	VSS	VCC	VCC	A
B[1]		RSVD	INIT#	LINT1	DPSLP#	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	B
C	RESET#	VSS	TEST7	IGNNE#	VSS	LINT0	THERM TRIP#	VSS	VCC	VCC	VSS	VCC	VCC	C
D	VSS	RSVD	RSVD	VSS	STPCLK#	PWRGO OD	SLP#	VSS	VCC	VCC	VSS	VCC	VSS	D
E	DBSY#	BNR#	VSS	HITM#	DPRSTP#	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VCC	E
F	BR0#	VSS	RS[0]#	RS[1]#	VSS	RSVD	VCC	VSS	VCC	VCC	VSS	VCC	VSS	F
G	VSS	TRDY#	RS[2]#	VSS	BPRI#	HIT#								G
H	ADS#	REQ[1]#	VSS	LOCK#	DEFER#	VSS								H
J	A[9]#	VSS	REQ[3]#	A[3]#	VSS	VCCP								J
K	VSS	REQ[2]#	REQ[0]#	VSS	A[6]#	VCCP								K
L	REQ[4]#	A[13]#	VSS	A[5]#	A[4]#	VSS								L
M	ADSTB[0]#	VSS	A[7]#	RSVD	VSS	VCCP								M
N	VSS	A[8]#	A[10]#	VSS	RSVD	VCCP								N
P	A[15]#	A[12]#	VSS	A[14]#	A[11]#	VSS								P
R	A[16]#	VSS	A[19]#	A[24]#	VSS	VCCP								R
T	VSS	RSVD	A[26]#	VSS	A[25]#	VCCP								T
U	A[23]#	A[30]#	VSS	A[21]#	A[18]#	VSS								U
V	ADSTB[1]#	VSS	RSVD	A[31]#	VSS	VCCP								V
W	VSS	A[27]#	A[32]#	VSS	A[28]#	A[20]#								W
Y	COMP[3]	A[17]#	VSS	A[29]#	A[22]#	VSS								Y
AA	COMP[2]	VSS	A[35]#	A[33]#	VSS	TDI	VCC	VSS	VCC	VCC	VSS	VCC	VCC	AA
AB	VSS	A[34]#	TDO	VSS	TMS	TRST#	VCC	VSS	VCC	VCC	VSS	VCC	VSS	AB
AC	PREQ#	PRDY#	VSS	BPM[3]#	TCK	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VCC	AC
AD	BPM[2]#	VSS	BPM[1]#	BPM[0]#	VSS	VID[0]	VCC	VSS	VCC	VCC	VSS	VCC	VSS	AD
AE	VSS	VID[6]	VID[4]	VSS	VID[2]	PSI#	VSS SENSE	VSS	VCC	VCC	VSS	VCC	VCC	AE
AF	TEST5	VSS	VID[5]	VID[3]	VID[1]	VSS	VCC SENSE	VSS	VCC	VCC	VSS	VCC	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	

NOTES:
1. Keying option for µFCPGA, A1 and B1 are depopulated.
2. Keying option for µFCBGA, A1 is depopulated and B1 is VSS.

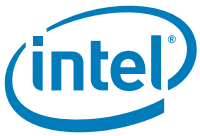


Figure 16. Processor Pinout (Top Package View, Right Side)

	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	VCC	VSS	VCC	VCC	VSS	VCC	BCLK[1]	BCLK[0]	VSS	THRMDA	VSS	TEST6	A
B	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	BSEL[0]	BSEL[1]	VSS	THRMDC	VCCA	B
C	VSS	VCC	VSS	VCC	VCC	VSS	DBR#	BSEL[2]	VSS	TEST1	TEST3	VSS	VCCA	C
D	VCC	VCC	VSS	VCC	VCC	VSS	IERR#	PROCHOT#	RSVD	VSS	DPWR#	TEST2	VSS	D
E	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	D[0]#	D[7]#	VSS	D[6]#	D[2]#	E
F	VCC	VCC	VSS	VCC	VCC	VSS	VCC	DRDY#	VSS	D[4]#	D[1]#	VSS	D[13]#	F
G								VCCP	D[3]#	VSS	D[9]#	D[5]#	VSS	G
H								VSS	D[12]#	D[15]#	VSS	DINV[0]#	DSTBP[0]#	H
J								VCCP	VSS	D[11]#	D[10]#	VSS	DSTBN[0]#	J
K								VCCP	D[14]#	VSS	D[8]#	D[17]#	VSS	K
L								VSS	D[22]#	D[20]#	VSS	D[29]#	DSTBN[1]#	L
M								VCCP	VSS	D[23]#	D[21]#	VSS	DSTBP[1]#	M
N								VCCP	D[16]#	VSS	DINV[1]#	D[31]#	VSS	N
P								VSS	D[26]#	D[25]#	VSS	D[24]#	D[18]#	P
R								VCCP	VSS	D[19]#	D[28]#	VSS	COMP[0]	R
T								VCCP	D[37]#	VSS	D[27]#	D[30]#	VSS	T
U								VSS	DINV[2]#	D[39]#	VSS	D[38]#	COMP[1]	U
V								VCCP	VSS	D[36]#	D[34]#	VSS	D[35]#	V
W								VCCP	D[41]#	VSS	D[43]#	D[44]#	VSS	W
Y								VSS	D[32]#	D[42]#	VSS	D[40]#	DSTBN[2]#	Y
AA	VSS	VCC	VSS	VCC	VCC	VSS	VCC	D[50]#	VSS	D[45]#	D[46]#	VSS	DSTBP[2]#	AA
AB	VCC	VCC	VSS	VCC	VCC	VSS	VCC	D[52]#	D[51]#	VSS	D[33]#	D[47]#	VSS	AB
AC	VSS	VCC	VSS	VCC	VCC	VSS	DINV[3]#	VSS	D[60]#	D[63]#	VSS	D[57]#	D[53]#	AC
AD	VCC	VCC	VSS	VCC	VCC	VSS	D[54]#	D[59]#	VSS	D[61]#	D[49]#	VSS	GTLREF	AD
AE	VSS	VCC	VSS	VCC	VCC	VSS	VCC	D[58]#	D[55]#	VSS	D[48]#	DSTBN[3]#	VSS	AE
AF	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	D[62]#	D[56]#	DSTBP[3]#	VSS	TEST4	AF
	14	15	16	17	18	19	20	21	22	23	24	25	26	

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
A[3]#	J4	Source Synch	Input/ Output
A[4]#	L5	Source Synch	Input/ Output
A[5]#	L4	Source Synch	Input/ Output
A[6]#	K5	Source Synch	Input/ Output
A[7]#	M3	Source Synch	Input/ Output
A[8]#	N2	Source Synch	Input/ Output
A[9]#	J1	Source Synch	Input/ Output
A[10]#	N3	Source Synch	Input/ Output
A[11]#	P5	Source Synch	Input/ Output
A[12]#	P2	Source Synch	Input/ Output
A[13]#	L2	Source Synch	Input/ Output
A[14]#	P4	Source Synch	Input/ Output
A[15]#	P1	Source Synch	Input/ Output
A[16]#	R1	Source Synch	Input/ Output
A[17]#	Y2	Source Synch	Input/ Output
A[18]#	U5	Source Synch	Input/ Output
A[19]#	R3	Source Synch	Input/ Output
A[20]#	W6	Source Synch	Input/ Output
A[21]#	U4	Source Synch	Input/ Output
A[22]#	Y5	Source Synch	Input/ Output
A[23]#	U1	Source Synch	Input/ Output
A[24]#	R4	Source Synch	Input/ Output
A[25]#	T5	Source Synch	Input/ Output
A[26]#	T3	Source Synch	Input/ Output

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
A[27]#	W2	Source Synch	Input/ Output
A[28]#	W5	Source Synch	Input/ Output
A[29]#	Y4	Source Synch	Input/ Output
A[30]#	U2	Source Synch	Input/ Output
A[31]#	V4	Source Synch	Input/ Output
A[32]#	W3	Source Synch	Input/ Output
A[33]#	AA4	Source Synch	Input/ Output
A[34]#	AB2	Source Synch	Input/ Output
A[35]#	AA3	Source Synch	Input/ Output
A20M#	A6	CMOS	Input
ADS#	H1	Common Clock	Input/ Output
ADSTB[0]#	M1	Source Synch	Input/ Output
ADSTB[1]#	V1	Source Synch	Input/ Output
BCLK[0]	A22	Bus Clock	Input
BCLK[1]	A21	Bus Clock	Input
BNR#	E2	Common Clock	Input/ Output
BPM[0]#	AD4	Common Clock	Input/ Output
BPM[1]#	AD3	Common Clock	Output
BPM[2]#	AD1	Common Clock	Output
BPM[3]#	AC4	Common Clock	Input/ Output
BPRI#	G5	Common Clock	Input
BR0#	F1	Common Clock	Input/ Output
BSEL[0]	B22	CMOS	Output
BSEL[1]	B23	CMOS	Output
BSEL[2]	C21	CMOS	Output
COMP[0]	R26	Power/Other	Input/ Output
COMP[1]	U26	Power/Other	Input/ Output
COMP[2]	AA1	Power/Other	Input/ Output

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
COMP[3]	Y1	Power/Other	Input/ Output
D[0]#	E22	Source Synch	Input/ Output
D[1]#	F24	Source Synch	Input/ Output
D[2]#	E26	Source Synch	Input/ Output
D[3]#	G22	Source Synch	Input/ Output
D[4]#	F23	Source Synch	Input/ Output
D[5]#	G25	Source Synch	Input/ Output
D[6]#	E25	Source Synch	Input/ Output
D[7]#	E23	Source Synch	Input/ Output
D[8]#	K24	Source Synch	Input/ Output
D[9]#	G24	Source Synch	Input/ Output
D[10]#	J24	Source Synch	Input/ Output
D[11]#	J23	Source Synch	Input/ Output
D[12]#	H22	Source Synch	Input/ Output
D[13]#	F26	Source Synch	Input/ Output
D[14]#	K22	Source Synch	Input/ Output
D[15]#	H23	Source Synch	Input/ Output
D[16]#	N22	Source Synch	Input/ Output
D[17]#	K25	Source Synch	Input/ Output
D[18]#	P26	Source Synch	Input/ Output
D[19]#	R23	Source Synch	Input/ Output
D[20]#	L23	Source Synch	Input/ Output
D[21]#	M24	Source Synch	Input/ Output
D[22]#	L22	Source Synch	Input/ Output
D[23]#	M23	Source Synch	Input/ Output

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
D[24]#	P25	Source Synch	Input/ Output
D[25]#	P23	Source Synch	Input/ Output
D[26]#	P22	Source Synch	Input/ Output
D[27]#	T24	Source Synch	Input/ Output
D[28]#	R24	Source Synch	Input/ Output
D[29]#	L25	Source Synch	Input/ Output
D[30]#	T25	Source Synch	Input/ Output
D[31]#	N25	Source Synch	Input/ Output
D[32]#	Y22	Source Synch	Input/ Output
D[33]#	AB24	Source Synch	Input/ Output
D[34]#	V24	Source Synch	Input/ Output
D[35]#	V26	Source Synch	Input/ Output
D[36]#	V23	Source Synch	Input/ Output
D[37]#	T22	Source Synch	Input/ Output
D[38]#	U25	Source Synch	Input/ Output
D[39]#	U23	Source Synch	Input/ Output
D[40]#	Y25	Source Synch	Input/ Output
D[41]#	W22	Source Synch	Input/ Output
D[42]#	Y23	Source Synch	Input/ Output
D[43]#	W24	Source Synch	Input/ Output
D[44]#	W25	Source Synch	Input/ Output
D[45]#	AA23	Source Synch	Input/ Output
D[46]#	AA24	Source Synch	Input/ Output
D[47]#	AB25	Source Synch	Input/ Output
D[48]#	AE24	Source Synch	Input/ Output

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
D[49]#	AD24	Source Synch	Input/ Output
D[50]#	AA21	Source Synch	Input/ Output
D[51]#	AB22	Source Synch	Input/ Output
D[52]#	AB21	Source Synch	Input/ Output
D[53]#	AC26	Source Synch	Input/ Output
D[54]#	AD20	Source Synch	Input/ Output
D[55]#	AE22	Source Synch	Input/ Output
D[56]#	AF23	Source Synch	Input/ Output
D[57]#	AC25	Source Synch	Input/ Output
D[58]#	AE21	Source Synch	Input/ Output
D[59]#	AD21	Source Synch	Input/ Output
D[60]#	AC22	Source Synch	Input/ Output
D[61]#	AD23	Source Synch	Input/ Output
D[62]#	AF22	Source Synch	Input/ Output
D[63]#	AC23	Source Synch	Input/ Output
DBR#	C20	CMOS	Output
DBSY#	E1	Common Clock	Input/ Output
DEFER#	H5	Common Clock	Input
DINV[0]#	H25	Source Synch	Input/ Output
DINV[1]#	N24	Source Synch	Input/ Output
DINV[2]#	U22	Source Synch	Input/ Output
DINV[3]#	AC20	Source Synch	Input/ Output
DPRSTP#	E5	CMOS	Input
DPSLP#	B5	CMOS	Input
DPWR#	D24	Common Clock	Input/ Output
DRDY#	F21	Common Clock	Input/ Output
DSTBN[0]#	J26	Source Synch	Input/ Output

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
DSTBN[1]#	L26	Source Synch	Input/ Output
DSTBN[2]#	Y26	Source Synch	Input/ Output
DSTBN[3]#	AE25	Source Synch	Input/ Output
DSTBP[0]#	H26	Source Synch	Input/ Output
DSTBP[1]#	M26	Source Synch	Input/ Output
DSTBP[2]#	AA26	Source Synch	Input/ Output
DSTBP[3]#	AF24	Source Synch	Input/ Output
FERR#	A5	Open Drain	Output
GTLREF	AD26	Power/Other	Input
HIT#	G6	Common Clock	Input/ Output
HITM#	E4	Common Clock	Input/ Output
IERR#	D20	Open Drain	Output
IGNNE#	C4	CMOS	Input
INIT#	B3	CMOS	Input
LINT0	C6	CMOS	Input
LINT1	B4	CMOS	Input
LOCK#	H4	Common Clock	Input/ Output
PRDY#	AC2	Common Clock	Output
PREQ#	AC1	Common Clock	Input
PROCHOT#	D21	Open Drain	Input/ Output
PSI#	AE6	CMOS	Output
PWRGOOD	D6	CMOS	Input
REQ[0]#	K3	Source Synch	Input/ Output
REQ[1]#	H2	Source Synch	Input/ Output
REQ[2]#	K2	Source Synch	Input/ Output
REQ[3]#	J3	Source Synch	Input/ Output
REQ[4]#	L1	Source Synch	Input/ Output
RESET#	C1	Common Clock	Input
RS[0]#	F3	Common Clock	Input
RS[1]#	F4	Common Clock	Input
RS[2]#	G3	Common Clock	Input

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
RSVD	B2	Reserved	
RSVD	D2	Reserved	
RSVD	D3	Reserved	
RSVD	D22	Reserved	
RSVD	F6	Reserved	
RSVD	M4	Reserved	
RSVD	N5	Reserved	
RSVD	T2	Reserved	
RSVD	V3	Reserved	
SLP#	D7	CMOS	Input
SMI#	A3	CMOS	Input
STPCLK#	D5	CMOS	Input
TCK	AC5	CMOS	Input
TDI	AA6	CMOS	Input
TDO	AB3	Open Drain	Output
TEST1	C23	Test	
TEST2	D25	Test	
TEST3	C24	Test	
TEST4	AF26	Test	
TEST5	AF1	Test	
TEST6	A26	Test	
TEST7	C3	Test	
THERMTRIP#	C7	Open Drain	Output
THRMDA	A24	Power/Other	
THRMDC	B25	Power/Other	
TMS	AB5	CMOS	Input
TRDY#	G2	Common Clock	Input
TRST#	AB6	CMOS	Input
VCC	A7	Power/Other	
VCC	A9	Power/Other	
VCC	A10	Power/Other	
VCC	A12	Power/Other	
VCC	A13	Power/Other	
VCC	A15	Power/Other	
VCC	A17	Power/Other	
VCC	A18	Power/Other	
VCC	A20	Power/Other	
VCC	AA7	Power/Other	
VCC	AA9	Power/Other	
VCC	AA10	Power/Other	

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	AA12	Power/Other	
VCC	AA13	Power/Other	
VCC	AA15	Power/Other	
VCC	AA17	Power/Other	
VCC	AA18	Power/Other	
VCC	AA20	Power/Other	
VCC	AB7	Power/Other	
VCC	AB9	Power/Other	
VCC	AB10	Power/Other	
VCC	AB12	Power/Other	
VCC	AB14	Power/Other	
VCC	AB15	Power/Other	
VCC	AB17	Power/Other	
VCC	AB18	Power/Other	
VCC	AB20	Power/Other	
VCC	AC7	Power/Other	
VCC	AC9	Power/Other	
VCC	AC10	Power/Other	
VCC	AC12	Power/Other	
VCC	AC13	Power/Other	
VCC	AC15	Power/Other	
VCC	AC17	Power/Other	
VCC	AC18	Power/Other	
VCC	AD7	Power/Other	
VCC	AD9	Power/Other	
VCC	AD10	Power/Other	
VCC	AD12	Power/Other	
VCC	AD14	Power/Other	
VCC	AD15	Power/Other	
VCC	AD17	Power/Other	
VCC	AD18	Power/Other	
VCC	AE9	Power/Other	
VCC	AE10	Power/Other	
VCC	AE12	Power/Other	
VCC	AE13	Power/Other	
VCC	AE15	Power/Other	
VCC	AE17	Power/Other	
VCC	AE18	Power/Other	
VCC	AE20	Power/Other	
VCC	AF9	Power/Other	

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	AF10	Power/Other	
VCC	AF12	Power/Other	
VCC	AF14	Power/Other	
VCC	AF15	Power/Other	
VCC	AF17	Power/Other	
VCC	AF18	Power/Other	
VCC	AF20	Power/Other	
VCC	B7	Power/Other	
VCC	B9	Power/Other	
VCC	B10	Power/Other	
VCC	B12	Power/Other	
VCC	B14	Power/Other	
VCC	B15	Power/Other	
VCC	B17	Power/Other	
VCC	B18	Power/Other	
VCC	B20	Power/Other	
VCC	C9	Power/Other	
VCC	C10	Power/Other	
VCC	C12	Power/Other	
VCC	C13	Power/Other	
VCC	C15	Power/Other	
VCC	C17	Power/Other	
VCC	C18	Power/Other	
VCC	D9	Power/Other	
VCC	D10	Power/Other	
VCC	D12	Power/Other	
VCC	D14	Power/Other	
VCC	D15	Power/Other	
VCC	D17	Power/Other	
VCC	D18	Power/Other	
VCC	E7	Power/Other	
VCC	E9	Power/Other	
VCC	E10	Power/Other	
VCC	E12	Power/Other	
VCC	E13	Power/Other	
VCC	E15	Power/Other	
VCC	E17	Power/Other	
VCC	E18	Power/Other	
VCC	E20	Power/Other	
VCC	F7	Power/Other	

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	F9	Power/Other	
VCC	F10	Power/Other	
VCC	F12	Power/Other	
VCC	F14	Power/Other	
VCC	F15	Power/Other	
VCC	F17	Power/Other	
VCC	F18	Power/Other	
VCC	F20	Power/Other	
VCCA	B26	Power/Other	
VCCA	C26	Power/Other	
VCCP	G21	Power/Other	
VCCP	J6	Power/Other	
VCCP	J21	Power/Other	
VCCP	K6	Power/Other	
VCCP	K21	Power/Other	
VCCP	M6	Power/Other	
VCCP	M21	Power/Other	
VCCP	N6	Power/Other	
VCCP	N21	Power/Other	
VCCP	R6	Power/Other	
VCCP	R21	Power/Other	
VCCP	T6	Power/Other	
VCCP	T21	Power/Other	
VCCP	V6	Power/Other	
VCCP	V21	Power/Other	
VCCP	W21	Power/Other	
VCCSENSE	AF7	Power/Other	
VID[0]	AD6	CMOS	Output
VID[1]	AF5	CMOS	Output
VID[2]	AE5	CMOS	Output
VID[3]	AF4	CMOS	Output
VID[4]	AE3	CMOS	Output
VID[5]	AF3	CMOS	Output
VID[6]	AE2	CMOS	Output
VSS	A2	Power/Other	
VSS	A4	Power/Other	
VSS	A8	Power/Other	
VSS	A11	Power/Other	
VSS	A14	Power/Other	
VSS	A16	Power/Other	

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	A19	Power/Other	
VSS	A23	Power/Other	
VSS	A25	Power/Other	
VSS	AA2	Power/Other	
VSS	AA5	Power/Other	
VSS	AA8	Power/other	
VSS	AA11	Power/Other	
VSS	AA14	Power/Other	
VSS	AA16	Power/Other	
VSS	AA19	Power/Other	
VSS	AA22	Power/Other	
VSS	AA25	Power/Other	
VSS	AB1	Power/Other	
VSS	AB4	Power/Other	
VSS	AB8	Power/Other	
VSS	AB11	Power/Other	
VSS	AB13	Power/Other	
VSS	AB16	Power/Other	
VSS	AB19	Power/Other	
VSS	AB23	Power/Other	
VSS	AB26	Power/Other	
VSS	AC3	Power/Other	
VSS	AC6	Power/Other	
VSS	AC8	Power/Other	
VSS	AC11	Power/Other	
VSS	AC14	Power/Other	
VSS	AC16	Power/Other	
VSS	AC19	Power/Other	
VSS	AC21	Power/Other	
VSS	AC24	Power/Other	
VSS	AD2	Power/Other	
VSS	AD5	Power/Other	
VSS	AD8	Power/Other	
VSS	AD11	Power/Other	
VSS	AD13	Power/Other	
VSS	AD16	Power/Other	
VSS	AD19	Power/Other	
VSS	AD22	Power/Other	
VSS	AD25	Power/Other	
VSS	AE1	Power/Other	

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	AE4	Power/Other	
VSS	AE8	Power/Other	
VSS	AE11	Power/Other	
VSS	AE14	Power/Other	
VSS	AE16	Power/Other	
VSS	AE19	Power/Other	
VSS	AE23	Power/Other	
VSS	AE26	Power/Other	
VSS	AF2	Power/Other	
VSS	AF6	Power/Other	
VSS	AF8	Power/Other	
VSS	AF11	Power/Other	
VSS	AF13	Power/Other	
VSS	AF16	Power/Other	
VSS	AF19	Power/Other	
VSS	AF21	Power/Other	
VSS	AF25	Power/Other	
VSS	B6	Power/Other	
VSS	B8	Power/Other	
VSS	B11	Power/Other	
VSS	B13	Power/Other	
VSS	B16	Power/Other	
VSS	B19	Power/Other	
VSS	B21	Power/Other	
VSS	B24	Power/Other	
VSS	C2	Power/Other	
VSS	C5	Power/Other	
VSS	C8	Power/Other	
VSS	C11	Power/Other	
VSS	C14	Power/Other	
VSS	C16	Power/Other	
VSS	C19	Power/Other	
VSS	C22	Power/Other	
VSS	C25	Power/Other	
VSS	D1	Power/Other	
VSS	D4	Power/Other	
VSS	D8	Power/Other	
VSS	D11	Power/Other	
VSS	D13	Power/Other	
VSS	D16	Power/Other	

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	D19	Power/Other	
VSS	D23	Power/Other	
VSS	D26	Power/Other	
VSS	E3	Power/Other	
VSS	E6	Power/Other	
VSS	E8	Power/Other	
VSS	E11	Power/Other	
VSS	E14	Power/Other	
VSS	E16	Power/Other	
VSS	E19	Power/Other	
VSS	E21	Power/Other	
VSS	E24	Power/Other	
VSS	F2	Power/Other	
VSS	F5	Power/Other	
VSS	F8	Power/Other	
VSS	F11	Power/Other	
VSS	F13	Power/Other	
VSS	F16	Power/Other	
VSS	F19	Power/Other	
VSS	F22	Power/Other	
VSS	F25	Power/Other	
VSS	G1	Power/Other	
VSS	G4	Power/Other	
VSS	G23	Power/Other	
VSS	G26	Power/Other	
VSS	H3	Power/Other	
VSS	H6	Power/Other	
VSS	H21	Power/Other	
VSS	H24	Power/Other	
VSS	J2	Power/Other	
VSS	J5	Power/Other	
VSS	J22	Power/Other	
VSS	J25	Power/Other	
VSS	K1	Power/Other	
VSS	K4	Power/Other	
VSS	K23	Power/Other	
VSS	K26	Power/Other	
VSS	L3	Power/Other	
VSS	L6	Power/Other	
VSS	L21	Power/Other	

Table 12. Pin Listing by Pin Name

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	L24	Power/Other	
VSS	M2	Power/Other	
VSS	M5	Power/Other	
VSS	M22	Power/Other	
VSS	M25	Power/Other	
VSS	N1	Power/Other	
VSS	N4	Power/Other	
VSS	N23	Power/Other	
VSS	N26	Power/Other	
VSS	P3	Power/Other	
VSS	P6	Power/Other	
VSS	P21	Power/Other	
VSS	P24	Power/Other	
VSS	R2	Power/Other	
VSS	R5	Power/Other	
VSS	R22	Power/Other	
VSS	R25	Power/Other	
VSS	T1	Power/Other	
VSS	T4	Power/Other	
VSS	T23	Power/Other	
VSS	T26	Power/Other	
VSS	U3	Power/Other	
VSS	U6	Power/Other	
VSS	U21	Power/Other	
VSS	U24	Power/Other	
VSS	V2	Power/Other	
VSS	V5	Power/Other	
VSS	V22	Power/Other	
VSS	V25	Power/Other	
VSS	W1	Power/Other	
VSS	W4	Power/Other	
VSS	W23	Power/Other	
VSS	W26	Power/Other	
VSS	Y3	Power/Other	
VSS	Y6	Power/Other	
VSS	Y21	Power/Other	
VSS	Y24	Power/Other	
VSSSENSE	AE7	Power/Other	Output

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
A1	Depopulated	keying option	
A2	VSS	Power/Other	
A3	SMI#	CMOS	Input
A4	VSS	Power/Other	
A5	FERR#	Open Drain	Output
A6	A20M#	CMOS	Input
A7	VCC	Power/Other	
A8	VSS	Power/Other	
A9	VCC	Power/Other	
A10	VCC	Power/Other	
A11	VSS	Power/Other	
A12	VCC	Power/Other	
A13	VCC	Power/Other	
A14	VSS	Power/Other	
A15	VCC	Power/Other	
A16	VSS	Power/Other	
A17	VCC	Power/Other	
A18	VCC	Power/Other	
A19	VSS	Power/Other	
A20	VCC	Power/Other	
A21	BCLK[1]	Bus Clock	Input
A22	BCLK[0]	Bus Clock	Input
A23	VSS	Power/Other	
A24	THRMDA	Power/Other	
A25	VSS	Power/Other	
A26	TEST6	Test	
AA1	COMP[2]	Power/Other	Input/ Output
AA2	VSS	Power/Other	
AA3	A[35]#	Source Synch	Input/ Output
AA4	A[33]#	Source Synch	Input/ Output
AA5	VSS	Power/Other	
AA6	TDI	CMOS	Input
AA7	VCC	Power/Other	
AA8	VSS	Power/other	
AA9	VCC	Power/Other	
AA10	VCC	Power/Other	
AA11	VSS	Power/Other	
AA12	VCC	Power/Other	
AA13	VCC	Power/Other	
AA14	VSS	Power/Other	

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
AA15	VCC	Power/Other	
AA16	VSS	Power/Other	
AA17	VCC	Power/Other	
AA18	VCC	Power/Other	
AA19	VSS	Power/Other	
AA20	VCC	Power/Other	
AA21	D[50]#	Source Synch	Input/ Output
AA22	VSS	Power/Other	
AA23	D[45]#	Source Synch	Input/ Output
AA24	D[46]#	Source Synch	Input/ Output
AA25	VSS	Power/Other	
AA26	DSTBP[2]#	Source Synch	Input/ Output
AB1	VSS	Power/Other	
AB2	A[34]#	Source Synch	Input/ Output
AB3	TDO	Open Drain	Output
AB4	VSS	Power/Other	
AB5	TMS	CMOS	Input
AB6	TRST#	CMOS	Input
AB7	VCC	Power/Other	
AB8	VSS	Power/Other	
AB9	VCC	Power/Other	
AB10	VCC	Power/Other	
AB11	VSS	Power/Other	
AB12	VCC	Power/Other	
AB13	VSS	Power/Other	
AB14	VCC	Power/Other	
AB15	VCC	Power/Other	
AB16	VSS	Power/Other	
AB17	VCC	Power/Other	
AB18	VCC	Power/Other	
AB19	VSS	Power/Other	
AB20	VCC	Power/Other	
AB21	D[52]#	Source Synch	Input/ Output
AB22	D[51]#	Source Synch	Input/ Output
AB23	VSS	Power/Other	
AB24	D[33]#	Source Synch	Input/ Output
AB25	D[47]#	Source Synch	Input/ Output

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
AB26	VSS	Power/Other	
AC1	PREQ#	Common Clock	Input
AC2	PRDY#	Common Clock	Output
AC3	VSS	Power/Other	
AC4	BPM[3]#	Common Clock	Input/ Output
AC5	TCK	CMOS	Input
AC6	VSS	Power/Other	
AC7	VCC	Power/Other	
AC8	VSS	Power/Other	
AC9	VCC	Power/Other	
AC10	VCC	Power/Other	
AC11	VSS	Power/Other	
AC12	VCC	Power/Other	
AC13	VCC	Power/Other	
AC14	VSS	Power/Other	
AC15	VCC	Power/Other	
AC16	VSS	Power/Other	
AC17	VCC	Power/Other	
AC18	VCC	Power/Other	
AC19	VSS	Power/Other	
AC20	DINV[3]#	Source Synch	Input/ Output
AC21	VSS	Power/Other	
AC22	D[60]#	Source Synch	Input/ Output
AC23	D[63]#	Source Synch	Input/ Output
AC24	VSS	Power/Other	
AC25	D[57]#	Source Synch	Input/ Output
AC26	D[53]#	Source Synch	Input/ Output
AD1	BPM[2]#	Common Clock	Output
AD2	VSS	Power/Other	
AD3	BPM[1]#	Common Clock	Output
AD4	BPM[0]#	Common Clock	Input/ Output
AD5	VSS	Power/Other	
AD6	VID[0]	CMOS	Output
AD7	VCC	Power/Other	
AD8	VSS	Power/Other	
AD9	VCC	Power/Other	
AD10	VCC	Power/Other	
AD11	VSS	Power/Other	

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
AD12	VCC	Power/Other	
AD13	VSS	Power/Other	
AD14	VCC	Power/Other	
AD15	VCC	Power/Other	
AD16	VSS	Power/Other	
AD17	VCC	Power/Other	
AD18	VCC	Power/Other	
AD19	VSS	Power/Other	
AD20	D[54]#	Source Synch	Input/ Output
AD21	D[59]#	Source Synch	Input/ Output
AD22	VSS	Power/Other	
AD23	D[61]#	Source Synch	Input/ Output
AD24	D[49]#	Source Synch	Input/ Output
AD25	VSS	Power/Other	
AD26	GTLREF	Power/Other	Input
AE1	VSS	Power/Other	
AE2	VID[6]	CMOS	Output
AE3	VID[4]	CMOS	Output
AE4	VSS	Power/Other	
AE5	VID[2]	CMOS	Output
AE6	PSI#	CMOS	Output
AE7	VSSSENSE	Power/Other	Output
AE8	VSS	Power/Other	
AE9	VCC	Power/Other	
AE10	VCC	Power/Other	
AE11	VSS	Power/Other	
AE12	VCC	Power/Other	
AE13	VCC	Power/Other	
AE14	VSS	Power/Other	
AE15	VCC	Power/Other	
AE16	VSS	Power/Other	
AE17	VCC	Power/Other	
AE18	VCC	Power/Other	
AE19	VSS	Power/Other	
AE20	VCC	Power/Other	
AE21	D[58]#	Source Synch	Input/ Output
AE22	D[55]#	Source Synch	Input/ Output
AE23	VSS	Power/Other	

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
AE24	D[48]#	Source Synch	Input/ Output
AE25	DSTBN[3]#	Source Synch	Input/ Output
AE26	VSS	Power/Other	
AF1	TEST5	Test	
AF2	VSS	Power/Other	
AF3	VID[5]	CMOS	Output
AF4	VID[3]	CMOS	Output
AF5	VID[1]	CMOS	Output
AF6	VSS	Power/Other	
AF7	VCCSENSE	Power/Other	
AF8	VSS	Power/Other	
AF9	VCC	Power/Other	
AF10	VCC	Power/Other	
AF11	VSS	Power/Other	
AF12	VCC	Power/Other	
AF13	VSS	Power/Other	
AF14	VCC	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VCC	Power/Other	
AF18	VCC	Power/Other	
AF19	VSS	Power/Other	
AF20	VCC	Power/Other	
AF21	VSS	Power/Other	
AF22	D[62]#	Source Synch	Input/ Output
AF23	D[56]#	Source Synch	Input/ Output
AF24	DSTBP[3]#	Source Synch	Input/ Output
AF25	VSS	Power/Other	
AF26	TEST4	Test	
B1	Depopulated for µFCPGA VSS for µFCBGA	Keying option	
B2	RSVD	Reserved	
B3	INIT#	CMOS	Input
B4	LINT1	CMOS	Input
B5	DPSLP#	CMOS	Input
B6	VSS	Power/Other	
B7	VCC	Power/Other	
B8	VSS	Power/Other	

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
B9	VCC	Power/Other	
B10	VCC	Power/Other	
B11	VSS	Power/Other	
B12	VCC	Power/Other	
B13	VSS	Power/Other	
B14	VCC	Power/Other	
B15	VCC	Power/Other	
B16	VSS	Power/Other	
B17	VCC	Power/Other	
B18	VCC	Power/Other	
B19	VSS	Power/Other	
B20	VCC	Power/Other	
B21	VSS	Power/Other	
B22	BSEL[0]	CMOS	Output
B23	BSEL[1]	CMOS	Output
B24	VSS	Power/Other	
B25	THRMDC	Power/Other	
B26	VCCA	Power/Other	
C1	RESET#	Common Clock	Input
C2	VSS	Power/Other	
C3	TEST7	TEST	
C4	IGNNE#	CMOS	Input
C5	VSS	Power/Other	
C6	LINT0	CMOS	Input
C7	THERMTRIP#	Open Drain	Output
C8	VSS	Power/Other	
C9	VCC	Power/Other	
C10	VCC	Power/Other	
C11	VSS	Power/Other	
C12	VCC	Power/Other	
C13	VCC	Power/Other	
C14	VSS	Power/Other	
C15	VCC	Power/Other	
C16	VSS	Power/Other	
C17	VCC	Power/Other	
C18	VCC	Power/Other	
C19	VSS	Power/Other	
C20	DBR#	CMOS	Output
C21	BSEL[2]	CMOS	Output
C22	VSS	Power/Other	
C23	TEST1	Test	
C24	TEST3	Test	

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
C25	VSS	Power/Other	
C26	VCCA	Power/Other	
D1	VSS	Power/Other	
D2	RSVD	Reserved	
D3	RSVD	Reserved	
D4	VSS	Power/Other	
D5	STPCLK#	CMOS	Input
D6	PWRGOOD	CMOS	Input
D7	SLP#	CMOS	Input
D8	VSS	Power/Other	
D9	VCC	Power/Other	
D10	VCC	Power/Other	
D11	VSS	Power/Other	
D12	VCC	Power/Other	
D13	VSS	Power/Other	
D14	VCC	Power/Other	
D15	VCC	Power/Other	
D16	VSS	Power/Other	
D17	VCC	Power/Other	
D18	VCC	Power/Other	
D19	VSS	Power/Other	
D20	IERR#	Open Drain	Output
D21	PROCHOT#	Open Drain	Input/ Output
D22	RSVD	Reserved	
D23	VSS	Power/Other	
D24	DPWR#	Common Clock	Input/ Output
D25	TEST2	Test	
D26	VSS	Power/Other	
E1	DBSY#	Common Clock	Input/ Output
E2	BNR#	Common Clock	Input/ Output
E3	VSS	Power/Other	
E4	HITM#	Common Clock	Input/ Output
E5	DPRSTP#	CMOS	Input
E6	VSS	Power/Other	
E7	VCC	Power/Other	
E8	VSS	Power/Other	
E9	VCC	Power/Other	
E10	VCC	Power/Other	
E11	VSS	Power/Other	

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
E12	VCC	Power/Other	
E13	VCC	Power/Other	
E14	VSS	Power/Other	
E15	VCC	Power/Other	
E16	VSS	Power/Other	
E17	VCC	Power/Other	
E18	VCC	Power/Other	
E19	VSS	Power/Other	
E20	VCC	Power/Other	
E21	VSS	Power/Other	
E22	D[0]#	Source Synch	Input/ Output
E23	D[7]#	Source Synch	Input/ Output
E24	VSS	Power/Other	
E25	D[6]#	Source Synch	Input/ Output
E26	D[2]#	Source Synch	Input/ Output
F1	BR0#	Common Clock	Input/ Output
F2	VSS	Power/Other	
F3	RS[0]#	Common Clock	Input
F4	RS[1]#	Common Clock	Input
F5	VSS	Power/Other	
F6	RSVD	Reserved	
F7	VCC	Power/Other	
F8	VSS	Power/Other	
F9	VCC	Power/Other	
F10	VCC	Power/Other	
F11	VSS	Power/Other	
F12	VCC	Power/Other	
F13	VSS	Power/Other	
F14	VCC	Power/Other	
F15	VCC	Power/Other	
F16	VSS	Power/Other	
F17	VCC	Power/Other	
F18	VCC	Power/Other	
F19	VSS	Power/Other	
F20	VCC	Power/Other	
F21	DRDY#	Common Clock	Input/ Output
F22	VSS	Power/Other	
F23	D[4]#	Source Synch	Input/ Output

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
F24	D[1]#	Source Synch	Input/ Output
F25	VSS	Power/Other	
F26	D[13]#	Source Synch	Input/ Output
G1	VSS	Power/Other	
G2	TRDY#	Common Clock	Input
G3	RS[2]#	Common Clock	Input
G4	VSS	Power/Other	
G5	BPRI#	Common Clock	Input
G6	HIT#	Common Clock	Input/ Output
G21	VCCP	Power/Other	
G22	D[3]#	Source Synch	Input/ Output
G23	VSS	Power/Other	
G24	D[9]#	Source Synch	Input/ Output
G25	D[5]#	Source Synch	Input/ Output
G26	VSS	Power/Other	
H1	ADS#	Common Clock	Input/ Output
H2	REQ[1]#	Source Synch	Input/ Output
H3	VSS	Power/Other	
H4	LOCK#	Common Clock	Input/ Output
H5	DEFER#	Common Clock	Input
H6	VSS	Power/Other	
H21	VSS	Power/Other	
H22	D[12]#	Source Synch	Input/ Output
H23	D[15]#	Source Synch	Input/ Output
H24	VSS	Power/Other	
H25	DINV[0]#	Source Synch	Input/ Output
H26	DSTBP[0]#	Source Synch	Input/ Output
J1	A[9]#	Source Synch	Input/ Output
J2	VSS	Power/Other	
J3	REQ[3]#	Source Synch	Input/ Output
J4	A[3]#	Source Synch	Input/ Output
J5	VSS	Power/Other	
J6	VCCP	Power/Other	

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
J21	VCCP	Power/Other	
J22	VSS	Power/Other	
J23	D[11]#	Source Synch	Input/ Output
J24	D[10]#	Source Synch	Input/ Output
J25	VSS	Power/Other	
J26	DSTBN[0]#	Source Synch	Input/ Output
K1	VSS	Power/Other	
K2	REQ[2]#	Source Synch	Input/ Output
K3	REQ[0]#	Source Synch	Input/ Output
K4	VSS	Power/Other	
K5	A[6]#	Source Synch	Input/ Output
K6	VCCP	Power/Other	
K21	VCCP	Power/Other	
K22	D[14]#	Source Synch	Input/ Output
K23	VSS	Power/Other	
K24	D[8]#	Source Synch	Input/ Output
K25	D[17]#	Source Synch	Input/ Output
K26	VSS	Power/Other	
L1	REQ[4]#	Source Synch	Input/ Output
L2	A[13]#	Source Synch	Input/ Output
L3	VSS	Power/Other	
L4	A[5]#	Source Synch	Input/ Output
L5	A[4]#	Source Synch	Input/ Output
L6	VSS	Power/Other	
L21	VSS	Power/Other	
L22	D[22]#	Source Synch	Input/ Output
L23	D[20]#	Source Synch	Input/ Output
L24	VSS	Power/Other	
L25	D[29]#	Source Synch	Input/ Output
L26	DSTBN[1]#	Source Synch	Input/ Output
M1	ADSTB[0]#	Source Synch	Input/ Output

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
M2	VSS	Power/Other	
M3	A[7]#	Source Synch	Input/ Output
M4	RSVD	Reserved	
M5	VSS	Power/Other	
M6	VCCP	Power/Other	
M21	VCCP	Power/Other	
M22	VSS	Power/Other	
M23	D[23]#	Source Synch	Input/ Output
M24	D[21]#	Source Synch	Input/ Output
M25	VSS	Power/Other	
M26	DSTBP[1]#	Source Synch	Input/ Output
N1	VSS	Power/Other	
N2	A[8]#	Source Synch	Input/ Output
N3	A[10]#	Source Synch	Input/ Output
N4	VSS	Power/Other	
N5	RSVD	Reserved	
N6	VCCP	Power/Other	
N21	VCCP	Power/Other	
N22	D[16]#	Source Synch	Input/ Output
N23	VSS	Power/Other	
N24	DINV[1]#	Source Synch	Input/ Output
N25	D[31]#	Source Synch	Input/ Output
N26	VSS	Power/Other	
P1	A[15]#	Source Synch	Input/ Output
P2	A[12]#	Source Synch	Input/ Output
P3	VSS	Power/Other	
P4	A[14]#	Source Synch	Input/ Output
P5	A[11]#	Source Synch	Input/ Output
P6	VSS	Power/Other	
P21	VSS	Power/Other	
P22	D[26]#	Source Synch	Input/ Output
P23	D[25]#	Source Synch	Input/ Output
P24	VSS	Power/Other	

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
P25	D[24]#	Source Synch	Input/ Output
P26	D[18]#	Source Synch	Input/ Output
R1	A[16]#	Source Synch	Input/ Output
R2	VSS	Power/Other	
R3	A[19]#	Source Synch	Input/ Output
R4	A[24]#	Source Synch	Input/ Output
R5	VSS	Power/Other	
R6	VCCP	Power/Other	
R21	VCCP	Power/Other	
R22	VSS	Power/Other	
R23	D[19]#	Source Synch	Input/ Output
R24	D[28]#	Source Synch	Input/ Output
R25	VSS	Power/Other	
R26	COMP[0]	Power/Other	Input/ Output
T1	VSS	Power/Other	
T2	RSVD	Reserved	
T3	A[26]#	Source Synch	Input/ Output
T4	VSS	Power/Other	
T5	A[25]#	Source Synch	Input/ Output
T6	VCCP	Power/Other	
T21	VCCP	Power/Other	
T22	D[37]#	Source Synch	Input/ Output
T23	VSS	Power/Other	
T24	D[27]#	Source Synch	Input/ Output
T25	D[30]#	Source Synch	Input/ Output
T26	VSS	Power/Other	
U1	A[23]#	Source Synch	Input/ Output
U2	A[30]#	Source Synch	Input/ Output
U3	VSS	Power/Other	
U4	A[21]#	Source Synch	Input/ Output
U5	A[18]#	Source Synch	Input/ Output
U6	VSS	Power/Other	

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
U21	VSS	Power/Other	
U22	DINV[2]#	Source Synch	Input/ Output
U23	D[39]#	Source Synch	Input/ Output
U24	VSS	Power/Other	
U25	D[38]#	Source Synch	Input/ Output
U26	COMP[1]	Power/Other	Input/ Output
V1	ADSTB[1]#	Source Synch	Input/ Output
V2	VSS	Power/Other	
V3	RSVD	Reserved	
V4	A[31]#	Source Synch	Input/ Output
V5	VSS	Power/Other	
V6	VCCP	Power/Other	
V21	VCCP	Power/Other	
V22	VSS	Power/Other	
V23	D[36]#	Source Synch	Input/ Output
V24	D[34]#	Source Synch	Input/ Output
V25	VSS	Power/Other	
V26	D[35]#	Source Synch	Input/ Output
W1	VSS	Power/Other	
W2	A[27]#	Source Synch	Input/ Output
W3	A[32]#	Source Synch	Input/ Output
W4	VSS	Power/Other	
W5	A[28]#	Source Synch	Input/ Output
W6	A[20]#	Source Synch	Input/ Output
W21	VCCP	Power/Other	
W22	D[41]#	Source Synch	Input/ Output
W23	VSS	Power/Other	
W24	D[43]#	Source Synch	Input/ Output
W25	D[44]#	Source Synch	Input/ Output
W26	VSS	Power/Other	
Y1	COMP[3]	Power/Other	Input/ Output

Table 13. Pin Listing by Pin Number

Pin #	Pin Name	Signal Buffer Type	Direction
Y2	A[17]#	Source Synch	Input/ Output
Y3	VSS	Power/Other	
Y4	A[29]#	Source Synch	Input/ Output
Y5	A[22]#	Source Synch	Input/ Output
Y6	VSS	Power/Other	
Y21	VSS	Power/Other	
Y22	D[32]#	Source Synch	Input/ Output
Y23	D[42]#	Source Synch	Input/ Output
Y24	VSS	Power/Other	
Y25	D[40]#	Source Synch	Input/ Output
Y26	DSTBN[2]#	Source Synch	Input/ Output

Table 14. Signal Description (Sheet 1 of 8)

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the processor FSB. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps, which are sampled before RESET# is deasserted.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address Bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/ output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** / **Associated Strobe** REQ[4:0]#, A[16:3]# / ADSTB[0]# A[35:17]# / ADSTB[1]#
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:1]# BPM[3,0]#	Output Input/ Output	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all processor FSB agents.This includes debug or performance monitoring tools. Refer to the appropriate *eXtended Debug Port: Debug Port Design Guide for UP and DP Platforms for detailed information.*

Table 14. Signal Description (Sheet 2 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BPRI#</td><td>Input</td><td>BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.</td></tr>
<tr><td>BR0#</td><td>Input/ Output</td><td>BR0# is used by the processor to request the bus. The arbitration is done between the processor (Symmetric Agent) and GMCH (High Priority Agent).</td></tr>
<tr><td>BSEL[2:0]</td><td>Output</td><td>BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. Table 3 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency.</td></tr>
<tr><td>COMP[3:0]</td><td>Analog</td><td>COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors.
Refer to the appropriate platform design guide for more details on implementation.</td></tr>
<tr><td>D[63:0]#</td><td>Input/ Output</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#
.
Quad-Pumped Signal Groups
<table>
<tr><th>Data Group</th><th>DSTBN# / DSTBP#</th><th>DINV#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBR#</td><td>Output</td><td>DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no-connect in the system. DBR# is not a processor signal.</td></tr>
</table>

Table 14. Signal Description (Sheet 3 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both FSB agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be ensured in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or input/ output agent. This signal must connect the appropriate pins of both FSB agents.</td></tr>
<tr><td>DINV[3:0]#</td><td>Input/ Output</td><td>DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.
DINV[3:0]# Assignment to Data Bus
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DINV[3]#</td><td>D[63:48]#</td></tr>
<tr><td>DINV[2]#</td><td>D[47:32]#</td></tr>
<tr><td>DINV[1]#</td><td>D[31:16]#</td></tr>
<tr><td>DINV[0]#</td><td>D[15:0]#</td></tr>
</table></td></tr>
<tr><td>DPRSTP#</td><td>Input</td><td>DPRSTP#, when asserted on the platform, causes the processor to transition from the Deep Sleep State to the Deeper Sleep state or C6 state. To return to the Deep Sleep State, DPRSTP# must be deasserted. DPRSTP# is driven by the ICH8M chipset.</td></tr>
<tr><td>DPSLP#</td><td>Input</td><td>DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. To return to the Sleep State, DPSLP# must be deasserted. DPSLP# is driven by the ICH8M chipset.</td></tr>
<tr><td>DPWR#</td><td>Input/ Output</td><td>DPWR# is a control signal used by the chipset to reduce power on the processor data bus input buffers. The processor drives this pin during dynamic FSB frequency switching.</td></tr>
<tr><td>DRDY#</td><td>Input/ Output</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr>
<tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr>
<tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr>
<tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr>
</table></td></tr>
</table>

Table 14. Signal Description (Sheet 4 of 8)

Name	Type	Description
DSTBP[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. Signals / Associated Strobe: D[15:0]#, DINV[0]# — DSTBP[0]# D[31:16]#, DINV[1]# — DSTBP[1]# D[47:32]#, DINV[2]# — DSTBP[2]# D[63:48]#, DINV[3]# — DSTBP[3]#
FERR#/PBE#	Output	FERR# (Floating-point Error)/PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volumes 3A and 3B of the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* and the *CPUID Instruction Application Note*. Refer to the appropriate platform design guide for termination requirements.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a Logical 0 or Logical 1.
HIT# HITM#	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall that can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by the processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.

Table 14. Signal Description (Sheet 5 of 8)

Name	Type	Description
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a non-control floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in Control Register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output write bus transaction. INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active-to-inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software-configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the FSB throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	Output	Probe Ready signal used by debug tools to determine processor debug readiness.
PREQ#	Input	Probe Request signal used by debug tools to request debug operation of the processor.

Table 14. Signal Description (Sheet 6 of 8)

Name	Type	Description
PROCHOT#	Input/ Output	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system deasserts PROCHOT#. By default PROCHOT# is configured as an output. The processor must be enabled via the BIOS for PROCHOT# to be configured as bidirectional.
PSI#	Output	Processor Power Status Indicator signal. This signal is asserted when the processor is both in the normal state (HFM to LFM) and in lower power states (Deep Sleep and Deeper Sleep).
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal remains low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents.
RSVD	Reserved/ No Connect	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use.

Table 14. Signal Description (Sheet 7 of 8)

Name	Type	Description
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued and the processor begins program execution from the SMM handler. If an SMI# is asserted during the deassertion of RESET#, then the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low-power stop-grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7	Input	TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, and TEST7 have termination requirements.
THRMDA	Other	Thermal Diode Anode.
THRMDC	Other	Thermal Diode Cathode.
THERMTRIP#	Output	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.

Table 14. Signal Description (Sheet 8 of 8)

Name	Type	Description
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
V_{CC}	Input	Processor core power supply.
V_{SS}	Input	Processor core ground node.
V_{CCA}	Input	V_{CCA} provides isolated power for the internal processor core PLLs.
V_{CCP}	Input	Processor I/O Power Supply.
V_{CC_SENSE}	Output	V_{CC_SENSE} together with V_{SS_SENSE} are voltage feedback signals to Intel® MVP6 that control the 2.1-mΩ loadline at the processor die. It should be used to sense voltage near the silicon with little noise. Refer to the platform design guide for termination and routing recommendations.
VID[6:0]	Output	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). Unlike some previous generations of processors, these are CMOS signals that are driven by the processor. The voltage supply for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 2 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
V_{SS_SENSE}	Output	V_{SS_SENSE} together with V_{CC_SENSE} are voltage feedback signals to Intel MVP6 that control the 2.1-mΩ loadline at the processor die. It should be used to sense ground near the silicon with little noise. Refer to the platform design guide for termination and routing recommendations.

§

5 Thermal Specifications

Maintaining the proper thermal environment is key to reliable, long-term system operation. A complete thermal solution includes both component and system-level thermal management features. To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so the processor remains within the minimum and maximum junction temperature (T_J) specifications at the corresponding thermal design power (TDP) value listed in Table 15. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods.

Table 15. Power Specifications for the Extreme Edition Processor

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	X9000	2.8 GHz & V_{CCHFM} 1.2 GHz & V_{CCLFM} 0.8 GHz & V_{CCSLFM}	44 29 22			W	1, 4, 5, 6
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at V_{CCHFM} at V_{CCSLFM}		—	—	17.1 7.4	W	2, 5, 7
P_{SLP}	Sleep Power at V_{CCHFM} at V_{CCSLFM}		—	—	16.1 7.1	W	2, 5, 7
P_{DSLP}	Deep Sleep Power at V_{CCHFM} at V_{CCSLFM}		—	—	7.5 4.2	W	2, 5, 8
P_{DPRSLP}	Deeper Sleep Power		—	—	1.9	W	2,8
P_{DC4}	Intel® Enhanced Deeper Sleep State Power		—	—	1.7	W	2,8
P_{C6}	Deep Power-Down Technology Power		—	—	1.3	W	2, 8
T_J	Junction Temperature		0	—	105	°C	3, 4

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode is less than TDP in HFM.
6. At Tj of 105°C
7. At Tj of 50°C
8. At Tj of 35°C

Table 16. Power Specifications for Dual-Core Standard Voltage Processors

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	T9500 T9300 T8300 T8100	2.6 GHz & V_{CCHFM} 2.5 GHz & V_{CCHFM} 2.4 GHz & V_{CCHFM} 2.1 GHz & V_{CCHFM} 1.2 GHz & V_{CCLFM} 0.8 GHz & V_{CCLFM}	35 35 35 35 22 12			W	1, 4, 5, 6
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at V_{CCHFM} at V_{CCSLFM}		—	—	12.5 5.0	W	2, 5, 7
P_{SLP}	Sleep Power at V_{CCHFM} at V_{CCSLFM}		—	—	11.8 4.8	W	2, 5, 7
P_{DSLP}	Deep Sleep Power at V_{CCHFM} at V_{CCSLFM}		—	—	5.5 2.2	W	2, 5, 8
P_{DPRSLP}	Deeper Sleep Power		—	—	1.7	W	2, 8
P_{DC4}	Intel® Enhanced Deeper Sleep State Power		—	—	1.3	W	2, 8
P_{C6}	Deep Power-Down Technology Power		—	—	0.3	W	2, 8
T_J	Junction Temperature		0	—	105	°C	3, 4

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. Processor TDP requirements in Intel Dynamic Acceleration Technology mode is lesser than TDP in HFM.
6. At Tj of 105°C
7. At Tj of 50°C
8. At Tj of 35°C

5.1 Thermal Features

The processor requires a thermal solution to maintain temperatures within operating limits as set forth in Section 5.1.

Caution: Operating the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system.

The processor incorporates three methods of monitoring die temperature:

- Thermal diode
- Intel Thermal Monitor
- Digital thermal sensor

Note: The Intel Thermal Monitor (detailed in Section 5.1.2) must be used to determine when the maximum specified processor junction temperature has been reached.

5.1.1 Thermal Diode

Intel's processors utilize an SMBus thermal sensor to read back the voltage/current characteristics of a substrate PNP transistor. Since these characteristics are a function of temperature, in principle one can use these parameters to calculate silicon temperature values. For older silicon process technologies it was possible to simplify the voltage/current and temperature relationships by treating the substrate transistor as though it were a simple diffusion diode. In this case, the assumption is that the beta of the transistor does not impact the calculated temperature values. The resultant diode model essentially predicts a quasi linear relationship between the base/emitter voltage differential of the PNP transistor and the applied temperature (one of the proportionality constants in this relationship is processor specific, and is known as the diode ideality factor). Realization of this relationship is accomplished with the SMBus thermal sensor that is connected to the transistor.

This processor, however, is built on Intel's advanced 45-nm processor technology. Due to this new, highly-advanced processor technology, it is no longer possible to model the substrate transistor as a simple diode. To accurately calculate silicon temperature one must use a full bi-polar junction transistor-type model. In this model, the voltage/current and temperature characteristics include an additional process dependant parameter which is known as the transistor "beta". System designers should be aware that the current thermal sensors on Santa Rosa platforms may not be configured to account for "beta" and should work with their SMB thermal sensor vendors to ensure they have a part capable of reading the thermal diode in BJT model.

Offset between the thermal diode-based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events. This offset is different than the diode Toffset value programmed into the processor model-specific register (MSR).

Table 17 to Table 18 provide the diode interface and transistor model specifications.

Table 17. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	A24	Thermal diode anode
THERMDC	B25	Thermal diode cathode

Table 18. Thermal Diode Parameters using Transistor Model

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5	—	200	µA	1
I_E	Emitter Current	5	—	200	µA	1
n_Q	Transistor Ideality	0.997	1.001	1.008		2, 3, 4
Beta		0.1	0.4	0.5		2, 3
R_T	Series Resistance	3.0	4.5	7.0	Ω	2

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50-105°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

$$I_C = I_S * (e^{qV_{BE}/n_Q kT} - 1)$$

where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).

5.1.2 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (thermal control circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power-intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep Technology transition when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

There are two automatic modes called Intel Thermal Monitor 1 (TM1) and Intel Thermal Monitor 2 (TM2). These modes are selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

When TM1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed-dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid

active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

When TM2 is enabled and a high temperature situation exists, the processor will perform an Enhanced Intel SpeedStep Technology transition to the LFM. When the processor temperature drops below the critical level, the processor will make an Enhanced Intel SpeedStep Technology transition to the last requested operating point. The processor also supports Enhanced Multi Threaded Thermal Monitoring (EMTTM). EMTTM is a processor feature that enhances TM2 with a processor throttling algorithm known as Adaptive TM2. Adaptive TM2 transitions to intermediate operating points, rather than directly to the LFM, once the processor has reached its thermal limit and subsequently searches for the highest possible operating point. Please ensure this feature is enabled and supported in the BIOS. Also with EMTTM enabled, the OS can request the processor to throttling to any point between Intel Dynamic Acceleration Technology frequency and SuperLFM frequency as long as these features are enabled in the BIOS and supported by the processor.

The Intel Thermal Monitor automatic mode and Enhanced Multi Threaded Thermal Monitoring must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 and TM2 be enabled on the processors.

TM1, TM2 and EMTTM features are collectively referred to as adaptive thermal monitoring features.

TM1 and TM2 can co-exist within the processor. If both TM1 and TM2 bits are enabled in the auto-throttle MSR, TM2 will take precedence over TM1. However, if Force TM1 over TM2 is enabled in MSRs via BIOS and TM2 is not sufficient to cool the processor below the maximum operating temperature, then TM1 will also activate to help cool down the processor.

If a processor load-based Enhanced Intel SpeedStep Technology transition (through MSR write) is initiated when a TM2 period is active, there are two possible results:

1. If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is **higher** than the TM2 transition-based target frequency, the processor load-based transition will be deferred until the TM2 event has been completed.
2. If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is **lower** than the TM2 transition-based target frequency, the processor will transition to the processor load-based Enhanced Intel SpeedStep Technology target frequency point.

The TCC may also be activated via on-demand mode. If Bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately, independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via Bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on/50% off; however, in on-demand mode the duty cycle can be programmed from 12.5% on/87.5% off to 87.5% on/12.5% off, in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

PROCHOT# will not be asserted when the processor is in the Stop Grant, Sleep, Deep Sleep, and Deeper Sleep low-power states, hence the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low-power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the low-power state and the processor junction temperature drops below the thermal trip point.

If thermal monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125°C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

In all cases, the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

5.1.3 Digital Thermal Sensor

The processor also contains an on-die digital thermal sensor (DTS) that can be read via an MSR (no I/O interface). Each core of the processor will have a unique digital thermal sensor whose temperature is accessible via the processor MSRs. The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation via the thermal monitor. The DTS is only valid while the processor is in the normal operating state (the normal package level low-power state).

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor ($T_{J,max}$). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below $T_{J,max}$. Catastrophic temperature conditions are detectable via an out of specification status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the out of specification status bit is set.

The DTS-relative temperature readout corresponds to the thermal monitor (TM1/TM2) trigger point. When the DTS indicates maximum processor core temperature has been reached, the TM1 or TM2 hardware thermal control mechanism will activate. The DTS and TM1/TM2 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient between the individual core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach, and software application. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

5.2 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shutdown before the THERMTRIP# is activated. If the processor's TM1 or TM2 are triggered and the temperature remains high, an "Out Of Spec" status and sticky bit are latched in the status MSR register, and it generates a thermal interrupt.

5.3 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If TM1 or TM2 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a package level of the processor. When either core's thermal sensor trips, PROCHOT# signal will be driven by the processor package. If only TM1 is enabled, PROCHOT# will be asserted regardless of which core is above TCC temperature trip point, and both cores will have their core clocks modulated. If TM2 is enabled, then regardless of which core(s) are above TCC temperature trip point, both cores will enter the lowest programmed TM2 performance state. It is important to note that Intel recommends both TM1 and TM2 to be enabled.

When PROCHOT# is driven by an external agent, if only TM1 is enabled on both cores, then both processor cores will have their core clocks modulated. If TM2 is enabled on both cores, then both processor cores will enter the lowest programmed TM2 performance state. It should be noted that force TM1 on TM2, enabled via BIOS, does not have any effect on external PROCHOT#. If PROCHOT# is driven by an external agent when TM1, TM2, and force TM1 on TM2 are all enabled, then the processor will still apply only TM2.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power-intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss. §