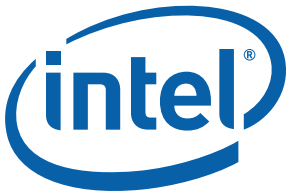

Intel® Core™2 Duo Processor T9400 and Intel® 5100 Memory Controller Hub Chipset

Development Kit User Guide

July 2008

Revision 001US

Order Number: 319653-001US

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Revision History

Date	Revision	Description
July 2008	001	Initial release

Revision Number Descriptions

Revision	Associated Life Cycle Milestone	Release Information
0.0	POP L3 Closure	Initial Documentation - Typically Internal Only
0.1–0.4	When Needed	Project Dependent - Typically Internal Only
0.5	Design Win Phase	First, Required Customer Release
0.6–0.7	When Needed	Project Dependent
0.7	Simulations Complete	Second, Recommended Customer Release
0.8–0.9	When Needed	Project Dependent
1.0	First Silicon Samples	Required Customer Release
1.1–1.4	When Needed	Project Dependent (Recommended)
1.5	Qualification Silicon Samples	Project Dependent
1.6–1.9	When Needed	Project Dependent
NDA - 2.0 Public - XXXXXX-001	First SKU Launch	Required Customer Release - Product Launch
2.1 and up	When Needed	Project Dependent

Note: Rows highlighted in gray are required revisions.

1.0 Product Description

1.1 Overview - Feature Summary

The Development Kit's Customer Reference Board (CRB) is a single-socket Intel® Core™2 Duo Processor T9400-based server platform that utilizes the Intel® 5100 MCH Chipset with DDR2 memory and the ICH9R. The platform chipset provides a single Front Side Bus (FSB) and supports the Intel® Core™2 Duo Processor T9400 using µFCPGA sockets. See Figure 1 below for overview.

Figure 1. Block Diagram

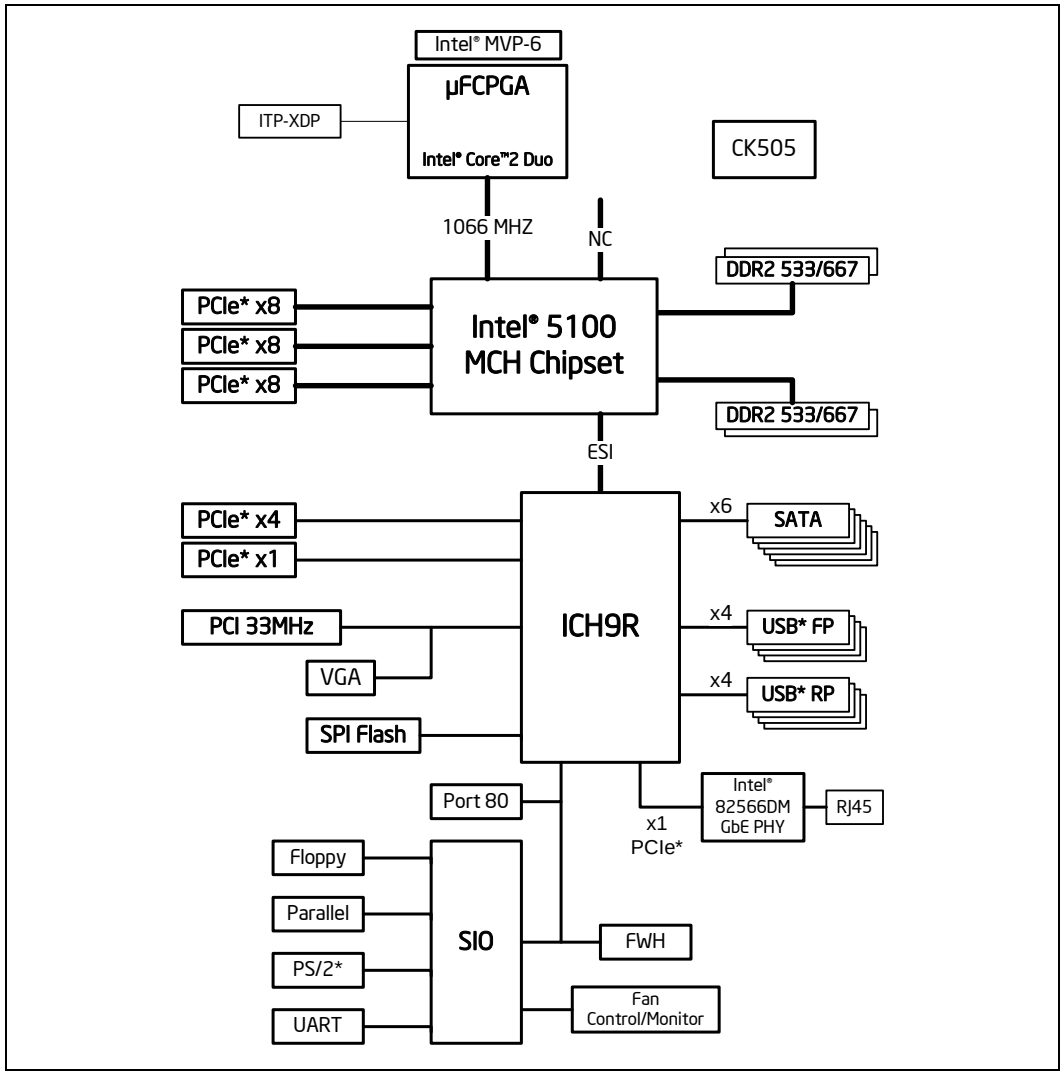


Table 1 summarizes the major features of the Customer Reference Board.

Table 1. Feature Summary

Feature	Description
Form Factor	Similar to Extended ATX (12.0 x 13.0 inches) and SSI 460 W power supply
Processors	One µFCPGA socket supporting the Intel® Core™2 Duo Processor T9400 - additional documentation is available at http://www.intel.com/design/intarch/devkits/5100MCH/index.htm (Additional processor information can be found in Table 4 on page 12.)
Chipset	Intel® 5100 MCH Chipset and Intel® 82801IR I/O Controller Hub (ICH9R)
Memory	Supports 533/667 MHz DDR2 Registered 240-pin ECC DIMMs only (four total) Up to 32 GB of system memory is supported
PCI Express*	Three x8 slots, One x4 slot, One x1 slot (*PCI Express* Base Specification*, Rev. 1.0a; all slots employ physical x8 connectors)
PCI	One *PCI Local Bus Specification*, Rev. 2.3 compliant 32-bit/33 MHz slot
Serial ATA	Six SATA 2 ports with AHCI support
USB*	Eight USB* 2.0 ports (four back panel and four front panel) UHCI or EHCI configurations
Video	On-board PCI video controller with standard VGA connector
LAN Support	Single 10/100/1000 network controller with RJ-45 connector
Other I/Os	• One floppy drive interface • PS/2* keyboard and mouse ports • One serial port • One parallel port
BIOS	• LPC FWH (8 MB) • SPI Flash (16 MB) Support for Advanced Configuration and Power Interface (ACPI), plug-and-play, SMBIOS
Hardware Subsystem	Supports S0, S3, S4, and S5 Sleep states Fan support • Four fan connectors with tachometer monitoring • Two fan connectors support PWM speed control inputs Monitoring • Thermal sense to detect out of range temperatures in the CPU and MCH. • Voltage sense to detect out of range voltages from either CPU Intel® MVP-6, the MCH 1.5 V core, and the DDR2 1.8 V power supplies. Debug • ITP-XDP0 connector for CPU • ITP-XDP1 connector for MCH

Table 2 describes what is included in the Development Kit.

Table 2. Development Kit Contents (Sheet 1 of 2)

Feature	Description
Customer Reference Board	PCB assembled with one µFCPGA-479 socket, Intel® 5100 MCH Chipset with active heatsink, and Intel® 82801IR I/O Controller Hub (ICH9R) passive heatsink
Processors	Intel® Core™2 Duo Processor T9400
Processor Heatsink	One Active Heatsink
Memory	Minimum of two 512 MB DDR2-667 DIMMs
Hard Drive	One SATA Hard Drive with cable

Table 2. Development Kit Contents (Sheet 2 of 2)

Feature	Description
Input/Output Device	One SATA Optical Drive with cable
Firmware Hub	Socketed LPC Firmware Hub (1 MB PLCC) for BIOS
Power Supply	SSI EPS12V 460 W silver box supply
Additional Peripherals	Acrylic stand with flame retardant pad (with installation hardware) ***Warning:*** Placing the board on an unknown surface without the acrylic stand may short the CRB and result in damage. If the CRB is not mounted in a chassis, Intel recommends using the provided acrylic stand or using standoffs to prevent risk of the bottom of the CRB shorting on a conductive surface.

Ensure a safe and static-free work environment before removing any components from their anti-static packaging. The Development Platform is susceptible to electrostatic discharge, which may cause failure or unpredictable operation.

Warning: The Development Platform must be operated on a flame retardant surface or the provided acrylic stand because a chassis is not included with the platform.

Caution: Connecting the wrong cable or reversing a cable may damage the board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to the board.

Caution: The power supply cord is the main disconnect device to the main power (AC power). The socket outlet should be installed near the equipment and should be readily accessible. To avoid shock, ensure that the power cord is connected to a properly wired and grounded receptacle. Do not connect/disconnect any cables or perform installation/ maintenance of the boards in this product during an electrical storm. Ensure that any equipment to which this product will be attached is also connected to properly wired and grounded receptacles.

Ensure that setting up the ATX power supply is the final step performed in the process of assembly.

Once the board is set up, plug the power cable into the back of the power supply, leaving the switch in the OFF position; then plug the cord into the power source and switch on the power supply.

The Intel® Electronic Design Kit (EDK) provides online, real-time collateral updates. The following link takes you to the EDK server and requires you to log into Intel® Business Link (IBL): Intel® Core™2 Duo Processors T9400 and SL9400 and Intel® 5100 Memory Controller Hub Chipset for Communications and Embedded Applications.

Table 3. Related Documents (Sheet 1 of 2)

Document	URL (Document Number)
ATX Specification Rev 2.02	http://www.formfactors.org/ formfactor.asp
Intel® 5100 Memory Controller Hub Chipset Datasheet	http://www.intel.com/ (318378)
Intel® 5100 Memory Controller Hub Chipset for Communications, Embedded, and Storage Applications Thermal/Mechanical Design Guide	http://www.intel.com/ (318676)
Intel® 5100 Memory Controller Hub Chipset Specification Update	http://www.intel.com/ (318385)

Notes:
1. Contact your Intel sales representative.

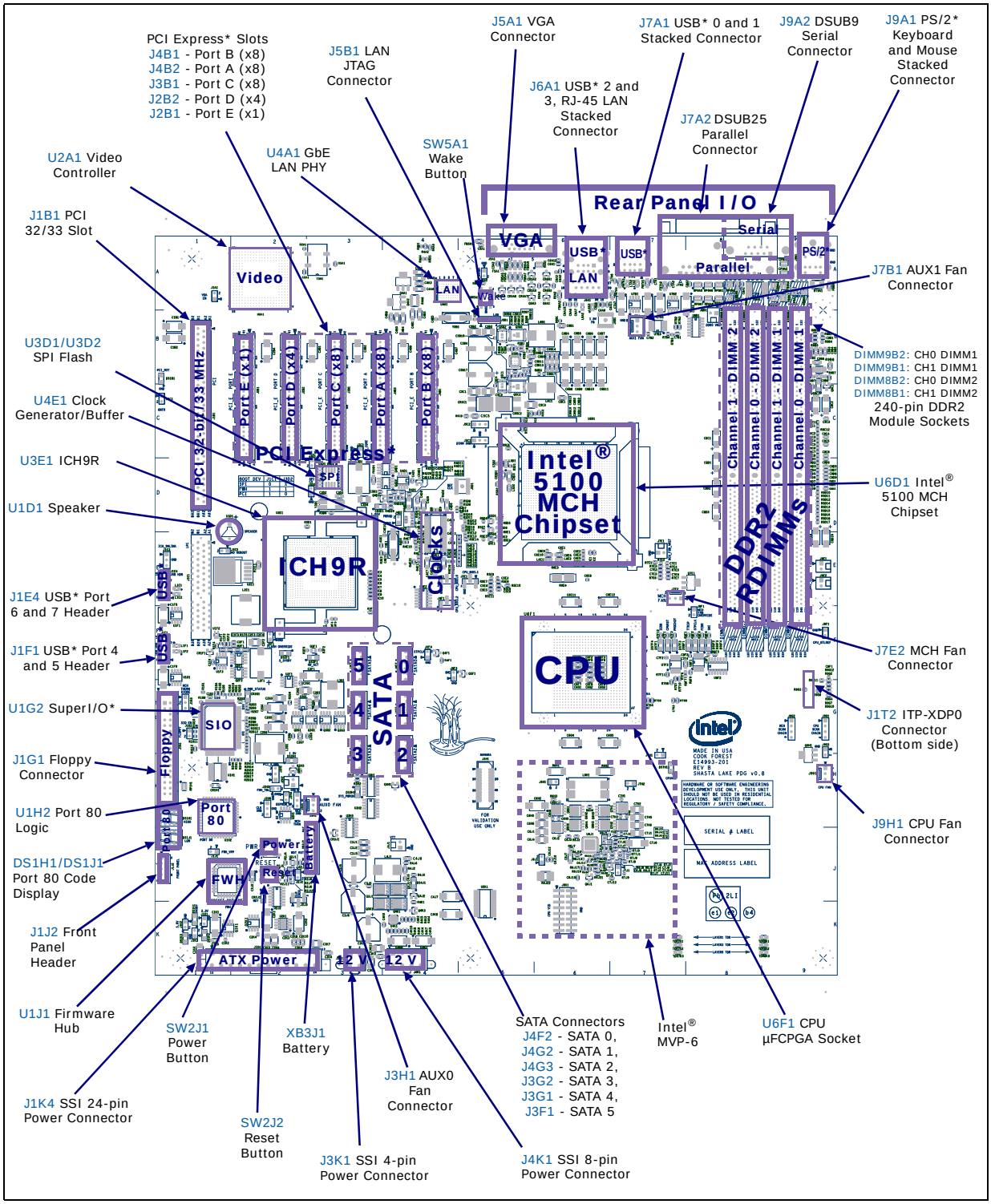
Table 3. Related Documents (Sheet 2 of 2)

Document	URL (Document Number)
Intel® Core™2 Duo Processors and Intel® Core™2 Extreme Processors on 45-nm Process Datasheet	http://www.intel.com/ (320120)
Intel® Core™2 Duo Processors and Intel® Core™2 Extreme Processors on 45-nm Process Specification Update	http://www.intel.com/ (320121)
Intel® Core™2 Duo Processors on 45-nm process for Embedded Applications Thermal Design Guide	http://www.intel.com/ (320028)
Intel® I/O Controller Hub 9 (ICH9) Family Datasheet	http://www.intel.com/ (316972)
Intel® I/O Controller Hub 9 (ICH9) Family Specification Update	http://www.intel.com/ (316973)
Intel® I/O Controller Hub 9 (ICH9) Family Thermal and Mechanical Design Guidelines	http://www.intel.com/ (316974)
Intel® Mobile Processor Micro-FCPGA Socket (mPGA479M) Design Guidelines	http://www.intel.com/ (298520)
PCI Express* Base Specification, Rev. 1.0a	http://www.pcisig.com/specifications/pciexpress/
PCI Local Bus Specification, Rev. 2.3	http://www.pcisig.com/specifications/conventional/
SSI Specification	http://ssiforum.org/specifications.aspx

Notes:
1. Contact your Intel sales representative.

1.2 Board Overview

Figure 2. Main Component Layout Reference



Note: Component reference designators are defined by their type, board mapped location, and end with a numerical index. The board mapped locations are sectioned horizontally 1 through 9 and vertically A through K on a grid pattern. The bottom side of the board has a similar grid pattern but with different call-outs. See grid call-outs along the edges of the board. U6D1, for example, is an IC (U), is on the top of the board at cross section 6D, and is the first indexed component (1) of that type in that area.

1.3 Processors and Chipset

The CRB is designed to support the following processor with a 1066 MT/s FSB speed.

Use only the processor listed in Table 4. Use of unsupported processors can damage the CRB, the processor, and the power supply.

Note: In this document, “processor” refers to the processor SKU listed in Table 4.

Table 4. Processors and Chipset

Ref Des Location	Description	
U6F1	CPU µFCPGA Socket	Intel® Core™2 Duo Processor T9400 (2.53 GHz, 1066 MHz, 35 W)
U6D1	Memory Controller Hub	Intel® 5100 MCH Chipset
U3E1	ICH9R	Intel® 82801IR I/O Controller Hub

1.4 System Memory

The CRB has four DIMM sockets and supports the following memory features:

- Supports DDR2-533/667 Registered ECC DIMMs only
- Two independent Channels with up to four Ranks per Channel
- Total system memory range
  - — Minimum of 256 MB for a Single Channel
  - — Maximum of 32 GB for Dual Channel
- Supports 256 Mb to 2 Gb device technologies
- Uses 240-pin vertical DIMMs only
- Raw cards A through L are supported
- Supports DIMM Self Refresh mode for low power (S3) mode

Table 5. System Memory Slots

Ref Des Location	Description	
DIMM9B2	Channel 0 - DIMM Slot 1	Typical RDIMMs supported: • **512 MB**: 667 MT/s, Single-Rank, x8, 512 Mb • **1 GB**: 533/667, Single-Rank, x4, 512 Mb • **2 GB**: 533/667, Dual-Rank, x4, 512 Mb • **2 GB**: 533/667, Single-Rank, x4, 1 Gb • **4 GB**: 533/667, Dual-Rank, x4, 1 Gb
DIMM9B1	Channel 1 - DIMM Slot 1	
DIMM8B2	Channel 0 - DIMM Slot 2	
DIMM8B1	Channel 1 - DIMM Slot 2	

1.4.1 DDR2-533/667 DIMM Slot Populations

Table 6 shows the supported DDR2-533/667 MHz RDIMM populations.

Table 6. DDR2-533/667 MHz DIMM Population Guidelines

Channel 1 DIMM 2	Channel 0 DIMM 2	Channel 1 DIMM 1	Channel 0 DIMM 1
Empty	*Empty*	Single-Rank	Single-Rank
Single-Rank	Single-Rank	Single-Rank	Single-Rank
Empty	*Empty*	Dual-Rank	Dual-Rank
Dual-Rank	Dual-Rank	Dual-Rank	Dual-Rank
Dual-Rank	Dual-Rank	Single-Rank	Single-Rank
Single-Rank	Single-Rank	Dual-Rank	Dual-Rank

Notes:
1. DIMM slots are shown as physically oriented with respect to the Intel® 5100 MCH Chipset.
2. DIMMs must be populated first in the slots furthest from the Intel® 5100 MCH Chipset.
3. Match DIMM 1 to DIMM 1 and DIMM 2 to DIMM 2 between channels.

1.5 Peripherals and I/O

1.5.1 On-board Peripheral Components

Table 7 below shows the on-board peripheral components indicated in Figure 2 on page 11.

Table 7. On-board Peripheral Devices

Ref Des Location	Description	
U4A1	GbE LAN PHY	Intel® 82566DM Gigabit Ethernet PHY • Provides 10/100/1000 LAN connection in conjunction with an integrated MAC in the ICH9R component
U2A1	PCI Video	A Silicon Motion* integrated video controller (SM712G) is located on the 32-bit, 33 MHz PCI bus.
U4E1	Clock Generator	CK505 Clock Generator (ICS* ICS9LPR501)
U1G2	SuperI/O*	The SIO (SMSC* SCH5027) is driven by the Low Pin Count (LPC) bus.
U1J1	Firmware Hub (FWH)	8 MB socketed PLCC *(primary boot)*
U3D1/ U3D2	SPI Flash	16 Mb with dual footprint for 8 or 16-pin devices
SW2J1	Power Button	
SW2J2	Reset Button	
SW5A1	Wake Button	
U1H2	Port 80 Logic Device	Xilinx* EPM7064 FPGA
DS1H1/ DS1J1	Port 80 Code Display	Two digit, 7-segment LED character displays
U1D1	Speaker	Board-mounted piezoelectric speaker
XB3J1	Battery	3 V Lithium CR2032 coin battery for Real Time Clock (RTC) and CMOS memory backup

1.5.2 On-board I/O Connections

Table 8 below shows the on-board I/O connections indicated in Figure 2 on page 11.

Table 8. On-board I/O Connections

Ref Des Location	Description	
J4F2	Serial ATA Port 0	The CRB provides a total of six SATA 2 interface connectors.
J4G2	Serial ATA Port 1	
J4G3	Serial ATA Port 2	
J3G2	Serial ATA Port 3	
J3G1	Serial ATA Port 4	
J3F1	Serial ATA Port 5	
J1F1	USB* Port 4 and 5 Header	These are 10-pin, dual-row headers that route two USB* Ports per header to an external USB* connector. In conjunction with the rear panel USB* Ports there are a total of eight USB* ports.
J1E4	USB* Port 6 and 7 Header	
J1G1	Floppy Connector	This is a 34-pin, dual-row header. The control interface comes from the SuperI/O*. Configuration of the floppy drive interface is provided by the BIOS Setup program.
J1J2	Front Panel Header	This is a 10-pin, dual-row header. It provides pins for: • Power Switch • Reset Switch • Power-on LED • HD Status LED See "9-pin Front Panel Connector Pins (Top-View)" for connector pin out.
J9H1	CPU Fan Header	3-wire with PWM fan speed control. See"3-Wire Fan Connectors (CPU, MCH, AUX0, and AUX1)" for connector pin out.
J7E2	MCH Fan Header	
J3H1	AUX0 Fan Header	3-wire with no fan speed control.
J7B1	AUX1 Fan Header	
J1T2	XDP0 CPU Connector	This is a bottom-side 60-pin connector for the ITP-XDP debug of the processors. XDP stands for Extended Debug Port and can be used for debugging and testing components on the board.
J6L1	XDP1 MCH Connector	An optional ITP-XDP debug port for the MCH. The connector is not installed on the CRB (*default*).
J5B1	LAN JTAG Connector	Dedicated JTAG connector to the LAN PHY device

1.5.3 Expansion I/O Slots

Table 9 below shows the expansion I/O slots indicated in Figure 2 on page 11.

Table 9. Expansion I/O Slots

Ref Des Location	Description	
J4B2	PCI Express* Port A (x8)	All of the PCI Express* Ports are *PCI Express* Base Specification*, Rev. 1.0a compliant and employ physical x8 connectors regardless of whether they are x1, x4, or x8. This enables use of x8 cards even if actual bandwidth and functionality is less.
J4B1	PCI Express* Port B (x8)	
J3B1	PCI Express* Port C (x8)	
J2B2	PCI Express* Port D (x4)	
J2B1	PCI Express* Port E (x1)	
J1B1	PCI 32-bit/33 MHz	The CRB provides one PCI slot that is *PCI Local Bus Specification*, Rev. 2.3 compliant. • 120 MB/s throughput

Warning: PCI Hot Plug* is *not* supported on this CRB.

1.5.4 Rear Panel I/O Connectors

Table 10 below shows the rear panel I/O connectors indicated in Figure 2 on page 11.

Table 10. Rear Panel I/O Connectors

Ref Des Location	Description	
J7A1	USB* Ports 0 and 1 Connector	Each of the two rear panel connectors provides two dual-stacked USB* 2.0 ports. In conjunction with the on-board USB* Ports there are a total of eight USB* ports. Two USB* modes: • UHCI • EHCI Refer to the *Intel® I/O Controller Hub 9 (ICH9) Family Datasheet* for details on USB* operating modes.
J6A1	USB* Ports 2 and 3 Connector	
	RJ-45 LAN Connector	Provides standard 10/100/1000 ethernet connection. NOTE: This is a stacked connector that also provides two LED indicators and two USB* ports.
J5A1	VGA Connector	The rear panel has one VGA connector for the on-board Silicon Motion* video controller. • 15-pin male D-sub connector • VGA port can be disabled
J9A1	PS/2* Keyboard and Mouse Connectors	The rear panel provides two stacked circular DIN PS/2* connectors. Turn off power before a keyboard or mouse is connected or disconnected. • Keyboard connector on bottom (nearest board) • Mouse connector on top
J9A2	Serial COM Port Connector	The rear panel provides a serial COM1 port. • RS232E 9-pin male D-sub connector
J7A2	Parallel Port Connector	The rear panel provides one parallel port. • 25-pin female D-sub connector (located above COM port)

1.5.5 On-board Power Connections

Table 11 below shows the on-board power connectors indicated in Figure 2 on page 11.

Table 11. On-board Power Connections

Ref Des Location	Description	
J4K1	SSI 8-pin Power Connector	Provides 12 V (+12V1) voltages from the external power supply that feed the Intel® MVP-6 regulator. See "8-pin Processor Power Connector Pins (Top-View)" for connector pin out.
J1K4	SSI 24-pin Power Connector	Provides 12 V (+12V2), -12 V, 5 V, 3.3 V, 5 VSB voltages from the external power supply. See "24-pin Main Power Connector Pins (Top-View)" for connector pin out.
J3K1	SSI 4-pin Power Connector	Provides 12 V (+12V2) voltage from the external power supply. See "4-pin +12 V Power Connector Pins (Top-View)" for connector pin out.

Note: These power connectors comply with the *Server System Infrastructure (SSI) Specification for Rack-Optimized Servers* Version 2.11.

1.6 Hardware Server Management Features

The CRB provides server management features like temperature, voltage, and fan tachometer monitoring. It also provides control for overall protection of the platform.

1.6.1 Voltage Monitoring

The CRB uses the SuperI/O* to monitor the following voltages:

- CPU core voltage (CPUVCC)
- MCH core voltage 1.5 V (1_5V)
- DDR2 core voltage 1.8 V (P1V8)

1.6.2 Temperature and Fan Tachometer Monitoring

The CRB uses the SMSC* SCH5027 device to monitor the following die temperatures and corresponding fan tachometers:

- Intel® Core™2 Duo Processor T9400
- Intel® 5100 MCH Chipset.

1.6.3 Watch Dog Timer (WDT)

The Watch Dog Timer (WDT) provides output to a red LED indicator (CR2J1) and optionally to the System Reset circuitry. Refer to jumper J2J2 description for more details.

1.6.4 Sleep States and Soft Off

ACPI 1.0, 2.0, 3.0 APM compliant.

- S0, S3, S4, and S5 sleep states
- Soft off capability (S5)
  - — Operating system dependent
  - — Requires a complete OS boot when the system wakes

1.6.5 Wake Events

- Power switch

1.6.6 Hardware Clock Throttling

- Provides support for hardware clock throttling through STPCLK#

1.6.7 Fan Power Connection

- One processor fan connector (CPU)
- One fan for Intel® 5100 MCH Chipset (MCH)
- Two auxiliary fan connectors (AUX0 / AUX1)

1.6.8 On Board Switches

The CRB has the following momentary push button switches to provide state control:

- Power

- Reset
- Wake (this button is not functional)

1.7 Supported Operating Systems

The CRB is validated with the following operating systems:

- MS-DOS*
  - — BIOS supports the installation and booting of the MS-DOS* 6.22 operating system
- QNX*
- Microsoft Windows XP SP2*
- Microsoft Windows XP SP2 x64*
- Microsoft Windows Vista*
- Microsoft Windows Server 2003 R2 Enterprise Edition*
- Microsoft Windows Server 2003 R2 Enterprise Edition x64*
- Wind River* VxWorks*
- Microsoft Windows* Longhorn
- Linux* Fedora* Core 6
- Red Hat* Enterprise Linux* 5 Advanced Server (IA-32)
- Red Hat* Enterprise Linux* 5 Advanced Server (Intel® 64)
- SUSE* Linux* Enterprise 10
- Solaris* 5.1

Note: Operating systems are to be purchased by the customer and are not distributed with this Development Kit.

1.8 Supported BIOS Features

The BIOS has an AMI* core with the following components:

Table 12. Supported BIOS Features (Sheet 1 of 2)

Name of BIOS component	Description
PCI 2.3	The BIOS is *PCI Local Bus Specification*, Rev. 2.3 compliant.
LAN boot	The BIOS supports booting from a plug in Ethernet device, if present.
Serial ATA boot	The BIOS supports booting from a Serial ATA hard drive.
CD-ROM boot	The BIOS supports booting from a Serial ATA CD-ROM.
USB* boot	The BIOS supports booting from a USB* boot device.
Floppy boot	The BIOS supports booting from a floppy drive
PCI Express*	The BIOS initializes and supports PCI Express* cards that are plugged into the CRB.
USB*	The BIOS supports the USB* 1.1 and USB* 2.0 interfaces.
CMOS Header	The BIOS supports recognizing the clear CMOS header.
ECC support	The BIOS detects and supports ECC memory.

Table 12. Supported BIOS Features (Sheet 2 of 2)

Name of BIOS component	Description
Watchdog Timer (WDT)	The BIOS provides watch dog timer support.
APIC and ACPI Control	The ability to enable and disable APIC and ACPI is present in the BIOS. Control is also required for OS plug-and-play features. The BIOS supports the following ACPI states: • G0 (S0) - Working • G1 (S3) - Sleeping [Suspend to RAM] • G2 (S5) - Soft Off The BIOS supports C0, C1, C1E and C2 states.
Patch Update Mechanism	The Patch Update Mechanism is used to upgrade and/or install micro-code patches into BIOS is supported.

1.8.1 ACPI

ACPI gives the OS direct control over the power management and plug-and-play functions of the platform. The use of ACPI with this CRB requires an OS that provides full ACPI support.

Table 13. Effects of Pressing the Power Switch

If the System is in this state...	...and the power switch is pressed for	...the system enters this state
Off (ACPI G2/G5 - soft off)	Less than four second	Power-on (ACPI G0 - working state)
On (ACPI G0 - working state)	Less than four seconds	Soft-off/Standby (ACPI G1 - sleeping state)
On (ACPI G0 - working state)	More than four seconds	Fail Safe Power-off (ACPI G2/G5 - soft off)
Sleep (ACPI G1 - sleeping state)	Less than four seconds	Wake-up (ACPI G0 - working state)
Sleep (ACPI G1 - sleeping state)	More than four seconds	Power-off (ACPI G2/G5 - soft off)

1.8.1.1 System States and Power States

Under ACPI, the OS directs all system and device power state transitions by managing devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The OS uses information from applications and user settings to put the system as a whole into a low-power state.

1.9 Thermal and Mechanical Components

Table 14. Thermal and Mechanical Components

Name	Description
Standard Processor Thermal Solution Mounting	The CRB supports full power processor thermal solution mounting provisions as delineated in the processor's Thermal/Mechanical Design Guidelines.
Processor Fan	The CRB provides fan headers for the processors that includes 12V with tachometer.
Intel® 5100 MCH Chipset Heatsink	The CRB supports the Intel® 5100 MCH Chipset heatsink mounting requirements.
Active Intel® 5100 MCH Chipset Heatsink	The CRB provides mounting provisions and a fan header for an active Intel® 5100 MCH Chipset thermal solution.
Power Measurement	The CRB provides a means for power measurement for the following components: • Processor • Intel® 5100 MCH Chipset • DDR2
Fan Headers	The CRB provides four fan headers.
Solder Down Anchors	The CRB provides solder down anchors for the Intel® 5100 MCH Chipset and ICH9R. The Intel® 5100 MCH Chipset includes active heatsink mounting holes.

1.9.1 Heatsinks

The processor and Intel® 5100 MCH Chipset use an active heatsink design with a built-in fan, and the Intel® 82801IR I/O Controller Hub (ICH9R) uses a passive heatsink. The active heatsink is powered by the platform. For details on the processor and MCH heatsink, please refer to the appropriate Thermal/Mechanical Design Guidelines. The ICH9R's passive heatsink requires no power.

1.9.2 Physical and Mechanical Board Specifications

The size of the Development Kit's CRB is approximately 12.0 inches long by 13.0 inches wide. The CRB provides non-plated mounting holes with top and bottom ground rings. The CRB mounting holes should align with most standoffs in a standard SSI chassis.

1.10 Debug Ports

The CRB provides an XDP header (J1T2) that can be used to debug the processor. An optional XDP header (J6L1), not installed, can be used to debug the Intel® 5100 MCH Chipset.

1.11 Real Time Clock (RTC), CMOS SRAM, and Battery

A coin-cell battery (XB3J1 type CR2032) powers the real time clock (RTC) and CMOS memory. The battery has an estimated life of three years when it is not plugged into a wall socket. When the platform is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

Note: If the battery and AC power fail, at boot-up the system will prompt you to either load optimized defaults or enter BIOS and manually adjust your BIOS settings.

2.0 Platform Setup

Caution: The following precautions will help promote safe and proper operation of the Customer Reference Board (CRB):

- Before connecting power, make sure that the CRB is mounted either in a chassis or on the provided acrylic stand to avoid accidental shorts.
- The CRB is susceptible to damage by electrostatic discharge (ESD) that may result in platform failure or unpredictable operation. Make sure you are in a static-free work environment before removing components from their anti-static packaging.
- Connecting the wrong cable, or reversing a cable, may damage the CRB or device being connected. Since the CRB is not in a protective chassis, use proper care when connecting cables to the platform.

Note: The CRB comes with all jumpers correctly set and will be ready to boot.

2.1 Processor Installation

Figure 3 shows a µFCPGA-479M socket and a properly aligned processor package.

Figure 3. µFCPGA-479M Socket and Processor Pin A1 Alignment (Top View)

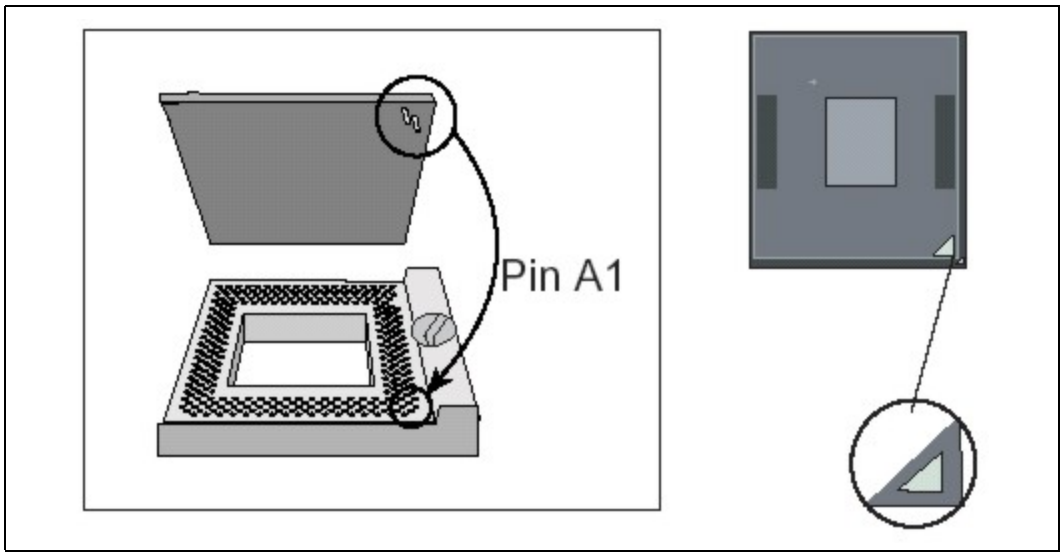
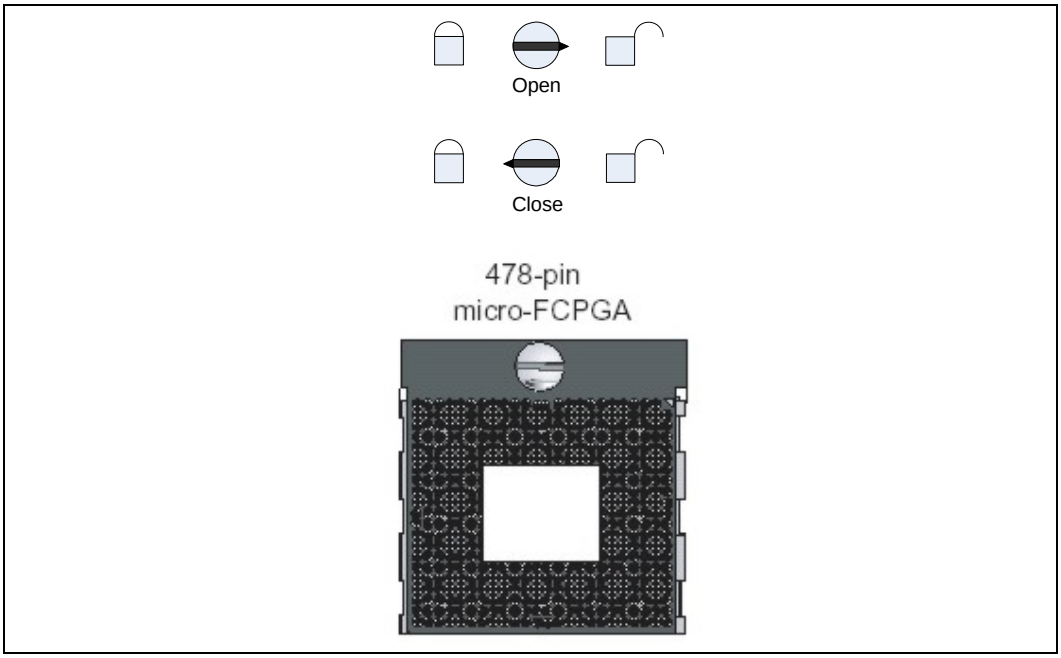


Figure 4. µFCPGA-479M Socket Actuator (Top View)



1. Align the processor's pin A1 with the arrow on the µFCPGA-479M. The processor's pin A1 is identified with an embroidered corner, and the socket's pin A1 is identified with a small arrow (Figure 3).
2. If the processor does not drop completely into the socket, turn the actuator to the Open position or until the processor drops completely in (Figure 4).

Note: You should *not* have to press down on the processor. Do *not* force the processor into the socket as it may cause damage to the package, socket, or electrical contacts.

3. While gently holding the processor down, secure the processor in the socket by turning the socket actuator to the Close position (Figure 4).
4. For more detail on the µFCPGA-479M socket or processor package, refer to related content on http://www.intel.com/. Example references include the *Intel® Mobile Processor Micro-FCPGA Socket (mPGA479M) Design Guidelines* and the *Intel® Core™2 Duo Processors and Intel® Core™2 Extreme Processors on 45-nm Process Datasheet*.

2.1.1 Attaching Heatsinks and Fans

1. The heatsinks for the Intel® 5100 MCH Chipset and the ICH9R should already be installed on the CRB.
2. For the processor, Thermal Interface Material (TIM) should be pre-applied to the Common Enabling Kit (CEK) heatsink solution. It will appear like a dry gray material located in the center position under the heatsink solution. If the heatsink solution is removed after the system is booted it will be necessary to clean the old thermal interface material off and replace it with a new TIM pad or thermal grease. Contact Intel Customer Support to get replacement TIM pads or grease.
3. Install the CEK heatsink over the processor that has been inserted in an µFCPGA-479M socket. The heatsink mounting screws should already have CEK springs pre-installed on the screws. It is recommended to start each screw then tighten them down in a crisscross pattern.

Caution: Align heatsink solution carefully and avoid over tightening. Over tightening can result in damage to the processor, heatsink, chassis, and/or the CRB.

4. Plug CPU fans into the appropriate 3-wire connectors on the CRB. The fan for the CPU connects to the "J9H1 CPU Fan Connector" on page 11.

Note: Fans should be installed so that airflow is directed down into the processors.

2.2 Memory Module Plug-In

Note: Refer to Section 1.4 for memory specific information and refer to "240-pin DDR2 Module Sockets" on page 11 for DIMM locations while reading below steps.

1. Beginning with Channel 0 - DIMM 1, (the DIMM connector closest to the edge of the CRB, furthest from the Intel® 5100 MCH Chipset) line up the DIMM with the slot and make sure that the end clips are moved outward to the open position.
2. Gently push the DIMM into the socket until you hear or feel the side clips lock into the side of the DIMMs.

Continue adding memory to the system sequentially starting from Channel 0 - DIMM 1 to Channel 1 - DIMM 2 in accordance with Table 6, "DDR2-533/667 MHz DIMM Population Guidelines" on page 13.

2.3 Peripheral Set-Up

2.3.1 Connect SATA cables

There are six Serial ATA (SATA) connectors on the CRB. Connect the cables to the appropriate drive sequentially starting from SATA Port 0 through Port 5. These six keyed connectors are located in board coordinate area 3F to 4H (see "SATA Connectors" on page 11). Intel recommends using SATA Port 0 as the boot drive.

2.3.2 Expansion Connectors

1. If necessary, connect PCI Express* add-in cards into the appropriate Port A through Port E PCI Express* slots. These five PCI Express*slots are located in board coordinate area 1B to 4C (see "PCI Express* Slots" on page 11).

Note: All of the PCI Express* connectors on this CRB are physical x8 connectors, Port A, B, and C utilize actual x8 link widths but Port D is only x4 and Port E is only x1.

2. Connect your PCI Cards into the PCI 32/33 slot located in area 1B through 1D.

2.3.3 Rear Panel Connectors

1. Connect a USB* or PS/2* keyboard and/or mouse to the rear panel connectors (see "Rear Panel I/O" on page 11).
2. If you are using the on-board video, connect the monitor to the 15-pin VGA rear panel connector.

2.4 Connect Power

1. Insert the main 24-pin baseboard power plug into the motherboard's J1K4 SSI 24-pin Power Connector making sure that the plug clip lines up with the clip lock and the connector pins fit easily into their appropriate slots.

2. Insert the 8-pin processor power plug into the motherboard's J4K1 SSI 8-pin Power Connector.
3. Insert the 4-pin baseboard power plug into the motherboard's J3K1 SSI 4-pin Power Connector.

Caution: Do *not* force the power plugs into the connectors; they should go in easily when plugged in correctly. Plugging them in incorrectly will result in severe damage to the CRB.

4. Plug in any remaining peripheral power connectors (e.g., for hard drives and disc drives).
5. Plug the AC power cable into the back of the power supply and *plug the cord into the wall once the board is setup*.

2.5 Turning On and Resetting the Board

There are two momentary push buttons on the CRB. One push button is the power-on button labeled "PWR" (see "SW2J1 Power Button" on page 11), and the other button is the reset button labeled "RESET" (see "SW2J2 Reset Button" on page 11).

Note: The power button is also used to wake a system that is in a sleep state.

Note: Refer to "J1J2 Front Panel Header" on page 11 for information on case buttons and LEDs.

3.0 Technical Reference

3.1 CMOS Battery and Memory

3.1.1 CMOS Battery Replacement

With the board shut down but power supply still connected, remove the 3 V coin battery (CR2032) and replace with a new battery, see "XB3J1 Battery" on page 11.

Warning: There is a risk of explosion if the lithium battery is replaced by an incorrect type. Dispose of used batteries according to the vendor's instructions.

Note: CMOS batteries rarely go bad, but a good indication of a bad battery is when you have to restore your BIOS settings and system time after unplugging the system and plugging it in again. This occurs every time power is removed from the power supply.

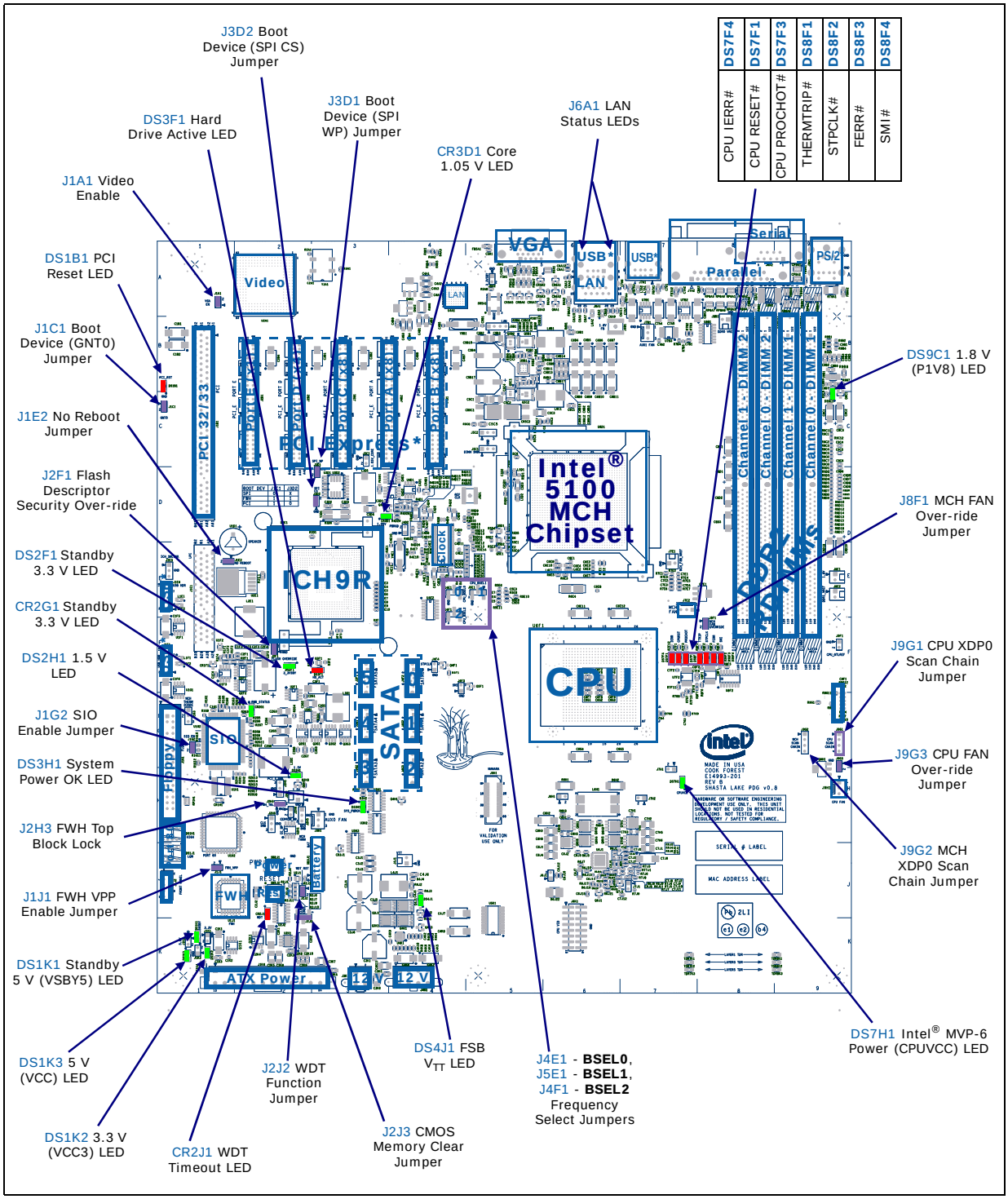
3.1.2 Clearing CMOS Memory

1. With system shutdown, unplug the power supply and/or switch the power supply to the off position (no power to board).
2. Remove jumper J2J3 from pins 1 and 2 and place it on pins 2 and 3, see "J2J3 CMOS Memory Clear Jumper" on page 25.
3. Leave the jumper in place for approximately a minute.
4. Remove the jumper from pins 2 and 3 and place it back on pins 1 and 2.

Tip: If the CMOS did not clear at this point, make sure power is removed from platform and leave the jumper on pins 2 and 3 for a longer duration to assure CMOS is cleared. The board should bring up a setup prompt before booting to either go with defaults or enter BIOS.

3.2 Board Details

Figure 5. Detailed Component Layout Reference



3.2.1 Configurable Jumper Settings

Warning: Do not move jumpers when the power is on. Always turn off the power and unplug the power cord before changing a jumper setting. Otherwise, the CRB may be damaged.

Table 15 provides details on the CRB's configurable jumper settings.

Table 15. Configurable Settings (Sheet 1 of 2)

<table>
<tr><th>Ref Des Location</th><th>Jumper Setting</th><th>Description†</th></tr>
<tr><td>J4E1</td><td>BSEL0 Select
(3-pin)</td><td rowspan="3">FSB Frequency Select Jumpers (short pin numbers as indicated):
<table><tr><th>BSEL2 (J4F1)</th><th>BSEL1 (J5E1)</th><th>BSEL0 (J4E1)</th><th>Configuration</th></tr><tr><td>2–3</td><td>2–3</td><td>2–3</td><td>266 MHz</td></tr><tr><td>1–2</td><td>1–2</td><td>1–2</td><td>CPU SELECT (default)</td></tr></table>Note: All other jumper configuration settings are RESERVED.</td></tr>
<tr><td>J5E1</td><td>BSEL1 Select
(3-pin)</td></tr>
<tr><td>J4F1</td><td>BSEL2 Select
(3-pin)</td></tr>
<tr><td>J9G1</td><td>CPU XDP0 Scan Chain Isolation
(4-pin)</td><td>Include or remove CPU from XDP0 scan chain:
• 1-2 and 3-4: CPU included (default)
• 2-3: CPU removed
Note: For other options refer to Appendix B, “External Debug Port Signal Overview”.</td></tr>
<tr><td>J9G2</td><td>MCH XDP0 Scan Chain Isolation
(4-pin)</td><td>Include or remove MCH from XDP0 scan chain:
• 1-2 and 3-4: MCH included (default)
• 2-3: MCH removed
Note: For other options refer to Appendix B, “External Debug Port Signal Overview”.</td></tr>
<tr><td>J2J3</td><td>CMOS Clear
(3-pin)</td><td>Clear Battery-backed CMOS Memory:
• 1–2: Normal (default)
• 2–3: Clear CMOS</td></tr>
<tr><td>J1A1</td><td>Video Enable
(2-pin)</td><td>Enable On-board Video:
• 1–2: VGA Enabled (default)
• OPEN: VGA Disabled
Note: A parallel 0 Ω resistor (R9L14) can force permanent enabled condition (this site is unpopulated by default).</td></tr>
<tr><td>J1E2</td><td>No Reboot Jumper</td><td><table><tr><th colspan="2">J1E2 (No Reboot)</th></tr><tr><td>Short</td><td>No Reboot</td></tr><tr><td>Open</td><td>Normal</td></tr></table></td></tr>
<tr><td>J1G2</td><td>SIO Enable Jumper
(2-pin)</td><td>Enable SuperI/O*:
• 1–2: SIO Enabled (default)
• OPEN: SIO Disabled
Note:
1. A parallel 0 Ω resistor (R1G10) can force permanent enabled condition (this resistor is unpopulated by default).
2. SIO disabled by removing its LPC Frame signal.</td></tr>
<tr><td>J1C1</td><td rowspan="2">Boot Device Selection
(Two 2-pin headers)</td><td rowspan="2">Select system boot device:
<table><tr><th>GNT0 (J1C1)</th><th>SPI_CS (J3D2)</th><th>Configuration</th></tr><tr><td>1–2</td><td>x</td><td>SPI Flash Device</td></tr><tr><td>OPEN</td><td>OPEN</td><td>Firmware Hub (FWH) Device (default)</td></tr><tr><td>OPEN</td><td>1–2</td><td>PCI Device</td></tr></table></td></tr>
<tr><td>J3D2</td></tr>
</table>

† Make selection by shorting only the indicated jumper pin numbers. The CRB silk-screen indicates pin 1 on the headers with an arrow ▲.

Table 15. Configurable Settings (Sheet 2 of 2)

Ref Des Location	Jumper Setting	Description†
J3D1	SPI Flash Write Protect (2-pin)	Enable SPI Flash Write Protect: • 1–2: Write Protect Enabled • OPEN: Write Protect Disabled *(default)*
J1J1	FWH VPP Enable Jumper (2-pin)	Enable Firmware Hub Programming Voltage: • 1–2: Erase/Program Enabled *(default)* • OPEN: Erase/Program Disabled
J2H3	FWH Top Block Lock Jumper (2-pin)	Lock the Top 64 kB Block of Memory in the Firmware Hub device: • 1–2: Locked • OPEN: Unlocked *(default)*
J2J2	WDT Function Jumper (2-pin)	Sets Watch Dog Timer Function after Timeout: • 1–2: WDT Triggers Reset and LED (CR2J1) • OPEN: WDT Triggers LED Only *(default)*
J9G3	CPU Fan Speed Over-ride (2-pin)	CPU Fan Operation: • 1–2: Fan Speed Full *(default)* • OPEN: Fan Speed Controlled by U1G2 (SMSC* SCH5027) PWM
J8F1	MCH Fan Speed Over-ride (2-pin)	MCH Fan Operation: • 1–2: Fan Speed Full *(default)* • OPEN: Fan Speed Controlled by U1G2 (SMSC* SCH5027) PWM
J2F1	Flash Descriptor Security Over-ride Strap (2-pin)	ICH9R Flash Descriptor Security: • 1-2: Flash Descriptor Security is over-ridden • OPEN: Security measures defined in the Flash Descriptor are in effect *(default)*

† Make selection by shorting only the indicated jumper pin numbers. The CRB silk-screen indicates pin 1 on the headers with an arrow ▲.

3.2.2 LED Indicators

Table 16 provides details on the CRB's LED indicators.

Table 16. LED Indicators (Sheet 1 of 2)

Ref Des Location	LED Display Status	Description (LED "ON" State)†
DS1K3	5 V Voltage	VCC is powered.
DS1K1	5 V Standby Voltage	VSBY5 is powered.
DS1K2	3.3 V Voltage	VCC3 is powered.
CR2G1	3.3 V Standby Voltage	VSBY3_3 is powered.
DS2F1	3.3 V Standby Voltage	VSBY3_3 is powered *(VSBY5 must also be powered)*.
DS9C1	1.8 V Voltage	P1V8 is powered *(VSBY5 must also be powered)*.
DS2H1	1.5 V Voltage	1_5V is powered *(VCC must also be powered)*.
DS7H1	Intel® MVP-6 Voltage	CPUVCC is powered *(VCC3 must also be powered)*.
DS4J1	V_{TT} Voltage	P_VTT FSB termination voltage is powered *(VCC3 must also be powered)*.
CR3D1	1.05 V Core Voltage	V_1P05_CORE is powered *(VCC must also be powered)*.
DS3H1	System Power OK	SYS_PWR_OK_DELAY signal is active
DS1B1	PCI Reset	PCIRST signal is active *(red)*.
CR2J1	WDT Timeout	Watch Dog Timer timeout (SIO_WDT_TOUT) is active *(red)*.

† The LED color is green unless specifically noted otherwise.

Table 16. LED Indicators (Sheet 2 of 2)

<table>
<tr><th>Ref Des Location</th><th>LED Display Status</th><th>Description (LED “ON” State)†</th></tr>
<tr><td>DS3F1</td><td>Hard Drive Active</td><td>HD_ACT_LED signal is active (red).</td></tr>
<tr><td>J6A1</td><td>LAN Link Status
(Left Green LED)

LAN Rate Status
(Right Green/Yellow LED)</td><td>LAN Link and Activity Indication:
<table>
<tr><th>LED</th><th>State</th><th>Condition</th></tr>
<tr><td rowspan="3">Left</td><td>Off</td><td>LAN link is not established.</td></tr>
<tr><td>On - Green</td><td>LAN link is established.</td></tr>
<tr><td>Blinking - Green</td><td>LAN activity is occurring.</td></tr>
<tr><td rowspan="3">Right</td><td>Off</td><td>10 Mb/s data rate</td></tr>
<tr><td>On - Green</td><td>100 Mb/s data rate</td></tr>
<tr><td>On - Yellow</td><td>1000 Mb/s data rate</td></tr>
</table>
Note: Both LEDs are physically located in the J6A1 RJ-45 connector housing.</td></tr>
<tr><td>DS7F4</td><td>CPU IERR#</td><td>CPU Internal Error output signal is active (red).</td></tr>
<tr><td>DS7F1</td><td>CPU RESET#</td><td>CPU Reset input signal (FSB0_CPURST) is active (red).</td></tr>
<tr><td>DS7F3</td><td>CPU PROCHOT#</td><td>CPU Processor Hot output signal is active (red).</td></tr>
<tr><td>DS8F1</td><td>THERMTRIP#</td><td>The CPU’s Thermal Trip output signal is active (red).</td></tr>
<tr><td>DS8F2</td><td>STPCLK#</td><td>The CPU’s Stop Clock input signal is asserted (red).</td></tr>
<tr><td>DS8F3</td><td>FERR#</td><td>The CPU’s Floating-point Error/Pending Break Event output signal is asserted (red).</td></tr>
<tr><td>DS8F4</td><td>SMI#</td><td>The CPU’s System Management Interrupt input signal is asserted (red).</td></tr>
</table>

† The LED color is green unless specifically noted otherwise.

3.3 Connectors

Warning: Only the following connectors have over-current protection: back panel USB*, front panel USB*, and PS/2* connector.

The other internal connectors are not over-current protected and should connect only to devices that go inside a computer’s chassis, such as fans and internal peripherals. Do not use these connectors to power devices that are external to a computer’s chassis. A fault in the load presented by the external devices can damage the computer, the power cable, and the external devices. This section describes the connectors.

3.3.1 Fan Connectors

For fan connector location details see “On-board I/O Connections” on page 14”.

Table 17. 3-Wire Fan Connectors (CPU, MCH, AUX0, and AUX1)

Pin	Signal Name
1	GND[1]
2	+12 V
3	Tach

Notes:
1. Optional fan speed control signal if Fan Over-ride Jumper is removed

3.3.2 Power Supply Connectors

The CRB has three power supply connectors. The main 24-pin power connector, the 8-pin processor power connector, and an additional 4-pin +12 V power connector. The power supply connectors conform to the SSI EPS12V specification.

Table 18. 24-pin Main Power Connector Pins (Top-View)

Signal Name	Pin		Signal Name
+3.3 V	13	1	+3.3 V
-12 V	14	2	+3.3 V
GND	15	3	GND
PS_ON	16	4	+5 V
GND	17	5	GND
GND	18	6	+5 V
GND	19	7	GND
RSVD	20	8	PWR_OK
+5 V	21	9	+5 V Standby (5VSB)
+5 V	22	10	+12 V (+12V2)
+5 V	23	11	+12 V (+12V2)
GND	24	12	+3.3 V

Table 19. 8-pin Processor Power Connector Pins (Top-View)

Signal Name	Pin		Signal Name
+12 V (+12V1)	5	1	GND
+12 V (+12V1)	6	2	GND
+12 V (+12V1)	7	3	GND
+12 V (+12V1)	8	4	GND

Table 20. 4-pin +12 V Power Connector Pins (Top-View)

Signal Name	Pin		Signal Name
+12 V (+12V2)	3	1	GND
+12 V (+12V2)	4	2	GND

3.3.3 Front Panel Connector

This section describes the functions of the front panel connector. Table 21 lists the signal names and descriptions on the front panel connector.

Table 21. 9-pin Front Panel Connector Pins (Top-View)

Description	Signal Name	Pin		Signal Name	Description
HDD Activity LED Anode	FP_PU1	1	2	HD_ACT_LED_N	HDD Activity LED Cathode
Power LED Anode	FP_PU2	3	4	FRNTPNL_PWR_LED	Power LED Cathode
Power Button Pin 1	FP_PD1	5	6	FP_PWR_BTN_N	Power Button Pin 2
Reset Button Pin 1	FP_RST_BTN_N	7	8	FP_PD2	Reset Button Pin 2
Ground	GND	9	10	N/A	

3.4 Memory Resources

Detailed memory information for addressable memory and memory maps can be found in the *Intel® 5100 Memory Controller Hub Chipset Datasheet*.

3.5 Interrupts

Interrupts can be routed through the I/O xAPIC and supports a total of 24 interrupts. The I/O xAPIC is supported by Microsoft Windows XP*. Table 22 provides the interrupts and their correlating functions.

Table 22. I/O xAPIC Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade input from slave PIC
3	User available
4	COM1[1]
5	User available
6	Diskette drive
7	LPT1[1]
8	Real-time clock
9	User available
10	User available
11	User available
12	On-board mouse port (if present, else available)
13	Reserved, math coprocessor
14	Primary Serial ATA
15	Secondary Serial ATA
16	User available (through PIRQA)[2]
17	User available (through PIRQB)[2]
18	User available (through PIRQC)[2]
19	User available (through PIRQD)[2]
20	User available (through PIRQE)[2]
21	User available (through PIRQF)[2]
22	User available (through PIRQG)[2]
23	User available (through PIRQH)[2]

Notes:
1. Default but can be changed to another IRQ.
2. Available in APIC mode only.

3.6 PCI Conventional Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI Conventional bus connectors and on-board PCI Conventional devices. The *PCI Local Bus Specification*, Rev. 2.3 describes how interrupts can be shared

between devices attached to the PCI Conventional bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI Conventional device should not share an interrupt with other PCI Conventional devices. Use the following information to avoid sharing an interrupt with a PCI Conventional add-in card.

Table 23. PCI Interrupt Routing Map PCI Interrupt Source

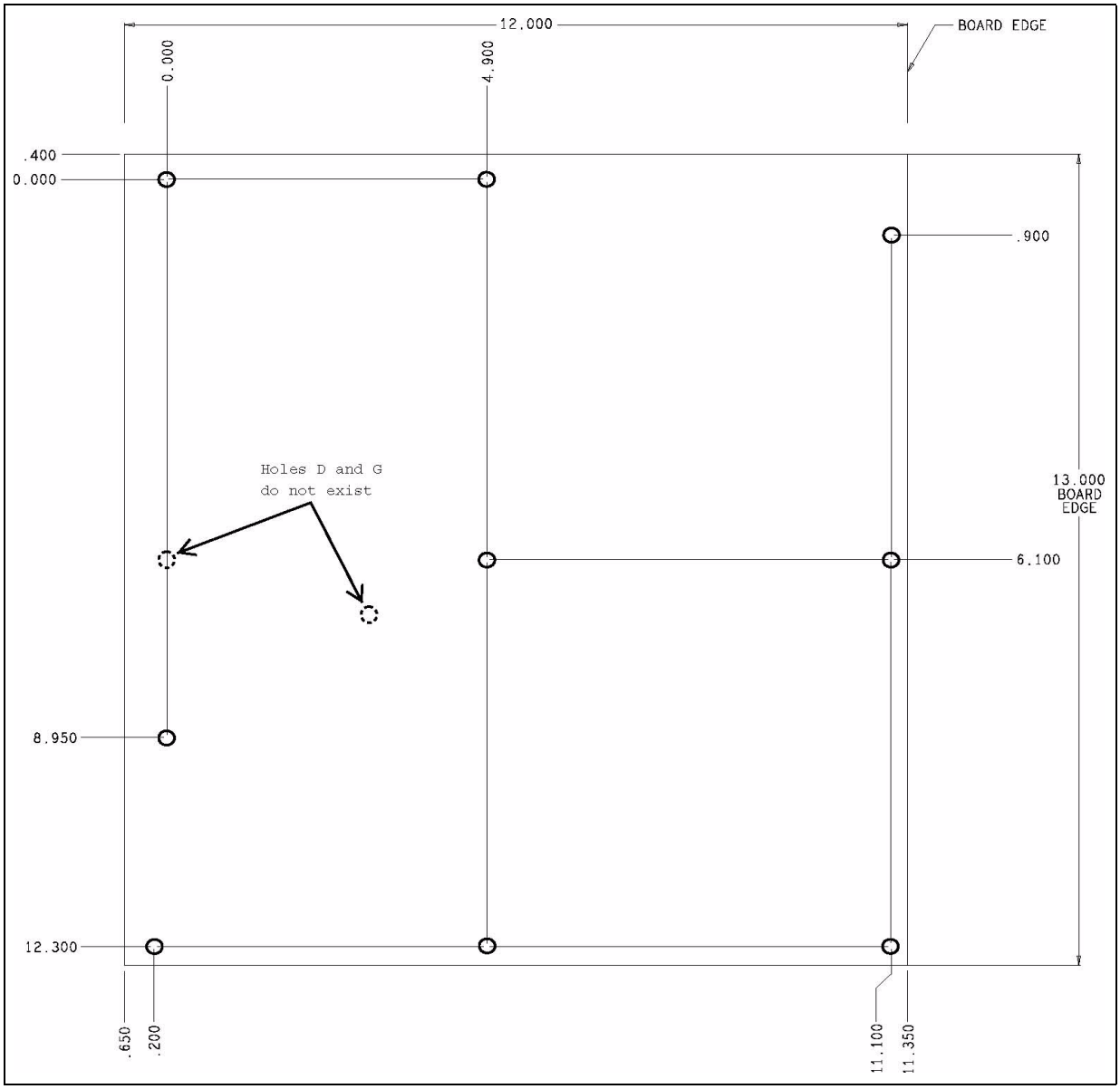
	Intel® 5100 MCH Chipset PIRQ Signal Name			
	PIRQA#	PIRQB#	PIRQC#	PIRQD#
PCI bus connector 1	INTA	INTB	INTC	INTD

3.7 Mechanical Considerations

3.7.1 Form Factor

The CRB fits a form factor similar to the Extended ATX specification. Figure 6 illustrates the mechanical form factor for the CRB. Dimensions are given in inches. The outer dimensions are 12.0 inches by 13.0 inches. The location of the I/O connectors and mounting holes do not necessarily correlate with the specification.

Figure 6. Form Factor



4.0 Overview of BIOS Features

4.1 Introduction

The BIOS is stored in the Firmware Hub (FWH) and can be updated manually or by using a BIOS flash programming tool. If SPI flash programming is necessary, contact your Intel sales representative about the SPI programming guide for ICH9R.

4.1.1 Updating the BIOS by Manually Reprogramming

In order to change the BIOS FWH chip, see "U1J1 Firmware Hub" on page 11, without damaging the pins, use an EPROM chip removal tool. Remove the BIOS chip by inserting the pinchers of the tool in each open corner of the socket, close the pinchers around the chip, and pull the chip out carefully. Use a standard off-the-shelf EPROM programming tool to update the firmware, and reinsert the chip making sure to properly align the package prior to gently pressing it into place.

4.1.2 Updating the BIOS with a Flash Programming Tool

The user is able to update the BIOS image on the Intel® Core™2 Duo Processor T9400 and Intel® 5100 Memory Controller Hub Chipset CRB with a utility called AFUDOS which is a DOS utility.

1. Create a DOS bootable USB* thumb drive in order to update the BIOS via this DOS utility. This link gives instructions on how to create the bootable DOS thumb drive: http://www.thepcspy.com/read/bootable_usb_flash_drive.
2. Install the ROM burner application from American Megatrends Inc. (AMI) which is called "AFUDOS.EXE." Here is the link for the DOS update utility from AMI called AFUDOS: http://www.ami.com/support/bios.cfm.
3. Copy both AFUDOS.EXE and the new BIOS ROM image onto the DOS bootable USB* drive.
4. Once you have booted the platform from the USB* thumb drive, update the BIOS image with the following command (the usage for this application is):
   `AFUDOS /ifilename.rom /pbnc`

4.2 Overview

The BIOS displays a message during POST identifying the type of BIOS and a revision code.

The BIOS Setup program can be used to view and change the BIOS settings for the CRB. The BIOS Setup program is accessed by pressing the <DELETE> key after the POST test and memory test begin and before the operating system begins to boot. The menu bar is shown in Figure 7.

Figure 7. Menu Bar

```
<MAIN> - <ADVANCED> - <PCIPnP> - <BOOT> - <SECURITY> - <CHIPSET>-<EXIT>
```

Table 24 lists the BIOS Setup program menu features.

Table 24. BIOS Setup Program Menu Bar

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit
Displays processor and memory configurations	Configures advanced features and settings	Sets up PCI and PCI Express*	Selects boot options and configurations	Sets passwords and security features	Configures different major components	Saves or discards changes to setup program options

Table 25. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
< or >	Selects a different menu screen (moves the cursor left or right)
^ or v	Selects an item (moves the cursor up or down)
Enter	Executes command or selects the submenu
F9	Load the optimal default configuration values for the current menu
F7	Discard changes
F8	Load fail safe defaults
F10	Save the current values and exits the BIOS Setup program
ESC	Exits the menu

4.3 Resource Configuration

4.3.1 PCI Auto-configuration

The BIOS automatically configures PCI devices. Currently on the CRB, there is a 32/33 PCI add-in card socket. Auto-configuration lets a user insert or remove PCI cards without having to manually configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to AVAILABLE in setup are considered to be available for use by the add-in card.

4.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI)-compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor clock frequency
- Dynamic data, such as event detection and error logging

4.5 Legacy USB* Support

Legacy USB* support enables USB* devices to be used even when the operating system's USB* drivers are not yet available. Legacy USB* support is used to access the BIOS Setup program and to install an operating system that supports USB*.

Legacy USB* support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB* support is enabled by the BIOS allowing you to use a USB* keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB* keyboards and mice are recognized and may be used to configure the operating system.

After the operating system loads the USB* drivers, all legacy and non-legacy USB* devices are recognized by the operating system, and legacy USB* support from the BIOS is no longer used.

To install an operating system that supports USB*, follow the operating system's installation instructions.

4.6 Language Support

The BIOS Setup program and help messages are supported in US English.

4.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, USB* device, or a network. The default setting is for the floppy to be the first and the hard drive to be the second.

4.7.1 CD-ROM Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system attempts to boot from the next defined drive. Refer to Section 4.7.4, "Changing the Boot Device" on page 36 for how to change this setting.

4.7.2 Network Boot

A network can be selected as a boot device using the on-board gigabit NIC or using a network add-in card plugged into a PCI slot. This selection allows booting from a network add-in card with a remote boot ROM installed.

In order to boot from the LAN, enter the BIOS, and select LAN boot as your first boot device. Refer to Section 4.7.4, "Changing the Boot Device" on page 36 for how to change this setting.

4.7.3 USB* Boot

In order to boot from a USB* device, enter the BIOS, and select USB* boot as your first boot device. The USB* device should be set as the first priority device under Removable devices, and the USB* device should be selected as the priority device in the Boot Priority menu.

Note: Have the USB* device plugged in when changing this BIOS setting.

4.7.4 Changing the Boot Device

Pressing the <DELETE> key during POST causes the BIOS menu to be displayed. Using your arrow keys, move over to <BOOT>, and then arrow down to <Boot Device Priority>, and then select which device you would like to boot first and second.

Note: Please follow the instructions on the right side of the BIOS screen to navigate and change BIOS settings.

4.8 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt is displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A–Z, a–z, and 0–9. Passwords may be up to 16 characters in length.

Appendix A Error Messages and Beep Codes

This appendix describes the various progress codes that are reported by the BIOS and the corresponding LED codes.

The LED codes are 8-bit quantities and can be used as Port 80 codes if the platform supports a Port 80 capturing device. The higher nibble alone is used for a 4-bit LED.

A.1 Speakers

The CRB-mounted speaker provides audible error message (beep code) information during POST. The location of the on-board speaker is coordinate 1D.

A.2 BIOS Beep Codes

Whenever an error occurs during POST, the BIOS exerts an error tone which indicates the problem.

Table 26. POST BIOS Beep Codes

Number of Beeps	Description
1	Memory refresh timer error.
3	Base memory read/write test error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)

Table 27. Troubleshooting POST BIOS Beep Codes

Number of Beeps	Troubleshooting Action
1, 3	Reseat the memory, or replace with known good modules.
6, 7	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

A.3 Port 80h POST Codes

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Table 28. POST Code Checkpoints (Sheet 1 of 2)

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable “wCMOSFlags.”
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to “POSTINT1ChHandlerBlock.”
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after auto-detection of KB/MS using AMI* KB-5.
C0	Early CPU Init Start - Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2* mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. USB* controllers are initialized at this point.
39	Initializes DMAC-1 and DMAC-2.

Table 28. POST Code Checkpoints (Sheet 2 of 2)

3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, ... etc.) successfully installed in the system and update the BDA, EBDA, etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Initialization of system management interrupt by invoking all handlers. *Please note that this checkpoint comes right after checkpoint 20h.*
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

A.4 BIOS Error Messages

Table 29 lists the error messages and provides a brief description of each.

Table 29. BIOS Error Messages

Error Message	Explanation
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.

A.5 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails or execution stops, the last POST code generated by the BIOS is left at port 80h. This code is useful for determining the point where an error occurred.

The following tables provide information about the POST codes generated by the BIOS:

- Table 30 lists the Port 80h POST code ranges.
- Table 31 lists the Port 80h POST sequence.

Table 30. Port 80h POST Code Ranges

Range (Hexadecimal)	Category/Subsystem
00–0Fh	Debug codes: Can be used by any PEIM/driver for debug.
10–1Fh	Host Processors: 1Fh is an unrecoverable processor error.
20–2Fh	Memory/Chipset: 2Fh is no memory detected or no useful memory detected.
30–3Fh	Recovery: 3Fh indicated recovery failure.
40–4Fh	Reserved for future use.
50–5Fh	I/O Busses: PCI, USB*, ISA, ATA, etc. 5Fh is an unrecoverable error. Start with PCI.
60–6Fh	Reserved for future use (for new busses).
70–7Fh	Output Devices: All output consoles. 7Fh is an unrecoverable error.
80–8Fh	Reserved for future use (new output console codes).
90–9Fh	Input devices: Keyboard/Mouse. 9Fh is an unrecoverable error.
A0–AFh	Reserved for future use (new input console codes).
B0–BFh	Boot Devices: Includes fixed media and removable media. BFh is an unrecoverable error.
C0–CFh	Reserved for future use.
D0–DFh	Boot device selection.
E0–FFh F0–FFh	FFh processor exception. E0–EEh: Miscellaneous codes. EFh boot/S3: resume failure.

Table 31. Typical Port 80h POST Sequence (Sheet 1 of 2)

POST Code	Description
21	Initializing a chipset component
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
25	Configuring memory
28	Testing memory
34	Loading recovery capsule
E4	Entered DXE phase
12	Starting Application processor initialization
13	SMM initialization
50	Enumerating PCI busses
51	Allocating resources to PCI bus
92	Detecting the presence of the keyboard

Table 31. Typical Port 80h POST Sequence (Sheet 2 of 2)

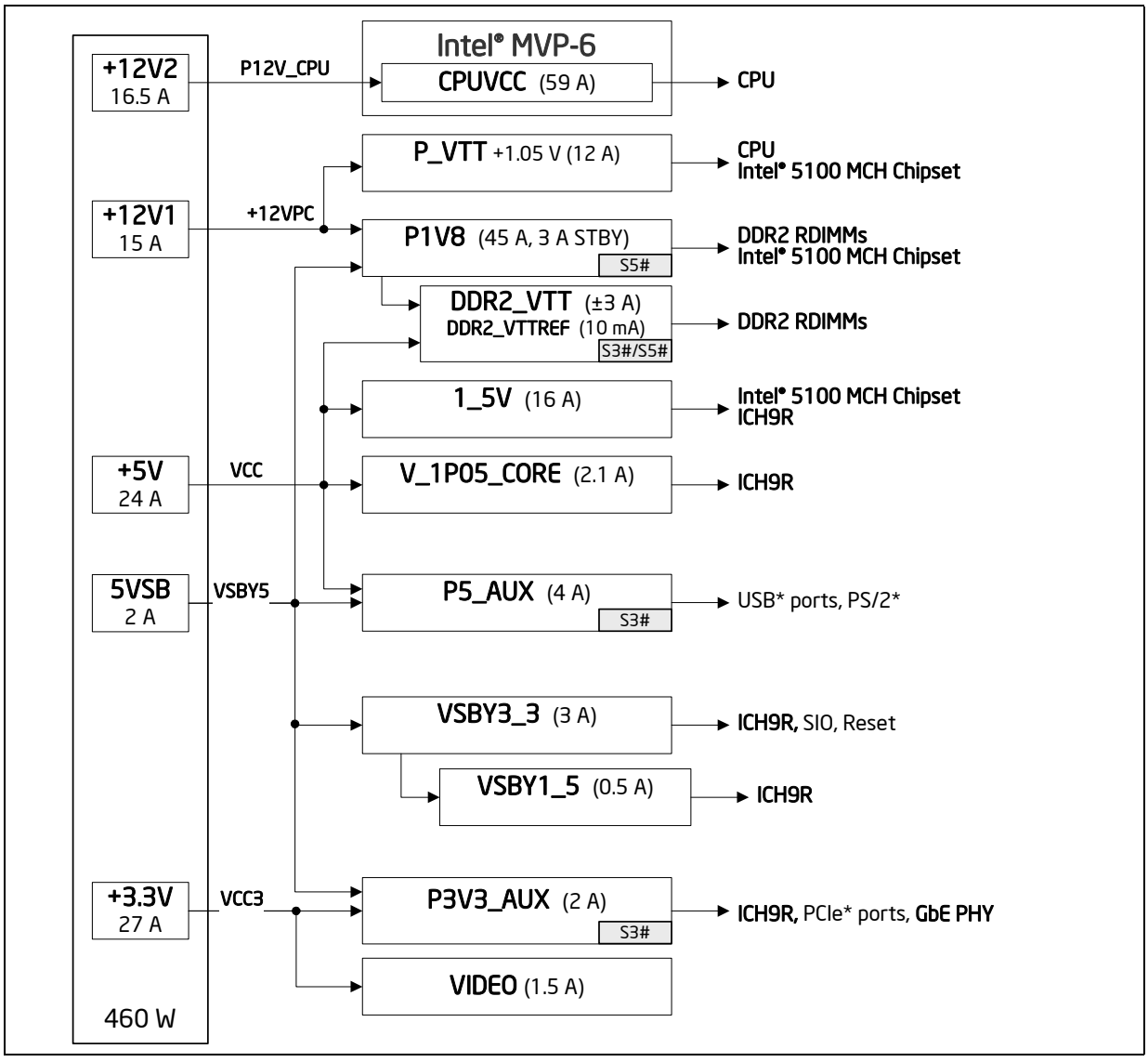
POST Code	Description
90	Resetting keyboard
94	Clearing keyboard input buffer
95	Keyboard Self Test EB Calling Video BIOS
58	Resetting USB* bus
5A	Resetting PATA/SATA bus and all devices
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
5A	Resetting PATA/SATA bus and all devices
28	Testing memory
90	Resetting keyboard
94	Clearing keyboard input buffer
E7	Waiting for user input
01	INT 19
00	Ready to boot

Appendix B Board Reference Diagrams

B.1 Power Overview

This diagram shows the CRB's power supply/loading scheme.

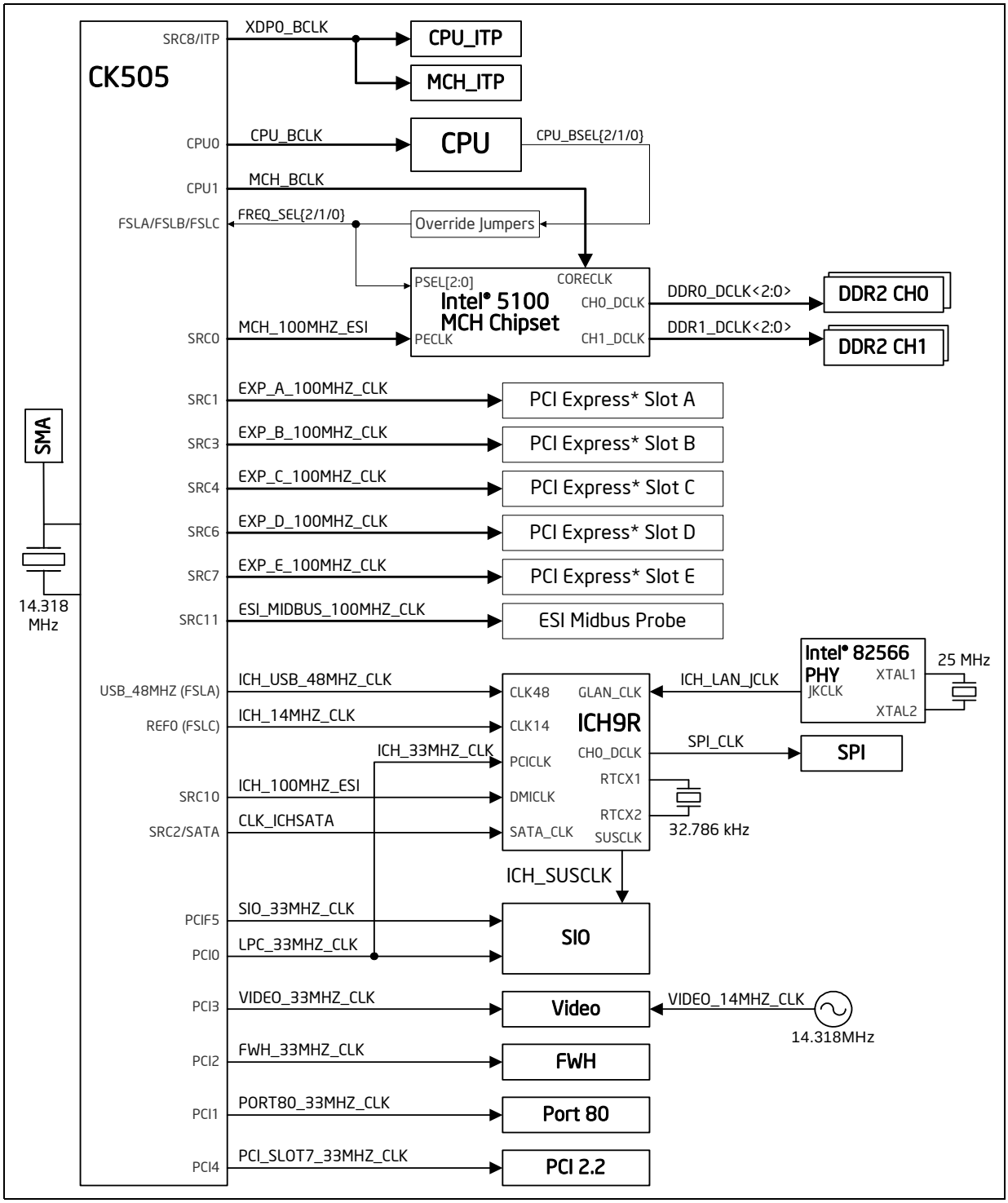
Figure 8. Power Diagram



B.2 Clocking Overview

This diagram shows the CRB's clock signaling scheme.

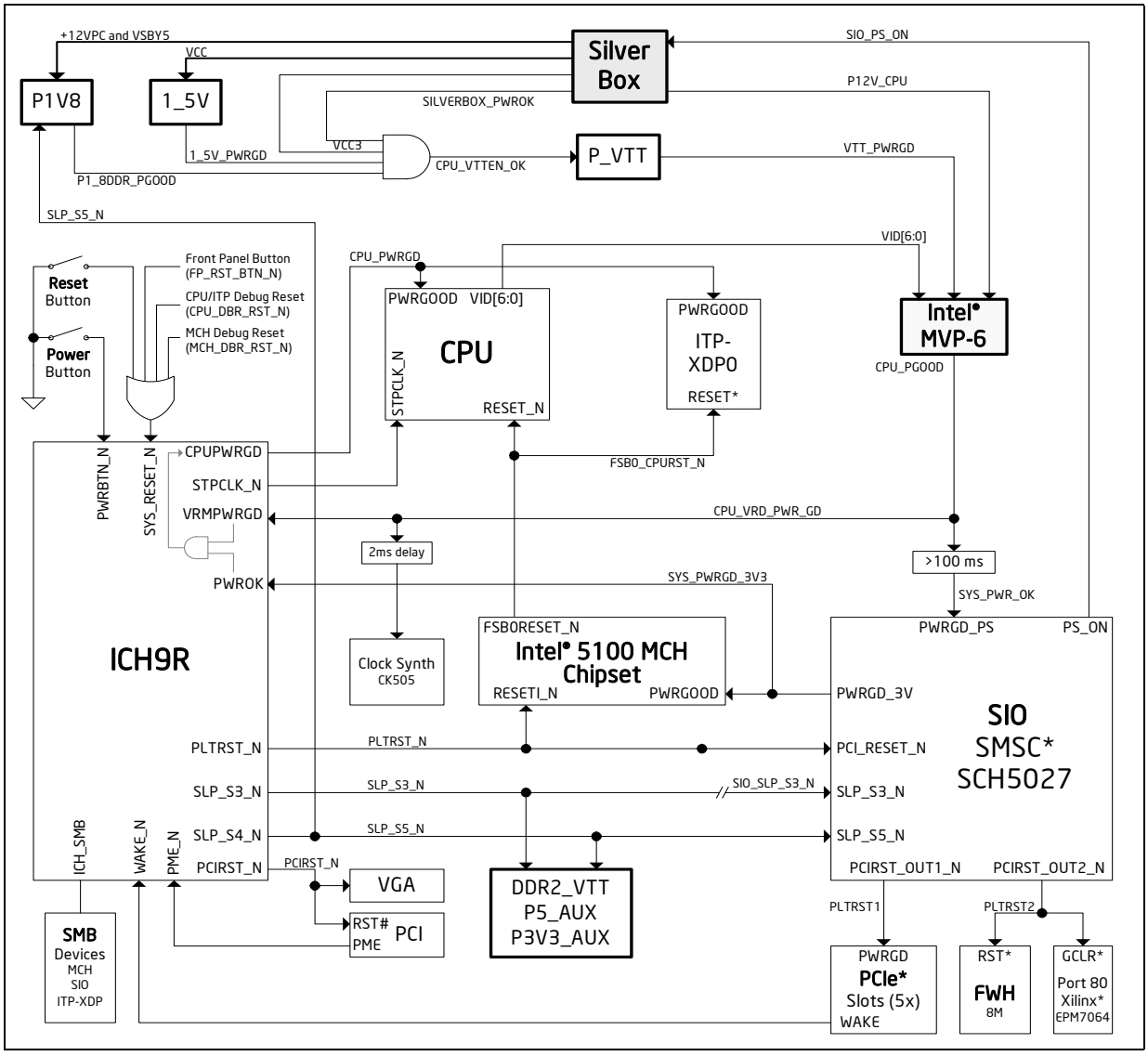
Figure 9. Clock Diagram



B.3 Reset and Power Management Signal Overview

This diagram shows the CRB's reset signaling scheme and power management signaling scheme.

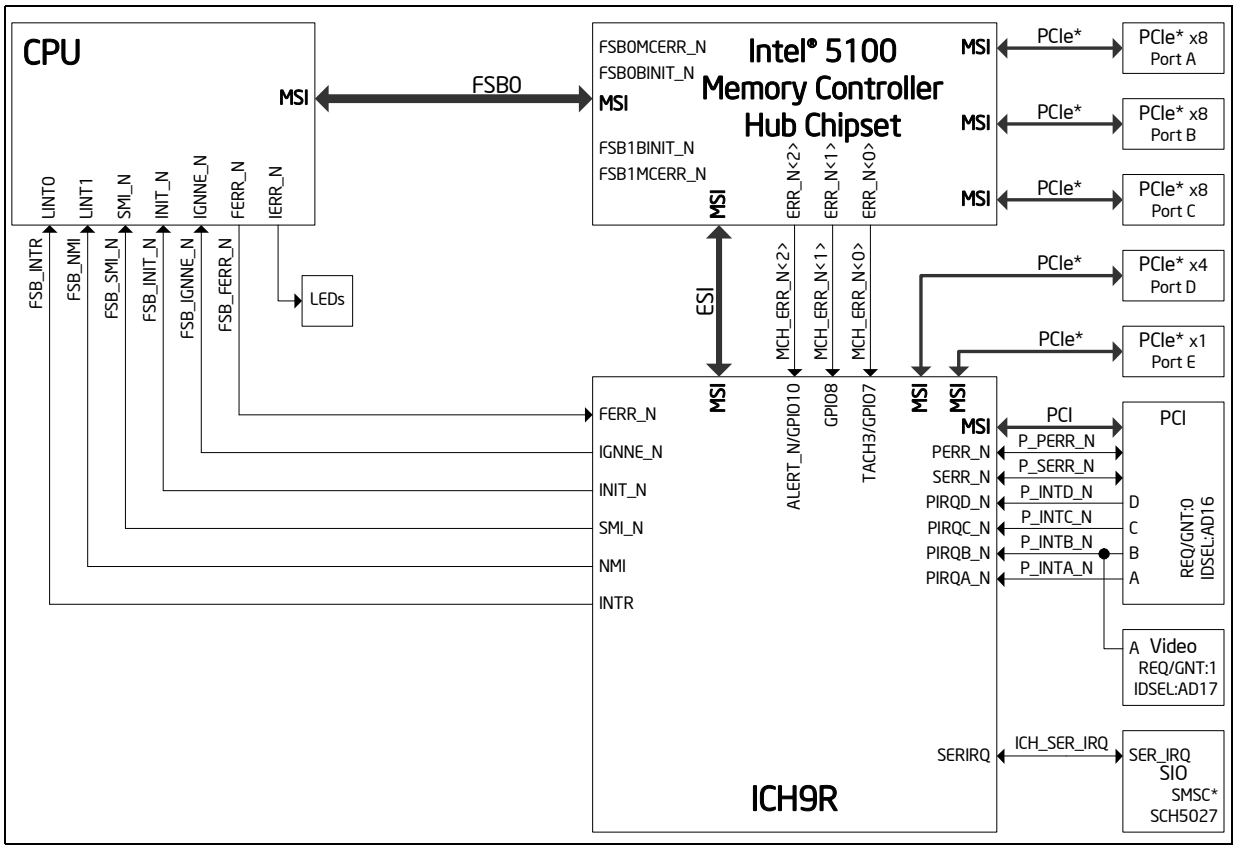
Figure 10. Reset and Power Management Signal Diagram



B.4 Interrupt and Error Signal Overview

This diagram shows the CRB's interrupt and error signaling scheme.

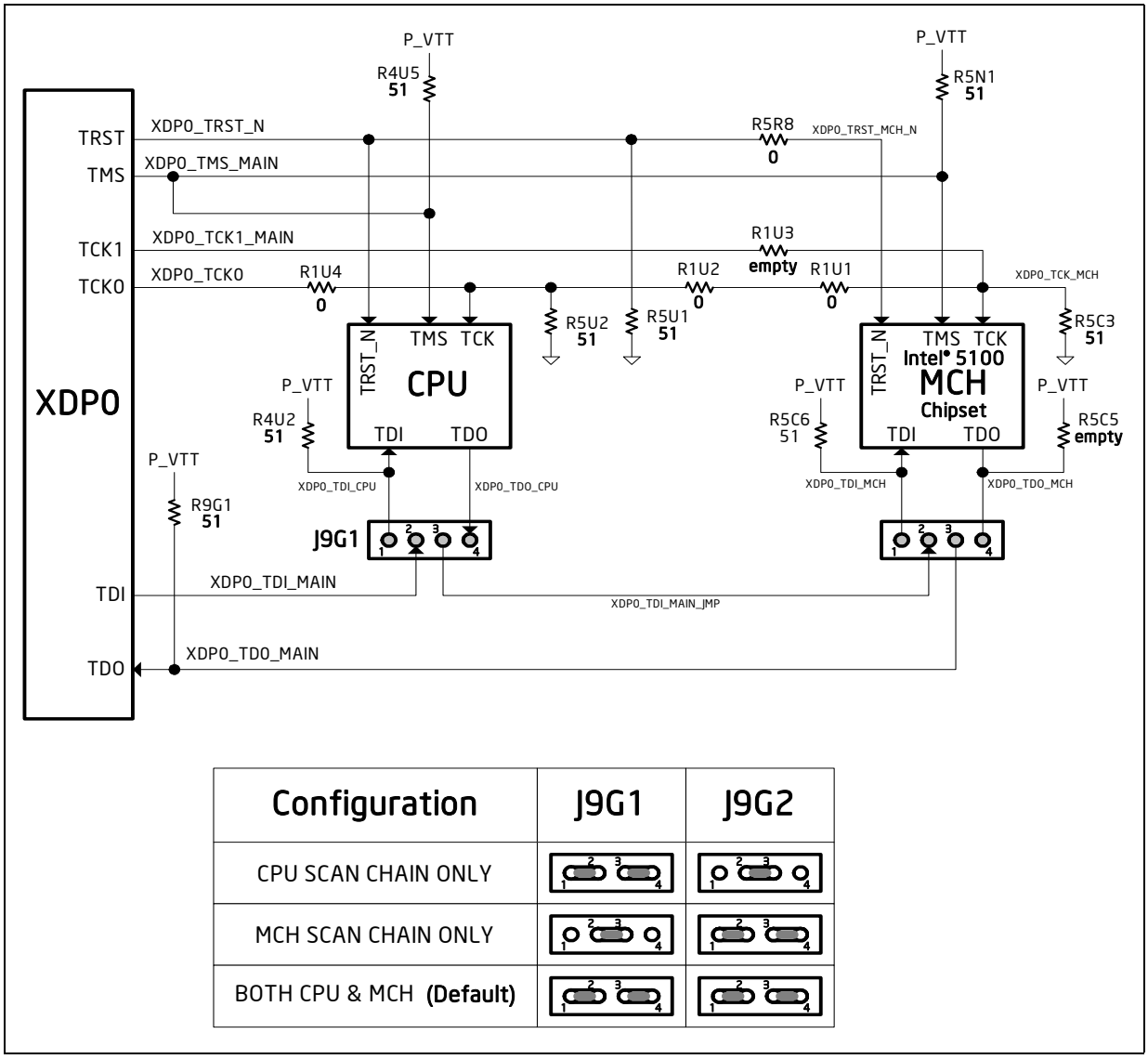
Figure 11. Interrupt and Error Signal Diagram



B.5 External Debug Port Signal Overview

This diagram shows the CRB's ITP-XDP0 signaling scheme for the scan chain test.

Figure 12. External Debug Port Signal Diagram - Scan Chain Test



Configuration	J9G1	J9G2
CPU SCAN CHAIN ONLY		
MCH SCAN CHAIN ONLY		
BOTH CPU & MCH **(Default)**		

B.6 System Management Bus Signal Overview

This diagram shows the CRB's SMBus signaling scheme.

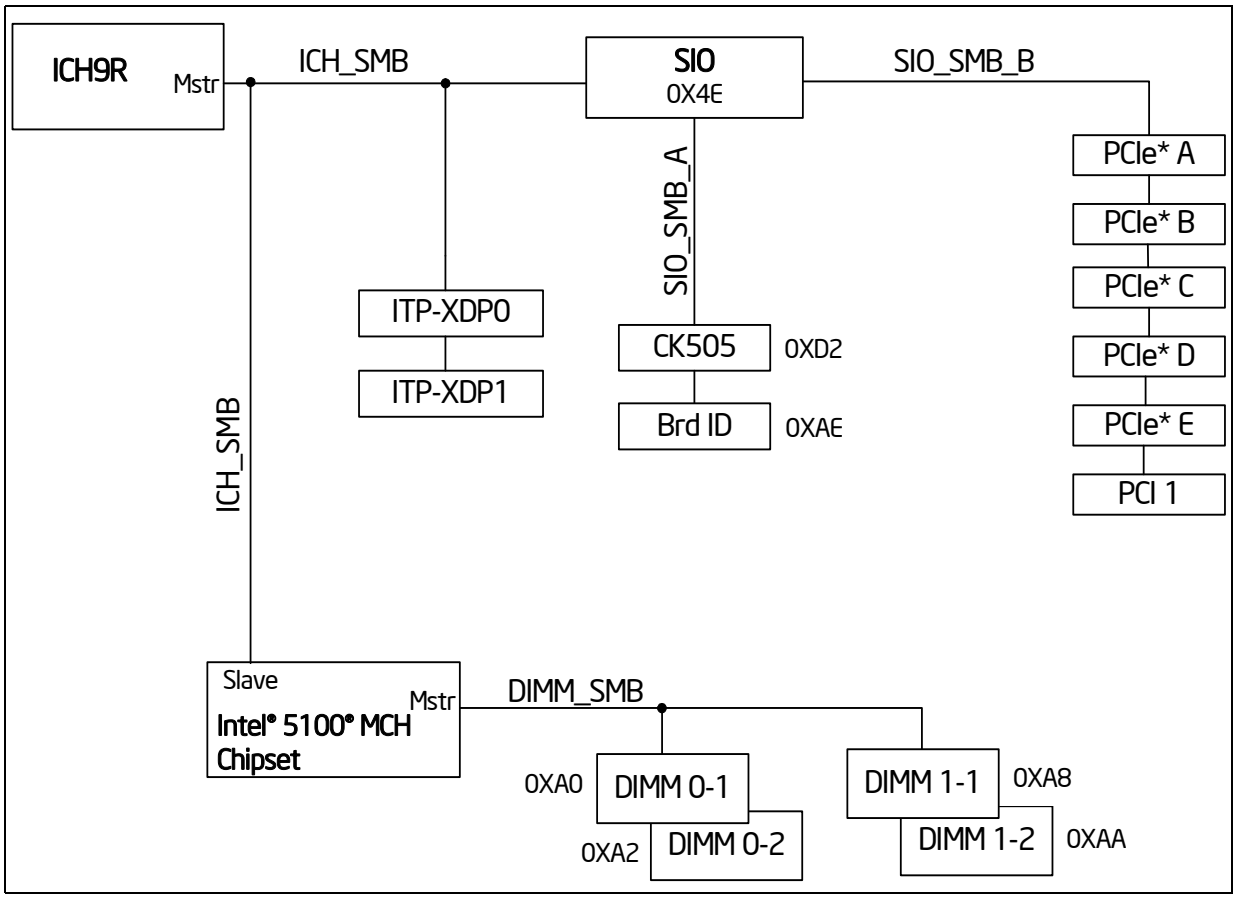



Figure 13. System Management Bus Signal Diagram