Display Panel Debugging with the Intel Graphics Memory Controller Hub

Application Note

January 2005

Order Number: 305964-001

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Revision History

Date	Revision	Description
January 2005	001	Initial release of this document.

1.0 Purpose of This Document

This document describes procedures for debugging display problems with Intel Graphics Memory Controller Hubs (GMCHs) that support the following chipset families:

- Intel® 830
- Intel® 845
- Intel® 852
- Intel® 855
- Intel® 865

The specific issues covered in this document include:

- Debugging Analog Displays
- Debugging Digital Video Out Displays
- Debugging the Internal LVDS Port
- Debugging Out of Sync/Flickering Displays
- Debugging Color Issues

2.0 Scope of This Document

This document is intended to be a preliminary guide in debugging display issues with Intel GMCHs.

This document assumes that the graphics driver and video BIOS are free of bugs that would infringe all the above mentioned debugging methods. If any of the methods used in this document do not match graphics driver or video BIOS output, it is likely to be a defect found in the graphics driver or video BIOS.

This document does not provide guidelines for designing GMCH embedded systems or reference boards.

The debugging methods are only applicable to Almador-class GMCHs and do not apply to newer GMCH classes. There are several GMCH graphics cores on the market. Older GMCHs provide only an analog port and digital port, while newer GMCHs have more than one digital port interface, one analog port, and a dedicated port for low voltage differential signals (LVDS).

3.0 Introduction to the GMCH

The GMCH lies on the North Bridge in Intel architecture systems. The device provides the processor interface, DDR SDRAM interface, display interface, and Hub Interface in an Intel chipset platform. GMCHs consist of three major components:

- Memory Controller Hub (MCH)— Maintains system memory.
- Graphics Controller — Produces visual output using Planes, Pipes, and Ports.
- Graphics Accelerator— Allows applications and operating systems to describe images with minimal CPU usage.

The graphics controller's main functionality is to provide graphics to the display panel. Originally designed to display to legacy cathode ray tube (CRT) panels using analog signals, the GMCH has evolved to support better quality display panels with digital signals and now the fast-growing LVDS. The GMCH provides high-quality performance through several interfaces:

- Legacy VGA
- VESA functions to Operating Systems (OS) Application Programming Interface (API) overlay
- 2D, 3D, Graphics Device Interface (GDI)
- Alpha blending calls

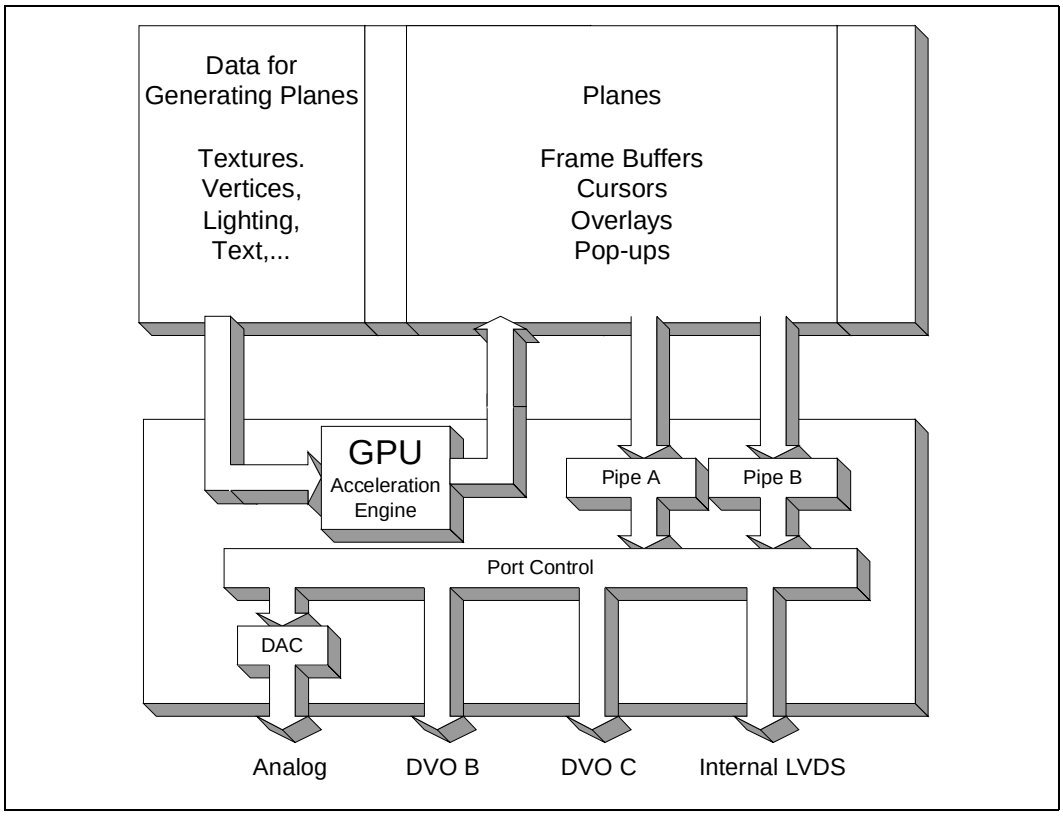
Understanding the basics of the display mechanism will make the debugging process easier.

Graphics controllers consist of:

- Plane— Size, position, and format characteristics of a rectangular shaped surface (image in memory). It is the characteristic that turns blocks of memory into an image.
- Pipe— Translates data from one or more planes to 24-bit RGB pixel data for constant streaming output. The pipe streams planes at a controlled clock rate. There are two display pipes on mobile chipsets, but only one display pipe on desktop chipsets.
- Port— The data stream output connection point, which also controls stream format.

The data path of the GMCH is shown in Figure 1.

Figure 1. GMCH Data Path



The GMCH has four dedicated display interfaces:

- Analog port
- LFP LVDS interface (available only on the mobile chipset)
- DVO B interface
- DVO C interface

The DVO B and DVO C interface can support TV-out encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure, and/or determine the capabilities of an external device. The data that is sent out the display port is selected from one of the two possible sources: display pipe A or display pipe B.

In order to produce an image on a display panel, two software components are needed: video BIOS and the graphics driver.

Video BIOS is one of the Option ROM flashed into the firmware hub. The size is 64 Kbit and is shadowed in C0000 - CFFFF memory area during POST to control the GMCH to support basic video mode.

The **graphics driver** is needed after the OS is successfully loaded. The graphics driver enables more display features and capabilities of the graphics controller, as shown in Table 1.

Table 1. Pipe Usage: Video BIOS and Graphics Driver Comparison

Pipe Usage	Video BIOS	Graphics Driver
Pipe 1 in Single mode to any ports	Yes	Yes
Pipe 1 in Twin mode to any ports	Yes	Yes
Pipe 2 in Twin mode to any ports	No	Yes
Pipe 1 in Clone mode to any ports	No	Yes
Pipe 2 in Clone mode to any ports	No	Yes
Dual Pipe Extended mode support	No	Yes

4.0 Debugging Analog Displays

The analog display port provides RGB signal output along with a H_{SYNC} and V_{SYNC} signal. An associated display data channel (DDC) signal pair uses GPIO pins dedicated to the analog port. The intended target device is a CRT-based monitor with a VGA connector.

Analog display is the most basic and simple display interface of the GMCH so the default video BIOS and graphics driver provided by Intel should function correctly. If there is no display or VGA output after plugging a CRT monitor into the platform, then follow the steps below to debug the display interface.

4.1 System BIOS Settings

An analog display will work once a CRT monitor is plugged into the analog port. However, system BIOS controls routing of the display signal to the internal graphics controller of the GMCH, or to a third-party display card, either through the PCI or AGP interface.

Note: Ensure that the system BIOS is set such that the display is directed to the analog port of the internal graphics controller.

4.2 Hardware Connection Checking

In normal operation, the GMCH sets up the display output by generating an Inter-IC (I^2C) or DDC signal to communicate with the display device. One method to check that the correct hardware connections are used is to send an I^2C command through the DDC pin pair.

Intel provides a display debugging utility called the GMCH Utility, which is capable of accessing the I^2C and memory-mapped I/O (MMIO) interface. On I^2C access, the utility adopts the same command and interface used by the Intel video BIOS, and is capable of retrieving the CRT monitor information through device address A0.

The recommended DDC pin pair connection for analog displays is DDCACLK and DDCADATA, which are the DDC clock and data signals between the CRT monitor and the GMCH. These are the default pin pair settings for the Intel video BIOS and graphics drivers. Check to see if the same settings are used on the platform. If not, the pin pair settings need to be updated in the video BIOS and graphics driver.

4.3 Signal Measurement

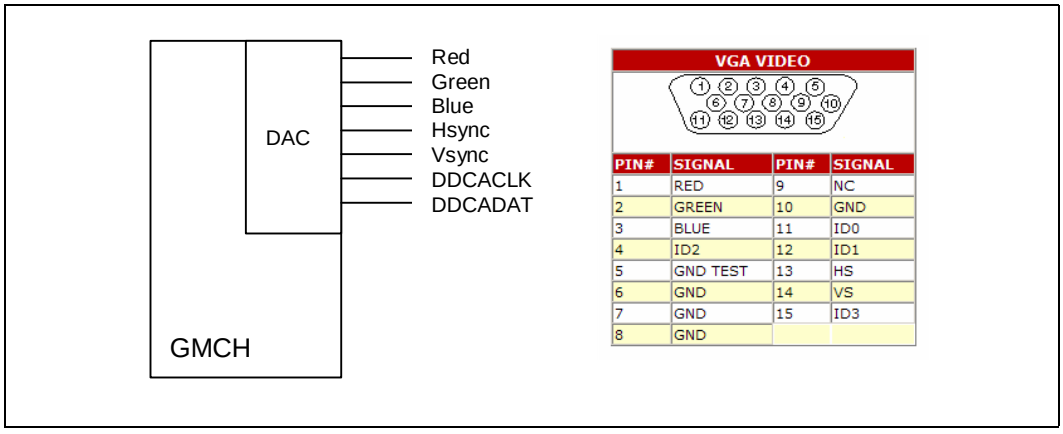
If the hardware connection appears to be correct, and settings have been updated in the video BIOS and graphics driver, and yet there is still no display on the CRT monitor, confirm the output display by measuring the signal from the analog port on the GMCH using a standard oscilloscope. Measurement can be done on the GMCH hardware itself, or from the analog connector.

Important signals to be measured are H_{SYNC} and V_{SYNC} signals, as these are the frequencies and polarities used by the monitor to determine image location in the stream.

DDC lines are used to read Plug and Play monitor information. A signal on the DDC lines indicates that communication is established between the GMCH and the CRT monitor.

Figure 2 illustrates the relationship between the GMCH, the digital-analog converter (DAC), and output signals on the analog VGA connector.

Figure 2. Essential Connections of the GMCH, DAC Component and Analog Connector



PIN#	SIGNAL	PIN#	SIGNAL
1	RED	9	NC
2	GREEN	10	GND
3	BLUE	11	ID0
4	ID2	12	ID1
5	GND TEST	13	HS
6	GND	14	VS
7	GND	15	ID3
8	GND		

4.3.1 Relationship Between Controller Output Data and Input Data Clock

Figure 3 and Figure 4 below explain the relationship between the data enable (DE) signal, H_{SYNCH} signal, and display data.

In these diagrams the DE, H_{SYNC}, and V_{SYNC} signals are shown with positive polarity. DE must always have positive polarity, whereas H_{SYNC}, V_{SYNC}, and other control signals (CLT[3:1]) can have either positive or negative polarity.

The DE signal is used to differentiate between "active" display area and "non-active" display area ("blank" time).

As illustrated in Figure 3, display data (D[23:0]) should only be sent after the DE signal is activated. If D[23:0] is sent before DE is high, then the data will not be displayed on the monitor. If H_{SYNC} is sent after the display hits the end of the horizontal line (on the right of the display panel), the display should be readjusted so that H_{SYNC} is sent when the display is at the beginning of the horizontal line (left of display panel).

Figure 3. Horizontal Input Timing

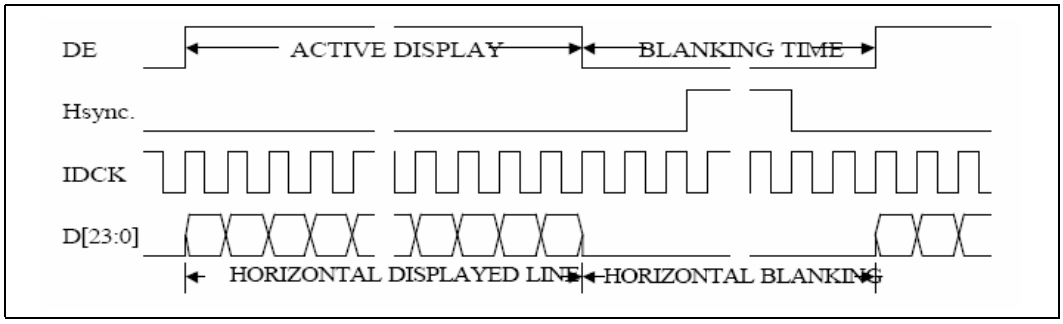
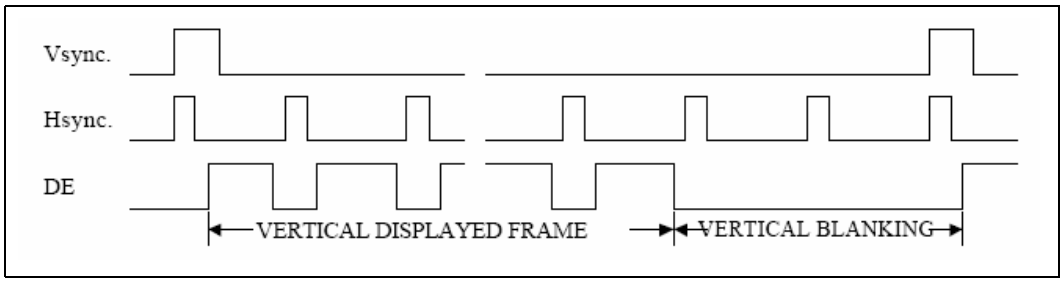


Figure 4 below illustrates the relationship between H_{SYNC} and V_{SYNC} signals. V_{SYNC} typically takes place after a number of H_{SYNC} occurrences. The ratio between H_{SYNC} and V_{SYNC} occurrences depends on the display mode/resolution. For example, if the display mode is 800 x 600, H_{SYNC} takes place after 800 pixels are drawn, while V_{SYNC} takes place after 600 H_{SYNC} occurrences.

Figure 4. Vertical Input Timing

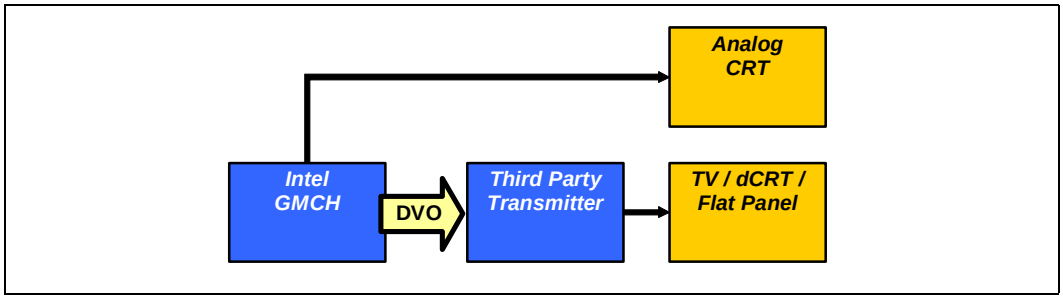


5.0 Debugging Digital Video Out Displays

Digital Video Out (DVO) is a proprietary bus/protocol for connecting third-party transmitters to Intel graphics chipsets. It is used by display transmitters that convert a DVO stream into a signal that can be displayed:

- DVI (DVO B/ C –>TMDS)
- LFP (DVO B/ C –> LVDS)
- TV (DVO B/C –> NTSC/PAL)

Figure 5. DVO Connection



After initialization of the GMCH, the video BIOS will try to detect the presence of any third-party transmitters and initialize them. Third-party transmitter device detection is done by issuing an I^2C signal through the I^2C pin pair, with the device address as identifier. A transmitter with the correct device address will respond to the I^2C signal. Video BIOS will then search for the initialization routine based on the device identifier.

5.1 Check Support for Digital Transmitter

For a third-party transmitter to function as designed, the initialization and functional routine needs to be included in the Intel video BIOS and graphics driver module. The user must determine whether the digital transmitter used is supported by the Intel video BIOS or graphics driver.

For a list of supported transmitters, please refer to the user guide of the video BIOS and graphics driver.

5.2 Check Hardware Connection

This section describes how to check the I^2C pin pair connection.

The I^2C bus is a simple bidirectional two-wire serial communication interface consisting of the serial data line (SDA) and the serial clock line (SCL). The I^2C bus provides for efficient inter-IC control and has a unique address so that a master/slave relationship can be maintained. The GMCH has several I^2C pin pairs available for display interface use, as described in Table 2:

Table 2. GMCH I²C Pin Pair Connection

Pair #	Signal Name	Buffer Type	Description	Notes
0	DDCADATA DDCACLK	3.3 V	DDC for Analog monitor (CRT) connection	This cannot be shared with other DDC or I²C pairs due to legacy monitor issues.
1	LCLKCTRLA LCLKCTRLB	3.3 V	For control of SSC clock generator devices down on motherboard	If SSC is not supported, can be used as GMBUS for DVOB or DVOC.
2	DDCPDATA DDCPCLK	3.3 V	DDC for Digital Display connection via the integrated LVDS display port for EDID panel support	If EDID panels are not supported, can be used as GMBUS for DVOB or DVOC.
3	MDVIDATA MDVICLK	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	Can optionally use as GMBUS for DVOB or DVOC.
4	MI2CDATA MI2CCLK	1.5 V	GMBUS control of DVI devices (TMDS or TV encoder)	Can optionally use as GMBUS for DVOB or DVOC.
5	MDDCDATA MDDCCLK	1.5 V	DDC for Digital Display connection via TMDS device	Can optionally use as GMBUS for DVOB or DVOC.

Third-party transmitters normally operate as a slave on the serial bus, so the SCL line is an input (no clock is generated by the third-party transmitter, except the TV encoder) and the SDA line is bi-directional. These transmitters have a 7-bit slave address. The address bits are controlled by the state of the address select pins, and are set by connecting these pins to ground for LOW (0) and to the VCC3V pin for HIGH (1).

Before testing, check these settings:

- GMCH I²C pin pairs that are connected to the third-party transmitter.
- Settings of the slave address select pins.

Ensure that the previous two settings are reflected correctly in the video BIOS and graphics driver configuration file.

Follow these steps to determine positive communication with the I²C pin:

1. Send and read data using the Intel display debugging utility (GMCH Utility).

   In order to use this utility for I²C connection checking, the user needs to have GMCH pin pair information and third-party transmitter device address information.

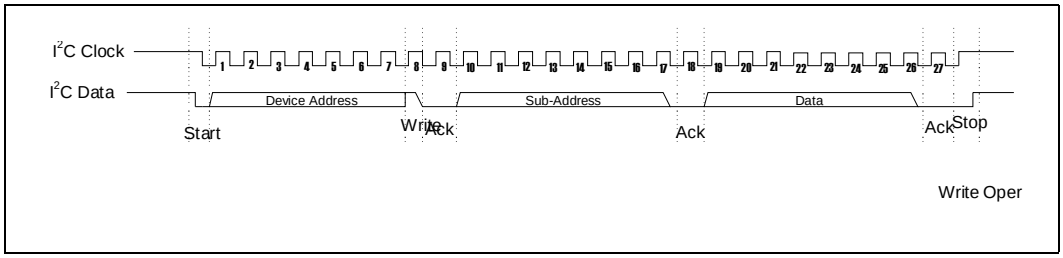
   Read and compare the vendor ID according to the I²C register mapping provided in the third-party transmitter datasheet.
2. Measure the I²C signal on the GMCH pin pair.
3. Refer to Table 3 below for signal identification.

Table 3. Pin Pair and Signal Translation

Pin Pair Number	Pin Use (Name)	Chipsets
5	MDDC (GSTOP#/GAD15)	83x, 85x
5	I2C (AGSTOPB/AGAD15)	845
4	I2C (GDEVSELB/GIRDBY)	All
3	Add Card DDC (GFRAMEB/GTRDYB)	All
2	DDC2 (DDC2Data/DDC2Clk)	83x
2	N/A	845
2	LVDS DDC (DDCPDATA/DDCPCLK)	85x
1	I2C (LCLKCTRLB/LCLKCTRLA)	85x
1	N/A	845
1	I2C (I2C_CLOCK/I2C_DATA)	83x
0	DDC1 (DDC1DATA/DDC1CLK)	83x, 85x
0	DDC	845

This is the sample waveform of a typical I^2C signal. Communication is positive if the information captured matches the hardware connection and software configuration.

Figure 6. Sample I^2C Signal



5.3 Identify Display Modes (Twin/Clone/Extended)

In order to debug the system, the user will first need to know what display output signals are to be expected. The expected signals will vary according to the display mode.

The following tables and figures describe how to identify each type of display mode.

Table 4. Display Configuration Definition

Display Configuration Mode	Description
Single	Normal desktop configuration, single monitor
Twin	Two displays, same content, single resolution
Clone	Two displays, same content, independent timings
Extended	Two displays, different content, independent resolutions

Figure 7. Single Mode

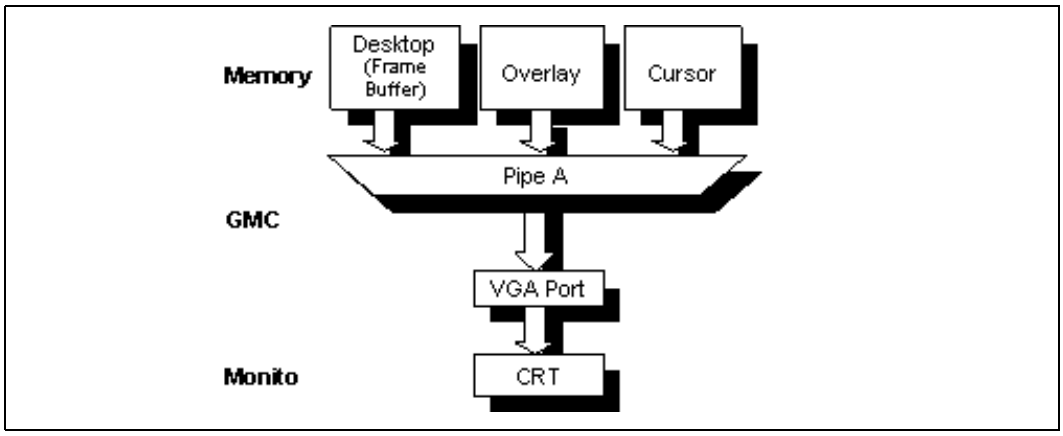


Figure 8. Dual Display Twin Mode

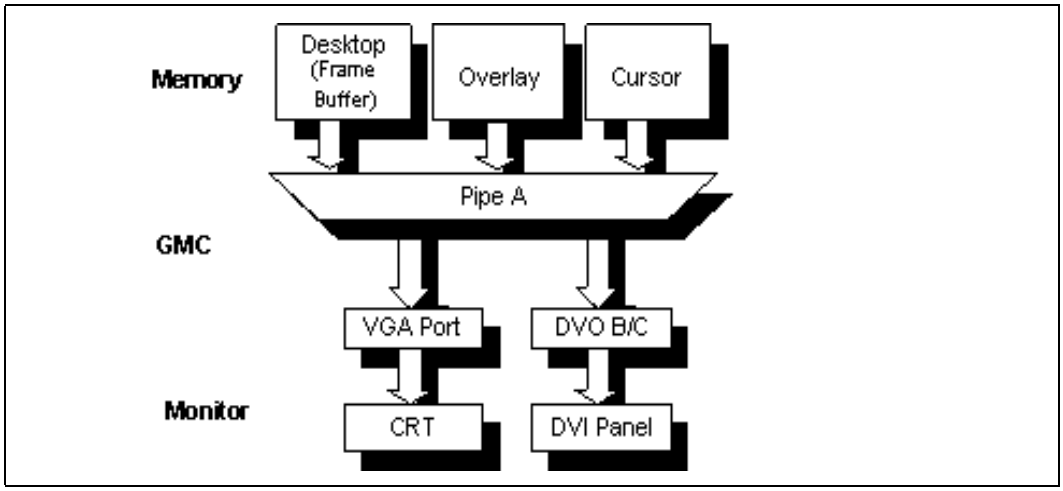


Figure 9. Dual Display Clone Mode

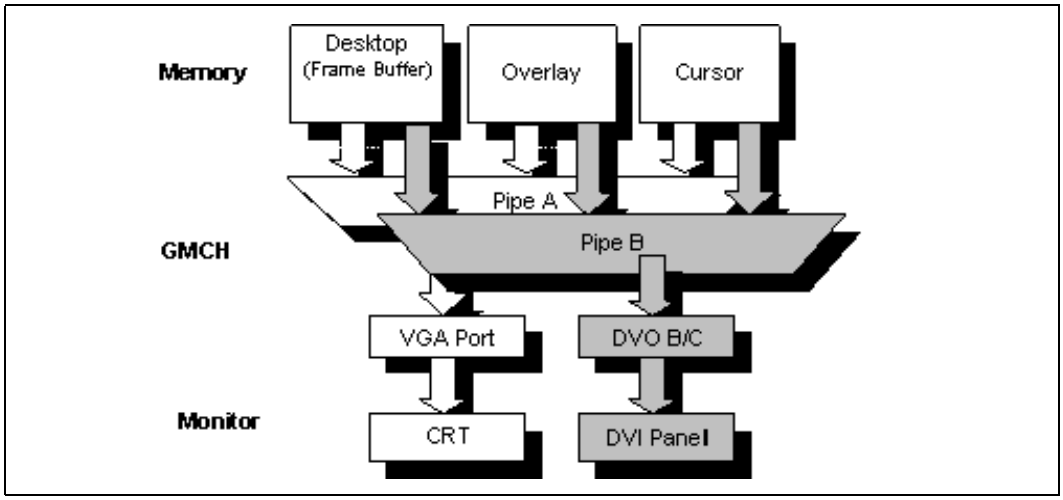
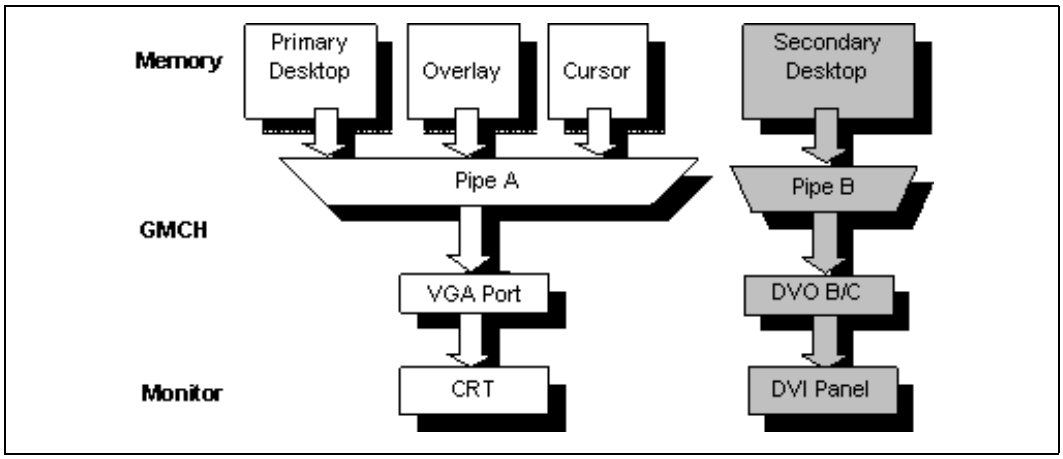


Figure 10. Extended Mode



5.3.1 Pipe Sharing Capability

Pipe sharing between display devices is subject to the limitations stated in the table below:

Table 5. Pipe Sharing Capabilities

	Internal LVDS	DVO B DVI	DVO C DVI	DVO B+C DVI	DVO TV	CRT
Internal LVDS		No	No	No	No	No
DVO B DVI	No		Yes	No	No	Yes
DVO C DVI	No	Yes		No	No	Yes
DVO B+C DVI	No	No	No		No	Yes
DVO TV	No	No	No	No		No
CRT	No	Yes	Yes	Yes	No	

Note: Ensure the display mode selected matches the hardware and software display capabilities. For example, no pipe sharing is possible between the internal LVDS and any other display devices at any time.

5.3.2 Video BIOS

As shown in Table 1 on page 9, there is only one display pipe available in video BIOS mode. (This is true of both the desktop and mobile chipsets.) Therefore, video BIOS can only be configured as single or twin mode.

5.3.3 Graphics Driver

In a fully loaded OS environment, two display pipes are available for mobile chipsets, which enable the support of dual-independent modes such as clone and extended. (With the desktop chipset, only single or twin mode is supported due to the single pipe limitation.)

5.4 Identify Display Panel Type—EDID and EDID-less

Extended Display Identification Data (EDID) is a VESA standard data format that contains basic information about a monitor and its capabilities, including vendor information, maximum image size, color characteristics, factory pre-set timings, frequency range limits, and character strings for the monitor name and serial number.

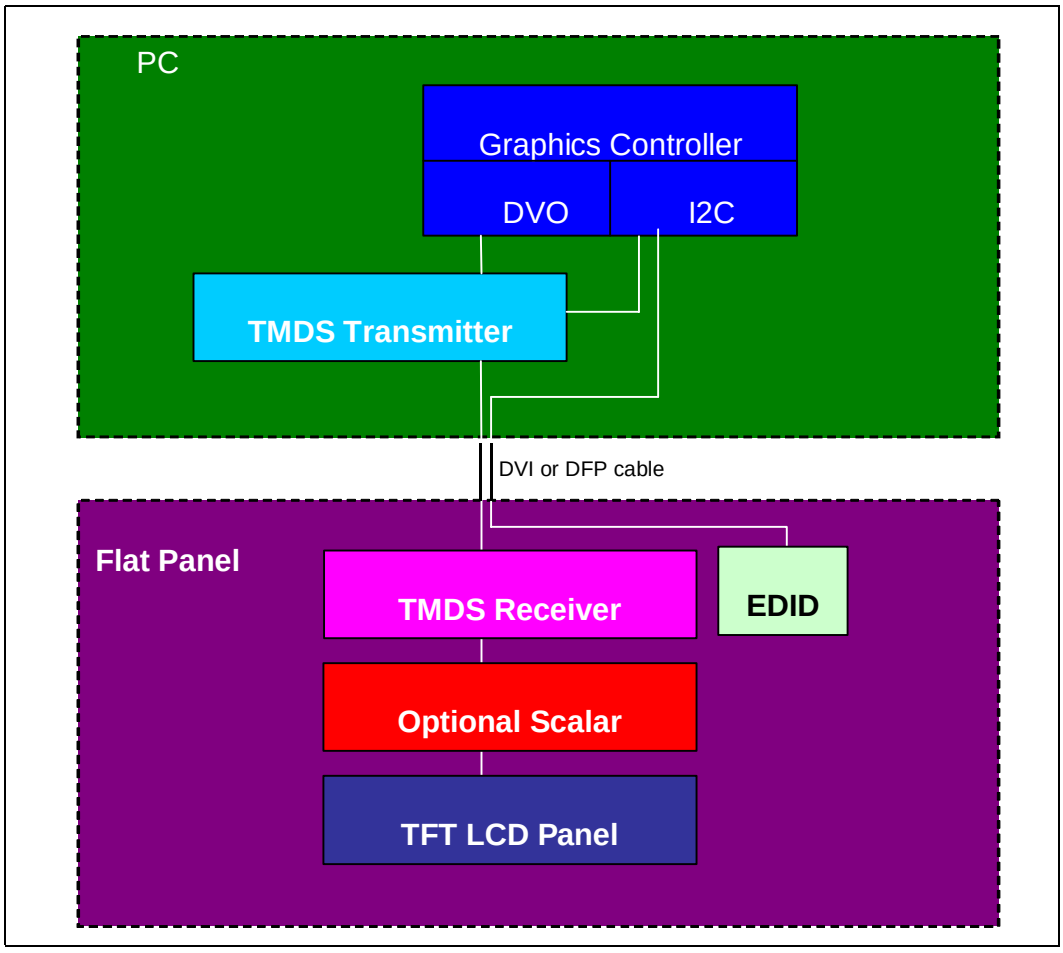
The information is stored in the display and is used to communicate with the system through a display data channel (DDC), which is situated between the monitor and the PC graphics adapter. The system uses this information for configuration purposes, so the monitor and system can work together.

5.4.1 Panels with EDID

Panel characteristics and timing information are programmed into the EPROM which is situated inside the panel. The panel is normally used with a TMDS transmitter, where the DDC connection is used to retrieve the panel information. The user only needs to ensure that the DDC setting is reflected in the video BIOS and graphics driver configuration files.

The layout for a system with EDID is illustrated in Figure 11 below.

Figure 11. Layout for Systems with EDID

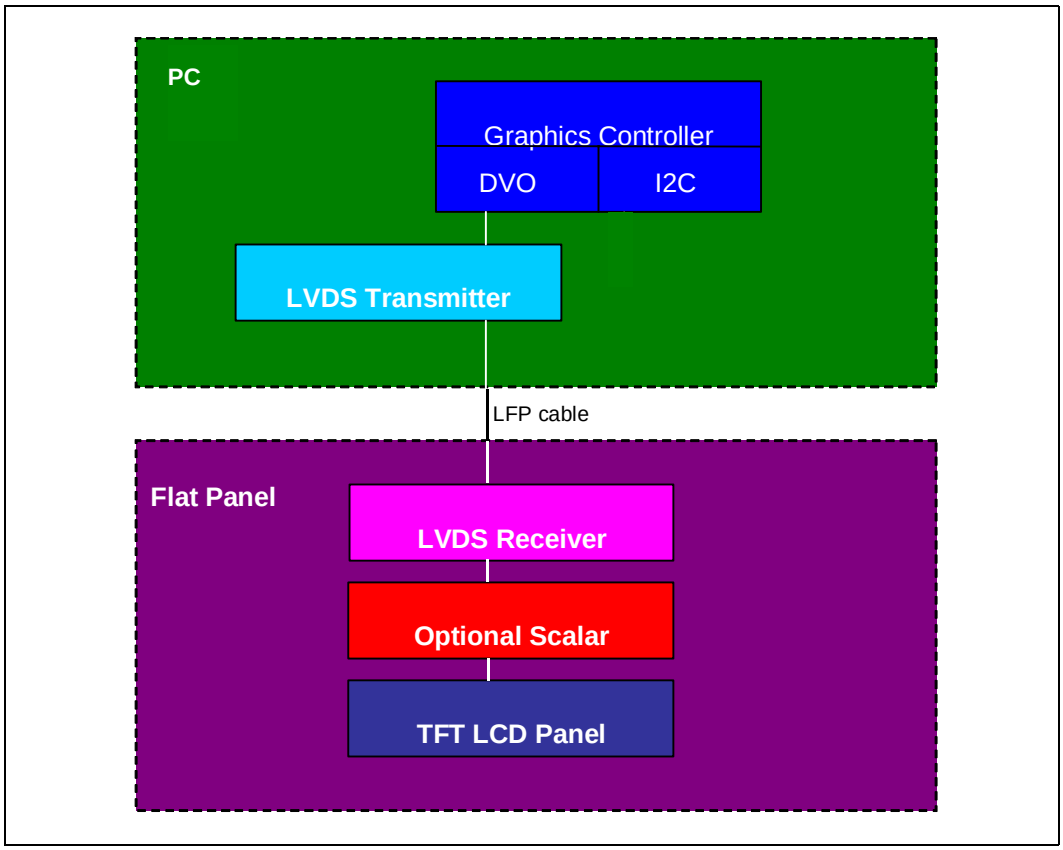


5.4.2 Panel Without EDID (EDID-less)

This type of panel does not include an EPROM and is normally used with an LVDS transmitter. Panel characteristics and timing information need to be supplied through software. The user needs to ensure that panel timing information is programmed correctly into the video BIOS and graphics driver.

EDID-less panel layout is illustrated in Figure 12 below.

Figure 12. Layout for Systems Without EDID



All information regarding the display panel (especially timing information), must be made available to the video BIOS and graphics driver.

5.5 Backlight Enabling for Local Flat Panels (Internal/External LVDS)

LVDS is the standard that is used to connect a display controller to a LCD panel in both mobile devices and all-in-one type desktop devices. Along with the LVDS interface, the panel also has a power sequencing function and a backlight brightness control. Backlights provide the necessary light source for typical LCD panels. A panel may appear to be nonfunctional if no light source is being supplied to the panel.

There are several different ways to turn on the backlight:

1. GMCH— For internal LVDS, in order to meet the panel power timing specification requirements, two signals (PANELVDDEN and PANELBKLTEN) are provided to control the timing sequencing function of the panel and the backlight power supplies.
2. GPIO pins on I/O Controller Hub (ICH)— For external LVDS, the user has the option to control the panel backlight separately from internal LVDS. GPIO pins on ICH can be used as the control pins, provided the setting is included in the video BIOS and graphics driver configuration to turn on the backlight and control the delay. Three GPIO pins are needed:
   a. GPIO pin for panel power
   b. GPIO pin for backlight power on/off sequencing
   c. GPIO pin to enable backlight signal
3. External transmitter— Some third-party transmitters have backlight control pins on the package. In this case, panel backlight will be controlled by the transmitter software routines.

Besides identifying the backlight control method, also take note of the panel-specific power cycle requirements:

- A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary between different panel vendors, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state, and the LVDS clock and data lines are all managed by an internal power sequencer.
- A requested power-up sequence is only allowed to begin after the power cycle delay time requirement T4 is met, as shown in Figure 13. The parameters for all of the sequence events shown below are described in Table 6.

Figure 13. Panel Power Sequencing

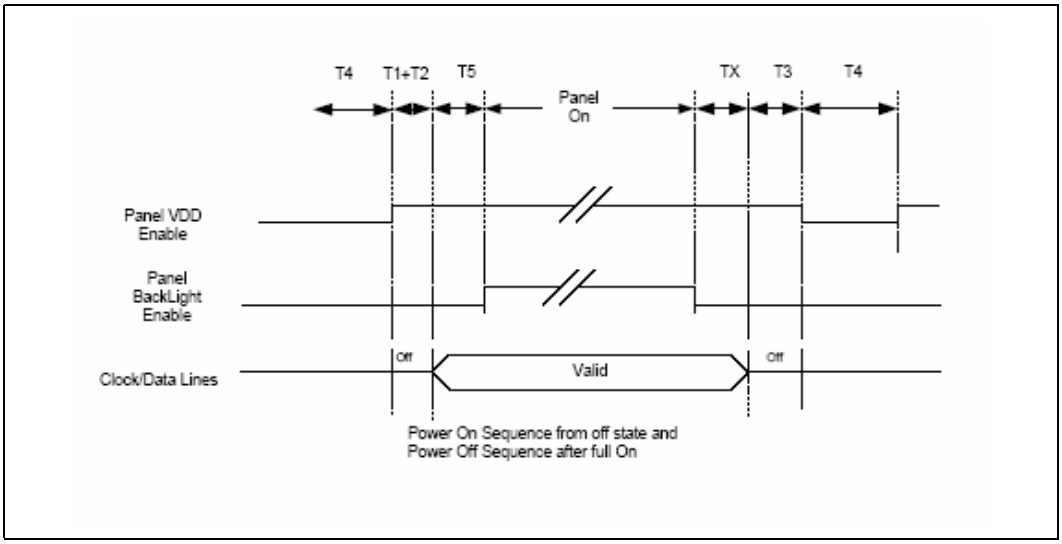


Table 6. Display Configuration Space

Name	Panel Power Sequence Timing Parameters		
	Spec Name	From	To
T1+T2	**VDD On to LVDS Active** Panel VDD must be on for a minimum time before the LVDS data stream is enabled.	0.1 VDD	LVDS Active
T5	**Backlight** LVDS data must be enabled for a minimum time before the backlight is turned on.	LVDS Active	Backlight on
TX	**Backlight State** Backlight must be disabled for a minimum time before the LVDS data stream is stopped.	Backlight Off	LVDS off
T3	**LVDS State** Data must be off for a minimum time before the panel VDD is turned off.	LVDS Off	Start power off
T4	**Power Cycle Delay** When panel VDD is turned from On to Off, a minimum wait must be satisfied before the panel VDD is enabled again.	Power Off	Power On Sequence Start

Note: These timing parameters must be taken from the panel specification document and must be communicated clearly to the video BIOS and graphics driver to ensure panel functionality and protection.

5.6 Signal Measurement

The final debugging procedure is to measure the signal from the DVO port. Only attempt this if the DVO display still fails after following the debugging procedures:

- Third-party transmitter selected is supported by the Intel software module, as described in Section 5.1.
- Hardware settings are correct— I^2C pin pair and transmitter device address, as described in Section 5.2.
- Display mode is supported, as described in Section 5.3.
- Panel information is correct, as described in Section 5.4.
- Backlight control is functional, as described in Section 5.5.

Signal measurement can be done before and after entering the transmitter. Figure 14 shows the locations of the input and output signals in the panel transmitter.

Figure 14. Transmitter Input and Output Signal

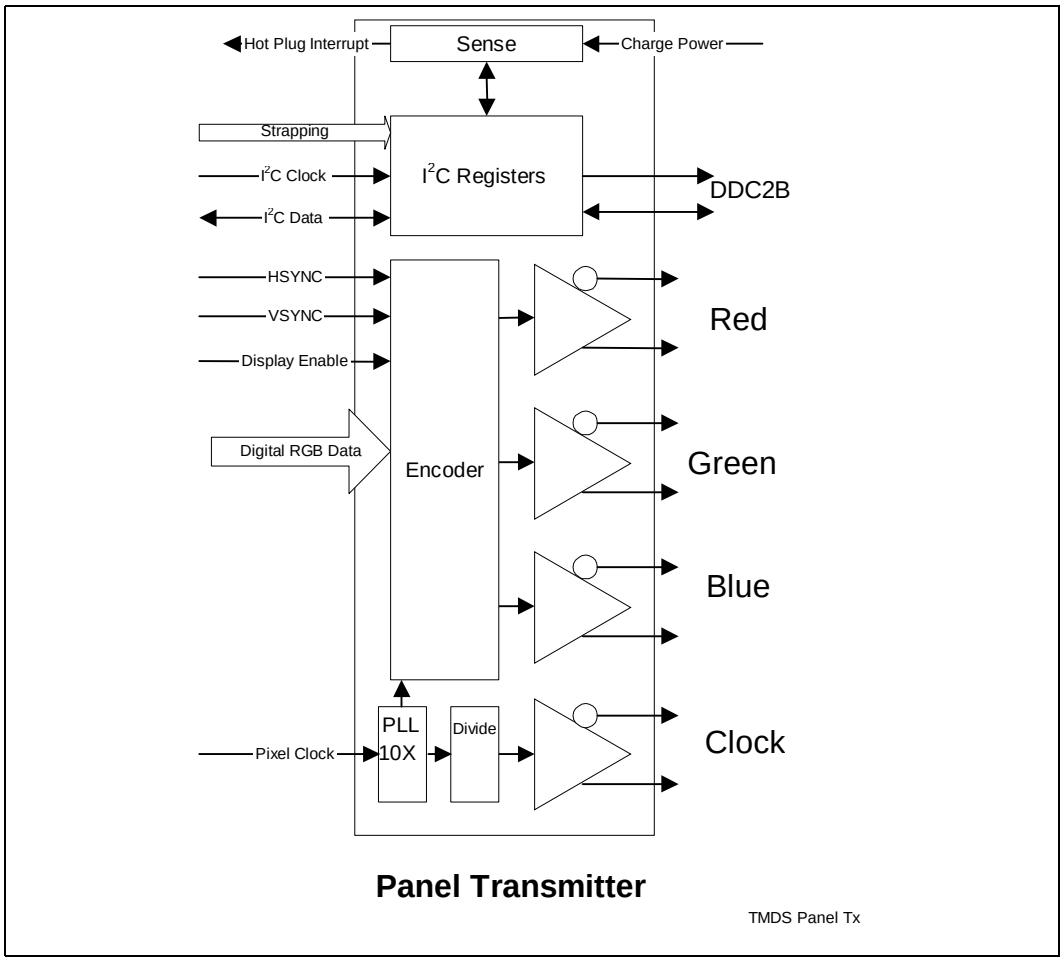
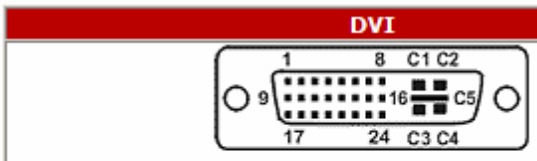


Figure 15. Pinout of DVI Connector



PIN#	SIGNAL	PIN#	SIGNAL
1	T.M.D.S DATA 2-	16	HOT PLUG DETECT
2	T.M.D.S DATA 2+	17	T.M.D.S DATA 0-
3	T.M.D.S DATA 2/4 SHIELD	18	T.M.D.S DATA 0+
4	T.M.D.S DATA 4-	19	T.M.D.S DATA 0/5 SHIELD
5	T.M.D.S DATA 4+	20	T.M.D.S DATA 5-
6	DDC CLOCK	21	T.M.D.S DATA 5+
7	DDC DATA	22	T.M.D.S CLOCK SHIELD
8	ANALOG VERT. SYNC	23	T.M.D.S CLOCK+
9	T.M.D.S DATA 1-	24	T.M.D.S CLOCK-
10	T.M.D.S DATA 1+		
11	T.M.D.S DATA 1/3 SHIELD	C1	ANALOG RED
12	T.M.D.S DATA 3-	C2	ANALOG GREEN
13	T.M.D.S DATA 3+	C3	ANALOG BLUE
14	+5V POWER	C4	ANALOG HORZ SYNC
15	GND	C5	ANALOG GROUND

6.0 Debugging the Internal LVDS Port

The GMCH has a dedicated LFP LVDS interface that can support TFT panel resolutions up to UXGA with a maximum pixel format of 18 bpp, and with a SSC-supported frequency range from 25–112 MHz.

The display pipe selected by the LVDS display port is programmed with the panel timing parameters. These are determined by the installed panel specifications or read from an onboard EDID ROM. The programmed timing values are then “locked” into the registers to prevent unwanted corruption of the values. From that point onwards, the display modes are changed by selecting a different source size for that pipe, programming the VGA registers, or selecting a source size and enabling the VGA. The timing signals will remain stable and active through mode changes.

6.1 Panel Selection

The GMCH LVDS port can only support the following LVDS panels. Only one of these display panels can be connected to the internal LVDS interface.

- 640 x 480
- 800 x 600
- 1024 x 768
- 1280 x 1024
- 1400 x 1050
- 1600 x 1200

The GMCH has no support for 24-bit LVDS panels; the user needs to ensure that only 18-bit LVDS panels are populated to the internal LVDS interface.

6.2 Checking Software Settings

The video BIOS and graphics driver rely on system BIOS settings in the panel information setup. When the system is powered up, values from the system BIOS are passed to the video BIOS and graphics driver.

The most important parameter passed by system BIOS is the panel native resolution, because it determines the timing set used for output display. This parameter must be updated if the display panel is changed. For example, if the user changes from a 1024 x 768 display panel to a 800 x 600 display panel, the panel resolution for a 800 x 600 system must be selected in the system BIOS settings menu.

6.3 Checking Hardware Connection

The output port of the GMCH has the following pins and LVDS signals. In the event of display failure, reconfirm the connection between the GMCH LVDS and the internal LVDS connector interface.

Table 7. Pinout of LVDS Connector (Sheet 1 of 2)

PIN Number	LVDS Signal
1	GND
2	3.3 V
3	3.3 V
4	3.3 V
5	Not connected
6	LVDS_DDCPCLK
7	LVDS_DDCPDATA
8	LVDS_YAM0
9	LVDS_YAP0

Table 7. Pinout of LVDS Connector (Sheet 2 of 2)

PIN Number	LVDS Signal
10	GND
11	LVDS_YAM1
12	LVDS_YAP1
13	GND
14	LVDS_YAM2
15	LVDS_YAP2
16	GND
17	LVDS_CLKAM
18	LVDS_CLKAP
19	GND
20	LVDS_YBM0
21	LVDS_YBP0
22	GND
23	LVDS_YBM1
24	LVDS_YBP1
25	GND
26	LVDS_YBM2
27	LVDS_YBP2
28	GND
29	LVDS_CLKBM
30	LVDS_CLKBP
31	GND
32	GND

7.0 Debugging Out of Sync/Flickering Displays

If the display image is successfully directed to display panel, but the image is not stable (out of sync or flickering), most likely it is related to a timing issue. To debug timing issues:

1. Confirm the panel timing information through the panel specification.
2. Use the Intel GMCH utility to read the display pipe timing and confirm that the display pipe timing matches the output requirement and panel specification. In order to perform this check, information is needed from the display pipe and plane control register. Consult your chipset's programmer reference guide for this information.
3. Use the GMCH utility to access the GMCH's MMIO (memory mapped I/O) register, which holds timing information for the current display output. Compare the values in this register with the panel's EDID data (for EDID systems) or the panel specification data (for EDID-less systems). The EDID is situated inside the panel and can be read using the GMCH utility. For EDID-less panels, the information can be obtained from the panel manufacturer's documentation.

If the timing information from a reading provided by the GMCH utility is different from the display panel specification (EDID or EDID-less), then the GMCH is providing incorrect timing information. In this event, please contact your Intel field representative for further assistance.

In addition to timing information, other critical values available from the MMIO include:

- V_{ACTIVE}
- V_{TOTAL}
- H_{ACTIVE}
- H_{TOTAL}

These values may also be compared against the panel specifications to debug out of synch or flickering displays.

8.0 Debugging Color Issues

Display output data sequence is selectable through the display port control register. If image color on the display output does not meet expectations:

1. Use the GMCH utility to check the dedicated display port control register (that is, check the DVOB port control register if the display is connected to DVOB).
2. Check that the data sequence selected in the display port control register matches the panel requirements. For display port control register settings, consult your chipset's programmer reference guide.

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