Ultra Low Voltage Intel® Celeron® Processor in 5.25" Form Factor

Overview

White Paper

October, 2003

Order Number: 274002

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1.0 Introduction

The Ultra Low Voltage Intel® Celeron® processor provides an exceptional value for thermally sensitive and space-constrained embedded computing applications by combining the optimal balance of cost, performance, and low power. It is available in small form factor micro-FCBGA packages at 400 MHz and 650 MHz with 256 Kbytes of on-die L2 cache.

The new 400 MHz processor, at just 0.95 V and 4.2 W TDP (max), and the 650 MHz processor, at just 1.1 V and 8.3 W TDP (max), are ideal solutions for communication appliances such as network attached storage, web pads, and other embedded applications in the embedded market with lower power envelopes and BOM requirements.

The 256 Kbytes of on-die cache combined with the efficiencies of 0.13-micron manufacturing processes offer good low-power processor performance for value-based systems. The compact form factor results in a low profile, meeting small space requirements. This enables a variety of value-based designs for thermally sensitive and space-constrained environments, especially in boards like the 5.25" single form factor that is becoming popular in embedded applications.

The Ultra Low Voltage Intel Celeron processors at 400 MHz and 650 MHz are validated with the Intel 440MX and Intel® 815E chipsets. The 815E chipset GMCH provides an integrated graphic solution to eliminate the requirement for an AGP display slot, saving space on the 5.25" form factor. Paired with the 815E GMCH supporting I/O bridge, the Intel I/O Controller Hub 2 (ICH2) provides rich I/O interfaces. ICH2 provides an AC'97 link for audio and telephony CODECs and is able to support up to six channels of PCM audio output (full AC3 decode). This allows an OEM to use its software-configurable AC'97 audio and modem CODEC instead of the traditional ISA devices. An Integrated LAN controller in ICH2 helps minimize PCB trace routing (although an external PHY layer is still required). This further reduces onboard space; normally a full LAN controller (MAC & PHY layers within silicon) requires more space due to silicon/package size. The USB 1.1 controller provides up to four USB ports. The LPC interface provides an interface for an external Super I/O chip for legacy component support. In short, the ICH2 provides a rich set of integrated functions and I/O interfaces for the 5.25" board's commonly used features.

> ***Note:*** For more information on ICH2 features, please refer to the ICH2 Datasheet, available from the Intel Developer's Site (http://developer.intel.com/design/chipsets/815e/index.htm)

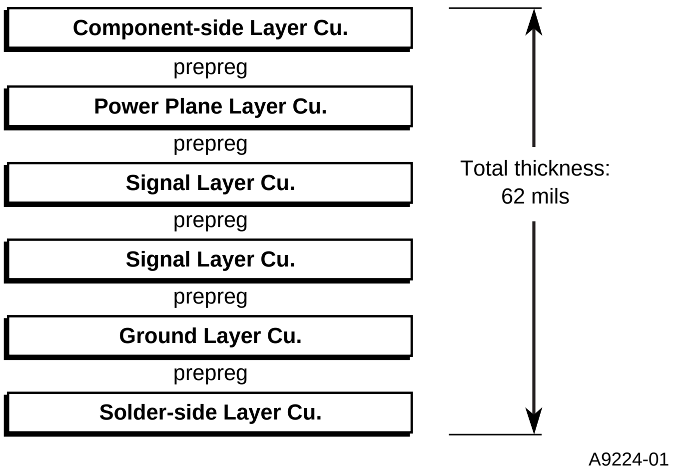
In any circumstance, where a 5.25" form factor embedded application requires ACPI power management, the Ultra Low Voltage Intel Celeron Processor with Intel 815E chipset platform provides ACPI functionality at the following power-management states:

- Full-on (S0)
- Stop Grant (SI)
- Suspend to RAM (S3)
- Suspend to Disk (S4)
- Soft-off (S5)

2.0 Nominal Board Stack-Up

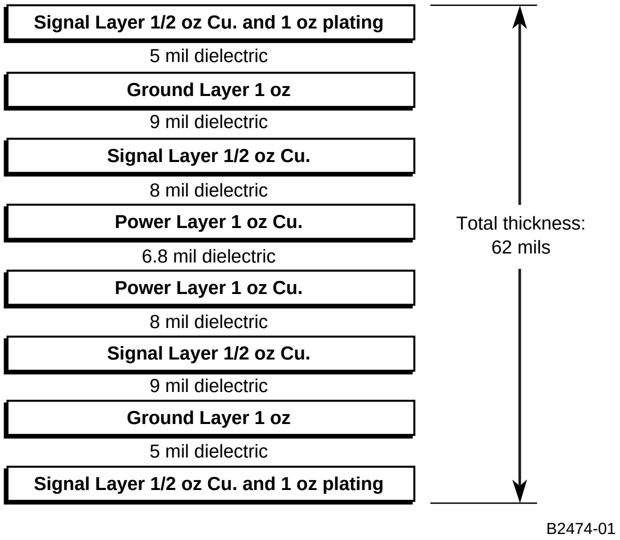
The Intel 815E chipset platform requires a board stack-up yielding a target impedance of 60 Ω ±15 percent with a 5-mil nominal trace width. This requirement is documented in the Low Voltage Intel® Pentium® III Processor with 512K Cache and Ultra Low Voltage Intel Celeron Processor/815E Chipset Platform Design Guides, available from Intel Developer's Web site (http://developer.intel.com/design/chipsets/815e/index.htm). Figure 1 below shows an example of a PCB stack-up that achieves this, as used in a standard micro-ATX form factor customer-reference board. It is a six-layer PCB construction using 53 percent resin FR4 material.

Figure 1. Board Construction Example for 60 Ω Nominal Stack



Due to the limited space on 5.25" boards, one might consider an eight-layer stack-up design. If an eight-layer stack-up design is used, it is recommended that platform designers run through simulations of every interface. An eight-layer design must be able to yield a 60 Ω ±15 percent with a 5 mil nominal trace width as to meet the requirement documented in the design guide. Figure 2 shows an example of a PCB arrangement in eight layers. The PCB layers are arranged so that each signal layer is adjacent to a reference ground plane.

Figure 2. Recommended Eight-Layer Construction for 60 Ω Nominal Stack

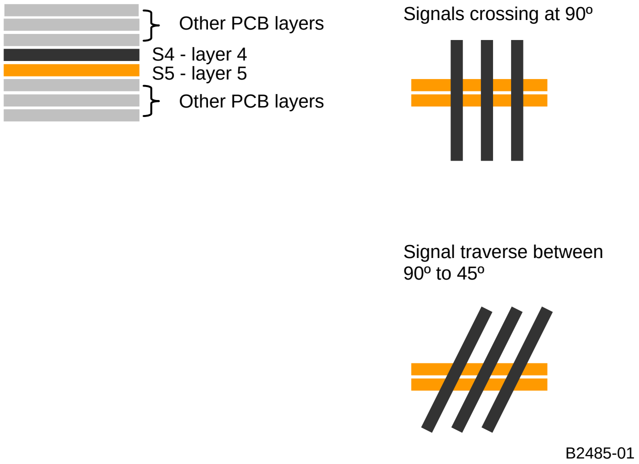


3.0 General Board Layout Guidelines

The Intel 815E platform using Low Voltage/Ultra Low Voltage Intel Celeron processor (400 MHz or 650 MHz) will fit into a 5.25' form factor with an eight-layer stackup provided that there is compliance with all the signal integrity and layout rules. When the signal travels along the trace, the platform must provide an effective signal return path with low inductance. Thus, it is recommended that high-speed signals be routed on the signal layer next to the solid reference ground plane, with no splits or cuts.

Whenever signal layers are beside (adjacent to) each other, the designer must eliminate situations in which traces from one signal layer parallel with traces on its neighboring signal layer to minimize crosstalk between traces on adjacent signal layers. This is true especially on high-speed signals like processor side bus signal traces. Figures 3 and 4 illustrate the correct implementation.

Figure 3. Correct Layout Implementation

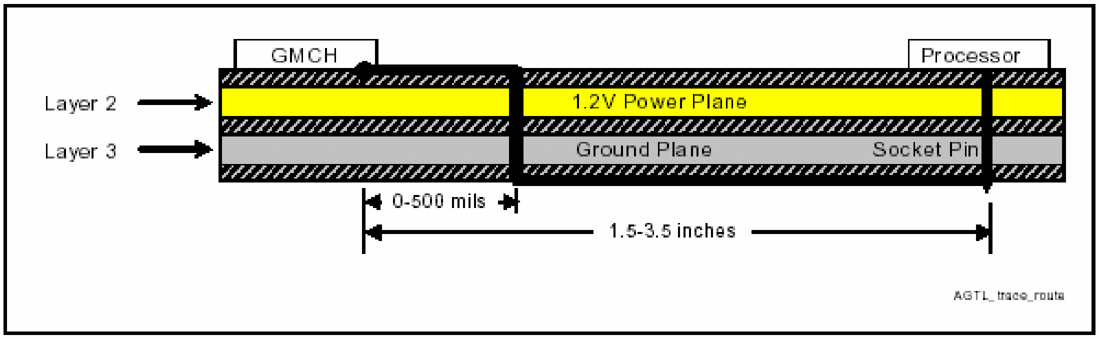


Signal traces traverse correctly between adjacent signal layers. However, it is still recommended to follow eight-layer construction as illustrated in Figure 2 and ensure high-speed signals reference the solid ground plane instead of the power plane, with no splits or cuts

If a signal must go through routing layers, the following recommendations can help improve signal integrity on high-speed signals (see Figure 4).

- For signals going from a ground reference to a power reference, add capacitors between ground and power near the vias to provide an AC return path. Use one capacitor for every three signal lines that change reference layers. Capacitor requirements are as follows: C=100 nF, ESR=80 mΩ, ESL=0.6 nH.
- For signals going from one ground reference to another, separate ground reference, add vias between the two ground planes to provide a better return path.

Figure 4. Routing Recommendation for High-Speed Signals



4.0 Platform Thermal Design Considerations

The Ultra Low Voltage Intel Celeron Processor in the Micro FC-BGA Package Thermal Design Guide describes the processor’s thermal characteristics and provides guidelines for meeting the thermal requirements applicable to embedded applications, including the 5.25” board. This design guide is available at the Intel Developer’s Site

Thermal solutions for the Ultra Low Voltage Intel Celeron Processor are designed to fit within the maximum component height allowed by the PICMG 2.0 Specification, with a maximum allowable heat sink height of 8.89 mm. A properly designed heat sink for the Celeron 400/650 MHz Processor (0.13 micron) can take advantage of natural convection.

Two heat sinks have been designed that meet the required thermal performance for a minimum ambient temperature of 50° C. The heat sinks shown in Figures 5 and 6 were optimized using Computational Fluid Dynamic (CFD) and thermal modeling software. The heat sink designs are optimized for a minimum airflow of 200 LFM, as measured one inch upstream from the processor. The heat sinks can also be applied to natural convection with the proper design.

Heat sink option 1 has been designed to maximize the available space within the keep-out zone. Thermal modeling and verification tests indicate that this heat sink has a junction-to-ambient thermal resistance less than 6.02° C/W with an airflow velocity of 75 LFM. Heat sink option 2 has been optimized to be the smallest size possible within the keep-out zone and using the standard mounting hole pattern. Thermal modeling and verification tests indicate that this heat sink has a junction-to-ambient thermal resistance of less than 6.02° C/W at 100 LFM. More detailed information and the thermal resistances at other airflow rates are available in the thermal design guide.

Figure 5. Heat Sink Option 1: Airflow and Acceptable Orientation to the Processor

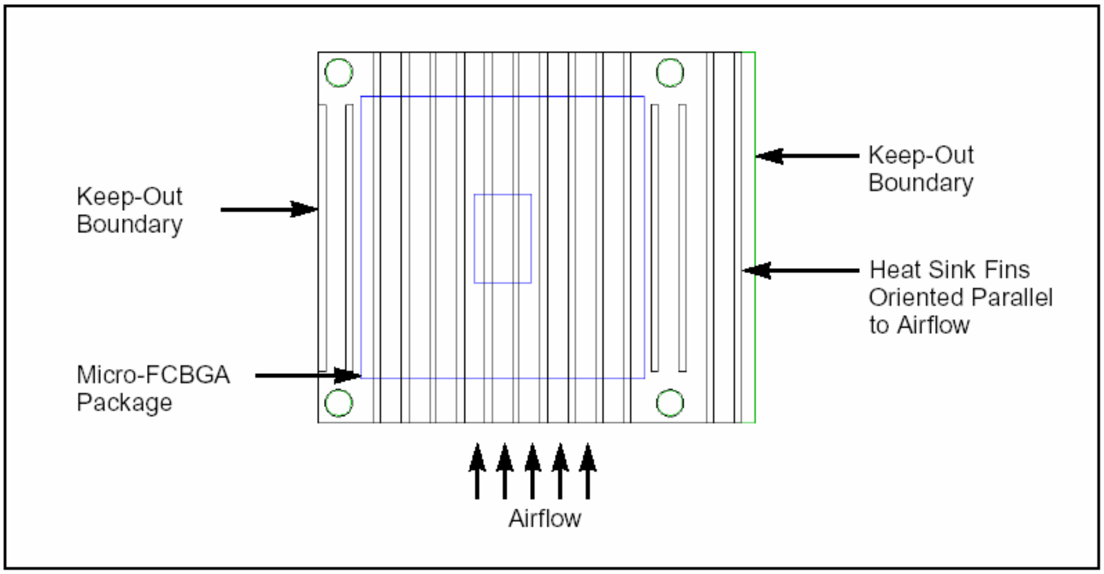
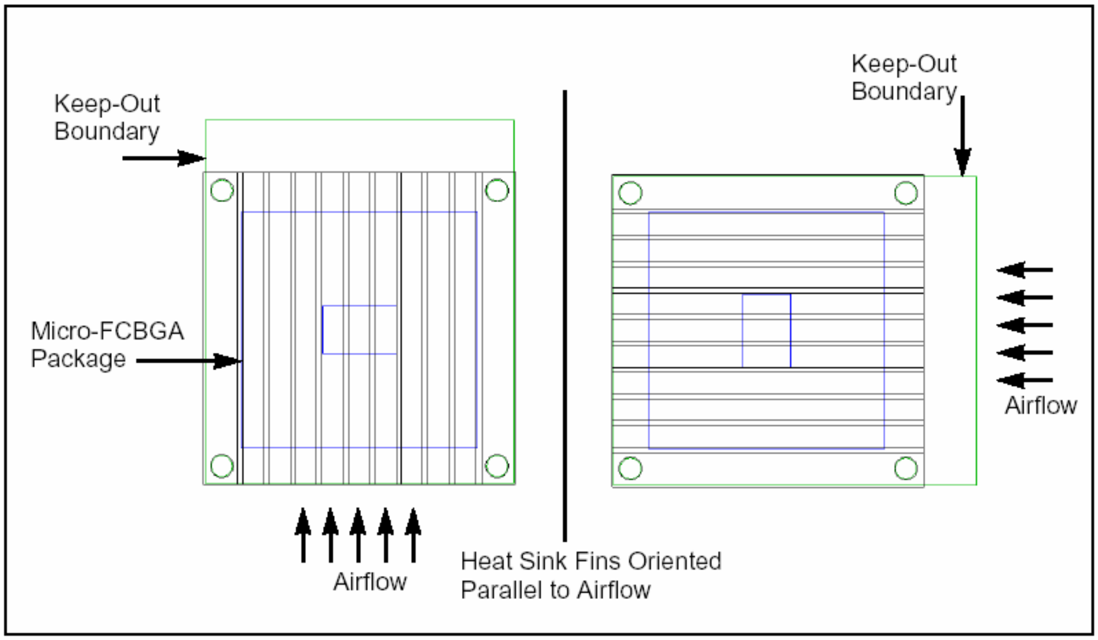


Figure 6. Heat Sink Option 2: Airflow and Acceptable Orientation to the Processor



The geometry is also optimized for high-volume manufacturing. All designs can be manufactured using extrusion and folded fin heat sink manufacturing technologies.

> ***Note:*** The information provided in this document is for reference only, and additional validation must be performed before implementing designs into final production.

Due to the low Thermal Design Power (TDP) associated with these Ultra-Low Voltage Celeron processors (0.13 micron), a natural convection thermal solution is practical. The Ultra-Low Voltage Celeron 400 MHz processor (0.13 micron) in particular is suitable for use in environments where natural convection cooling is needed. The thermal resistance values are reasonable to achieve with a relatively small aluminum heat sink and proper chassis venting. At lower local ambient temperatures, it is more feasible to cool the 400 MHz processor with natural convection. Likewise, at lower ambient temperatures, it may be possible to cool the 650 MHz processor with natural convection cooling as well.

It is important to design the system with a suitable heat sink and venting for natural convection cooled systems. Natural convection cooling refers to the absence of forced airflow from a fan and instead requires adequate system venting to allow for a natural convection effect.

> ***Note:*** The Thermal Design Guide lists vendors of recommended thermal interface material, heat sinks, mounting fasteners, etc.

With the small z-height heat sink and the potential usage of a heat sink under natural convection cooling, the Ultra Low Voltage Intel Celeron processor-based 5.25” board can be used in a space-limited chassis design.