Intel® E7500 and Intel® E7501 Chipsets MCH

Thermal Design Guide for Embedded Applications

March 2003

Order Number: 273819-002

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Revision History

Date	Revision	Description
March 2003	002	Revised Table 3, “Intel® E7500 and Intel® E7501 Chipsets MCH Thermal Specifications.” Revised Table 4, “Theta ja Required versus Device and Configuration.”
November 2002	001	Initial release of this document.

1.0 Introduction

1.1 Document Goals

The objective of thermal management is to ensure that the temperatures of all components in a system are maintained within functional limits. The functional temperature limit is the range within which the electrical circuits may be expected to meet specified performance requirements. Operation outside the functional limit may degrade system performance, cause logic errors, or cause component and/or system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component. The goal of this document is to provide an understanding of the operating limits of the Intel® E7500 and Intel® E7501 chipset MCHs and describe a reference thermal solution for embedded applications.

1.2 Document Scope

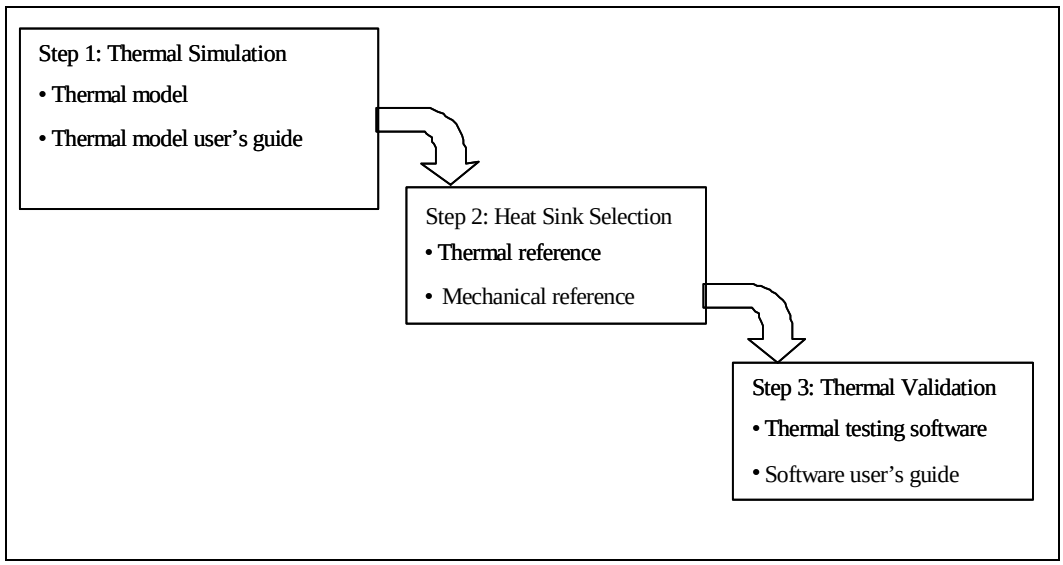
This document addresses thermal design and specifications for the Intel E7500 and Intel E7501 chipset MCH components only. For thermal design information on other chipset components, refer to the respective component thermal design guides. For the Intel® P64H2, refer to the *Intel® PCI-64 Hub 2 (P64H2) Thermal Design Guidelines*.

For general thermal enabling of the Intel E7501 chipset, refer to the *Intel® E7500, Intel® E7501, and Intel® E7505 Chipsets MCH Thermal Design Guidelines.*

1.3 Design Flow

To develop a reliable, cost-effective thermal solution, several tools have been provided to the system designer. Figure 1 shows the design process implicit to this document and the tools appropriate for each step.

Figure 1. Thermal Design Process



1.4 Definition of Terms

Table 1 lists the definitions of terms used in this document.

Table 1. Definition of Terms

Term	Definition
BGA	Ball Grid Array. A package type defined by a resin-fiber substrate, onto which a die is mounted, bonded and encapsulated in molding compound. The primary electrical interface is an array of solder balls attached to the substrate opposite the die and molding compound.
ICH3-S	I/O Controller Hub. The chipset component that contains the primary PCI interface, LPC interface, USB, ATA-100, and other legacy functions.
MBGA	Mini Ball Grid Array. A version of the BGA with a smaller ball pitch.
MCH	Memory Controller Hub. The chipset component that contains the processor interface and the memory interface.
FC-BGA	Flip Chip Ball Grid Array. A packaging technology used for the Intel® E7500 and Intel® E7501 chipset MCHs.
P64H2	Bus Controller Hub. The chipset component that interfaces the PCI-X buses.
$T_{case\text{-}nhs}$	The maximum package case temperature without any package thermal solution. This temperature is measured at the geometric center of the top of the package case.
$T_{die\text{-}nhs}$	The maximum die temperature without any package thermal solution. This temperature is measured at the geometric center of the top of the package die.
$T_{die\text{-}hs}$	The maximum die temperature with the reference thermal solution attached. This temperature is measured at the geometric center of the top of the package die.
TDP	Thermal Design Power. Thermal solutions should be designed to dissipate this target power level.

1.5 Reference Documents

Table 2 lists the reference documents and related document number or source.

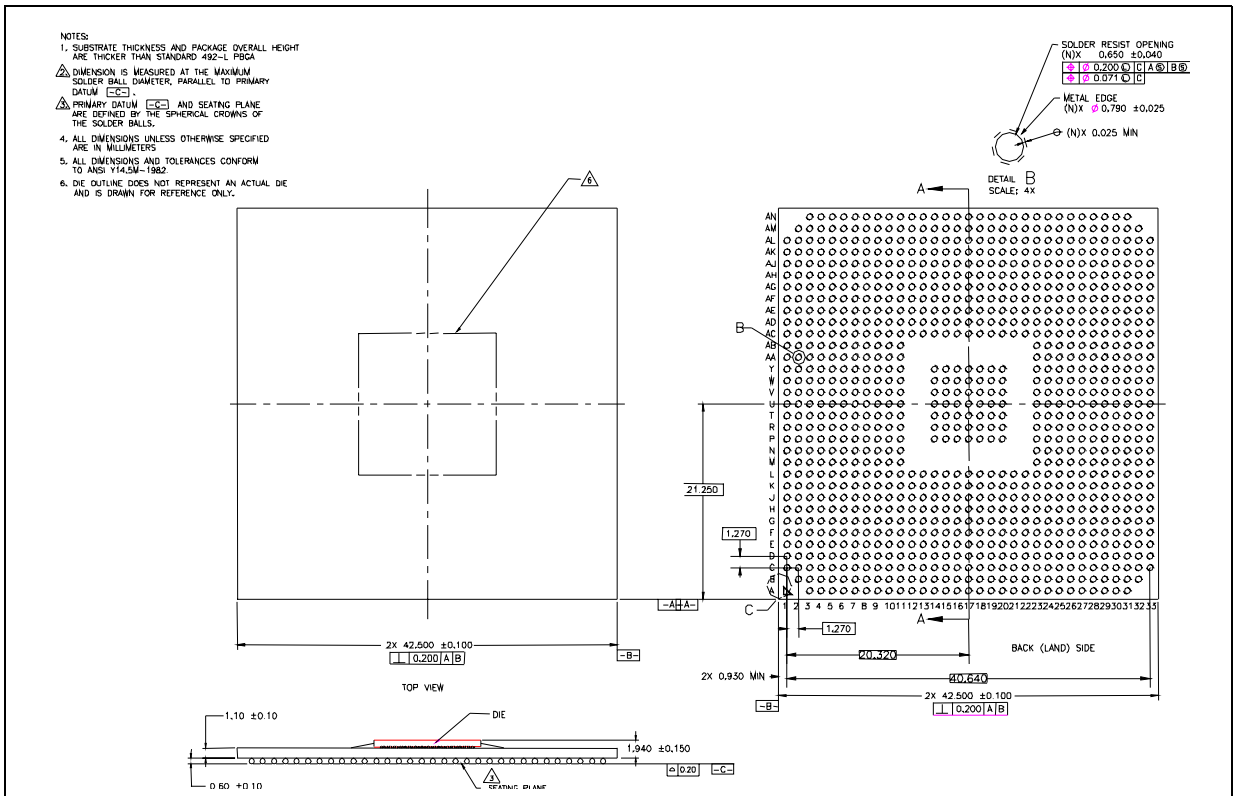
Table 2. Reference Documents

Document	Document Number
Intel® E7500, Intel® E7501, and Intel® E7505 Chipsets MCH Thermal Design Guidelines	298647
Low Voltage Intel® Xeon™ Processor for Embedded Applications Thermal Design Guidelines	273764
Intel® Xeon™ Processor MP Thermal Design Guidelines	298650
Intel® PCI-64 Hub 2 (P64H2) Thermal Design Guidelines	Contact your local Intel Representative
Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet	290733
Intel® E7500 and Intel® E7501 Chipset Flotherm Model and User's Guide*	Contact your local Intel Representative
Thermal Design Suggestions for Various Form Factors	Available at http://www.formfactors.org
Intel® E7500 Chipset MCH Thermal Testing Software	Contact your local Intel Representative
Intel® Xeon™ Processor Thermal Design Guidelines	298348

2.0 Packaging Technology

The Intel® E7500 and Intel® E7501 chipsets consist of three individual components, the memory controller hub (MCH), bus controller hub (P64H2), and I/O controller hub (ICH3-S). The Intel® E7500 and E7501 MCHs utilize a 42.5 mm, 6-layer FC-BGA package shown in Figure 2. Refer to the *Intel® PCI-64 Hub 2 (P64H2) Thermal Design Guidelines* for information on the P64H2 component and to the *Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Datasheet* for information on the ICH3-S component.

Figure 2. Intel® E7500 and Intel® E7501 Chipsets MCH Package Dimensions



NOTE: Dimensions are in mm.

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3.0 Thermal Simulation

Intel provides thermal simulation models of the Intel® E7500 chipset MCH and associated user's guides to aid system designers in simulating, analyzing, and optimizing their thermal solutions in an integrated system-level environment. The models are for use with the commercially available Computational Fluid Dynamics (CFD)-based thermal analysis tool FLOTHERM* (version 3.1 or higher) by Flomerics Inc. Contact your Intel Field Sales representative to order the thermal models and user's guides. The Intel E7500 chipset MCH thermal model may also be used for simulating the Intel E7501 chipset MCH.

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4.0 Thermal Specifications

4.1 Power

See Table 3 for TDP specifications for the Intel® E7500 MCH and the Intel® E7501 chipset MCH. FC-BGA packages have poor heat transfer capability into the board and have minimal thermal capability without thermal solutions. Intel recommends that system designers plan for one or more heat sinks when using the Intel E7500 or Intel E7501 chipset components.

4.2 Die Temperature

To ensure proper operation and reliability of the Intel E7500 and Intel E7501 chipset MCHs, the die temperatures must be at or below the values specified in Table 3. Refer to Section 5.0 for guidelines on accurately measuring package die temperatures.

Table 3. Intel® E7500 and Intel® E7501 Chipsets MCH Thermal Specifications

Device	Parameter (Maximum)	
	T_{die-hs} †	TDP
Intel® E7500 Chipset MCH	102° C	7.5 W
Intel® E7501 Chipset MCH (Paired with Intel® Xeon™ processor or Low Voltage Intel Xeon processor, **dual** channel memory configuration)	105° C	8.5 W
Intel E7501 Chipset MCH (Paired with Intel Xeon processor or Low Voltage Intel Xeon processor, **single** channel memory configuration)	105° C	7.8 W
Intel E7501 Chipset MCH (Paired with Intel® Pentium® M processor, **dual** channel memory configuration)	105° C	7.1 W
Intel E7501 Chipset MCH (Paired with Intel Pentium M processor, **single** channel memory configuration)	105° C	6.2 W

† T_{die-hs} is defined as the maximum die temperature with the reference thermal solution attached.

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5.0 Thermal Metrology

The system designer must obtain temperature measurements in order to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques of measuring chipset MCH die temperatures. Section 5.1 provides guidelines on how to accurately measure the MCH die temperatures. Section 5.2 contains information on running an application program that will emulate anticipated maximum thermal design power. The flowchart in Figure 6 offers useful guidelines for thermal performance and evaluation.

5.1 Die Temperature Measurements

To ensure functionality and reliability, the chipset MCH is specified for proper operation when T_{die} is maintained at or below its respective maximum temperature listed in Table 3. The surface temperature at the geometric center of the die corresponds to T_{die}. Measuring T_{die} requires special care to ensure an accurate temperature measurement.

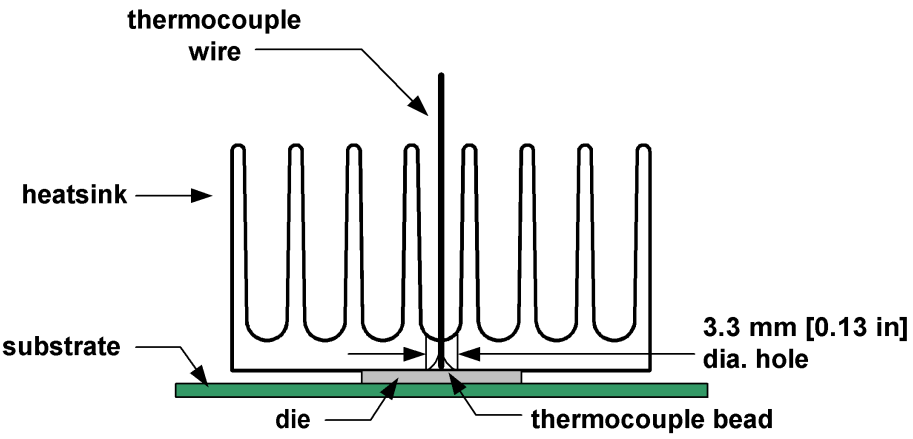
Temperature differences between the temperature of a surface and the surrounding local ambient air may introduce error in the measurements. The measurement errors may be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, or contact between the thermocouple cement and the heat sink base (when a heat sink is used). To minimize these measurement errors, the following approaches are recommended for thermocouple attach.

5.1.1 90° Angle Attach Methodology

1. Use 36-gauge or smaller diameter K-type thermocouples.
2. Ensure that the thermocouple has been properly calibrated.
3. Attach the thermocouple bead or junction to the top surface of the die in the center using a high thermal conductivity cement. **It is critical that the thermocouple bead makes contact with the die.**
4. The thermocouple should be attached at a 90° angle when no interference exists between the thermocouple wire and retention mechanism (see Figure 3). This is the preferred method and is recommended for use with both bare packages as well as packages employing a thermal solution.
5. The hole size through the heat sink base to route the thermocouple wires out should be smaller than 3.3 mm [0.13 in] in diameter.
6. Make sure no contact exists between the thermocouple cement and heat sink base. This contact will affect the thermocouple reading.

Figure 3 shows the 90° angle attach methodology.

Figure 3. 90° Angle Attach Methodology



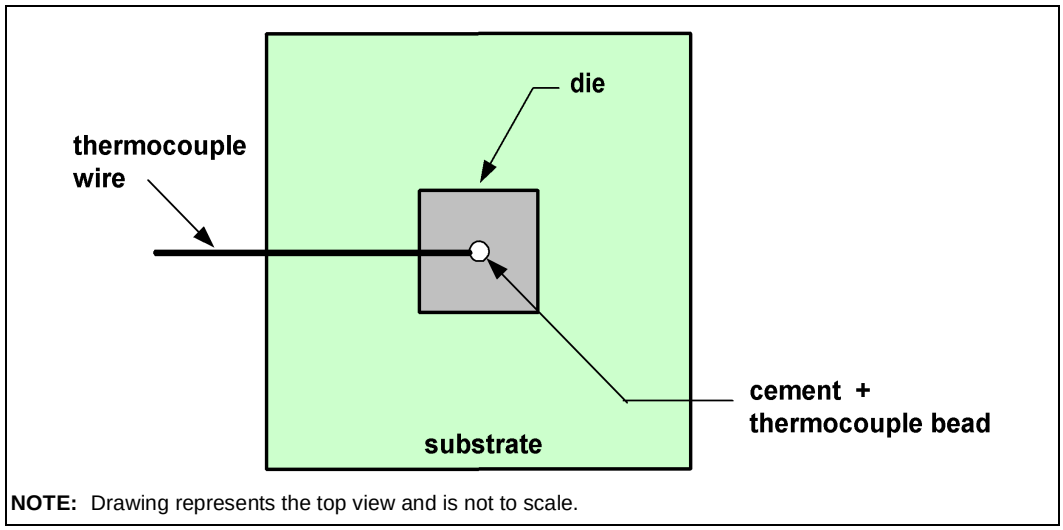
NOTE: Drawing is not to scale.

5.1.2 0° Angle Attach Methodology

1. Mill a 3.3-mm [0.13 in] diameter hole centered on bottom of the heat sink base. The milled hole should be approximately 1.5 mm [0.06 in] deep.
2. Mill a 1.3 mm [0.05 in] wide slot, 0.5 mm [0.02 in] deep, from the centered hole to one edge of the heat sink. The slot should be in the direction parallel to the heat sink fins (see Figure 5).
3. Attach thermal interface material (TIM) to the bottom of the heat sink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heat sink base.
5. Attach a 36-gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, make sure no contact is present between the thermocouple cement and the heat sink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see Figure 4).
6. Attach heat sink assembly to the MCH, and route thermocouple wires out through the milled slot.

Figure 4 shows the 0° angle attach methodology.

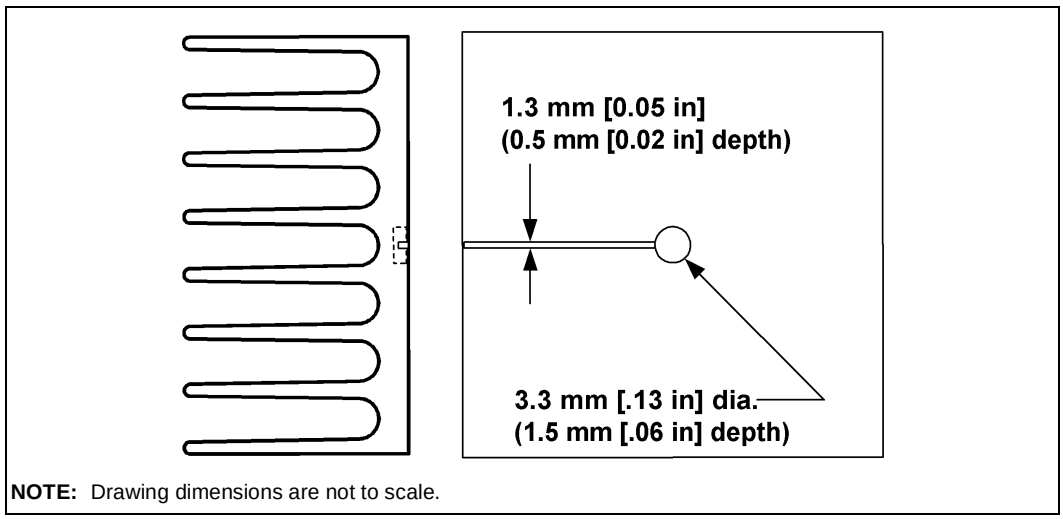
Figure 4. 0° Angle Attach Methodology



NOTE: Drawing represents the top view and is not to scale.

Figure 5 shows the 0° angle attach heat sink modifications.

Figure 5. 0° Angle Attach Heat Sink Modifications



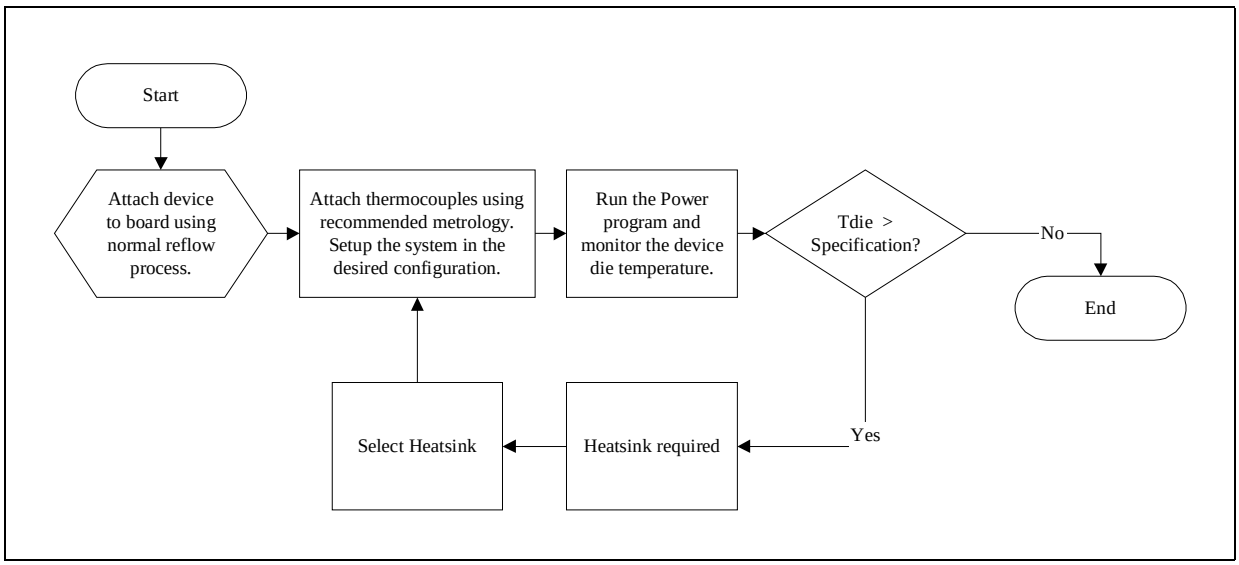
NOTE: Drawing dimensions are not to scale.

5.2 Power Simulation Software

The power simulation software is a utility designed to dissipate the thermal design power on an Intel® E7501 chipset MCH when used in conjunction with Intel® Xeon™ processor(s) with 512 Kbytes L2 cache or a Low Voltage Intel® Xeon™ processor with 512 Kbytes L2 cache. To assess the thermal performance of the chipset MCH thermal solution under "worst-case realistic application" conditions, Intel has developed a software utility that operates the chipset at near worst-case power dissipation.

The utility has been developed solely for testing customer thermal solutions at near the thermal design power. Figure 6 shows a decision flowchart for determining thermal solution needs. Real future applications may exceed the thermal design power limit for transient time periods. For power supply current requirements under these transient conditions, please refer to each component's EDS or EDS Addendum for the I_{CC} (Max Power Supply Current) specification. Contact your Intel Field Sales representative to obtain a copy of this software.

Figure 6. Thermal Solution Decision Flowchart



6.0 Reference Thermal Solution

Intel has developed a reference thermal solution designed to meet the cooling needs of the Intel® E7500 and Intel® E7501 chipset MCHs at worst-case embedded conditions. This section describes the overall requirements for the reference thermal solution, including critical-to-function dimensions, operating environment, and validation criteria. Other chipset components may or may not need attached thermal solutions, depending on your specific system local-ambient operating conditions. Refer to the *Intel® PCI-64 Hub 2 (P64H2) Thermal Design Guidelines* and *Intel® I/O Controller Hub 4 (ICH4) Thermal Design Guidelines* for information on thermal solution requirements and reference thermal solutions.

6.1 Operating Environment and Thermal Performance

The reference thermal solution was designed assuming a maximum local-ambient temperature of 55° C with a minimum airflow velocity directly upstream of the heatsink of 50 LFM. Assuming these boundary conditions are met, the reference thermal solution will meet the thermal specifications for the Intel E7500 and Intel E7501 chipset MCHs in all memory and Hub Interface configurations. See Figure 7 for a plot of the theta ja versus airflow for the reference heatsink design, and Table 4 for the required theta ja heatsink performances for the Intel E7500 and Intel E7501 chipset MCHs.

The reference thermal solution provides enough thermal capability to meet the required theta ja for all of the configurations listed in Table 4 with 50 LFM airflow.

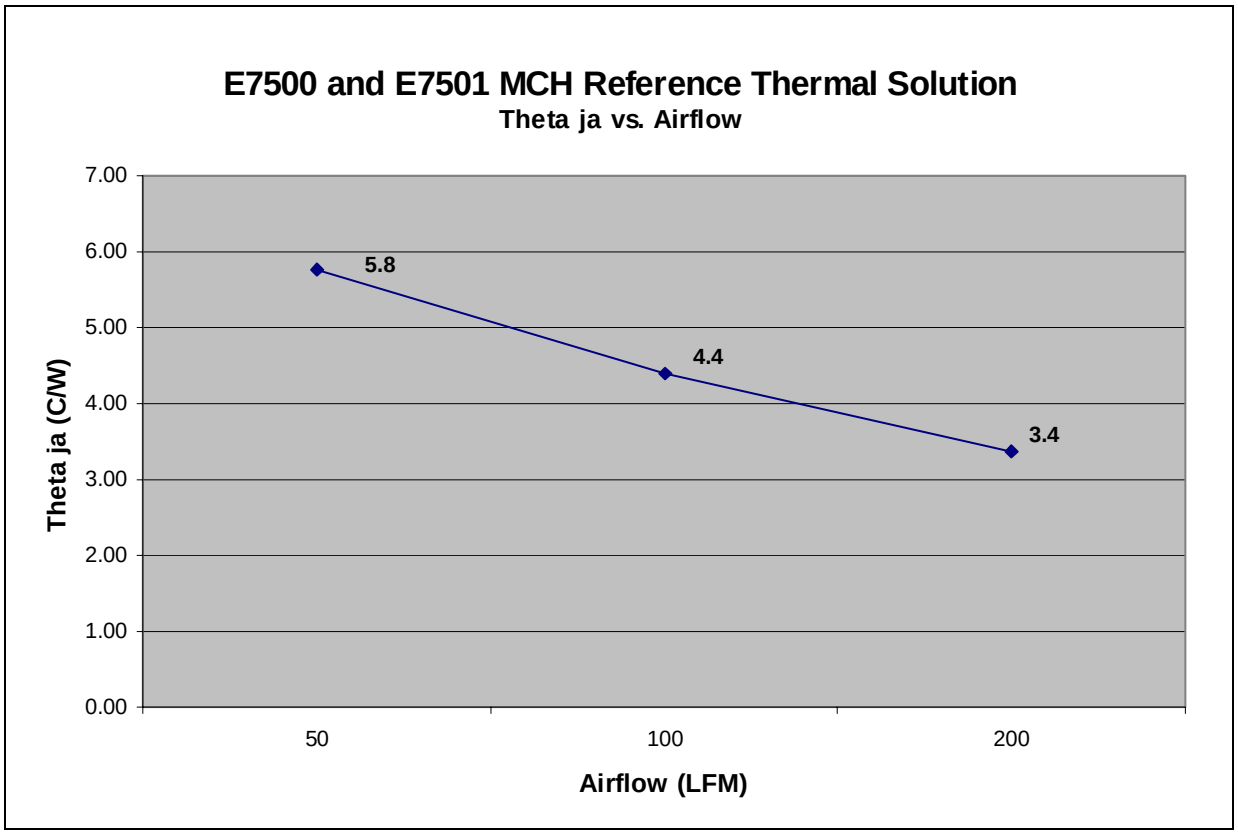
Table 4. Theta ja Required versus Device and Configuration

Device	Theta ja Max (° C/W) at T_{LA} = 55° C
Intel® E7500 Chipset MCH	6.27° C/W
Intel® E7501 Chipset MCH (Paired with Intel® Xeon™ processor or Low Voltage Intel Xeon processor, **dual** channel memory configuration)	5.88° C/W
Intel E7501 Chipset MCH (Paired with Intel Xeon processor or Low Voltage Intel Xeon processor, **single** channel memory configuration)	6.41° C/W
Intel E7501 Chipset MCH (Paired with Intel® Pentium® M processor, **dual** channel memory configuration)	7.04° C/W
Intel E7501 Chipset MCH (Paired with Intel Pentium M processor, **single** channel memory configuration)	8.06° C/W

† T_{LA} is defined as the local (internal) ambient temperature directly upstream of the chipset.

Figure 7 shows the theta ja versus airflow for the reference thermal solution.

Figure 7. Theta ja versus Airflow for the Reference Thermal Solution



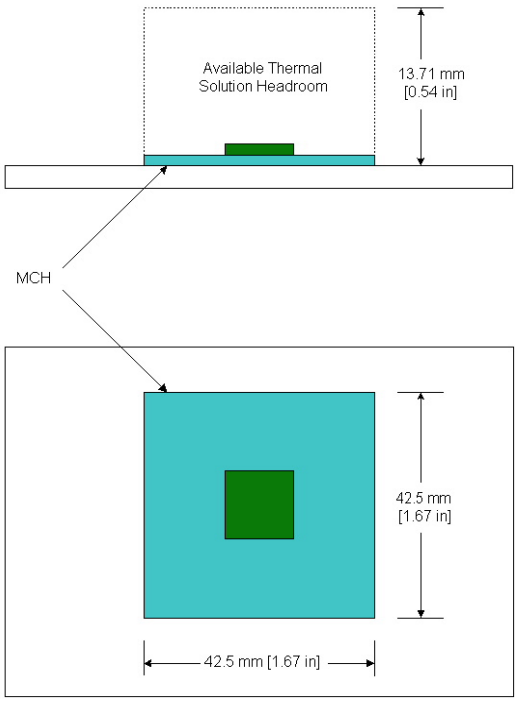
6.2 Mechanical Design Envelope

Though each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the Intel E7500 chipset and Intel E7501 chipset MCHs in embedded environments are shown in Figure 8. These constraints assume the use of the CompactPCI* blade form factor.

When using heat sinks that extend beyond the MCH reference heat sink envelope shown in Figure 8, any motherboard components placed between the underside of the heat sink and motherboard cannot exceed 2.286 mm [0.090 in] in height.

Figure 8 shows the reference heat sink volumetric envelope for the MCH.

Figure 8. Reference Heat Sink Volumetric Envelope for the MCH



NOTE: Drawing dimensions are not to scale.

6.3 Thermal Solution Assembly

The reference thermal solution is a passive extruded heat sink with thermal and mechanical interfaces. There are two methods for attaching the heat sink to the motherboard. The first method (Retention Method A) uses a clip with each end hooked through an anchor soldered to the board. The second method (Retention Method B) employs the use of four push-pins through the board using the four holes provided on the heat sink. This method might face layout constraints as the four holes through the motherboard must be accounted for during board layout. Full mechanical drawings of the thermal solution assembly and the heat sink clip may be found in Appendix B, "Mechanical Drawings."

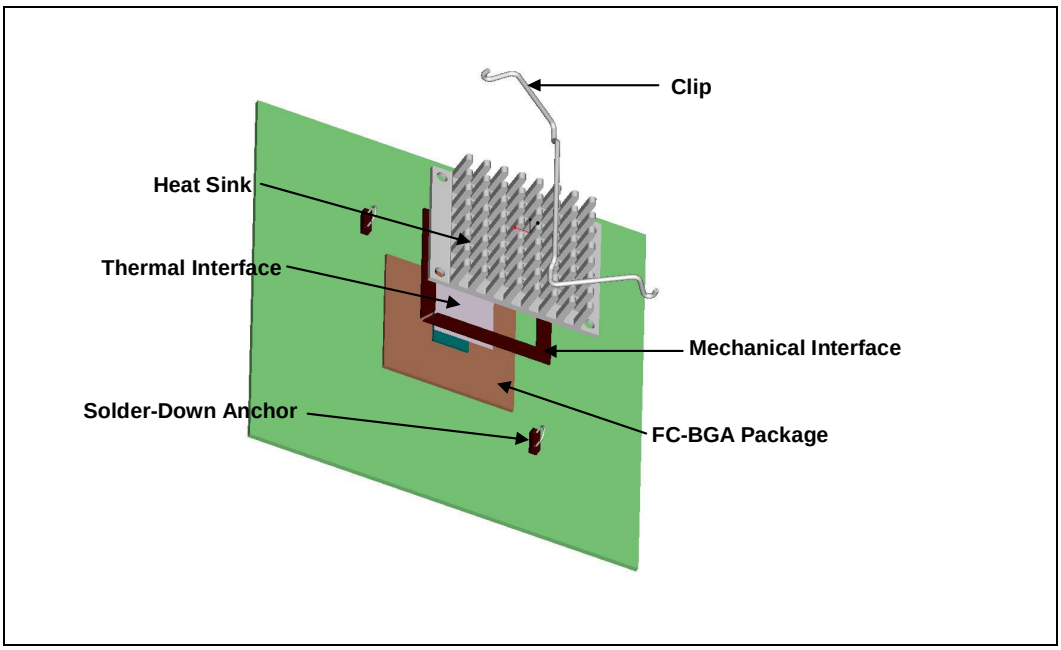
Appendix A, "Thermal Solution Component Suppliers" lists the Bill-of-Materials and vendor information for each thermal solution component.

6.3.1 Retention Method A

Retention Method A employs the use of a clip and two solder-down through board anchors for mechanical retention. This method is preferred when layout constraints hamper the use of Retention Method B.

Figure 9 shows the reference thermal solution assembly using Retention Method A.

Figure 9. Reference Thermal Solution Assembly Using Retention Method A



6.3.1.1 Heat Sink Orientations

When using Retention Method A, the heat sink must be aligned as shown in Figure 9. The heat sink holes on the same side of the heat sink must be parallel with the clip that applies pressure through the center of the heat sink.

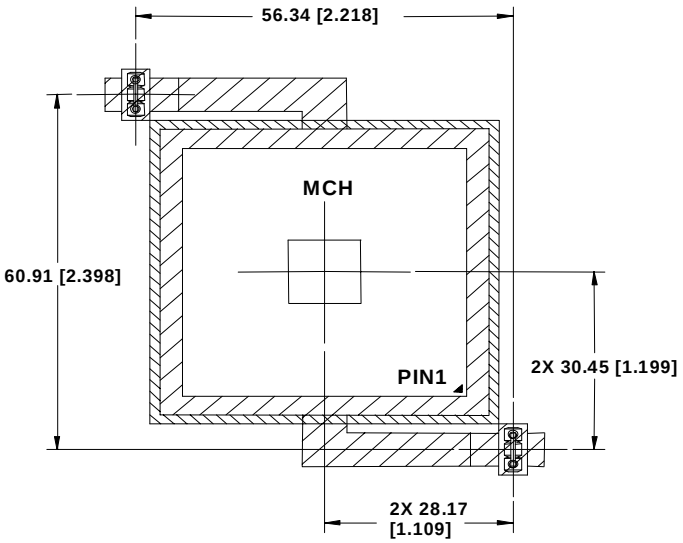
The airflow may approach the heat sink from either perpendicular direction. Aligning the heat sink 45° relative to the airflow is acceptable but delivers reduced thermal performance.

6.3.1.2 Board Level Keep-out Dimensions

The locations of hole patterns and keep-out zones for the reference thermal solution are shown in Figure 10 and Figure 11.

Figure 10 shows the heat sink retention mechanism layout for Retention Method A.

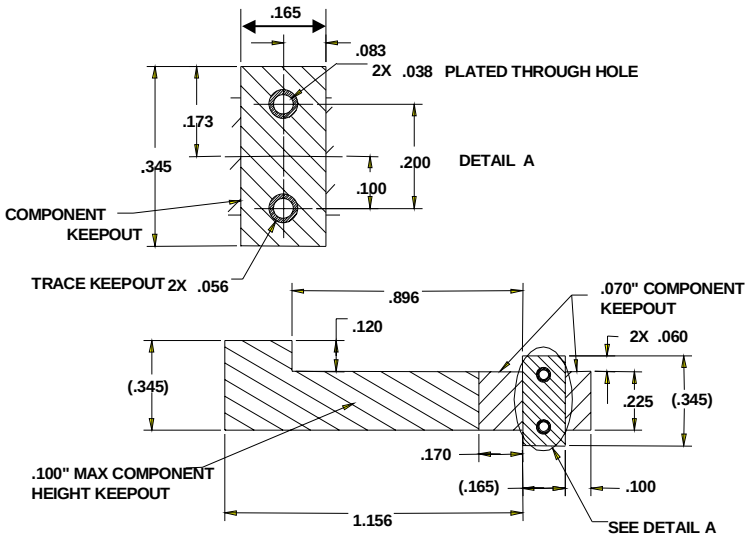
Figure 10. Heat Sink Retention Mechanism Layout for Retention Method A



NOTE: Drawing dimensions are in millimeters [in] and are not to scale.

Figure 11 shows the retention mechanism component keep-out zones for Retention Method A.

Figure 11. Retention Mechanism Component Keep-out Zones for Retention Method A



NOTE: Drawing dimensions are in inches and are not to scale.

6.3.1.3 Heat Sink Clip

Retention Method A employs the use of a wire clip with hooked ends. The hooks attach to anchors to fasten the clip to the board. See Figure 16 in Appendix B, "Mechanical Drawings" for a mechanical drawing of the clip.

6.3.1.4 Solder-Down Anchors

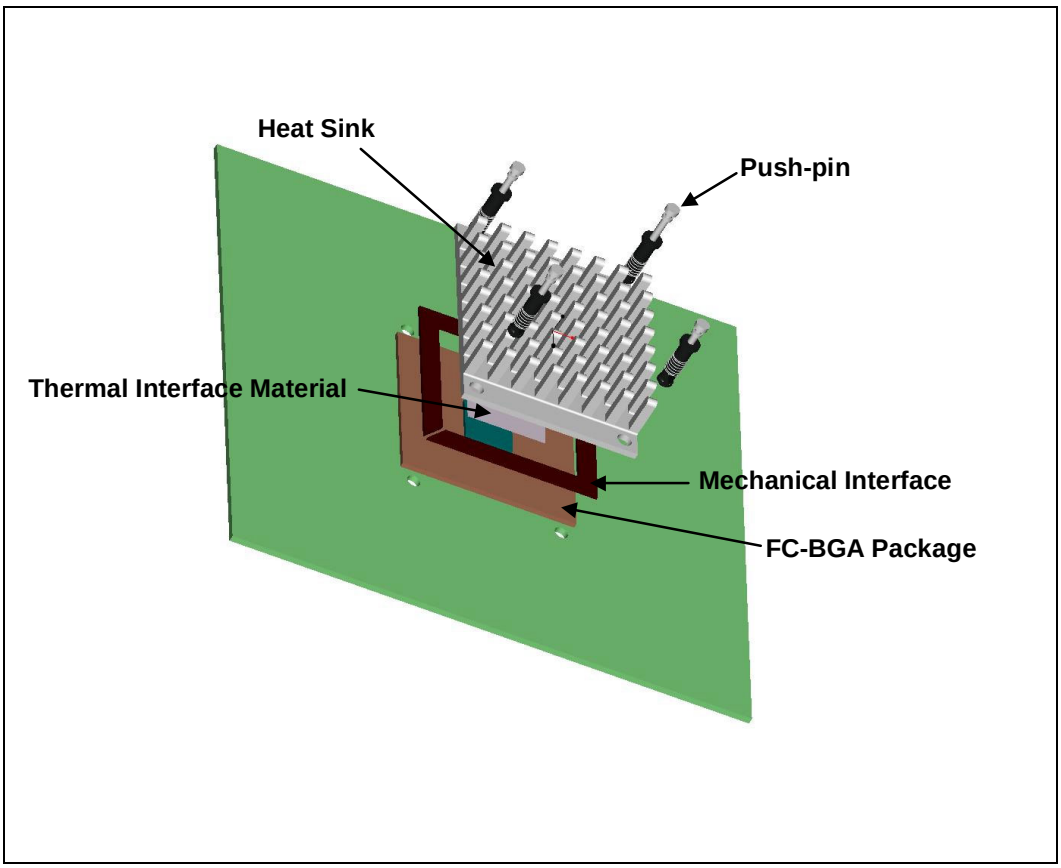
For platforms that have very limited board space, a clip retention solder-down anchor has been developed to minimize the impact of clip retention on the board. It is based on a standard three-pin jumper and is soldered to the board like any common through-hole header. A new anchor design is available with 45° bent leads to increase the anchor attach reliability over time. See Appendix A, "Thermal Solution Component Suppliers" for the part number and supplier information.

6.3.2 Retention Method B

Retention Method B employs the use of four push-pins mounted through the four holes on the heat sink and the motherboard. This method requires advance layout notification for the four through holes on the motherboard.

Figure 12 shows the reference thermal solution assembly using Retention Method B.

Figure 12. Reference Thermal Solution Assembly Using Retention Method B



6.3.2.1 Heat Sink Orientations

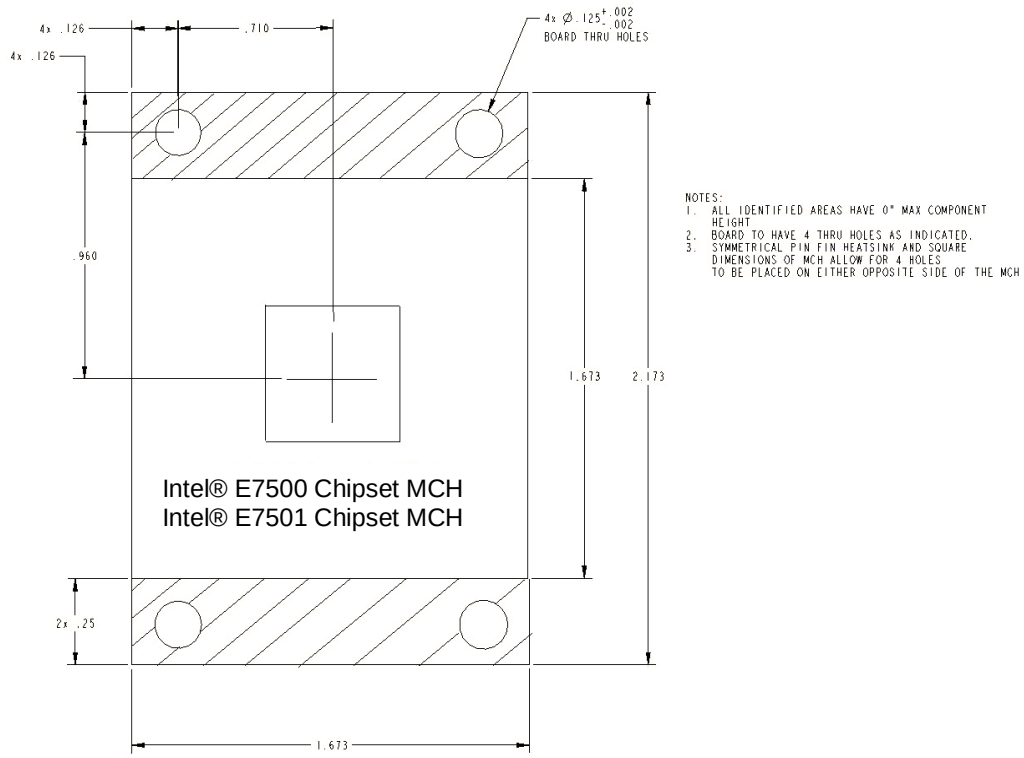
Retention Method B supports an omni-directional placement for the heat sink. Airflow may pass either perpendicular direction over the fins and the heat sink may be mounted in either the vertical or horizontal position atop the MCH, depending on hole placement.

Aligning the heat sink 45° relative to the airflow is acceptable but delivers reduced thermal performance.

6.3.2.2 Board Level Keep-Out Dimensions

Figure 13 shows the board component keep-out for Retention Method B.

Figure 13. Board Component Keep-out for Retention Method B



NOTE: Drawing dimensions are in inches and are not to scale.

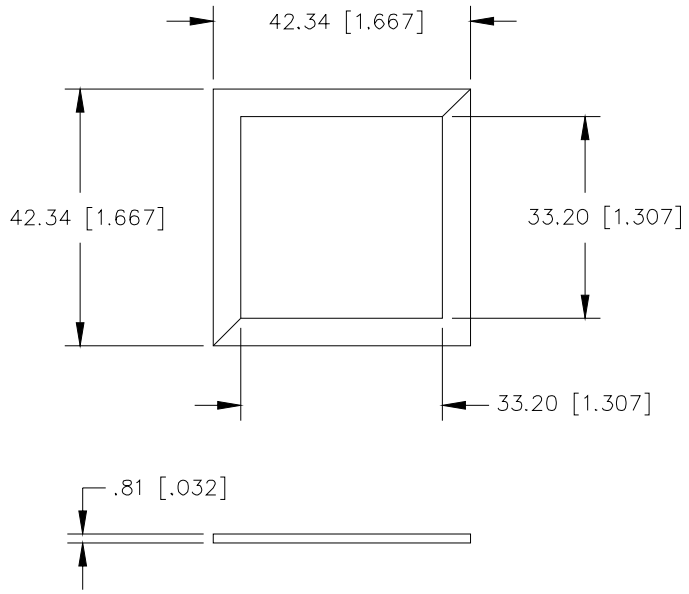
6.3.2.3 Heat Sink Push-Pin

Four push-pins are required to implement Retention Method B. Vendor information and a detailed mechanical drawing are located in Appendix B. Currently, the push-pin is available for 0.096 inch thick motherboards. Other size motherboards might require custom parts from the vendor.

6.3.3 Mechanical Interface Material

Intel recommends the use of a mechanical interface material to avoid cracking of the exposed die under loading. The interface material reduces mechanical loads experienced by the die. The reference thermal solution uses a picture frame gasket of 0.813 mm [0.032 in] thick Poron* foam. The foam gasket is a two-piece design, with diagonal cuts at two corners, as shown in Figure 14. A one-piece gasket design may be used instead without any impact to mechanical performance.

Figure 14. Heat Sink Mechanical Gasket, Optional Two-Piece



NOTE: Drawing dimensions are in millimeters [in] and are not to scale.

6.3.4 Thermal Interface Material

A thermal interface material provides improved conductivity between the die and heat sink. The reference thermal solution is delivered with Powerstrate 51* (manufactured by Power Devices, Inc.) phase change material attached.

6.4 Reliability Requirements

Each motherboard, heat sink, and attach combination may vary the mechanical loading of the component. The user should carefully evaluate the reliability of the completed assembly prior to use in high volume. Some general recommendations are presented in Table 5.

Table 5. Reliability Requirements

Test[1]	Requirement	Pass/Fail Criteria[2]
Mechanical Shock	50 g, board level, 11 msec, 3 shocks/axis	Visual Check and Electrical Functional Test
Random Vibration	7.3 g, board level, 45 min/axis, 50 Hz to 2000 Hz	Visual Check and Electrical Functional Test
Temperature Life	85° C, 2000 hours total, checkpoints at 168, 500, 1000, and 2000 hours	Visual Check
Thermal Cycling	-5° C to +70° C, 500 cycles	Visual Check
Humidity	85% relative humidity, 55° C, 1000 hours	Visual Check

NOTES:
1. The above tests should be performed on a sample size of at least 12 assemblies from three lots of material.
2. Additional Pass/Fail Criteria may be added at the discretion of the user.

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7.0 Conclusion

As the complexity of computer systems increases, so do the power dissipation requirements. Care must be taken to ensure that the additional power is properly dissipated. Heat may be dissipated using improved system cooling, selective use of ducting, and/or passive heat sinks.

The simplest and most cost effective method is to improve the inherent system cooling characteristics through careful design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heat sink may be varied to balance size and space constraints with acoustic noise.

This document has presented the conditions and requirements to properly design a cooling solution for systems implementing Intel® E7500 or Intel® E7501 chipsets in an embedded application. Properly designed solutions provide adequate cooling to maintain the chipset die temperatures at or below thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the chipset MCH die temperature at or below those recommended in this document, a system designer may ensure the proper functionality, performance, and reliability of these chipsets.

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Appendix A Thermal Solution Component Suppliers

A.1 Extruded Pin Fin Heat Sink

Part	Supplier (Part Number)	Contact Information
Pin Fin Heat Sink (Includes heat sink and attached thermal interface material)	CoolerMaster (ECB-00028-01)	Wendy Lin 886-2-3434-0050, x333 wendy@coolermaster.com.tw

A.2 Materials for Retention Method A

Part	Qty Required (per assy)	Intel Part Number	Supplier	Contact Information
Heatsink Clip	1	A69230-001	CCI/ACK	Harry Lin 714-739-5797 hlinack@aol.com
			Foxconn	Bob Hall 503-693-3509 x235 bhall@foxconn.com
Board Mount Solder-Down Anchors (Two anchors required per heat sink.)	2	A13494-005	Foxconn	Julia Jiang (408) 919-6178 juliaj@foxconn.com

A.3 Materials for Retention Method B

Part	Supplier (Part Number)	Contact Information
Push-Pin	Peninsula Components (PL 1674)	Steve Blank (562) 694-4477 steve@pencomsf.com

NOTE: Four push-pins are required per heat sink.

A.4 Attach Hardware

Part	Intel Part Number	Supplier	Contact Information
Thermal Interface (Powerstrate 51*)	--	Power Devices, Inc.	Mike McPherson 916-686-1432 Mike.McPherson@loctite.com
Mechanical Interface (Poron*)	A69141-001	Boyd	Rhoda Kennedy 503-972-3170 rkennedy@boydcorp.com

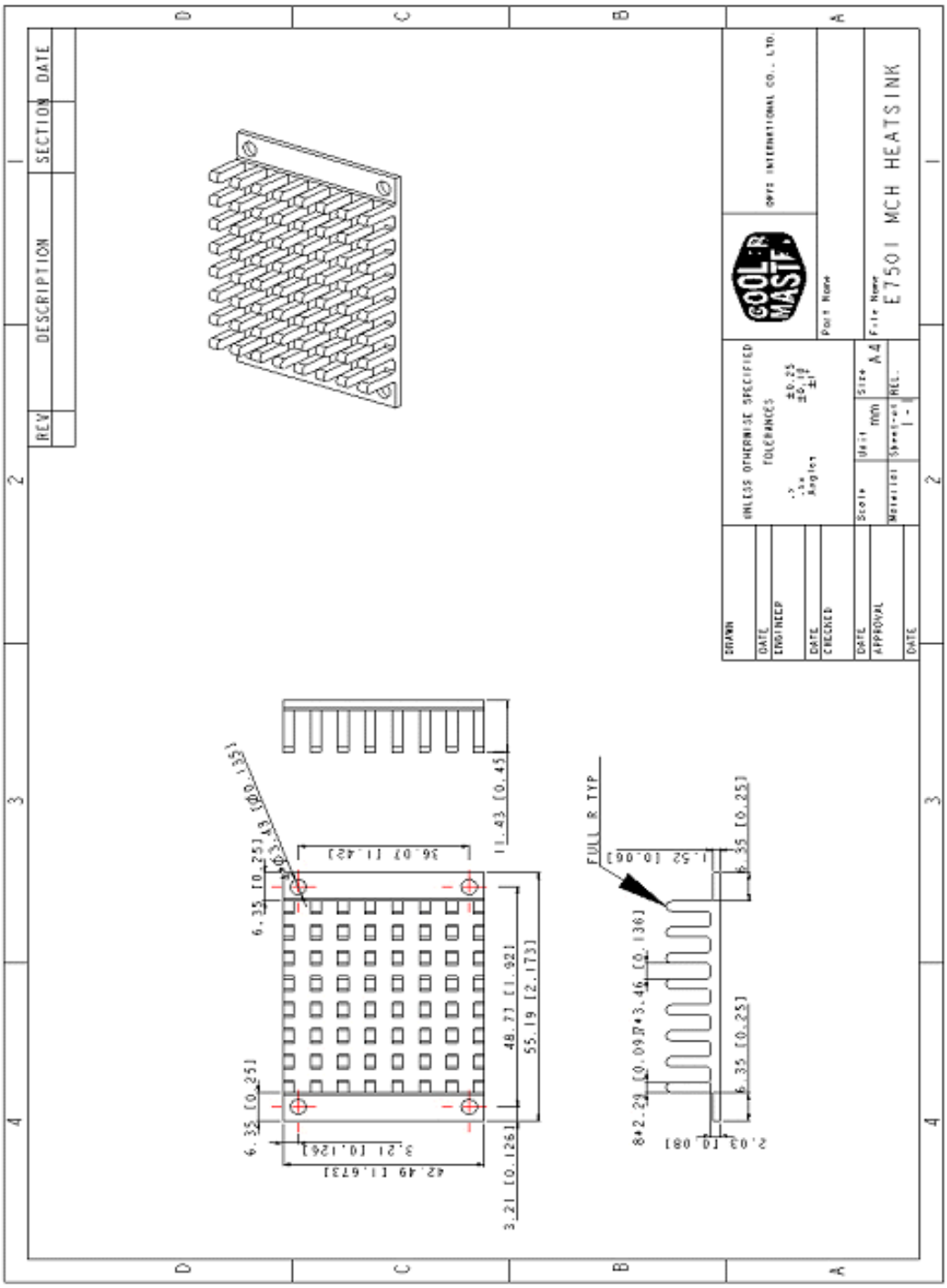
Note: The enabled components may not be currently available from all suppliers. Contact the supplier directly to verify time of component availability.

Appendix B Mechanical Drawings

Table 6 lists the mechanical drawings included in this section.

Table 6. Mechanical Drawing List

Figure 15. MCH Heat Sink



Used by permission.

Figure 16. Heat Sink Clip

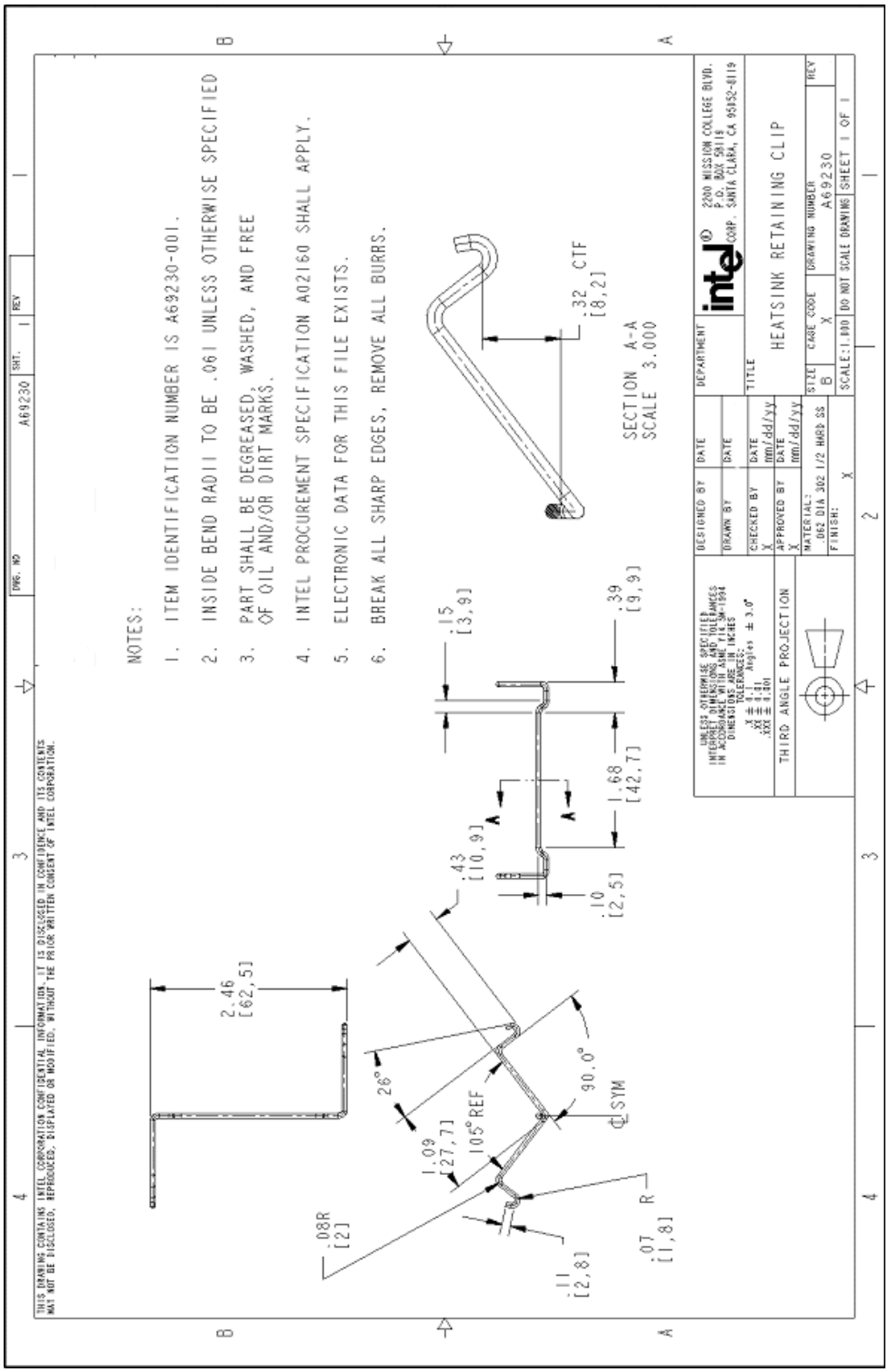
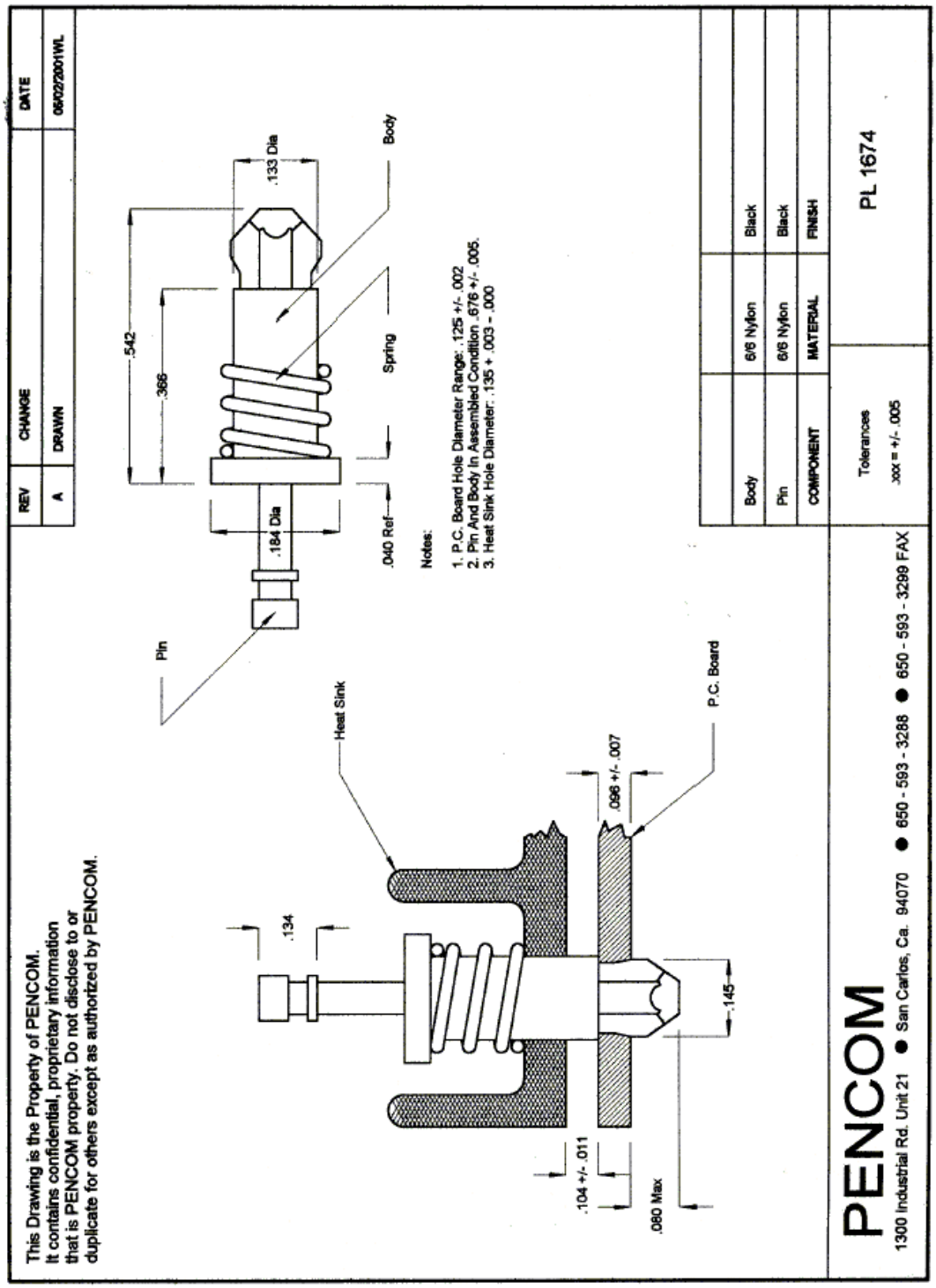


Figure 17. Push-pin



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