# Intel® Pentium® 4 Processor in 478-pin Package and Intel® 845E Chipset Platform for DDR

## Design Guide

*August 2004*

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# Revision History

| Revision | Description | Date |
|---|---|---|
| -001 | • Initial Release. | May 2002 |
| -002 | • Updated ICH4 section | August 2004 |

# 1 Introduction

In this document "processor" and "Intel® Pentium® 4 processor" refer to the Pentium 4 processor in the 478 pin package.

This design guide documents Intel's design recommendations for systems based on the Pentium 4 processor and the Intel® 845E chipset. Design issues such as thermal considerations should be addressed using specific design guides or application notes for the processor or 845E chipset.

These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of the two following categories.

- *Design Recommendations* are items based on Intel's simulations and lab experience to date and are strongly recommended, if not necessary, to meet timing and signal quality specifications.
- *Design Considerations* are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They should be used as examples, but may not be applicable to particular designs.

***Note:*** The guidelines recommended in this document are based on experience and preliminary simulation work performed at Intel while developing Pentium 4 processor and 845E chipset based systems. This work is ongoing, and the recommendations and considerations are subject to change.

Platform schematics are provided in *Appendix A, Customer Reference Board Schematics*. The schematics are a reference for board designers. While the schematics may cover a specific design, the core schematics will remain the same for most platforms. The schematic set provides a reference schematic for each platform component as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components.

## 1.1 Related Documentation

Reference the following documents or models for more information. All Intel issued documentation revision numbers are subject to change, and the latest revision should be used. The specific revision numbers referenced should be used for all documents not released by Intel. Contact the field representative for information on how to obtain Intel issued documentation.

| Document | Document Source |
|---|---|
| *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet* | http://www.intel.com/design/pentium4/datashts/249887.htm |
| *Intel® Pentium® 4 Processor in the 478 Pin Package Thermal Design Guidelines* | http://www.intel.com/design/pentium4/guides/249889.htm |
| *Intel® 845E Chipset: Intel® 82845 Memory Controller Hub (MCH) for DDR Datasheet* | http://www.intel.com/design/chipsets/datashts/290742.htm |
| *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet* | http://www.intel.com/design/chipsets/datashts/290744.htm |
| *Intel® 845 Chipset Thermal and Mechanical Design Guidelines* | http://www.intel.com/design/chipsets/designex/298586.htm |
| *Intel® Pentium® 4 Processor in the 478 pin package Processor Signal Integrity Models* | Contact your Intel Field Representative |
| *Intel® Pentium® 4 Processor VR Down Design Guidelines* | http://www.intel.com/design/Pentium4/guides/249891.htm |
| *mPGA478 Socket Design Guidelines* | http://www.intel.com/design/pentium4/guides/249890.htm |
| *Accelerated Graphics Port Interface Specification Rev 2.0* | http://www.agpforum.org/ |
| *Low Pin Count Interface Specification Rev 1.0* | http://www.intel.com/design/chipsets/industry/lpc.htm |
| *PCI Local Bus Specification Rev. 2.2* | www.pcisig.com |
| *PCI-PCI Bridge Specification Rev. 1.0* | www.pcisig.com |
| *PCI Bus Power Management Interface Specification Rev. 1.0* | www.pcisig.com |
| *Universal Serial Bus Revision 2.0 Specification* | http://www.usb.org/developers/docs.html |
| *Advanced Configuration and Power Interface Specification (ACPI) Rev. 1.0b* | http://www.teleport.com/~acpi/ |
| *Audio Codec 97 Component Specification Revision 2.3* | http://developer.intel.com/ial/scalableplatforms/audio/index.htm#97spec/ |
| *PC'01 Specification* | www.microsoft.com |
| *PC 99 System Design Guide, Revision 1.0* | http://www.microsoft.com/hwdev/pc99.htm |
| *ITP700 Debug Port Design Guide* | http://developer.intel.com/design/pentium4/guides/249679.htm |
| *82562ET Platform LAN Connect (PLC) Networking Silicon Advance Information Datasheet* | |

| Document | Document Source |
|---|---|
| *82562EM Platform LAN Connect (PLC) Networking Silicon Advance Information Datasheet* | Contact Intel Field Representative |
| *Communication and Networking Riser (CNR) Specification Revision 1.2* | http://www.intel.com/labs/media/audio/#cnr |
| *82562ET 10/100 Mbps Platform LAN Connect (PLC) Product Preview Datasheet* | Contact Intel Field Representative |
| *82562ET LAN on Motherboard Design Guide (AP-414)* | Contact Intel Field Representative |
| *82562ET/EM PCB Design Platform LAN Connect (AP-412)* | Contact Intel Field Representative |
| *CNR Reference Design Application Note (AP-418)* | Contact Intel Field Representative |

## 1.2 Conventions and Terminology

This section defines conventions and terminology that are used throughout this document.

**Table 1-1. Conventions and Terminology**

| Convention/ Terminology | Definition |
|---|---|
| Aggressor | A network that transmits a coupled signal to another network is called the aggressor network. |
| AGTL+ | The processor System Bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors that provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers by the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition. |
| Bus Agent | A component or group of components that, when combined, represent a single load on the AGTL+ bus. |
| Corner | Describes how a component performs when all parameters that could impact performance are adjusted simultaneously to have the best or worst impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. Performance of an electronic component may change as a result of (including, but not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the “slow” corner means having a component operating at its slowest, weakest drive strength performance. Similar discussion of the “fast” corner means having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance. |

| Convention/ Terminology | Definition |
|---|---|
| Crosstalk | The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks.<br><br>Backward Crosstalk—coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal.<br><br>Forward Crosstalk—coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal.<br><br>Even Mode Crosstalk—coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching.<br><br>Odd Mode Crosstalk—coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching. |
| Flight Time | Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the $T_{CO}$ of the driver, and any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, *flight time* is defined to be:<br><br>Time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; e.g., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings.<br><br>Maximum and Minimum Flight Time—Flight time variations can be caused by many different variables. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects.<br><br>Maximum flight time is the largest acceptable flight time a network will experience under all variations of conditions.<br><br>Minimum flight time is the smallest acceptable flight time a network will experience under all variations of conditions. |
| GTL+ | GTL+ is the bus technology used by the Intel® Pentium® Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) bus technology. |
| Hub Interface | Proprietary Hub interconnect that ties the MCH to the Intel® ICH4. |
| Intel® ICH4 | The I/O Controller Hub component that contains various IO functions. It communicates with the MCH through the Hub Interface. |
| ISI | Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity. |
| Network | The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components. |
| Network Length | The distance between one agent pin and the corresponding agent pin at the far end of the bus. |
| Overshoot | Maximum voltage observed for a signal at the device pad. |

| Convention/ Terminology | Definition |
|---|---|
| Pad | The electrical contact point of a semiconductor die to the package substrate. A pad is observable only in simulation. |
| Pin | The contact point of a component package to the traces on a substrate, like the system board. Signal quality and timings can be measured at the pin. |
| Ringback | The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena. |
| System Bus | The System Bus is the microprocessor bus of the Intel® Pentium 4 processor. It may also be termed “system bus” in implementations where the System Bus is routed to other components. The P6 bus was the microprocessor bus of the Intel® Pentium® Pro, Intel® Pentium® II, and Intel® Pentium® III processors. The System Bus is not compatible with the P6 bus. |
| Setup Window | The time between the beginning of Setup to Clock ($T_{SU\_MIN}$) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system. |
| SSO | Simultaneous Switching Output (SSO) effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or “push-out”), or a decrease in propagation delay (or “pull-in”). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects. |
| Stub | The branch from the bus trunk terminating at the pad of an agent. |
| Trunk | The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad. |
| Undershoot | Minimum voltage observed for a signal that falls below $V_{SS}$ at the device pad. |
| Victim | A network that receives a coupled crosstalk signal from another network is called the victim network. |
| VREF Guardband | A guardband defined above and below VREF to provide a more realistic model accounting for noise such as VTT and VREF variation. |

## 1.3 System Overview

The Pentium 4 processor with the 845E chipset delivers a high performance and professional desktop platform solution. The processor and chipset support the System Bus protocol.

### 1.3.1 Intel® Pentium® 4 Processor

The Pentium 4 processor in the 478-pin package is the next generation IA-32 processor. This processor has a number of features that significantly increase its performance with respect to previous generation IA-32 processors. The Intel® NetBurst® microarchitecture includes a number of new features as well as some improvements on existing features.

Intel NetBurst microarchitecture features include hyper-pipelined technology, rapid execution engine, 400 & 533 MHz system bus, and an execution trace cache. The hyper pipelined technology doubles the pipeline depth in the Pentium 4 processor in the 478-pin package, allowing the processor to reach much higher core frequencies. The rapid execution engine's two integer ALUs run at twice the core frequency, which allows many integer instructions to execute in 1/2 clock tick. The 400 MHz / 533 MHz system bus is a quad-pumped bus clocked by a 100 MHz /133 MHz system clock, making 3.2 GB/sec / 4.2GB/sec data transfer rates possible. The execution trace cache is a level 1 cache that stores approximately 12K decoded micro-operations, which removes the decoder from the main execution path thereby increasing performance.

Improved features within the Intel NetBurst microarchitecture include advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 256 KB, on-die level 2 cache with an increased bandwidth over previous micro-architectures. The floating point and multi-media units have been improved by making the registers 128 bits wide and adding a separate register for data movement. SSE2 adds 144 new instructions for double precision floating point, SIMD integer, and memory management functions.

The Pentium 4 processor in the 478-pin package supports only uni-processor configurations.

## 1.3.2 Intel® 845E Chipset

The 845E chipset consists of the following main components: Intel® 82845 Memory Controller Hub (MCH) and the I/O Controller Hub (ICH4). These components are interconnected via an Intel proprietary interface called Hub Interface. The Hub Interface is designed into the 845E chipset to provide efficient communication between components.

Additional hardware platform features include AGP 4x mode, DDR SDRAM System memory, Ultra ATA/100, Low Pin Count interface (LPC), integrated LAN* and Universal Serial Bus. The platform is also ACPI compliant and supports Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-off power management states. Through the use of an appropriate LAN* connect, the platform supports Wake-on-LAN* for remote administration and troubleshooting.

### 1.3.2.1 Memory Controller Hub (MCH)

The 845E MCH component provides the processor interface, system memory interface, AGP interface and hub interface in an 845E chipset platform.

The MCH is in a 593 ball FC-BGA package and has the following functionality:

- Supports a single processor with a data transfer rate of 400MHz and 533 MHz
- Supports DDR-SDRAM at 100 MHz/133MHz operation. (DDR)
- AGTL+ host bus with integrated termination supporting 32-bit host addressing
- 1.5 V AGP interface with 4x SBA/data transfer and 2x/4x fast write capability
- 8-bit, 66 MHz 4x Hub Interface to the ICH4. Supports 1.0 Hub Interface running at 1.8 V.

### 1.3.2.2 Accelerated Graphics Port (AGP) Interface

- Supports AGP 2.0 including 1x/2x/4x AGP data transfers and 2x/4x Fast Write protocol

- Supports a single Accelerated Graphics Port (AGP) device (either via a connector or on the motherboard)
- AGP 1.5 V Connector support only. No support for 3.3 V or Universal AGP connectors.
- **AGP 1.5 V support only. Serious damage may occur if a 3.3 V AGP Card is plugged in an 845E chipset based platform.**
- High priority access support
- Delayed transaction support for AGP reads that cannot be serviced immediately

#### 1.3.2.3 DDR-SDRAM

- Supports one DDR-SDRAM channel, 64b wide (72b with ECC)
- Supports 200MHz and 266MHz DDR devices
- Supports 64Mb, 128Mb, 256Mb and 512Mb technologies for x8 and x16 devices
- All supported devices must have 4 banks
- Supports page sizes of 2KB, 4KB, 8KB and 16KB. Page size is individually selected for every row.
- Supports JEDEC DIMM configurations defined in the JEDEC spec (no support for DS x16 DIMMs)

#### 1.3.2.4 Intel® I/O Controller Hub (ICH4)

The ICH 4 provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions. The ICH4 integrates:

- Upstream Hub Interface for access to the MCH
- 2 channel Ultra ATA/100 Bus Master IDE controller
- 6 USB 2/1.1 ports
- I/O APIC
- SMBus 2.0 controller
- FWH interface
- LPC interface
- AC'97 2.2 interface
- PCI 2.2 interface
- Integrated System Management Controller
- Integrated LAN Controller

The ICH4 also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces.

### 1.3.3 Bandwidth Summary

Table 1-2 lists the bandwidths of critical 845E chipset platform interfaces.

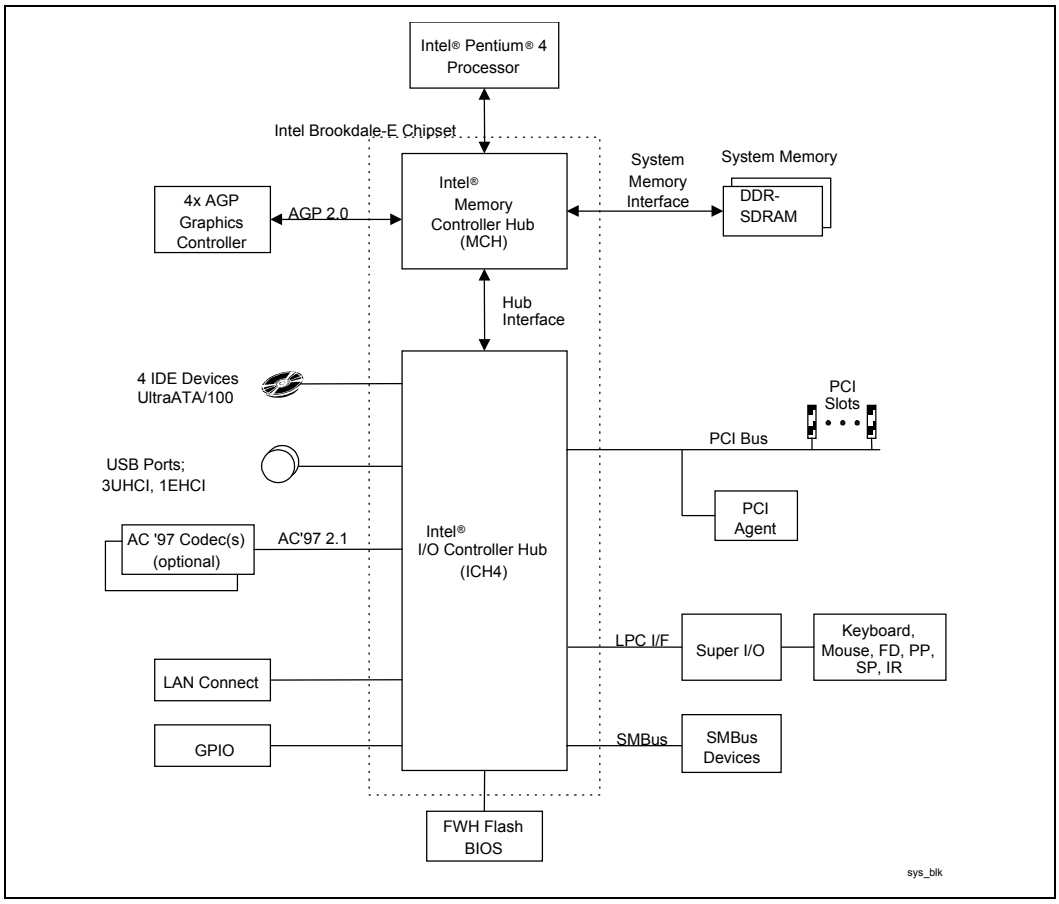
**Table 1-2. Platform Bandwidth Summary**

| Interface | Clock Speed (MHz) | Samples per Clock | Data Width (Bytes) | Bandwidth (MB/s) |
|---|---|---|---|---|
| System Bus | 100/133 | 4 | 8 | 3200/4200 |
| AGP | 66 | 4 | 4 | 1066 |
| Hub Interface | 66 | 4 | 1 | 266 |
| PCI | 33 | 1 | 4 | 133 |
| DDR-SDRAM 200MHz/266MHz | 100/133 | 2/2 | 8/8 | 1600/2100 |

### 1.3.4 System Configurations

Figure 1-1 illustrates a typical Pentium 4 processor and 845E chipset based system configuration for both high performance desktop and mainstream desktop applications.

**Figure 1-1. Typical System Configuration**




## 1.4 Platform Initiatives

### 1.4.1 Intel® 845E Chipset

#### 1.4.1.1 Processor/Host Interface (System Bus)

- Supports single processor
- System Bus interrupt delivery
- Supports 400/533 MHz System Bus
- 32-bit host bus addressing, allowing the processor to access the entire 4 GB of the MCH memory address space.

#### 1.4.1.2 System Memory Interface

The system memory interface delivers high bandwidth to Pentium 4 processors. The MCH DDR-SDRAM interface runs at 100 MHz and 133MHz operations, delivering 1.6 GB/s or 2.1GB/s of memory bandwidth respectively. 64-Mb, 128-Mb, 256-Mb, and 512-Mb DDR-SDRAM technologies are supported.

The 845E chipset supports Suspend-to-RAM power management through system memory self-refresh mode using the SCKE signal.

#### 1.4.1.3 Accelerated Graphics Port (AGP)

AGP is a high performance, component-level interconnect that is designed for 3D graphical display applications. AGP is based on a set of performance extensions and enhancements to the PCI bus. The 845E chipset employs an AGP interface that is optimized for a point-to-point topology using 1.5 V signaling in 4x mode. The 4x mode provides a peak bandwidth of 1066 MB/s.

**AGP 1.5 V support only. Serious damage may occur if a 3.3 V AGP Card is plugged in an 845E chipset based platform.**

For additional information, refer to the *Accelerated Graphics Port Interface Specification, Rev. 2.0* located at:
http://www.agpforum.org.

### 1.4.2 Intel® ICH4

#### 1.4.2.1 Integrated LAN Controller

- WfM 2.0 Compliant
- Interface to discrete Platform LAN Connect component
- 10/100 Mbit/sec Ethernet support

#### 1.4.2.2 Expanded USB Support

- 3 UHCI Host Controllers that includes a root hub with two separate USB ports each, for a total of six legacy USB ports
- 1 EHCI Host Controller that includes a root hub that supports up to six USB 2.0 ports
- Supports a maximum of 6 USB ports at any given time. The connection to either a UCHI or the EHCI is dynamic and dependent on the USB device capability.

#### 1.4.2.3 Ultra ATA/100 Support

- Ultra ATA/100/66/33, BMIDE and PIO modes
- Independent timing of up to 4 drives, with separate IDE connections for Primary and Secondary cables
- Supports “Native Mode” Register and Interrupt support

#### 1.4.2.4 AC'97 6-Channel Support

- AC'97 2.2 compliant
- 20 bit/16 bit audio capability with support for up to six channels of PCM audio output (full AC3 decode)
- Supports 3 codecs with independent PCI functions for audio and modem
- Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center and Woofer for a complete surround sound effect
- Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution.
- Integrated digital link allows several external codecs to be connected
- Third SDATA_IN line
- S/PDIF directed output
- Supports wake-up events (Wake on ring from suspend is supported with an appropriate modem codec)

***Note:*** Modem implementation for different countries must be considered as telephone systems may vary.

#### 1.4.2.5 Manageability and Other Enhancements

- Integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system.
- System management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller

#### 1.4.2.6 SMBus 2.0

- Provides an interface to manage peripherals such as serial presence detection (SPD) on DIMMs.
- 32 byte buffer
- Hardware Packet Error Checking
- Host interface allows the processor to communicate via SMBus
- Slave interface allows an external Microcontroller to access system resources
- Compatible with most 2-Wire components that are also I2C compatible.

#### 1.4.2.7 Interrupt Controller

- Support for up to 8 PCI interrupt pins
- Supports PCI 2.2 Message Signaled Interrupts
- Two cascaded 82C59 with 15 interrupts
- Integrated I/O APIC capability with 24 interrupts
- Supports Serial Interrupt Protocol

- Supports Front-Side Bus interrupt delivery

### 1.4.3 PC ’99/’01 Platform Compliance

PC ’99 and PC ‘01 are intended to provide guidelines for hardware design that will result in optimal user experience, particularly when the hardware is used with the Windows* family of operating systems. This document includes PC ‘99 and PC ’01 requirements and recommendations for basic consumer and office implementations such as desktop, mobile, and workstation systems, and entertainment PCs. This document includes guidelines that address the following design issues:

- Design requirements for specific types of system that will run either Windows* 98, Windows* 2000 or Windows* Millennium Edition operating systems.
- Design requirements related to OnNow design initiative, including requirements related to ACPI, Plug and Play device configuration, and power management in PC systems.
- Manageability requirements that focus on improving Windows* 98, Windows* 2000 and Windows* Millennium Edition, with the end goal of reducing TCO.
- Clarification and additional design requirements for devices supported by Windows* 98, Windows* 2000 and Windows* Millennium Edition, including new graphics and video device capabilities, DVD, scanners and digital cameras, and other devices.

Refer to the PC ‘99 System Design Guide and PC ’01 System Design Guide at http://www.pcdesguide.org/ for additional information.

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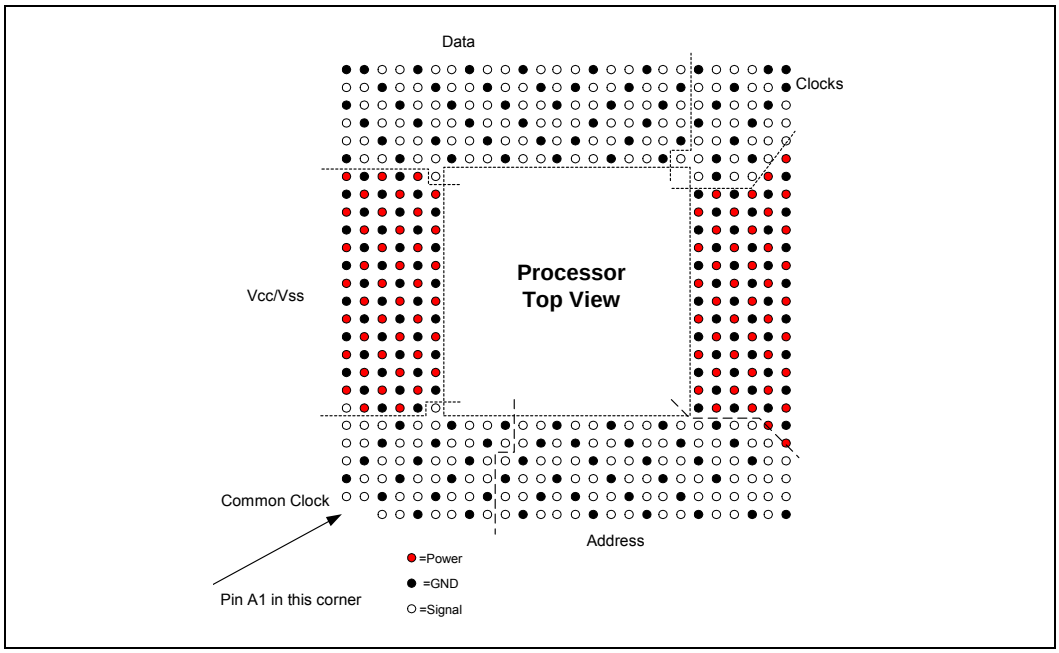
# 2 Component Quadrant Layout

The quadrant layout figures do not show the exact component ball count. The figures show only general quadrant information that is intended for reference while using this document. Only the exact pin or ball assignment should be used to conduct routing analysis. Reference the following documents for pin or ball assignment information.

- *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*
- *Intel® 845E Chipset: 845E Memory Controller Hub (MCH) Datasheet*
- *Intel I/O Controller Hub (Intel®ICH4) Datasheet*

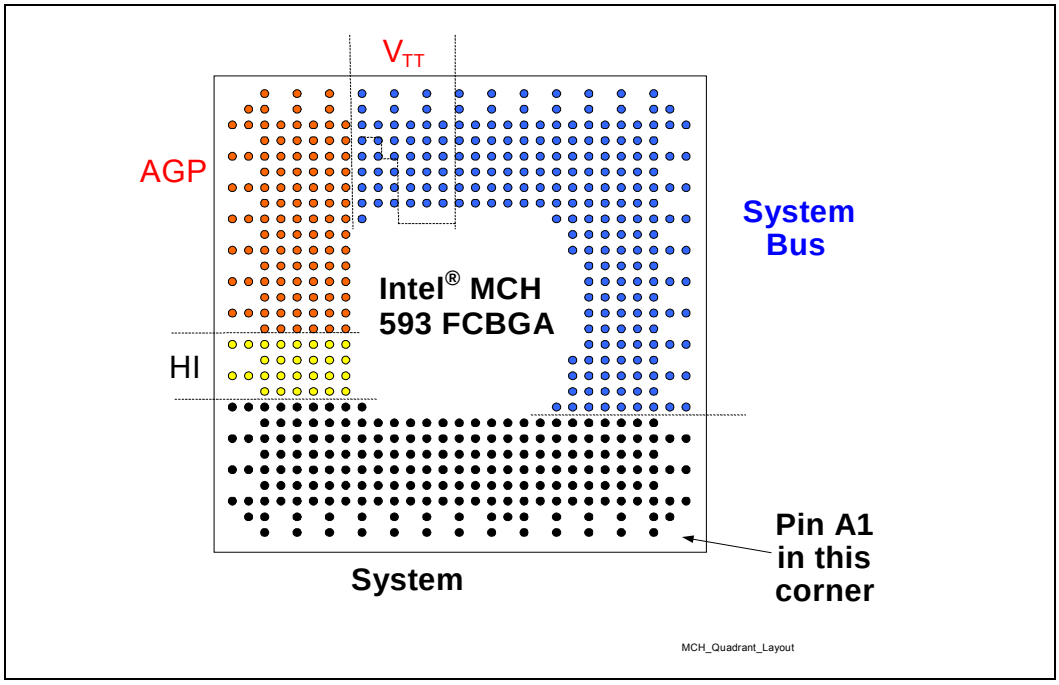
## 2.1 Intel® Pentium® 4 Processor Component Quadrant Layout

**Figure 2-1. Pentium® 4 Processor Component Quadrant Layout (Top View–478 Pin Package)**



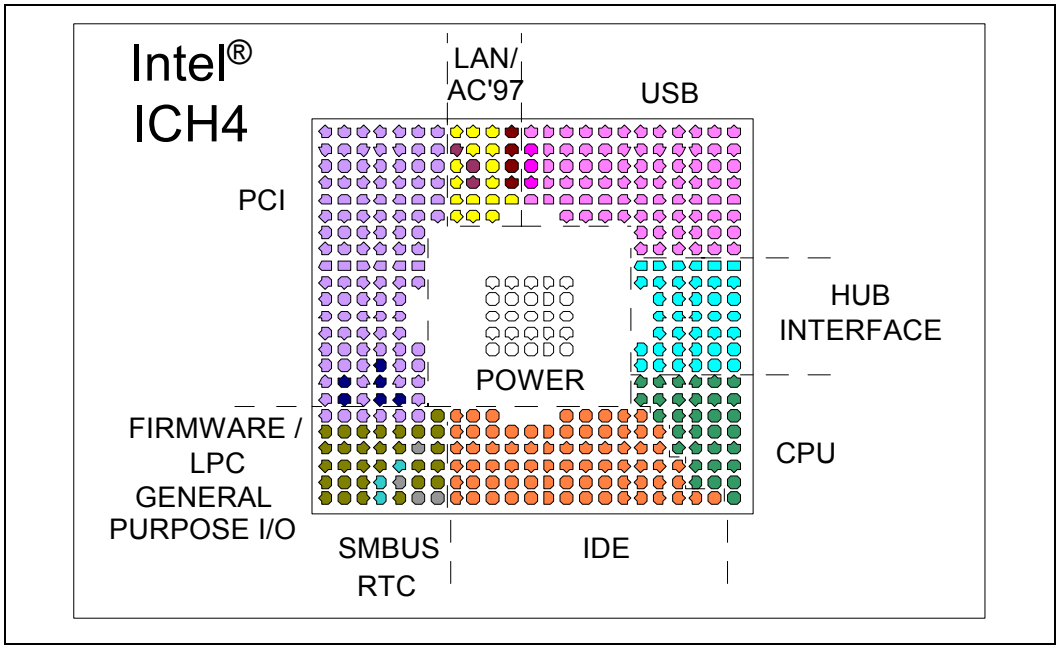
## 2.2 Intel® 845E Chipset Component Quadrant Layout

**Figure 2-2. MCH Component Quadrant Layout (Top View)**




## 2.3 Intel® ICH4 Component Quadrant Layout

**Figure 2-3. Intel® ICH4 Quadrant Layout (top view)**

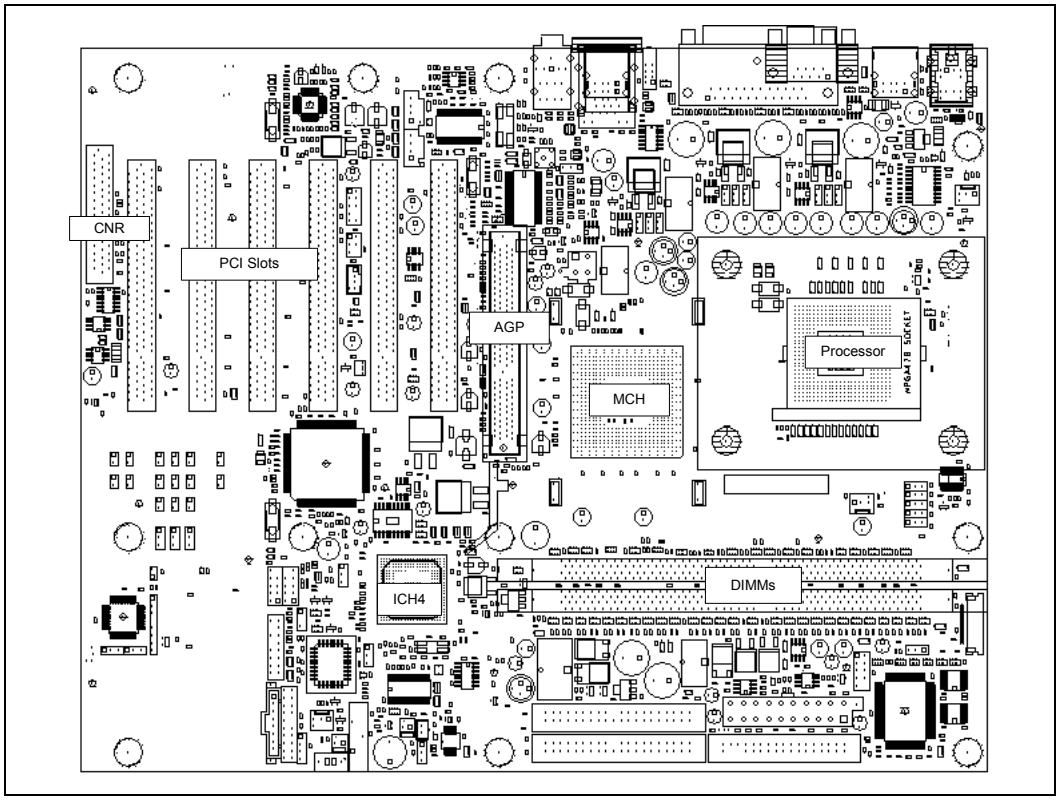


# 3 Platform Placement and Stackup Overview

In this section, an example of a 845E chipset platform component placement and stackup is presented for a desktop system in ATX form factor for DDR. Although the DDR Customer Reference Board is an ATX form factor, the core components are placed within an area equal to a uATX form factor.

## 3.1 Platform Component Placement (DDR SDRAM)

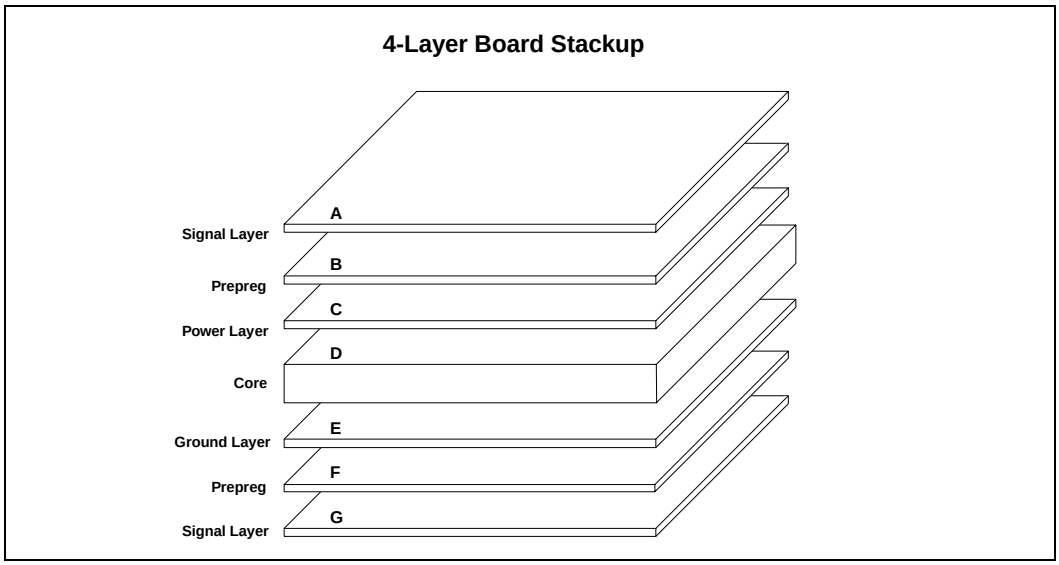
**Figure 3-1. Component Placement Example using DDR-SDRAM DIMMs**



## 3.2 Nominal 4-Layer Board Stackup

The 845E chipset platform requires a board stackup yielding a target board impedance ± 15% of 50 Ω for the System Bus and 60 Ω for the AGP interface, system memory, and hub interface. Recommendations in this design guide are based on the following a 4-layer board stackup.

**Figure 3-2. 4-layer PCB Stackup**




| Description | Target Value |
|---|---|
| Target Board Impedance $Z_0$ | 50 Ω ± 15% with a 7 mil nominal Trace width.<br>60 Ω ± 15% with a 5 mil nominal Trace width. |
| Micro-stripline Er | 4.2–4.5 |
| Er @ 1 MHz | 4.5 |
| Er @ 1 GHz | 4.35 |

| Description | Typical Values |
|---|---|
| Trace Thickness | 1.3–1.42 mils. |
| Board Thickness | 62 mils total 0.062 + 0.008 - 0.005. |
| Material | Fiberglass made of FR4. |
| Fab Construction | 4 layer. |

| Layer | Description | Nominal Thickness | Tolerance (± mils) |
|---|---|---|---|
| A | Signal Layer | 0.7 mil (0.5 oz Cu) (See note 1) | (See note 2) |
| B | Prepreg | 4.0 mil | 0.3 |
| C | Power Layer | 1.4 mil (1.0 oz Cu) | 0.2 |
| D | Core | 48 mil | 5 |
| E | Ground Layer | 1.4 mil (1.0 oz Cu) | 0.2 |
| F | Prepreg | 4.0 mil | 0.3 |
| G | Signal Layer | 0.7 mil (0.5 oz Cu) (See note 1) | (See note 2) |

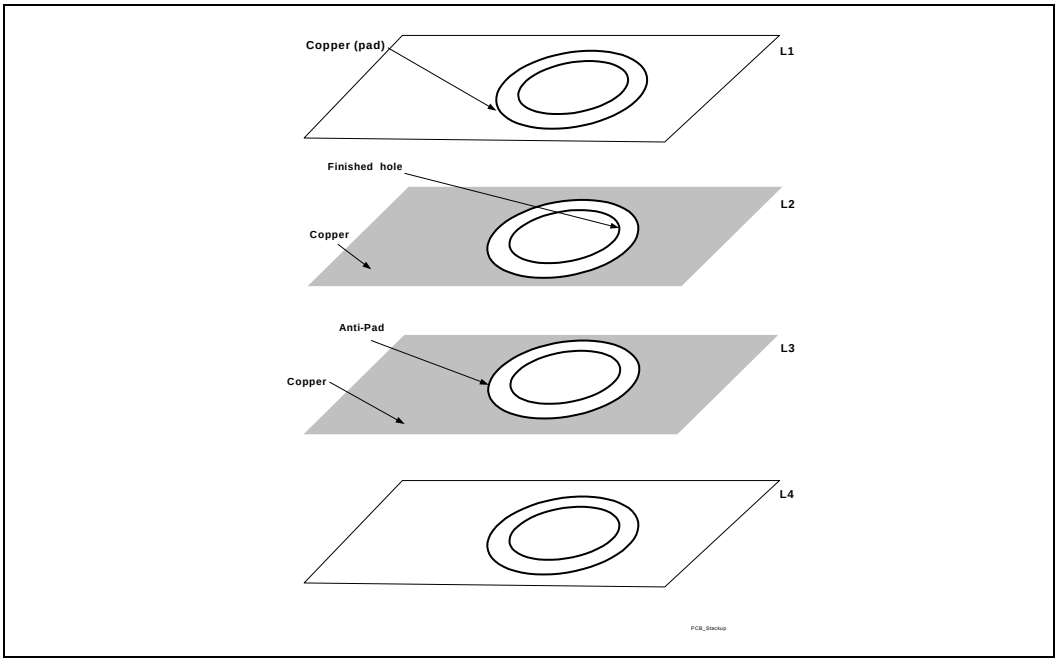
**NOTES:**
1. Thickness before Plating
2. Final Plating Thickness varies 1.3 mils—1.42 mils

# 3.3 PCB Technologies

## 3.3.1 Design Considerations

Intel has found that the following recommendation aids in the design of an 845E chipset-based platform. Simulations and reference platform are based on the following technology and is recommended that designers adhere to these guidelines.

**Figure 3-3. PCB Technologies—Stack Up**



| Number of Layers | |
|---|---|
| Stack Up | 4 Layer |
| Cu Thickness | 0.5 oz Outer; (before Plating) 1 oz inner |
| Final Board Thickness | 0.062 in. +0.008—0.005 in. |
| **Signal and Power Via Stack /Processor / MCH / Intel® ICH4 / Memory Breakout** | |
| Via Pad | 0.026 in. |
| Via Anti-Pad | 0.040 in. |
| Via Finished Hole | 0.014 in. |
| Solder Mask Opening (top side only) [1] | 0.020 in. |
| Signal Pad (BGA) | 0.020 in. |

**NOTE:** [1]For solder bridge avoidance these pads are to be partially covered by solder mask on the primary side. Solder mask residue must not be left in the holes.

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# 4 Processor System Bus Guidelines

## 4.1 Processor System Bus Design Guidelines

Table 4-1 summarizes the layout recommendations for Pentium 4 processor configurations and expands on specific design issues and recommendations.

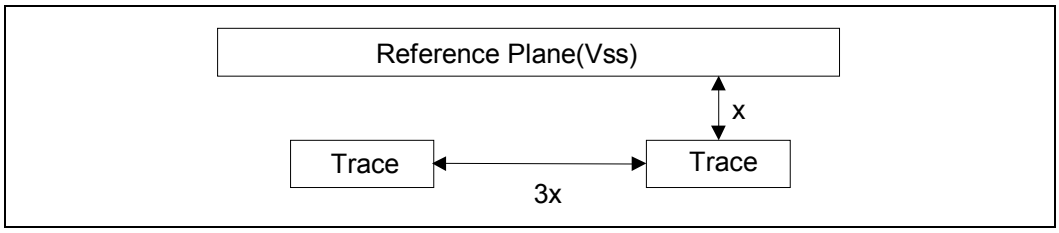
**Table 4-1. System Bus Routing Summary for the Processor**

| Parameter | Processor Routing Guidelines |
|---|---|
| Line to line spacing | Data and common clock system bus must be routed at 7 mil wide traces and with 13 mils spacing. |
| Breakout Guidelines (PROCESSOR & MCH) | 7 mil wide with 5 mil spacing for a maximum of 250 mils from the component ball. |
| Data Line lengths (agent to agent spacing) | 2 in.—8 in. from pin to pin.<br>Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Signals should be referenced to VSS. |
| DSTBn/p[3:0]# | A layer transition may occur if the reference plane remains the same (VSS) and the layers are of the same configuration (all stripline or all microstrip).<br>A data strobe and its complement should be routed within ± 25 mils of the same pad-to-pad length.<br>If one strobe switches layers, its complement must switch layers in the same manner.<br>DSTBn/p# should be referenced to VSS. |
| Address line lengths (agent to agent spacing)<br>ADSTB[1:0]# | 2 in.—10 in. from pin to pin.<br>Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS), and the layers are of the same configuration (all stripline or all microstrip). |
| Common Clock line lengths | 3.0 in.—10 in. pin to pin.<br>No length compensation is necessary. |
| Topology | Point to point (chipset to processor). |

| Parameter | Processor Routing Guidelines |
|---|---|
| Routing priorities | All signals should be referenced to VSS.<br>Ideally, layer changes should not occur for any signals. If a layer change must occur, the reference plane must be VSS and the layers must all be of the same configuration (all stripline or all microstrip for example).<br>The data bus must be routed first, then the address bus, then common clock. |
| Clock keep out zones | Refer to Table 15-3 of the Platform Design Guide Revision 1.0. |
| Trace Impedance | 50 Ω ± 15% |

***Note:*** Refer to the *Intel® 845E Chipset: 845E Memory Controller Hub (MCH) Datasheet* for MCH package dimensions, and refer to *Intel® Pentium® 4 Processor in the 478 pin package Processor Signal Integrity Models* for processor package dimensions.

**Figure 4-1. Cross Sectional View of 3:1 Ratio**




The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, and vias, VRMs etc. It is useful to think of the return path as following a path of least resistance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths must be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance will be.

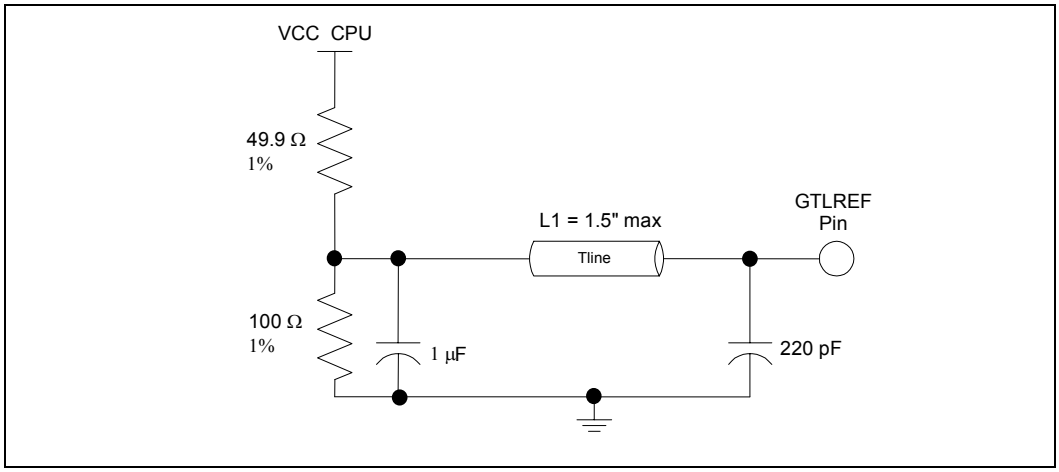
The following sets of return path rules apply:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near system bus signals.
- Maintain VSS as a reference plane for all system bus signals.
- Do not route over via anti-pads or socket anti-pads.

### 4.1.1 GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF). Because all of these pins are connected inside the processor package, the GTLREF voltage must be supplied to only one of the four pins.

**Figure 4-2. GTLREF Routing**




- The processor must have one dedicated voltage divider.
- Decouple the voltage divider with a 1 µF capacitor.
- Keep the voltage divider within 1.5 inches of the GTLREF pin.
- Decouple the pin with a high-frequency capacitor (such as a 220 pF 603) as close to the pin as possible.
- Keep signal routing at least 10 mils separated from the GTLREF routes. Use at least a 7 mil trace for routing.
- Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the front side bus signals).

### 4.1.2 HVREF, HSWNG, HRCOMP Layout and Routing Recommendations at the MCH

The HVREF signals must be tied to a resistor divider network that supplies 2/3*VCC_CPU. Use one 49.9 Ω 1% resistor to the VCC_CPU plane and one 100 Ω 1% resistor to ground for the divider. Decouple with one 0.1 µF capacitor at the MCH. The trace to the voltage divider should be routed at a maximum of 3 in. at 12 mils wide. Keep this trace at a minimum of 10 mils away from other signals.

The HSWNG signals must be tied to a resistor divider network that supplies 1/3*VCC_CPU. Use one 300 Ω 1% resistor to the VCC_CPU plane and one 150 Ω 1% resistor to ground for the divider. Decouple with one 0.01 µF capacitor at the MCH. The trace to the voltage divider should be routed at a maximum of 3 in. at 12 mils wide. Keep this trace at a minimum of 10 mils away from other signals.

Each HRCOMP signal must be tied to ground through a 24.9 Ω 1% resistor. The trace to each resistor should be routed a maximum of 0.5 in. at 10 mils wide. Keep each trace a minimum of 7 mils away from other signals.

## 4.2 Processor Configuration

### 4.2.1 Intel® Pentium® 4 Processor Configuration

This section provides more details for routing Pentium 4 processor based systems. Both recommendations and considerations are presented.

For proper operation of the processor and the 845E chipset, it is necessary that the system designer meet the timing and voltage specifications of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation based on assumptions that may not apply to an OEM's system design. The most accurate way to understand the signal integrity and timing of the system bus in a platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stackup and other parameters can be made that improve system performance.

Refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet* for a system bus signal list, signal types, and definitions.

## 4.2.2 Topology and Routing

**Table 4-2. Source Synchronous Signal Groups and the Associated Strobes**

| Signals | Associated Strobe |
|---|---|
| REQ[4:0]#, A[16:3]# | ADSTB0# |
| A[31:17]# | ADSTB1# |
| D[15:0]#, DBI0# | DSTBP0#, DSTBN0# |
| D[31:16]#, DBI1# | DSTBP1#, DSTBN1# |
| D[47:32]#, DBI2# | DSTBP2#, DSTBN2# |
| D[63:48]#, DBI3# | DSTBP3#, DSTBN3# |

Design recommendations are presented first, followed by design considerations.

### 4.2.2.1 Design Recommendations

The following are the design recommendations for the data, address, strobes, and common clock signals. Based on the example of Figure 3-2 the data, address, strobe and common clock should be routed 7 mils with 13-mil spacing. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

#### DATA

The pad-to-pad distance for the data signals from the processor to the chipset should be between 2.0 in. and 8 in. (i.e., 2.0 in. < L1 < 8 in.). Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. As a result, additional trace will be added to some data nets on the system board in order for all trace lengths within the same data group to be the same length (± 100 mils) from the pad of the processor to the pad of the chipset. This length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without the length compensation the flight times between a data signal and its strobe will be different, which results in an inequity between the setup and hold times. Data signals may change layers if the reference plane remains VSS.

The following equation is used to calculate package delta addition to motherboard length for UP systems.

$$\text{delta}_{\text{net,strobe}} = (\text{cpu\_pkglen}_{\text{net}} - \text{cpu\_pkglen}_{\text{strobe*}}) + (\text{cs\_pkglen}_{\text{net}} - \text{cs\_pkglen}_{\text{strobe}})$$

**NOTES:**
1. Refer to section 0 for package lengths.
2. * Strobe package length is the average of the strobe pair.

### ADDRESS

Address signals follow the same rules as data signals except they should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. Address signals may change layers if the reference plane remains VSS.

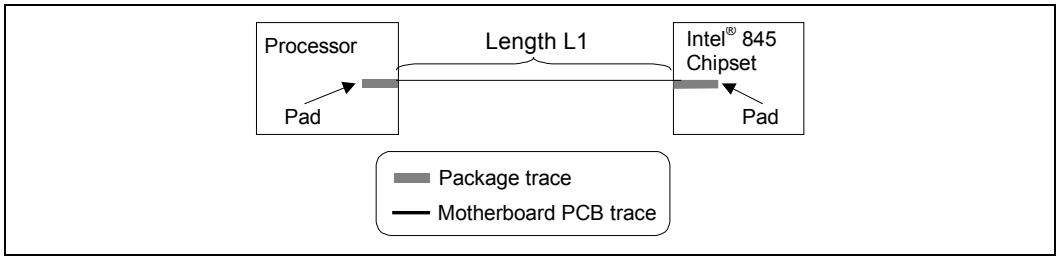
### DATA STROBES

A strobe and its complement should be routed to a length equal to their corresponding data group's mean pad-to-pad length ± 25 mils. This causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. A strobe and its complement (xSTBp/n#) should be routed to ± 25 mils of the same length. It is recommended to simulate skew to determine the length that best centers the strobe for a given system.

### COMMON CLOCK

Common clock signals should be routed to a minimum pin-to-pin motherboard length of 3.0 inches and a maximum motherboard length of 10 inches.

**Figure 4-3. Processor Topology**



## 4.3 Routing Guidelines for Asynchronous GTL+ and Other Signals

This section describes layout recommendations for signals other than data, strobe, and address. Table 4-3 lists the signals covered in this section.

**Table 4-3. Miscellaneous Signals (Signals That Are Not Data, Address, or Strobe)**

| Signal Name | Type | Direction | Topology | Driven By |
|---|---|---|---|---|
| A20M# | Asynchronous GTL+ | I | 2A | ICH4 |
| BR0# | AGTL+ | I/O | 4 | Processor |
| COMP[1:0] | Analog | I | 5 | |
| FERR# | Asynchronous GTL+ Open Drain | O | 1A | Processor |
| IGNNE# | Asynchronous GTL+ | I | 2A | ICH4 |
| INIT# | Asynchronous GTL+ | I | 2B | ICH4 |
| LINT0/INTR LINT1/NMI | Asynchronous GTL+ | I | 2A | ICH4 |
| PROCHOT# | Asynchronous GTL+ Open Drain | O | 1B | Processor |
| PWRGOOD | Asynchronous GTL+ Open Drain | I | 2C | ICH4 |
| RESET# | AGTL+ Open Drain | I | 4 | MCH |
| SLP# | Asynchronous GTL+ | I | 2A | ICH4 |
| SMI# | Asynchronous GTL+ | I | 2A | ICH4 |
| STPCLK# | Asynchronous GTL+ | I | 2A | ICH4 |
| THERMTRIP# | Asynchronous GTL+ Open Drain | O | 1C | Processor |
| $V_{CCA}$ | Power | I | 3 | External logic |
| $V_{CCIOPLL}$ | Power | I | 3 | External logic |
| $V_{CCSENSE}$ | Other | O | | Processor |
| VID[4:0] | Open Drain 3.3 V Tolerant | O | 8 | Processor |
| $V_{SSA}$ | Power | I | 3 | Ground |
| $V_{SSSENSE}$ | Other | O | | Processor |
| THERMDA/THERMDC | Other | I/O | 6 | External logic |
| TESTHI | Other | I/O | 7 | External logic |

**NOTE:** Refer to Section 14, Schematic Checklist, for Debug Port signals.

All signals must meet the AC and DC specifications as documented in the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*.

## 4.3.1 Topologies

The following sections describe the topologies and layout recommendations for the miscellaneous signals.

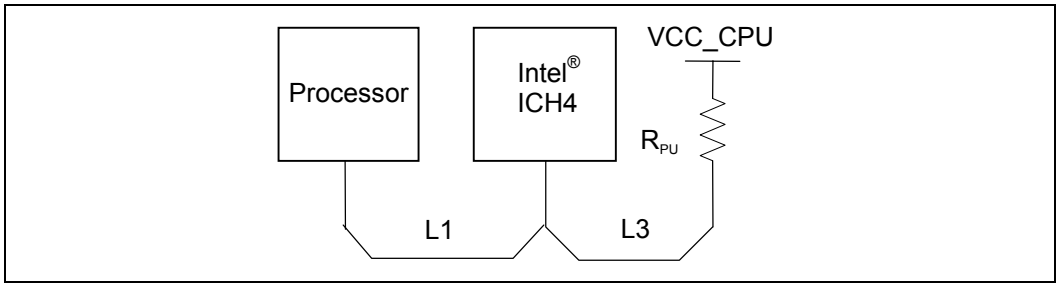
### 4.3.1.1 Topology 1A: Asynchronous GTL+ Signal Driven by the Processor—FERR#

FERR# should adhere to the routing and layout recommendations described and illustrated in Table 4-4 and Figure 4-4.

**Table 4-4. Layout Recommendations for FERR# Signal—Topology 1A**

| Trace Zo | Trace Spacing | L1 | L3 | Rpu |
|---|---|---|---|---|
| 60 Ω | 7 mil | 1 in.—12 in. | 3 in. max | 62 Ω ± 5% |

**Figure 4-4. Routing Illustration for FERR#**



### 4.3.1.2 Topology 1B: Asynchronous GTL+ Signal Driven by the Processor—PROCHOT#

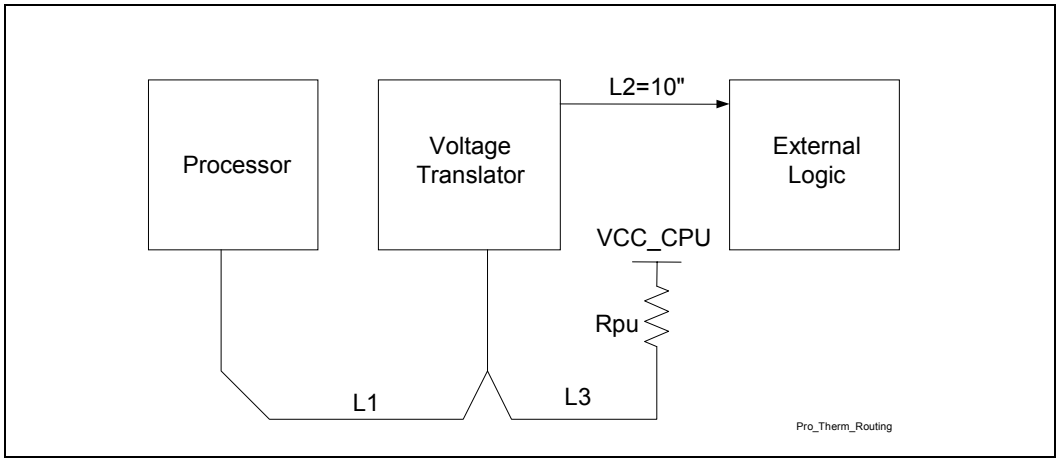
PROCHOT# should adhere to the routing and layout recommendations described and illustrated in Table 4-5 and Figure 4-5.

If PROCHOT# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

**Table 4-5. Layout Recommendations for PROCHOT# Signal—Topology 1B**

| Trace Zo | Trace Spacing | L1 | L2 | L3 | Rpu |
|---|---|---|---|---|---|
| 60 Ω | 7 mil | 1 in.—17 in. | 10 in. max | 3 in. max | 62 Ω ± 5% |

**Figure 4-5. Routing Illustration for PROCHOT#**



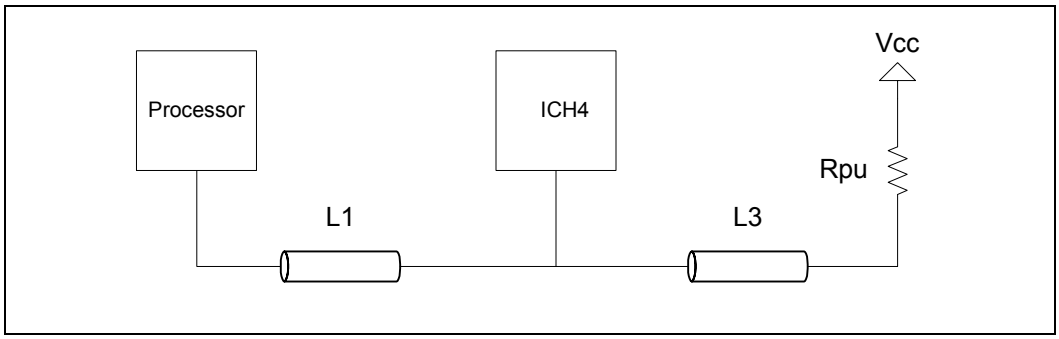
### 4.3.1.3 Topology 1C: Asynchronous GTL+ Signal Driven by the Processor—THERMTRIP#

THERMTRIP# should adhere to the routing and layout recommendations described and illustrated in Table 4-6 and Figure 4-6. If THERMTRIP# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

**Table 4-6. Layout Recommendations for THERMTRIP# Signal—Topology 1C**

| Trace Zo | Trace Spacing | L1 | L3 | Rpu |
|---|---|---|---|---|
| 60 □ | 7 mil | 1 in.—12 in. | 3 in. max | 62 □ +/- 5% |

**Figure 4-6. Routing Illustration for THERMTRIP#**



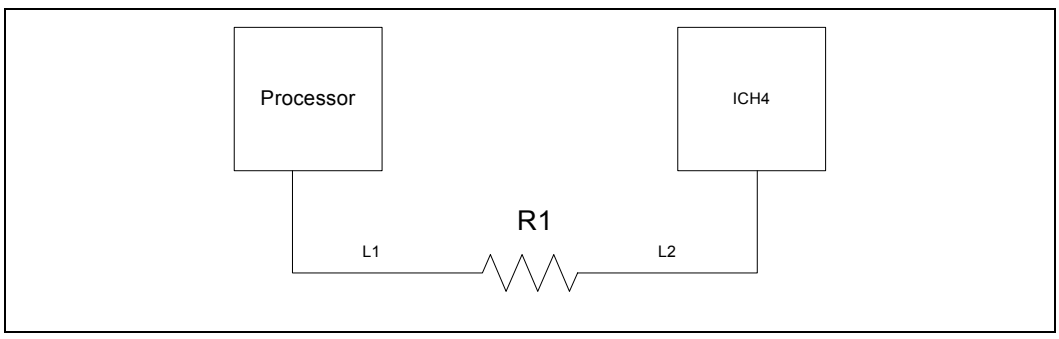

### 4.3.1.4 Topology 2A: Asynchronous GTL+ Signals Driven by the Intel® ICH4—A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#

These signals should adhere to the routing and layout recommendations described and illustrated in Table 4-7 and Figure 4-7.

**Table 4-7. Layout Recommendations for A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#—Topology 2A**

| Trace Zo | Trace Spacing | L1 | L2 | R1 |
|---|---|---|---|---|
| 60 Ω | 7 mil | 1 in.—17 in. | 2 in. max | 60 Ω - 80 Ω |

**Figure 4-7. Routing Illustration for A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#**



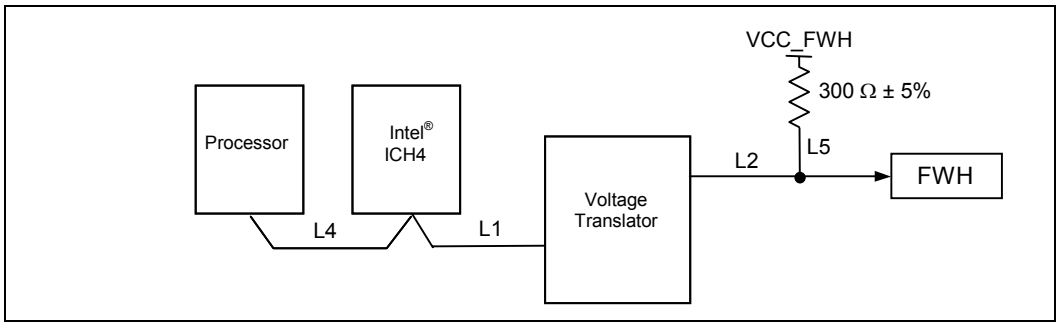
### 4.3.1.5 Topology 2B: Asynchronous GTL+ Signal Driven by the ICH4—INIT#

INIT# should adhere to the routing and layout recommendations described and illustrated in Table 4-8 and Figure 4-8.

**Table 4-8. Layout Recommendations for INIT#—Topology 2B**

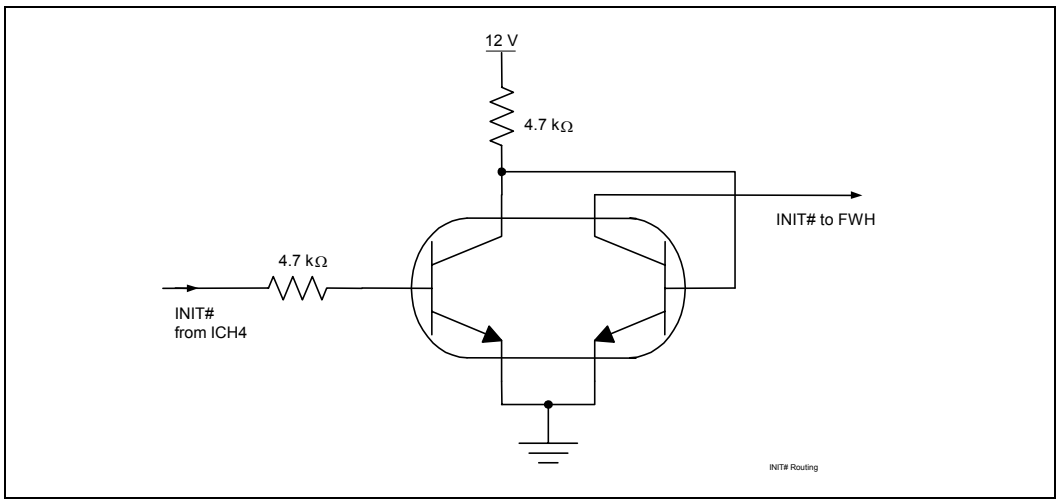
| Trace Zo | Trace Spacing | L1 | L2 | L4 | L5 | Rpu |
|---|---|---|---|---|---|---|
| 60 Ω | 7 mils | 2 in. max | 10 in. max | 17 in. max | 3 in. max | 300 Ω 5% |

**Figure 4-8. Routing Illustration for INIT#**




Level shifting is required for the INIT# signal to the FWH to meet the input logic levels of the FWH. Figure 4-9 illustrates one method of level shifting.

**Figure 4-9. Voltage Translation of INIT#**



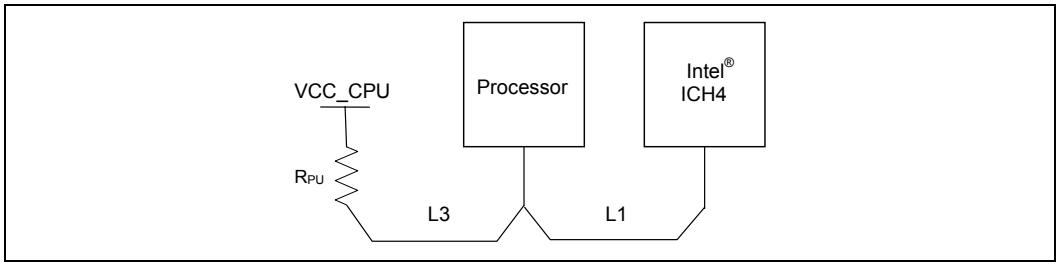
### 4.3.1.6 Topology 2C: Asynchronous GTL+ Signal Driven by the Intel® ICH4 Open Drain—PWRGOOD

PWRGOOD should adhere to the routing and layout recommendations described and illustrated in Table 4-9 and Figure 4-10.

**Table 4-9. Layout Recommendations for Miscellaneous Signals—Topology 2C**

| Trace Zo | Trace Spacing | L1 | L3 | Rpu |
|---|---|---|---|---|
| 60 Ω | 7 mil | 1 in.–12 in. | 3 in. max | 300 Ω ± 5% |

**Figure 4-10. Routing Illustration for PWRGOOD**



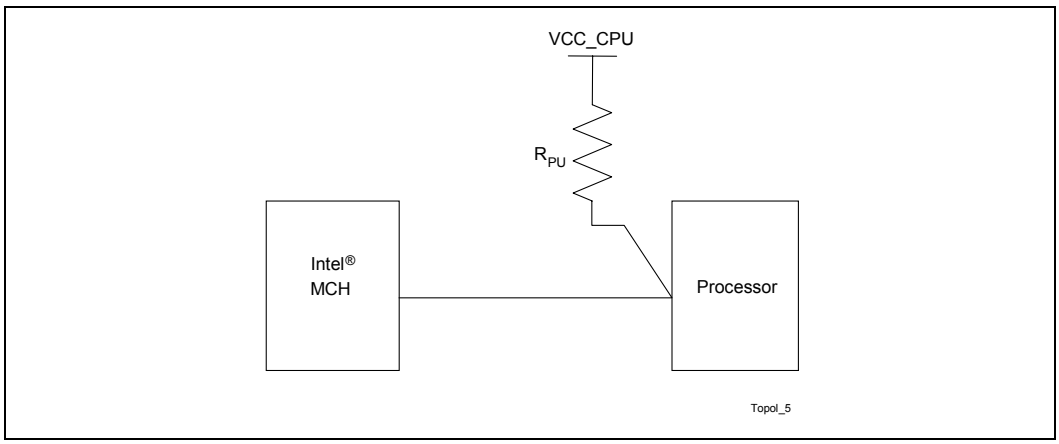

### 4.3.1.7 Topology 3—VCCIOPLL, VCCA and VSSA

VCCIOPLL and VCCA are isolated power for internal PLLs. It is critical that they have clean, noiseless power on their input pins. Further details can be found in Section 4.6.5.1.

### 4.3.1.8 Topology 4—BR0# and RESET#

Because the processor does not have on-die termination on the BR0# and RESET# signals, it is necessary to terminate the signals using discrete components on the system board. Connect the signals between the components as shown in Figure 4-11. The 845E chipset has on-die termination; therefore it is necessary to terminate only at the processor end. The value of Rt should be 51 Ω ± 5%.

**Figure 4-11. Routing Illustration for BR0# and RESET#**



#### 4.3.1.9 Topology 5: COMP[1:0] Signals

Terminate the COMP[1:0] pins to ground through a 51 Ω ± 1% resistor as close as possible to the pin. Do not wire COMP pins together; connect each pin to its own termination resistor. RCOMP value can be adjusted to set external drive strength of I/O and to control the edge rate.

#### 4.3.1.10 Topology 6: THERMDA/THERMDC Routing Guidelines

The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the processor for thermal management/long term die temperature change monitoring purpose. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. The following are some guidelines:

- The remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4 to 8 inches away as long as the worst noise sources such as clock generators, data buses, and address buses, etc., are avoided.
- Route the THERMDA and THERMDC lines in parallel and close together with ground guards enclosed.
- Use wide tracks to reduce inductance and noise pickup that may be introduced by narrow ones. A width of 10 mils and spacing of 10 mils is recommended.

#### 4.3.1.11 Topology 7: TESTHI and RESERVED Pins

The TESTHI pins should be tied to the processor Vcc using a matched resistor, where a matched resistor has a resistance value within +- 20% of the impedance of the board transmission line traces. For example, If the trace impedance is 50 ohms, then a value between 40 and 60 ohms is required.

The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. A matched resistor should be used for each group:

1) TESTHI[1:0]

2) TESTHI[5:2]

3) TESTHI[10:8]

4) TESTHI[12:11]

Additionally, if the ITPCLKOUT[1:0] pins are not used then they may be connected individually to VCC using matched resistors or grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1k ohm resistors is acceptable. Tying ITPCLKOUT[1:0] directly to VCC or sharing a pull-up resistor to VCC will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an onboard debug port.

As an alternative, group 2 ( TESTHI [5:2] ), and the ITPCLKOUT[1:0] pins may be tied directly to the processor Vcc. This has no impact on system functionality. TESTHI[0] and TESTHI[12] may also be tied directly to processor Vcc if resistor termination is a problem, but matched resistor termination is recommended. In the case of the ITPCLKOUT[1:0], direct tie to Vcc is strongly discouraged for system boards that do not implement an onboard debug port.

#### 4.3.1.12 Topology 8: Processor Voltage Regulator Sequencing Requirements

- The output of the voltage regulator used to generate VCCVID should be no more than 1.5 inches away from pin AF4 of the processor.
- The trace connecting the voltage regulator output to pin AF4 should be as wide as practical, but not less than 0.025 inches.
- The trace connecting the voltage regulator output to pin AF4 should have both a 0.1 µF and 1.0 µF capacitor for decoupling. The 1.0 µF capacitor should be located as close as possible to the output of the voltage regulator. The 0.1 µF capacitor should be located as close as possible to pin AF4 on the processor.

If an integrated voltage regulator such as the MIC5248 is used, the voltage input (pin 1) should be connected to the system board's VCC or 3.3 V rails through a zero ohm resistor. The input of the voltage regulator should also be decoupled with a 0.1 µF capacitor at the pin. The trace connecting the voltage regular input to the zero resistor should be equal to or greater than the voltage regulator output trace connected to the processor (i.e. if the connection to the processor is 0.025 inches than the trace width to the input of the voltage regulator should be 0.025 inches or greater). The voltage regulator power good signal (pin 4) should be connected to the voltage regulator output (pin 5) through a 10k ohm resistor.

During power-on the rising edge of the VCCVID power supply needs to be monotonic. Examples of an acceptable monotonic and an unacceptable non-monotonic rising edge are show below for reference.

**Figure 4-12. Passing Monotonic Rising Edge Voltage Waveform**

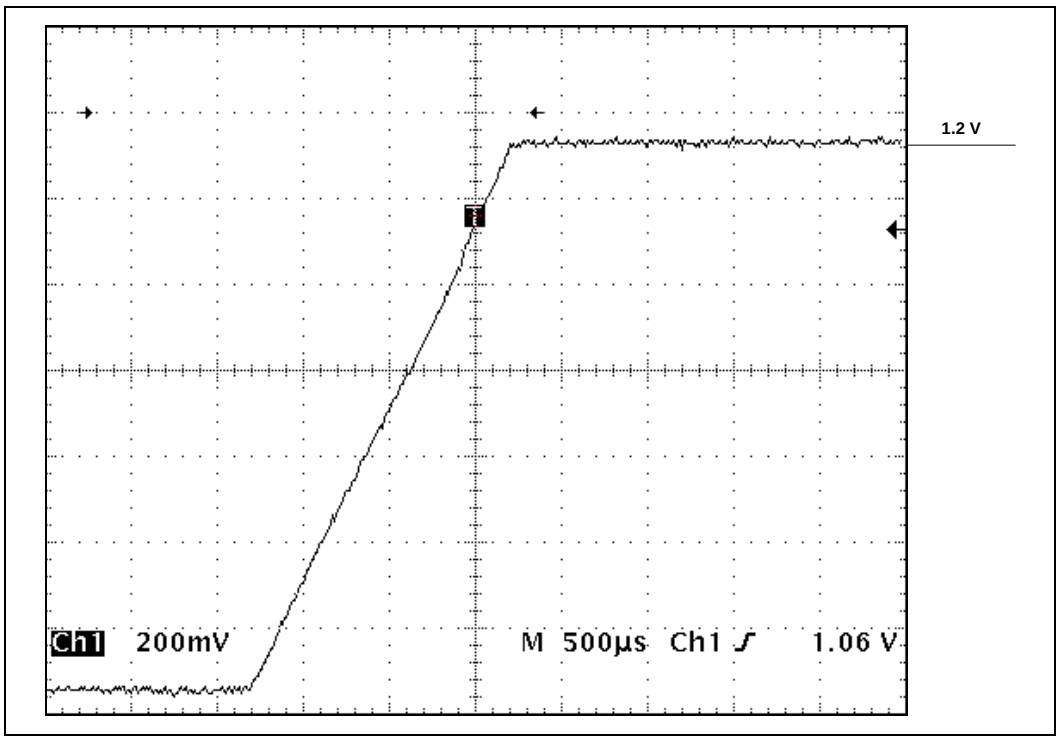
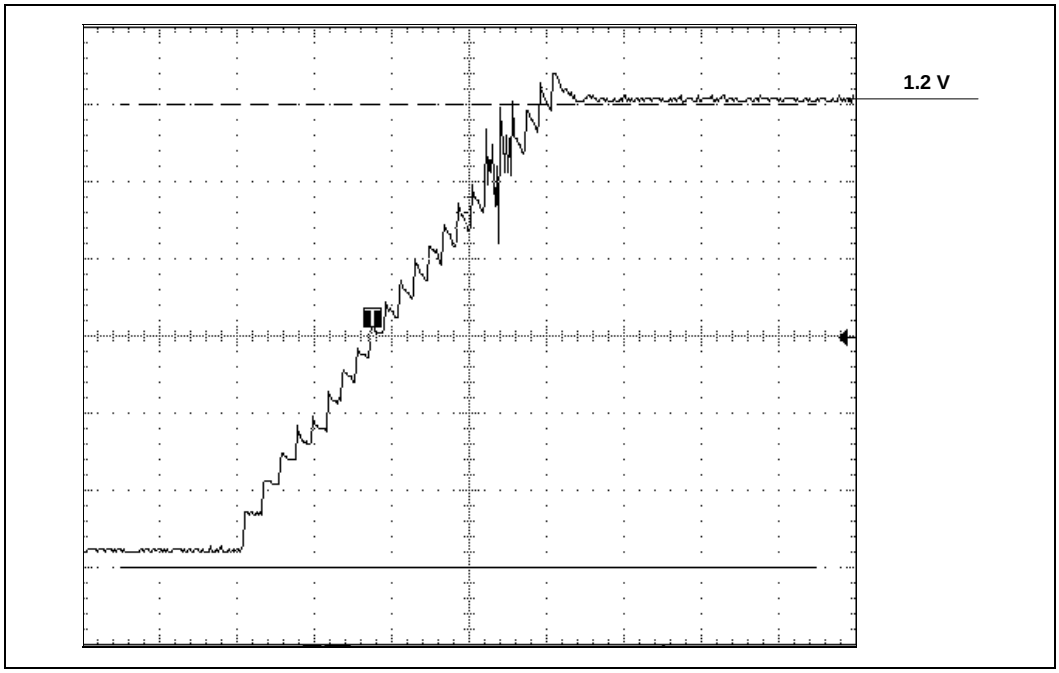


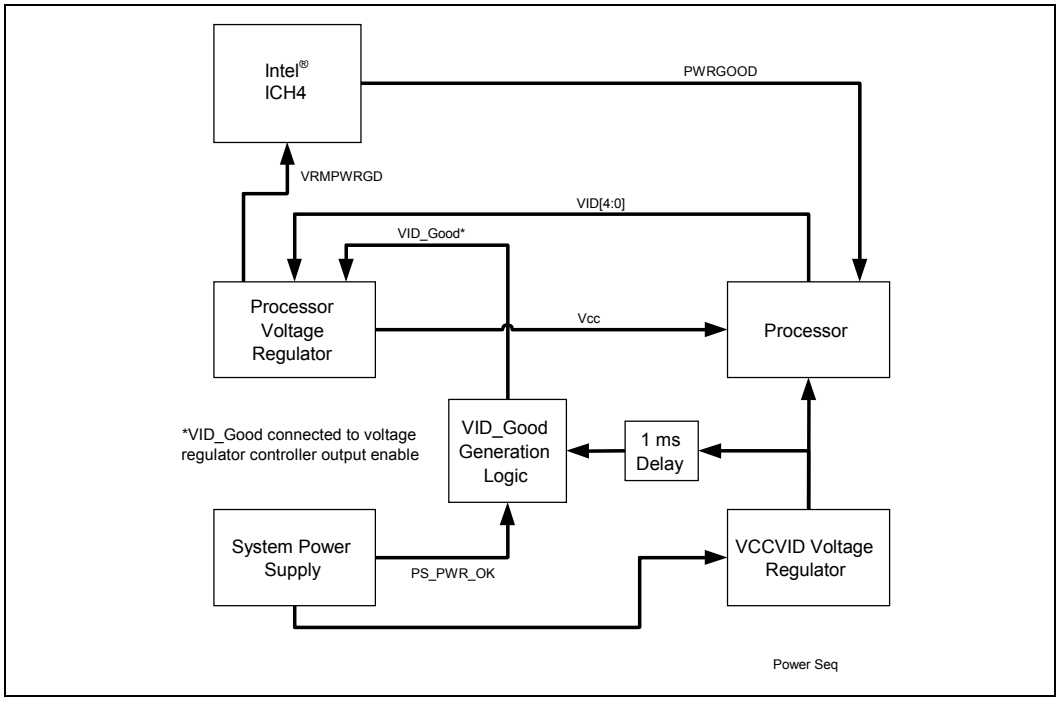

**Figure 4-13. Failing Non-Monotonic Rising Voltage Waveform**




Please refer to Section 4.6 for more details.

The platform requires a 1.2 V supply to the VCCVID pins to support the on-die VID generation circuitry. A linear regulator is recommended to generate this voltage. The on-die VID generation circuitry has some power sequencing requirements. Figure 4-14 shows a block diagram of a power sequencing implementation.

**Figure 4-14. Power Sequencing Block Diagram**



## 4.4 Additional Processor Design Considerations

This section documents system design considerations not addressed in previous sections.

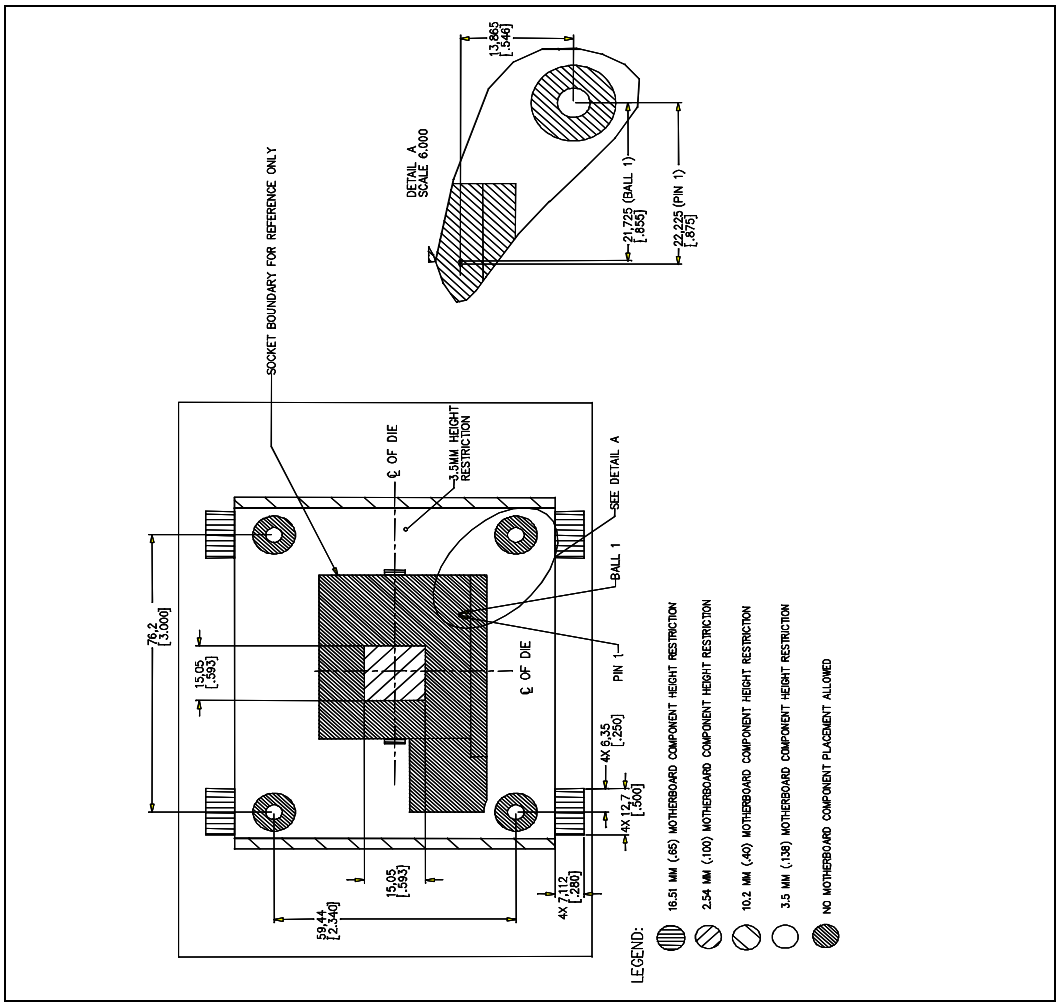
### 4.4.1 Retention Mechanism Placement and Keepouts

The RM requires a keep out zone for a limited component height area under the RM as shown in Figure 4-15 and Figure 4-16. The figures show the relationship between the RM mounting holes, and pin one of the socket. In addition it also documents the keepouts.

The retention holes should be a non-plated hole. The retention holes should have a primary and secondary side route keepout area of 0.409 inches diameter.

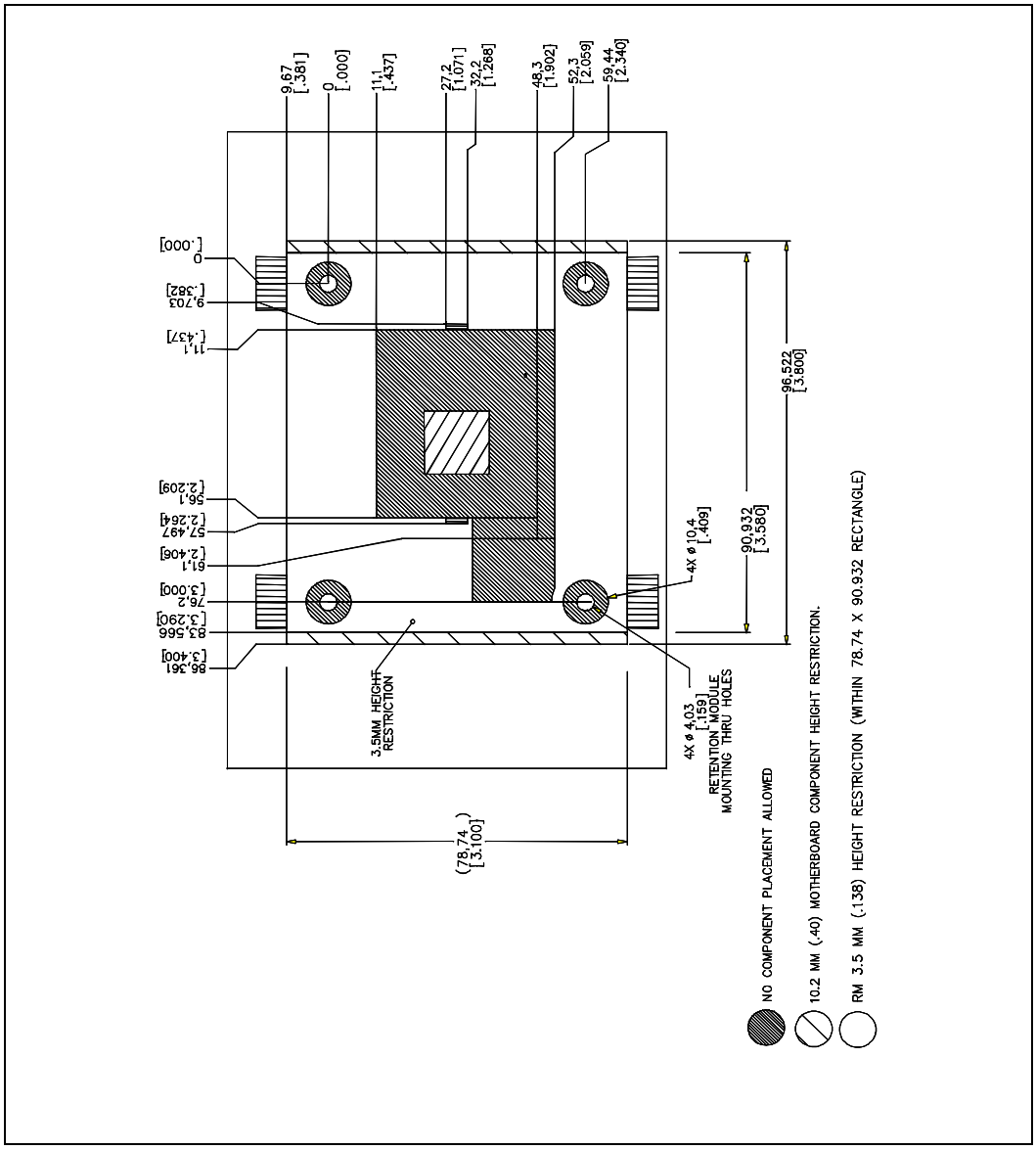
For heat sink volumetric information refer to the *Intel® Pentium® 4 Processor in the 478-pin package Thermal Design Guidelines*.

**Figure 4-15. RM Keepout Drawing 1**




**NOTE:** Dimensions are in millimeters with inch dimensions in brackets.

**Figure 4-16. RM Keepout Drawing 2**




**NOTE:** Dimensions are in millimeters with inch dimensions in brackets.

### 4.4.2 Power Header for Active Cooling Solutions

The Intel reference-design heatsink includes an integrated fan. The recommended connector for the active cooling solution is a Walden*/Molex 22-01-3037, AMP* 643815-3, or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described Table 4-10

**Table 4-10. Reference Solution Fan Power Header Pinout**

| Pin Number | Signal |
|---|---|
| 1 | Ground |
| 2 | +12 V |
| 3 | No Connect |

The Intel boxed processor heatsink includes an integrated fan. The recommended connector for the active cooling solution is a Walden*/Molex* 22-23-2037, AMP* 640456-3 or equivalent. The integrated fan requires the system board to supply a minimum of 740 mA at 12 V for proper operation. The fan connector pinout is described in Table 4-11

**Table 4-11. Boxed Processor Fan Power Header Pinout**

| Pin Number | Signal |
|---|---|
| 1 | Ground |
| 2 | +12 V |
| 3 | Sense |

The fan heatsink outputs a SENSE signal, which is an open-collector output that pulses at a rate of two pulses per fan revolution. The system board requires a pull-up resistor to provide the appropriate Voh level to match the fan speed monitor. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 should be tied to GND.

For more information on boxed processor requirements, refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet.*

## 4.5 Debug Port Routing Guidelines

Refer to the latest revision of the *ITP700 Debug Port Design Guide* for details on the implementation of the debug port.

### 4.5.1 Debug Tools Specifications

#### 4.5.1.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging the Pentium® 4 processor systems. Tektronix* and Agilent* should be contacted

for specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Pentium® 4 processor systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a Pentium 4 processor system that can make use of an LAI: mechanical and electrical.

#### 4.5.1.2 Mechanical Considerations

The LAI is installed between the processor socket and the Pentium 4 processor. The LAI pins plug into the socket, while the Pentium 4 processor plugs into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Pentium 4 processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include space normally occupied by the Pentium 4 processor heat sink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

#### 4.5.1.3 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models for each of the logic analyzers to be able to run system level simulations to prove that they will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

## 4.6 Intel® Pentium® 4 Processor Power Distribution Guidelines

### 4.6.1 Power Requirements

Intel recommends using an Pentium 4 processor in the 478-pin package VR Down Design Guidelines-compliant regulator for the processor system board designs. A Pentium 4 processor and VR Down Design Guidelines –compliant regulator may be integrated as part of the system board or on a module. The system board designer should properly place high-frequency and bulk-decoupling capacitors as needed between the voltage regulator and the processor to ensure that voltage fluctuations remain within *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet* specifications. See Table 4-12 for recommendations on the amount of decoupling required.

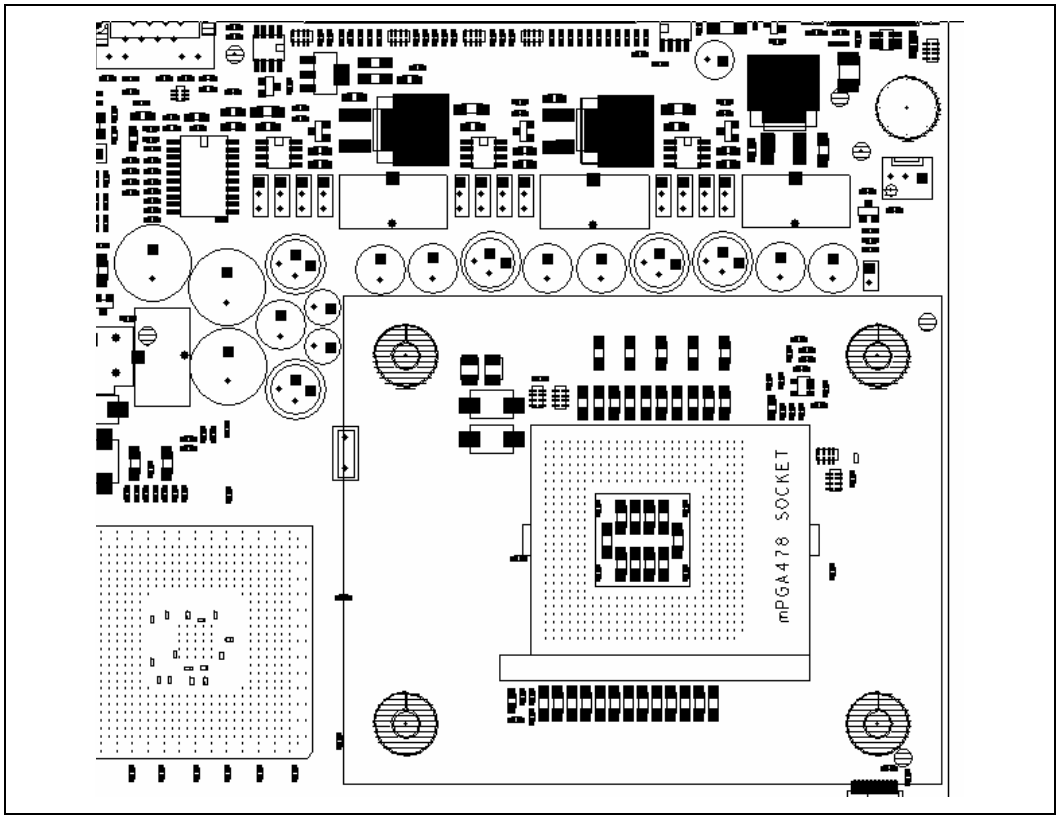
Specifications for the processor voltage are contained in the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*. These specifications are for the processor die. For guidance on correlating the die specifications to socket level measurements, refer to the socket loadlines in the *Intel® Pentium® 4 Processor in the 478 Pin Package VR Down Design Guidelines*.

The voltage tolerance of the loadlines contained in these documents helps the system designer achieve a flexible motherboard design solution for all processor frequencies. Failure to meet the load line requirements when modeling the system power delivery may result in a system that is not upgradeable.

The processor requires local regulation because of its higher current requirements, and to maintain power supply tolerance. For example, an onboard DC-to-DC converter converts a higher DC voltage to a lower level using a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R). More important, however, an onboard regulator regulates the voltage locally, which minimizes DC line losses by reducing motherboard resistance on the processor voltage. Figure 4-17 shows an example of the placement of the local voltage regulation circuitry.

In this section, North and South are used to describe a specific side of the socket based on the placement of the customer reference board shown in Figure 3-1 North refers to the side of the processor closest to the back panel, and South refers to the side of the processor closest to the system memory.

**Figure 4-17. VR Component Placement**



## 4.6.2 Decoupling Requirements

For the processor voltage regulator circuitry to meet the transient specifications of the processor, proper bulk and high-frequency decoupling is required. The decoupling requirements for the processor power delivery in this case are shown in Table 4-12.

**Table 4-12. Decoupling Requirements**

| Capacitance | ESR (Each) | ESL (Each) | Ripple Current Rating (Each) |
|---|---|---|---|
| 9 OSCONs, 560 µF | 9.28 mΩ, max | 6.4 nH, max | 4.080 $A_{rms}$ |
| 3 Al, Electolytic, 3300 µF | 12 mΩ, max | 5 nH, max | |
| 38 1206 package, 10 µF | 3.5 mΩ, typ | 1.15 nH, typ | |

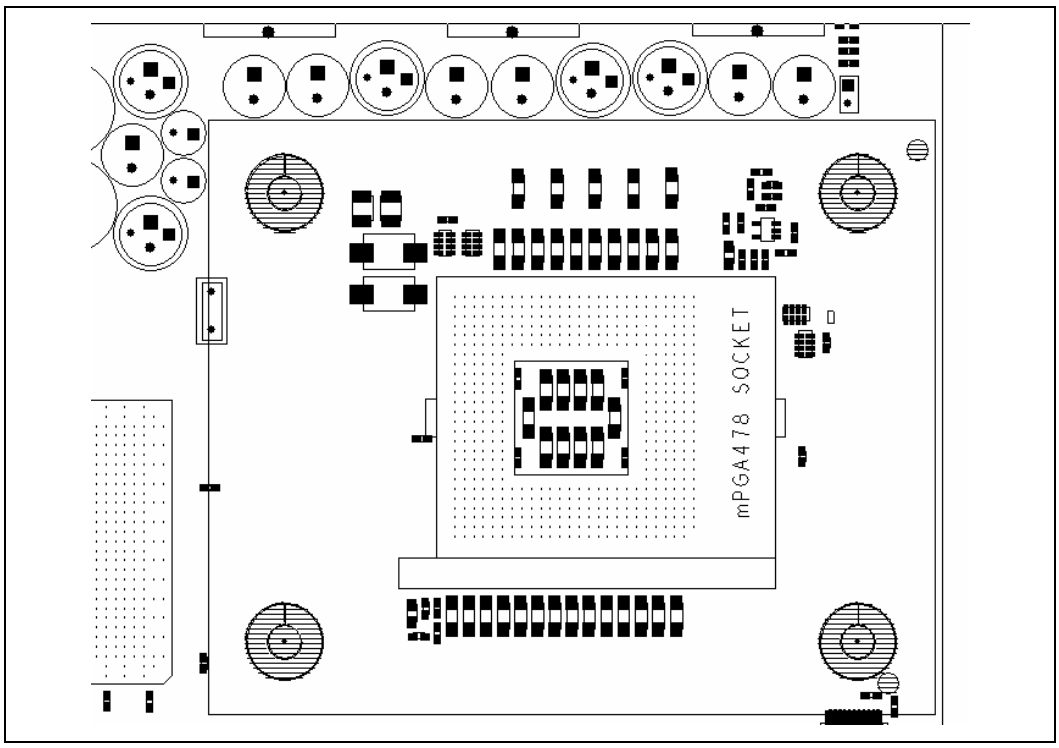
**NOTES:**
1. The ESR, ESL and ripple current values in this table are based on the values used in power delivery simulation by Intel, and are not vendor specifications.

The decoupling should be placed as close as possible to the processor power pins. Table 4-13 and Figure 4-18 describe and illustrate the recommended placement.

**Table 4-13. Decoupling Locations**

| Type | Number | Location |
|---|---|---|
| 560 µF OS-CONs | 9 | North side of the processor as close as possible to the keepout area for the retention mechanism |
| 3 Al, Electolytic, 3300 µF | 3 | North side of the processor as close as possible to the keepout area for the retention mechanism |
| 1206 package, 10 µF | 14 | North side of the processor as close as possible to the processor socket |
| 1206 package, 10 µF | 10 | Inside the processor socket cavity |
| 1206 package, 10 µF | 14 | South side of the processor as close as possible to the processor socket |

**Figure 4-18. Decoupling Placement**



### 4.6.3 Layout

All four layers in the processor area should be used for power delivery. Two layers should be used for VCC_CPU, and two layers should be used for ground. Traces are not sufficient for supplying power to the processor due to the high current and low resistance required to meet the processor voltage specifications. To satisfy these requirements, shapes that encompass the power delivery part of the processor pin field are required. Figure 4-19 through Figure 4-22 show examples of how to use shapes to deliver power to the processor.

**Figure 4-19. Top Layer Power Delivery Shape (VCC_CPU)**

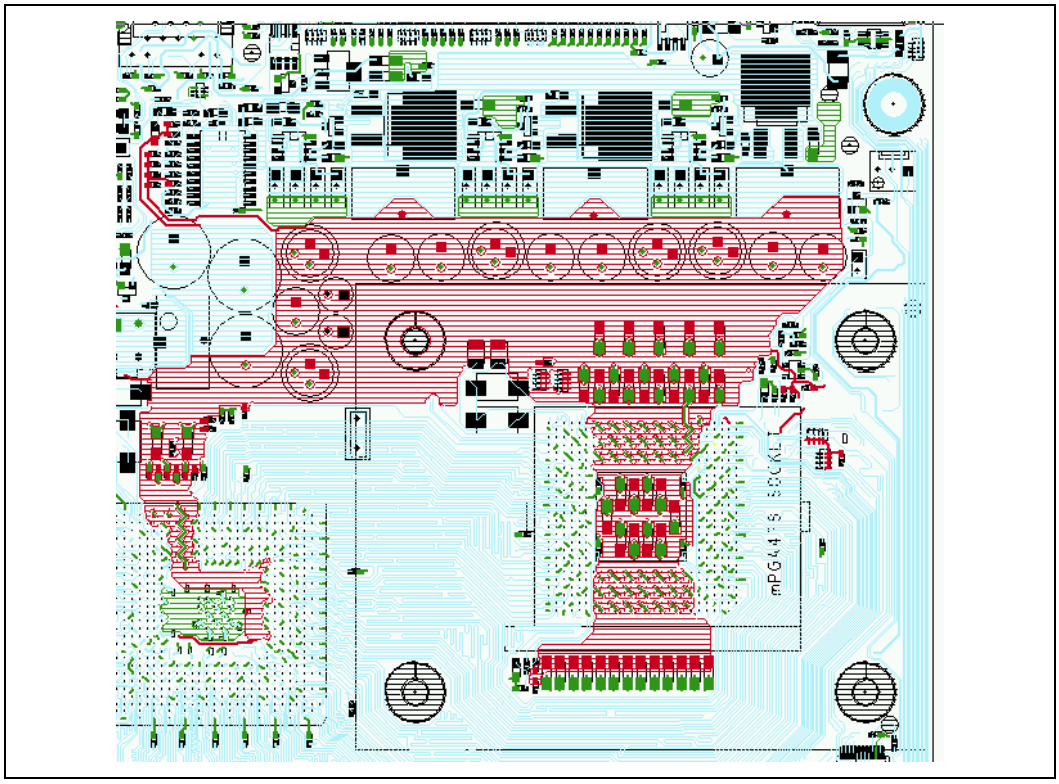


**Figure 4-20. Layer 2 Power Delivery Shape (VSS)**

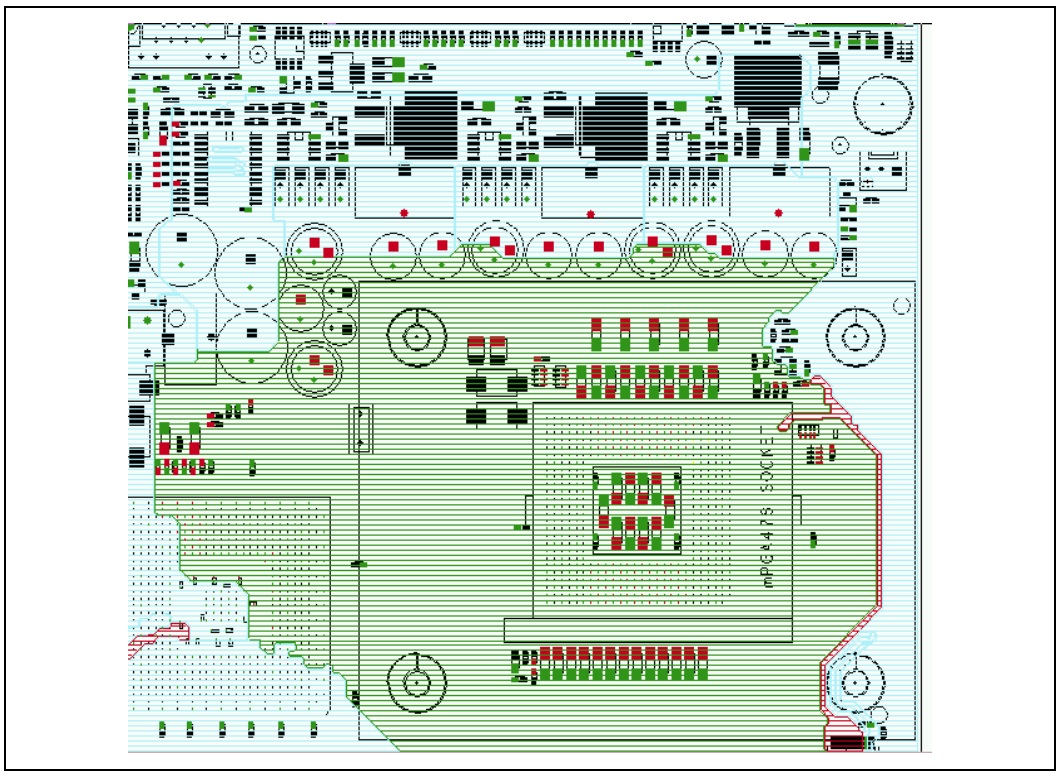



**Figure 4-21. Layer 3 Power Delivery Shape (VSS)**

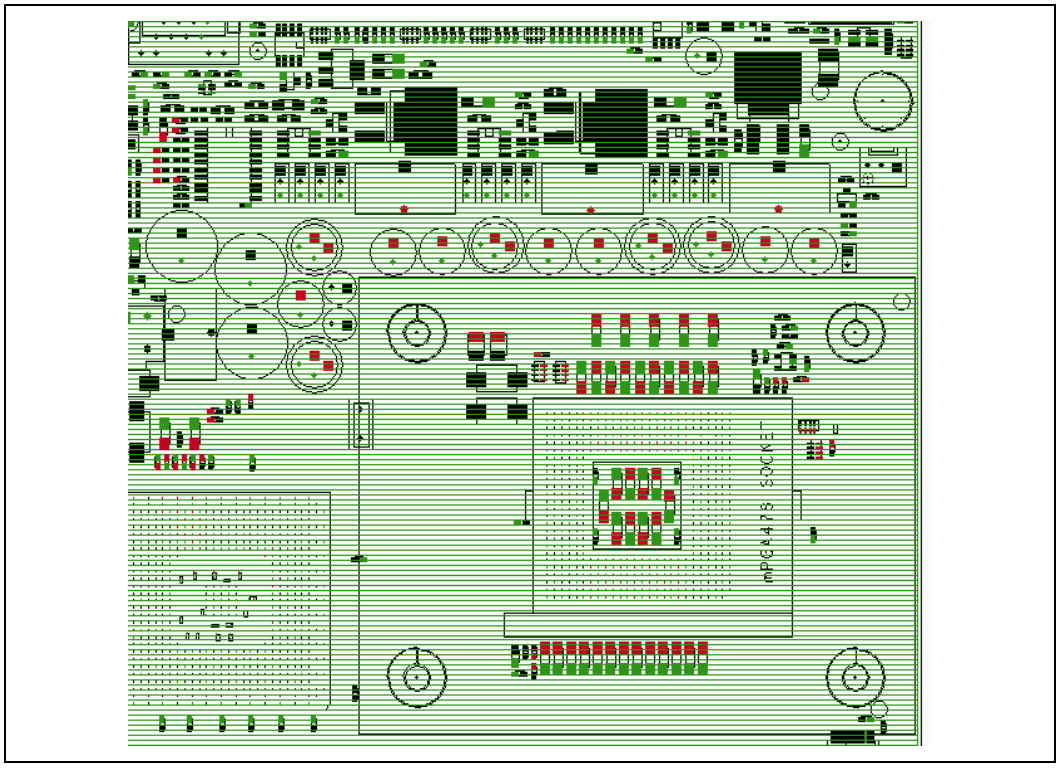
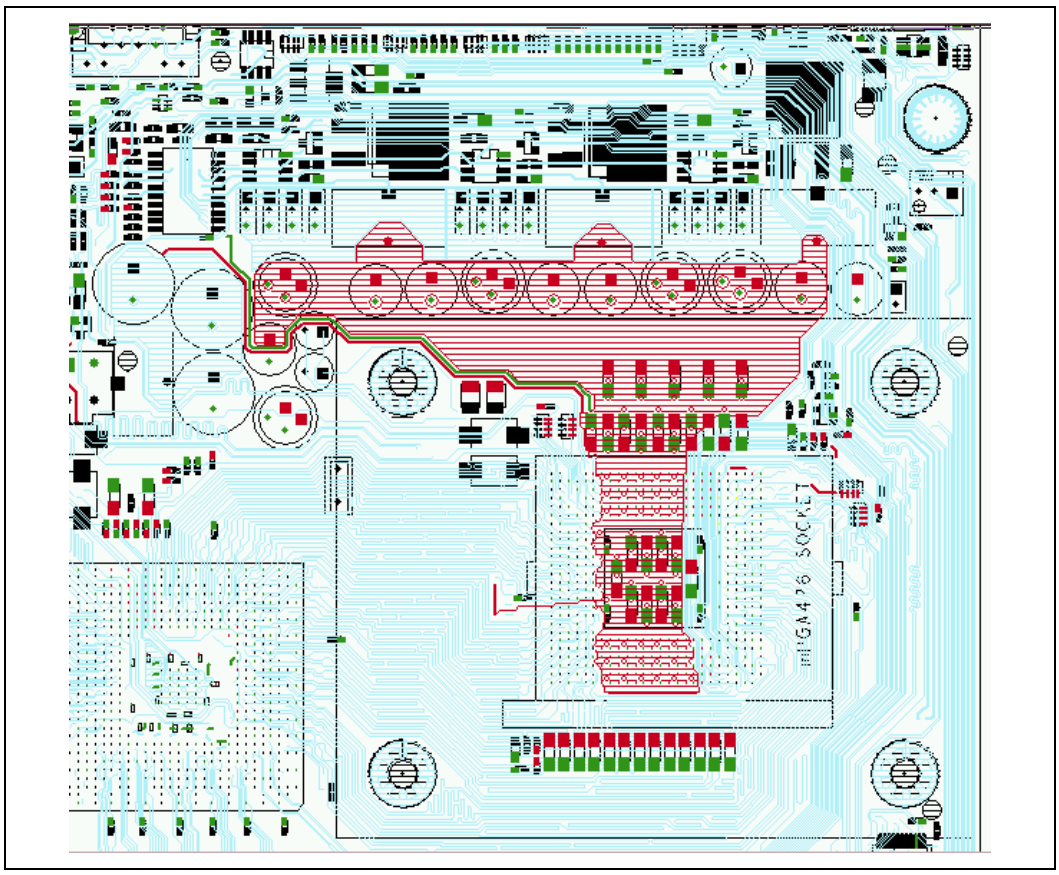
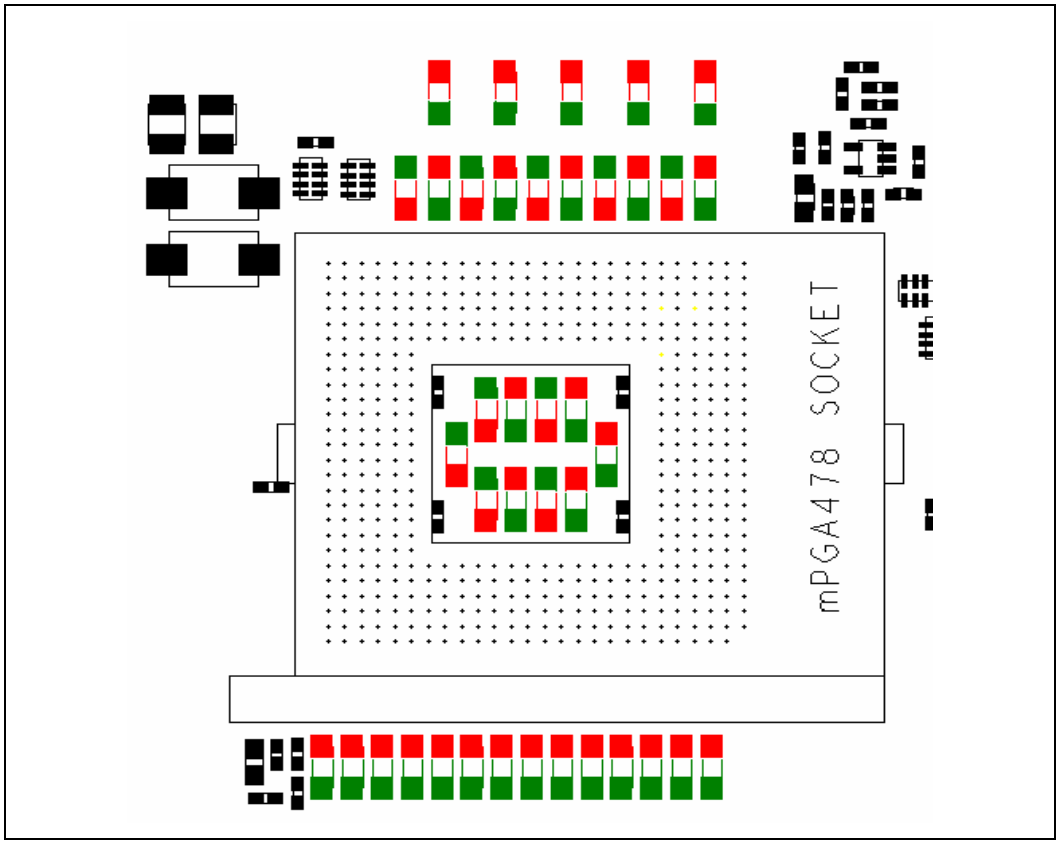


**Figure 4-22. Bottom Layer Power Delivery Shape (VCC_CPU)**



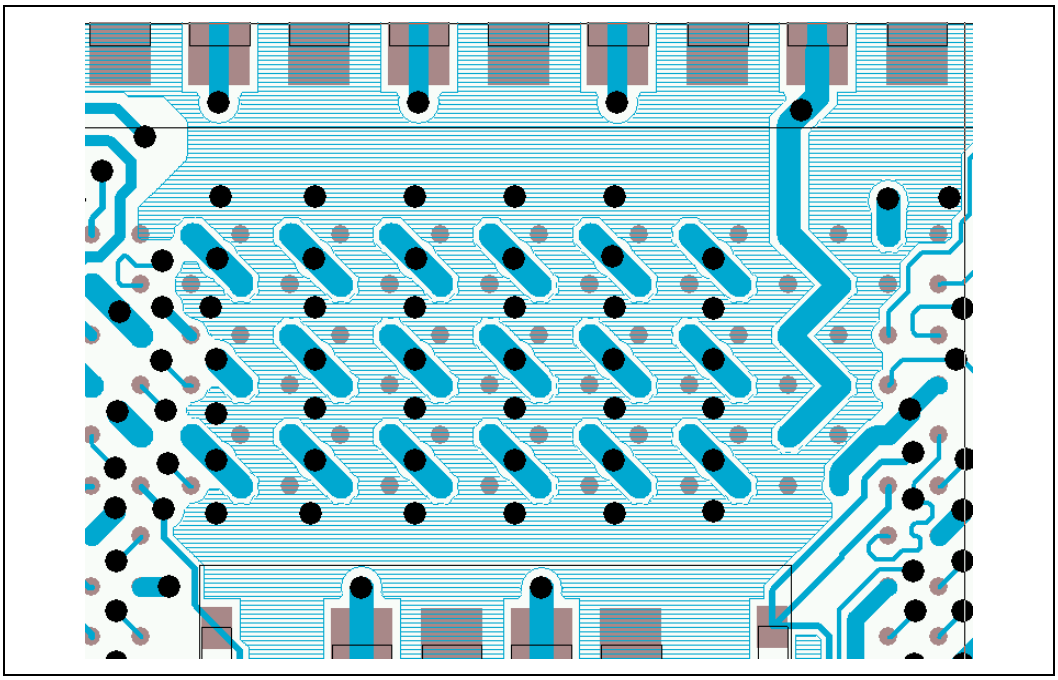
The high-frequency decoupling capacitors on the North side and within the socket cavity should be placed with alternating VCC_CPU and VSS to provide a better path for power delivery through the capacitor field. An example of this placement is shown in Figure 4-23.

**Figure 4-23. Alternating VCC_CPU/VSS Capacitor Placement**



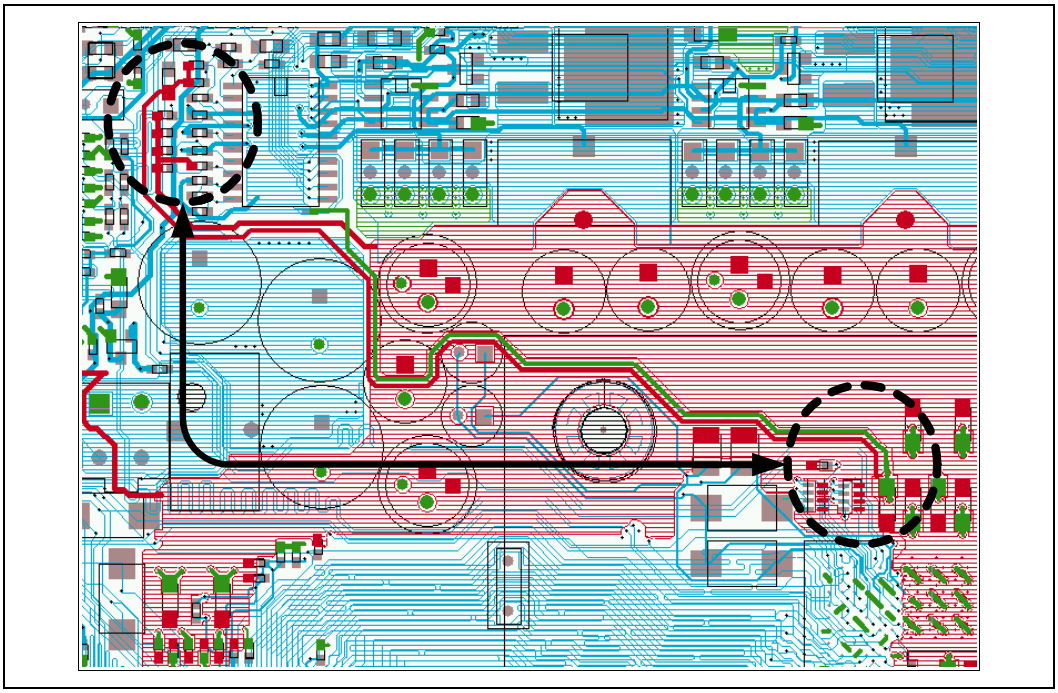
The processor socket has 478 pins with 50-mil pitch. The routing of the signals, power and ground pins require creation of many vias. These vias cut up the power and ground planes beneath the processor resulting in increased inductance of these planes. To provide the best path through the via field, it is recommended that vias be shared for two processor ground pins and for two processor power pins. Figure 4-24 illustrates this via sharing.

**Figure 4-24. Shared Power and Ground Vias**



The switching voltage regulators typically used for processor power delivery require the use of a feedback signal for output error correction. The VCC_SENSE and VSS_SENSE pins on the processor should not be used for generating this feedback. These pins should be used as measurement points for lab measurements only. They can be routed to a test point or via on the back of the motherboard with a trace that is a maximum length of 100 mils for this purpose. The socket loadline defined in the *Intel® Pentium® 4 Processor VR Down Design Guidelines* is defined from pins AC14 (VCC_CPU) and AC15 (VSS) and should be validated from these pins as well. These pins are located approximately in the center of the pin field on the North side of the processor. Feedback for the voltage regulator controller should therefore be taken close to this area of the power delivery shape. Figure 4-25 shows an example routing of the feedback signal. It is routed as a trace from the 1206 capacitor in the Northwest corner of the processor back to the voltage regulator controller. Because the feedback in this case is not taken from the exact point that defines the socket loadline (pins AC14/AC15), it is important to consider any voltage drop from the feedback point to these pins in the design.

**Figure 4-25. Routing of VR Feedback Signal**



## 4.6.4 Thermal Considerations

For a power delivery solution to meet the flexible motherboard (FMB) requirements, it must be able to deliver a high amount of current. This high amount of current also requires that the solution be able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow, and layout to ensure adequate thermal performance of the processor power delivery solution.

## 4.6.5 Simulation

To completely model the system board, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins and body of components (such as resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in Figure 4-26.

**Figure 4-26. Detailed Power Distribution Model for Processor with Voltage Regulator on System Board**

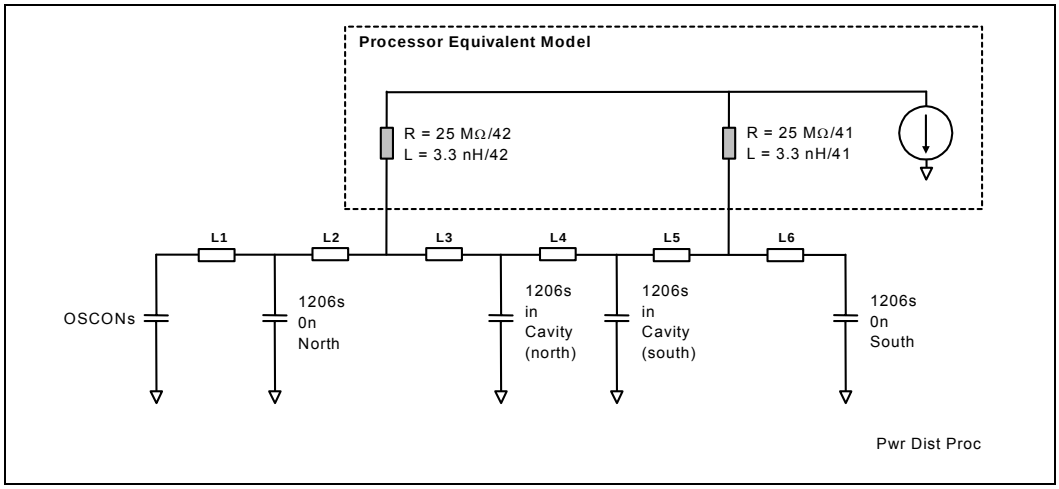



Table 4-14 lists model parameters for the system board shown in Figure 3-1.

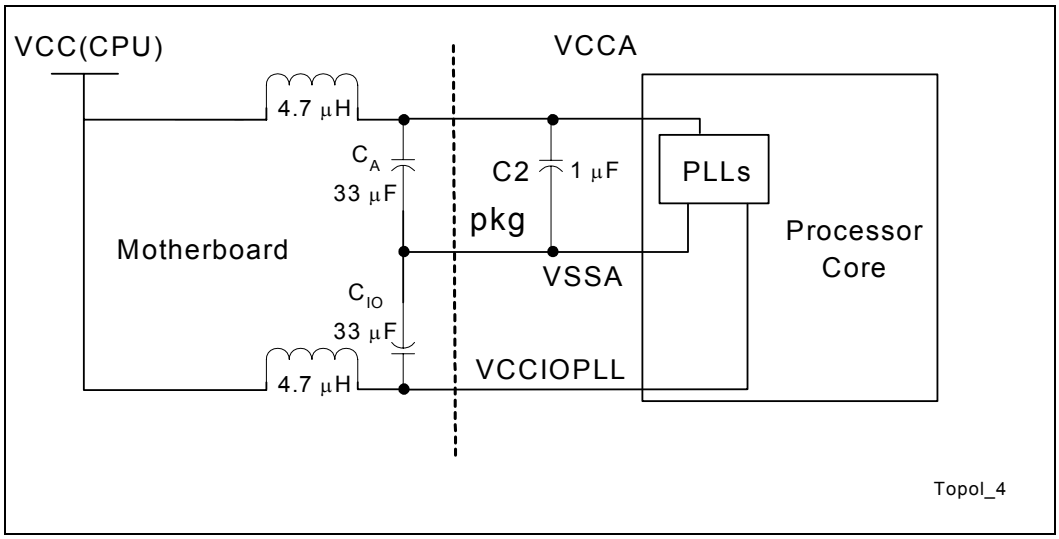
**Table 4-14. Intel® Pentium® 4 Processor Power Delivery Model Parameters**

| Segment | Resistance | Inductance |
|---|---|---|
| L1 | 0.27 mΩ | 80 pH |
| L2 | 0.33 mΩ | 113 pH |
| L3 | 0.392 mΩ | 104 pH |
| L4 | 0.196 mΩ | 52 pH |
| L5 | 0.392 mΩ | 104 pH |
| L6 | 0.64 mΩ | 200 pH |

### 4.6.5.1 Filter Specifications For VCCA, VCCIOPLL, and VSSA

VCCA and VCCIOPLL are power sources required by the PLL clock generators on the processor silicon. Because these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system. It degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from VCC. The general desired filter topology is shown in Figure 4-27. Not shown in the core is parasitic routing. Excluded from the external circuitry are parasitics associated with each component.

**Figure 4-27. Typical VCCIOPLL, VCCA and VSSA Power Distribution**




The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity this document will address the recommendation for the VCCA filter design. The same characteristics and design approach is applicable for the VCCIOPLL filter design.

The AC low-pass recommendation, with input at VCC and output measured across the capacitor (CA or CIO in Figure 4-27), is as follows:

< 0.2 dB gain in pass band.

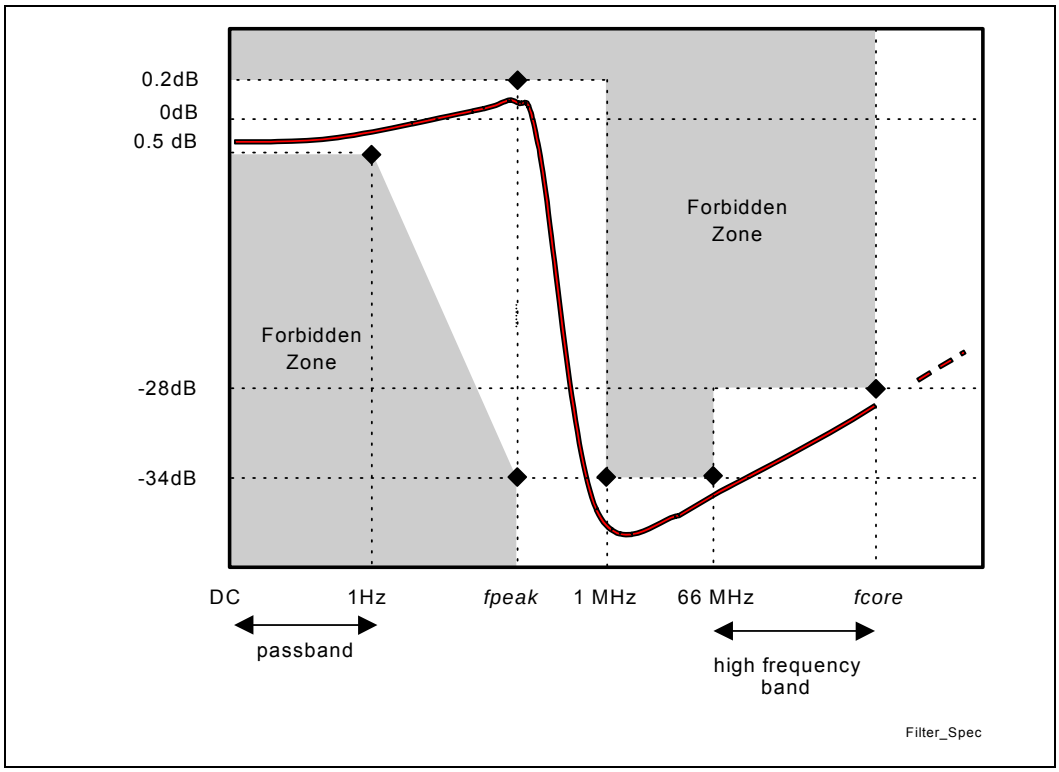
< 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements).

> 34 dB attenuation from 1 MHz to 66 MHz.

> 28 dB attenuation from 66 MHz to core frequency.

The filter recommendation (AC) is graphically shown in Figure 4-28.

**Figure 4-28. Filter Recommendation**

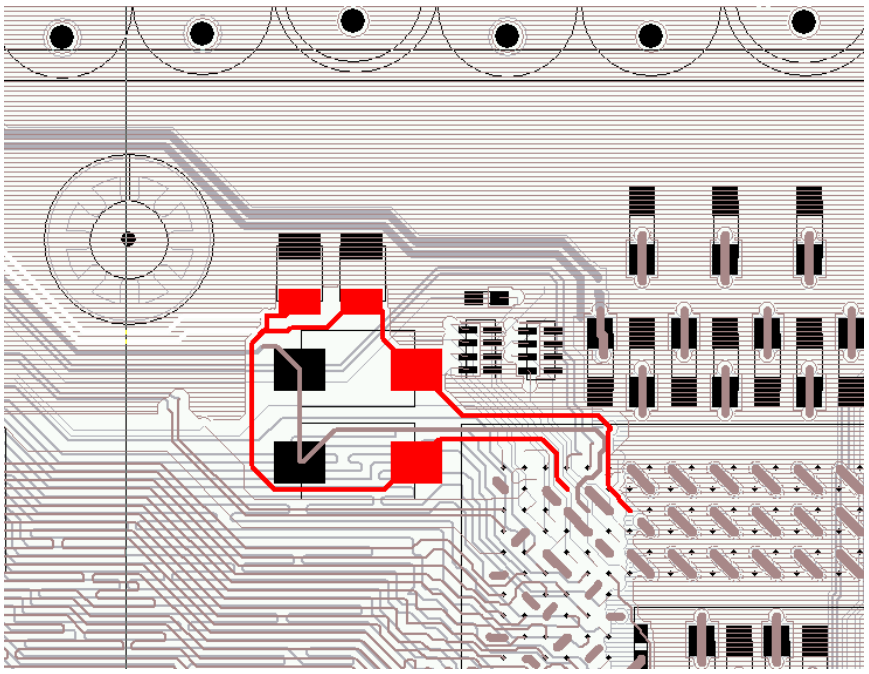



**NOTES:**
1. Diagram not to scale.
2. No specification for frequencies beyond fcore (core frequency).
3. Fpeak, if existent, should be less than 0.05 MHz.

## Other Recommendations

1. Use shielded type inductors to minimize magnetic pickup.
2. Capacitors for the filters can have any value between 22 µF and 100 µF as long as components with ESL ≤ 5 nH and ESR <0.3 Ω are used.
3. Values of either 4.7 uH or 10 uH may be used for the inductor.
4. Filter should support DC current > 60 mA.
5. DC voltage drop from VCC to VCCA should be < 60 mV.
6. To maintain a DC drop of less than 60 mV, the total DC resistance of the filter from VCC_CPU to the processor socket should be a maximum of 1 Ω.
7. Other routing requirements:
   - C should be within 600 mils of the VCCA and VSSA pins. An example of the component placement is shown in Figure 4-29.
   - VCCA route should be parallel and next to VSSA route (minimize loop area).
   - A minimum 12 mil trace should be used to route from the filter to the processor pins.
   - L should be close to C.

**Figure 4-29. Example Component Placement of PLL Filter**



## 4.7 Intel® Pentium® 4 Processor and Intel® 845E Chipset Package Lengths

| Processor Lengths | | | MCH Lengths | | |
|---|---|---|---|---|---|
| **Signal** | **Processor ball** | **Length (inches)** | **Signal** | **MCH ball** | **Length (inches)** |
| **Address Group 0** | | | | | |
| ADSTB0# | L5 | 0.210 | HADSTB0# | R5 | 0.530 |
| A03# | K2 | 0.368 | HA03# | T4 | 0.518 |
| A04# | K4 | 0.265 | HA04# | T5 | 0.434 |
| A05# | L6 | 0.155 | HA05# | T3 | 0.728 |
| A06# | K1 | 0.415 | HA06# | U3 | 0.577 |
| A07# | L3 | 0.304 | HA07# | R3 | 0.551 |
| A08# | M6 | 0.144 | HA08# | P7 | 0.359 |
| A09# | L2 | 0.372 | HA09# | R2 | 0.643 |
| A10# | M3 | 0.327 | HA10# | P4 | 0.533 |
| A11# | M4 | 0.246 | HA11# | R6 | 0.397 |
| A12# | N1 | 0.394 | HA12# | P5 | 0.463 |
| A13# | M1 | 0.408 | HA13# | P3 | 0.576 |
| A14# | N2 | 0.349 | HA14# | N2 | 0.660 |
| A15# | N4 | 0.241 | HA15# | N7 | 0.407 |
| A16# | N5 | 0.198 | HA16# | N3 | 0.570 |
| REQ0# | J1 | 0.427 | HREQ0# | U6 | 0.402 |
| REQ1# | K5 | 0.207 | HREQ1# | T7 | 0.350 |
| REQ2# | J4 | 0.270 | HREQ2# | R7 | 0.393 |
| REQ3# | J3 | 0.337 | HREQ3# | U5 | 0.475 |
| REQ4# | H3 | 0.356 | HREQ4# | U2 | 0.599 |
| **Address Group 1** | | | | | |
| ADSTB1# | R5 | 0.214 | HADSTB1# | N6 | 0.438 |
| A17# | T1 | 0.470 | HA17# | K4 | 0.550 |
| A18# | R2 | 0.404 | HA18# | M4 | 0.580 |
| A19# | P3 | 0.303 | HA19# | M3 | 0.648 |
| A20# | P4 | 0.246 | HA20# | L3 | 0.604 |
| A21# | R3 | 0.334 | HA21# | L5 | 0.521 |
| A22# | T2 | 0.388 | HA22# | K3 | 0.624 |

| Processor Lengths | | | MCH Lengths | | |
|---|---|---|---|---|---|
| **Signal** | **Processor ball** | **Length (inches)** | **Signal** | **MCH ball** | **Length (inches)** |
| A23# | U1 | 0.458 | HA23# | J2 | 0.685 |
| A24# | P6 | 0.156 | HA24# | M5 | 0.509 |
| A25# | U3 | 0.379 | HA25# | J3 | 0.636 |
| A26# | T4 | 0.281 | HA26# | L2 | 0.648 |
| A27# | V2 | 0.417 | HA27# | H4 | 0.634 |
| A28# | R6 | 0.166 | HA28# | N5 | 0.472 |
| A29# | W1 | 0.493 | HA29# | G2 | 0.792 |
| A30# | T5 | 0.217 | HA30# | M6 | 0.449 |
| A31# | U4 | 0.285 | HA31# | L7 | 0.365 |
| **Data Group 0** | | | | | |
| DSTBN0# | E22 | 0.338 | HDSTBN0# | AD4 | 0.759 |
| DSTBP0# | F21 | 0.326 | HDSTBP0# | AD3 | 0.801 |
| D00# | B21 | 0.414 | HD00# | AA2 | 0.649 |
| D01# | B22 | 0.475 | HD01# | AB5 | 0.564 |
| D02# | A23 | 0.538 | HD02# | AA5 | 0.531 |
| D03# | A25 | 0.608 | HD03# | AB3 | 0.678 |
| D04# | C21 | 0.386 | HD04# | AB4 | 0.628 |
| D05# | D22 | 0.386 | HD05# | AC5 | 0.635 |
| D06# | B24 | 0.535 | HD06# | AA3 | 0.623 |
| D07# | C23 | 0.464 | HD07# | AA6 | 0.468 |
| D08# | C24 | 0.515 | HD08# | AE3 | 0.802 |
| D09# | B25 | 0.590 | HD09# | AB7 | 0.495 |
| D10# | G22 | 0.274 | HD10# | AD7 | 0.609 |
| D11# | H21 | 0.203 | HD11# | AC7 | 0.548 |
| D#12 | C26 | 0.589 | HD12# | AC6 | 0.579 |
| D13# | D23 | 0.462 | HD13# | AC3 | 0.709 |
| D14# | J21 | 0.183 | HD14# | AC8 | 0.590 |
| D15# | D25 | 0.550 | HD15# | AE2 | 0.856 |
| DBI0# | E21 | 0.309 | DBI0# | AD5 | 0.637 |
| **Data Group 1** | | | | | |
| DSTBN1# | K22 | 0.301 | HDSTBN1# | AE6 | 0.693 |
| DSTBP1# | J23 | 0.306 | HDSTBP1# | AE7 | 0.638 |
| D16# | H22 | 0.272 | HD16# | AG5 | 0.845E |

| Processor Lengths | | | MCH Lengths | | |
|---|---|---|---|---|---|
| **Signal** | **Processor ball** | **Length (inches)** | **Signal** | **MCH ball** | **Length (inches)** |
| D17# | E24 | 0.480 | HD17# | AG2 | 0.904 |
| D18# | G23 | 0.358 | HD18# | AE8 | 0.663 |
| D19# | F23 | 0.418 | HD19# | AF6 | 0.759 |
| D20# | F24 | 0.443 | HD20# | AH2 | 0.965 |
| D21# | E25 | 0.508 | HD21# | AF3 | 0.798 |
| D22# | F26 | 0.513 | HD22# | AG3 | 0.898 |
| D23# | D26 | 0.597 | HD23# | AE5 | 0.709 |
| D24# | L21 | 0.176 | HD24# | AH7 | 0.863 |
| D25# | G26 | 0.524 | HD25# | AH3 | 0.904 |
| D26# | H24 | 0.412 | HD26# | AF4 | 0.794 |
| D27# | M21 | 0.171 | HD27# | AG8 | 0.789 |
| D28# | L22 | 0.245 | HD28# | AG7 | 0.785 |
| D29# | J24 | 0.401 | HD29# | AG6 | 0.785 |
| D30# | K23 | 0.313 | HD30# | AF8 | 0.711 |
| D31# | H25 | 0.473 | HD31# | AH5 | 0.892 |
| DBI1# | G25 | 0.458 | DINVB_1 | AG4 | 0.888 |
| **Data Group 2** | | | | | |
| DSTBN2# | K22 | 0.252 | HDSTBN2# | AE11 | 0.595 |
| DSTBP2# | J23 | 0.266 | HDSTBP2# | AD11 | 0.532 |
| D32# | M23 | 0.300 | HD32# | AC11 | 0.514 |
| D33# | N22 | 0.226 | HD33# | AC12 | 0.565 |
| D34# | P21 | 0.178 | HD34# | AE9 | 0.652 |
| D35# | M24 | 0.371 | HD35# | AC9 | 0.566 |
| D36# | N23 | 0.271 | HD36# | AE10 | 0.605 |
| D37# | M26 | 0.454 | HD37# | AD9 | 0.635 |
| D38# | N26 | 0.437 | HD38# | AG9 | 0.724 |
| D39# | N25 | 0.383 | HD39# | AC10 | 0.543 |
| D40# | R21 | 0.165 | HD40# | AE12 | 0.558 |
| D41# | P24 | 0.343 | HD41# | AF10 | 0.666 |
| D42# | R25 | 0.381 | HD42# | AG11 | 0.703 |
| D43# | R24 | 0.329 | HD43# | AG10 | 0.705 |
| D44# | T26 | 0.420 | HD44# | AH11 | 0.754 |
| D45# | T25 | 0.380 | HD45# | AG12 | 0.669 |
| D46# | T22 | 0.221 | HD46# | AE13 | 0.563 |

| Processor Lengths | | | MCH Lengths | | |
|---|---|---|---|---|---|
| **Signal** | **Processor ball** | **Length (inches)** | **Signal** | **MCH ball** | **Length (inches)** |
| D47# | T23 | 0.279 | HD47# | AF12 | 0.596 |
| DBI2# | P26 | 0.441 | DINVB_2 | AH9 | 0.775 |
| **Data Group 3** | | | | | |
| DSTBN3# | W22 | 0.298 | HDSTBN3# | AC15 | 0.443 |
| DSTBP3# | W23 | 0.300 | HDSTBP3# | AC16 | 0.395 |
| D48# | U26 | 0.419 | HD48# | AG13 | 0.668 |
| D49# | U24 | 0.324 | HD49# | AH13 | 0.712 |
| D50# | U23 | 0.270 | HD50# | AC14 | 0.412 |
| D51# | V25 | 0.384 | HD51# | AF14 | 0.548 |
| D52# | U21 | 0.167 | HD52# | AG14 | 0.621 |
| D53# | V22 | 0.252 | HD53# | AE14 | 0.520 |
| D54# | V24 | 0.341 | HD54# | AG15 | 0.612 |
| D55# | W26 | 0.447 | HD55# | AG16 | 0.610 |
| D56# | Y26 | 0.454 | HD56# | AG17 | 0.619 |
| D57# | W25 | 0.426 | HD57# | AH15 | 0.703 |
| D58# | Y23 | 0.336 | HD58# | AC17 | 0.399 |
| D59# | Y24 | 0.386 | HD59# | AF16 | 0.580 |
| D60# | Y21 | 0.222 | HD60# | AE15 | 0.534 |
| D61# | AA25 | 0.426 | HD61# | AH17 | 0.672 |
| D62# | AA22 | 0.268 | HD62# | AD17 | 0.419 |
| D63# | AA24 | 0.394 | HD63# | AE16 | 0.503 |
| DBI3# | V21 | 0.202 | DINVB_3 | AD15 | 0.431 |

§

# 5 Double Data Rate Synchronous DRAM (DDR-SDRAM) System Memory Design Guidelines

## 5.1 Introduction

The Intel® 845E chipset Double Data Rate (DDR) SDRAM system memory interface consists of 120 CMOS signals. These CMOS signals have been divided into several signal groups: Data, Command, Control, Feedback, and Clock signals. Table 5-1 summarizes the different signal groupings. Refer to the *Intel® 845E Chipset Memory Controller Hub (MCH) External Design Specification Datasheet* for details on the signals listed in Table 5-1

The MCH AGP ST[0] signal is sampled by the MCH on power-on to indicate what system memory mode, SDR or DDR, the MCH should configure and operate at. An internal MCH pull-up resistor on this signal sets the default system memory configuration to PC133 SDRAM. To enable the MCH to operate in DDR mode an external pull-down resistor to ground is required on ST[0]. The recommended pull-down resistor is 2 kΩ.

**Table 5-1. Intel® 845E Chipset DDR Signal Groups**

| Group | Signal Name | Description |
|---|---|---|
| Data | SDQ[63:0] | Data Bus |
| | SCB[7:0] | Check Bits for ECC Function |
| | SDQS[8:0] | Data Strobes |
| | | |
| Command | SMA[12:0] | Memory Address Bus |
| | SBS[1:0] | Bank Select |
| | SRAS# | Row Address Select |
| | SCAS# | Column Address Select |
| | SWE# | Write Enable |
| | | |
| Control | SCKE[3:0] | Clock Enable - (One per Device Row) |
| | SCS#[3:0] | Chip Select – (One per Device Row) |
| | | |
| Feedback | RCVENOUT# | Output Feedback Signal |
| | RCVENIN# | Input Feedback Signal |
| | | |
| Clocks | SCK[5:0] | DDR-SDRAM Differential Clocks – (3 per DIMM) |
| | SCK#[5:0] | DDR-SDRAM Inverted Differential Clocks – (3 per DIMM) |

### 5.1.1 Data Mask (DQM) Signals

The 845E chipset does not support data masking. The system memory DQM[7:0] pins on the DDR-DIMMs must be tied to ground.

## 5.2 DDR-SDRAM Stack-up and Referencing Guidelines

Intel 845E chipset designs using the DDR-SDRAM memory sub system require continuous ground referencing for all DDR signals. Based on the four-layer stack-up in section 0 the DDR channel requires the following referencing stack-up in order to ground reference all of the DDR signals from the MCH to the parallel termination at the end of the channel.

***Note:*** Note this only applies to the DDR channel and doesn't effect any of the other interfaces

**Table 5-2. DDR Channel Referencing Stack-up**

| Motherboard Layer | Description |
|---|---|
| Layer 1 | Signal |
| Layer 2 | Ground Flood |
| Layer 3 | Ground |
| Layer 4 | Power/Signal |

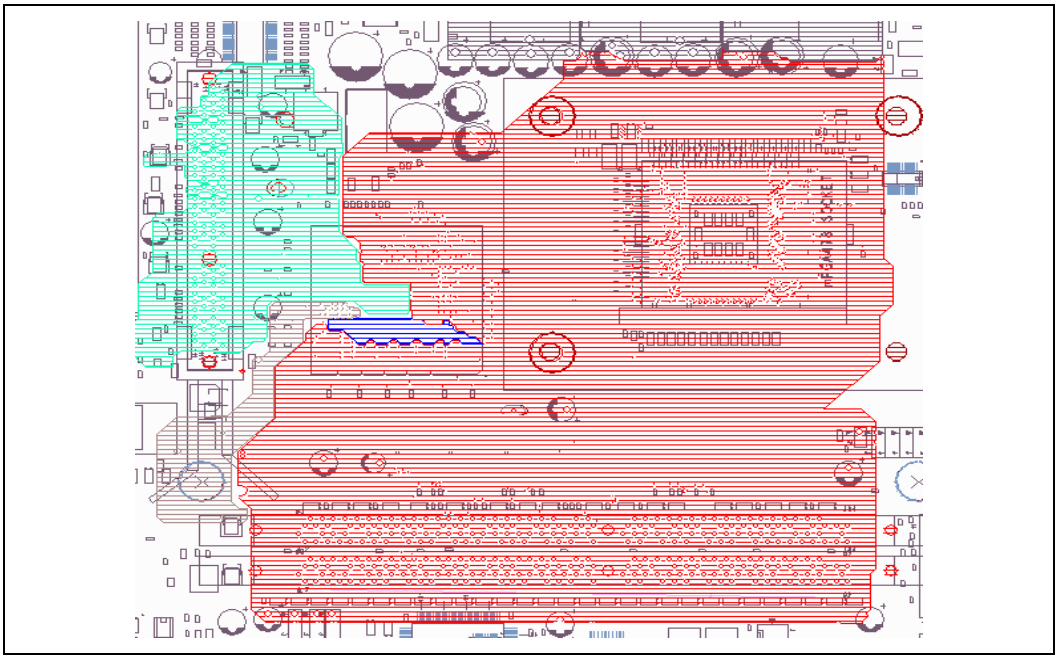
All DDR signals must be ground referenced to provide an optimal current return path. In order to do this a solid ground flood needs be placed on layer two under the DDR channel. This ground flood must be solid and continuous from the MCH DDR signal pins all the way beyond the Vtt termination capacitors at the end of the channel. The return current for the DDR signals will flow through the Vtt termination capacitors at the end of the channel into the ground flood under the DDR traces on the top signal layer. Any split in the ground flood will provide a sub-optimal return path. As a result, there should not be any splits in this flood.

The ground flood must be well stitched to the ground plane on layer three to ensure the same potential between the two.

- The DIMM connector ground pins must connect to both the ground flood and the ground plane.
- The MCH DDR ground pins, in the DDR interface section, must connect to both the ground flood and the ground plane through a via.
- Any ground via that is placed in the DDR routing area, must connect to both the ground flood and the ground plane.
- The ground ends of the DDR-DIMM high-frequency bypass and low-frequency bulk capacitors must connect to both the ground flood and the ground plane.
- The ground vias for the MCH 2.5 V high-frequency decoupling capacitors must connect to both the ground flood and the ground plane.
- The ground ends of the Vtt termination high-frequency decoupling and low-frequency bulk capacitors must connect to both the ground flood and the ground plane.

- The processor and the DDR ground floods on layer two must be connected to each other in order to create one large ground flood. Ground vias connecting the ground flood and the ground plane should be placed wherever possible around the edge of the ground flood. It is also recommended that vias between the ground flood and the ground plane be placed around the edge where the DDR and FSB ground floods connect on layer two.

**Figure 5-1. Layer Two Ground Flood Picture**



## 5.3 DDR System Memory Topology and Layout Design Guidelines

The 845E chipset Double Data Rate (DDR) SDRAM system memory interface implements the low swing, high speed, terminated SSTL_2 topology. It supports one DDR SDRAM channel with two DDR-DIMMs.

This section contains information and details on the DDR topologies, the DDR layout and routing guidelines, and the DDR power delivery requirements that will provide for a robust DDR solution on a two DIMM 845E chipset-based design.

Based on the four-layer DDR referencing stack-up detailed in Section 5.2, the MCH system memory ball field, and the fact that all DDR signals must be ground referenced the following DDR-SDRAM system memory guidelines should be followed in a 845E chipset DDR-SDRAM based system

## 5.3.1 Data Signals – SDQ[63:0], SDQS[8:0], SCB[7:0]

The MCH data signals are source synchronous signals that include the 64-bit wide data bus, 8 check bits for Error Checking and Correction (ECC), and 9 data strobe signals. There is an associated data strobe (DQS) for each data (DQ) and check bit (CB) group. Table 5-4 summarizes the DQ/CB to DQS mapping.

The MCH system memory pin out has been optimized to breakout all the data and strobe signals on the top signal layer. The data signals must break out of the MCH and route entirely on the top signal layer referenced to ground, from the MCH to the series termination resistor, from the series termination resistor to the first DIMM, from DIMM to DIMM, and from the second DIMM to the parallel termination.

Resistor packs are acceptable for the series (Rs) and parallel (Rt) data and strobe termination resistors but data and strobe signals can NOT be placed within the same RPACK's as the command or control signals.

The table and diagrams below depict the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

**Figure 5-2. Data Signal Routing Topology**

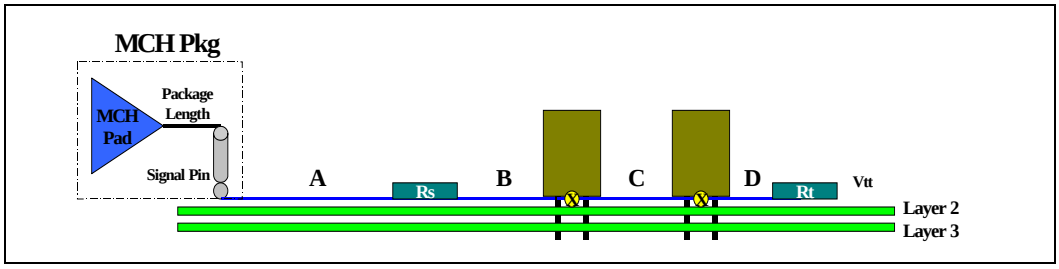
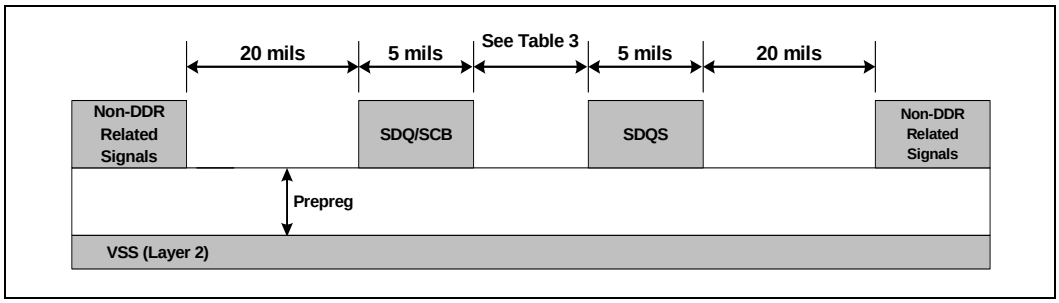



**Table 5-3. Data Group Routing Guidelines**

| Parameter | Routing Guidelines | Figure |
|---|---|---|
| Signal Group | Data – SDQ[63:0], SCB[7:0], SDQS[8:0] | |
| Topology | Daisy Chain | 5-2 |
| Reference Plane | Ground Referenced | 5-2 |
| Characteristic Trace Impedance (Zo) | 60Ω +/- 15% | |
| Trace Width | 5 mils | 5-3 |
| Trace Spacing | • MCH to 1st DIMM = 12 mils<br>• Within DIMM Pin Field = 7 mils minimum<br>• From DIMM to DIMM = 12 mils<br>• 2nd DIMM to Rt = 7 mils minimum | 5-3 |
| Group Spacing | Isolation spacing from non-DDR related signals = 20 mils minimum | 5-3 |

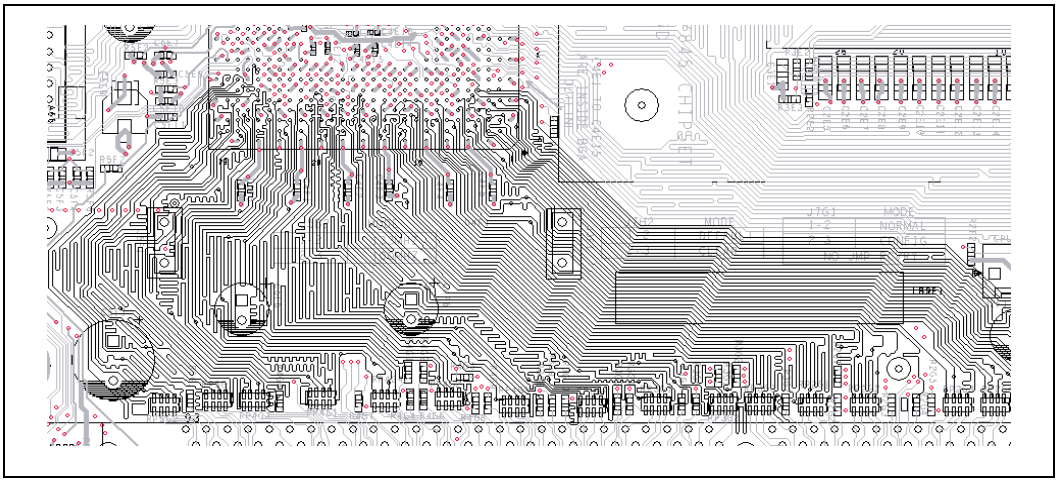
| Parameter | Routing Guidelines | Figure |
|---|---|---|
| Trace Length A – MCH signal Ball to Series Termination Resistor Pad | Min = 2.0”<br>Max = 5.0” | 5-2 |
| Trace Length B – Series Termination Resistor Pad to First DIMM Pin | Max = 500mils | 5-2 |
| Trace Length C – DIMM Pin to DIMM Pin | Min = 300mils<br>Max = 500mils | 5-2 |
| Trace Length D – Last DIMM Pin to Parallel termination Resistor Pad | Min = 100mils<br>Max = 800mils | 5-2 |
| Series Resistor (Rs) | 33Ω +/- 5% | |
| Termination Resistor (Rtt) | 47Ω +/- 5% | |
| Maximum via Count per signal | 0 | 5-2 |
| MCH Breakout Guidelines | 5 mil width with 7 mil spacing for a max of 350 mils. | |
| Length Matching Requirements | • SDQ[63:0], SCB[7:0] to SDQS[8:0]<br>• SDQS[8:0] to SCK/SCK#[5:0]<br>• See section 5.3.1.2 for details | 5-5,5-6 |

**Figure 5-3. Data Group Signal Trace Width/Spacing Routing**



#### 5.3.1.1 Routing Example – SDQ[63:0], SCB[7:0], SDQS[8:0]

**Figure 5-4. Data Group Top Signal Layer Routing Example to First DIMM**



### 5.3.1.2 Data Group Signal Length Matching Requirements

#### 5.3.1.2.1 Data to Strobe Length Matching Requirements

The data signals, SDQ[63:0], and check bit signals, SCB[7:0], for a byte group require the matching of the trace lengths from MCH pad to the pins on the first **AND** second DIMM connectors within ±25 mils of its associated data strobe, SDQS[8:0].

SDQS Length = X

Associated SDQ/SCB Byte Group Length = Y, where ( X – 25 mils ) ≤ Y ≤ ( X + 25 mils )

***Note:*** - 1st DIMM length X and Y include: MCH Package Length + Motherboard Length A + Motherboard Length B
- 2nd DIMM length X and Y include: MCH Package Length + Motherboard Length A + Motherboard Length B + Motherboard Length C
- Motherboard lengths A, B, and C are documented in Table 5-3. No length matching is required from the 2nd DIMM to the parallel termination resistors.
– Refer to section 5.6 for MCH data and strobe package length data.

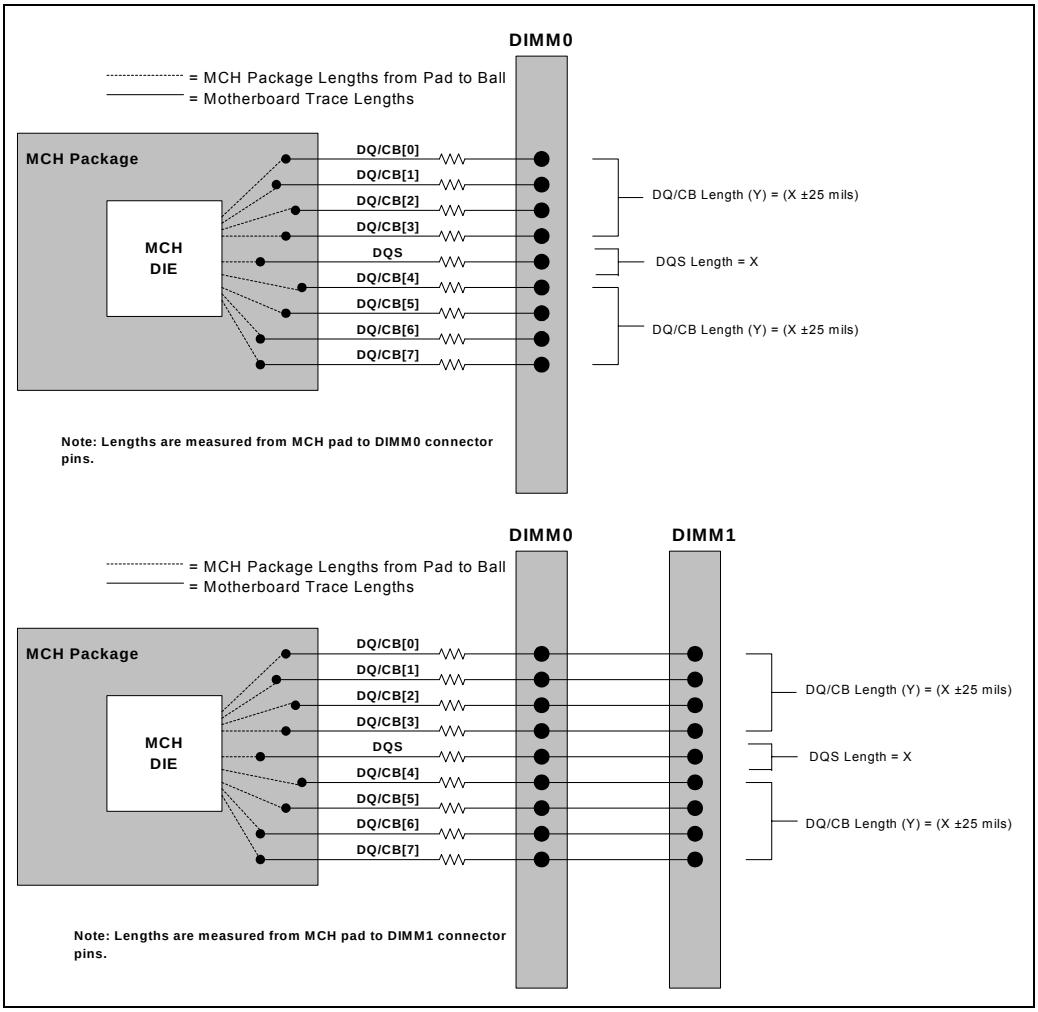
The table and diagram below depict the length matching requirements between the DQ, CB, and DQS signals.

**Table 5-4. DQ/CB to DQS Length Mismatch Mapping**

| Signal | Length Mismatch | Relative To |
|---|---|---|
| SDQ[7:0] | ±25 mils | SDQS0 |
| SDQ[15:8] | ±25 mils | SDQS1 |
| SDQ[23:16] | ±25 mils | SDQS2 |
| SDQ[31:24] | ±25 mils | SDQS3 |

| Signal | Length Mismatch | Relative To |
|---|---|---|
| SDQ[39:32] | ±25 mils | SDQS4 |
| SDQ[47:40] | ±25 mils | SDQS5 |
| SDQ[55:48] | ±25 mils | SDQS6 |
| SDQ[63:56] | ±25 mils | SDQS7 |
| SCB[7:0] | ±25 mils | SDQS8 |

**Figure 5-5. DQ/CB to DQS Trace Length Matching Requirements**




### 5.3.1.2.2 Strobe to Clock Length Matching Requirements

The data strobe lengths, SDQS[8:0], going from the MCH pad to the pins on the first DIMM connector must be between 1.0” and 2.0” shorter then the SCK/SCK#[2:0] differential clock signals. The data strobe lengths, SDQS[8:0], going from the MCH pad to the pins on the second DIMM connector must be between 1.0” and 2.0” shorter then the SCK/SCK#[5:3] differential clock signals.

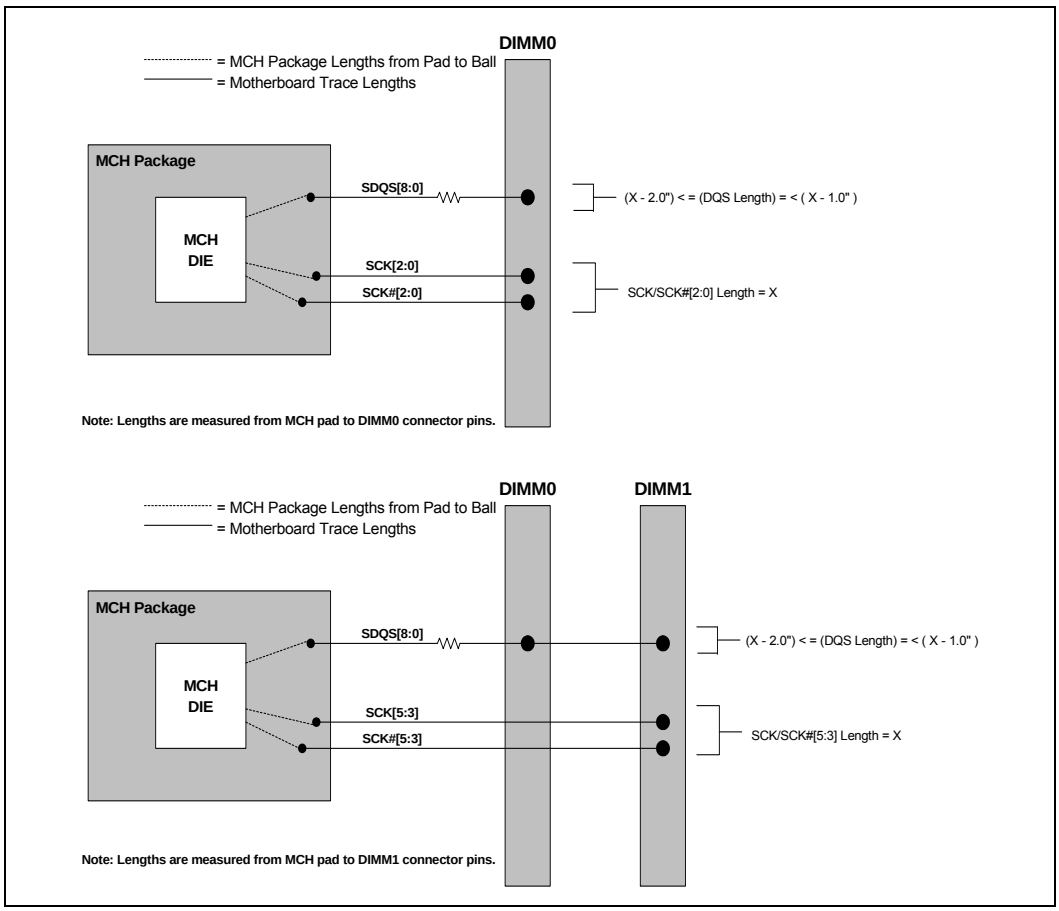
SCK/SCK# Length = X

SDQS Length = Y, where ( X – 2.0” ) ≤ Y ≤ ( X – 1.0” )

***Note:*** - 1st DIMM length X and Y include: MCH Package Length + Motherboard Length A + Motherboard Length B
- 2nd DIMM length X includes: MCH Package Length + Motherboard Length A + Motherboard Length B
- 2nd DIMM length Y includes: MCH Package Length + Motherboard Length A + Motherboard Length B + Motherboard Length C
- SDQS[8:0] Motherboard lengths A, B, and C are documented in Table 5-3.
- SCK/SCK#[5:0] Motherboard lengths A and B are documented in Table 5-9.
- Refer to section 5.6 for MCH strobe and clock package length data.

The diagram below depicts the length matching requirements between the DQS and clock signals.

**Figure 5-6. SDQS to SCK/SCK# Trace Length Matching Requirements**



## 5.3.2 Control Signals – SCKE[3:0], SCS#[3:0]

The MCH control signals are source clocked signals which are "clocked" into the DIMMs using the clock signals, SCK/SCK#[5:0]. The MCH drives the control and clock signals together, with the clocks centered in the valid control window. The MCH provides one chip select and one clock enable control signal per DDR-SDRAM Physical DIMM device Row. Two chip selects and two clock enables will be routed to each DIMM (one for each side). Table 5-5 summarizes the control signal mapping.

**Table 5-5. Control Signal DIMM Mapping**

| Signal | Relative To | DIMM Pin |
|---|---|---|
| SCS#[0] | DIMM0 | 157 |
| SCS#[1] | DIMM0 | 158 |
| SCS#[2] | DIMM1 | 157 |
| SCS#[3] | DIMM1 | 158 |
| SCKE[0] | DIMM0 | 21 |
| SCKE[1] | DIMM0 | 111 |
| SCKE[2] | DIMM1 | 21 |
| SCKE[3] | DIMM1 | 111 |

The MCH system memory pin out has been optimized to breakout the control signals onto the bottom signal layer. The control signals must transition from the top signal layer to the bottom signal layer under the MCH. They should route on the bottom signal layer until they transition to the top signal layer, within 500 mils before the first DIMM connector, and then continue on the top signal layer to its specified DIMM pin. Finally, the control signals should then route from the DIMM connector pins to the parallel termination resistors at the end of the memory channel on the top signal layer referenced to ground.

***Note:*** In order to ease routing in congested areas on the top signal layer (specifically from 500mils before the first DIMM connector to the end of the channel) the following additional guidelines can be applied for the DDR control signals:

- The control signals may route for short distances on the bottom signal layer ground referenced to layer three.
- These backside control trace segments must be kept to no more then two additional segments per control signal and they must be as short as possible.
- Special attention must be paid to how these backside signals affect the 2.5 V copper flooding to any 2.5 V DIMM pin.
- Figure 5-11 below gives an example of some control signal trace segments between the first DIMM and the end of the channel.

Since the control signals are routed on the bottom signal layer this reduces the 2.5 V copper flooding on the bottom signal layer. This copper flooding is used for the 2.5 V power delivery to the MCH system memory interface and for the DDR-DIMMs. For 2.5 V power delivery guidelines please reference Section 5.5.1 In order to maximize this flooding, for better 2.5 V

power delivery to the MCH and the DIMMs, the control signals should be kept as short as possible.

Also since the control signals transition signal layers near the first DIMM, a via connecting the ground flood and ground plane on layer two and three should be placed as close as possible to each control signal transition via. This will ensure that the control signals return currents can transition layers appropriately.

Resistor packs are acceptable for the parallel (Rt) control termination resistors but control signals can NOT be placed within the same RPACK's as data, strobe, or command signals.

The diagrams and tables below depict the recommended topology and layout routing guidelines for the DDR-SDRAM control signals going to the first and second DIMM.

**Figure 5-7. DIMM0 Control Signal Routing Topology (SCS#[1:0], SCKE[1:0])**

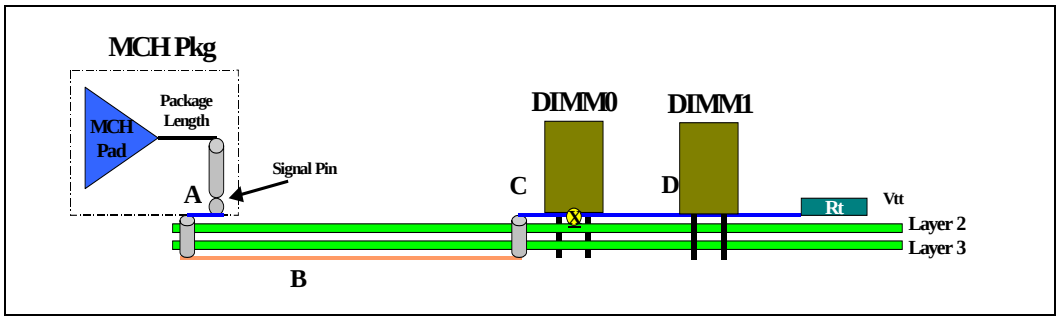



**Figure 5-8. DIMM1 Control Signal Routing Topology (SCS#[3:2], SCKE[3:2])**

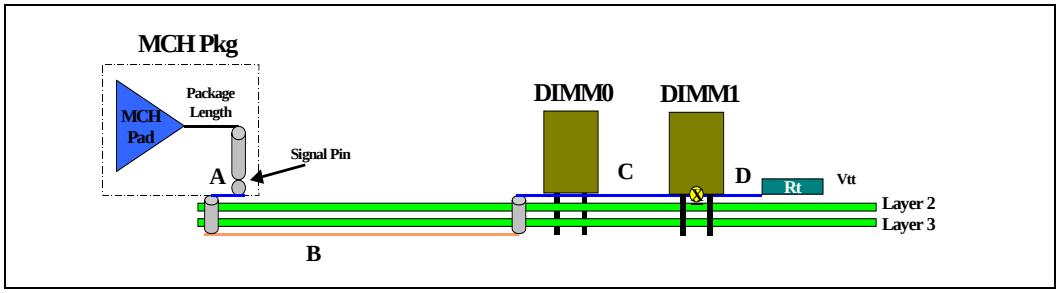
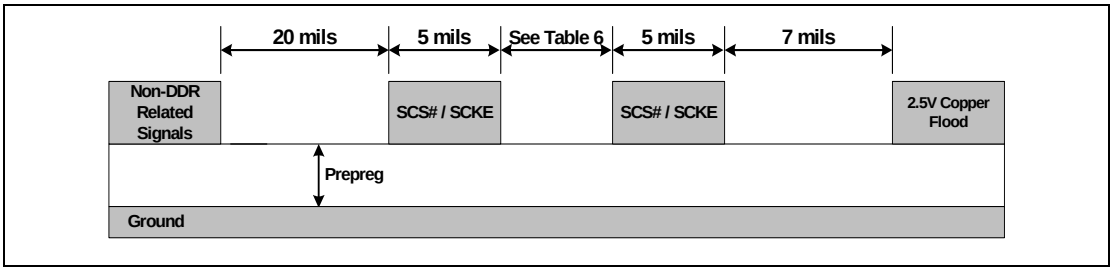



**Table 5-6. Control Signal Group Routing Guidelines**

| Parameter | Routing Guidelines | Figure |
|---|---|---|
| Signal Group | Control – SCS#[3:0], SCKE[3:0] | |
| Topology | Point to Point | 5-7, 5-8 |
| Reference Plane | Ground Referenced | 5-7, 5-8 |
| Characteristic Trace Impedance (Zo) | 60Ω +/- 15% | |
| Trace Width | 5 mils | 5-9 |

| Parameter | Routing Guidelines | Figure |
|---|---|---|
| Trace Spacing | • MCH to 1st DIMM = 12 mils<br>• Within DIMM Pin Field = 7 mils minimum<br>• From DIMM to DIMM = 12 mils<br>• 2nd DIMM to Rt = 7 mils minimum | 5-9 |
| Group Spacing | Isolation spacing from non-DDR related signals = 20 mils | 5-9 |
| 2.5 V Copper Flood Spacing | Isolation spacing from the 2.5 V copper flood on layer four = 7 mils minimum | |
| Trace Length A – MCH Signal Pin to MCH Signal Via | Max = 40 mils | 5-7, 5-8 |
| Trace Length B – MCH Signal Via to Layer Transition Via | Min = 2.0”<br>Max = 3.5” | 5-7, 5-8 |
| Trace Length C (SCS#/SCKE[1:0]) – Layer Transition Via to DIMM Pins on 1st DIMM | Max = 500 mils | 5-7 |
| Trace Length C (SCS#/SCKE[3:2]) – Layer Transition Via to DIMM Pins on 2nd DIMM | Max = 1.0” | 5-8 |
| Trace Length D (SCS#/SCKE[1:0]) – DIMM pins on 1st DIMM to Rtt Pad | Min = 400 mils<br>Max = 1.3” | 5-7 |
| Trace Length D (SCS#/SCKE[3:2]) – DIMM pins on 2nd DIMM to Rtt Pad | Min = 100 mils<br>Max = 800 mils | 5-8 |
| Termination Resistor (Rtt) | 47Ω +/- 5% | |
| Maximum via Count per signal | 2 (without Additional Trace Segments)<br>5 (with two Additional Trace Segments) | 5-7, 5-8 |
| Signal Transition Via Distance | 500 mils max from the pins on the first DIMM Connector | 5-7, 5-8 |
| MCH Breakout Guidelines | 5 mil width with 7 mil spacing for a max of 350 mils | |
| Control to SCK Routing Requirements | SCS#/SCKE[3:0] to SCK/SCK#[5:0]<br>See section 5.3.2.2 for details | 5-12 |

**Figure 5-9. Control Signal Trace Width/Spacing Routing**



### 5.3.2.1 Routing Examples – SCS#[3:0], SCKE[3:0]

**Figure 5-10. Control Group Bottom Signal Layer Routing Example to within 500mils of First DIMM**

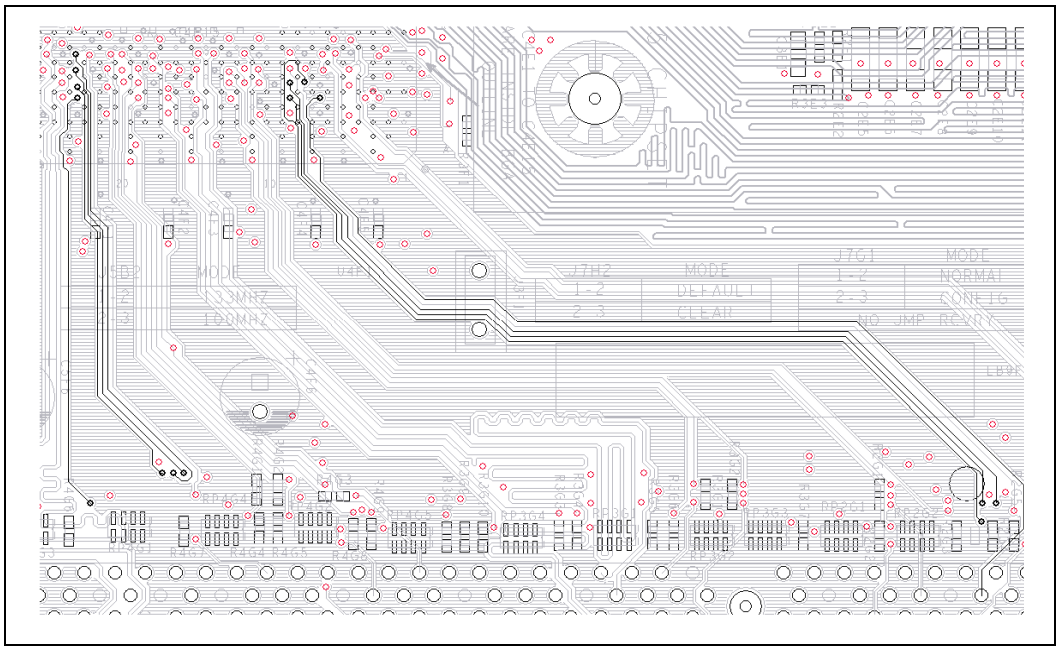
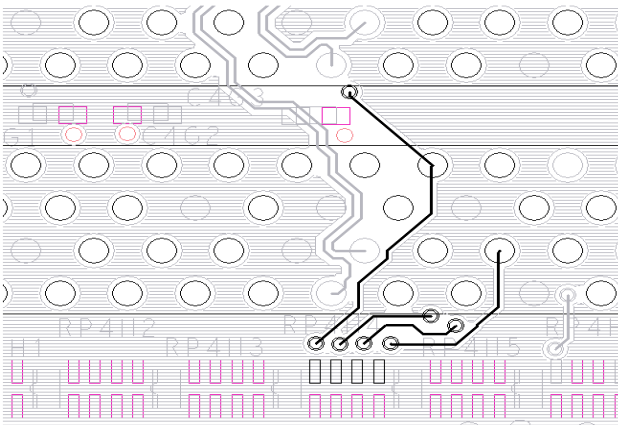


**Figure 5-11. Backside Control Signal Trace Segment Routing Example between the first DIMM and the End of the Channel**



### 5.3.2.2 Control Signal to System Memory Clock Routing Requirements

The control signals, SCS#/SCKE[1:0], going from the MCH pins to the pins on the first DIMM connector must be at least 1.0” shorter then the shortest SCK/SCK#[2:0] differential clock signal motherboard length. The control signals, SCS#/SCKE[3:2], going from the MCH pins to the pins on the second DIMM connector must be at least 1.0” shorter then the shortest SCK/SCK#[5:3] differential clock signal motherboard length.

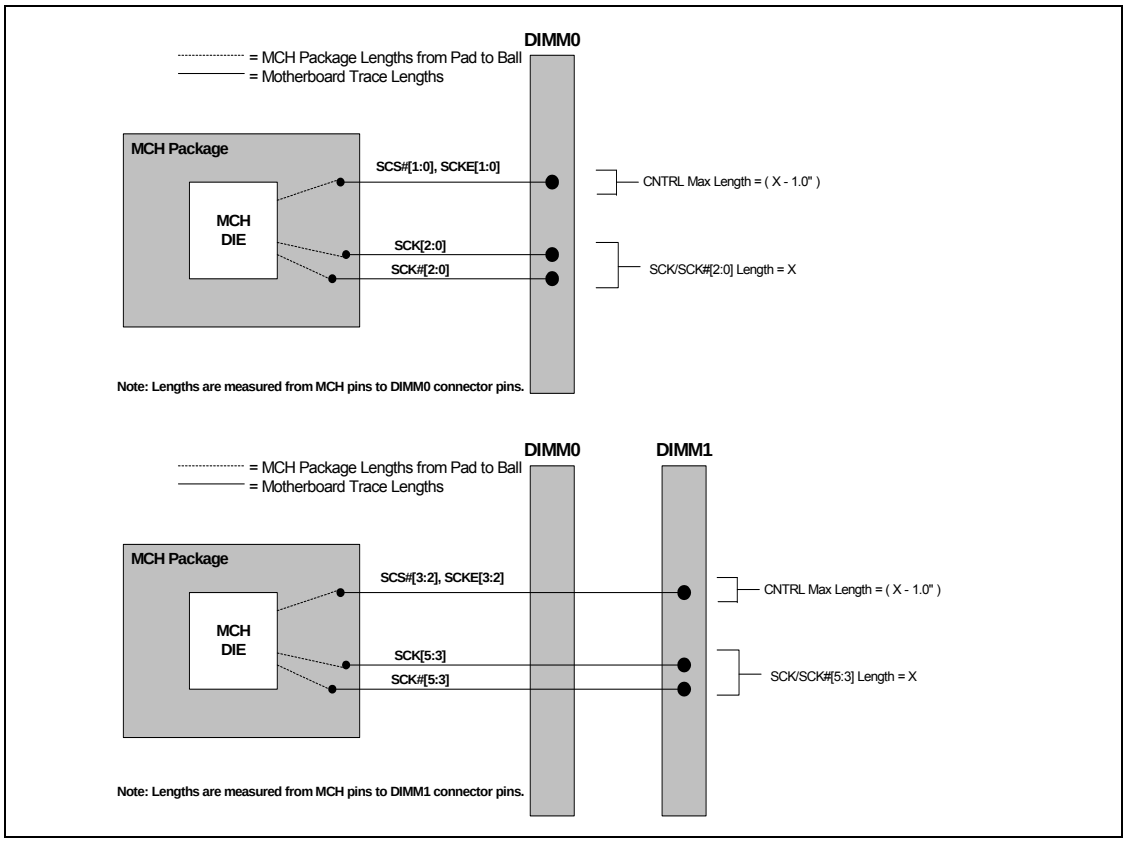
SCK/SCK# Length = X

SCS#/SCKE Max Length = Y, where Y = ( X – 1.0” )

***Note:*** - 1st and 2nd DIMM length X and Y include Motherboard Length only.
- 1st DIMM Length X is the shortest SCK/SCK#[2:0] motherboard length.
- 2nd DIMM Length X is the shortest SCK/SCK#[5:3] motherboard length.
– The MCH control and clock package lengths don’t need to be taken into account.

The diagram below depicts the routing requirements between the control signals and the clock signals.

**Figure 5-12. Control Signal to SCK/SCK# Routing Requirements**




## 5.3.3 Command Signals – SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#

The MCH command signals are source clocked signals that are “clocked” into the DIMMs using the clock signals SCK/SCK#[5:0]. The MCH drives the command and clock signals together with the clocks centered in the valid command window.

The MCH system memory pin out has been optimized to breakout the command signals onto the bottom signal layer. The command signals include SMA[12:0], SBS[1:0], SRAS#, SCAS#, and

SWE#. They must transition from the top signal layer to the bottom signal layer under the MCH. They should route on the bottom signal layer until they transition to the top signal layer, within 500 mils before the first DIMM connector. They should continue on the top signal layer to the pins on the first DIMM, from DIMM pin to DIMM pin, and finally from the pins on the second DIMM to the parallel termination resistors at the end of the memory channel on the top signal layer referenced to ground.

Note: To ease routing in congested areas on the top signal layer (specifically from 500mils before the first DIMM connector to the end of the channel), the following additional guidelines can be applied for the DDR command signals:

- The command signals may route for short distances on the bottom signal layer ground referenced to layer three.
- These backside command trace segments must be kept to no more then two additional segments per command signal, and they must be as short as possible.
- Special attention must be paid to how these backside signals affect the 2.5 V copper flooding to any 2.5 V DIMM pin.
- Figure 5-13 shows an example of some command signal trace segments between the first DIMM and the end of the channel.

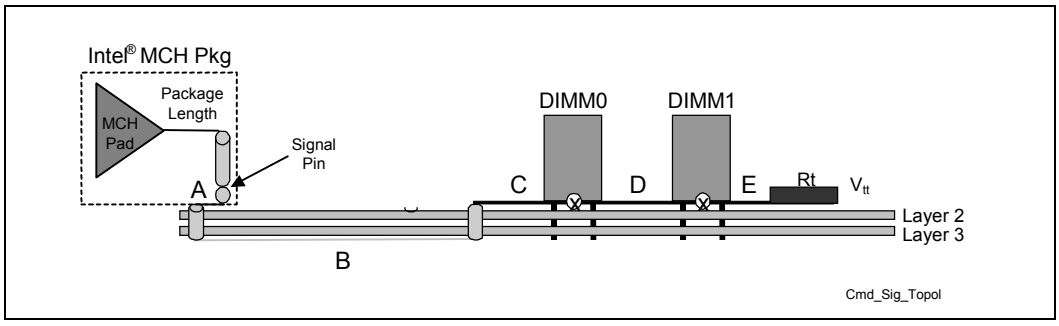
Because the command signals are routed on the bottom signal layer, the 2.5 V copper flooding on the bottom signal layer is reduced. This copper flooding is used for the 2.5 V power delivery to the MCH system memory interface, and for the DDR-DIMMs. For 2.5 V power delivery guidelines, refer to Section 5.5.1. To maximize this flooding, for better 2.5 V power delivery to the MCH and the DIMMs, the command signals should be kept as short as possible.

Because the command signals transition signal layers near the first DIMM, a via connecting the ground flood and ground plane on layer two and three should be placed as close as possible to each command signal transition via. This will ensure that the command signals return currents can transition layers appropriately.

Resistor packs are acceptable for the parallel (Rt) command termination resistors, but command signals can NOT be placed within the same RPACK's as data, strobe, or control signals.

The following figures and table describe the recommended topology and layout routing guidelines for the DDR-SDRAM command signals.

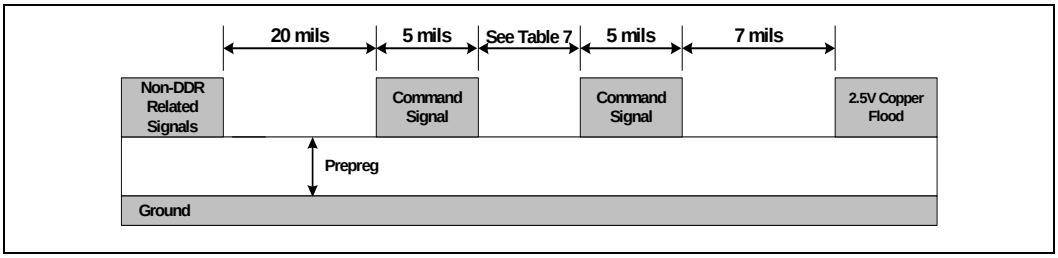
**Figure 5-13. Command Signal Routing Topology**



### Table 5-7. Command Signal Group Routing Guidelines

| Parameter | Routing Guidelines | Figure |
|---|---|---|
| Signal Group | Command – SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE# | |
| Topology | Daisy Chain | 5-13 |
| Reference Plane | Ground Referenced | 5-13 |
| Characteristic Trace Impedance (Zo) | 60Ω +/- 15% | |
| Trace Width | 5 mils | 5-14 |
| Trace Spacing from MCH | • MCH to 1st DIMM = 12 mils<br>• Within DIMM Pin Field = 7 mils minimum<br>• From DIMM to DIMM = 12 mils<br>• 2nd DIMM to Rt = 7 mils minimum | 5-14 |
| Group Spacing | Isolation spacing from non-DDR related signals = 20 mils | 5-14 |
| 2.5 V Copper Flood Spacing | Isolation spacing from the 2.5 V copper flood on layer four = 7 mils minimum | |
| Trace Length A – MCH Signal Pin to MCH Signal Via | Max = 40 mils | 5-13 |
| Trace Length B – MCH Signal Via to Rs Pad | Min = 2.0”<br>Max = 3.5” | 5-13 |
| Trace Length C – Rs Pad to First DIMM Pin | Max = 500mils | 5-13 |
| Trace Length D – DIMM pin to DIMM pin. | Min = 300 mils<br>Max = 500 mils | 5-13 |
| Trace Length E – DIMM pins on second DIMM to Rtt Pad | Min = 100 mils<br>Max = 800 mils | 5-13 |
| Series Resistor (Rs) | 0Ω | |
| Termination Resistor (Rt) | 56Ω +/- 5% | |
| Maximum via Count per signal | 2 (without Additional Trace Segments)<br>5 (with two Additional Trace Segments) | 5-13 |
| Signal Via Distance from Rs Pads | Max = 25 mils | 5-13 |
| MCH Breakout Guidelines | 5 mil width with 7 mil spacing for a max of 350 mils | |
| CMD to SCK Routing Requirements | CMD to SCK/SCK#[5:0]<br>See section 5.3.3.2 for details | 5-17 |

**Figure 5-14. Command Signal Trace Width/Spacing Routing**




### 5.3.3.1 Routing Examples – SMA[12:0], SBS[1:0], SCAS#, SRAS#, SWE#

**Figure 5-15. Command Group Bottom Signal Layer Routing Example to within 500mils of First DIMM**

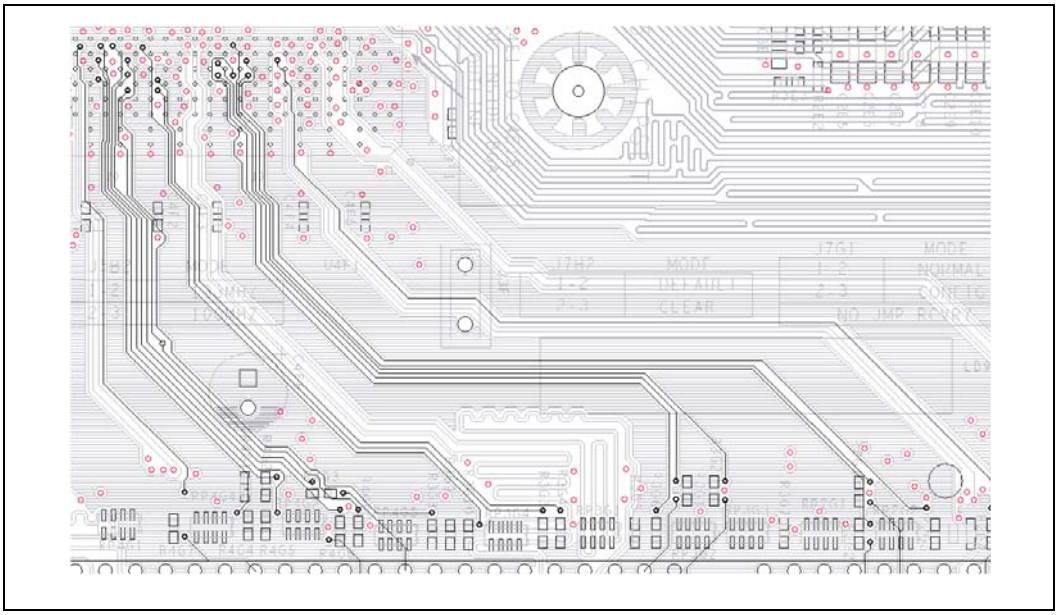
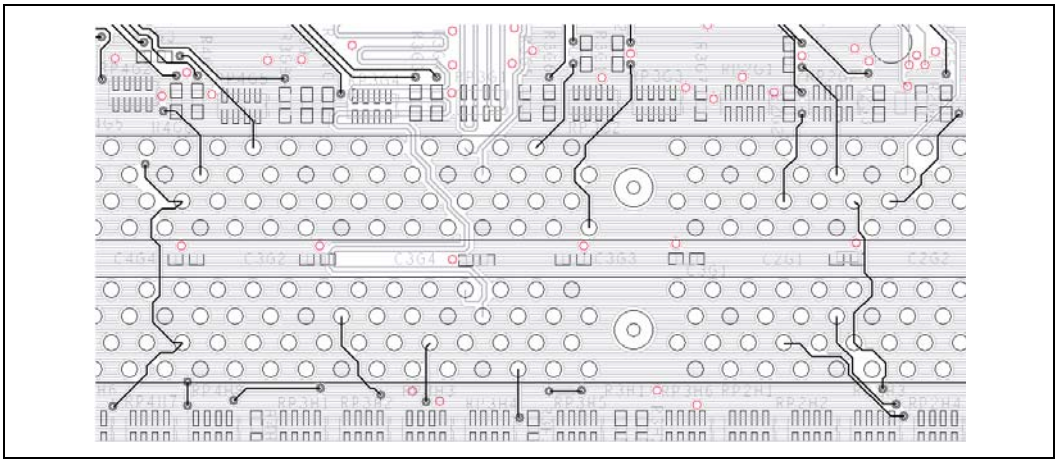


**Figure 5-16. Backside Command Trace Segment Routing Example between the Series Resistors and the End of the Channel**



### 5.3.3.2 Command Group Signal to System Memory Clock Routing Requirements

The command signals, SMA[12:0], SBS[1:0], RAS#, CAS#, and WE#, going from the MCH pins to the pins on the first DIMM connector must be at least 1.0” shorter than the shortest SCK/SCK#[2:0] differential clock signal motherboard length. The command signals, SMA[12:0], SBS[1:0], RAS#, CAS#, and WE#, going from the MCH pins to the pins on the second DIMM must be at least 1.0” shorter than the shortest SCK/SCK#[5:3] differential clock signal motherboard length.

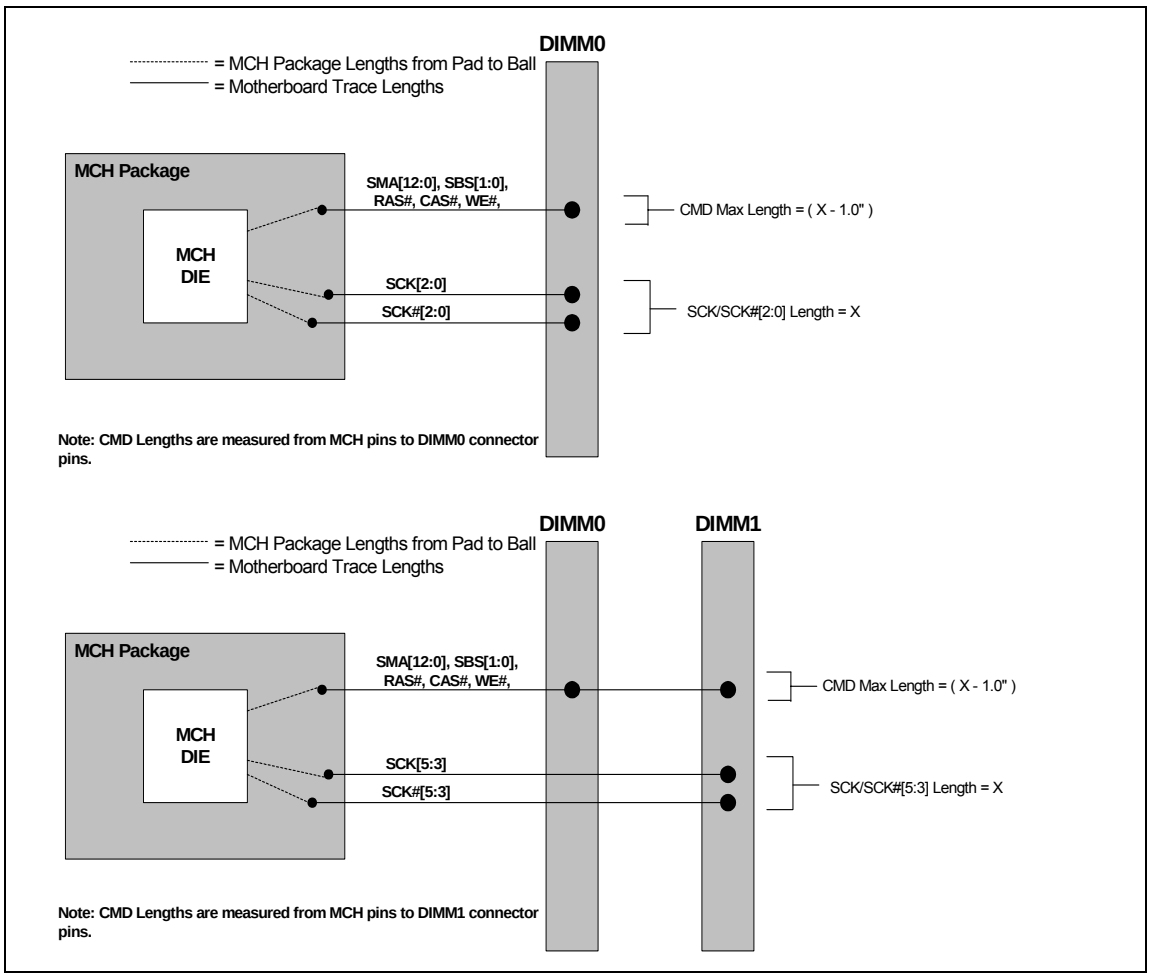
SCK/SCK# Length = X

CMD Signal Max Length = Y, where Y = ( X – 1.0” )

***Note:*** - 1st and 2nd DIMM length X and Y include Motherboard Length only.
- 1st DIMM Length X is the shortest SCK/SCK#[2:0] motherboard length.
- 2nd DIMM Length X is the shortest SCK/SCK#[5:3] motherboard length.
– The MCH command and clock package lengths don’t need to be taken into account.

The diagram below depicts the routing requirements between the command signals and the clock signals.

**Figure 5-17. Command Signal to SCK/SCK# Routing Requirements**




## 5.3.4 Clock Signals – SCK[5:0], SCK#[5:0]

The clock signal group includes the differential clock pairs SCK[5:0] and SCK#[5:0]. The MCH generates and drives these differential clock signals required by the DDR interface; therefore, no external clock driver is required for the DDR interface. Since the MCH only supports unbuffered DDR DIMMs, three differential clock pairs are routed to each DIMM connector. Table 5-8 summarizes the clock signal mapping.

**Table 5-8. Clock Signal Mapping**

| Signal | Relative To |
|---|---|
| SCK[2:0], SCK#[2:0] | DIMM0 |
| SCK[5:3], SCK#[5:3] | DIMM1 |

The MCH system memory pin out has been optimized to breakout the clock signals onto the bottom signal layer. The clock signals **must** transition from the top signal layer to the bottom signal layer under the MCH and route referenced to ground, on the bottom signal layer, for the entire length to their associated DIMM pins. The clock signal pairs must be routed differentially from the MCH to their associated DIMM pins, they must maintain the correct isolation spacing from other signals, and when they serpentine together they MUST maintain a minimum of 20 mil spacing.

Since the clock signals are routed on the bottom signal layer this reduces the 2.5 V copper flooding on the bottom signal layer. This copper flooding is used for the 2.5 V power delivery to the MCH system memory interface and for the DDR-DIMMs. For 2.5 V power delivery guidelines please reference section 5.5.1. Special attention must be paid to how these backside clock signals affect the 2.5 V copper flooding to any 2.5 V DIMM pin. Figure 5-21 and Figure 5-22 below show examples of the clock routing on the bottom signal layer.

The diagrams and table below depict the recommended topology and layout routing guidelines for the DDR-SDRAM differential clocks.

**Figure 5-18. DDR Clock Routing Topology (SCK/SCK#[2:0])**

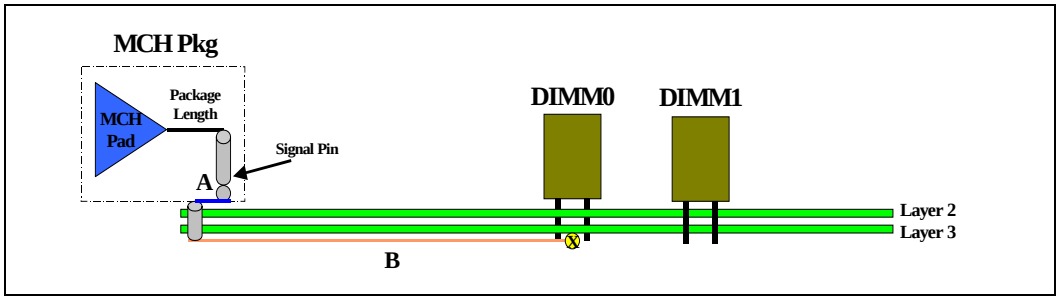
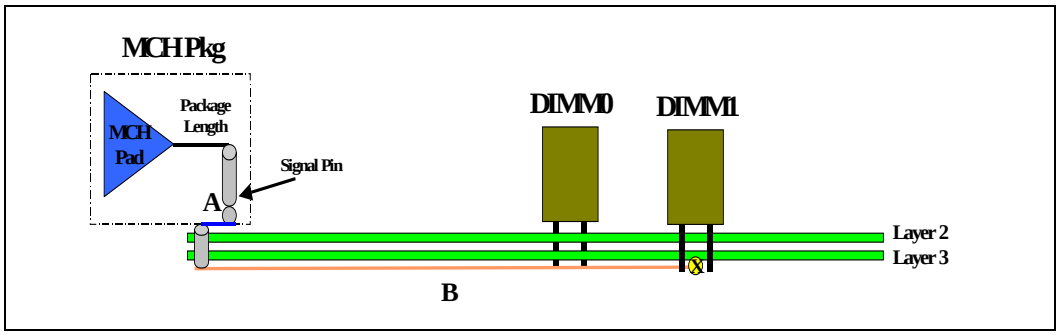


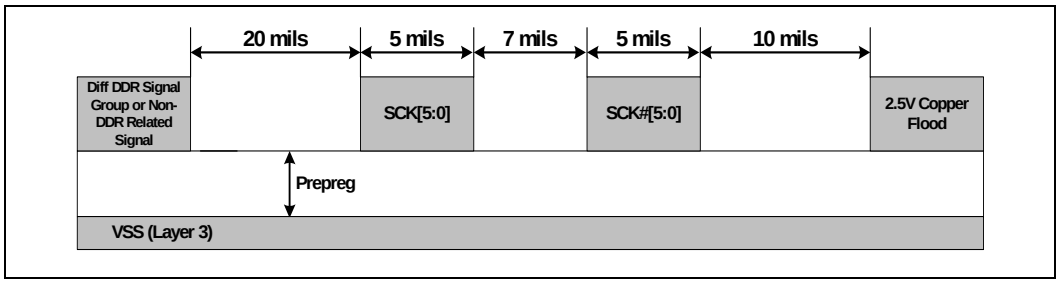

**Figure 5-19. DDR Clock Routing Topology (SCK/SCK#[5:3])**



### Table 5-9. Clock Signal Group Routing Guidelines

| Parameter | Routing Guidelines | Figure |
|---|---|---|
| Signal Group | Clock – SCK[5:0], SCK#[5:0] | |
| Topology | Point to Point | 5-18, 5-19 |
| Reference Plane | Ground Referenced | 5-18, 5-19 |
| Characteristic Trace Impedance (Zo) | Single Ended =60Ω +/- 15%<br>Differential = 120Ω +/- 15% | |
| Trace Width | 5 mils | 5-20 |
| Differential Trace Spacing | 7 mils | 5-20 |
| Group Spacing | Isolation spacing from another DDR signal group = 20 mils<br>Isolation spacing from non-DDR related signals = 20 mils | 5-20 |
| Serpentine Spacing | 20 mils minimum | |
| 2.5 V Copper Flood Spacing | Isolation spacing from the 2.5 V copper flood on layer four = 10 mils minimum | |
| Trace Length A – MCH Signal Pin to MCH Signal Via | Max = 40 mils | 5-18, 5-19 |
| Trace Length B (SCK/SCK[2:0]) – MCH Signal Via to Associated DIMM Pins | Min = 2.0”<br>Max = 6.5” | 5-18 |
| Trace Length B (SCK/SCK[5:3]) – MCH Signal Via to Associated DIMM Pins | Min = 2.5”<br>Max = 7.0” | 5-19 |
| Maximum via Count per signal | 1 | 5-18, 5-19 |
| MCH Breakout Guidelines | 5 mil width with 7 mil differential spacing with a minimum of 7 mil isolation spacing from another signal for a max of 350 mils | |
| Length Matching Requirements | SCK = SCK#<br>All DIMM0 Clock Pairs are equal in length, and all DIMM1 Clock Pairs are equal in length.<br>See section 5.3.4.2 for details | 5-23, 5-24 |

### Figure 5-20. Clock Signal Trace Width/Spacing Routing



### 5.3.4.1 Routing Examples – SCK[5:0], SCK#[5:0]

**Figure 5-21. DDR Clock Bottom Signal Layer Routing Example #1**

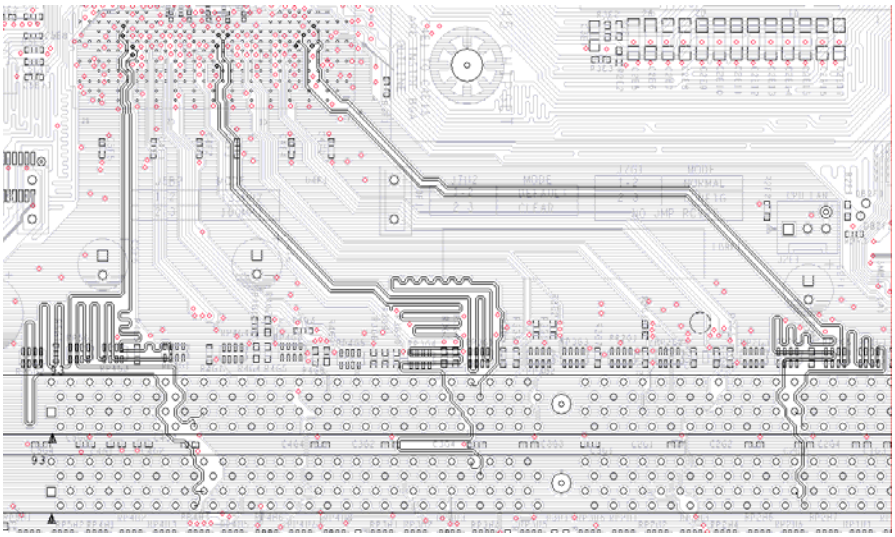
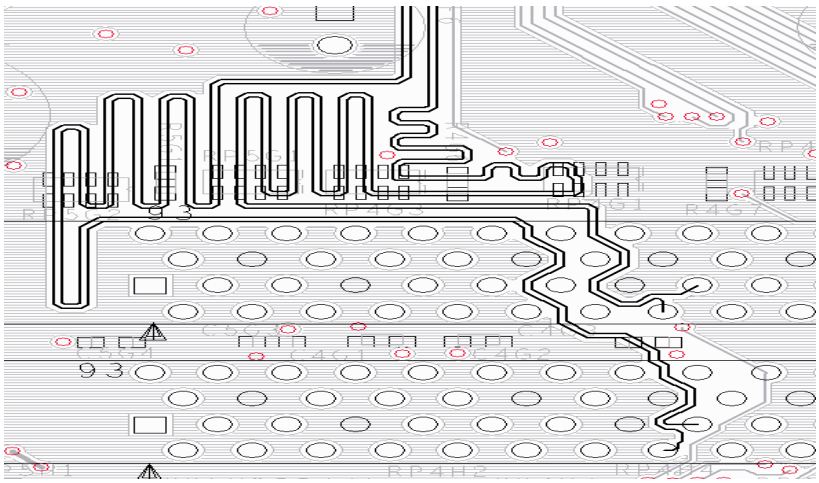


**Figure 5-22. DDR Clock Bottom Signal Layer Routing Example #2**



### 5.3.4.2 Clock Group Signal Length Matching Requirements

The MCH provides three differential clock pair signals for each DIMM. A differential clock pair is made up of a SCK signal and its complement signal SCK#. SCK and its complement SCK# within every differential clock pair requires exact length matching from the MCH pad to the DIMM pins.

SCK[0] = SCK#[0]
SCK[1] = SCK#[1]
SCK[2] = SCK#[2]
SCK[3] = SCK#[3]

SCK[4] = SCK#[4]
SCK[5] = SCK#[5]

***Note:*** The SCK and SCK# lengths include the compensated MCH Package Length + the Motherboard Trace Length. Refer to section 5.6 for the MCH clock package length data.

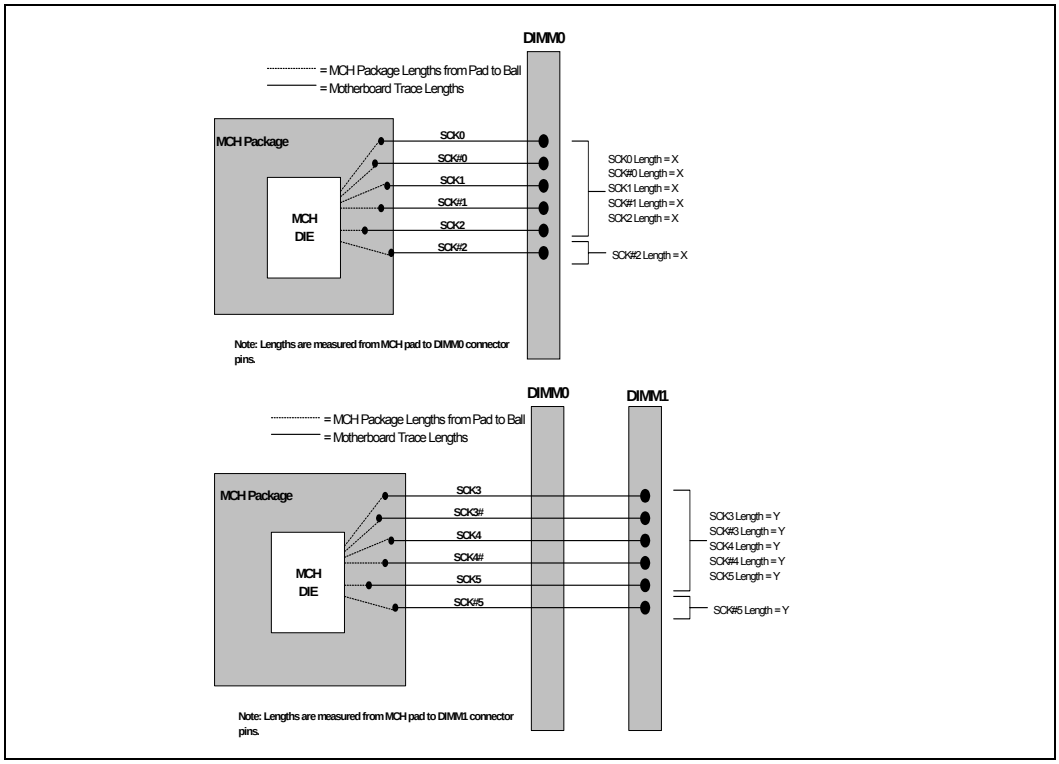
Clock length matching is also required between clock pairs to their specified DIMM. The differential clock pairs for the first DIMM connector, SCK/SCK#[2:0] require exact matching of the trace lengths from MCH pad to the pins of the first DIMM connector. The differential clock pairs for the second DIMM connector, SCK/SCK#[5:3] require exact matching of the trace lengths from MCH pad to the pins of the second DIMM connector.

SCK/SCK#[0] = SCK/SCK#[1] = SCK/SCK#[2]
SCK/SCK#[3] = SCK/SCK#[4] = SCK/SCK#[5]

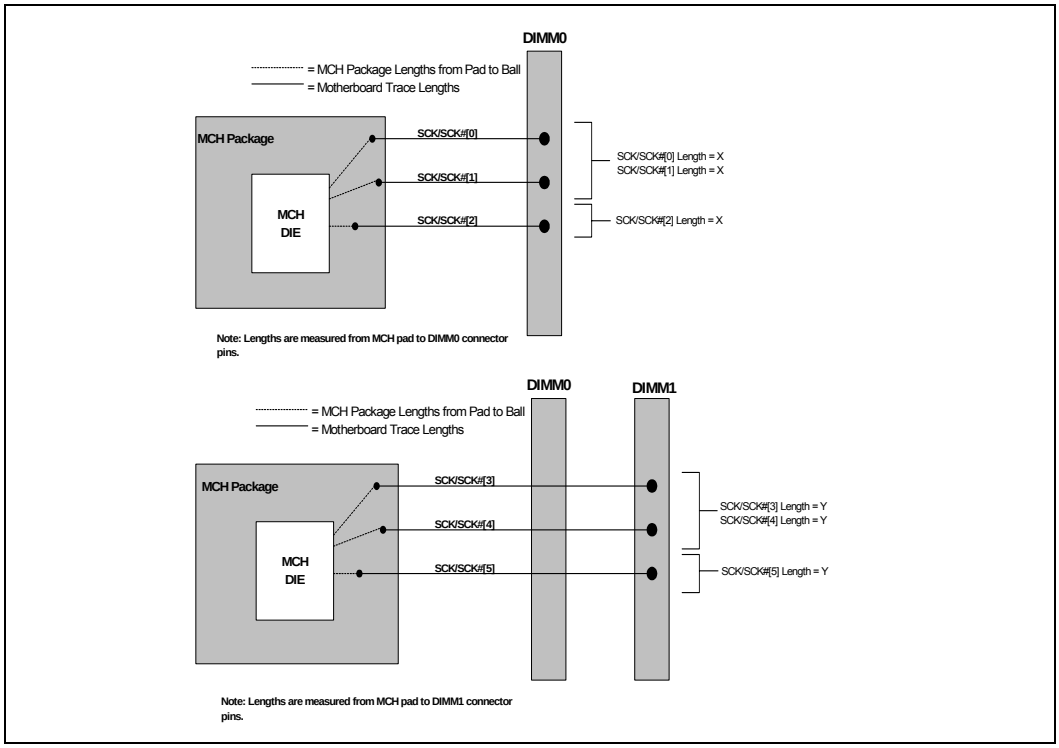
***Note:*** The SCK and SCK# lengths include the compensated MCH Package Length + the Motherboard Trace Length. Refer to section 5.6 for the MCH clock package length data.

Keep in mind that the differential clocks must be 1.0” to 2.0” longer then the strobe signals, and at least 1.0” longer then the control and command signals without exceeding its maximum motherboard trace lengths. For information covering the data strobe to clock length matching requirements reference section 5.3.1.2.2, for information covering the control signal to clock routing requirements reference section 5.3.2.2, and for information covering the command signal to clock routing requirements reference section 5.3.3.2. The diagrams below depict the clock length matching requirements.

## Figure 5-23. SCK to SCK# Trace Length Matching Requirements




## Figure 5-24. Clock Pair Trace Length Matching Requirements



## 5.3.5 Feedback – RCVENOUT#, RCVENIN#

The MCH provides a feedback signal called "receive enable" (RCVEN#) which is used by the MCH to determine the approximate roundtrip flight time (command flight + Read data flight) to and from the DIMMs. There are two pins on the MCH to facilitate the use of RCVEN#. The RCVENOUT# pin is an output of the MCH and the RCVENIN# pin is an input to the MCH. The board designer must connect RCVENOUT# to RCVENIN#.

The RCVEN# signal must be routed on the same layer as the system memory clocks. It should transition from the top signal layer to the bottom signal layer under the MCH, routed referenced to ground for the entire length, and then transition from the bottom signal layer back to the top signal layer under the MCH.

The diagrams and table below depicts the recommended topology and layout routing guidelines for the DDR-SDRAM feedback signal.

**Figure 5-25. DDR Feedback (RCVEN#) Routing Topology**

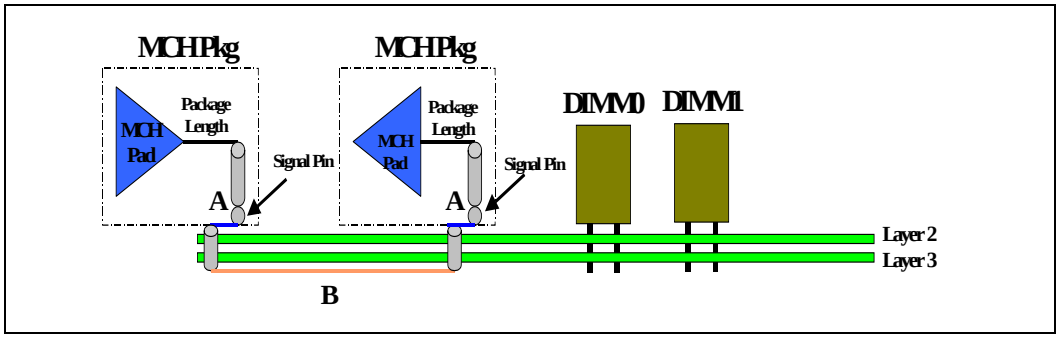
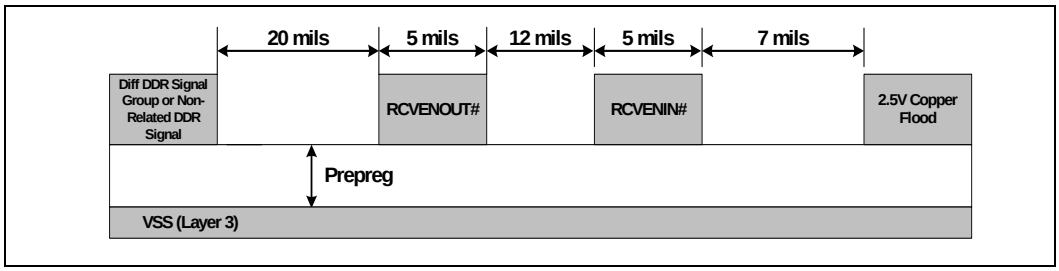



**Table 5-10. DDR-SDRAM Feedback Signal Routing**

| Parameter | Routing Guidelines | Figure |
|---|---|---|
| Signal Group | Feedback – RCVENOUT# and RCVENIN# | |
| Topology | Point to Point | 5-25 |
| Reference Plane | Ground Referenced | 5-25 |
| Characteristic Trace Impedance (Zo) | 60Ω +/- 15% | |
| Trace Width | 5 mils | 5-26 |
| Trace Spacing | 12 mils | 5-26 |
| Group Spacing | Isolation spacing from another DDR signal group = 10 mils<br>Isolation spacing from non-DDR related signals = 10 mils | 5-26 |
| 2.5 V Copper Flood Spacing | Isolation spacing from the 2.5 V copper flood on layer four = 7 mils minimum | |

| Parameter | Routing Guidelines | Figure |
|---|---|---|
| Trace Length A – MCH Signal Ball to MCH Signal Via | Max = 40 mils | 5-25 |
| Trace Length B – MCH RCVEN# Output Signal Via to RCVEN# Input Signal Via | Must equal 1.0” | 5-25 |
| Maximum via Count per signal | 2 | 5-25 |
| Breakout Guidelines | 5 mil width with 7 mil spacing for a max of 350 mils | |
| Length Matching Requirements | None | |

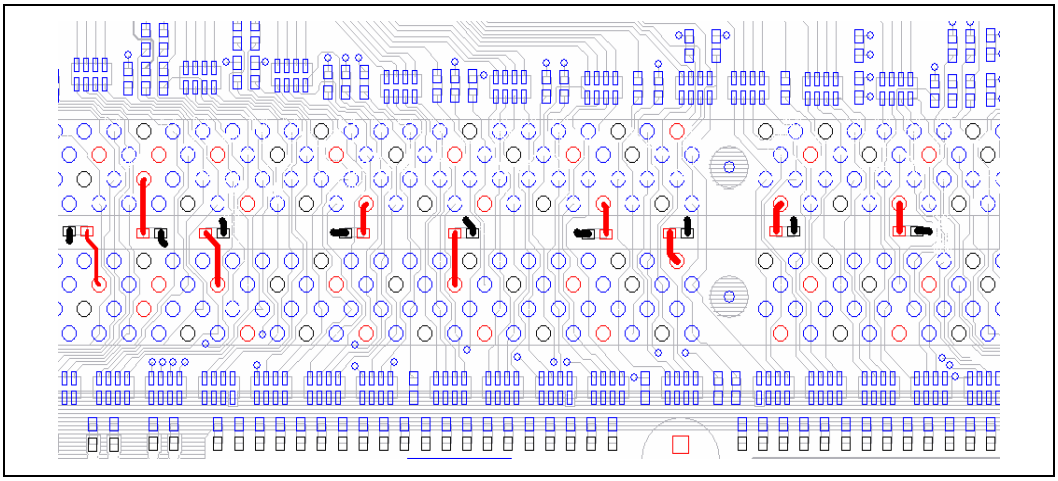
**Figure 5-26. Feedback (RCVEN#) Signal Trace Width/Spacing Routing**




## 5.4 System Memory Bypass Capacitor Guidelines

Discontinuities in the DDR signal return paths will occur when the signals transition between the motherboard and the DIMMs. To account for this ground to 2.5 V discontinuity, a minimum of nine 0603 0.1 µF high-frequency bypass capacitors are required between the DIMMs to help minimize any anticipated return path discontinuities that will be created. The bypass capacitors should connect to 2.5 V and ground. The ground trace should connect to a via that transitions to the ground flood on layer two and to the ground plane on layer three. The ground via should be placed as close to the ground pad as possible. The 2.5 V trace should connect to a via that transitions to the 2.5 V copper flood on layer four, and it should connect to the closet 2.5 V DIMM pin on either the first or second DIMM connector, with a wide trace. The capacitors 2.5 V traces should be distributed as evenly as possible amongst the two DIMMs. Finally, the 2.5 V via should be placed as close to the 2.5 V pad as possible.

**Figure 5-27. DDR-DIMM Bypass Capacitor Placement**



## 5.5 Power Delivery

The following guidelines are recommended for a 845E chipset DDR system memory design. The main focus of these MCH guidelines is to minimize signal integrity problems and improve the power delivery of the MCH system memory interface and the DDR-DIMMs.

### 5.5.1 2.5 V Power Delivery Guidelines

The 2.5 V power for the MCH system memory interface and the DDR-DIMMs is delivered on layer four around the DDR command, control, and clock signals. Special attention must be paid to the 2.5 V copper flooding on layer four to ensure proper MCH and DIMM power delivery. This 2.5 V flood must extend from the MCH 2.5 V power vias all the way to the 2.5 V DDR voltage regulator and its bulk capacitors, located at the end of the DDR channel on layer one, beyond the second DIMM connector. The 2.5 V DDR voltage regulator must connect to the 2.5 V flood with a minimum of six vias, and the DIMM connector 2.5 V pins as well as the MCH 2.5 V power vias must connect to the 2.5 V copper flood on layer four.

The copper flooding to the MCH should include at least seven fingers to allow for the routing of the DDR signals and for optimal MCH power delivery. The copper fingers must be kept as wide as possible in order to keep the loop inductance path from the 2.5 V voltage regulator to the MCH at a minimum. In the areas where the copper flooding necks down under the MCH make sure to keep these neck down lengths as short and wide as possible. Table 5-11 below details the minimum width requirements for the copper fingers going from the MCH system memory high-frequency capacitors to the MCH package edge (approximately 150mils). It also details the minimum neck down width requirements that the copper fingers can be reduced to for short distances from the MCH package edge through the MCH pin field. **These neck down lengths must be kept as short as possible.** The width requirements listed below must be met at a minimum for the copper fingers in order to supply good 2.5 V power delivery to the MCH. The following table references Figure 5-29, which has a total of eight copper fingers for MCH 2.5 V power deliver (at least seven are required). The copper finger numbering starts from the far left and moves to the right.

### Table 5-11. Minimum 2.5 V Copper Finger Width Requirements

| Cu Finger | Min Width (From Caps to Pkg Edge) | Min Neck Down Widths (within MCH Pin Field) |
|---|---|---|
| Number 1 (Left most finger) | 215 mils | 170 mils |
| Number 2 | 36 mils | 32 mils |
| Number 3 | 36 mils | 22 mils |
| Number 4 | 105 mils | 30 mils |
| Number 5 | 85 mils | 24 mils |
| Number 6 | 52 mils | 40 mils |
| Number 7 | 140 mils | 32 mils |
| Number 8 (Right most finger) | 80 mils | 45 mils |

The 2.5 V copper flooding under the DIMM connectors must encompass all the DIMM 2.5 V pins. Figure 5-28 and Figure 5-30 show examples of the layer four 2.5 V power delivery to the DIMMs.

A small 2.5 V cooper flood shape should be placed on layer two under the MCH to increase the copper area to the back row 2.5 V MCH pins. This flood must not be placed under any of the DDR data, strobe, clock, or receive enable signals. The number of DDR command and control signals that are placed over this small layer two 2.5 V shape must be kept to a minimum, and for no longer then 40mils.

Since the DDR command, control, and clock signals are routed on the bottom signal layer, between the MCH and the first DIMM, this limits the 2.5 V copper flooding. In order to maximize the copper flooding these signals should be kept as short as possible in order to reduce the amount of serpentining needed in this area on the bottom layer.

Finally, the six MCH 2.5 V high-frequency decoupling capacitors, located on the top signal layer, should have their 2.5 V via placed directly over and connected to a separate 2.5 V copper finger. For guidelines on the MCH 2.5 V high-frequency decoupling capacitors please reference section 5.5.2.1.

The figures below show examples of the 2.5 V power delivery copper flood for the MCH and the DIMMs.

**Figure 5-28. Layer Four 2.5 V Power Delivery**

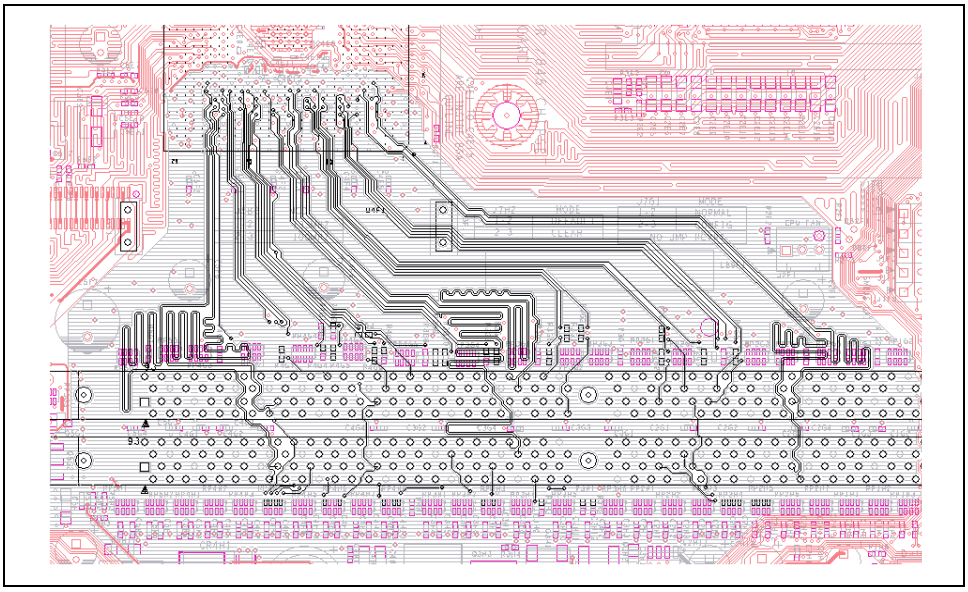


**Figure 5-29. Layer Four 2.5 V MCH Power Delivery**

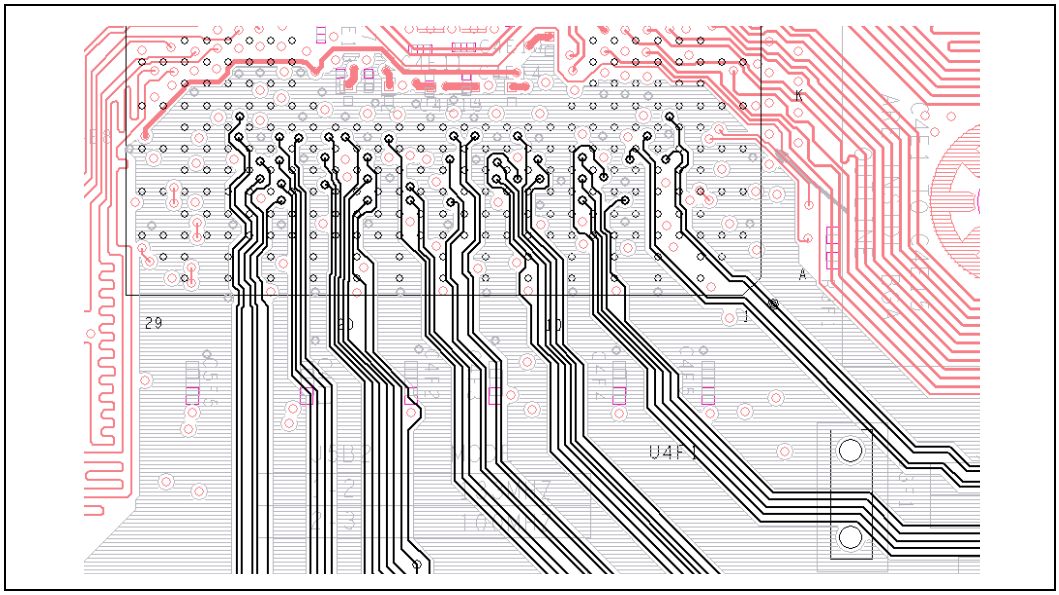


**Figure 5-30. Layer Four 2.5 V DIMM Power Delivery**

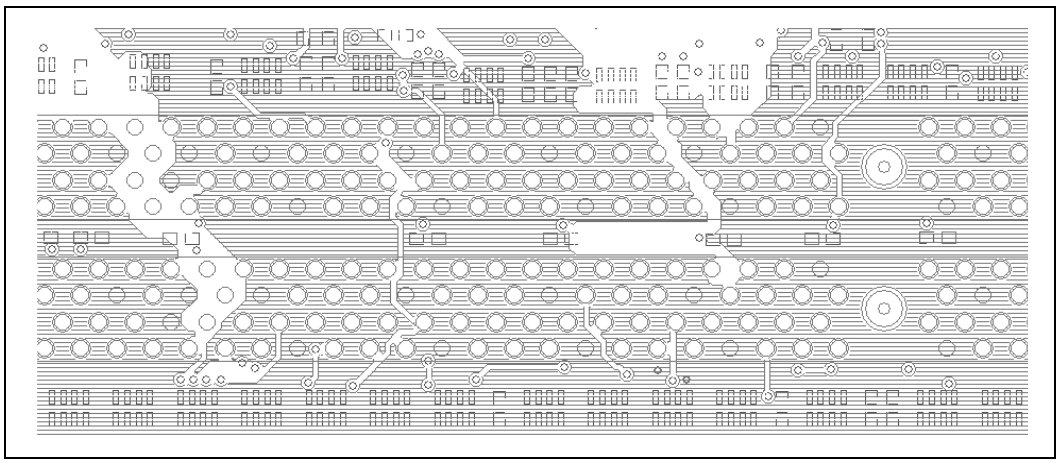
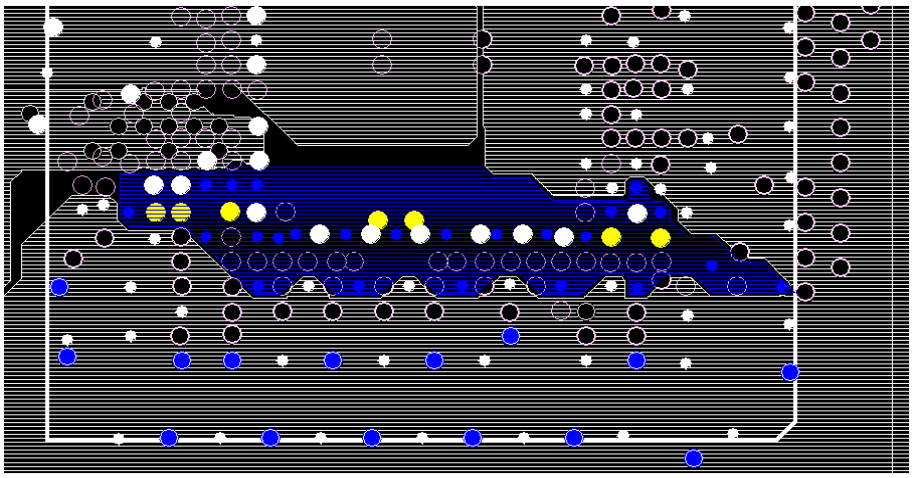


**Figure 5-31. Layer Two 2.5 V Power Delivery Picture**



## 5.5.2 MCH System Memory Interface Decoupling Requirements

### 5.5.2.1 MCH System Memory High-Frequency Decoupling

Every MCH ground and power ball in the system memory interface should have its own via. For 2.5 V high-frequency decoupling, a minimum of six 0603 0.1 µF high-frequency capacitors is required, and must be within 150mils of the MCH package. The six capacitors should be evenly distributed along the MCH DDR system memory interface and must be placed perpendicular to the MCH with the power (2.5 V) side of the capacitors facing the MCH. The trace from the power end of the capacitor should be as wide as possible and it must connect to a 2.5 V power ball on the outer row of balls on the MCH. Each capacitor should have their 2.5 V via placed directly over and connected to a separate 2.5 V copper finger located on layer four, and they should be as close to the capacitor pad as possible, within 25mils. The ground end of the capacitors must connect to the ground flood on layer two and to the ground plane on layer three through a via. This via should be as close to the capacitor pad as possible, within 25mils with as

thick a trace as possible. The following figures represent the MCH DDR 2.5 V high-frequency decoupling requirements.

**Figure 5-32. MCH DDR 2.5 V Decoupling Picture**

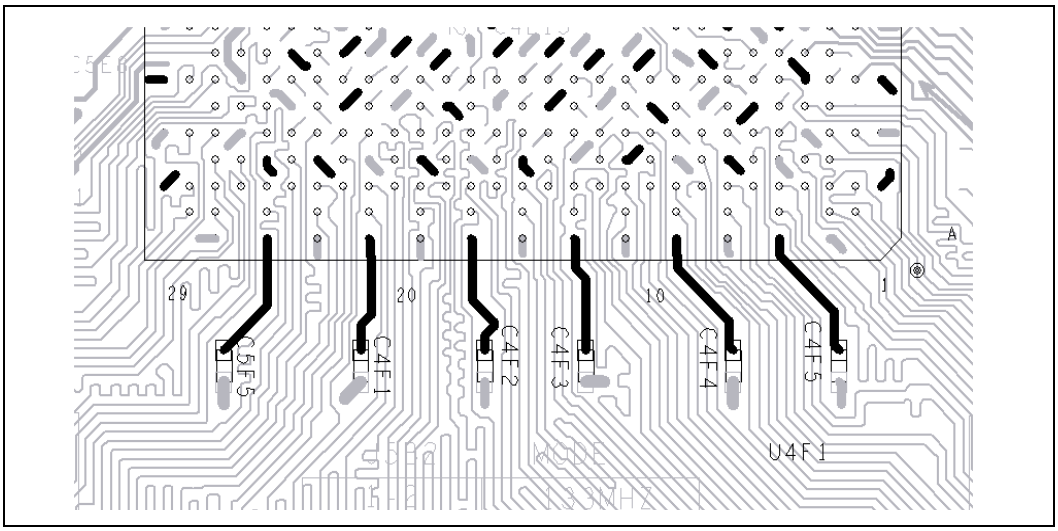
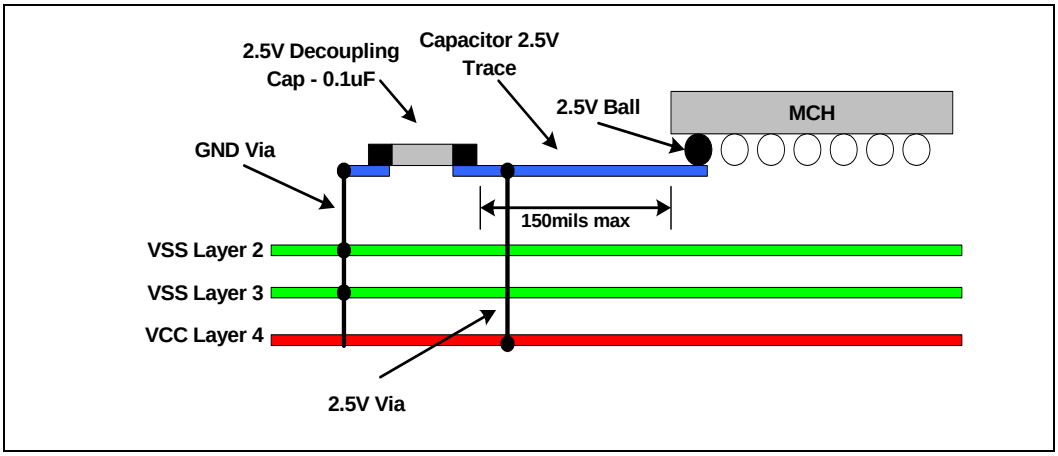


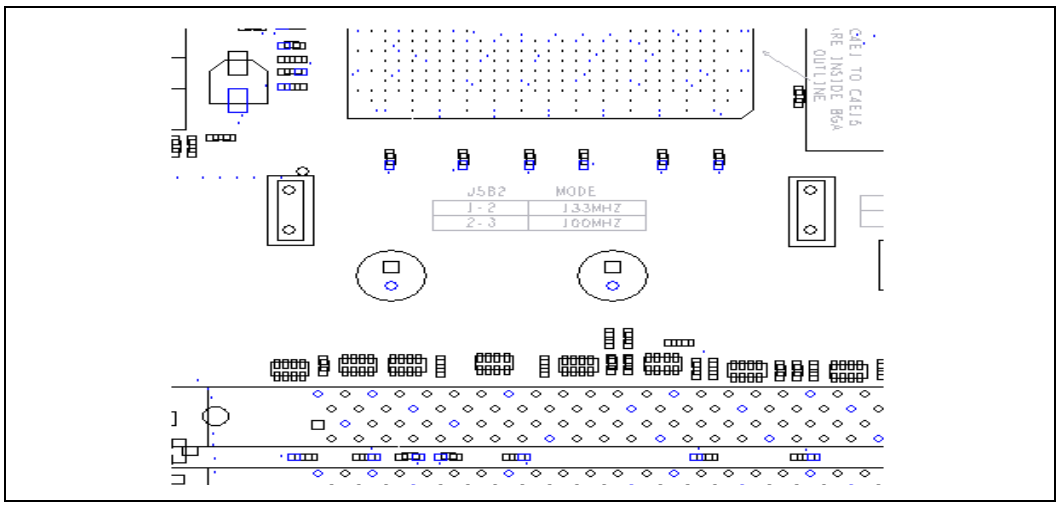

**Figure 5-33. MCH DDR 2.5 V Decoupling Capacitor Routing Alignment**




## 5.5.2.2 MCH System Memory Low-Frequency Bulk Decoupling

The MCH system memory interface requires low-frequency bulk decoupling. Place two 100 µF electrolytic capacitors between the MCH and the first DIMM connector. The power end of the capacitors must connect to 2.5 V on layer four, and the ground end of the capacitors must connect to ground on layer two and three. Also, the output of the 2.5 V regulator must have enough bulk decoupling to ensure the stability of this regulator. The amount of bulk decoupling required at the output of the 2.5 V regulator will vary according to the needs of different OEM design targets.

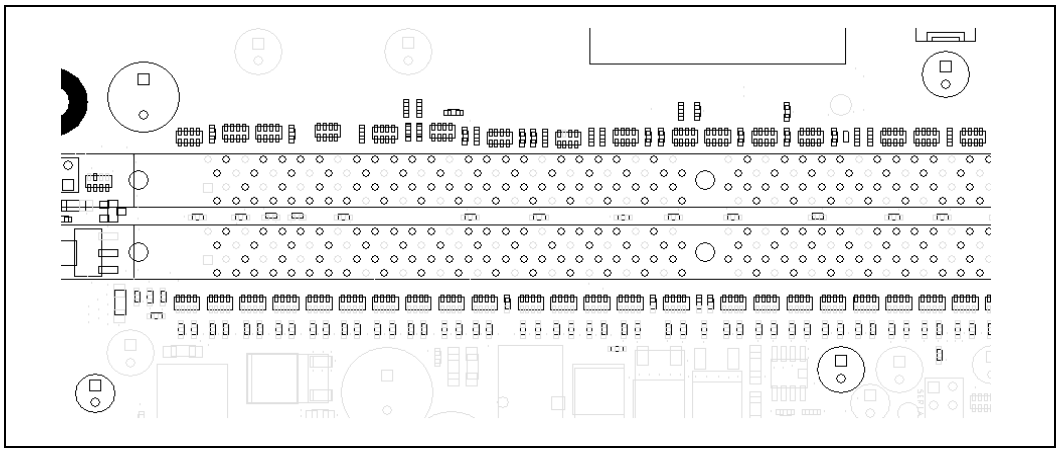
Figure 5-34. MCH 2.5 V Bulk Decoupling Example




## 5.5.3 DDR-DIMM Decoupling Requirements

The DDR-DIMMs require low-frequency bulk decoupling. Place a total of four 100 µF capacitors, one at each corner of each DIMM connector. The power end of the capacitors must connect to 2.5 V on layer four, and the ground end of the capacitors must connect to ground on layer two and three. The output of the 2.5 V regulator must have enough bulk decoupling to ensure the stability of the regulator. The amount of bulk decoupling required at the output of the 2.5 V regulator will vary according to the needs of different OEM design targets.

Figure 5-35. DDR-DIMM 2.5 V Bulk Decoupling Example

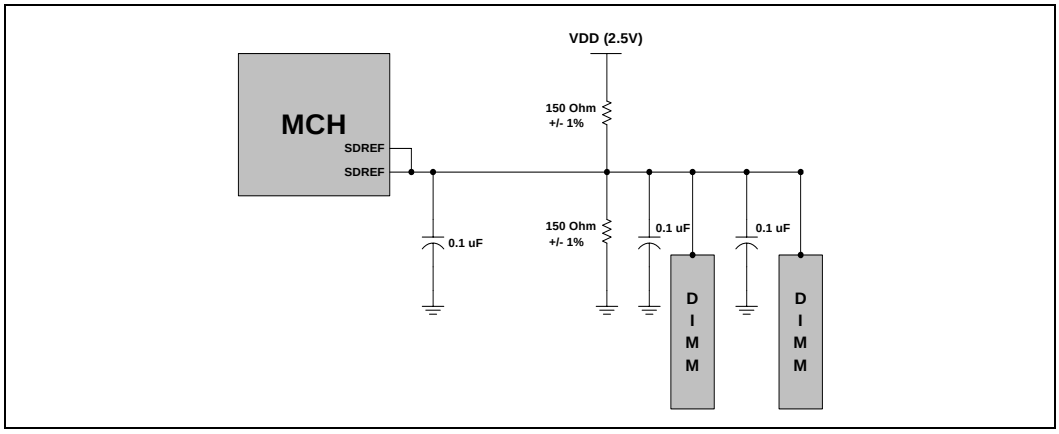


## 5.5.4 DDR Reference Voltage

The DDR system memory reference voltage (VREF) is used by the DDR-SDRAM devices to compare the input signal levels of the data, command, and control signals, and is also used by the MCH to compare the input data signal levels. VREF must be generated as shown in Figure 5-36. It should be generated from a typical resistor divider using 1%-tolerance resistors. The VREF

resistor divider should be placed no further then 1.0” from the DIMMs. Additionally, VREF must be decoupled locally at each DIMM connector, at the resistor divider, and at the MCH. Finally, the VREF signal should be routed with as wide a trace as possible, minimum of 12 mils wide and isolated from other signals with a minimum of 12mil spacing (min of 7 mil spacing for a max of 350mils within the breakout area of the MCH).

**Figure 5-36. DDR VREF Generation Example Circuit**



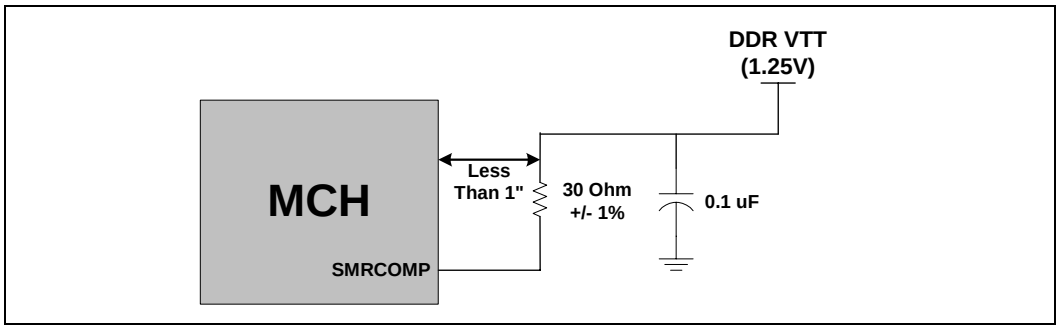

## 5.5.5 DDR SMRCOMP Resistive Compensation

The MCH uses a compensation signal to adjust the system memory buffer characteristics over temperature, process, and voltage variations. The DDR system memory (SMRCOMP) must be connected to the DDR termination voltage (1.25 V) through a 30 Ω ±1% resistor and one 0603 0.1 µF decoupling capacitor to ground as illustrated in Figure 5-37.

The 0.1 µF decoupling capacitor must go from Vtt ( DDR termination voltage) to ground and must be placed on the Vtt side of the SMRCOMP resistor and not the MCH side.

Place the resistor as close to the MCH as possible, within 1.0” of the MCH package. The compensation signal and the VTT trace should be routed with as wide a trace as possible, minimum of 12 mils wide and isolated from other signals with a minimum of 10mil spacing.

**Figure 5-37. DDR SMRCOMP Resistive Compensation**

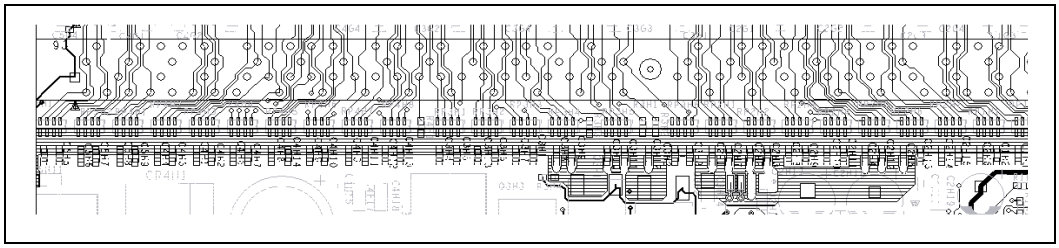


## 5.5.6 DDR VTT Termination

All DDR signals, except the command clocks, must be terminated to 1.25 V (VTT) using 5% resistors at the end of the channel opposite the MCH. Place a solid 1.25 V (VTT) termination island on the top signal layer, just beyond the last DIMM connector, as shown in Figure 5-38 and Figure 5-39 . The VTT Termination Island must be at least 50mils wide. Use this termination island to terminate all DDR signals, using one resistor per signal. Resistor packs are acceptable, with the understanding that the signals within an RPACK are from the same DDR signal group. No mixing of signals from different DDR signal groups is allowed within an RPACK. The parallel termination resistors connect directly to the VTT Island on the top signal layer.

### 5.5.6.1 Routing Example – DDR Vtt Termination Island

**Figure 5-38. DDR Vtt Termination Island Example**



### 5.5.6.2 VTT Termination Island High-Frequency Decoupling Requirements

The VTT Island must be decoupled using high-speed bypass capacitors, one 0603 0.1 µF capacitor per two DDR signals. These decoupling capacitors connect directly to the VTT Island and to ground, and must be spread-out across the Termination Island so that all the parallel termination resistors are near high-frequency capacitors. The capacitor ground via should be as close to the capacitor pad as possible, within 25mils with as thick a trace as possible. The ground end of the capacitors must connect to the ground flood on layer two and to the ground plane on layer three through a via. The distance from any DDR termination resistor pin to a 0.1 µF VTT capacitor pin must not exceed more then 100 mils.

Finally, place one 4.7 µF ceramic capacitor on each end of the termination island, and also place one 4.7 µF ceramic capacitor near the center of the termination island. The power end of these capacitors must connect to the Vtt termination island directly, and the ground end of the capacitors must connect to ground on layer two and three.

**Figure 5-39. DDR VTT Termination 0.1 µF High-Frequency Capacitor Example #1**

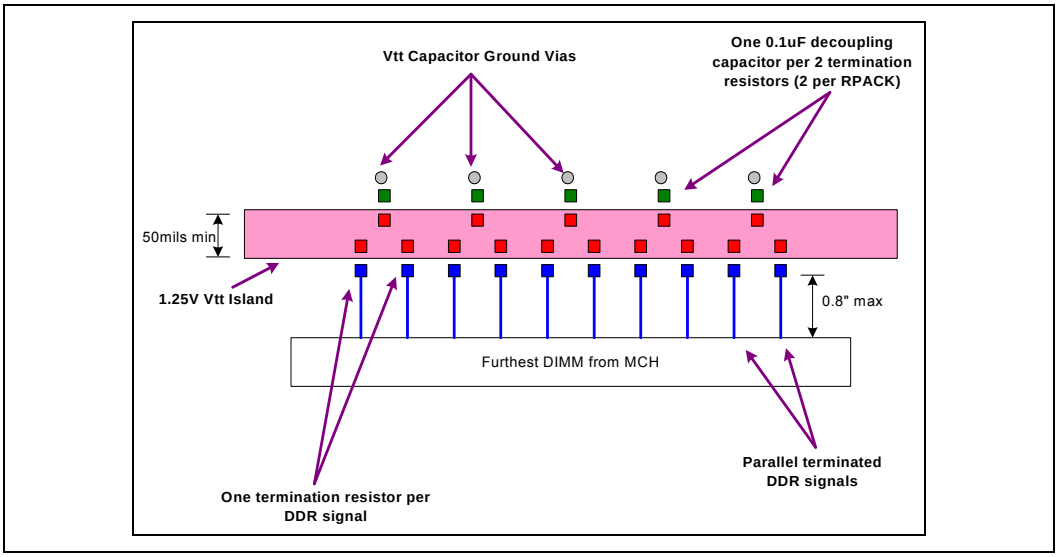



**Figure 5-40. DDR VTT Termination 0.1 µF High-Frequency Capacitor Example #2**

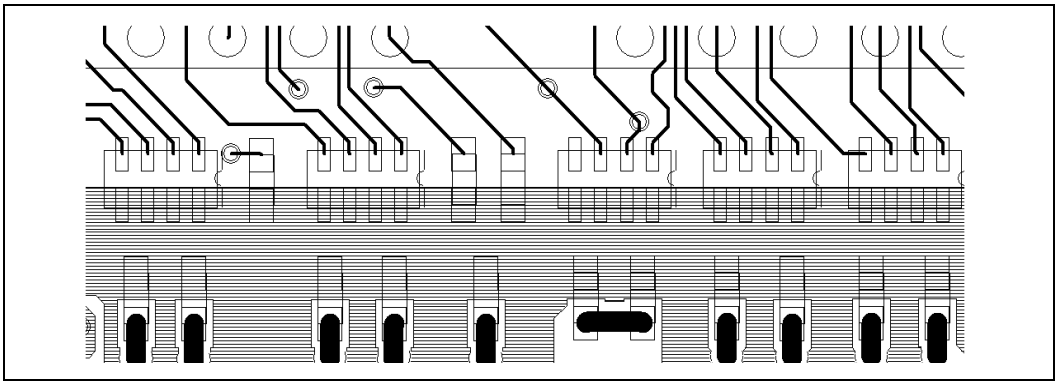
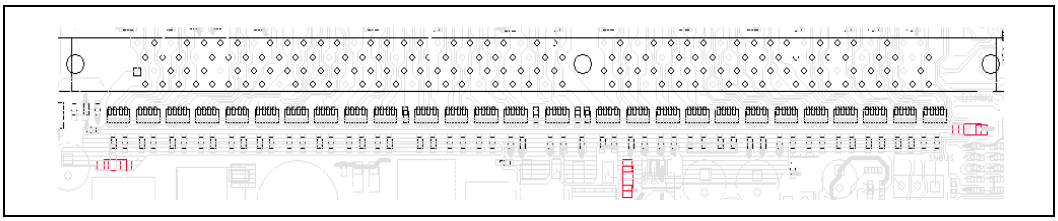


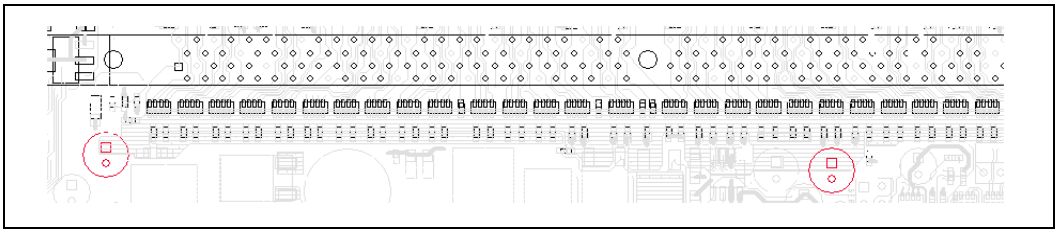
**Figure 5-41. DDR VTT Termination 4.7 µF High-Frequency Capacitor Example**



### 5.5.6.3 VTT Termination Island Low-Frequency Bulk Decoupling Requirements

The VTT Termination Island requires low-frequency bulk decoupling. Place one 220 µF electrolytic capacitor at each end of the termination island. The power end of the capacitors must connect to the Vtt termination island directly, and the ground end of the capacitors must connect to ground on layer two and three. Also, the output of the 1.25 V regulator must have enough bulk decoupling to ensure the stability of the regulator. The amount of bulk decoupling required at the output of the 1.25 V regulator will vary according to the needs of different OEM design targets.

**Figure 5-42. DDR VTT Termination Low-Frequency Capacitor Example**



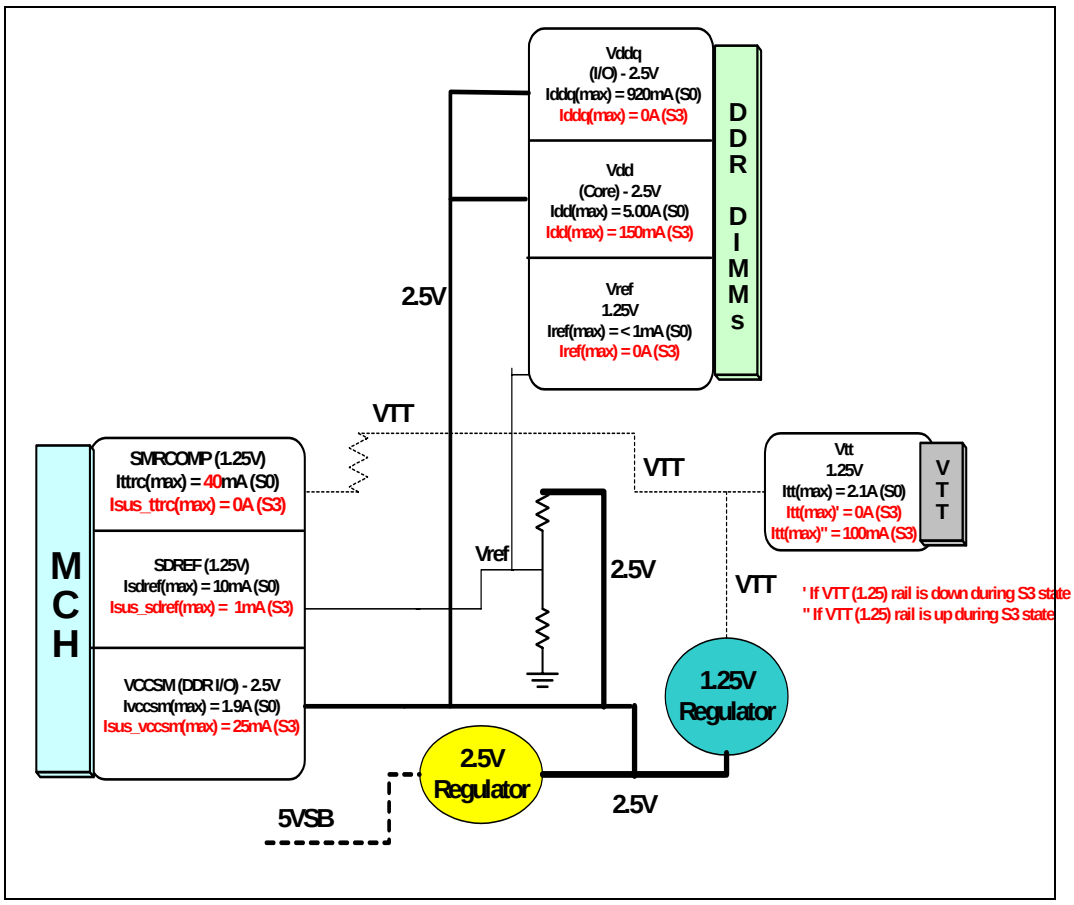
## 5.5.7 DDR Voltage Regulator Guidelines

Intel 845E chipset designs using the DDR-SDRAM memory sub system require several different voltages, Vdd, Vddq, Vtt, and Vref. In order to generate these voltages, a 2.5 V and 1.25 V regulator is required, and must be designed to supply the required voltage and current levels to meet both the MCH and DDR-SDRAM device requirements. The following sections define the range of DC and AC operating Voltage and Current conditions the 2.5 V and 1.25 V voltage regulators should meet for a two DIMM DDR-SDRAM based system with the 845E chipset. It does not attempt to define a specific voltage regulator implementation. DDR voltage regulation will be governed by either an on-motherboard regulator circuitry or a module with the necessary complement of external capacitance, and will vary according to the needs of different OEM design targets.

### 5.5.7.1 Intel® 845E Chipset DDR Reference Board Power Delivery

Figure 5-43 shows the power delivery architecture for the 845E chipset DDR memory subsystem. This power delivery example provides support for the suspend-to-RAM (STR) and the full Power-on State.

**Figure 5-43. Intel® 845E Chipset DDR Power Delivery Example**




### 5.5.7.2 DDR 2.5 V Power Plane

The 2.5 V power plane, which is generated by the 2.5 V regulator, is used to supply power to the MCH 2.5 V I/O Ring, the DDR-SDRAM 2.5 V Core, and the DDR-SDRAM 2.5 V I/O Ring. The 2.5 V regulator should be placed at the end of the DDR channel near the Vtt Termination Island.

### 5.5.7.3 DDR 1.25 V Power Plane

The 1.25 V power plane, which is generated by the 1.25 V regulator, is used to supply the DDR termination voltage (Vtt) and the MCH SMRCOMP pull-up voltage (Vtt). Special considerations need to be taken for the 1.25 V regulator design since it must be able to source and sink a significant amount of current. The 1.25 V regulator should be placed at the end of the DDR channel near the Vtt Termination Island.

### 5.5.7.4 DDR Reference Voltage (Vref)

The MCH and DDR-DIMM reference voltage (Vref) is generated from a typical resistor divider circuit off of the 2.5 V power plane. For guidelines on the Vref resistor divider please reference section 5.5.4

### 5.5.7.5 DC and AC Electrical Characteristics (DIMM Supply Rails)

The DDR 2.5 V voltage regulator supplies the required voltages – Vdd, Vddq, and Vref – and current for up to two DDR-DIMMs as shown in the following tables. The following DRAM Device specifications were determined at the DIMM connectors.

#### 5.5.7.5.1 DDR-SDRAM DIMM Core and I/O Voltage (Vdd, VddQ)

The following conditions apply to the specifications listed below:

- IDD and IDDQ are measured at maximum VDD/VDDQ and under maximum signal loading conditions.
- Note that these worst case values are for reference only, and are based on current and future expected DRAM vendor specific specifications for maximum current.
- The worst-case Idd current draw was determined with the following criteria:
  - Both DIMM slots are populated with double-sided ECC x8 device DDR-DIMMs
  - Continuous back to back burst reads, with a burst length of 4, to one single bank in the same physical DIMM device Row.
  - All other banks are in the active standby state where a row in each bank is activated/open.

**Table 5-12. DDR-SDRAM DIMM Core and I/O Voltage and Current Requirements (at the DIMM Connectors)**

| Parameter | Symbol | Unit | Minimum | Nominal | Maximum |
|---|---|---|---|---|---|
| Core Supply Voltage, Static | Vdd | Volts, V | 2.3 | 2.5 | 2.7 |
| I/O Supply Voltage, Static | VddQ | Volts, V | 2.3 | 2.5 | 2.7 |
| Core Supply Current, Static | Idd | Amperes, A | | | 5.0<br>0.150 (Standby) |
| I/O Supply Current, Static | IddQ | Amperes, A | | | 0.920<br>0 (Standby) |

#### 5.5.7.5.2 DDR-SDRAM DIMM Reference Voltage (Vref)

The following conditions apply to the specifications listed below:

- IREF is measured at maximum VREf under maximum signal loading conditions.

**Table 5-13. DDR-SDRAM DIMM Reference Voltage and Current Requirements (at the DIMM Connectors)**

| Parameter | Symbol | Unit | Minimum | Nominal | Maximum |
|---|---|---|---|---|---|
| I/O Reference Supply Voltage, Static | Vref | Volts, V | Vdd/2 – 0.05 | Vdd/2 | Vdd/2 + 0.05 |
| I/O Reference Supply Current, Static | Iref | Amperes, A | | | < 0.001<br>0 (Standby) |

### 5.5.7.6 DC and AC Electrical Characteristics (MCH Supply Rails)

The 2.5 V DDR voltage regulator supplies the required MCH voltages, VCCSM and SDREF, and current as shown in the following tables. The following MCH specifications were determined at the MCH supply pins.

#### 5.5.7.6.1 MCH DDR Supply Voltage (VCCSM)

The following conditions apply to the specifications:

- Ivccsm is measured at maximum VCCSM under maximum signal loading conditions.

***Note:*** Note that these values are for reference only. Please refer to the latest revision on the *Intel® 845E Chipset MCH Addendum for DDR Memory*.

**Table 5-14. MCH DDR Supply Voltage and Current Requirements (at the MCH)**

| Parameter | Symbol | Unit | Minimum | Nominal | Maximum |
|---|---|---|---|---|---|
| MCH DDR Supply Voltage, Static | VCCSM | Volts, V | 2.375 | 2.5 | 2.625 |
| MCH DDR Supply Current, Static | Ivccsm | Amperes, A | | | 1.9<br>0.025 (Standby) |

#### 5.5.7.6.2 MCH Reference Voltage (Vref)

The following conditions apply to the specifications:

- Isdref is measured at maximum Vsdref under maximum signal loading conditions.

***Note:*** Note that these values are for reference only. Please refer to the latest revision on the *Intel® 845E Chipset MCH Addendum for DDR Memory.*

**Table 5-15. MCH DDR Reference Voltage and Current Requirements (at the MCH)**

| Parameter | Symbol | Unit | Minimum | Nominal | Maximum |
|---|---|---|---|---|---|
| MCH Reference Supply Voltage, Static | SDREF | Volts, V | 0.48 x VCCSM | 0.5 x VCCSM | 0.52 x VCCSM |
| MCH Reference Supply Current, Static | Isdref | Amperes, A | | | 0.010<br>0.001 (Standby) |

### 5.5.7.7 DC and AC Electrical Characteristics (Vtt Supply Rail)

The 1.25 V DDR voltage regulator supplies the required DDR Termination Voltage (Vtt) and current (Itt), and supplies the MCH system memory resistive compensation pull-up voltage (Vtt), and current (IttRC) as shown in the following tables.

#### 5.5.7.7.1 DDR Termination Voltage (Vtt)

The following conditions apply to the specifications:

- ITT is measured at maximum VTT under maximum signal loading conditions by looking at all the DDR signals, excluding the command clocks, with their specified series and parallel termination resistors.

**Table 5-16. DDR Termination Voltage and Current Requirements**

| Parameter | Symbol | Unit | Minimum | Nominal | Maximum |
|---|---|---|---|---|---|
| Termination Supply Voltage, Static | Vtt | Volts, V | Vref – 0.04 | Vref | Vref + 0.04 |
| Termination Supply Current, Static | Itt | Amperes, A | | | 2.1<br>0 (Standby) [1]<br>0.100 (Standby) [2] |

**NOTES:**
If DDR Termination Voltage (VTT) Rail is Down During S3 Standby State
If DDR Termination Voltage (VTT) Rail is Up During S3 Standby State

#### 5.5.7.7.2 DDR SMRCOMP Pull-up Voltage (Vtt)

The following conditions apply to the specifications:

- Ittrc is measured at maximum VTT under maximum signal loading conditions.

**Table 5-17. DDR Termination Voltage and Current Requirements**

| Parameter | Symbol | Unit | Minimum | Nominal | Maximum |
|---|---|---|---|---|---|
| SMRCOMP Termination Supply Voltage, Static | Vtt | Volts, V | Vref – 0.04 | Vref | Vref + 0.04 |
| SMRCOMP Termination Supply Current, Static | Ittrc | Amperes, A | | | 0.040<br>0 (Standby) |

### 5.5.7.8 DDR Voltage Regulator Reference Design Example

Please reference the latest revision of the *Intel® 845E Reference Schematics (DDR).*

## 5.5.8 Power Sequencing Requirements

### 5.5.8.1 MCH Power Sequencing Requirements

There are no MCH power sequencing requirements. All MCH power rails should be stable before deasserting reset, but the power rails can be brought up in any order desired. Good design practice would have all MCH power rails come up as close in time as practical, with the core voltage (1.5 V) coming up first.

### 5.5.8.2 DDR-SDRAM Power Sequencing Requirements

No DDR-SDRAM power sequencing requirements are specified during power up or power down if the following criteria are met:

- VDD and VDDQ are driven from a single power converter output.
- VTT is limited to 1.44V (reflecting VDDQ(max)/2 + 50mV VREF variation + 40mV VTT variation)
- VREF < VDDQ + 0.3 V
- A minimum resistance of 42 Ω (22 Ω series resistor + 22 Ω parallel resistor - 5% tolerance) limits the input current from the VTT supply into any pin.

If the above criteria cannot be met by the system design, then the following table must be adhered to during power up:

**Table 5-18. Power-up Initialization Sequence (should above listed requirements not be met)**

| Voltage Description | Sequencing | Voltage Relationship to Avoid Latch-up |
|---|---|---|
| $V_{DD}Q$ | After or with $V_{DD}$ | < $V_{DD}$ + 0.3 V |
| $V_{TT}$ | After or with $V_{DD}Q$ | < $V_{DD}Q$ + 0.3 V |
| $V_{REF}$ | After or with $V_{DD}Q$ | < $V_{DD}Q$ + 0.3 V |

## 5.6 MCH DDR Signal Package Lengths

| DDR Data Signals | | | | | |
|---|---|---|---|---|---|
| Data Signal | MCH Ball | Package Length (inches) | Data Signal | MCH Ball | Package Length (inches) |
| SDQ0 | G28 | 0.716 | SDQ36 | B13 | 0.639 |
| SDQ1 | F27 | 0.699 | SDQ37 | C13 | 0.552 |
| SDQ2 | C28 | 0.874 | SDQ38 | C11 | 0.588 |
| SDQ3 | E28 | 0.754 | SDQ39 | D10 | 0.626 |
| SDQ4 | H25 | 0.532 | SDQ40 | E10 | 0.533 |
| SDQ5 | G27 | 0.666 | SDQ41 | C9 | 0.605 |
| SDQ6 | F25 | 0.592 | SDQ42 | D8 | 0.587 |
| SDQ7 | B28 | 0.892 | SDQ43 | E8 | 0.522 |
| SDQ8 | E27 | 0.797 | SDQ44 | E11 | 0.523 |
| SDQ9 | C27 | 0.833 | SDQ45 | B9 | 0.715 |
| SDQ10 | B25 | 0.812 | SDQ46 | B7 | 0.706 |
| SDQ11 | C25 | 0.753 | SDQ47 | C7 | 0.643 |
| SDQ12 | B27 | 0.886 | SDQ48 | C6 | 0.7 |
| SDQ13 | D27 | 0.867 | SDQ49 | D6 | 0.664 |
| SDQ14 | D26 | 0.773 | SDQ50 | D4 | 0.76 |
| SDQ15 | E25 | 0.645 | SDQ51 | B3 | 0.922 |
| SDQ16 | D24 | 0.722 | SDQ52 | E6 | 0.64 |
| SDQ17 | E23 | 0.602 | SDQ53 | B5 | 0.846 |
| SDQ18 | C22 | 0.699 | SDQ54 | C4 | 0.81 |
| SDQ19 | E21 | 0.566 | SDQ55 | E5 | 0.67 |
| SDQ20 | C24 | 0.785 | SDQ56 | C3 | 0.859 |
| SDQ21 | B23 | 0.781 | SDQ57 | D3 | 0.811 |
| SDQ22 | D22 | 0.64 | SDQ58 | F4 | 0.723 |
| SDQ23 | B21 | 0.711 | SDQ59 | F3 | 0.814 |
| SDQ24 | C21 | 0.627 | SDQ60 | B2 | 0.949 |
| SDQ25 | D20 | 0.555 | SDQ61 | C2 | 0.893 |
| SDQ26 | C19 | 0.587 | SDQ62 | E2 | 0.865 |
| SDQ27 | D18 | 0.522 | SDQ63 | G5 | 0.689 |
| SDQ28 | C20 | 0.615 | SCB0 | C16 | 0.57 |

| DDR Data Signals | | | | | |
|---|---|---|---|---|---|
| **Data Signal** | **MCH Ball** | **Package Length (inches)** | **Data Signal** | **MCH Ball** | **Package Length (inches)** |
| SDQ29 | E19 | 0.487 | SCB1 | D16 | 0.526 |
| SDQ30 | C18 | 0.579 | SCB2 | B15 | 0.623 |
| SDQ31 | E17 | 0.521 | SCB3 | C14 | 0.533 |
| SDQ32 | E13 | 0.432 | SCB4 | B17 | 0.621 |
| SDQ33 | C12 | 0.543 | SCB5 | C17 | 0.583 |
| SDQ34 | B11 | 0.596 | SCB6 | C15 | 0.54 |
| SDQ35 | C10 | 0.59 | SCB7 | D14 | 0.503 |
| **DDR Data Strobe Signals** | | | **DDR Clock Signals** | | |
| **Data Signal** | **MCH Ball** | **Package Length (inches)** | **Data Signal** | **MCH Ball** | **Package Length (inches)** |
| SDQS0 | F26 | 0.651 | SCK0 | E14 | 0.453 |
| SDQS1 | C26 | 0.775 | SCK#0 | F15 | 0.432 |
| SDQS2 | C23 | 0.738 | SCK1 | J24 | 0.454 |
| SDQS3 | B19 | 0.636 | SCK#1 | G25 | 0.587 |
| SDQS4 | D12 | 0.493 | SCK2 | G6 | 0.551 |
| SDQS5 | C8 | 0.596 | SCK#2 | G7 | 0.543 |
| SDQS6 | C5 | 0.776 | SCK3 | G15 | 0.371 |
| SDQS7 | E3 | 0.821 | SCK#3 | G14 | 0.349 |
| SDQS8 | E15 | 0.52 | SCK4 | E24 | 0.610 |
| | | | SCK#4 | G24 | 0.548 |
| | | | SCK5 | H5 | 0.589 |
| | | | SCK#5 | F5 | 0.693 |

§

# 6 AGP Interface Design Guidelines

For detailed AGP Interface functionality (protocols, rules, signaling mechanisms, etc.) refer to the AGP Interface Specification, Rev. 2.0, which can be obtained from:
http://www.agpforum.org.

This design guide focuses only on specific 845E chipset-based platform recommendations.

The latest AGP Interface Specification enhances the functionality of the original AGP Interface Specification, Rev. 1.0 by allowing 4x data transfers and 1.5 V operation. In addition to these enhancements, additional performance enhancement and clarifications, such as fast write capability, are featured in the *AGP Interface Specification, Rev. 2.0*. The 845E chipset supports these enhanced features and 1.5 V signaling only.

The 4x mode of operation on the AGP interface provides for "quad-sampling" of the AGP address/data and sideband address buses. This means data is sampled four times during each 66 MHz AGP clock cycle, or each data cycle is ¼ of 15 ns or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time, not the clock cycle time. During 2x mode, data is sampled twice during a 66 MHz clock cycle; therefore, the data cycle time is 7.5 ns. These high-speed data transfers are accomplished using source synchronous data strobing for 2x mode, and differential source synchronous data strobing for 4x mode.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, it is important to minimize noise and propagation delay mismatch. Noise on the data lines will cause the settling time to be high. If the mismatch between a data line and the associated strobe is too great or if there is noise on the interface, incorrect data will be sampled.

The AGP signals are broken into three groups: 1x timing domain, 2x/4x timing domain, and miscellaneous signals. In addition, the 2x/4x timing domain signals are divided into three sets of signals (#1-#3). All signals must meet the minimum and maximum trace length, width and spacing requirements. The trace length matching requirements are applicable only between the 2x/4x timing domain signal sets.

**Table 6-1. AGP 2.0 Signal Groups**

| 1x Timing Domain | 2x/4x Timing Domain | Miscellaneous Signals |
|---|---|---|
| AGPCLK<br>PIPE#<br>RBF#<br>WBF#<br>ST[2:0]<br>G_FRAME#<br>G_IRDY#<br>G_TRDY#<br>G_STOP#<br>G_DEVSEL#<br>G_REQ#<br>G_GNT#<br>G_PAR | SET #1<br>G_AD[15:0]<br>G_C/BE[1:0]#<br>AD_STB0<br>AD_STB0#<br><br>SET #2<br>G_AD[31:16]<br>G_C/BE[3:2]#<br>AD_STB1<br>AD_STB1#<br><br>SET #3<br>SBA[7:0]<br>SB_STB<br>SB_STB# | USB+<br>USB-<br>OVRCNT#<br>PME#<br>TYPDET#<br>PERR#<br>SERR#<br>INTA#<br>INTB# |

Strobe signals are not used in the 1x AGP mode. In 2x AGP mode, G_AD[15:0] and G_C/BE[1:0]# are associated with AD_STB0, G_AD[31:16] and G_C/BE[3:2]# are associated with AD_STB1, and SBA[7:0] is associated with SB_STB. In 4x AGP mode, AD[15:0] and G_C/BE[1:0]# are associated with AD_STB0 and AD_STB0#, AD[31:16] and C/BE[3:2]# are associated with AD_STB1 and AD_STB1#, and SBA[7:0] is associated with SB_STB and SB_STB#.

## 6.1 AGP Routing Guidelines

The following section documents the recommended routing guidelines for 845E chipset-based designs. All aspects of the interface will be covered from signal trace length to decoupling. These trace length guidelines apply to ALL of the signals listed as 2x/4x timing domain signals. These signals should be routed using 5 mils traces for a 60 Ω impedance, using the stack-up described in Figure 3-2.

These guidelines are not intended to replace thorough system simulations and validation. These guidelines are subject to change as simulation data is gathered.

### 6.1.1 1X Timing Domain Signal Routing Guidelines

The 1x signals should adhere to the follow routing guidelines:

- All 1x timing domain signal maximum trace lengths are 7.5 inches.
- 1x timing domain signals can be routed with 5 mil minimum trace separation.
- There are no trace length matching requirements for 1x timing domain signals.

## 6.1.2 2X/4X Timing Domain Signal Routing Guidelines

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6 in.) and the long AGP interfaces (e.g., > 6 in. and < 7.25 in.) are documented separately. The maximum length allowed for the AGP interface is 7.25 inches.

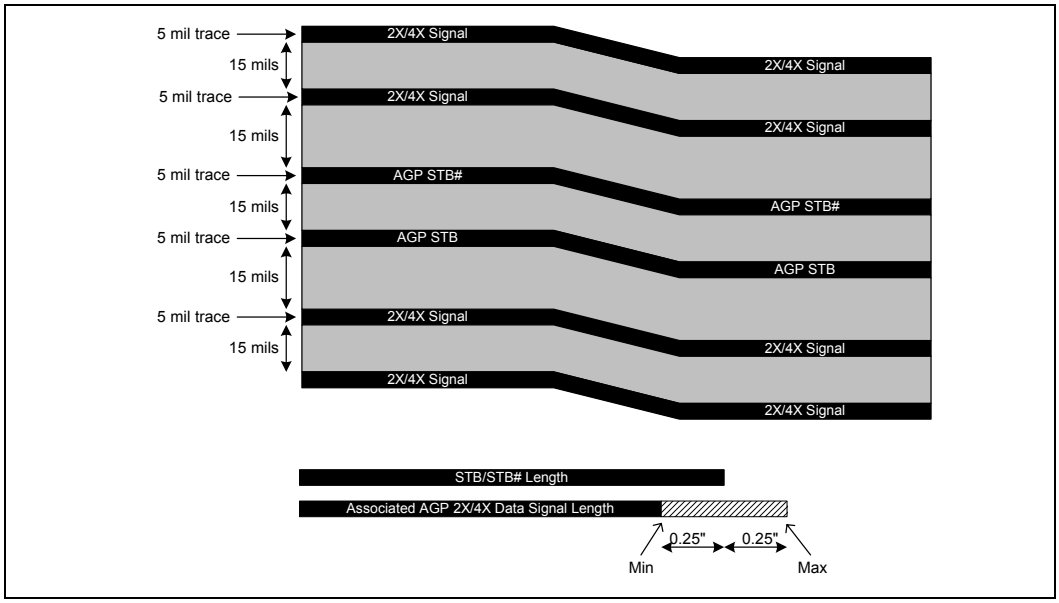
### 6.1.2.1 Trace Lengths Less Than 6 Inches

If the AGP interface is less than 6 inches with 60 Ω ±15% board impedance, at least 5 mil traces with at least 15 mils of space (1:3) between signals is required for 2x/4x lines (data and strobes). These 2x/4x signals must be matched to their associated strobe within ± 0.25 in.

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 5.3 in. long, the data signals associated with those strobe signals (e.g., G_AD[15:0] and G_C/BE[3:0]#), can be 5.05 in. to 5.55 in. long. While another strobe set (e.g., SB_STB and SB_STB#) could be 4.2 in. long and the data signals associated to those strobe signals (e.g., SBA[7:0]) can be 3.95 in. to 4.45 in. long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface. Special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from all other signals by at least 15 mils. The strobe pair must be length matched to less than ±0.1 in. (that is, a strobe and its compliment must be the same length within 0.1 in.).

**Figure 6-1. AGP 2X/4X Routing Example for Interfaces Less Than 6 Inches**



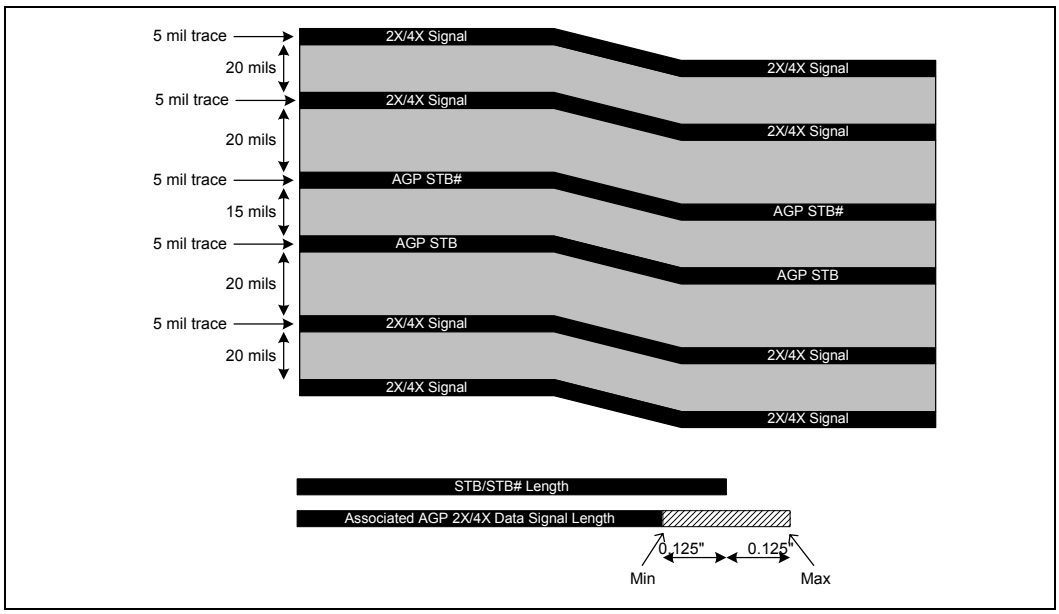
### 6.1.2.2 Trace Lengths Greater Than 6 Inches and Less Than 7.25 Inches

If the AGP interface is greater than 6 inches and less than 7.25 inches with 60 Ω ± 15% board impedance then at least 5 mil traces with at least 20 mils of space (1:4) between signals is required for 2x/4x lines (data and strobes). These 2x/4x signals must be matched to their associated strobe within ± 0.125 in.

For example, if a set of strobe signals (e.g., AD_STB0 & AD_STB0#) are 6.5 in. long, the data signals that are associated with those strobe signals (e.g., AD[15:0] & C/BE2:0]#), can be 6.475 in. to 6.625 in. long. Another strobe set (e.g., SB_STB & SB_STB#) could be 6.2 in. long, and the data signals that are associated with those strobe signals (e.g., SBA[7:0]), can be 6.075 in. to 6.325 in. long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface. Special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from all other signals by at least 20 mils. The strobe pair must be length matched to less than ± 0.1 in. (that is, a strobe and its compliment must be the same length within 0.1 in.).

**Figure 6-2. AGP 2X/4X Routing Example for Interfaces Between 6 Inches and 7.25 Inches**



## 6.1.3 AGP Interfaces Trace Length Summary

The 2X/4X Timing Domain Signals can be routed with 5-mil spacing when breaking out of the MCH. The routing must widen to the documented requirements within 0.15 in. of the MCH package.

When matching trace length for the AGP 4X interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.

To reduce trace to trace coupling (cross-talk), separate the traces as much as possible. The trace length and trace spacing requirements must not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.

### Table 6-2. AGP 2.0 Routing Summary

| Signal | Maximum Length | Trace Spacing (5 mil traces) | Length Mismatch | Relative To |
|---|---|---|---|---|
| 1X Timing Domain | 7.5 in. | 5 mils | No requirement | N/A |
| 2X/4X Timing Domain Set #1 | 7.25 in. | 20 mils | ± 0.125 in. | AD_STB0 and AD_STB0# |
| 2X/4X Timing Domain Set #2 | 7.25 in. | 20 mils | ± 0.125 in. | AD_STB1 and AD_STB1# |
| 2X/4X Timing Domain Set #3 | 7.25 in. | 20 mils | ± 0.125 in. | SB_STB and SB_STB# |
| 2X/4X Timing Domain Set #1 | 6 in. | 15 mils | ± 0.25 in. | AD_STB0 and AD_STB0# |
| 2X/4X Timing Domain Set #2 | 6 in. | 15 mils | ± 0.25 in. | AD_STB1 and AD_STB1# |
| 2X/4X Timing Domain Set #3 | 6 in. | 15 mils | ± 0.25 in. | SB_STB and SB_STB# |

**NOTES:**
1. All trace widths are 5 mils.
2. Each strobe pair must be separated from other signals by at least 15 mils for signal maximum lengths of 6 in., and at least 20 mils for signal maximum lengths of 7.25 in.
3. Strobe and strobe bar pairs must be separated from each other by 15 mils and must be the same length.
4. These guidelines apply to board stackups described in Section 3.

### Table 6-3. AGP Signal Routing Guidelines

| Parameter | Routing Guidelines |
|---|---|
| Breakout Guidelines | 5 mil width with 5 mil spacing for a max of 0.15 in. |

### 6.1.4 Signal Power/Ground Referencing Recommendations

It is strongly recommended that signals do not change referencing. If a signal is power referenced it should stay referenced to power, and if it is referenced to ground it should stay referenced to ground. It is strongly recommended that AGP signals have a maximum of 1 via. All signals in a signal group should be routed on the same layer. If a signal is power referenced, it MUST stay referenced to power.

### 6.1.5 VDDQ and TYPEDET#

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller and is always 3.3 V.VDDQ is the interface voltage. The 845E chipset supports only an interface voltage of 1.5 V.

AGP 2.0 specification requires VCC and VDDQ to be tied to separate power planes, and implements a TYPEDET# (type detect) signal on the AGP connector that determines the interface operating voltage (VDDQ). Designs based on the 845E chipset do not require TYPEDET# detection because the 845E chipset supports 1.5 V AGP add-in cards. 3 V AGP add-in cards are not supported.

### 6.1.6 VREF Generation

For 1.5 V add-in cards, the graphics controller and MCH generate AGP voltage reference VREF and distribute it through the connector. Two signals have been defined on the 1.5 V connector to allow VREF delivery:

- VREFGC—VREF from the graphics controller to the chipset
- VREFCG—VREF from the chipset to the graphics controller

However, the usage of the source generated VREFCG at the MCH is not required per the AGP Interface Specification, rev 2.0. Given this and the fact that the MCH requires the presence of VREF when an AGP add-in card is present and not present, the following circuit is recommended for VREF generation.

The VREF divider network should be placed near the AGP connector. The minimum trace spacing around the VREF signal must be 25 mils to reduce cross talk and maintain signal integrity, and a 0.1 µF bypass capacitor should be placed within 0.8 in. of the MCH AGPREF ball. VREF voltage must be 0.5 x VDDQ for 1.5 V operation.

**Figure 6-3. AGP 2.0 VREF Generation and Distribution for 1.5 V Cards**

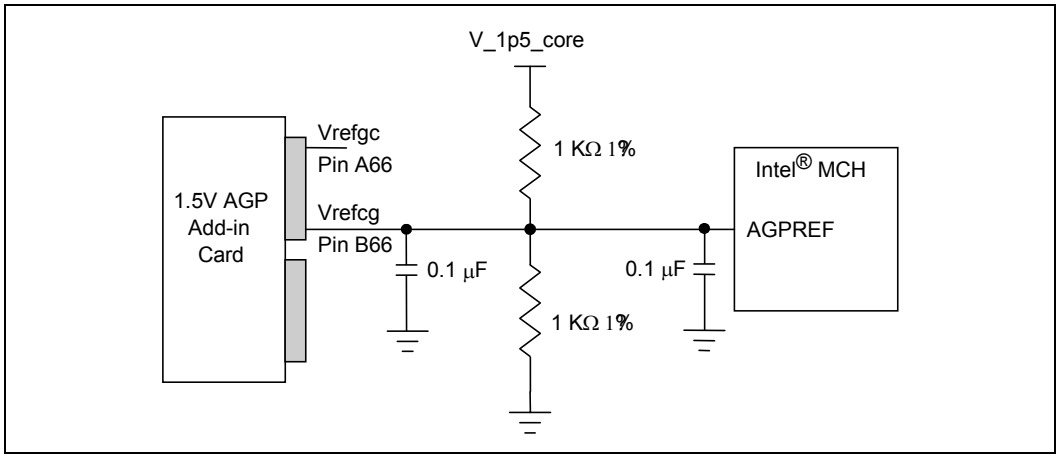



**Table 6-4. AGP VREF Routing Guidelines**

| Parameter | Routing Guidelines |
|---|---|
| AGP VREF trace width | 12 mils |
| AGP VREF trace spacing to other signals | 25 mils |
| AGP VREF trace breakout guidelines | 5 mil width with 5 mil spacing for a max of 0.15 in. |
| AGP VREF decoupling—MCH max distance | 0.8 in. |

## 6.1.7 MCH AGP Interface Buffer Compensation

The MCH AGP interface supports resistive buffer compensation (GRCOMP). The GRCOMP signal must be tied to a 40 Ω 2% resistor to ground. This trace should be kept to 10 mils wide and less than 0.5 in. long.

AGP signals have integrated pull-up resistors to AGP VDDQ, and pull-down resistors to ground. This is to ensure stable values are maintained when agents are not actively driving the bus. Table 6-5 lists signals that have integrated AGP pull-up/pull-down resistors. Their value is between 4 kΩ and 16 kΩ. External pull-ups and pull-downs are not needed for these signals.

***Note:*** 1x mode, trace stub to pull-up resistor should be kept to less than 0.5 in.
2x/4x mode, trace stub to pull-up resistor should be kept to less than 0.1 in.

Short stub lengths help minimize signal reflections from the stub. The strobe signals require pull-up/pull-down on the motherboard to ensure stable values when there are no agents driving the bus.

### Table 6-5. MCH AGP Signals with Integrated Pull-up/Pull-down Resistors

| Signals | Pull-Up/Pull-Down |
|---|---|
| **1x Timing Domain** | |
| G_FRAME# | pull-up resistor to VCC1_5 |
| G_TRDY# | pull-up resistor to VCC1_5 |
| G_IRDY# | pull-up resistor to VCC1_5 |
| G_DEVSEL# | pull-up resistor to VCC1_5 |
| G_STOP# | pull-up resistor to VCC1_5 |
| RBF# | pull-up resistor to VCC1_5 |
| PIPE# | pull-up resistor to VCC1_5 |
| G_REQ# | pull-up resistor to VCC1_5 |
| WBF# | pull-up resistor to VCC1_5 |
| **2x/4x Timing Domain** | |
| AD_STB[1:0] | pull-up resistor to VDDQ |
| SB_STB | pull-up resistor to VDDQ |
| AD_STB[1:0]# | pull-down resistor to GND |
| SB_STB# | pull-down resistor to GND |

## 6.1.8 MCH External AGP Pull-up/Pull-down Resistors

The MCH G_GNT# output signal is tri-stated during RSTIN# assertion. This signal must have an external 6.8 kΩ pull-up resistor to keep it from floating during the RSTIN# assertion.

***Note:*** The G_GNT# signals require pull-up resistor to the MCH's VCC1_5.

The MCH ST1 signal is sampled by the MCH at power-on to configure MCH processor system bus speed. If MCH ST1 is sampled high, the processor bus speed is 400MHz. If MCH ST1 is sampled low, the processor bus speed is 533MHz. An internal MCH pull-up resistor on this signal sets the default processor system bus speed to 400MHz. Refer to section 12.5.1 for an example circuit where the processor's BSEL signals select the processor bus speed.

The MCH AGP ST0 signal requires a 2 kΩK to ground.

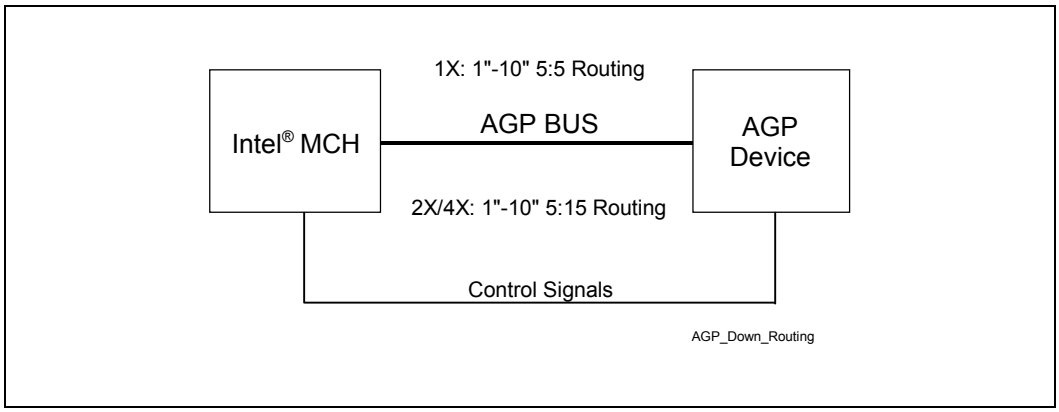
**Table 6-6. MCH AGP Signals Requiring External Pull-up/Pull-down Resistors**

| Signals | Pull-Up/Pull-Down |
|---|---|
| G_GNT# | 6.8 kΩ pull-up resistor to VCC1_5 |
| ST0 | 2 kΩ pull-down resistor to ground |

## 6.1.9 AGP Device Down Routing Guidelines

Routing guidelines for the AGP device 'down' option are very similar to those used when routing to an AGP connector. For any routing/layout information that is not included in this section of design guidelines, refer to the AGP up routing/layout guidelines in this chapter. Figure 6-4 shows the on-board AGP layout.

**Figure 6-4. AGP Device Down Routing Guidelines**



### 6.1.9.1 1X Timing Domain Signal Routing Guidelines

The 1x signals should adhere to the follow routing guidelines:

- All 1x timing domain signals have a maximum trace length of 10 inches.
- 1x timing domain signals can be routed with 5 mil minimum trace separation.
- 1x timing domain signals can be routed with 5 mil minimum trace width.
- There are no trace length matching requirements for 1x timing domain signals.

In all cases it is best to reduce the line length mismatch wherever possible to insure added margin. It is also best to separate the traces by as much as possible to reduce the amount of trace-to-trace coupling.

**Table 6-7. 1X Timing Domain Trace Length Recommendations for AGP Device Down**

| Width: Space | Trace | Line Length | Line Length Matching |
|---|---|---|---|
| 5:5 | Control | 1.0 in < line length < 10 in | Not required |

### 6.1.9.2 2X/4X Timing Domain Signal Routing Guidelines

The 2x/4x signals should adhere to the follow routing guidelines:

- All 2x/4x timing domain signals have a maximum trace length of 10 inches.
- 2x/4x timing domain signals can be routed with 15 mil minimum trace separation.
- 2x/4x timing domain signals can be routed with 5 mil minimum trace width.

**Table 6-8. 2X/4X Timing Domain Trace Length Recommendations for AGP Device Down**

| Width:Space | Trace | Line Length | Line Length Matching |
|---|---|---|---|
| 5:15 | Data/Strobe | 1.0 in < line length < 10 in | Refer to section 6.1.2.2 |

Some of the signals require pull-up or pull-down resistors to be installed on the motherboard. Refer to Table 6-6 for a list of these signals.

## 6.1.10 AGP Connector

The 845E chipset supports only 1.5 V add-in cards. A 1.5 V AGP card uses the AGP 3 V connector and rotates it 180 degrees on the planar. Therefore, the key of the connector moves to the opposite side of the planar away from the I/O panel and will not allow 3 V add-in cards. A 1.5 V AGP Pro50* connector is an extension of the AGP connector. It has additional power and ground pins at each end of the connector and is back compatible with a 1.5 V AGP card. Intel recommends a 1.5 V AGP Pro50* connector for workstations, and a 1.5 V AGP connector for desktop systems.

The designer should ensure that the AGP connector is well decoupled as described in the revision 1.0 of the AGP Design Guide, Section 1.5.3.3 (i.e., use a 0.01 µF capacitor for each power pin, a bulk 10 µF tantalum capacitor on VDDQ, and 20 µF tantalum capacitor on VCC3_3 plane near the connector.).

## 6.1.11 AGP Connector Decoupling Guidelines

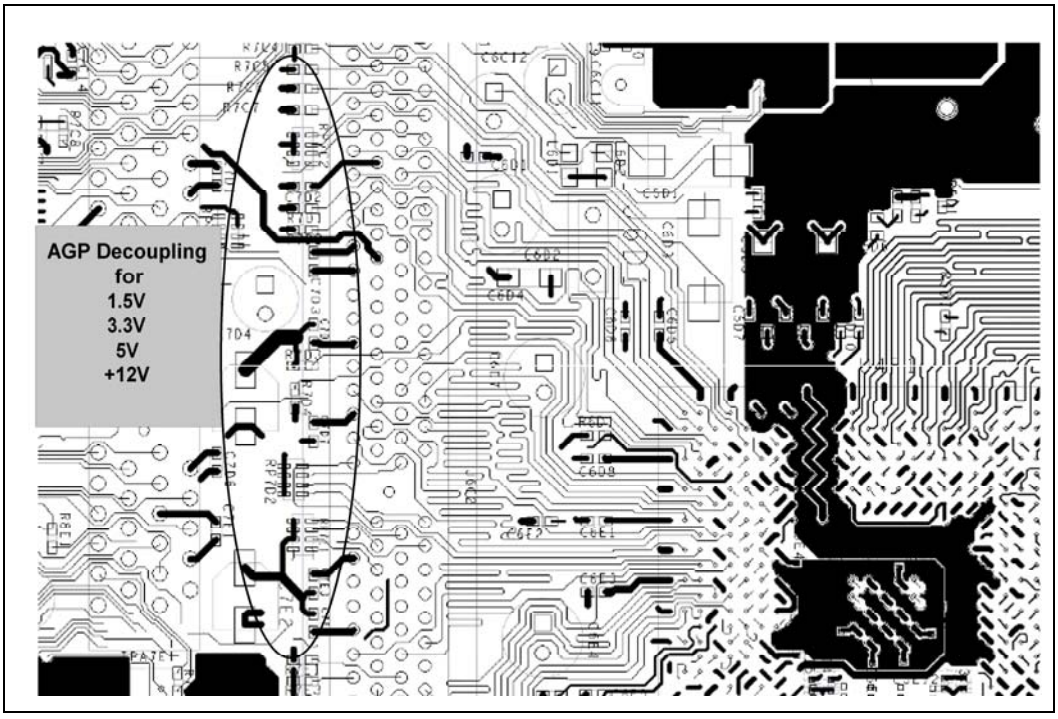
The following decoupling is suggested for decoupling the 1.5 V power plane at the AGP connector. Figure 6-5 shows the general location of AGP decoupling capacitors on layer 1. Actual component placement will depend upon how the 1.5 V, 3.3 V, 5 V, and +12 V power planes are split on layer 2.

**Table 6-9. 1.5 V Decoupling at the AGP Connector**

| Voltage | Number of Capacitors | Component |
|---|---|---|
| 1.5 V | 6 | 0.1 µF ceramic capacitor, 603 body type, X7R dielectric |
| 3.3 V | 3 | 0.1 µF ceramic capacitor, 603 body type, X7R dielectric |
| | 1 | 22 µF electrolytic capacitor |
| | 1 | 100 µF electrolytic capacitor |
| 5 V | 1 | 0.1 µF ceramic capacitor, 603 body type, X7R dielectric |
| | 1 | 10 µF aluminum electrolytic capacitor |
| 12 V | 1 | 0.1 µF ceramic capacitor, 603 body type, X7R dielectric |

The designer should ensure that the AGP connector is well decoupled as described in the revision 1.0 of the AGP Design Guide, Section 1.5.3.3.

**Figure 6-5. AGP Decoupling on Layer 1**



## 6.1.12 AGP Universal Retention Mechanism (RM)

Environmental testing and field reports indicate that, without proper retention, AGP cards may become unseated during system shipping and handling. To prevent the disengagement of AGP cards, Intel recommends that AGP-based platforms use the AGP retention mechanism (RM).

The AGP RM is a mounting bracket used to properly locate the card with respect to the chassis, and to assist with card retention. The AGP RM is available in two different handle orientations: left-handed (Figure 6-6), and right-handed. Most system boards accommodate the left-handed AGP RM. Because the manufacturing capacity is greater for the left-handed RM, Intel recommends that customers design into their systems the left-handed AGP RM. The right-handed AGP RM is identical to the left-handed AGP RM except for the position of the actuation handle, which is located on the same end as in the primary design but extends from the opposite side, parallel to the longitudinal axis of the part. Figure 6-7 details the keep-out information for the left-handed AGP RM. Use this information to ensure that motherboard designs leave adequate space for RM installation.

The AGP interconnect design requires that the AGP card be retained to limit card back out within the AGP connector to 0.99 mm (0.039 in.) max. For this reason, new cards should have an additional mechanical keying tab notch that provides an anchor point on the AGP card for interfacing with the AGP RM. The RM's round peg engages with the AGP card's retention tab, thereby preventing the card from disengaging during dynamic loading. The additional notch in the mechanical keying tab is required for 1.5 V AGP cards, and is recommended for the new 3.3 V AGP cards.

**Figure 6-6. AGP Left-Handed Retention Mechanism**

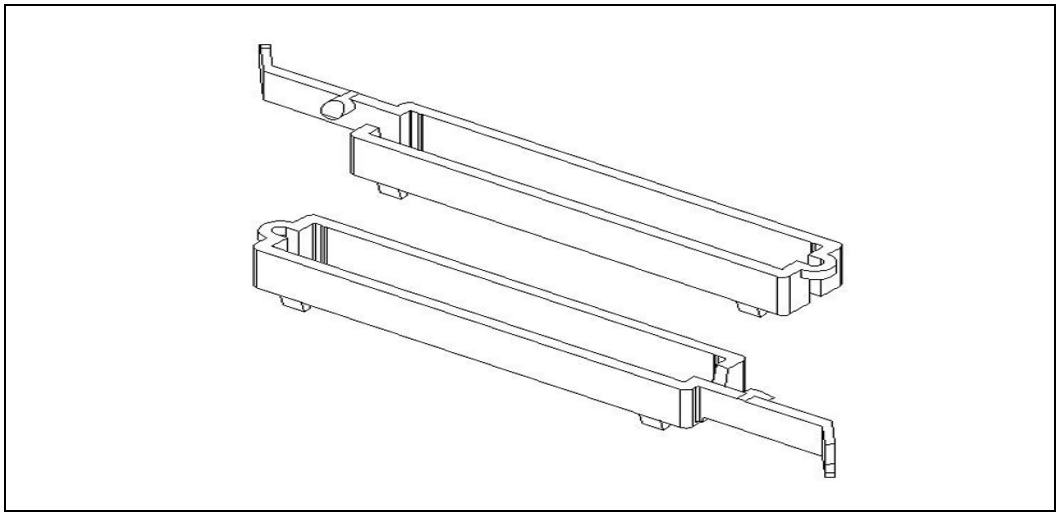
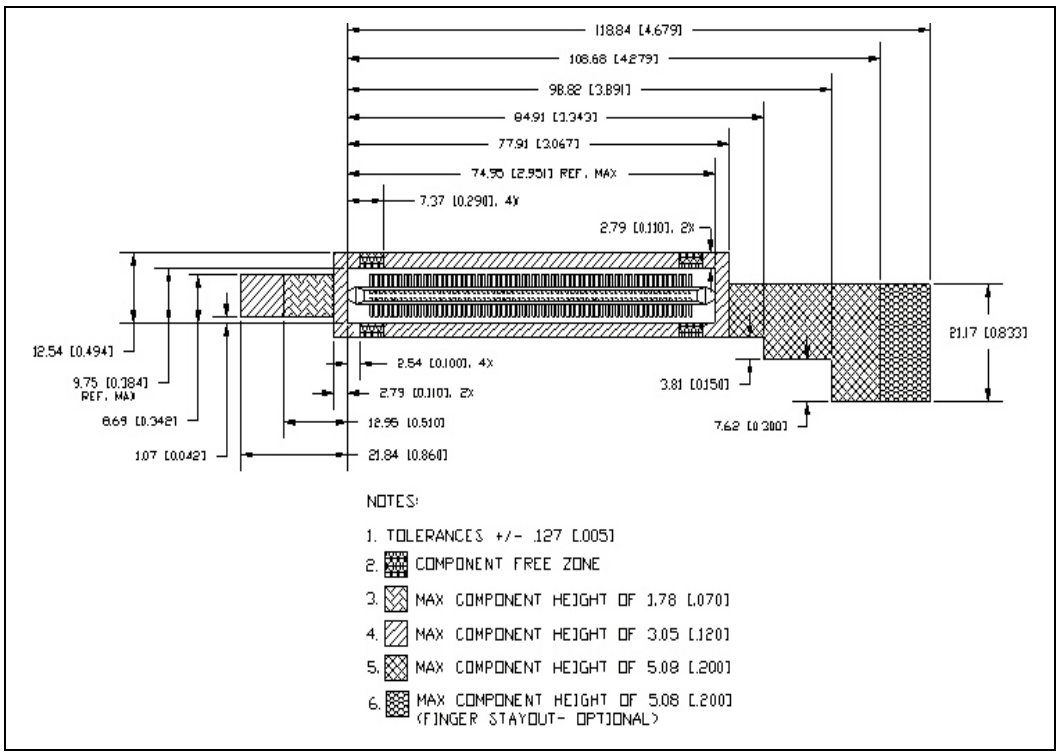


**Figure 6-7. Left-Handed RM Keep-Out Information**




Recommended for all AGP cards, the AGP RM is detailed in Engineering Change Request No. 48 (ECR #48), which details approved changes to the *Accelerated Graphics Port (AGP) Interface Specification, Revision 2.0*. Intel intends to incorporate the AGP RM changes into later revisions of the AGP interface specification. In addition, Intel has defined a reference design for a mechanical device utilizing the features defined in ECR #48.

ECR #48 can be viewed on the Intel Web site at:
http://developer.intel.com/technology/agp/ecr.htm

More information regarding this component (AGP RM) is available from the following vendors:

| Resin Color | Supplier | Part Number | |
|---|---|---|---|
| | | Left-Handed Orientation (Preferred) | Right-Handed Orientation (Alternate) |
| Black | AMP P/N | 136427-1 | 136427-2 |
| | Foxconn P/N | 006-0002-939 | 006-0001-939 |
| Green | Foxconn P/N | 009-0004-008 | 009-0003-008 |

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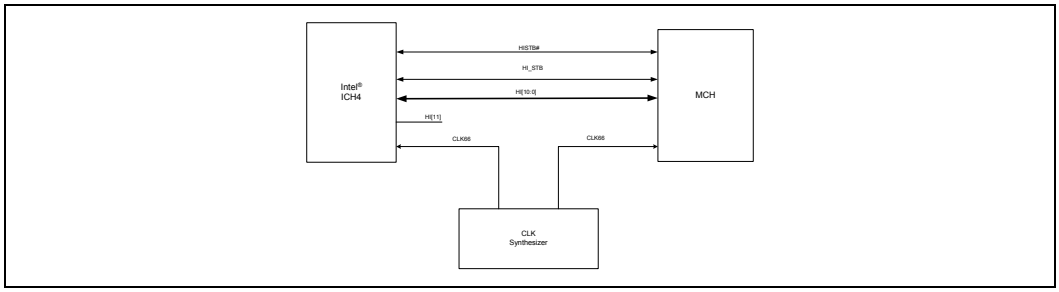
# 7 Hub Interface

The MCH and ICH4 ballout assignments have been optimized to simplify the hub interface routing between these devices. It is recommended that the hub interface signals be routed directly from the MCH to ICH4 with all signals referenced to VSS. Layer transition should be keep to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signal on the same layer.

The hub interface signals are broken into two groups: data signals (HI) and strobe signals (HI_STB). For the 8-bit hub interface, HI[11:0] are associated with HI_STB/HI_STBS and HI_STB#/HI_STBF.

**Figure 7-1. Hub Interface Routing Example**




## 7.1 Hub Interface Routing Guidelines

This section documents the routing guidelines for the Hub Interface. This Hub Interface connects the ICH4 to the MCH. The trace impedance must equal 60 Ω ± 15%.

**Table 7-1. 8-Bit Hub Interface Buffer Configuration Setting**

| Trace Impedance | Strap |
|---|---|
| 50Ω, 56Ω, or 60Ω | HICOMP pulled to $V_{SS}$[1] |

- Reference Section 7.1.5 for the specific resistor value.

### 7.1.1 Hub Interface Strobe Signals

The Hub Interface strobe signals should be routed 5 mils wide with 15 mils trace spacing (5 on 15). This strobe pair should have a minimum of 15 mils spacing from any adjacent signals. The maximum length for the strobe signals is 2” to 8”. Each strobe signal must be the same length and each data signal must be matched within ± 100mils of the strobe signal.

## 7.1.2 Hub Interface Data Signals

The Hub Interface data signal traces should be routed 5 mils wide with 15 mils trace spacing (5 on 15). In order to break out of the MCH and ICH4 package, the Hub Interface data signals can be routed 5 on 5 within 300 mils of the package.

The maximum Hub Interface data signal trace length is 2" to 8". Each data signal must be matched within ± 100mils of the HISTB/HISTB# pair.

## 7.1.3 Hub Interface Signal Referencing

The Hub Interface signal traces (HI[10:0]) and the two Hub Interface strobe signals (HISTB and HISTB#) must all be referenced to ground to insure proper noise immunity.

## 7.1.4 Hub Interface HIREF/HI_SWING Generation/Distribution

HIREF is the hub interface reference voltage. The HIREF voltage requirement and associated resistor recommendations for the voltage divider circuit must be set according to the table below.

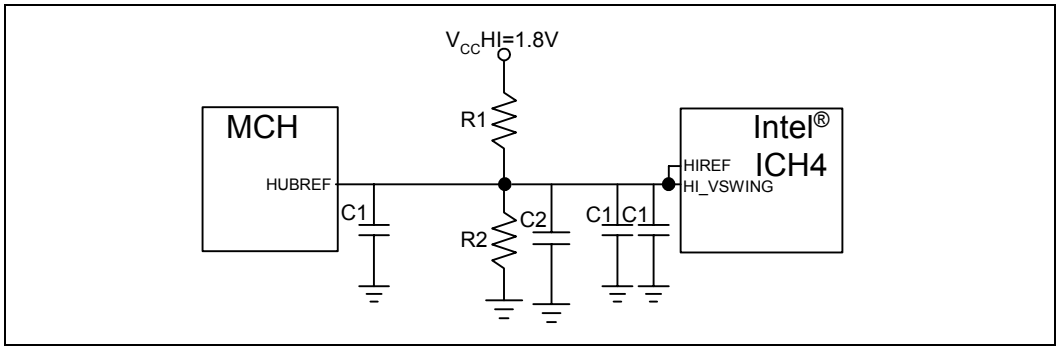
**Table 7-2. Hub Interface HIREF/HI_SWING Generation Circuit Specifications**

| HIREF Voltage Specification | Recommended Resistor Values for the HIREF Divider Circuit |
|---|---|
| ½ VCC1_8 ± 2% | R1 = R2 = 150 Ω ± 1% |

The HIREF divider should not be located more than 4 inches away from either MCH or ICH4. The reference voltage generated by a single HIREF divider should be bypassed to ground at each component with a 0.01 µF capacitor located close to the component HIREF pin.

The resistor values R1 & R2, must be rated at 1% tolerance. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. A 0.1 µF capacitor should be placed close to R1 and R2.

**Figure 7-2. Hub Interface with Resistor Divider Circuit**



## 7.1.5 Hub Interface Compensation

The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires resistive compensation (RCOMP).

**Table 7-3. Hub Interface HICOMP Resistor Values**

| Component | Trace Impedance | RCOMP Resistor Value | RCOMP Resistor Tied to |
|---|---|---|---|
| ICH4 | 60Ω ± 15% | 40.2 Ω ± 1% | Vss |
| MCH | 60Ω + 15% | 40.2 Ω ± 1% | 1.8 V |

## 7.1.6 Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors per each component (i.e. the ICH4 and MCH). These capacitors should be placed within 150 mils from each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCCHI=1.8 V side of the capacitors to the VCCHI=1.8 V power pins. Similarly, if layout allows, metal fingers running on the VCCHI=1.8 V side of the board should connect the ground side of the capacitors to the VSS power pins.

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# 8 Intel® ICH4

## 8.1 IDE Interface

This section contains guidelines for connecting and routing the ICH4 IDE interface. The ICH4 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH4 has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors may be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5-mil traces on 7-mil spaces and must be less than 8 inches long (from ICH4 to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inch.

**Table 8-1. IDE Routing Summary**

| Trace Impedance | IDE Routing Requirements | Maximum Trace Length | IDE Signal Length Matching |
|---|---|---|---|
| 51Ω to 69 Ω, 60 Ω Target | 5 on 7 | 8 inches | No more than 0.5 inch (500 mils) between the shortest data signal and the longest strobe signal of a channel. |

### 8.1.1 Cabling

**Length of cable**: Each IDE cable must be equal to or less than 18 inches.

**Capacitance**: Less than 35 pF.

**Placement**: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).

**Grounding**: Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.

#### 8.1.1.1 Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH4 IDE controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5, and native mode IDE. Note that there are no motherboard hardware requirements for supporting native mode IDE. Native mode IDE is supported through the operating system and system driver. The ICH4 must determine the type of cable that is present to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector).

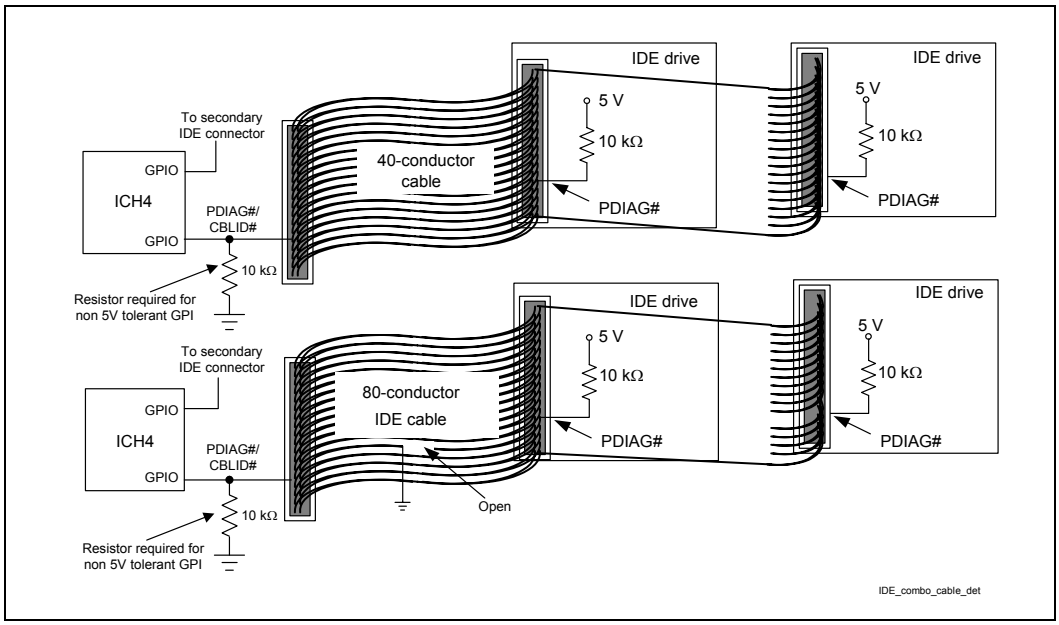
To determine if Ultra DMA modes greater than 2 (Ultra ATA/33) can be enabled, the ICH4 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA mode 2 (Ultra ATA/33).

Intel recommends that cable detection be done using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system, because this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

### 8.1.1.2 Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the *ATA/ATAPI-6 Standard*) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 8-1. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. A 10 kΩ pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present and allows for use of a non-5 V tolerant GPIO.

**Figure 8-1. Combination Host-Side/Device-Side IDE Cable Detection**



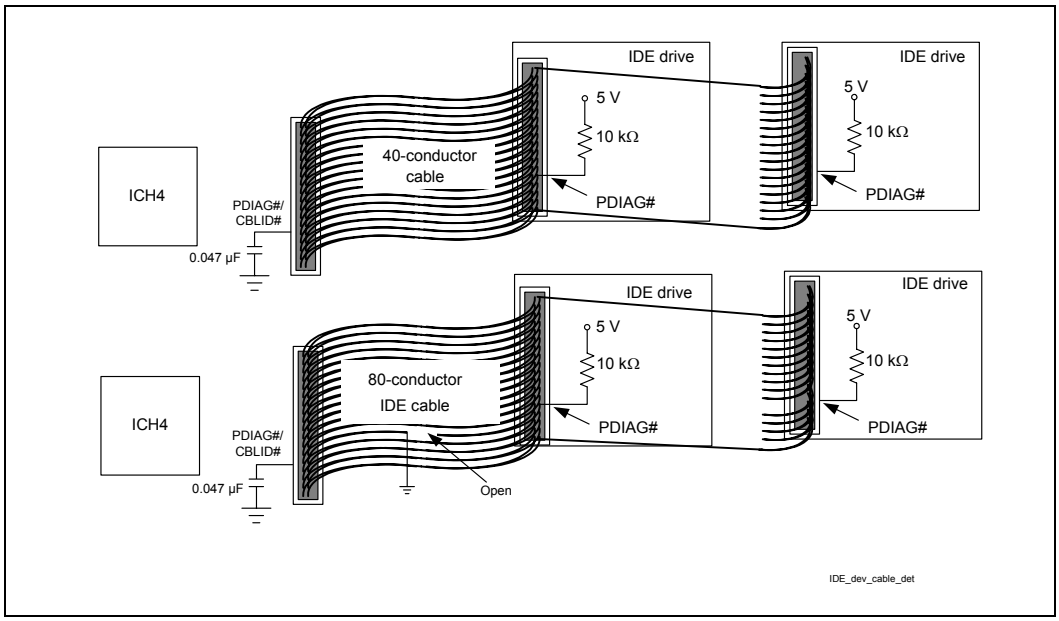

This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high, there is 40-conductor cable in the system and Ultra DMA modes greater than 2 must not be enabled.

If PDIAG#/CBLID# is detected low, there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the *ATA/ATAPI-6 Standard*. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is a 1, an 80-conductor cable is present. If this bit is 0, a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present, and notify the user of the problem.

### 8.1.1.3 Device-Side Cable Detection

For platforms that must implement Device-Side detection only (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 8-2. This capacitor should not be populated when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described above. Note that some drives may not support device-side cable detection.

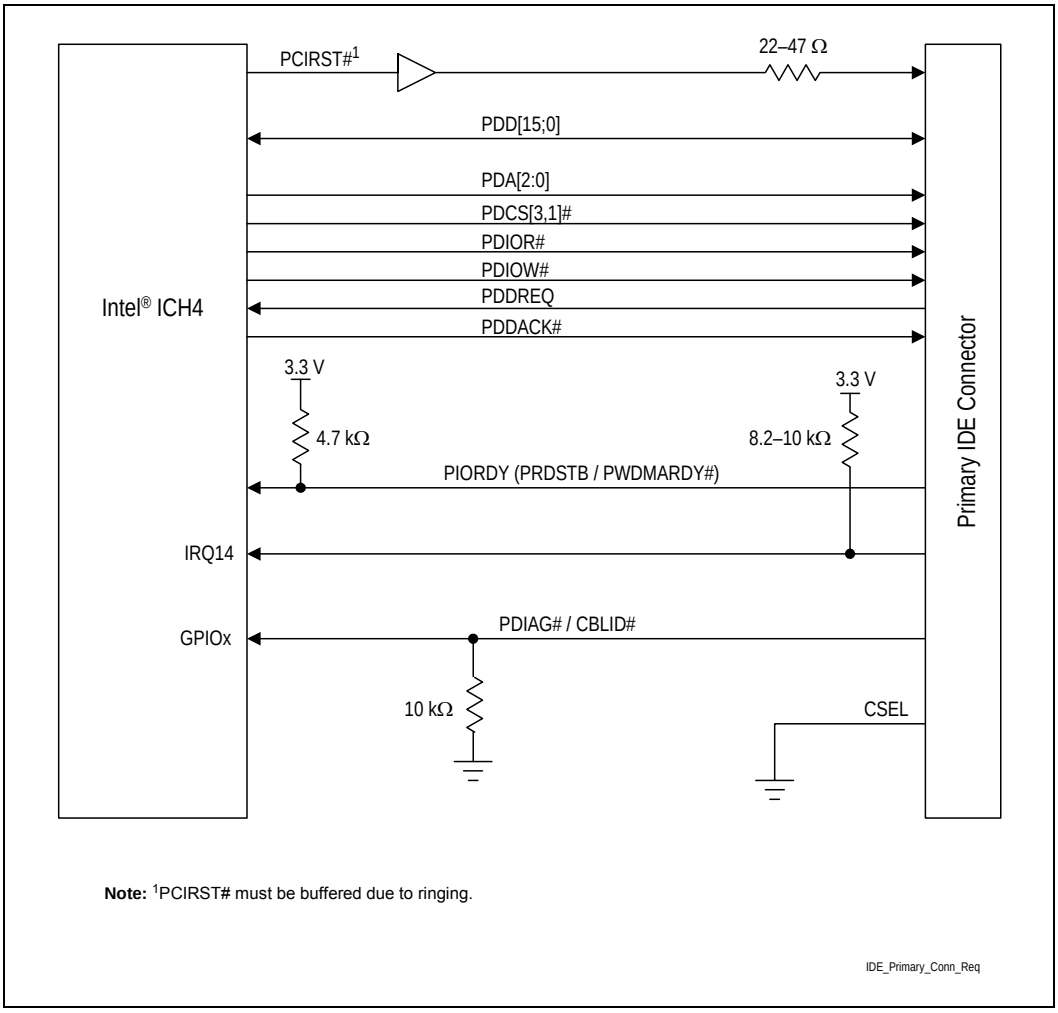
**Figure 8-2. Device Side IDE Cable Detection**




This mechanism creates a resistor-capacitor (RC) time constant. Drives supporting Ultra DMA modes greater than 2 (Ultra DMA/33) drive PDIAG#/CBLID# low and then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host and therefore the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore, the signal rises more slowly, as the capacitor charges. The drive can detect the difference in rise times and it will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the *ATA/ATAPI-6 Standard*.

## 8.1.2 Primary IDE Connector Requirements

**Figure 8-3. Connection Requirements for Primary IDE Connector**

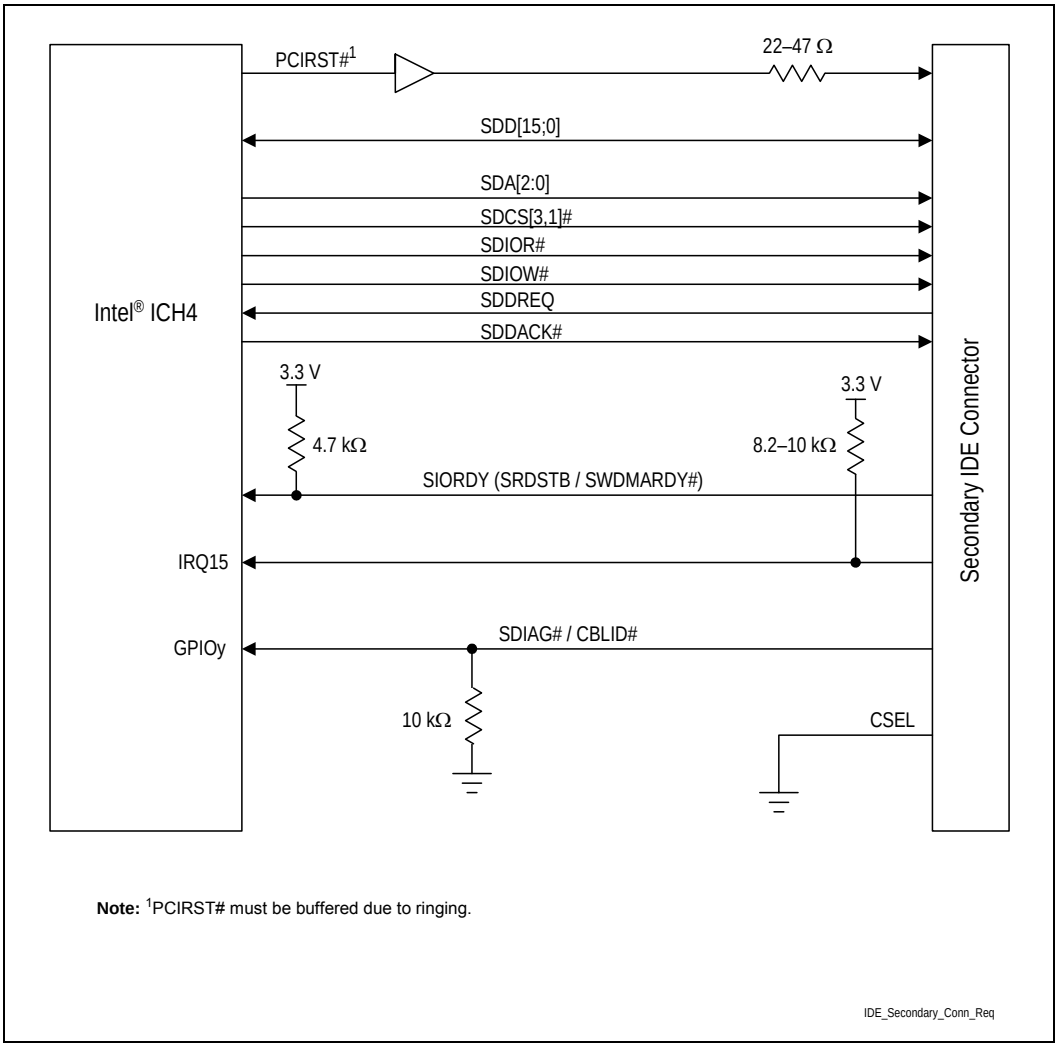



**NOTES:**

1. 22 kΩ – 47 kΩ series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 to VCC3_3.
3. A 4.7 kΩ pull-up resistor to VCC3_3 is required on PIORDY.
4. Series resistors can be placed on the control and data line to improve signal quality. The resistors are place as close to the connector as possible. Values are determined for each unique motherboard design.
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the primary connector. This change is to prevent the GPIO pin from floating if a device is not present on the IDE interface.

## 8.1.3 Secondary IDE Connector Requirements

**Figure 8-4. Connection Requirements for Secondary IDE Connector**




**Note:** [1]PCIRST# must be buffered due to ringing.

**NOTES:**

1. 22 kΩ – 47 kΩ series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
2. An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ15 to VCC3_3.
3. A 4.7 kΩ pull-up resistor to VCC3_3 is required on SIORDY.
4. Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.
5. The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is required on the secondary connector. This change is to prevent the GPIO pin from floating if a device is not present on the IDE interface.

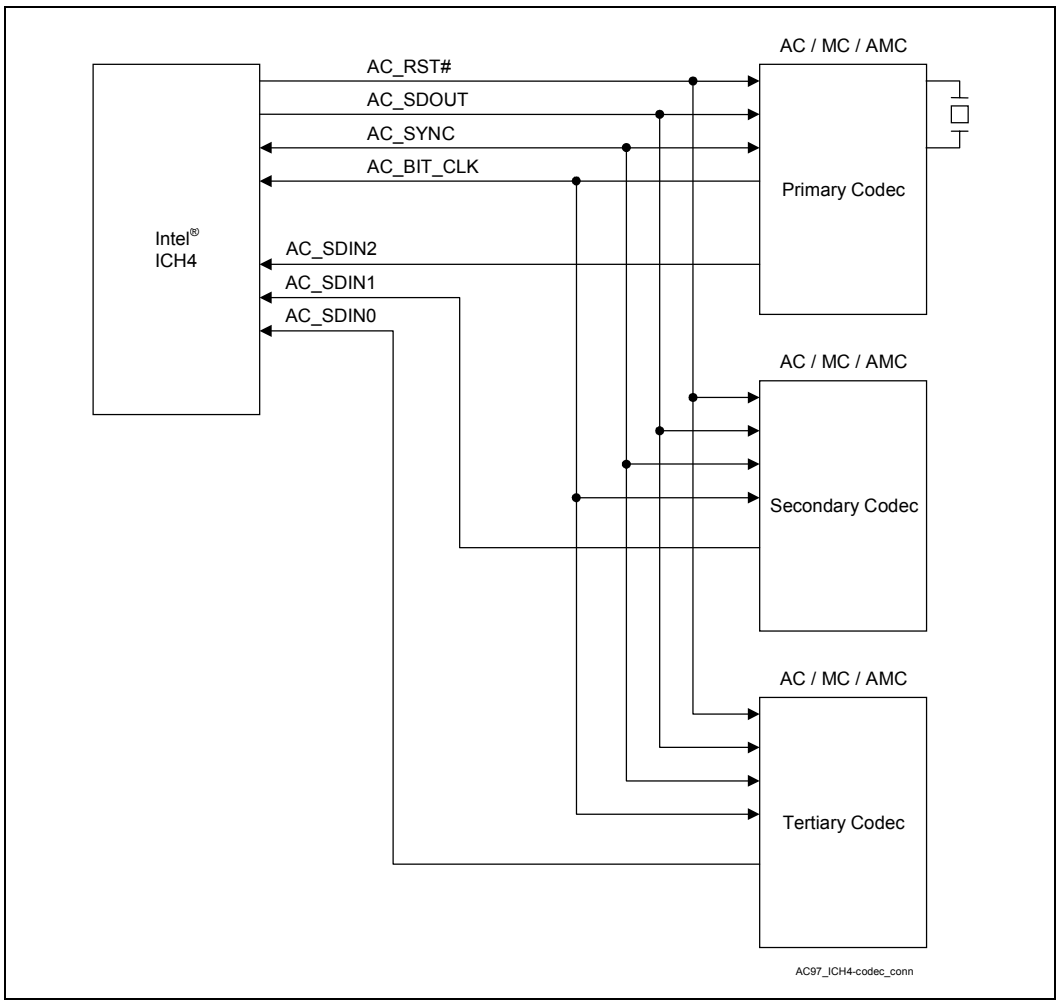
## 8.2 AC '97

The ICH4 implements an AC '97 2.3 compatible digital controller. Contact your codec IHV (Independent Hardware Vendor) for information on AC '97 2.3 compliant products. The AC '97 2.3 specification is on the Intel website:

http://developer.intel.com/ial/scalableplatforms/audio/index.htm#97spec

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4 AC-link allows a maximum of three codecs to be connected. Figure 8-5 shows a three-codec topology of the AC-link for the ICH4.

**Figure 8-5. Intel® ICH4 AC '97 — Codec Connection**




**NOTE:** If a modem codec is configured as the primary AC-link Codec, there should not be any Audio Codecs residing on the AC-link. The primary codec must be connected to AC_SDIN2 if also routing to CNR. If no CNR exists on the platform, the primary codec may be connected to AC_SDIN0 (see the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*).

Using the assumed 4-layer stack-up, the AC '97 interface can be routed using 5 mil traces with 5-mil spacing between the traces. Maximum length between ICH4 to down CODEC is 14 inches. Maximum length between ICH4 to CNR is 14 inches. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 6 inches for the AC-link. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$.

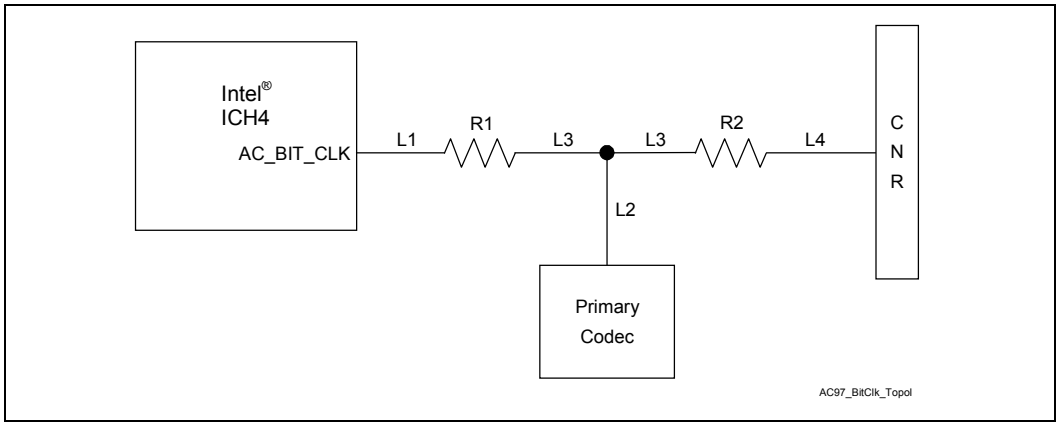
Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH4), and to any other codec present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK directly off the CK408 14.31818 MHz clock is not supported.**

The ICH4 supports wake on ring from S1–S5 via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4 has weak pull-downs/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off, or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT will be driven by the codec and ICH4 respectively. However, AC_SDIN0, AC_SDIN1 and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

### Figure 8-6. Intel® ICH4 AC '97 — AC_BIT_CLK Topology



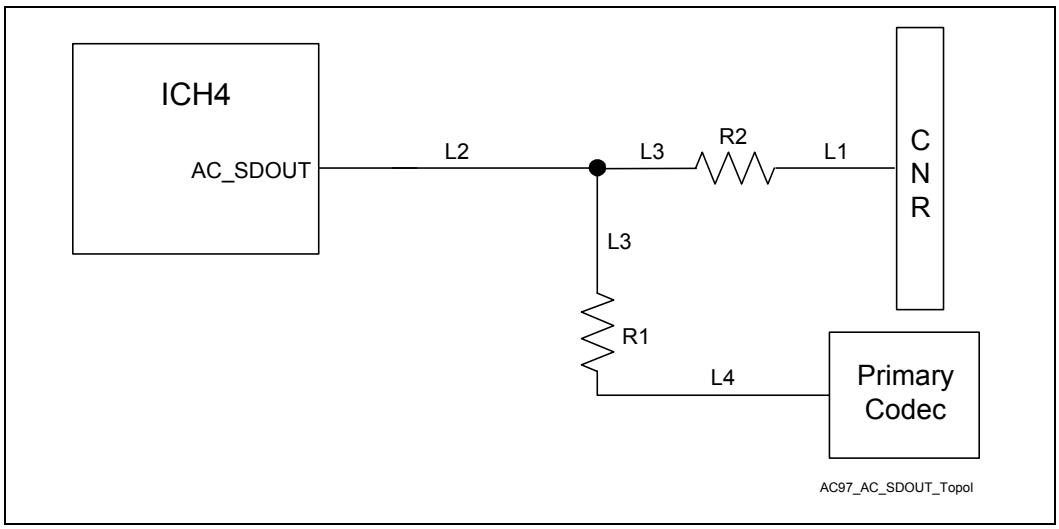

### Table 8-2. AC '97 AC_BIT_CLK Clock Routing Summary

| Trace Impedance | AC '97 Routing Requirements | Maximum Trace Length | Series Termination Resistance | AC_BIT_ CLK Signal Length Matching |
|---|---|---|---|---|
| 51Ω to 69 Ω, 60 Ω Target | 5 on 5 | L1 = (1 to 8) – L3 inches<br>L2 = (0.1 to 6) inches<br>L3 = (0.1 to 0.4) inches<br>L4 = (1 to 6) – L3 inches | R1 = 33 Ω - 47Ω<br>R2 = Optional 0 Ω resistor for debug purposes | N/A |

**NOTES:**

1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec

### Figure 8-7. Intel® ICH4 AC '97 — AC_SDOUT/AC_SYNC Topology

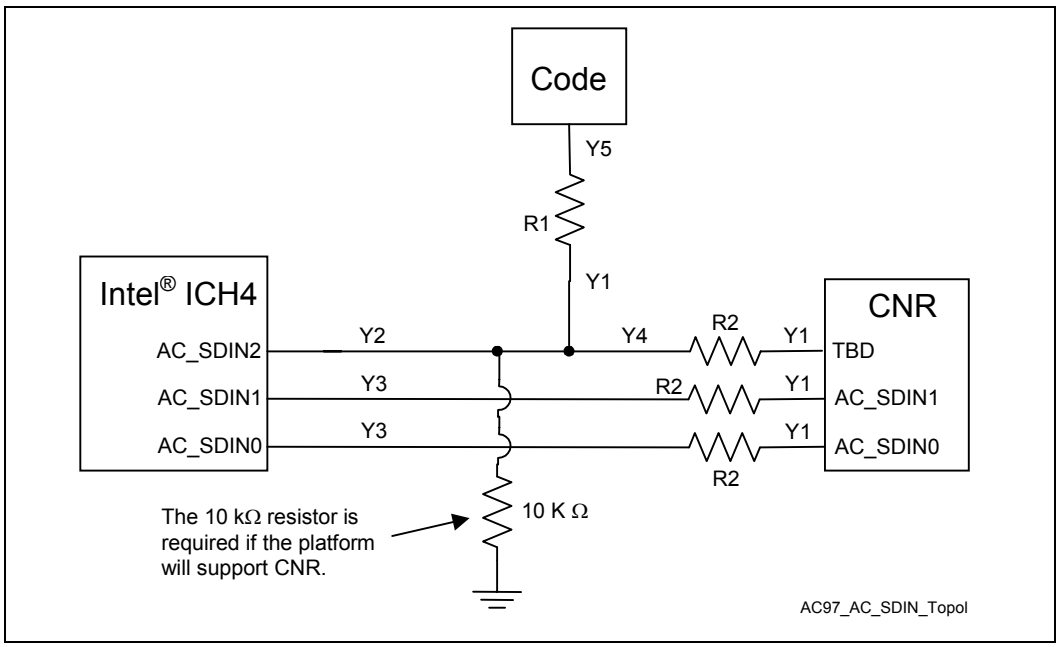



### Table 8-3. AC '97 AC_SDOUT/AC_SYNC Routing Summary

| Trace Impedance | AC '97 Routing Requirements | Maximum Trace Length | Series Termination Resistance | AC_SDOUT/ AC_SYNC Signal Length Matching |
|---|---|---|---|---|
| 51Ω to 69Ω, 60 Ω Target | 5 on 5 | L1 = (1 to 6) – L3 inches<br>L2 = (1 to 8) inches<br>L3 = (0.1 to 0.4) inches<br>L4 = (0.1 to 6) – L3 inches | R1 = 33 Ω – 47 Ω<br>R2 = R1 if the CNR card that will be used with the platform does not have a series termination resistor on the card.<br>Otherwise, R2 = 0 Ω | N/A |

**NOTES:**
1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec

### Figure 8-8. Intel® ICH4 AC '97 — AC_SDIN Topology




### Table 8-4. AC '97 AC_SDIN Routing Summary

| Trace Impedance | AC '97 Routing Requirements | Maximum Trace Length | Series Termination Resistance | AC_SDIN Signal Length Matching |
|---|---|---|---|---|
| 50 Ω to 69 Ω, 60 Ω Target | 5 on 5 | Y1 = (0.1 to 0.4) inches<br>Y2 = (1 to 8) – Y1 inches<br>Y3 = (1 to 14) – Y1 inches<br>Y4 = (1 to 6) – Y1 inches<br>Y5 = (0.1 to 6) – Y1 inches | R1 = 33 Ω – 47 Ω<br>R2 = R1 if the CNR card that will be used with the platform does not have a series termination resistor on the card.<br>Otherwise, R2 = 0 Ω | N/A |

**NOTES:**
1. Simulations were performed using Analog Device's Codec (AD1885) and the Cirrus Logic's Codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1 is best for the Sigmatel 9750 codec

### 8.2.1 AC ’97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes, from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inch to 0.5 inch wide) where the analog/isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inch wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

## 8.2.2 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH4 platform using AC ’97. These design guidelines have been developed to ensure maximum flexibility for board designers, while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH4 platform.

- Active Components such as FET switches, buffers or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.
- The ICH4 supports wake-on-ring from S1-S5 states via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pull-downs will prevent the inputs from floating, so external resistors are not required.
- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

### 8.2.2.1 Valid Codec Configurations

**Table 8-5. Codec Configurations**

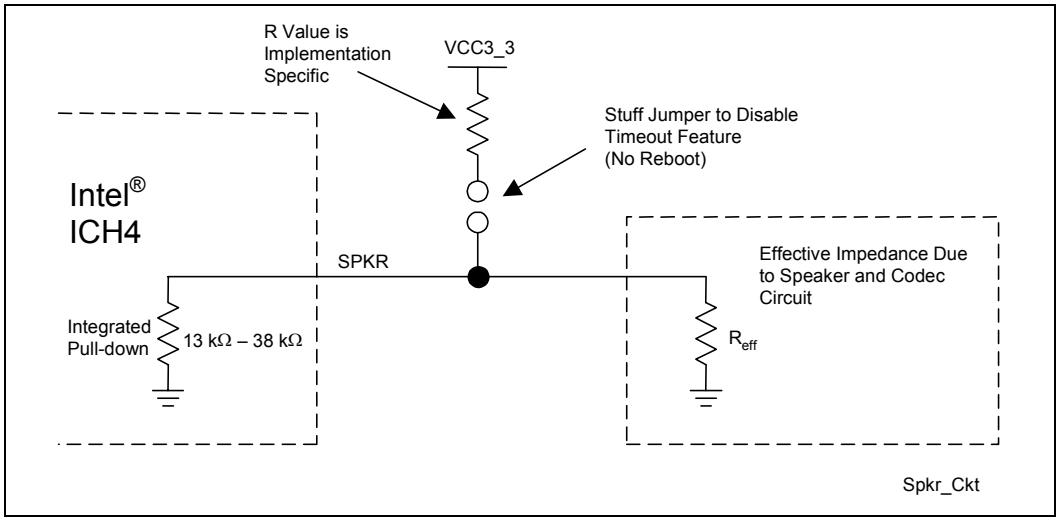
| Option | Primary Codec | Secondary Codec | Tertiary Codec |
|---|---|---|---|
| 1 | Audio | Audio | Audio |
| 2 | Audio | Audio | Modem |
| 3 | Audio | Audio | Audio / Modem |
| 4 | Audio | Modem | Audio |
| 5 | Audio | Audio / Modem | Audio |
| 6 | Audio / Modem | Audio | Audio |

**NOTES:**
1. For power management reasons, codec power management registers are in audio space. As a result, if there is an audio codec in the system, it must be Primary.
2. There cannot be two modems in a system because there is only one set of modem DMA channels
3. The ICH4 supports a modem codec on any of the AC_SDIN lines; however, the Modem Codec ID must be either 00 or 01.

## 8.2.3 SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 8-9). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down ($R_{eff}$), and the ICH4 integrated pull-down resistor will be read as logic high (0.5 VCC3_3 to VCC3_3 + 0.5 V).

**Figure 8-9. Example Speaker Circuit**



## 8.3 CNR

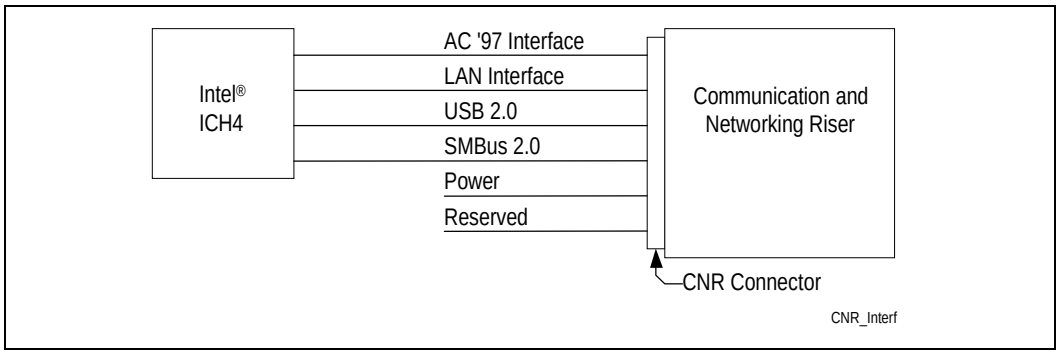
The Communication and Networking Riser (CNR) Specification defines a hardware scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. For more information on the specification, refer to the following document:

- *Communication Network Riser Specification Revision 1.2*
  Available at http://www.intel.com/labs/media/audio/#cnr

The CNR interface supports multi-channel audio, V.90 analog modem, phone-line based networking, 10/100 Ethernet based networking, SMBus Interface Power Management Revision 1.1, and USB 2.0. The CNR specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot; therefore, the system designer will not sacrifice a PCI slot if they decide not to include a CNR in a particular build.

Figure 8-10 indicates the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN connection (PLC) can either be an 82562ET/EZ or 82562EM/EX component. Refer to the CNR specification for additional information.

**Figure 8-10. CNR Interface**



## 8.3.1 AC ’97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Refer to the *Communication Network Riser Specification, Revision 1.2* for Intel’s recommended codec configurations

**Table 8-6. Signal Descriptions**

| Signal | Description |
|---|---|
| CDC_DN_ENAB# | When low, this signal indicates that the codec on the motherboard is enabled and primary on the AC ’97 Interface. When high, the signal indicates that the motherboard codec(s) must be removed from the AC ’97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC ’97 Interface. |
| AC_RST# | Reset signal from the AC ’97 Digital Controller (ICH4). |
| AC_SDIN*n* | AC ’97 serial data from an AC ’97-compaible t codec to an AC ’97-compatible controller (i.e., the ICH4). |

### 8.3.1.1 CNR 1.2 AC ’97 Disable and Demotion Rules for the Motherboard

The following are the CNR1.1/1.2 AC ’97 disable and demotion rules for the motherboard.

- All AC ’97 Revision 2.2 *non-chaining* codecs on the motherboard **must** always disable themselves when the CDC_DWN_ENAB# signal is in a high state.
- A motherboard AC ’97 codec **must** never change its address or AC_SDIN line used, regardless of the state of the CDC_DWN_ENAB# signal.
- A motherboard containing an AC ’97 controller supporting three AC ’97 codecs the AC ’97 Revision 2.2 or AC ’97 Revision 2.3 codec, on the motherboard, **must** be connected to the AC_SDIN2 signal of the CNR connector.
- A motherboard should not contain any more than a single AC ’97 codec.

These rules allow for forward and backward compatibility between CNR Version 1.1/1.2 cards. For more information on chaining, consult the *Communication Network Riser Specification, Revision 1.2*.

**Figure 8-11. Motherboard AC '97 CNR Implementation with a Single Codec Down On Board**

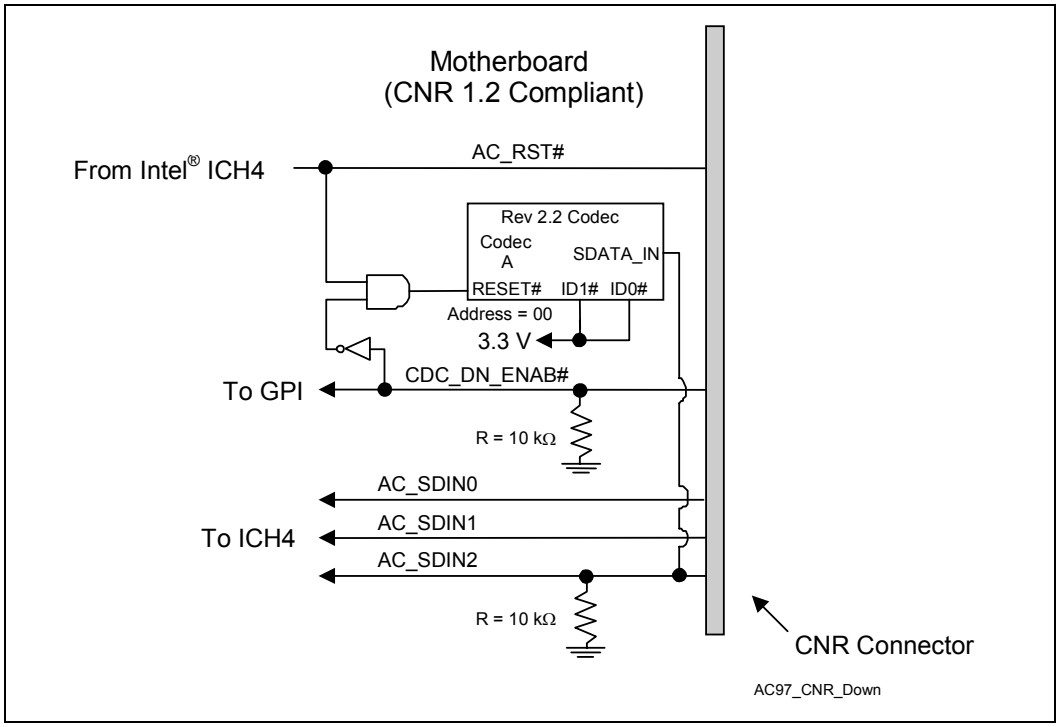
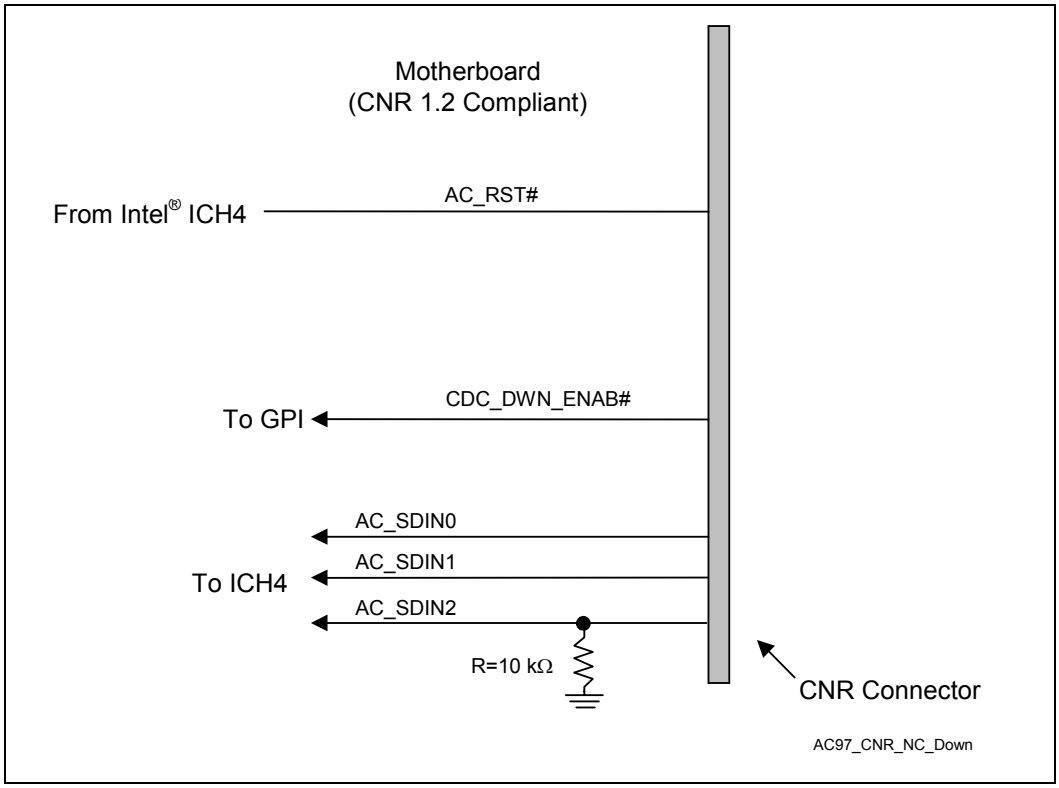



**Figure 8-12. Motherboard AC '97 CNR Implementation with No Codec Down On Board**



## 8.3.2 CNR Routing Summary

Table 8-7 is a summary of the various interfaces routing requirements to the CNR Riser.

**Table 8-7. CNR Routing Summary**

| Trace Impedance | CNR Routing Requirements | Maximum Trace Length to CNR Connector | Signal Length Matching | Signal Referencing |
|---|---|---|---|---|
| 77 Ω to 103 Ω Differential, 90 Ω Differential Target | USB (7.5 on 7.5)<br>Data pair must be at least 20 mils from nearest neighbor | 10 inches | No more than 150-mils trace mismatch | Ground |
| 51 Ω to 69 Ω, 60 Ω Target | AC '97 (5 on 5) | AC_BIT_CLK (See **Error! Reference source not found.**)<br>AC_SDOUT (See **Error! Reference source not found.**)<br>AC_SDIN (See **Error! Reference source not found.**) | N/A | Ground |
| 51 Ω to 69 Ω, 60 Ω Target | LAN (5 on 10) | 9.5 inches (See Table 8-19) | Equal to or up to 500 mils shorter than the LAN_CLK trace | Ground |

# 8.4 USB 2.0

## 8.4.1 Layout Guidelines

### 8.4.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. The USB 2.0 validation efforts focused on a four-layer motherboard where the first layer is a signal layer, the second plane is power, the third plane is ground and the fourth is a signal layer. This results in placing most of the routing on the fourth plane closest to the ground plane, and allowing a higher component density on the first plane.

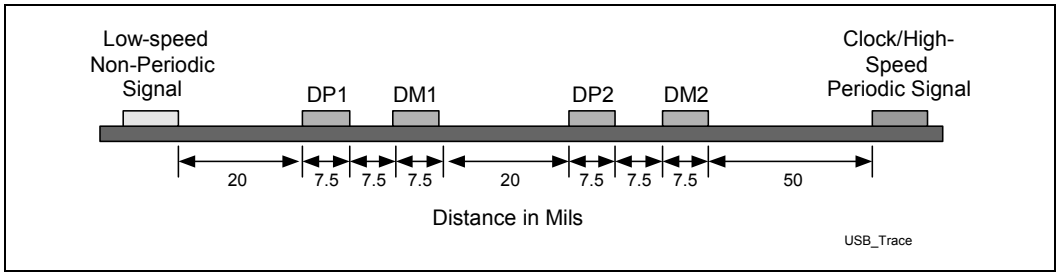
- Place the ICH4 and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, or power connectors).
- USB 2.0 signals should be ***ground referenced***
- Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.
- When it becomes necessary to turn 90 degree, use two 45-degree turns or an arc instead of making a single 90-degree turn. This reduces reflections on the signal by minimizing impedance discontinuities. (See Figure 8-41).
- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices, or IC's that use and/or duplicate clocks.
- Stubs on high speed USB signals should be avoided, as stubs will cause signal reflection and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.
- Route all traces over continuous planes (VCC or GND) with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 8.4.2.
- Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
- Keep USB 2.0 signals clear of the core logic set. High current transients are produced during internal state transitions, which can be very difficult to filter out.
- Follow the 20*h thumb rule by keeping traces at least 20* (height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

### 8.4.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. Figure 8-13 shows the recommended trace spacing.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. Deviations normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used. For the board stack-up parameters referred to in Section 0,
  7.5-mil traces with 7.5-mil spacing results in approximately 90 Ω differential trace impedance.
- Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

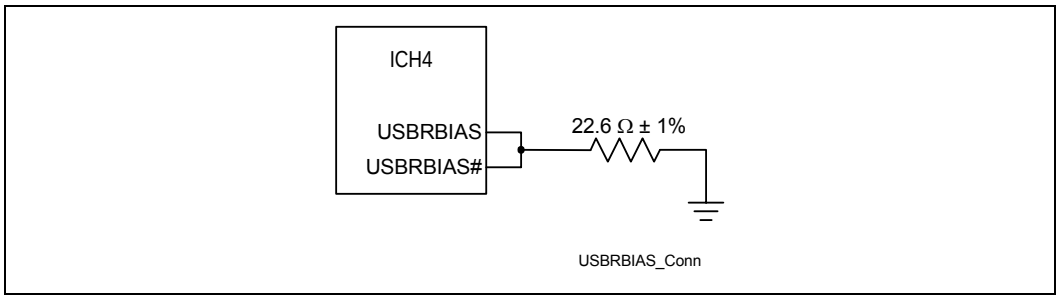
**Figure 8-13. Recommended USB Trace Spacing**




### 8.4.1.3 USBRBIAS Connection

The USBRBIAS pin and the USBRBIAS# pin can be shorted and routed 5 on 5 to one end of a 22.6 Ω ± 1% resistor to ground. Place the resistor within 500 mils of the ICH4 and avoid routing next to clock pins.

**Figure 8-14. USBRBIAS Connection**



### Table 8-8. USBRBIAS/USBRBIAS# Routing Summary

| Trace Impedance | USBRBIAS/ USBRBIAS# Routing Requirements | Maximum Trace Length | Signal Length Matching | Signal Referencing |
|---|---|---|---|---|
| 51 Ω to 69 Ω, 60 Ω Target | 5 on 5 | 500 mils | N/A | N/A |

## 8.4.1.4 USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 8.4.4 for common-mode choke details.

## 8.4.1.5 USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should be no greater that 150 mils.

## 8.4.1.6 USB 2.0 Trace Length Guidelines

Use the following trace length guidelines.

### Table 8-9. USB 2.0 Trace Length Guidelines (with Common-Mode Choke)

| Trace Imped. | USB 2.0 Routing Req. | Topology | Signal Ref | Signal Matching | Motherboard Trace Length | Card Trace Length | Maximum Total Length |
|---|---|---|---|---|---|---|---|
| 77Ω to 103 Ω differential, 90 Ω Differential Target | 7.5 on 7.5 | Back Panel | Ground | The max mismatch between data pairs should not be greater than 150 mils | 17 inches | N/A | 17 inches |
| | | CNR | | | 8 inches | 6 inches | 14 inches |
| | | Front Panel | | | **Cable Length** | **Mother board Trace Length** | **Daughter Card Trace Length** | **Max. Total Length** |
| | | | | | 9 | 6 | 2 | 17 |
| | | | | | 10.5 | 5 | 2 | 17.5 |
| | | | | | 12 | 4 | 2 | 18 |
| | | | | | 13.5 | 3 | 2 | 18.5 |
| | | | | | 15 | 2 | 2 | 19 |

**NOTES:**
1. These lengths are based upon simulation results and may be updated in the future.
2. All lengths are based upon using a common-mode choke (see Section 8.4.4.1 for details on common-mode choke).
3. Numbers in this table are based on the following simulation assumptions:
   CNR configuration: max 6 inches trace on add-on card.
4. An Approximate 1:1 trade-off can be assumed from Motherboard Trace Length vs. Daughter card Trace Length (e.g., trade 1 inch of Daughter card for 1 inch of Motherboard Trace Lengths).
5. Routing guidelines are based on the stack-up assumptions in Section 0
6. Numbers in this table are based on the following simulation assumptions
   a. Trace length on front panel connector card assumed a max of 2 inches.
   b. USB twisted-pair shielded cable as specified in USB 2.0 specification was used.
7. For front panel solutions, signal matching is considered from the ICH4 to the front panel header.

## 8.4.2 Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cutouts.

### 8.4.2.1 VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane.

- Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the full-speed single-ended zero is common mode).
- Avoid routing of USB 2.0 signals 25-mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching caps can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 µF or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates VCC5 and VCC3_3 planes should have a stitching cap placed near any high-speed signal crossing. One side of the cap should tie to VCC5 and the other side should tie to VCC3_3. Stitching caps provide a high-frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

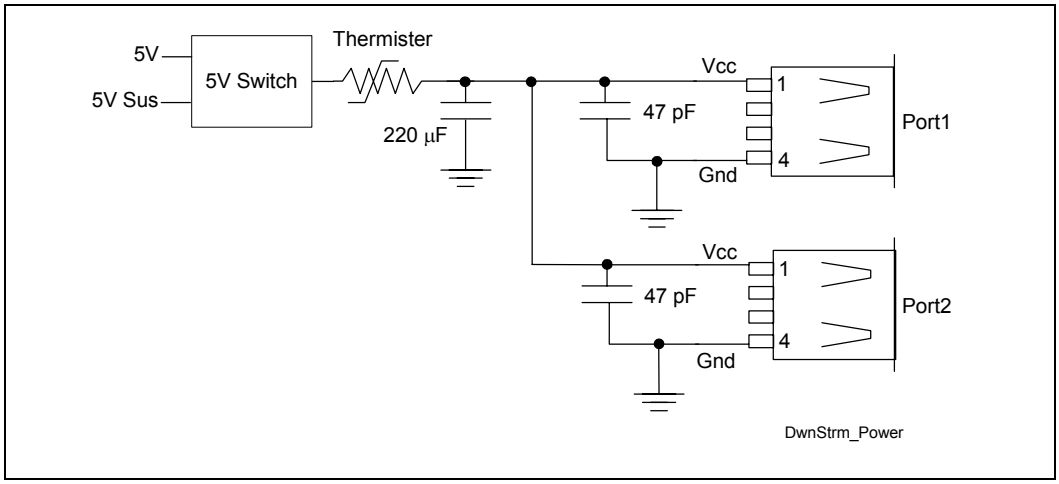
### 8.4.2.2 GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

## 8.4.3 USB Power Line Layout Topologies

The following is a suggested topology for power distribution of VBUS to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop) and dynamic detach flyback protection. These two different situations require both bulk capacitance (droop) and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port and the power-carrying traces should be as wide as possible, preferably, a plane. A good "rule-of-thumb" is to make the power-carrying traces wide enough that the system fuse will blow on an over current event. If the system fuse is rated at 1amps then the power-carrying traces should be wide enough to carry at least 1.5 amps.

**Figure 8-15. Good Downstream Power Connection**



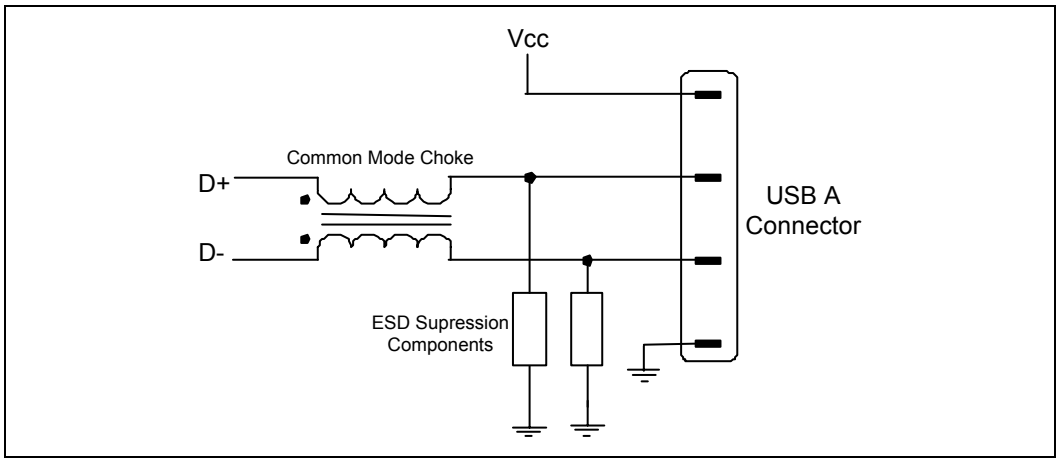
## 8.4.4 EMI Considerations

The following guidelines apply to the selection and placement of common chokes and ESD protection devices.

### 8.4.4.1 Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design should include a common mode choke footprint to provide a stuffing option **in the event** the choke is needed to pass EMI testing. Figure 8-16 shows the schematic of a typical common mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins. In systems that route USB to a front panel header the choke should be placed on the front panel card.

**Figure 8-16. A Common-Mode Choke**




Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases, the distortion will increase, so the effects of the common mode choke on full-speed and high-speed signal quality should be tested. Common Mode Chokes with a target impedance of 80 Ω to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's requirements is a two-step process.

- A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen and the frequency and strength of the noise present on the USB traces that you are trying to suppress.
- Once you have a part that gives passing EMI results the second step is to test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for Low-speed, Full-speed and High-speed USB operation.

## 8.4.5 ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 due to the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common mode choke and the USB connector data pins as shown in Figure 8-16. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, it is recommended to include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

## 8.4.6 Front Panel Solutions

### 8.4.6.1 Internal USB Cables

The front panel internal cable solution chosen must meet all the requirements of Chapter 6 of the *USB 2.0 Specification* for high-/full-speed cabling for each port with the exceptions described in Cable Option 2.

#### 8.4.6.1.1 Internal Cable Option 1

Use standard High-Speed/Full-Speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *USB 2.0 Specification*. Recommended motherboard mating connector pin-out is covered in detail later in this document.

#### 8.4.6.1.2 Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of *the USB 2.0 Specification* with the following additions/exceptions.

- They can share a common jacket, shield and drain wire.
- Two ports with signal pairs that share a common jacket may combine VBUS and ground wires into a single wire provided the following conditions are met:
  - The bypass capacitance required by Section 7.2.4.1 of the USB 2.0 Specification is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughter card). Refer to the front panel daughter card referenced later for details.
  - Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the USB 2.0 Specification that has ≤ ½ the resistance of either of the two wires being combined. The data is provided for reference in Table 8-10.

**Table 8-10. Conductor Resistance**

| American Wire Gauge (AWG) | Ohm (Ω) / 100 Meters Maximum |
|---|---|
| 28 | 23.20 |
| 26 | 14.60 |
| 24 | 9.09 |
| 22 | 5.74 |
| 20 | 3.58 |

**Example**: 2 – 24 gauge (AWG) power or ground wires can be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the *USB 2.0 Specification* at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port can usually meet droop requirements by providing adequate capacitance near the motherboard mating connector because droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients will be seen/dampened by the capacitance at the motherboard mating connector before they can cause problems with the adjacent port sharing the same cable. See section 7.2.2 and 7.2.4.1 of the *USB 2.0 Specification* for more details.

Cables that contain more than two signal pairs are not recommended due to unpredictable impedance characteristics.

### 8.4.6.2 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure signal quality is not adversely affected due to a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the *USB 2.0 Specification*.

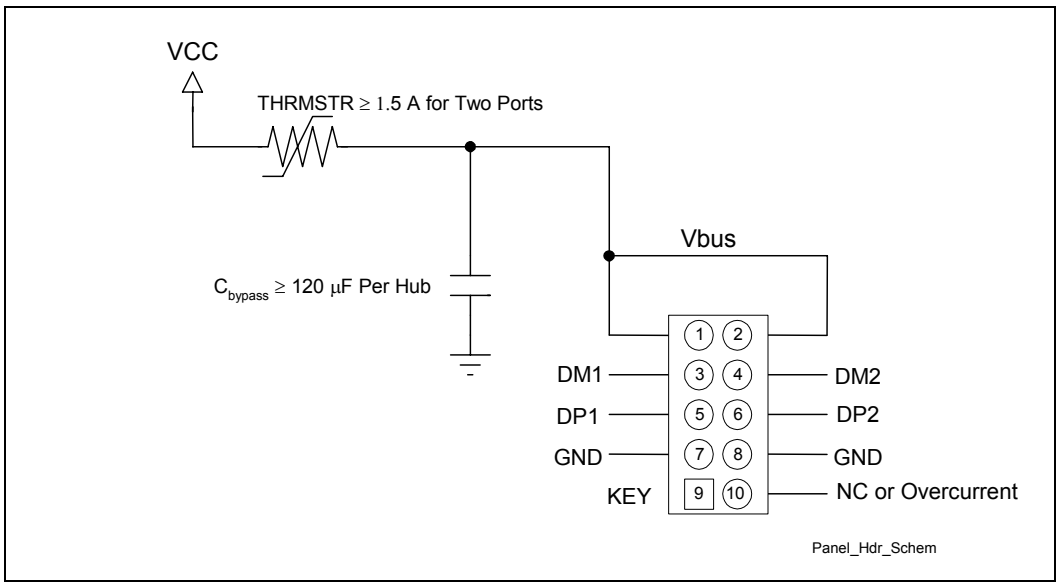
#### 8.4.6.2.1 Pinout

A ten pin, 0.1-inch pitch stake pin assembly is recommended with the pinout listed in Table 8-11 and in the following schematic.

**Table 8-11. Front Panel Header Pinout**

| Pin | Description |
|---|---|
| 1 | VCC |
| 2 | VCC |
| 3 | Dm1 |
| 4 | Dm2 |
| 5 | Dp1 |
| 6 | Dp2 |
| 7 | Gnd |
| 8 | Gnd |
| 9 | key |
| 10 | No connect or over-current sense |

**Figure 8-17. Front Panel Header Schematic**




It is **highly** recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage.

- This protects the motherboard from damage in the case where an un-fused front panel cable solution is used.
- It also provides protection from damage if an un-keyed cable is inadvertently plugged onto the front panel USB connector.
- It provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between VBUS and ground.

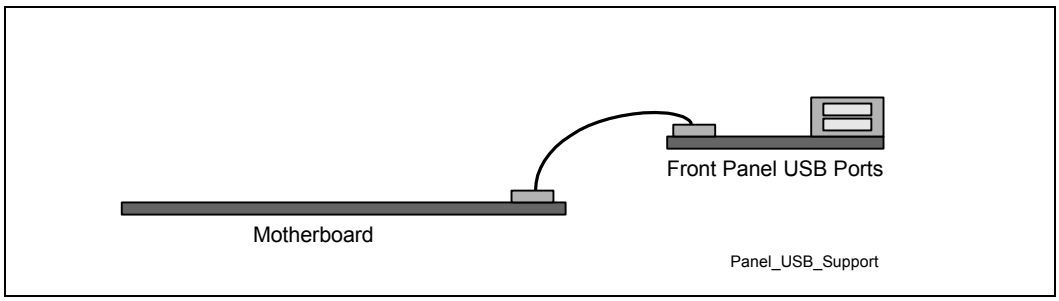
#### 8.4.6.2.2 Routing Considerations

- Traces or surface shapes from VCC to the thermistor, to Cbypass and to the connector power and ground pins should be at least 50-mils wide to ensure adequate current carrying capability.
- There should be double vias on power and ground nets and the trace lengths should be kept as short as possible.

### 8.4.6.3 Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 8-18 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card.

Figure 8-18. Motherboard Front Panel USB Support




***Note:*** The terms “connector card” and “daughter card” are used interchangeably.

When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there aren’t duplicate EMI/ESD/thermistor components placed on the motherboard, as this will usually cause drop/droop and signal quality degradation or failure.

#### 8.4.6.3.1 Front Panel Daughter Card Design Guidelines

- Place the VBUS bypass capacitance, Common Mode Choke, and ESD suppression components on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing and impedance control guidelines as specified for motherboards.
- Minimize the trace length on the front panel connector card. Less than 2-inch trace length is recommended.
- Use the same mating connector pin-out as outlined for the motherboard in Section 8.4.6.2.1.
- Use the same routing guidelines as described in Section 8.4.1.
- Trace length guidelines are given in Table 8-9.

## 8.5 I/O APIC Design Recommendation

UP systems not using the IOAPIC Bus should follow these recommendations:

**On the ICH4**

- Tie APICCLK directly to ground
- Tie APICD [1:0] to ground through a 10 kΩ resistor (Separate pull-downs are required if using XOR chain testing.)

**On the processor**

- Consult processor documentation

## 8.5.1 PIRQ Routing Example

Table 8-12 describes how the ICH4 uses the PCI IRQ when the I/O APIC is active.

**Table 8-12. IOAPIC Interrupt Inputs 16 Through 23 Usage**

| No | I/O APIC INTIN PIN | Function in Intel® ICH4 Using the PCI IRQ in IOAPIC |
|---|---|---|
| 1 | I/O APIC INTIN PIN 16 (PIRQA) | USB1 UHCI Controller 1 |
| 2 | I/O APIC INTIN PIN 17 (PIRQB) | AC '97 Audio and Modem; option for SMBus |
| 3 | I/O APIC INTIN PIN 18 (PIRQC) | USB1 UHCI Controller 3; Native IDE |
| 4 | I/O APIC INTIN PIN 19 (PIRQD) | USB1 UHCI Controller 2 |
| 5 | I/O APIC INTIN PIN 20 (PIRQE) | Internal LAN; option for SCI, TCO, MMT 0,1,2 |
| 6 | I/O APIC INTIN PIN 21 (PIRQF) | Option for SCI, TCO, MMT 0,1,2 |
| 7 | I/O APIC INTIN PIN 22 (PIRQG) | Option for SCI, TCO, MMT 0,1,2 |
| 8 | I/O APIC INTIN PIN 23 (PIRQH) | USB2 EHCI Controller, Option for SCI, TCO, MMT 0,1,2 |

Due to different system configurations, IRQ line routing to the PCI slots ("swizzling") should be made to minimize the sharing of interrupts between both internal ICH4 functions and PCI functions. Figure 8-19shows an example of IRQ line routing to the PCI slots (note: it is not necessarily an optimal routing scheme; an optimal scheme depends on individual system PCI IRQ usage).

**Figure 8-19. Example PIRQ Routing**

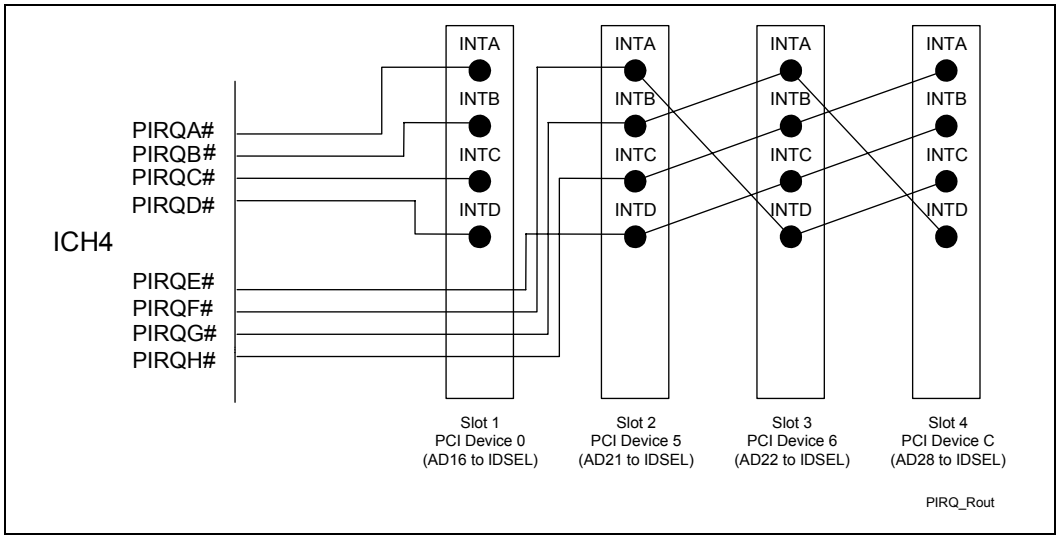



Figure 8-19 is an example. It is up to the board designer to route these signals in a way that will prove the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH4 internal device/functions (but at a higher latency cost).

## 8.6 SMBus 2.0/SMLink Interface

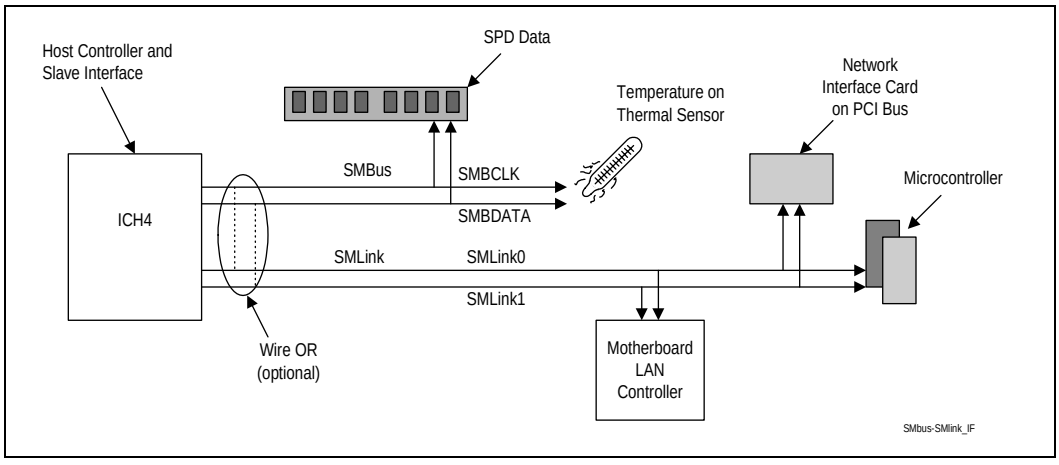
The SMBus interface on the ICH4 uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH4.

The ICH4 incorporates an SMLink interface supporting Alert on LAN*, Alert on LAN2* and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK0 corresponds to an SMBus clock signal and SMLINK1 corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN* functionality, the ICH4 transmits heartbeat and event messages over the interface. When using the 82562EM/82562EX platform LAN connect component, the ICH4 integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2*-enabled LAN Controller (i.e., 82562EM/82562EX 10/100 Mbps platform LAN connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4 SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (such as 82562EM/82562EX 10/100 Mbps platform LAN connect) to access targets on the SMBus as well as the ICH4 Slave interface. Additionally, the ICH4 supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals **must** be tied together externally. This is done by connecting SMLink0 to SMBCLK and SMLink1 to SMBDATA.

**Figure 8-20 SMBUS 2.0/SMLink Interface**




***Note:*** Intel does not support external access of the ICH4 Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH4 SMBus Slave Interface by the ICH4 SMBus Host Controller. Refer to the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet* for full functionality descriptions of the SMLink and SMBus interface.

## 8.6.1 SMBus Architecture and Design Considerations

### SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging because they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in choosing a design are based on:

- Devices that must run in S3
- Amount of VCC_Suspend current available (i.e., minimizing load of VCC_Suspend)
- Device class: High power/Low power. Most designs use primarily high power devices.

### General Design Issues / Notes

Regardless of the architecture used, there are some general considerations.

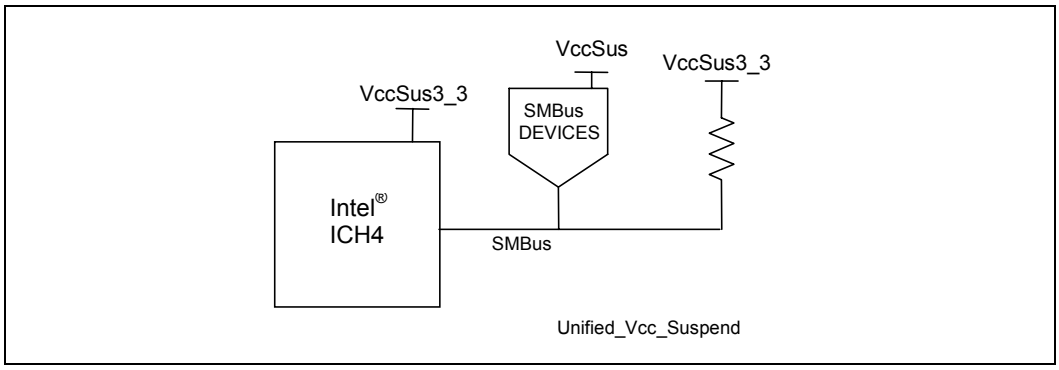
- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor can not be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and fall time specification.
- The maximum bus capacitance that a physical segment can reach is 400 pF.
- The ICH4 does not run SMBus cycles while in S3
- SMBus devices that can operate in S3 must be powered by the VCC_Suspend supply.
- If SMBus is to be connected to PCI, it must be connected to all PCI slots.

### 8.6.1.1 Power Supply Considerations

#### The Unified VCC_ Suspend Architecture

In this design all SMBus devices are powered by the VCC_Suspend supply. Consideration must be made to provide enough VCC_Suspend current while in S3.

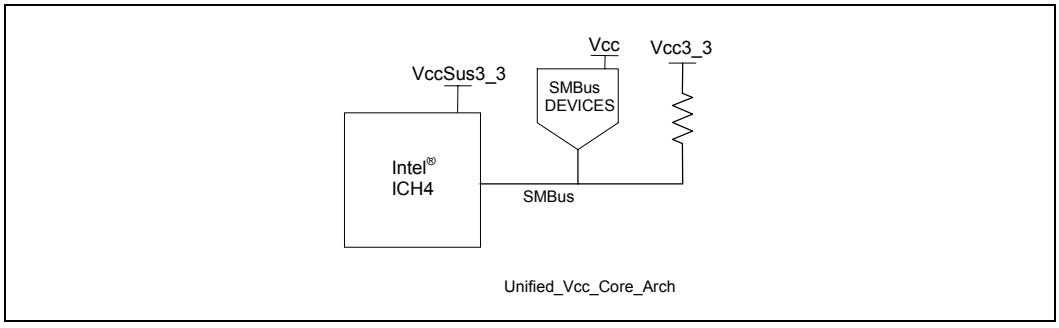
**Figure 8-21. Unified VCC_Suspend Architecture**




#### The Unified VCC_CORE Architecture

In this design, all SMBUS devices are powered by the VCC_CORE supply. This architecture allows none of the devices to operate in S3, but minimizes the load on VCC_Suspend.

**Figure 8-22. Unified VCC_CORE Architecture**

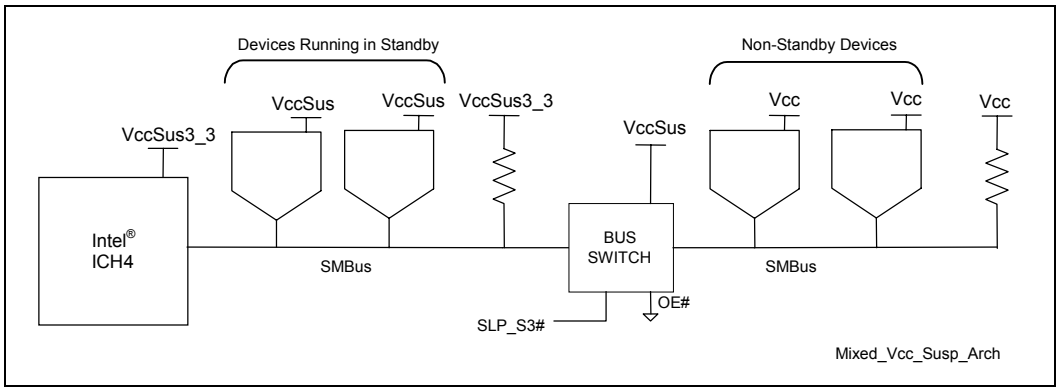



**NOTES:**
1. The SMBus device must be back-drive safe while its supply (Vcore) is off and VCC_Suspend is still powered.
2. In suspended modes where VCC_CORE is OFF & VCC_Suspend is on, the VCC_CORE node will be very near ground. In this case the input leakage of the ICH4 will be approximately 10 uA.

### Mixed Power Supply Architecture

This design allows for SMBus devices to communicate while in S3, yet minimizes VCC_Suspend leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a "bus switch" to isolate the devices powered by the core and suspend supplies. See Figure 8-23.

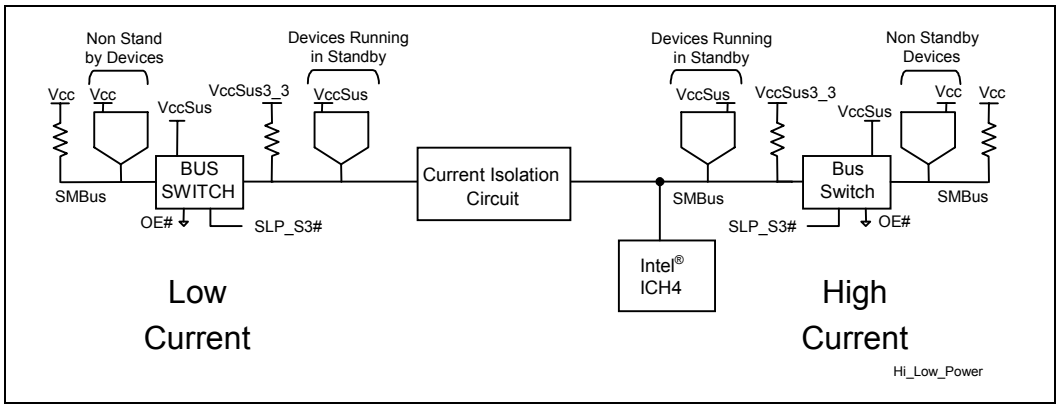
**Figure 8-23. Mixed VCC_Suspend/VCC_CORE Architecture**




## 8.6.1.2 Device Class Considerations

In addition to the power supply considerations described above, system designers should take into consideration the SMBus device class (high power/low power) used on the bus. If the design supports both high- power and low-power devices on the bus, current isolation of high-power segment and low-power segment of the bus is needed as shown in Figure 8-24.

**Figure 8-24. High Power/Low Power Mixed VCC_SUSPEND/VCC_CORE Architecture**



## 8.7 PCI

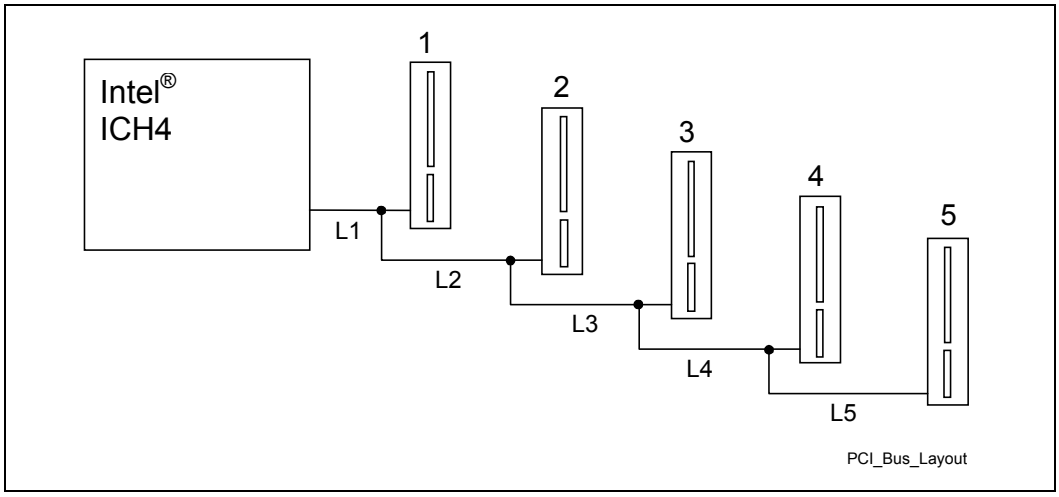
The ICH4 provides a PCI Bus interface that is compliant with the PCI Local Bus Specification, Revision 2.2. The implementation is optimized for high-performance data streaming when the ICH4 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification Revision 2.2*.

The ICH4 supports six PCI Bus masters (excluding the ICH4), by providing six REQ#/GNT# pairs. In addition, the ICH4 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

### 8.7.1 PCI Routing Summary

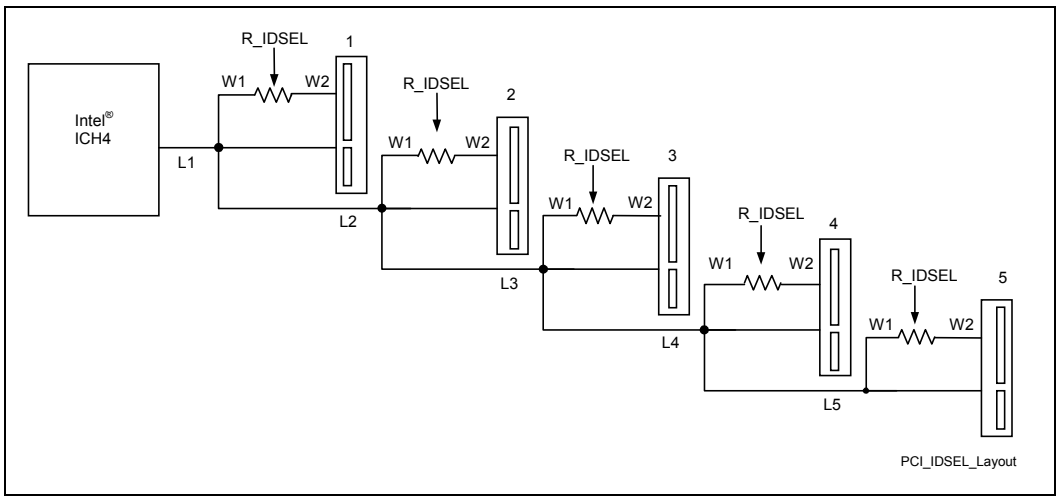
The following represents a summary of the routing guidelines for the PCI Slots. Simulations assume that PCI cards follow the *PCI Local Bus Specification, Revision 2.2* trace length guidelines.

**Figure 8-25. PCI Bus Layout Example**




***Note:*** Note that if a CNR connector is placed on the platform, it will share a slot space with one of the PCI slots; however, it will not take away from the slot functionality unless the CNR slot is occupied by a CNR card.

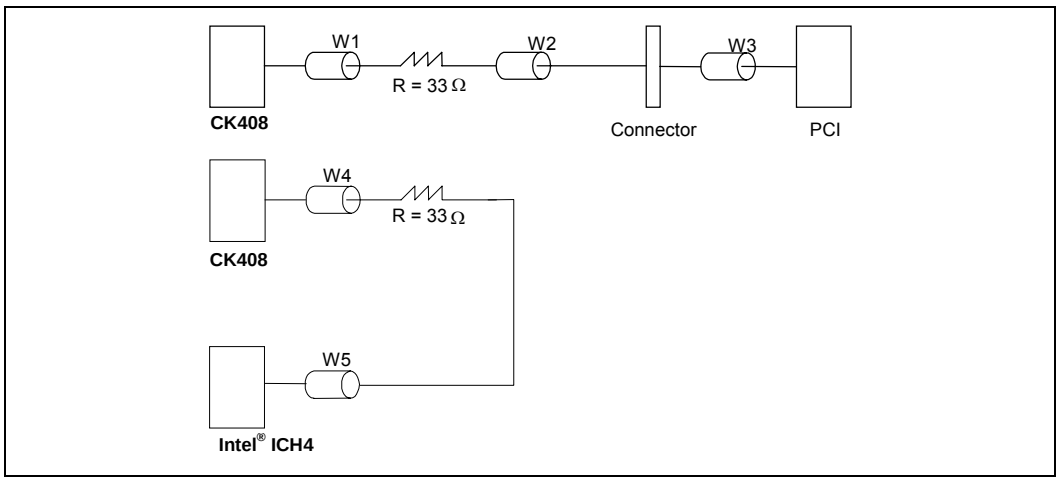
### Figure 8-26. PCI Bus Layout Example with IDSEL




### Table 8-13. PCI Data Signals Routing Summary

| PCI Routing Req. | Trace Impedance | Topology | Maximum Trace Length (Inches) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | L1 | L2 | L3 | L4 | L5 | L6 |
| 5 of 7 | 47Ω to 69 Ω<br>60 Ω target | 2 Slots<br>W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω | 5 to 10 | 1.5 | N/A | N/A | N/A | N/A |
| | | 2 Slots with 1 down device<br>W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω | 5 to 10 | 1.0 | 3.0 | N/A | N/A | N/A |
| | | 3 Slots<br>W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω | 5 to 10 | 1.5 | 1.5 | N/A | N/A | N/A |
| | | 3 Slots with 1 down device<br>W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω | 5 to 10 | 1.0 | 1.0 | 3.0 | N/A | N/A |
| | | 4 Slots<br>W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω | 5 to 10 | 1.0 | 1.0 | 1.0 | N/A | N/A |
| | | 4 Slots with 1 down device<br>W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω | 5 to 10 | 1.0 | 1.0 | 1.0 | 3.0 | N/A |
| | 51Ω to 69 Ω<br>60 Ω target | 5 Slots<br>W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω | 5 to 8 | 1.0 | 1.0 | 1.0 | 1.0 | N/A |
| | | 6 Slots<br>W1=W2= 0.5 inch, R_IDSEL = 300 to 900 Ω | 5 to 7 | 1.0 | 1.0 | 1.0 | 1.0 | 1.0 |

### Figure 8-27. PCI Clock Layout Example




**NOTE:** Clocks should be routed first.

### Table 8-14. PCI Clock Signals Routing Summary

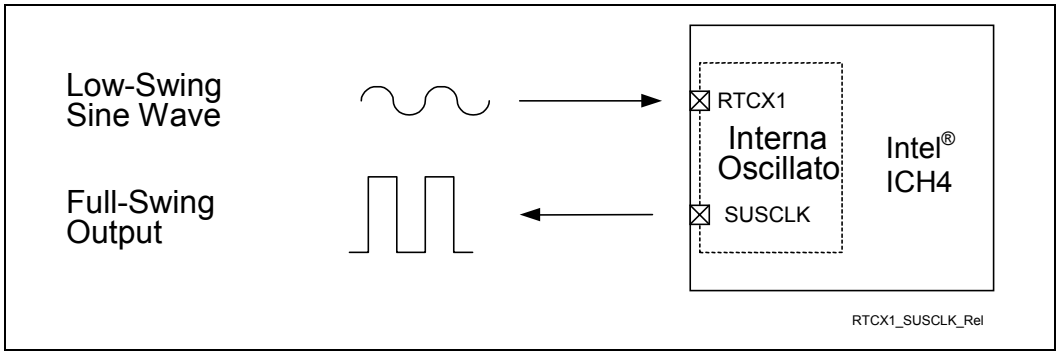
| Trace Impedance | PCI Routing Requirements | Topology | Maximum Trace Length | | | | |
|---|---|---|---|---|---|---|---|
| | | | W1 | W2 | W3 | W4 | W5 |
| 51 Ω to 69 Ω, 60 Ω Target | 5 on 7 | 2 – 5 Slots | 0.5” | W5 – 4.5” | 2.5 inches (Shown as a reference only) | 0.5” | Can be as long as needed (as long as W2 is scaled accordingly |

## 8.8 RTC

The ICH4 contains a real time clock (RTC) with 256 bytes of battery backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4 uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4, the RTCX1 signal is amplified to drive internal logic as well as generate a free running full swing clock output for system use. This output ball of the ICH4 is called SUSCLK. This is shown in Figure 8-28.

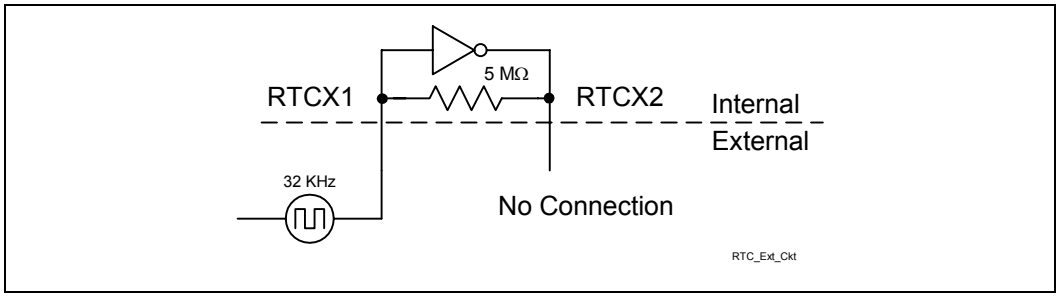
**Figure 8-28. RTCX1 and SUSCLK Relationship in the Intel® ICH4**




For further information on the RTC, consult Application Note AP-728 *"ICH/ICH2/ICH2M/ICH3S/ICH3M Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions"*. This application note is valid for ICH4.

Even if the ICH4 internal RTC is not used, it's still necessary to supply a clock input to RTCX1 of the ICH4 because other signals are gated off that clock in suspend modes. However, in this case, the frequency accuracy (32.768 kHz) of the clock inputs is not critical. A crystal can be used or a single clock input can be driven into RTCX1with RTCX2 left as no connect. Figure 8-29 illustrates the connection. This is not a validated feature on ICH4. Note that the peak-to-peak swing on RTCX1 cannot exceed 1.0 V.

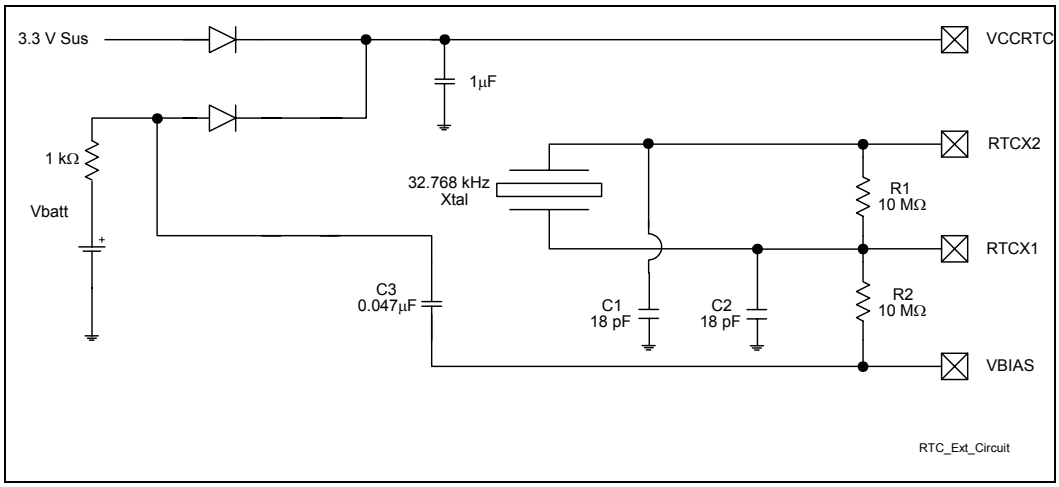
**Figure 8-29. External Circuitry for the Intel® ICH4 Where the Internal RTC Is Not Used**



## 8.8.1 RTC Crystal

The ICH4 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 8-30 shows the external circuitry that comprises the oscillator of the ICH4 RTC.

**Figure 8-30. External Circuitry for the Intel® ICH4 RTC**




**NOTES:**

1. The exact capacitor value must be based on what the crystal maker recommends. (Typical values for C1 and C2 are 18 pF – based on crystal load 12.5 pF).
2. Reference designators are arbitrarily assigned.
3. 3.3 V Sus is active whenever the system is plugged in.
4. Vbatt is voltage provided by the battery.
5. VCCRTC, RTCX2, RTCX1, and VBIAS are ICH4 pins.
6. VCCRTC: Power for RTC Well.
7. RTCX2: Crystal Input 2 – Connected to the 32.768 kHz crystal.
8. RTCX1: Crystal Input 1 – Connected to the 32.768 kHz crystal.
9. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.
10. VSS: Ground.
11. Diodes should be Schottkey diodes.

**Table 8-15. RTC Routing Summary**

| Trace Impedance | RTC Routing Requirements | Maximum Trace Length To Crystal | Signal Length Matching | R1, R2, C1, and C2 Tolerances | Signal Referencing |
|---|---|---|---|---|---|
| 45 Ω to 69 Ω, 60 Ω Target | 5 mil trace width (results in ~2pF per inch) | 1 inch | NA | R1 = R2 = 10 MΩ ± 5%<br>C1 = C2 = (NPO class)<br>See Section 8.8.2 for calculating a specific capacitance value for C1 and C2 | Ground |

## 8.8.2 External Capacitors

To maintain the RTC accuracy, the external capacitor $C_3$ must be 0.047 µF and capacitor values $C_1$ and $C_2$ should be chosen to provide the manufacturer's specified load capacitance ($C_{load}$) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{load} = [(C_1 + C_{in1} + C_{trace1})*(C_2 + C_{in2} + C_{trace2})]/[(C_1 + C_{in1} + C_{trace1} + C_2 + C_{in2} + C_{trace2})] + C_{parasitic}$$

Where:

- $C_{load}$ = Crystal's load capacitance. This value can be obtained from Crystal's specification.
- $C_{in1}$, $C_{in2}$ = input capacitances at RTCX1, RTCX2 balls of the ICH4. These values can be obtained in the ICH4 data sheet.
- $C_{trace1}$, $C_{trace2}$ = Trace length capacitances measured from Crystal terminals to RTCX1, RTCX2 balls. These values depend on the characteristics of board material, the width of signal traces and the length of the traces. Typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to:

  $$C_{trace} = \text{trace length} * 2\text{pF/inch}$$

- $C_{parasitic}$ = Crystal's parasitic capacitance. This capacitance is created by the existence of 2 electrode plates and the dielectric constant of the crystal blank inside the Crystal part. Refer to the crystal's specification to obtain this value.

Ideally, $C_1$, $C_2$ can be chosen such that $C_1 = C_2$. Using the equation of $C_{load}$ above, the value of $C_1$, $C_2$ can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, $C_2$ can be chosen such that $C_2 > C_1$. Then $C_1$ can be trimmed to obtain the 32.768 kHz.

In certain conditions, both $C_1$, $C_2$ values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When $C_1$, $C_2$ values are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example will illustrates the use of the practical values $C_1$, $C_2$ in the case that theoretical values can not guarantee the accuracy of the RTC in low temperature condition:

### Example

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH4, the calculated values of $C_1 = C_2$ is 10 pF at room temperature (25 °C) to yield a 32.768 kHz oscillation.

At 0 °C the frequency stability of crystal gives –23 ppm (assumed that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of $C_1$, $C_2$ are chosen to be 6.8 pF instead of 10 pF, this will make the RTC oscillate at higher frequency at room temperature (+23 ppm) but this configuration of $C_1$ / $C_2$ makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C1 and 2 is the **practical value**.

Note that the temperature dependency of crystal frequency is parabolic relationship (ppm / degree square). The effect of changing crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature).

## 8.8.3 RTC Layout Considerations

Because the RTC circuit is very sensitive and requires high accurate oscillation, reasonable care must be taken during layout and routing RTC circuit. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. ICH4 requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn ball). Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances. Trace capacitance depends on the trace width and dielectric constant of board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.
- Trace signal coupling must be importantly reduced, by avoiding routing of adjacent PCI signals close to RTCX1 & RTCX1, VBIAS.
- Ground guard plane is highly recommended.
- The oscillator VCC should be clean; use a filter, such as an RC low-pass, or a ferrite inductor.

## 8.8.4 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4 is not powered by the system.

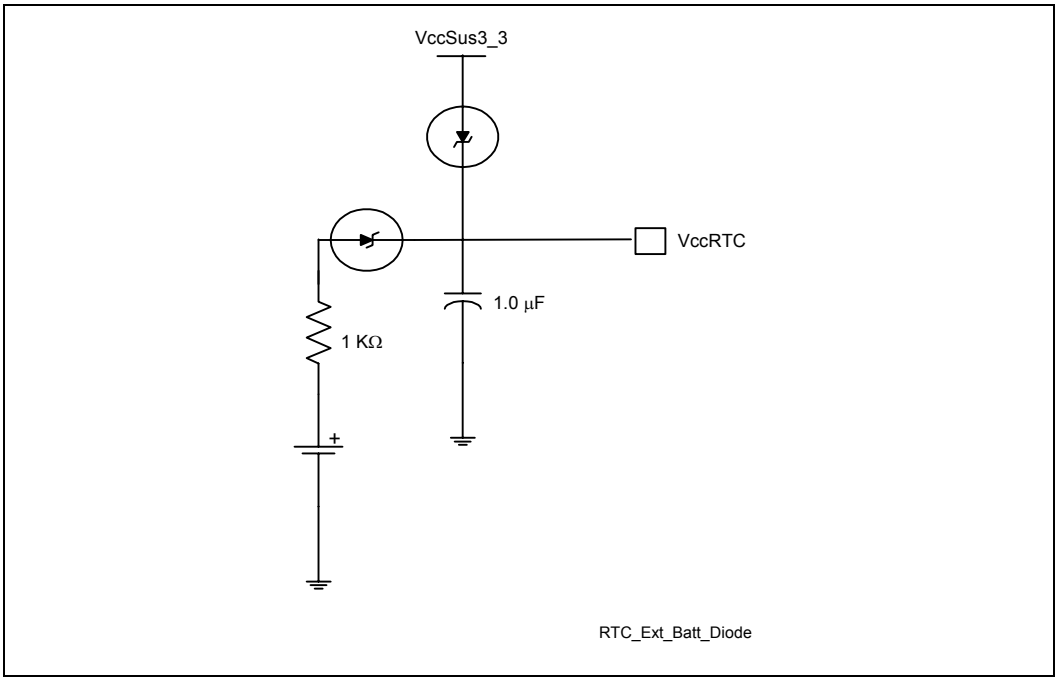
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 5 uA, the battery life will be at least:

170,000 uAh / 5 uA = 34,000 h = 3.9 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH4 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 8-31 is an example of a diode circuit that is used.

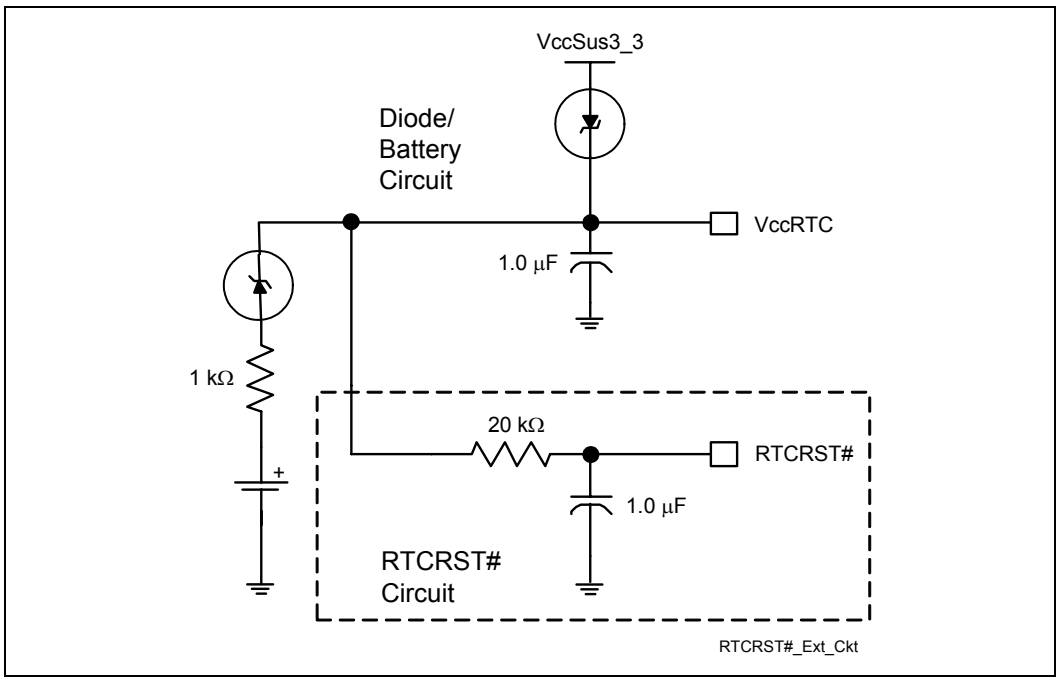
**Figure 8-31. A Diode Circuit to Connect the RTC External Battery**




A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

## 8.8.5 RTC External RTCRST# Circuit

**Figure 8-32. RTCRST# External Circuit for the Intel® ICH4 RTC**




The ICH4 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (VBAT) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms – 25 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in Figure 8-31) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 8-32 is an example of this circuitry that is used in conjunction with the external diode circuit.

### 8.8.6 VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered out from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 8-30) therefore it is self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

- VBIAS should be at least 200 mV DC. The RC network of R2 and C3 will filter out most of AC signal that exist on this ball, however, the noise on this ball should be kept minimal to guarantee the stability of the RTC oscillation.
- Probing VBIAS requires the same technique as probing the RTCX1, RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details on measuring techniques.
- Note that VBIAS is also very sensitive to environmental conditions.

### 8.8.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), SUSCLK duty cycle can be between 30 – 70%. If the SUSCLK duty cycle is beyond 30 – 70% range, it indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50 Ω input impedance probe) and it is an appropriated signal to check the RTC frequency to determine the accuracy of the ICH4's RTC Clock (see Application Note AP-728 for further details).

### 8.8.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST#, when configured as shown in Figure 8-32, meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up (330k ohm) to VCCRTC. This prevents these nodes from floating in G3, and correspondingly prevents ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

## 8.9 Internal LAN Layout Guidelines

The ICH4 provides several options for integrated LAN capability. The platform supports several components depending on the target market. Available LAN components include the 82540EM Gigabit Ethernet controller (GbE), 82551QM Fast Ethernet controller, 82562EZ/82562ET and 82562EX/82562EM platform LAN connect (PLC) components.

**Table 8-16. LAN Component Connections/Features**

| LAN Component | Interface To ICH4 | Connection | Features |
|---|---|---|---|
| 82540EM (196 BGA) | PCI | Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting | Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible |
| 82551QM (196 BGA) | PCI | Performance 10/100 Ethernet with ASF alerting | Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible |
| 82562EM (48 Pin SSOP)<br>82562EX (196 BGA) | LCI | 10/100 Ethernet with Alert on LAN (AoL) alerting | Ethernet 10/100 connection, Alert on LAN (AoL) |
| 82562ET (48 Pin SSOP)<br>82562EZ (196 BGA) | LCI | Basic 10/100 Ethernet | Ethernet 10/100 connection |

Which LAN component to use on the ICH4 platform will depend on the end user's need for connection speed, manageability needs, and bus connection type. In addition, footprint compatible packages make it possible to design a platform that can use any of the LAN components without the need for a motherboard redesign.

## 8.9.1 Footprint Compatibility

The 82540EM GbE controller, 82551QM Fast Ethernet controller, and the 82562EX/82562EZ platform LAN connect devices are all manufactured in a footprint compatible 15 mm x 15 mm (1 mm pitch), 196-ball grid array package. Many of the critical signal pin locations on the 82540EM, 82551QM, and 82562EX/82562EZ are identical, allowing designers to create a single design that accommodates any one of these parts. Because the usage of some pins on the 82540EM differ from the usage on the 82551QM or the 82562EX/82562EZ, the parts are not referred to as "pin compatible". The term "footprint compatible" refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design. Therefore, it is easy to populate a single board design with either part to maximize value while matching your customers' performance needs.

Design guidelines are provided for each required interface and connection. Refer to the following figures and table for the corresponding section of the design guide. The guidelines use the 82546EZ to refer to both the 82562EZ and 82562EX. The 82562EX is specified in those cases where there is a difference.

**Figure 8-33. Intel® ICH4/Platform LAN Connect Section**

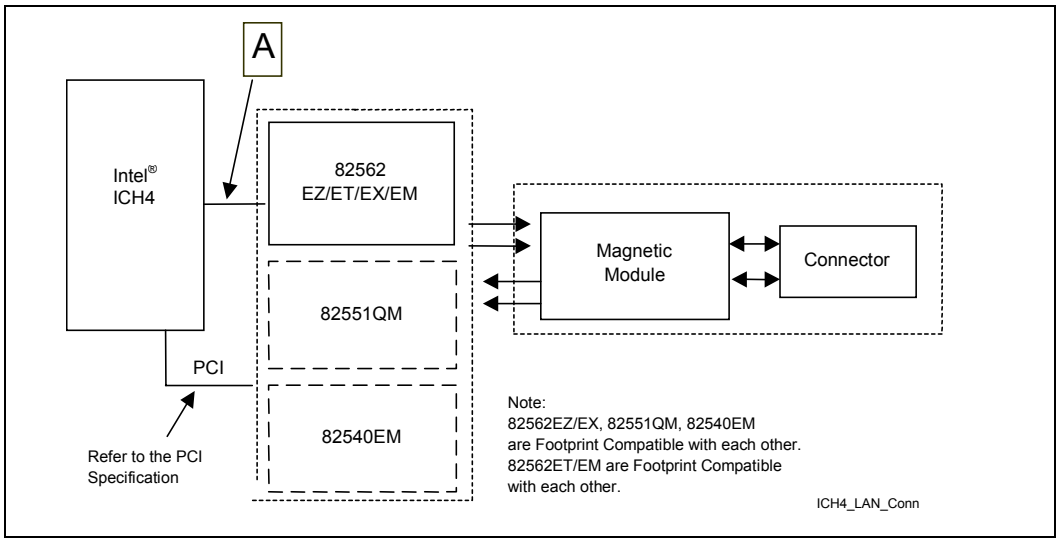



**Table 8-17. LAN Design Guide Section Reference**

| Layout Section | Figure 8-33 Reference | Design Guide Section |
|---|---|---|
| ICH4 – LAN Connect Interface (LCI) | A | 8.9.2, Intel® ICH4 — LAN Connect Interface Guidelines |
| 82562EZ/EX<br>82562ET / 82562EM | A | 8.9.3, Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM and Intel® 82551QM |
| 82551QM | PCI | 8.9.3, Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM and Intel® 82551QM |
| 82540EM | PCI | 8.10.2, Design and Layout Considerations for Intel® 82540EM |

## 8.9.2 Intel® ICH4 — LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN connect device on a system motherboard or on a CNR riser card. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH4 to LAN connect interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports 82562EZ/ET and 82562EX/EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD0, and LAN_TXD0 are shared by all components. The AC characteristics for this interface are found in the *Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet*.

### 8.9.2.1 Bus Topologies

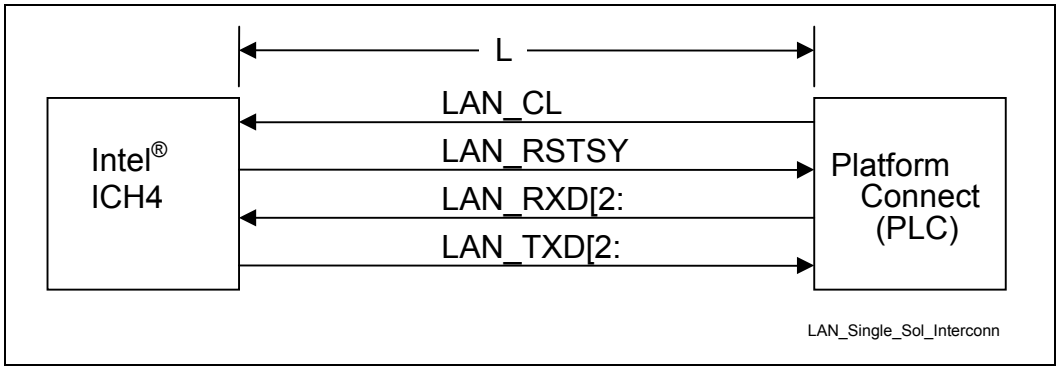
The platform LAN connect interface can be configured in several topologies:

- Direct point-to-point connection between the ICH4 and the LAN component
- LOM/CNR Implementation

#### 8.9.2.1.1 LOM (LAN on Motherboard) or CNR Point-to-Point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EZ/ET, 82562EX/EM, or CNR are uniquely installed.

**Figure 8-34. Single Solution Interconnect**



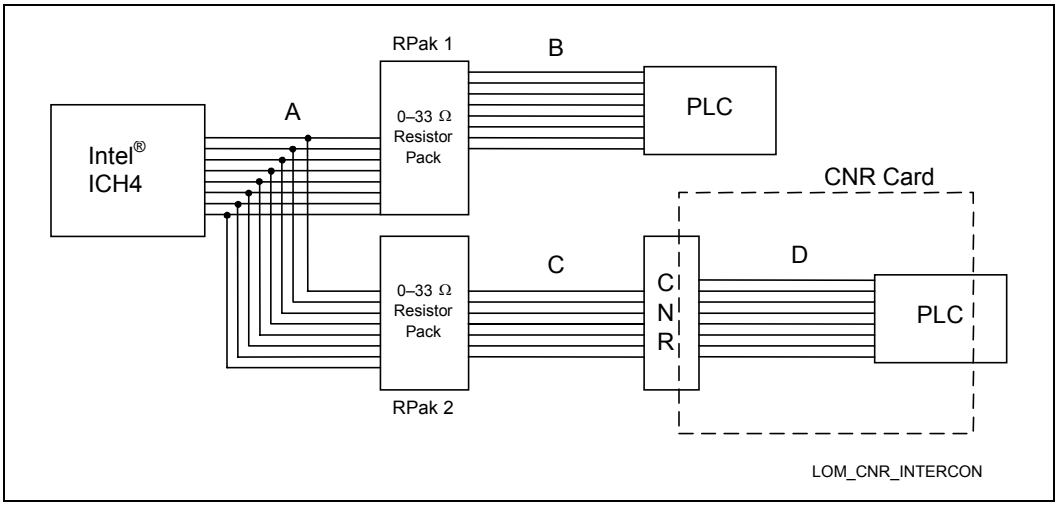
### Table 8-18. LAN LOM or CNR Routing Summary

| Trace Impedance | LAN Routing Requirements | Maximum Trace Length | | Signal Referencing | LAN Signal Length Matching |
|---|---|---|---|---|---|
| 51 Ω to 69 Ω, 60 Ω Target | 5 on 10 | 82562EZ/ET/EX/EM | 4.5” to 12” | Ground | Data signals must be equal to no more than 0.5 inch (500 mils) shorter than the LAN clock trace. |
| | | 82562EZ/ET/EX/EM on CNR | 2” to 9.5” | | |

## 8.9.2.1.2 LOM (LAN on Motherboard) and CNR Interconnect

The following guidelines apply to an all-inclusive configuration of PLC design. This layout combines LAN on motherboard and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN on motherboard option can be implemented at one time.

### Figure 8-35. LOM/CNR Interconnect




### Table 8-19. LOM/CNR Dual Routing Summary

| Trace Impedance | LAN Routing Req. | Maximum Trace Length | Sig. Ref. | LAN Signal Length Matching |
|---|---|---|---|---|
| 51 Ω to 69 Ω, 60 Ω Target | 5 on 10 | **82562EZ /ET/EX/EM**<br>**A** 0.5” to 7.5”; **B** 4” to (11.5 – A) “; **C** NA; **D** NA<br>**82562EZ /ET/EX/EM on CNR[1]**<br>**A** 0.5” to 7.5”; **B** NA; **C** 1.5” to (9.0 – A) “; **D** 0.5” to 3” | Gnd. | Data signals must be equal to or no more than 0.5 inch (500 mils) shorter than the LAN clock trace. |

**NOTES:**
1. Total motherboard trace length should not exceed 9.0”

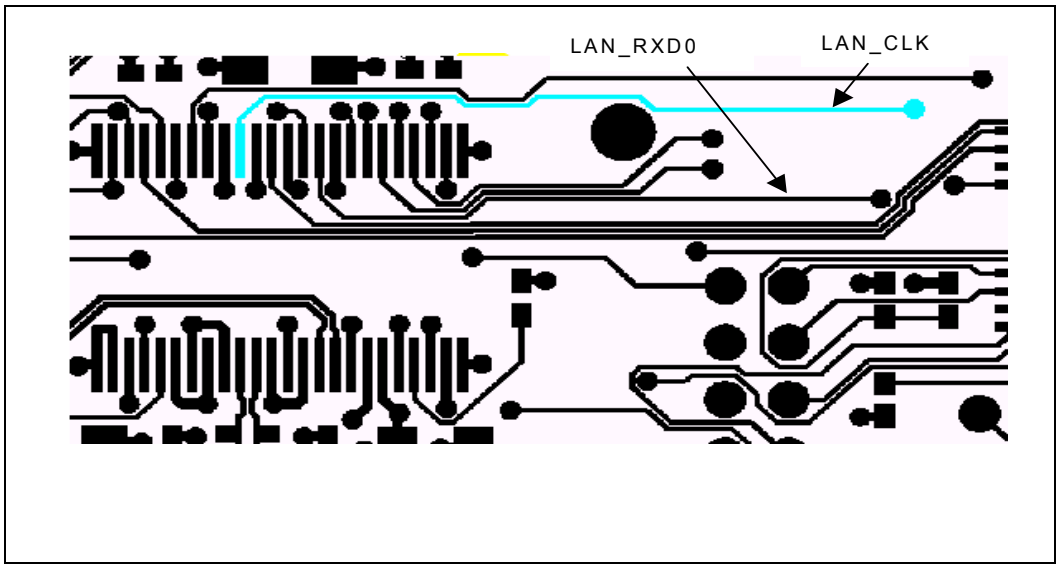
Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 Ω to 33 Ω (See Section 8.9.2.5).

### 8.9.2.2 Signal Routing and Layout

Platform LAN connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inch shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

**Figure 8-36. LAN_CLK Routing Example**




### 8.9.2.3 Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the tRMATCH skew parameter. TRMATCH is the sum of the trace length mismatch between LAN_CLK and LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inch shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

### 8.9.2.4 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ±15% is strongly recommended; otherwise, signal integrity requirements may be violated.

#### 8.9.2.5 Line Termination

Line termination mechanisms are not specified for the LAN connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0 to 33 Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

#### 8.9.2.6 Terminating Unused LAN Connect Interface Signals

The LAN connect interface on the ICH4 can be left as a no-connect if it is not used.

### 8.9.3 Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM and Intel® 82551QM

For correct LAN performance, designers must follow the general guidelines outlined in Section 8.9.2 (General LAN Routing Guidelines and Considerations). Additional guidelines for implementing an 82562EZ/ET/EX/EM or 82551QM platform LAN connect component are provided below.

#### 8.9.3.1 Guidelines for Intel® 82562EZ/ET/EX/EM / Intel® 82551QM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

### 8.9.3.2 Crystals and Oscillators

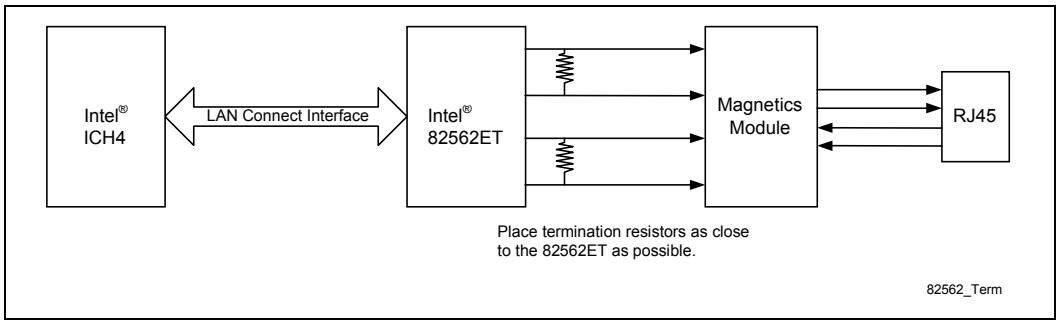
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to the 82562EZ/ET/EX/EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

### 8.9.3.3 Intel® 82562EZ/ET/EX/EM / Intel® 82551QM Termination Resistors

The 100 Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 121 Ω (±1%) receive differential pairs (RDP/RDN) should be placed as close to the platform LAN connect component (82562EZ/ET/EX/EM and 82551QM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

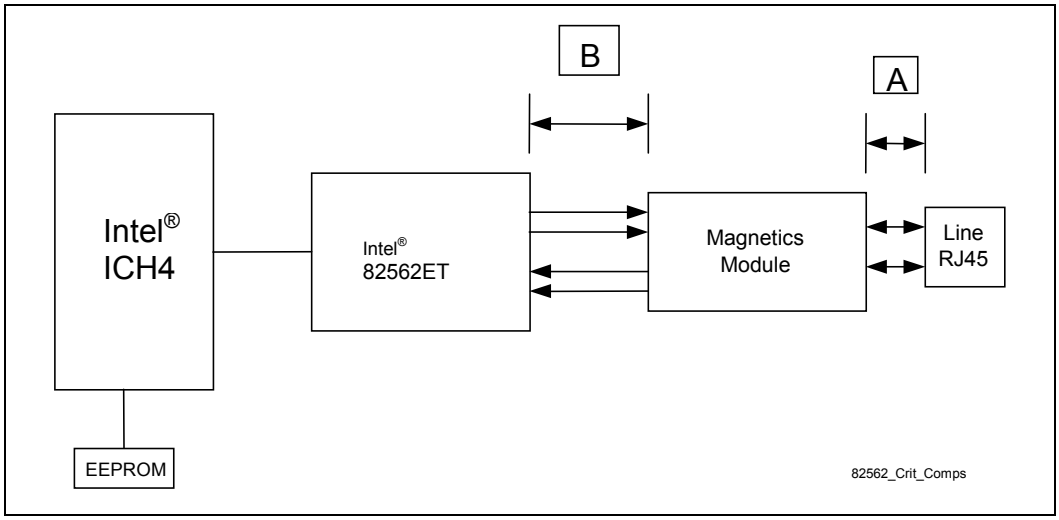
**Figure 8-37.Intel® 82562ET/82562EM Termination**



### 8.9.3.4 Critical Dimensions

There are two dimensions to consider during layout. Distance ‘A’ from the line RJ45 connector to the magnetics module and distance ‘B’ from the 82562EZ/ET/EX/EM or 82551QM to the magnetics module. The combined total distances of A and B must not exceed 4 inches (preferably, less than 2 inches — see Figure 8-38).

**Figure 8-38. Critical Dimensions for Component Placement**




| Distance | Priority | Guideline |
|---|---|---|
| A | 1 | < 1 inch |
| B | 2 | < 1 inch |

#### 8.9.3.4.1 Distance from Magnetics Module to RJ45 (Distance A)

The distance A in the preceding figure should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- **Differential Impedance:** The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 60 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- **Trace Symmetry:** Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

***Caution:*** Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit’s performance and contribute to radiated emissions from the transmit circuit. If the 82562EZ/ET/EX/EM or 82551QM must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562EZ/ET/EX/EM or 82551QM and RJ45 as short as possible should be a priority.

***Note:*** Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105–110 Ω should compensate for second order effects.

#### 8.9.3.4.2 Distance from Intel® 82562EZ/ET/EX/EM / Intel® 82551QM to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and equal length within each differential pair.

### 8.9.3.5 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Signals with fast rise and fall times contain many high-frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

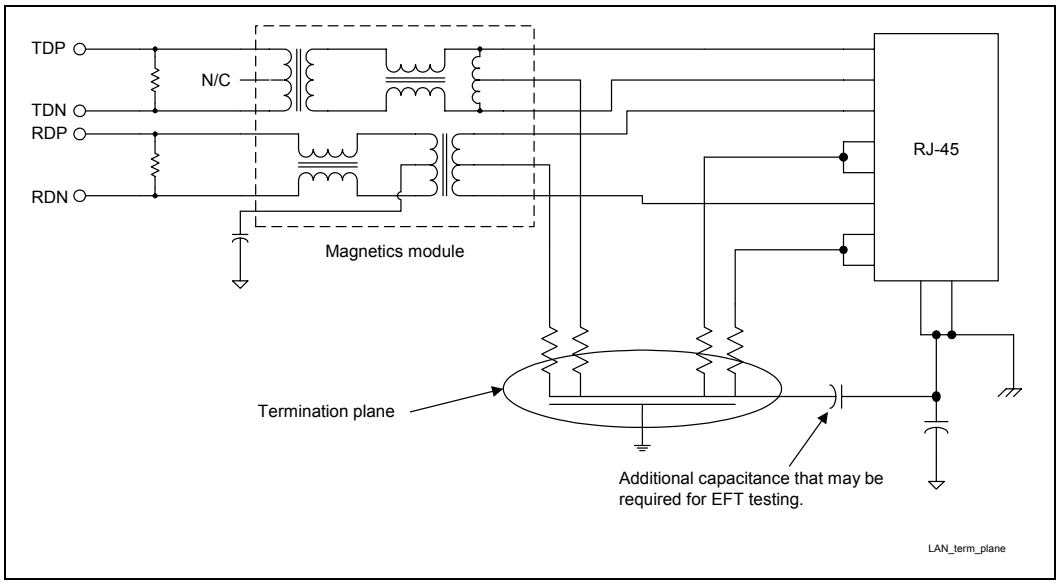
#### Terminating Unused Connections

In Ethernet designs it is common practice to terminate unused connections on the RJ45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

#### 8.9.3.5.1 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

**Figure 8-39. Termination Plane**

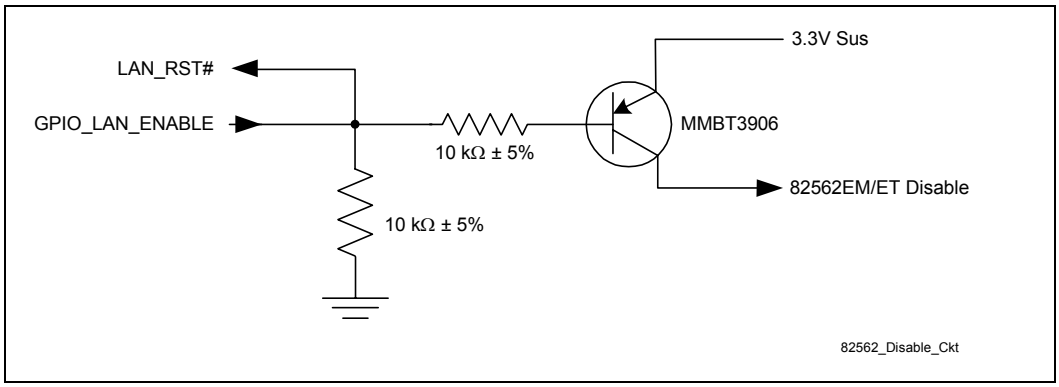


# 8.10 Intel® 82562EZ/ET/EX/EM Disable Guidelines

## 8.10.1 Intel® 82562EZ/ET/EX/EM Disable Guidelines

To disable the 82562EZ/ET/EX/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS controlling the GPIO can disable the LAN microcontroller.

**Figure 8-40. Intel® 82562EZ/ET/EX/EM Disable Circuitry**




There are 4 pins that are used to put the 82562EZ/ET/EX/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 8-20 describes the operational/disable features for this design.

The four control signals shown in Table 8-20 should be configured as follows: Test_En should be pulled-down thru a 100 Ω resistor. The remaining 3 control signals should each be connected thru 100 Ω series resistors to the common node “82562EZ/ET/EX/EM _Disable” of the disable circuit.

**Table 8-20. Intel® 82562EZ/ET/EX/EM Control Signals**

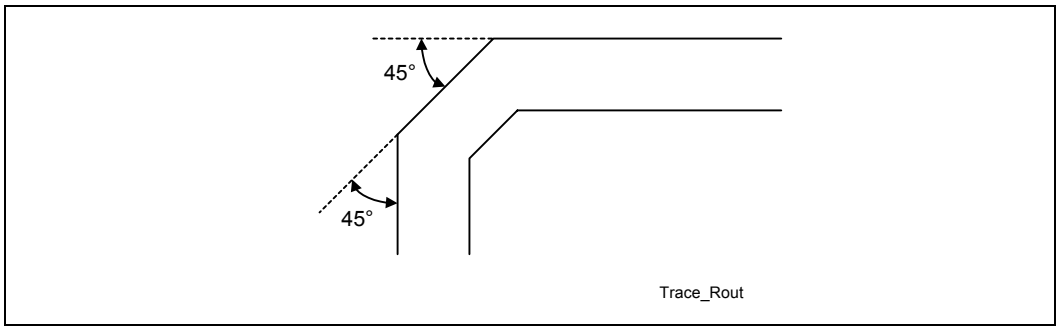
| Test_En | Isol_Tck | Isol_Ti | Isol_Tex | State |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Enabled |
| 0 | 1 | 1 | 1 | Disabled w/ Clock (low power) |
| 1 | 1 | 1 | 1 | Disabled w/out Clock (lowest power) |

### 8.10.1.1 General Intel® 82562ET/82562EM Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance: (Note: Some suggestions are specific to a 4.3 mil stack-up.)

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).]
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces. (300 mils recommended)
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two 45-degree bends instead. Refer to Figure 8-41.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

**Figure 8-41. Trace Routing**



#### 8.10.1.1.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

#### 8.10.1.1.2 Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together.

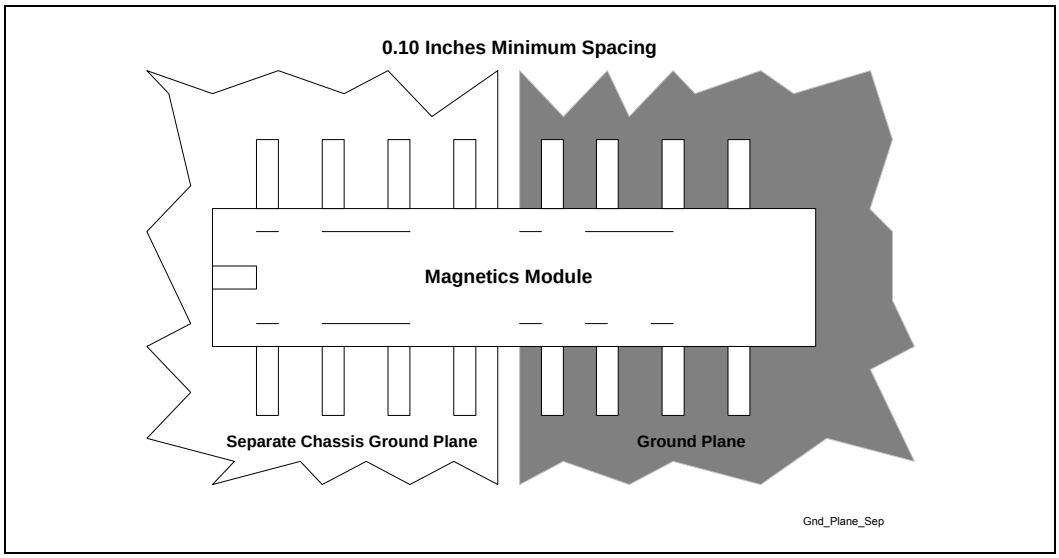
  **Note:** Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

### 8.10.1.1.3 Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

**Figure 8-42. Ground Plane Separation**




Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both back planes and motherboards.

- Route traces over a continuous plane with no interruptions (don't route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This minimizes the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics that can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

### 8.10.1.2 Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

- Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
- Lack of symmetry between the two traces within a differential pair. [Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.] Asymmetry can create common-mode noise and distort the waveforms.
- Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer. The magnetics should be as close to the connector as possible (less than or equal to one inch).
- Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
- Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45, and the PLC.
- Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
- Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or application note.
- Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or term plane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The AP-Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
- Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. [To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive

coupling between the two traces. When the two traces within a differential pair are kept close† to each other the edge coupling can lower the effective differential impedance by 5 to 20 Ω. A 10 to 15 Ω drop in impedance is common.] Short traces will have fewer problems if the differential impedance is a little off.

- Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetics transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. [6 pF to 12 pF values have been used on past designs with reasonably good success.] These caps are not necessary, unless there is some overshoot in 100 Mbps mode.

***Note:*** It is important to keep the two traces within a differential pair close† to each other. Keeping them close† helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.

***Note:*** † Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

## 8.10.2 Design and Layout Considerations for Intel® 82540EM

For specific design and layout considerations for the 82540EM refer to the *82540EM Gigabit Ethernet Controller Preliminary Datasheet and Hardware Design Guide.*

# 8.11 Intel® ICH4 – SYS_RESET#/PWRBTN# Usage Models and Power-Well Isolation Control Strap Requirements

This section describes the SYS_RESET# and PWRBTN# Usage Models and Power-Well Isolation Control Strap Requirements.

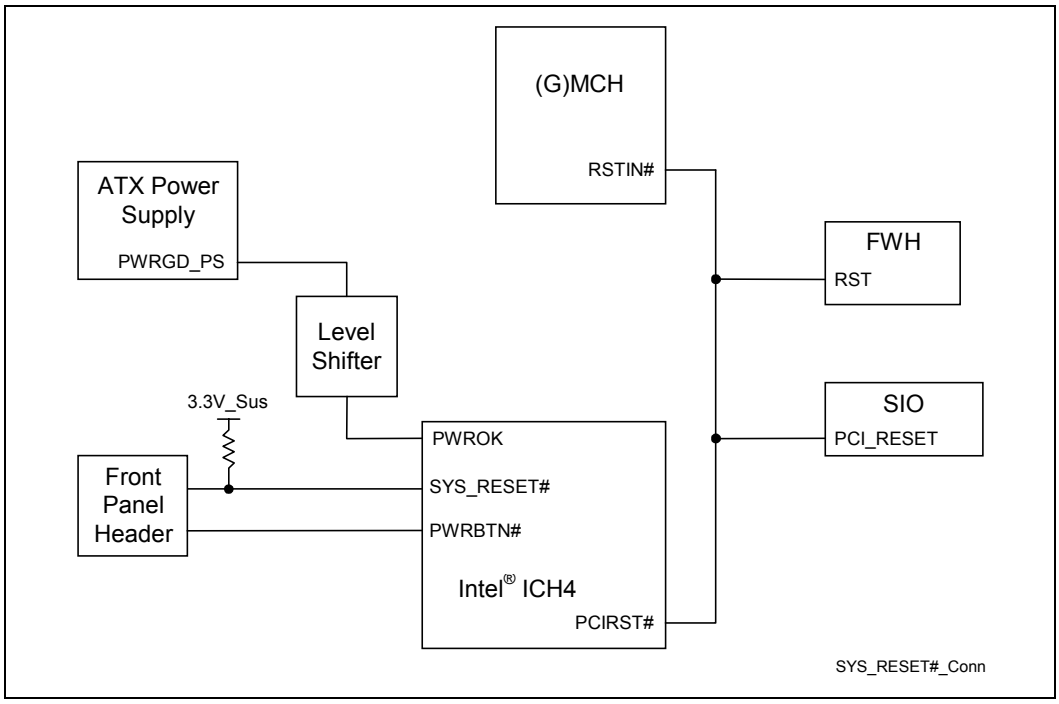
## 8.11.1 SYS_RESET# Usage Model

The System Reset ball (SYS_RESET#) on the ICH4 can be connected directly to the reset button on the systems front panel provided that the front panel header pulls this signal up to 3.3 V standby through a weak pull-up resistor. The ICH4 will debounce signals on this pin (16ms) and allow the SMBus to go idle before resetting the system; thus helping prevent a slave device on the SMBus from "hanging" by resetting in the middle of a cycle.

## 8.11.2 PWRBTN# Usage Model

The Power Button ball (PWRBTN#) on the ICH4 can be connected directly to the power button on the systems front panel. This signal is internally pulled-up in the ICH4 to 3.3 V standby through a weak pull-up resistor (24 kΩ nominal). The ICH4 has 16ms of internal debounce logic on this pin.

**Figure 8-43. SYS_RESET# and PWRBTN# Connection**

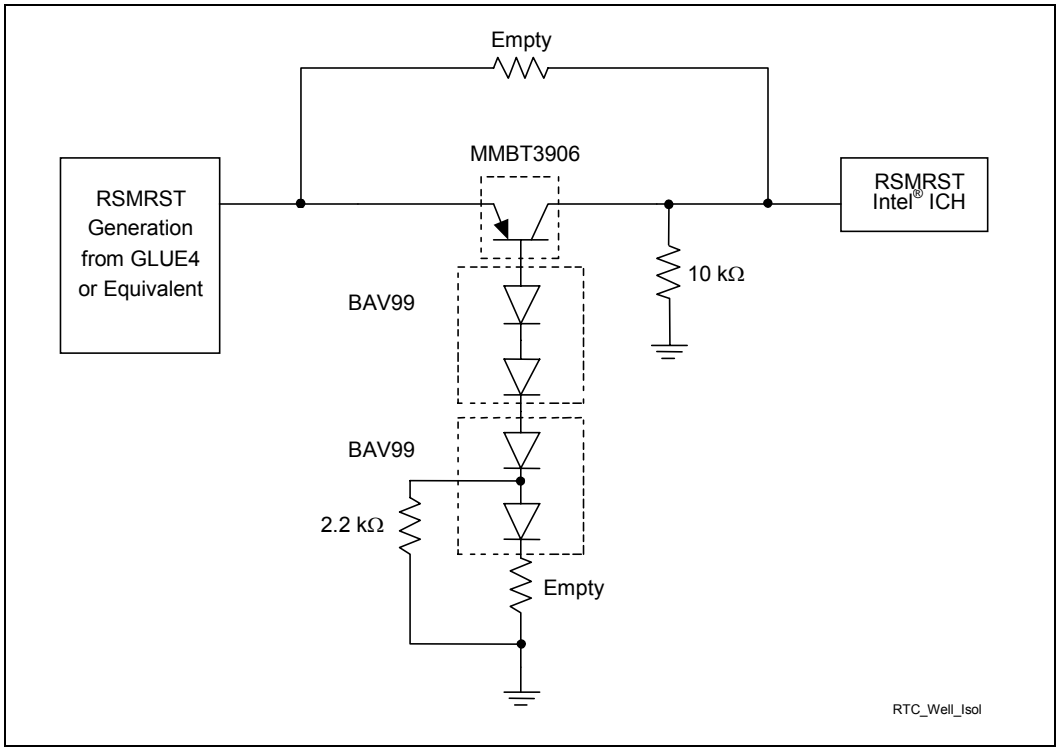


### 8.11.3 Power-Well Isolation Control Requirement

The RSMRST# signal of the ICH4 must transition from 20 % signal level to 80 % signal level and vice-versa in 50 µs or less. Slower transitions may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node can potentially cause the CMOS to be cleared or corrupted, the RTC to loose time after several AC power cycles, or the intruder bit might assert erroneously.

The circuit shown in Figure 8-44 can be implemented to control well isolation between the VccSus3_3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail or does not meet the above rise/fall time.

**Figure 8-44. RTC Power Well Isolation Control**




## 8.12 General Purpose I/O

### 8.12.1 GPIO Summary

The ICH4 has 12 general purpose inputs, 8 general purpose outputs, and 16 general purpose inputs/outputs.

### Table 8-21. GPIO Summary

| GPIO Number | Power Well | Input, Output, I/O | Tolerance | Note |
|---|---|---|---|---|
| 0 | Core | Input | 5 V | 2 |
| 1 | Core | Input | 5 V | 2 |
| 2 | Core | Input | 5 V | 2 |
| 3 | Core | Input | 5 V | 2 |
| 4 | Core | Input | 5 V | 2 |
| 5 | Core | Input | 5 V | 2 |
| 6 | Core | Input | 5 V | |
| 7 | Core | Input | 5 V | |
| 8 | Resume | Input | 3.3 V | |
| 11 | Resume | Input | 3.3 V | 2 |
| 12 | Resume | Input | 3.3 V | |
| 13 | Resume | Input | 3.3 V | |
| 16 | Core | Output | 3.3 V | 2 |
| 17 | Core | Output | 3.3 V | 2 |
| 18 | Core | Output | 3.3 V | |
| 19 | Core | Output | 3.3 V | |
| 20 | Core | Output | 3.3 V | |
| 21 | Core | Output | 3.3 V | |
| 22 | Core | Output (Open Drain) | 3.3 V | |
| 23 | Core | Output | 3.3 V | |
| 24 | Resume | I/O | 3.3 V | 1 |
| 25 | Resume | I/O | 3.3 V | 1 |
| 27 | Resume | I/O | 3.3 V | 1 |
| 28 | Resume | I/O | 3.3 V | 1 |
| 32 | Core | I/O | 3.3 V | 1 |
| 33 | Core | I/O | 3.3 V | 1 |
| 34 | Core | I/O | 3.3 V | 1 |
| 35 | Core | I/O | 3.3 V | 1 |
| 36 | Core | I/O | 3.3 V | 1 |
| 37 | Core | I/O | 3.3 V | 1 |
| 38 | Core | I/O | 3.3 V | 1 |
| 39 | Core | I/O | 3.3 V | 1 |
| 40 | Core | I/O | 3.3 V | 1 |
| 41 | Core | I/O | 3.3 V | 1 |
| 42 | Core | I/O | 3.3 V | 1 |
| 43 | Core | I/O | 3.3 V | 1 |

**NOTES:**
1. Defaults as an output.
2. Can be used as a GPIO if the native function is not needed. ICH4 defaults these signals to native functionality.

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# 9 Firmware Component Guidelines

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent.

## 9.1 FWH Vendors

The following vendors manufacture firmware hubs, which conform to the *Intel® FWH Specification*. Contact the vendor directly for information on packaging and density.

SST http://www.ssti.com/

STM http://us.st.com/stonline/index.shtml

ATMEL http://www.atmel.com/

## 9.2 FWH Decoupling

A 0.1 µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple high-frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple low-frequency noise. The capacitors should be placed no further than 390 mils from the Vcc supply pins.

## 9.3 In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The ICH4 Hub Interface to PCI Bridge will put all CPU boot cycles out on PCI (before sending them out on the FWH interface). If the ICH4 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. In order to boot off a PCI card it is necessary to keep the ICH4 in subtractive decode mode. If a PCI boot card is inserted and the ICH4 is programmed for positive decode, there will be two devices positively decoding the same cycle.

## 9.4 FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points need to be considered because they are NOT consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH4 INIT# signal needs to be at a value slightly higher than the $V_{IH}$ min FWH INIT# pin specification. The ICH4 inactive state of this signal is typically governed by the formula V_CPU_IOmin - noise margin. Therefore if the V_CPU_IOmin of the processor is 1.6 V, the noise margin is 200mV and the $V_{IH}$ min spec of the FWH INIT# input signal is 1.35 V, there

would be no compatibility issue because 1.6 V - 0.2 V = 1.40 V which is greater than the 1.35 V minimum of the FWH. If the $V_{IH}$ min of the FWH was 1.45 V, then there would be an incompatibility and logic translation would need to be used. Note that these examples do not take into account actual noise that may be encountered on INIT#. Care must be taken to ensure that the $V_{IH}$ min specification is met with ample noise margin. In applications where it is necessary to use translation logic, refer to the circuit in the following table.

The following solutions assume that level translation is necessary. The figures below implement a topology solution for the ICH4 FWH signal INIT# and the CPU solution. Trace lengths and resistor values are found in the subsequent table.

**Figure 9-1. FWH/CPU Signal Topology Solution**

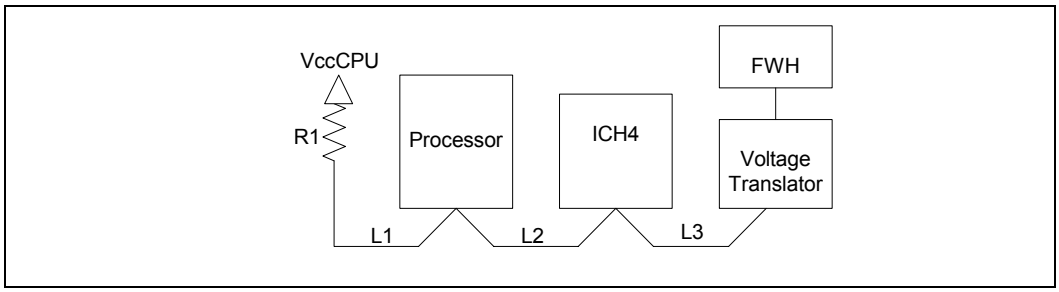
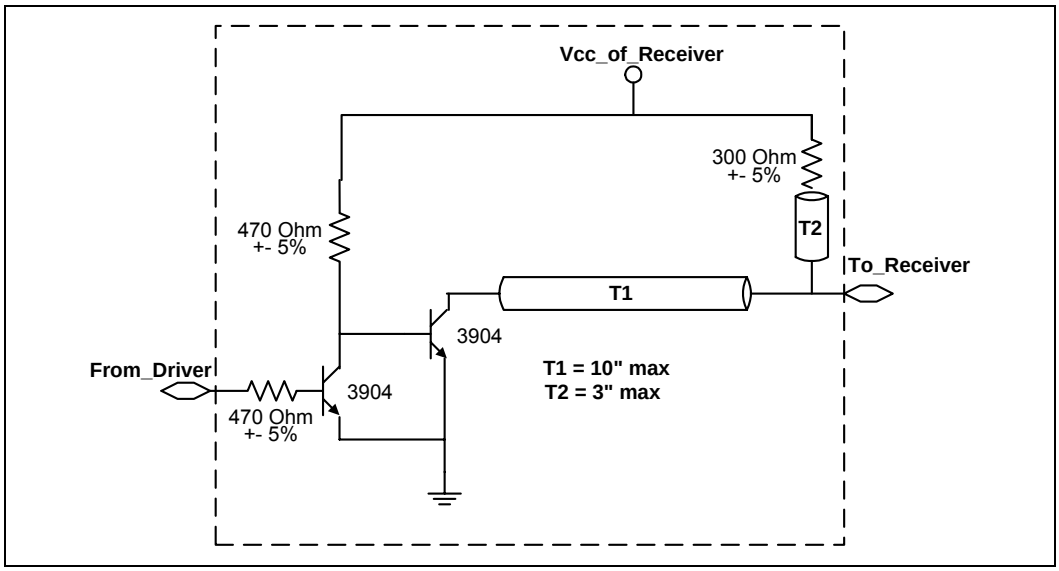



**Table 9-1. CPU/ICH FWH Topology Table: Resistor and Length Values**

| R1 | L1 | L2 | L3 |
|---|---|---|---|
| TBD | TBD | TBD | TBD |

**Figure 9-2 FWH Level Translation Circuitry**

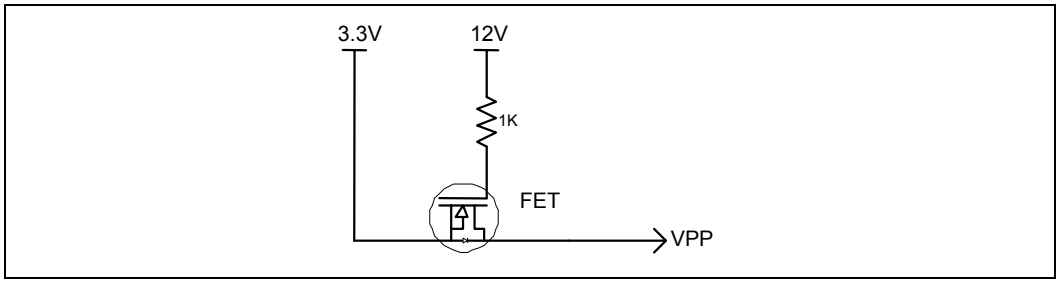


## 9.5 FWH VPP Design Guidelines

The $V_{PP}$ pin on the FWH is used for programming the flash cells. The FWH supports $V_{PP}$ of 3.3 V or 12 V. If $V_{PP}$ is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH only supports 12 V $V_{PP}$ for 80 hours (3.3 V on Vpp does not affect the life of the device). The 12 V $V_{PP}$ would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The $V_{PP}$ pin MUST be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the $V_{PP}$ pin. The following circuit will allow testers to put 12 V on the $V_{PP}$ pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

**Figure 9-3. FWH VPP Isolation Circuitry**

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# 10 Miscellaneous Logic

The ICH4 requires additional external circuitry in order to function properly. Some of these functionalities include meeting timing specifications, buffering signals, and switching between power wells. This logic may be implemented through the use of the Glue Chip or discrete logic.

## 10.1 Glue Chip 4

In order to reduce the component count and BOM (Bill of Materials) cost of the ICH4 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The ICH4 Glue Chip is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Features

- Dual, Strapping, Selectable Feature Sets
- Audio-disable circuit
- Mute Audio Circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWRGD signal generation
- Power Sequencing / BACKFEED_CUT
- Power Supply turn on circuitry
- RSMRST# generation
- VGA DDC voltage translation
- HSYNC / VSYNC voltage translation to VGA monitor
- Tri-state buffers for test
- Extra GP Logic Gates
- Power LED Drivers
- Flash FLUSH# / INIT# circuit

More information regarding this component is available from the following vendors:

| Vendor | Contact Information |
|---|---|
| Philips Semiconductors | 6028 44th Way NE<br>Olympia, WA 98516-2477<br>Fax: (360) 438-3606 |
| Fujitsu Microelectronics | 3545 North 1st Street, M/S 104<br>San Jose, CA 95134-1804<br>Fax: 1-408-922-9179 |

## 10.2 Discrete Logic

As an alternative solution, discrete circuitry may be implemented into a design instead of using the Glue Chip.

# 11 Platform Clock Routing Guidelines

The following sections describe platform clock routing layout guidelines for 845E chipset-based systems.

## 11.1 Clock Generation

Only one clock generator component is required in an 845E chipset-based system. Clock synthesizers that meet the *Intel CK_408 Clock Synthesizer/Driver Specification* are suitable for 845E chipset based systems. For more information on CK_408 compliance, refer to the *CK_408 Clock Synthesizer/Driver Specification*. The following tables and figure list and illustrate the 845E chipset clock groups, the platform system clock cross-reference, and the platform clock distribution.

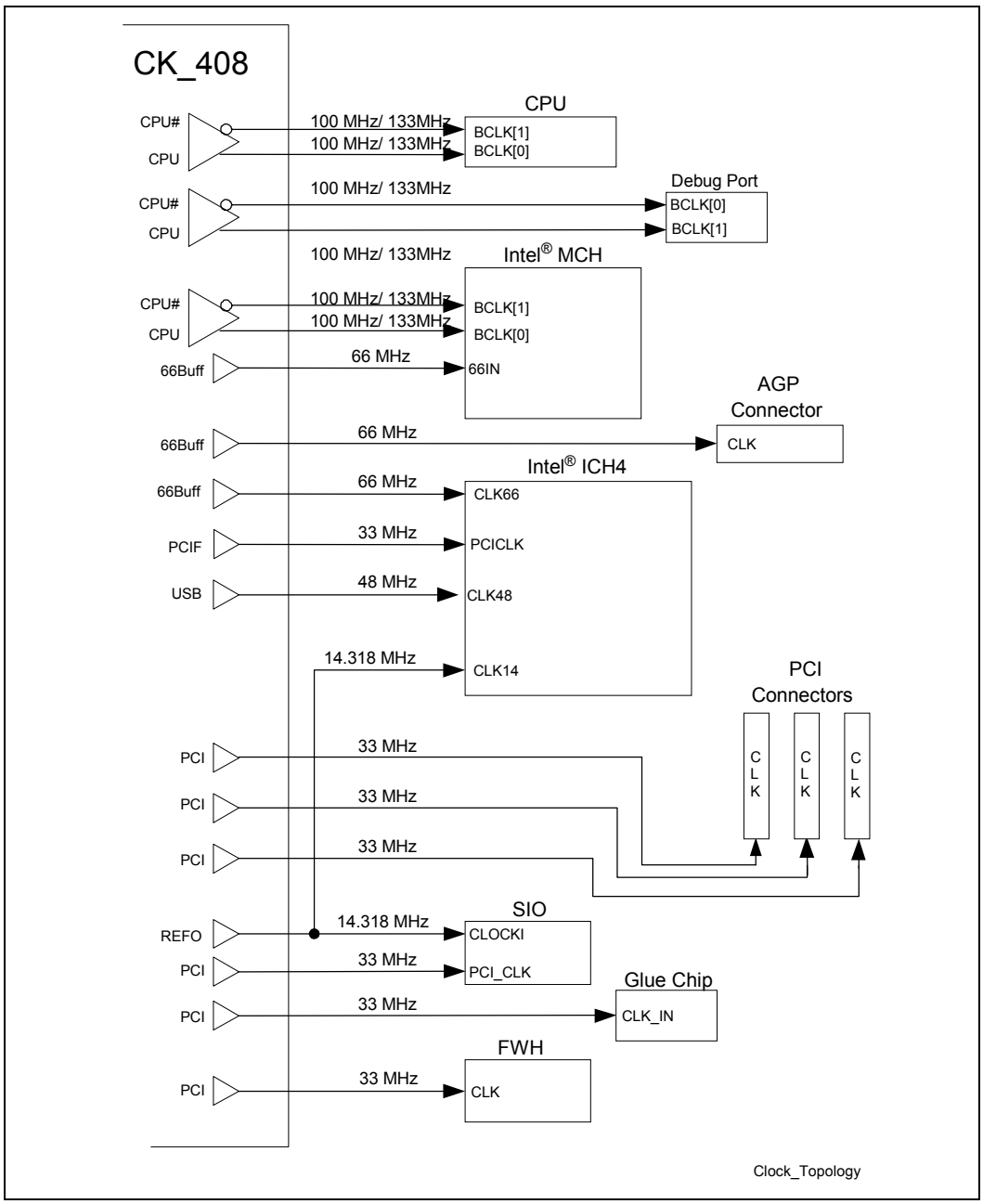
**Table 11-1. Intel® 845E Chipset Clock Groups**

| Clock Name | Frequency | Receiver |
|---|---|---|
| Host_CLK | 100 MHz / 133MHz | Processor, Debug Port, and MCH |
| CLK66 | 66 MHz | MCH and Intel® ICH4 |
| AGPCLK | 66 MHz | AGP Connector or AGP Device |
| CLK33 | 33 MHz | ICH4, SIO, Glue Chip, and FWH |
| CLK14 | 14.318 MHz | ICH4 and SIO |
| PCICLK | 33 MHz | PCI Connector |
| USBCLK | 48 MHz | ICH4 |

### Table 11-2. Platform System Clock Cross-Reference

| Clock Group | CK_408 Pin | Component | Component Pin Name |
|---|---|---|---|
| HOST_CLK | CPU | CPU | BCLK0 |
| | CPU# | CPU | BCLK1 |
| | CPU | Debug Port | BCLK0 |
| | CPU# | Debug Port | BCLK1 |
| | CPU | MCH | BCLK0 |
| | CPU# | MCH | BCLK1 |
| CLK66 | 66BUFF | MCH | 66IN |
| | | ICH4 | CLK66 |
| AGPCLK | 66BUFF | AGP Connector or AGP Device | CLK |
| CLK33 | PCIF | ICH4 | PCICLK |
| | PCI | SIO | PCI_CLK |
| | PCI | Glue Chip | CLK_IN |
| | PCI | FWH | CLK |
| CLK14 | REF0 | ICH4 | CLK14 |
| | | SIO | CLOCKI |
| PCICLK | PCI | PCI Connector #1 | CLK |
| | | PCI Connector #2 | CLK |
| | | PCI Connector #3 | CLK |
| USBCLK | USB | ICH4 | CLK48 |

**Figure 11-1. Clock Topology**



## 11.2 Clock Group Topology and Layout Routing Guidelines

### 11.2.1 HOST_CLK Clock Group

The clock synthesizer provides three sets of 100 MHz / 133MHz differential clock outputs. The 100 MHz / 133MHz differential clocks are driven to the processor, the 845E chipset, and the processor debug port as shown in Figure 11-1.

The clock driver differential bus output structure is a “Current Mode Current Steering” output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying IOUT by the value of Rt. The current IOUT is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedances or to accommodate future load requirements.

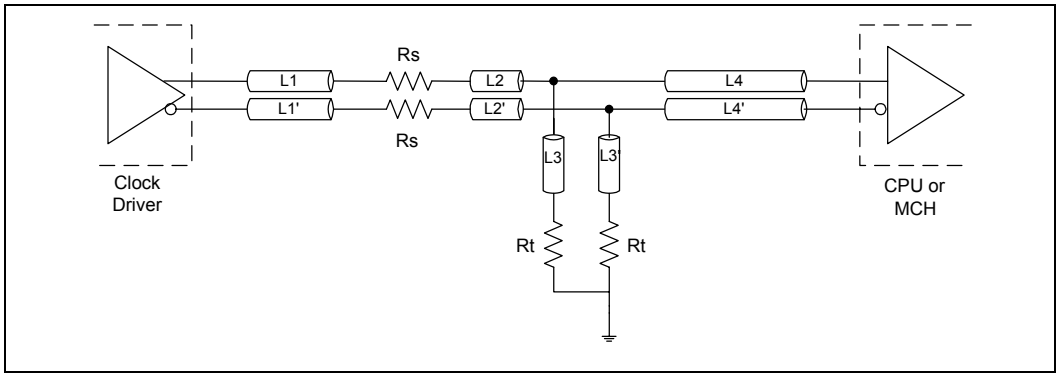
The recommended termination for the differential bus clock is a “Shunt Source termination.” Refer to Figure 11-2 for an illustration of this termination scheme. Parallel Rt resistors perform a dual function, converting the current output of the clock driver to a voltage, and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver’s output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the system board, and Rs should be between 20 and 33 Ω. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity and only degrade the edge rate.

Mult0 pin (pin #43) is connected to HIGH, making the multiplication factor 6.

The IREF pin (pin # 42) is connected to ground through a 475 Ω ± 1% resistor, making the IREF 2.32 mA.

**Figure 11-2. Source Shunt Termination**



### Table 11-3. BCLK [1:0]# Routing Guidelines

| Layout Guideline | Value | Illustration | Notes |
|---|---|---|---|
| BCLK Skew between agents | 400 ps total<br>Budget:<br>150 ps for Clock driver<br>250 ps for interconnect | Figure 11-1 | 1, 2, 3, 4 |
| Differential pair spacing | W max. | Figure 11-4 | 5, 6 |
| Spacing to other traces | 4 W–5 W mils | Figure 11-4 | -- |
| Line width | 7.0 mils | Figure 11-4 | 8 |
| System board Impedance—Differential | 100 Ω ± 15% | — | 9 |
| System board Impedance—odd mode | 50 Ω ± 15% | — | 10 |
| Processor routing length—<br>L1, L1': Clock driver to Rs | 0.5 in. max | Figure 11-2 | 14 |
| Processor routing length—<br>L2, L2': Rs to Rs-Rt node | 0–0.2 in. | Figure 11-2 | 14 |
| Processor routing length—<br>L3, L3': RS-RT node to Rt | 0–0.2 in. | Figure 11-2 | 14 |
| Processor routing length—<br>L4, L4': RS-RT Node to Load | 2–9 in. | Figure 11-2 | |
| MCH routing length—<br>L1, L1': Clock Driver to RS | 0.5 in. max | Figure 11-2 | 14 |
| MCH routing length—<br>L2, L2': Rs to Rs-Rt node | 0–0.2 in. | Figure 11-2 | 14 |
| MCH routing length—<br>L3, L3': RS-RT node to Rt | 0–0.2 in. | Figure 11-2 | 14 |
| MCH routing length—<br>L4, L4': RS-RT Node to Load | 2–9 in. | Figure 11-2 | |
| Clock driver to Processor and clock driver to Chipset length matching. | 400 mils—600 mils | Figure 11-2 | 7,11 |
| BCLK0—BCLK1 length matching | ± 10 mils | Figure 11-2 | — |
| Rs Series termination value | 33 Ω ± 5% | Figure 11-2 | 12 |
| Rt Shunt termination value | 49.9 Ω ± 5% (for 50 Ω impedance) | Figure 11-2 | 13 |

**NOTES:**

1. The skew budget includes clock driver output pair to output pair jitter (differential jitter) and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers, and are routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two-bus agents. Measured at the crossing point.
5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing because this will degrade the noise rejection of the network.

7. The clock driver to MCH trace length must be greater than the clock driver to processor socket trace length. This accounts for delay through the processor socket.
8. Set the line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stackup.
9. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1—2*Kb), where Kb is the backwards cross-talk coefficient. Kb is very small for the recommended trace spacing, and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
10. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the BCLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
11. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the system board trace length for the chipset will be longer than that for the processor.
12. Rs values between 20–33 Ω have been shown to be effective.
13. Rt shunt termination value should match the system board impedance.
14. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ring back.

## BCLK General Routing Guidelines

- When routing the 100 MHz differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.
- If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.
- Do not place vias between adjacent complementary clock traces, and avoid differential vias. A via that is placed in one half of a differential pair must be matched by a via in the other half of the differential pair. Differential vias can be placed within length L1, between clock driver and RS, if needed to shorten length L1.

## EMI Constraints

Clocks are a significant contributor to EMI and should be treated with care. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to the VSS reference plane only.

**Figure 11-3. Clock Skew as Measured From Agent to Agent**

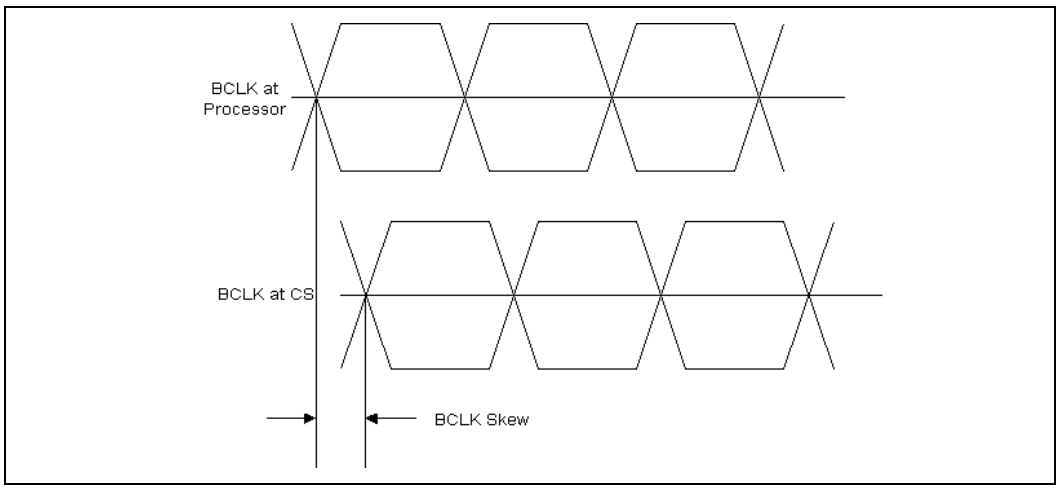
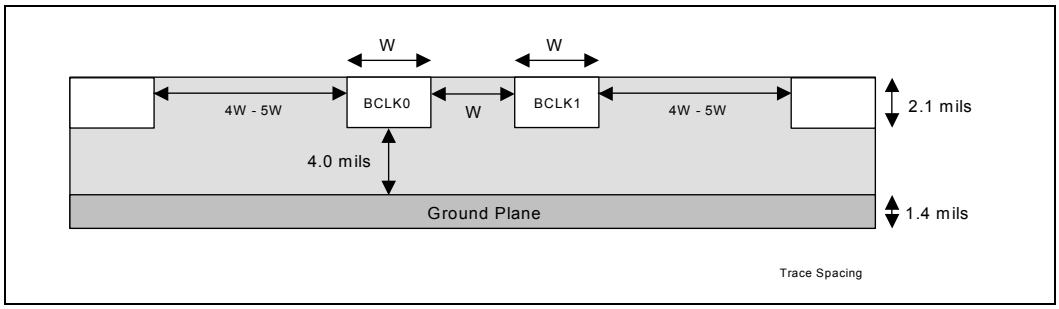


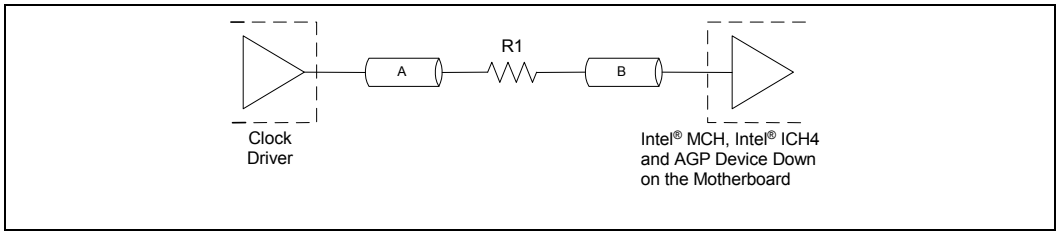

**Figure 11-4. Trace Spacing**




## 11.2.2 CLK66 Clock Group

The driver is the clock synthesizer 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the MCH and the ICH4. If an AGP device is placed down on the motherboard, these guidelines should be used. Note that the goal is to have as little skew as possible between the clocks within this group.

**Figure 11-5. Topology for CLK66**



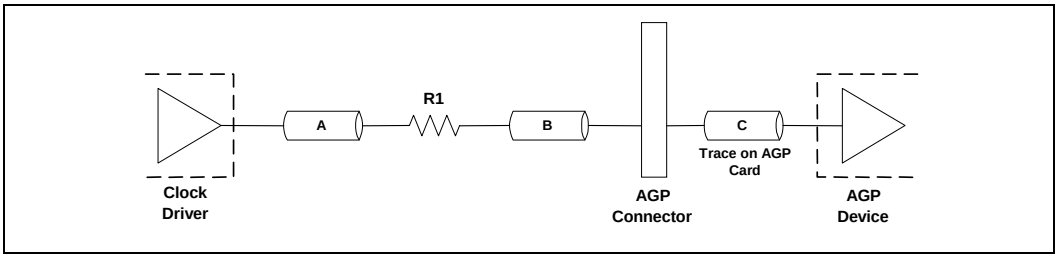
### Table 11-4. CLK66 Routing Guidelines

| Parameter | Routing Guidelines |
|---|---|
| Topology | Point to point |
| Characteristic Trace Impedance (Zo) | 60 Ω ± 15% |
| Trace Width | 5 mils |
| Trace Spacing | 20 mils |
| Spacing to other traces | 20 mils |
| Trace Length–A | 0.00 in. to 0.50 in. |
| Trace Length–B | 4.00 in. to 8.50 in. |
| CLK66 Total Length (A+B) | Matched to ± 100 mils of each other |
| Resistor | R1 = 33 Ω ± 5% |

## 11.2.3 AGPCLK Clock Group

The driver is the clock synthesizer 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the AGP device. Use these guidelines when routing to an AGP connector.

### Figure 11-6. Topology for AGPCLK to AGP Connector




### Table 11-5. AGPCLK Routing Guidelines

| Parameter | Routing Guidelines |
|---|---|
| Topology | Point to point |
| Characteristic Trace Impedance (Zo) | 60 Ω ± 15% |
| Trace Width | 5 mils |
| Trace Spacing | 20 mils |
| Spacing to other traces | 20 mils |
| Trace Length—A | 0.00 in. to 0.50 in. |
| Trace Length—B | (CLK66 Trace B) – 4 in. |
| Trace Length—C | Trace length on AGP add-in card |
| AGPCLK Total Length (A+B) | Must be matched to ± 100 mils of CLK66 Total Length |
| Resistor | R1 = 33 Ω ± 5% |

## 11.2.4 33 MHz Clock Group

The driver is the clock synthesizer 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer at the ICH4, FWH, Glue Chip, SIO, and all PCI devices. The skew between these clocks at their respective devices must be less than 2 ns.

**Figure 11-7. Topology for CLK33 to Intel® ICH4**

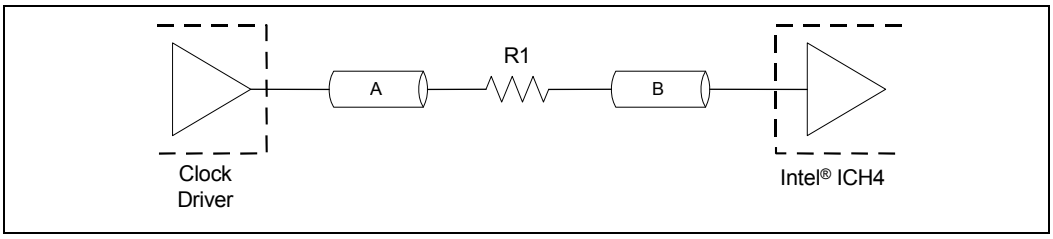



**Figure 11-8. Topology for CLK33 to SIO, Glue Chip, FWH, and PCI Device Down on the Motherboard**

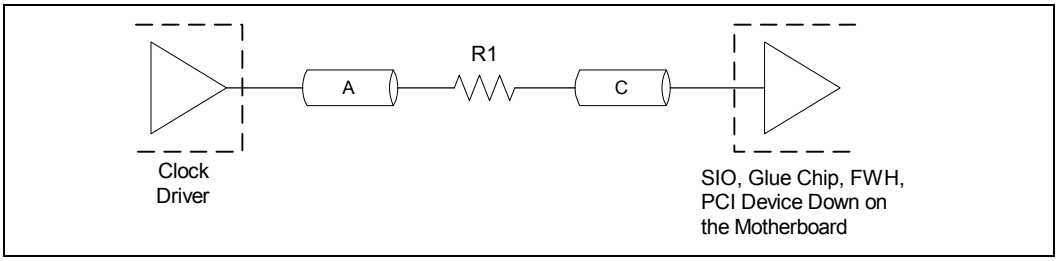
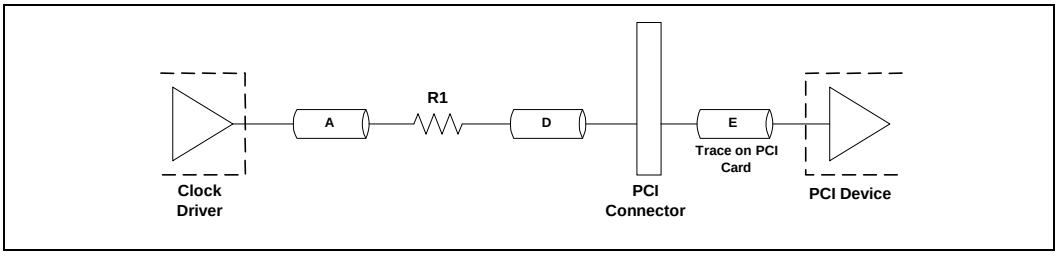



**Figure 11-9. Topology for PCICLK to PCI Connector**



### Table 11-6. 33 MHz Clock Routing Guidelines

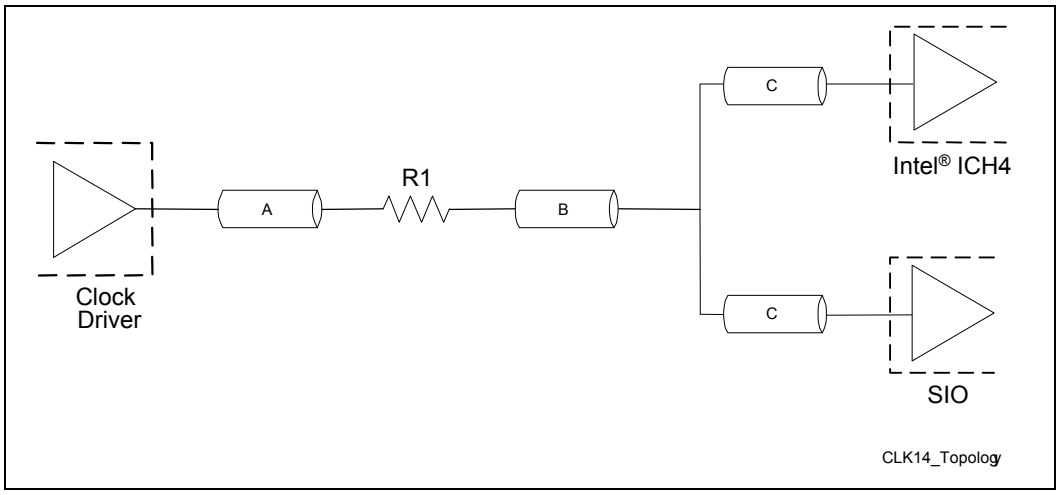
| Parameter | Routing Guidelines |
|---|---|
| Topology | Point to point |
| Characteristic Trace Impedance (Zo) | 60 Ω ± 15% |
| Trace Width | 5 mils |
| Trace Spacing | 15 mils |
| Spacing to other traces | 15 mils |
| Trace Length—A | 0.0 in. to 0.50 in. |
| Total Length (A+B) | Must be matched to ± 100 mils of CLK66 Total Length. See Note 1 |
| Total Length (A+C) | See Note 2 |
| Total Length (A+D+E) | See Note 2 |
| Resistor | R1 = 33 Ω ± 5% |

**NOTES:**
1. The 33 MHz clock **must always** lag the 66 MHz clock at the ICH4 by 1–4 ns. The clock generator guarantees this phase offset. There is no need to intentionally add trace length to the 33 MHz clock. This length-matching requirement applies to the 33 MHz ICH4 clock only.
2. There should be no more than 7.5 inches of total mismatch between any two clocks in this group. If routing to a PCI connector, a 2.6 inch max trace length is assumed on the PCI card. These 2.6 inches must be included in the 7.5 inch total mismatch.

## 11.2.5 CLK14 Clock Group

The driver is the clock synthesizer 14.318 MHz clock output buffer, and the receiver is the 14.318 MHz clock input buffer at the ICH4 and SIO. Note that the clocks within this group should have minimal skew (~ 0) between each other. However, each clock in this group is asynchronous to clocks in other groups.

### Figure 11-10. Topology for CLK14



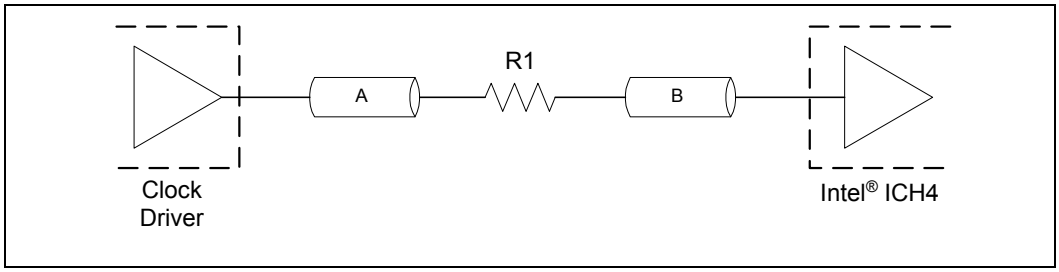
### Table 11-7. CLK14 Routing Guidelines

| Parameter | Routing Guidelines |
|---|---|
| Topology | Balanced T topology |
| Characteristic Trace Impedance (Zo) | 60 Ω ± 15% |
| Trace Width | 5 mils |
| Trace Spacing | 10 mils |
| Spacing to other traces | 10 mils |
| Trace Length—A | 0.00 in. to 0.50 in. |
| Trace Length—B | 0.00 in. to 12 in. |
| Trace Length—C | 0.00 in. to 6 in. |
| CLK14 Total Length (A+B+C) | Matched to ± 0.5 in. of each other |
| Resistor | R1 = 33 Ω ± 5% |

## 11.2.6 USBCLK Clock Group

The driver is the clock synthesizer USB clock output buffer, and the receiver is the USB clock input buffer at the ICH4. Note that this clock is asynchronous to other clocks on the board.

### Figure 11-11. Topology for USB_CLOCK




### Table 11-8. USBCLK Routing Guidelines

| Parameter | Routing Guidelines |
|---|---|
| Topology | Point to point |
| Characteristic Trace Impedance (Zo) | 60 Ω ± 15% |
| Trace Width | 5 mils |
| Spacing to other traces | 15 mils |
| Trace Length—A | 0.00 in.—0.50 in. |
| Trace Length—B | 3.00 in.—12.00 in. |
| Resistor | R1 = 33 Ω ± 5% |
| Skew Requirements | None—USBCLK is asynchronous to any other clock on the board |

## 11.3 Clock Driver Decoupling

The decoupling requirements for a CK_408 compliant clock synthesizer are as follows:

- One 10 µF bulk decoupling capacitor in a 1206 package placed close to the Vdd generation circuitry.
- Six 0.1 µF high-frequency decoupling capacitors in a 0603 package placed close to the Vdd pins on the Clock driver.
- Three 0.01 µF high-frequency decoupling capacitors in a 0603 package placed close to the VddA pins on the Clock driver.
- One 10 µF bulk decoupling capacitor in a 1206 package placed close to the VddA generation circuitry.

# 12 Platform Power Guidelines

## 12.1 Definitions

*Suspend-To-RAM (STR)*
In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered.

*Full-power Operation*
During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state, and the S1 (processor stop-grant state) state.

*Suspend Operation*
During *suspend* operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3), and Soft-off (S5).

*Power Rails*
An ATX 12 V power supply has 6 power rails: +5 V, -5 V, +12 V, -12 V, +3.3 V, 5 VSB. In addition to these power rails from the power supply, several other power rails are created with voltage regulators.

*Core Power Rail*
A power rail that is only on during *full-power* operation. These power rails are on when the PS_ON signal is asserted to the ATX power supply. The core power rails are distributed directly from the ATX 12 V power supply are +5 V, -5 V, +12 V, -12 V, +3.3 V.

*Standby Power Rail*
A power rail that is on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times when the power supply is plugged into AC power. The only standby power rail that is distributed *directly* from the ATX power supply is $5V_{SB}$ (5 V Standby). There are other standby rails that are created with voltage regulators on the board.

*Derived Power Rail*
A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, $3.3V_{SB}$ is usually derived on the motherboard from $5V_{SB}$ using a voltage regulator.

*Dual Power Rail*
A *dual* power rail is derived from different rails at different times depending on the power state of the system. Usually a dual power rail is derived from a *standby supply* during *suspend* operation, and derived from a *core supply* during *full-power* operation. Note that the voltage on a *dual* power rail may be misleading.

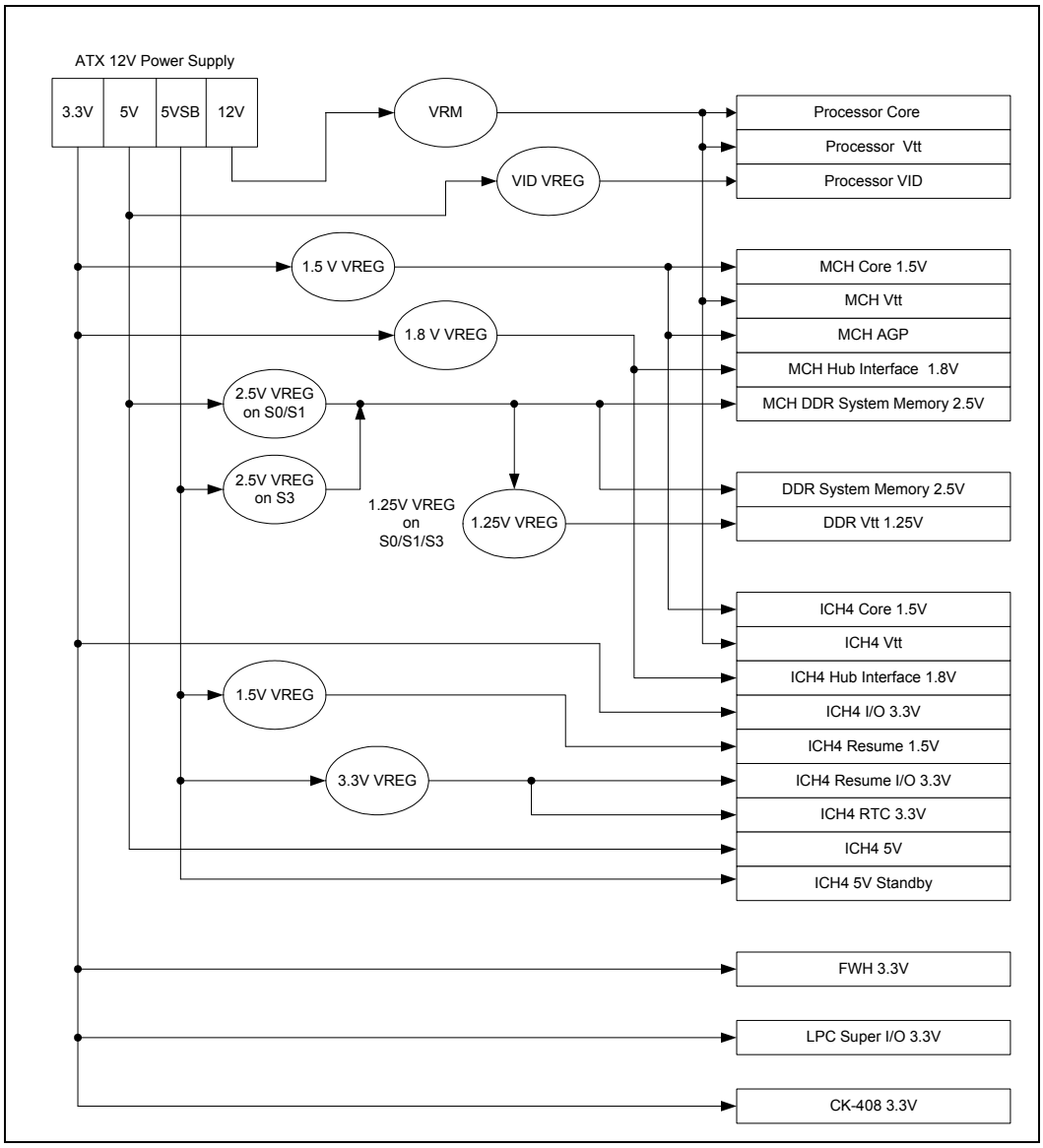
## 12.2 Power Delivery Map

The following figure shows the power delivery architecture for an example 845E Chipset platform. This power delivery architecture supports the “Instantly Available PC Design Guidelines”.

During STR, only the necessary devices are powered. These devices include: main memory, the ICH4 resume well, PCI wake devices (via 3.3 Vaux), AC’97, and USB. To ensure that enough power is available during STR, a thorough power budget should be completed. The power requirements should include each device’s power requirements, both in suspend and in full-power. The power requirements should be compared with the power budget supplied by the power supply. Due to the requirements of main memory and the PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create dual power rails.

The solutions in this Design Guide are only examples. Many power distribution methods achieve similar results. When deviating from these examples, it is critical to consider the effect of a change.

**Figure 12-1. Intel® 845E Chipset Platform Using DDR-SDRAM System Memory Power Delivery Map**



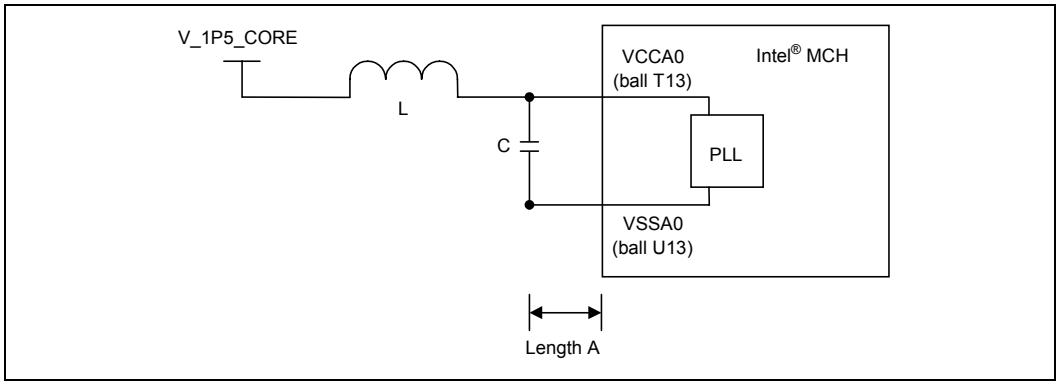

## 12.3 MCH Power Delivery

There are no MCH power sequencing requirements. All MCH power rails should be stable before deasserting reset, but the power can be brought up in any order desired. Good design practice would have all power rails come up as close in time as practical.

### 12.3.1 MCH PLL Power Delivery

VCCA1 and VSSA1, and VCCA0 and VSSA0 are power sources required by the MCH's PLL clock generators.

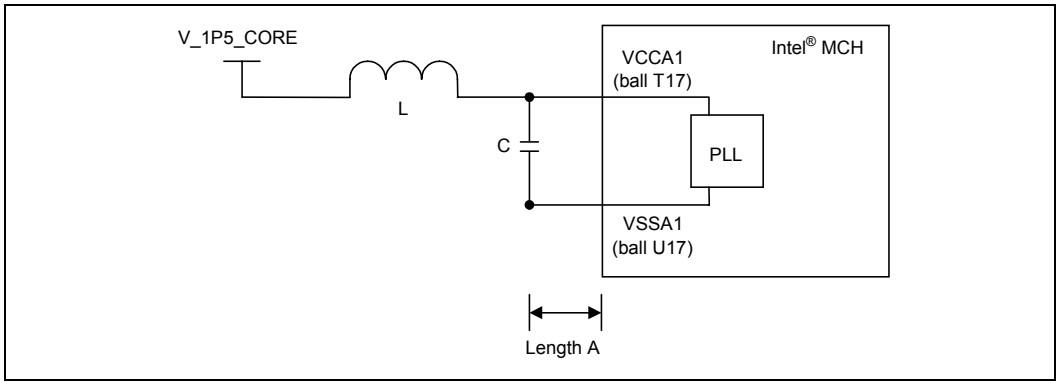
### Figure 12-2. Intel® 845E Chipset PLL0 Filter




### Table 12-1. PLL0 Filter Routing Guidelines

| Parameter | Routing Guidelines |
|---|---|
| Trace Width | 5 mils |
| Trace Spacing | 10 mils |
| Trace Length—A | 1.5 in. |
| Capacitor—C | 33 µF |
| Inductor—L | 4.7 µH |

### Figure 12-3. Intel® 845E Chipset PLL1 Filter




### Table 12-2. PLL1 Routing Guidelines

| Parameter | Routing Guidelines |
|---|---|
| Trace Width | 5 mils |
| Trace Spacing | 10 mils |
| Trace Length—A | 1.5 in. |
| Capacitor—C | 33 µF |
| Inductor—L | 4.7 µH |

**Table 12-3. Recommended Inductor Components for MCH PLL Filter**

| Value | Tolerance | SRF | Rated I | DCR |
|---|---|---|---|---|
| 4.7 µH | 10% | 35 MHz | 30 mA | 0.56 Ω (1Ω max) |
| 4.7 µH | 10% | 47 MHz | 30 mA | 0.7 Ω (± 50%) |
| 4.7 µH | 30% | 35 MHz | 30 mA | 0.3 Ω max |

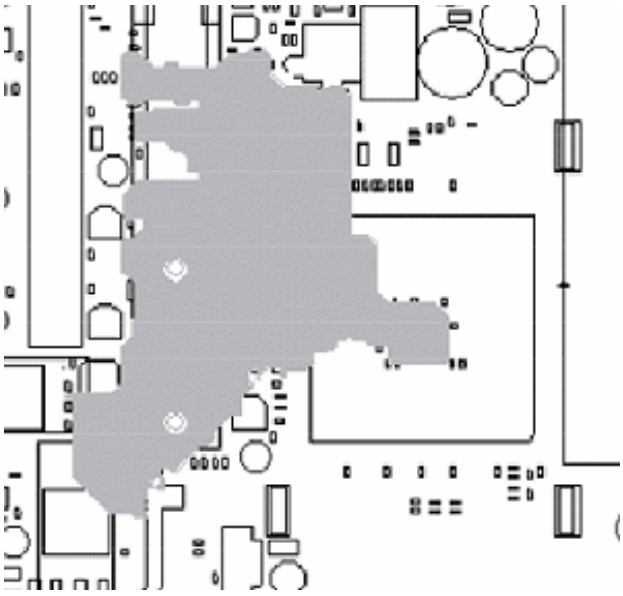
**Table 12-4. Recommended Capacitor Components for MCH PLL Filter**

| Value | ESL | ESR |
|---|---|---|
| 33 µF | 2.5 nH | 0.225 Ω |
| 33 µF | 2.5 nH | 0.2 Ω |

## 12.3.2 MCH 1.5 V Power Delivery

The MCH core and AGP I/O is supplied by 1.5 V. Adequate high-frequency decoupling is needed to ensure one does not adversely impact the other.

**Figure 12-4. 1.5 V Power Plane—Board View**



### 12.3.3 MCH 1.5 V Decoupling

The following minimum decoupling components are recommended:

- Six 0.1 µF ceramic capacitor, 603 body type, X7R dielectric
- Two 10 µF ceramic capacitor, 1206 body type, X7R dielectric
- Two 100 µF electrolytic capacitor

It is recommended that low ESL ceramic capacitors, such as 0603 body types, X7R dielectric, be used. The designer should evenly distribute placement of decoupling capacitors among the AGP interface signal field, and place them as close to the MCH as possible (no further than 0.25 in. from the MCH VCC1_5 ball in the AGP ball field). Figure 12-5 shows an example placement of 1.5 V decoupling capacitors.

**Figure 12-5. MCH 1.5 V Core and 1.5 V AGP I/O Decoupling Placement**

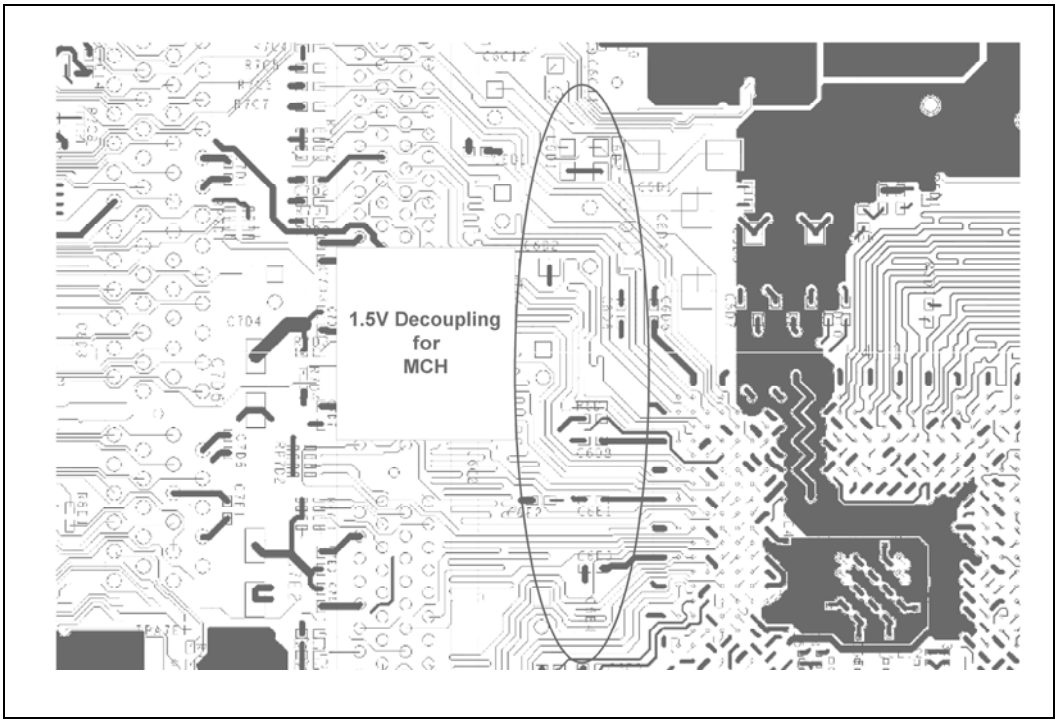
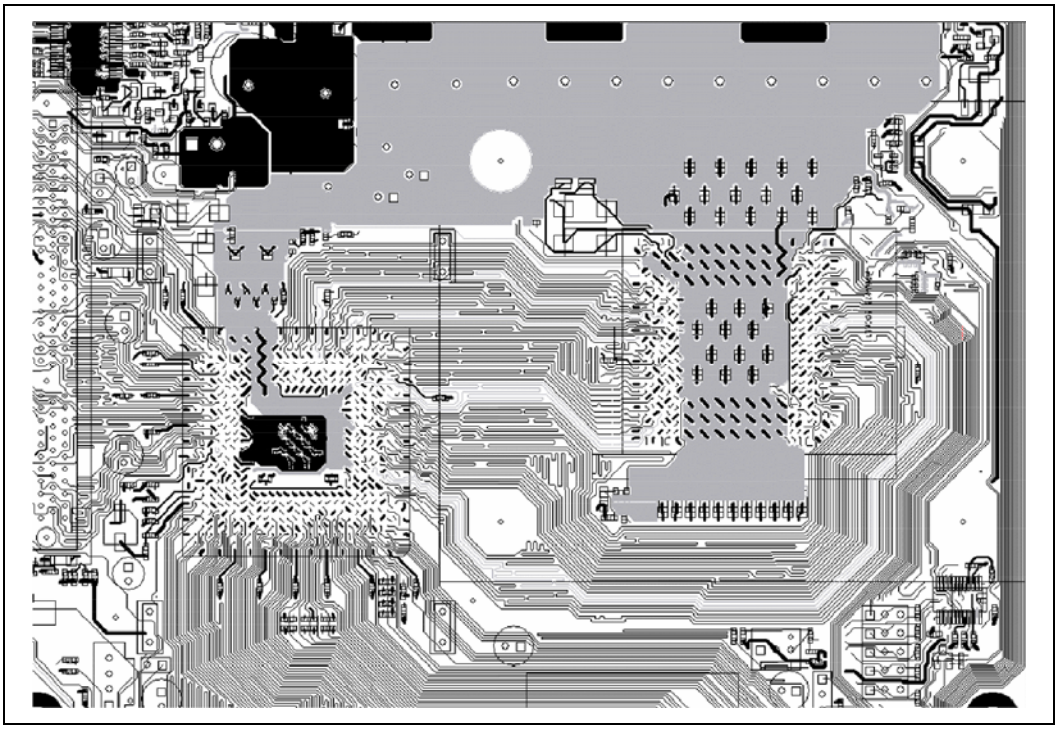


Figure 12-6. VTT Power Plane—Processor and MCH



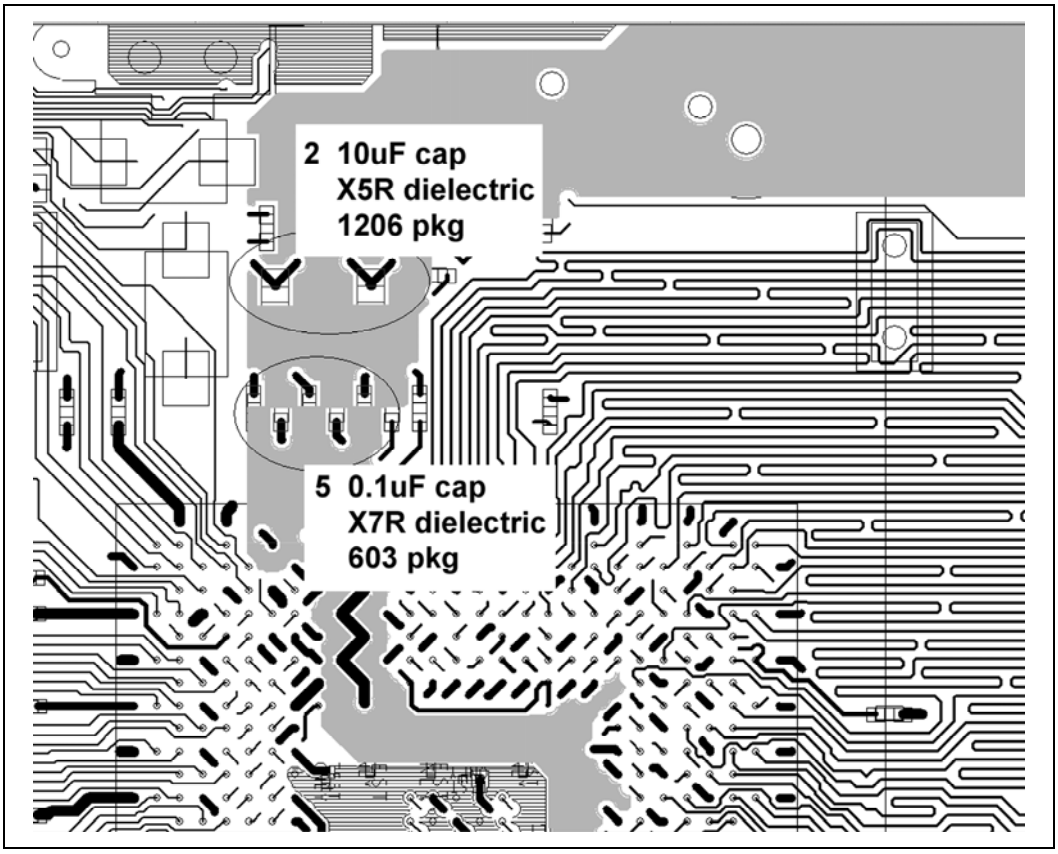
## 12.3.4 MCH VTT Decoupling

The following minimum decoupling components are recommended:

- Two 10 µF ceramic capacitor, 1206 body type, X5R dielectric
- Five0.1 µF ceramic capacitor, 1206 type, X7R dielectric

The alternating polarity of the five 0.1 µF capacitors minimizes the area reduction caused by the vias.

Figure 12-7. VTT Power Plane at MCH—VTT Decoupling at MCH




# 12.4 Intel® ICH4 Power Delivery and Decoupling

## 12.4.1 Power Sequencing

### 12.4.1.1 1.5 V/1.8 V/3.3 V Power Sequencing

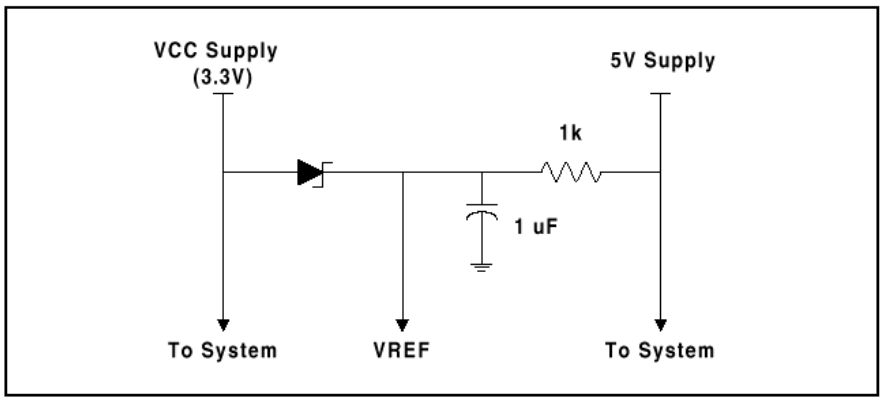
There is no power sequencing requirements for the ICH4 1.5 V core, 1.8 V Hub Interface, and 3.3 V I/O. It is generally good design practice to power core up as closely to the other rails as possible.

### 12.4.1.2 3.3 V/V5REF Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH4. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0.7 V. It must also power down after or simultaneous to VCC3_3. These rules must be followed in order to ensure the safety of the Intel ICH4. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 12-8 shows a sample implementation of how to satisfy the V5REF/ 3.3 V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the $V_{CCSUS3\_3}$ rail is derived from the $V_{CCSUS5}$ rail and therefore, the $V_{CCSUS3\_3}$ rail will always come up after the $V_{CCSUS5}$ rail. As a result, $V_{5REF\_SUS}$ will always be powered up before $V_{CCSUS3\_3}$. In platforms that do not derive the $V_{CCSUS3\_3}$ rail from the $V_{CCSUS5}$ rail, this rule must be comprehended in the platform design.

**Figure 12-8. Example $V_{5REF}$ / 3.3 V Sequencing Circuitry**




### 12.4.1.3 Power Supply PS_ON Consideration

If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10-100mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this issue.

## 12.4.2 Intel® ICH4 Power Delivery

ICH4 Power Delivery is accomplished through layer 1, layer 2, and layer 4.

**Figure 12-9. Intel® ICH4 Layer 1 Power Delivery**

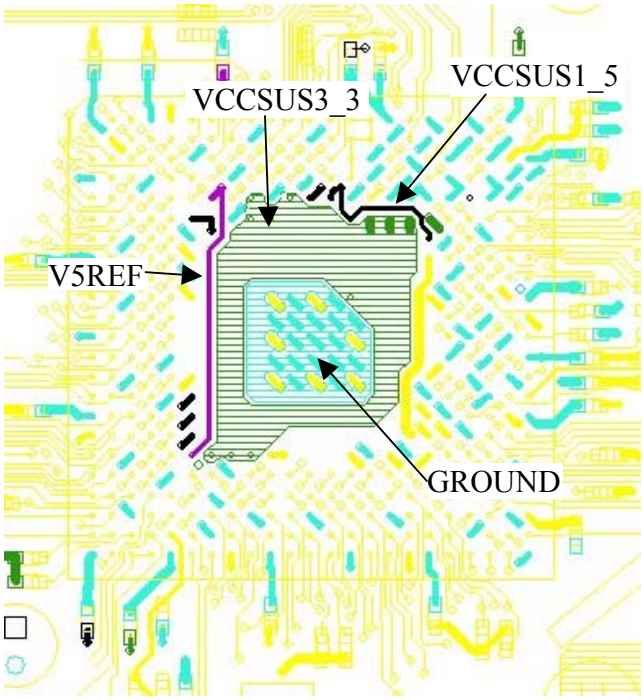
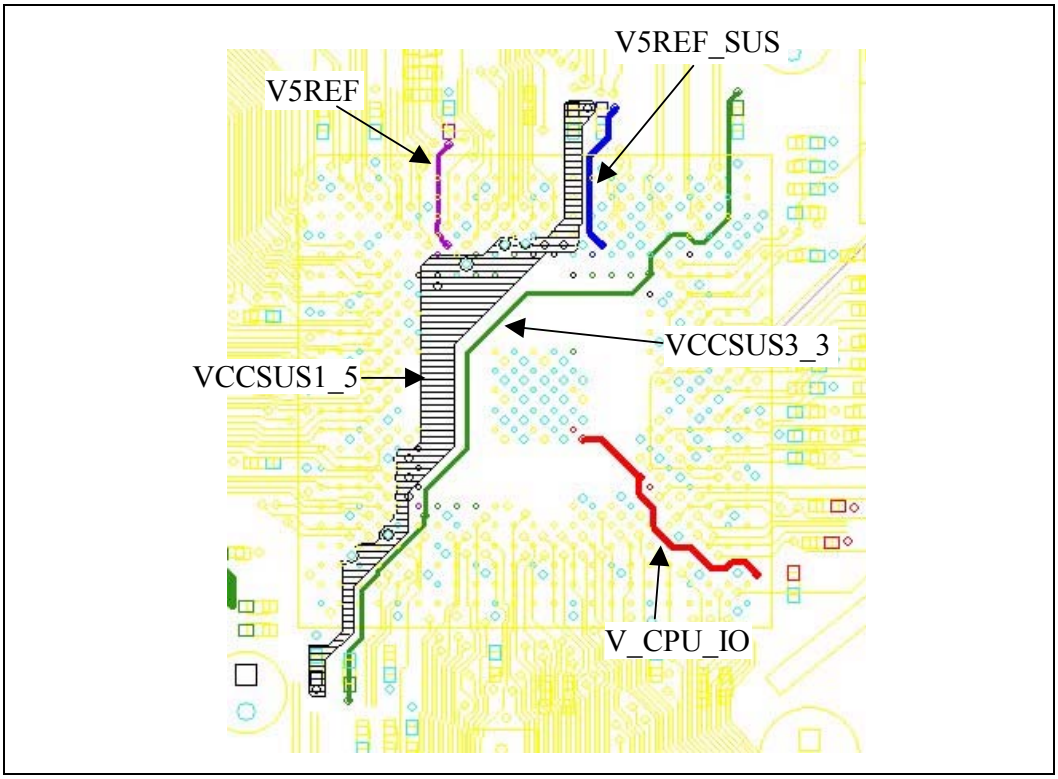


Figure 12-10. Intel® ICH4 Layer 4 Power Delivery




## 12.4.3 Intel® ICH4 Decoupling

Table 12-5. Decoupling Requirements for Intel® ICH4

| Pin | Decoupling Requirements | Decoupling Type (Ball type) | Decoupling Placement |
|---|---|---|---|
| VCC3_3 | (6) 0.1 µF | Decoupling Cap (Vss) | Place near balls: A4, A1, H1, T1, AC10, and AC18 |
| VCCSUS3_3 | (2) 0.1 µF | Decoupling Cap (Vss) | Place near balls: A22 and AC5 |
| V_CPU_IO | (1) 0.1 µF | Decoupling Cap (Vcc) | Place near ball: AA23 |
| VCC1_5 | (2) 0.1 µF | Decoupling Cap (Vss) | Place near balls: K23 and C23 |
| VCCSUS1_5 | (2) 0.1 µF | Decoupling Cap (Vss) | Place near balls: A16 and AC1 |
| V5REF | (1) 0.1 µF | Decoupling Cap (Vcc) | Place near ball: E7 |
| V5_REF_SUS | (1) 0.1 µF | Decoupling Cap (Vss) | Place near ball: A16 |
| VCCRTC | (1) 0.1 µF | Decoupling Cap (Vcc) | Place near ball: AB5 |
| VCCHI | (2) 0.1 µF | Decoupling Cap (Vss) | Place near balls: T23 and N23 |
| VCCPLL | (1) 0.1µF<br>(1) 0.01µF | Decoupling Cap (Vcc) | Place near ball: C22 |

***Note:*** Capacitors should be placed less than 100 mils from the package.

## 12.5 CK_408 Power Delivery

### Differential Routing

- The host clock pairs must be routed differentially and on the same physical routing layer.
- DO NOT split the two halves of a differential clock pair. Route them referenced to ground for the entire length.
- The differential clock must have no more than two via transitions.

### Isolation

- Special care must be taken to provide a quiet VddA supply to the Ref Vdd, VddA, and the 48 MHz Vdd.
- These VddA signals are especially sensitive to switching noise induced by the other Vdds on the clock chip.
- The VddA signals are also sensitive to switching noise generated elsewhere in the system such as CPU VRM. The LC Pie filter should be designed to provide the best reasonable isolation.

### Referencing

- Ground referencing is strongly recommended for all platform clocks.
- Motherboard layer transitions and power plane split crossing must be kept to a minimum.

### Flooding

***Option 1 (Signal-Power-Ground-Signal)***

For the stack up shown in Figure 3-2 (Signal-Power-Ground-Signal), it is strongly recommended that:

- A solid ground flood be placed on layer 1 (signal layer) inside the part pads.
- A solid 3.3 V Power plane be present on layer 2 (power layer).
- A solid ground plane be present on layer 3 (ground layer).
- Signals after termination should via to the backside to be ground referenced.
- Here the host clocks will be power referenced for a small portion of time while they route from CK_408 pin to their transition via.
- Keep this MB length as short as possible.

***Option 2 (Signal-Ground-Power-Signal)***

If using a stack up such as **Signal-Ground-Power-Signal**, It is **strongly recommended** that:

- A ground flood be present on layer1 (signal layer) inside the part pads.
- A solid ground plane be present on layer 2 (ground layer).
- A solid 3.3 V Power plane be present on layer 3 (power layer).
- Signals after termination should remain on the top layer to be ground referenced (via to the front side).

## Decoupling

- For ALL power connections to planes, decoupling capacitors, and vias, the MAXIMUM trace width allowable and shortest possible lengths should be used to ensure the lowest possible inductance.
- The decoupling capacitors should be connected as shown in Figure 12-12, taking care to connect the Vdd pins directly to the Vdd side of the capacitors.
- The VSS pins should not be connected directly to the VSS side of the capacitors. They should be connected to the ground flood under the part that is viaed to the ground plane to avoid Vdd glitches propagating out and getting coupled through the decoupling capacitors to the VSS pins. This method has been shown to provide the best clock performance.
- The ground flood should be via'd through to the ground plane with no less than 12–16 vias under the part. It should be well connected.
- For all power connections, heavy duty and/or dual vias should be used.
- It is imperative that the standard signal vias and small traces not be used for connecting decoupling capacitors and ground floods to the power and ground planes.
- VddA should be generated by using an LC filter. This VddA should be connected to the Vdd side of the three capacitors that require it using a hefty trace on the top layer. This trace should be routed from the LC filter.

## 12.5.1 CK_408 Power Sequencing

Platforms need proper power sequencing of the CK_408 with respect to the voltage regulators, processor, and MCH. Figure 12-11 is a schematic showing the relationship between the VCCVID voltage regulator, the VCCP voltage regulator, CK_408, processor, and MCH.

**Figure 12-11. CK_408 Schematic**

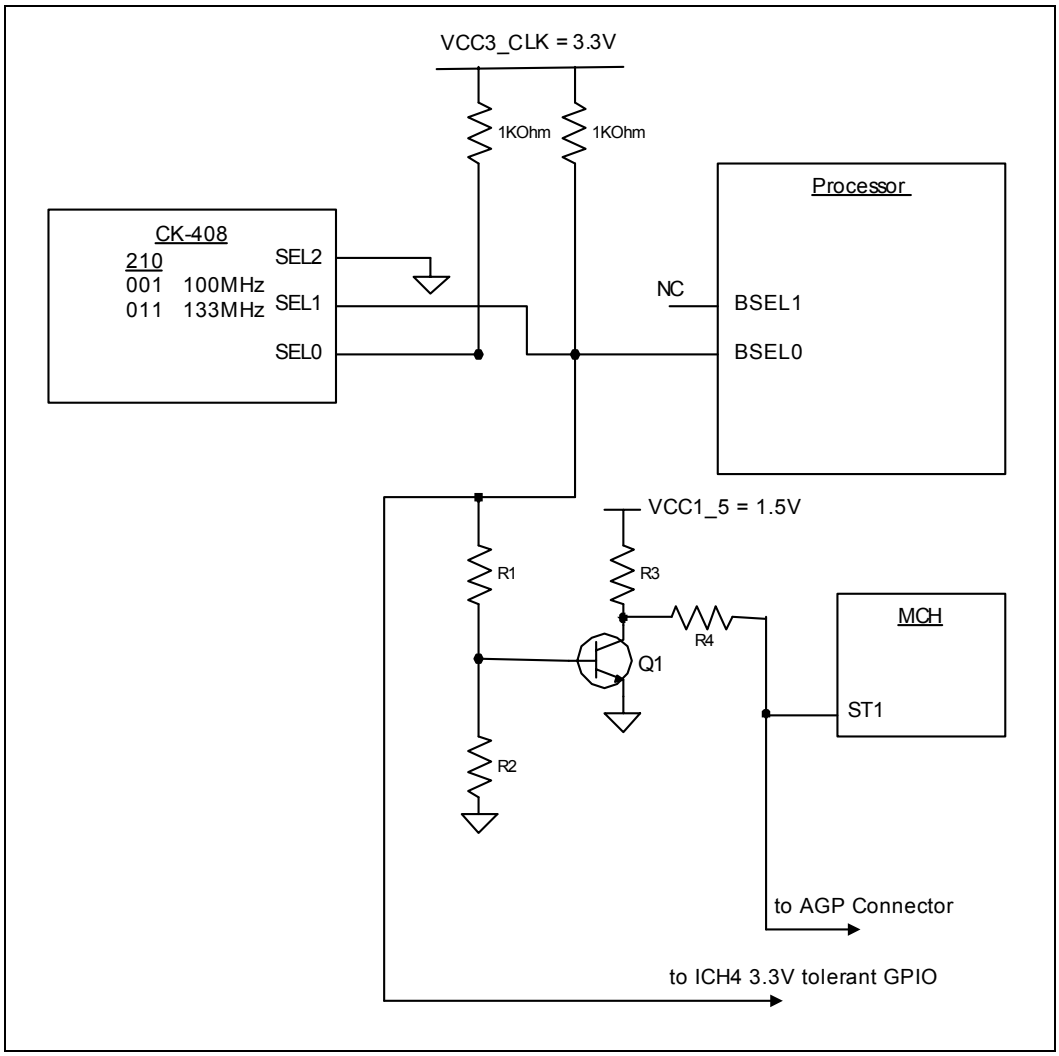



**Table 12-6. PLL1 Routing Guidelines**

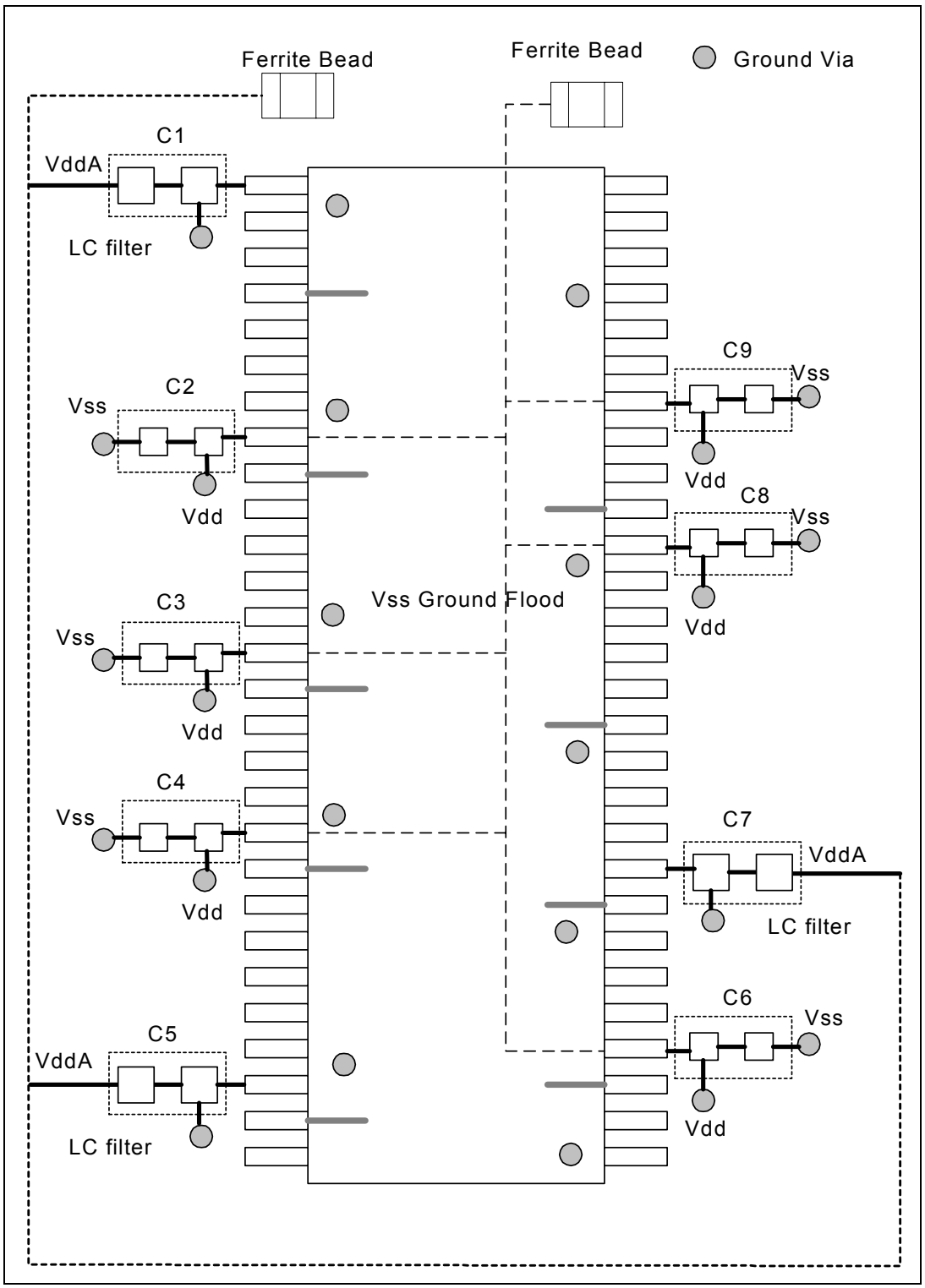
| Parameter | Routing Guidelines |
|---|---|
| Resistor—R1 | 1.5 kΩ |
| Resistor—R2 | 1.5 kΩ |
| Resistor—R3 | 1 kΩ |
| Resistor—R4 | 1 kΩ |

### 12.5.2 CK_408 Decoupling

The decoupling requirements for a CK_408 compliant clock synthesizer are as follows:

- One 10 µF bulk-decoupling capacitor in a 1206 package placed close to the Vdd generation circuitry.
- Six 0.1 µF high-frequency decoupling capacitors in a 0603 package placed close to the Vdd pins on the clock driver.
- Three 0.01 µF high-frequency decoupling capacitors in a 0603 package placed close to the VddA pins on the clock driver.
- One 10 µF bulk decoupling capacitor in a 1206 package placed close to the VddA generation circuitry.

**Figure 12-12. Decoupling Capacitors Placement and Connectivity**



# 13 Platform Mechanical Guidelines

## 13.1 MCH Retention Mechanism and Keepouts

Figure 13-1 shows the motherboard keepout dimensions intended for the reference thermal / mechanical components for the 845E chipset.

**Figure 13-1. MCH Retention Mechanism and Keepout Drawing**

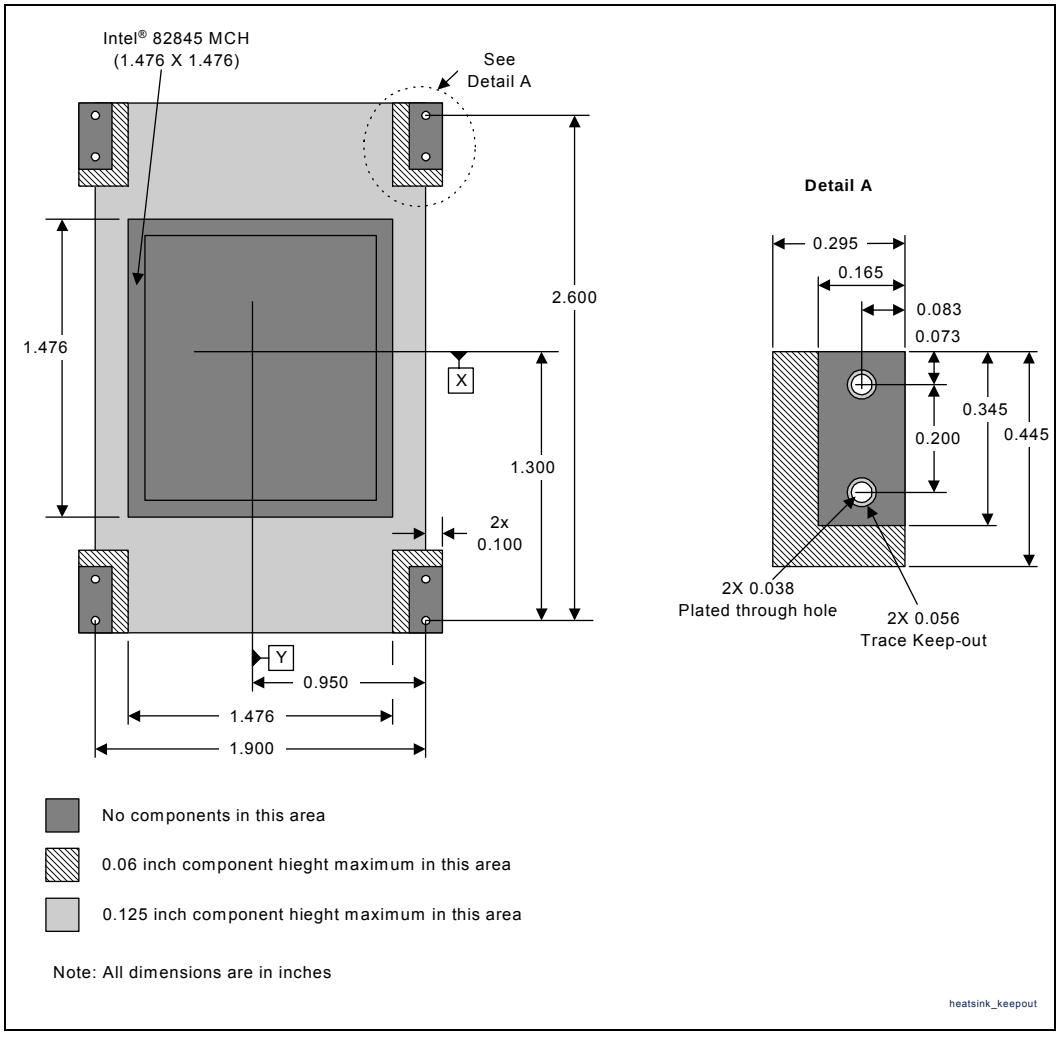
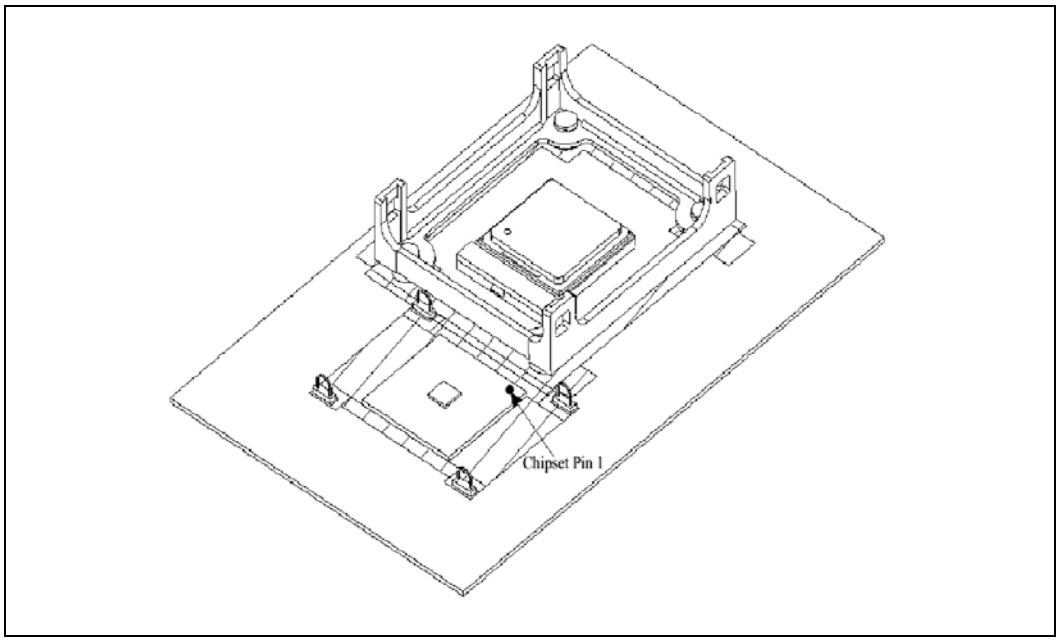


Figure 13-2 shows a typical orientation of the 845E chipset keepout relative to the Pentium 4 processor. The 845E chipset mechanical reference design assumes this orientation, or a rotation of 180 degrees of the chipset relative to the orientation shown in this figure. Intel will not qualify other orientations.

**Figure 13-2. Typical Orientation of the Chipset Relative to the Processor**



# 14 Schematic Checklist

## 14.1 Host Interface

| Signal | Description | ✓ |
|---|---|---|
| **PROCESSOR/ MCH Signals** | | |
| A[31:3]# | • Connect to HA[31:3] pins on MCH. | |
| ADS# | • Connect to the associated pin on the MCH. | |
| ADSTB[1:0]# | • Connect to HADSTB[1:0]# pins on MCH. | |
| BNR# | • Connect to the associated pin on the MCH. | |
| BPRI# | • Connect to the associated pin on the MCH. | |
| BR0# | • Connect to the associated pin on the MCH.<br>• Terminate to VCC_CPU through a 51 Ω ± 5% resistor near the processor. | |
| RESET# | • Connect to the associated pin on the MCH.<br>• Terminate to VCC_CPU through a 51Ω ± 5% resistor near the processor. | |
| D[63:0]# | • Connect to HD[63:0] pins on MCH. | |
| DBI[3:0]# | • Connect to the associated pin on the MCH. | |
| DBSY# | • Connect to the associated pin on the MCH. | |
| DEFER# | • Connect to the associated pin on the MCH. | |
| DRDY# | • Connect to the associated pin on the MCH. | |
| DSTBN[3:0]# | • Connect to HDSTBN[3:0]# pins on MCH. | |
| DSTBP[3:0]# | • Connect to HDSTBP[3:0]# pins on MCH. | |
| HIT# | • Connect to the associated pin on the MCH. | |
| HITM# | • Connect to the associated pin on the MCH. | |
| LOCK# | • Connect to HLOCK# pin on MCH. | |
| REQ[4:0]# | • Connect to HREQ[4:0]# pins on MCH. | |
| RS[2:0]# | • Connect to the associated pin on the MCH. | |
| TRDY# | • Connect to HTRDY# pin on MCH. | |

| Signal | Description | ✓ |
|---|---|---|
| **Processor/ Intel® ICH4 Signals** | | |
| A20M# | • Connect to the associated pin on the ICH4 (No extra pull-up resistors required). | |
| CPUSLP# | • Connect to the associated pin on the ICH4 (No extra pull-up resistors required). | |
| FERR# | • Connect to the associated pin on the ICH4.<br>• Terminate to VCC_CPU through a 62 Ω ± 5% resistor near the processor. | |
| IGNNE# | • Connect to the associated pin on the ICH4 (No extra pull-up resistors required). | |
| INIT# | • Connect to the associated pin on the ICH4 (No extra pull-up resistors required).<br>• A voltage translator is required for FWH.<br>• Connect to Firmware Hub. | |
| INTR | • Connect to the associated pin on the ICH4 (No extra pull-up resistors required). | |
| LINT[1:0] | • LINT1 connects to ICH4 NMI (No extra pull-up resistors required).<br>• LINT0 connects to ICH4 INTR (No extra pull-up resistors required). | |
| NMI | • Connect to the associated pin on the ICH4 (No extra pull-up resistors required). | |
| PWRGOOD | • Connects to ICH4 CPUPWRGD pin (Weak external pull-up resistor required).<br>• Terminate to VCC_CPU through a 300 Ω ± 5% resistor. | |
| SLP# | • Connect to the associated pin on the ICH4 (No extra pull-up resistors required). | |
| SMI# | • Connect to the associated pin on the ICH4 (No extra pull-up resistors required). | |
| STPCLK# | • Connect to the associated pin on the ICH4 (No extra pull-up resistors required) | |
| **PROCESSOR Only Signals** | | |
| A[35:32]# | • No Connect. | |
| AP[1:0]# | • No Connect. | |
| BCLK[1:0] | • Connect to CK_408.<br>• Connect 20—33 Ω series resistors to each clock signal.<br>• Connect a 49.9 Ω ± 1% shunt source termination (Rt) resistor to GND for each signal on the processor side of the series resistor (50 Ω motherboard impedance). | |
| BPM[5:0]# | • These signals should be terminated with a 51 Ω ± 5% resistor to VCC_CPU near the processor. If a debug port is implemented termination is required near the debug port as well. Refer to the *ITP700 Debug Port Design Guide* for further information. | |
| BINIT# | • No Connect. | |

| Signal | Description | ✓ |
|---|---|---|
| BSEL[1:0] | • Connect to CK_408. Connect BSEL0 to MCH ST1 through resistor divider and transistor circuit.<br>• Terminate to CK_408 3.3 V supply through a 1 kΩ resistor. | |
| COMP[1:0] | • Terminate to GND through a 51.1 Ω ± 1% resistor.<br>• Minimize the distance from termination resistor and processor pin. | |
| DBR# | • Refer to the *ITP700 Debug Port Design Guide* for further information. | |
| DP[3:0]# | • No Connect. | |
| IERR# | • Terminate to VCC_CPU through a 62 Ω ± 5% resistor near the processor. | |
| GTLREF[3:0] | • Terminate to VCC_CPU through a 49.9 Ω ± 1% resistor.<br>• Terminate to GND through a 100 Ω ± 1% resistor.<br>• Should be 2/3 VCC_CPU. | |
| ITP_CLK0 | • Refer to the *ITP700 Debug Port Design Guide* for further information. | |
| ITP_CLK1 | • Refer to the *ITP700 Debug Port Design Guide* for further information. | |
| MCERR# | • No Connect. | |
| PROCHOT# | • Terminate to VCC_CPU though a 62 Ω ± 1% resistor near the processor. | |
| RSP# | • No Connect. | |
| SKTOCC# | • Connect to Glue Chip / Discrete Logic (If pin is used). | |
| TCK | • Refer to the *ITP700 Debug Port Design Guide* for further information. | |
| TDI | • Refer to the *ITP700 Debug Port Design Guide* for further information. | |
| TDO | • Refer to the *ITP700 Debug Port Design Guide* for further information. | |
| TESTHI | • Refer to Section 4.3.1.11 | |
| THERMTRIP# | • Terminate to VCC_CPU through a 62 Ω ± 5% resistor near the processor. | |
| THERMDA | • Connect to thermal monitor circuitry if used. | |
| THERMDC | • Connect to thermal monitor circuitry if used. | |
| TMS | • Refer to the *ITP700 Debug Port Design Guide* for further information. | |
| TRST# | • Refer to the *ITP700 Debug Port Design Guide* for further information. | |
| VCCA | • Connect with isolated power circuitry to VCC_CPU. | |
| VCCIOPLL | • Connect with isolated power circuitry to VCC_CPU. | |
| VCCSENSE | • Leave as no-connect. | |
| VCCVID | • Connect to 1.2 V linear regulator. | |
| VID[4:0] | • Connect to VR or VRM. These signals must be pulled up to 3.3 V through either 1 kΩ pull-ups on the motherboard or with internal pull-ups in the VR or VRM. | |
| VSSA | • Connect with isolated power circuitry to VCC_CPU. | |
| VSSSENSE | • Leave as no-connect. | |

| Signal | Description | ✓ |
|---|---|---|
| | **MCH Signals Only** | |
| HRCOMP[1:0] | • Pull-down to GND through a 24.9Ω ±1% resistor. | |
| HSWNG[1:0] | • Connect voltage divider circuit to VTT through a 300 Ω ± 1% pull-up resistor and to GND through a 150 Ω ± 1% pull-down resistor.<br>• Decouple the voltage divider with a 0.01 µF capacitor to GND. | |
| HVREF | • Connect voltage divider circuit to VCC_CPU through a 49.9 Ω ± 1% pull-up resistor and to GND through a 100 Ω ± 1% pull-down resistor<br>Decouple the voltage divider with a 0.1 µF capacitor. | |
| VTT | • Connect to VCC_CPU power supply. | |

## 14.2 Memory Interface

### 14.2.1 DDR SDRAM

| Signal | Description | ✓ |
|---|---|---|
| | **MCH/DIMM Signals** | |
| SBS[1:0] | • Connect to BA[1:0] pin on each DIMM<br>• Terminate to VTT through a parallel 56Ω ±5% resistor | |
| SCAS# | • Connect to CAS# pin on each DIMM<br>• Terminate to VTT through a parallel 56Ω ±5% resistor | |
| SCB[7:0] | • Connect to CB[7:0] pins on each DIMM<br>• Connect to a series 33Ω ±5% resistor and terminate to VTT through a parallel 47Ω ±5% resistor | |
| SCK[2:0] | • Connect to CK[2:0] pins on first DIMM | |
| SCK#[2:0] | • Connect to CK#[2:0] pins on first DIMM | |
| SCK[5:3} | • Connect to CK[2:0] on second DIMM | |
| SCK#[5:3] | • Connect to CK#[2:0] on second DIMM | |
| SCKE[0] | • Connect to pin 21 on first DIMM<br>• Terminate to VTT through a parallel 47Ω ±5% resistor | |
| SCKE[1] | • Connect to pin 111 on first DIMM<br>• Terminate to VTT through a parallel 47Ω ±5% resistor | |
| SCKE[2] | • Connect to pin 21 on second DIMM<br>• Terminate to VTT through a parallel 47Ω ±5% resistor | |
| SCKE[3] | • Connect to pin 111 on second DIMM<br>• Terminate to VTT through a parallel 47Ω ±5% resistor | |
| SCS#[0] | • Connect to pin 157 on first DIMM<br>• Terminate to VTT through a parallel 47Ω ±5% resistor | |

| Signal | Description | ✓ |
|---|---|---|
| SCS#[1] | • Connect to pin 158 on first DIMM<br>• Terminate to VTT through a parallel 47Ω ±5% resistor | |
| SCS#[2] | • Connect to pin 157 on second DIMM<br>• Terminate to VTT through a parallel 47Ω ±5% resistor | |
| SCS#[3] | • Connect to pin 158 on second DIMM<br>• Terminate to VTT through a parallel 47Ω ±5% resistor | |
| SDQ[63:0] | • Connect to DQ[63:0] pins on each DIMM<br>• Connect to a series 33Ω ±5% resistor and terminate to VTT through a parallel 47Ω ±5% resistor | |
| SDQS[8:0] | • Connect to DQS[8:0] pins on each DIMM<br>• Connect to a series 33Ω ±5% resistor and terminate to VTT through a parallel 47Ω ±5% resistor | |
| SMA[12:0] | • Connect to A[12:0] pins on each DIMM<br>• Connect to a series 0Ω resistor and terminate to VTT through a parallel 56Ω ±5% resistor | |
| SRAS# | • Connect to RAS# pin on each DIMM<br>• Connect to a series 0Ω resistor and terminate to VTT through a parallel 56Ω ±5% resistor | |
| SWE# | • Connect to WE# pin on each DIMM<br>• Connect to a series 0Ω resistor and terminate to VTT through a parallel 56Ω ±5% resistor | |
| **MCH Signals Only** | | |
| RCVENOUT# | • Connect directly to MCH RCVENIN# pin | |
| RCVENIN# | • Connect directly to MCH RCVENOUT# pin | |
| RSVD | • No Connect | |
| SDREF | • Connect to DDR Reference Voltage (VREF)<br>• Terminate to ground through a 0.1 µF capacitor | |
| SMRCOMP | • Connect to DDR Termination Voltage (VTT) through a 30Ω ±1% pull-up resistor.<br>• Terminate to GND through a 0.1 µF capacitor<br>• Place the 0.1 µF capacitor on the VTT side of the SMRCOMP 30Ω ±1% pull-up resistor | |
| VCCSM | • Connect to 2.5 V | |
| **DIMM Signals Only** | | |
| A13 | • No Connect | |
| DM[8:0]/DQS[17:9] | • Connect to GND | |
| FETEN | • No Connect | |
| NC | • No Connect | |

| Signal | Description | ✓ |
|---|---|---|
| SA[2:0] | • DIMM0: Connect to GND<br>• DIMM1: Connect SA[2:1] to GND, and Connect SA0 to 2.5 V | |
| SDA | • Connect to I2C_DATA | |
| SCL | • Connect to I2C_CLOCK | |
| VDD | • Connect to 2.5 V | |
| VDDQ | • Connect to 2.5 V | |
| VREF | • Connect to DDR Reference Voltage (VREF)<br>• Terminate to ground through a 0.1 µF capacitor | |
| VSS | • Connect to GND | |
| VDDSPD | • Connect to power (from a minimum of 2.3 V to a maximum of 3.6 V)<br>• Strongly recommend connecting to 2.5 V | |
| VDDID | • No Connect | |

## 14.3 AGP Interface

| Signal | Description | ✓ |
|---|---|---|
| **MCH/ Connector Signals** | | |
| AD_STB[1:0] | • Connect together. | |
| AD_STB[1:0]# | • Connect together. | |
| G_AD[31:0] | • Connect together. | |
| G_C/BE[3:0]# | • Connect together. | |
| G_DEVSEL# | • Connect together. | |
| G_FRAME# | • Connect together. | |
| G_GNT# | • Connect together. | |
| G_IRDY# | • Connect together. | |
| G_PAR | • Connect together. | |
| G_PIPE# | • Connect together. | |
| G_REQ# | • Connect together. | |
| G_STOP# | • Connect together. | |
| G_TRDY# | • Connect together. | |
| INTA# | • Connect together.<br>• Terminate to 3.3 V through a pull-up resistor. | |
| INTB# | • Connect together.<br>• Terminate to 3.3 V through a pull-up resistor. | |
| PIPE# | • Connect together. | |
| RBF# | • Connect together. | |

| Signal | Description | ✓ |
|---|---|---|
| SBA[7:0] | • Connect together. | |
| SB_STB | • Connect together | |
| SB_STB# | • Connect together. | |
| SBA[7:0] | • Connect together. | |
| ST0 | • Connect together.<br>• Use a 2 kΩ pull down resistor to ground. | |
| ST1 | • Connect together.<br>• Site required for pull-down resistor to ground but do not populate. | |
| ST2 | • Connect together. | |
| WBF# | • Connect together. | |
| VCC1_5 | • Connect to 1.5 V power supply. | |
| **CONNECTOR Signals Only** | | |
| 3.3Vaux | • Connect to PCI 3.3VAUX. | |
| 12 V | • Connect to 12 V. | |
| AGPCLK | • Connect to CK_408. | |
| G_PERR# | • Terminate to VDDQ through a 4 kΩ to 16 kΩ resistor (6.8 kΩ resistor value recommended). | |
| G_SERR# | • Terminate to VDDQ through a 4 kΩ to 16 kΩ resistor (6.8 kΩ resistor value recommended). | |
| OVRCNT | • | |
| PCIRST | • Connect to PCI slot PCIRST. | |
| PME# | • Connect to PCI PME#. | |
| TYPEDET# | • Not required. | |
| USB+ | • | |
| USB– | • | |
| VCC | • Connect to VCC3. | |
| VCC5 | • Connect to VCC. | |
| VDDQ | • Connect to V1.5CORE. | |
| VREFCG | • Connect to VREF divider network at the AGP connector. | |
| VREFGC | • Not required. | |
| **MCH Signals Only** | | |
| AGPREF | • Connect to VREFCG pin on connector.<br>• Terminate to ground through a 0.1 μF capacitor at the MCH. | |
| GRCOMP | • Pull-down to GND through a 40.2 Ω ±1% resistor. | |

## 14.4 Hub Interface

| Signal | Description | ✓ |
|---|---|---|
| **MCH/ Intel® ICH4 Signals** | | |
| HI[10:0] | • Connect to HI[10:0] in ICH4 | |
| HI[11] | Leave as No connect | |
| HISTB | • Connect to HISTB in ICH4 | |
| HI_STB# | • Connect to HISTB# in ICH4 | |
| HIREF | • Connect to voltage divider circuit | |
| HI_SWING | • Connect to voltage divider circuit | |
| **MCH Signals Only** | | |
| HI_RCOMP | • Connect to Vss through a 24.9 Ω ± 1% resistor | |
| VCCHI | • Connect to 1.8 V through (2) 0.1 µF decoupling capacitor. | |
| **Intel® ICH4 Signals Only** | | |
| HICOMP | • Terminate to Vss through a 40.2Ω ±1% resistor | |

## 14.5 Intel® ICH4 Interface

| Signal | Description | ✓ |
|---|---|---|
| **Intel® ICH4 / IDE Signals** | | |
| IDERST# | • The PCIRST# signal should be buffered to form the IDERST# signal.<br>• 33 Ω series termination resistor is recommended on this signal. | |
| PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3# | • No extra series termination resistors required.<br>• Pads for series resistors can be implemented should the system designer have signal integrity concerns.<br>• These signals have integrated series resistors<br>• Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω. | |

| Signal | Description | ✓ |
|---|---|---|
| PDD[15:0], SDD[15:0] | • No extra series termination resistors or other pull-ups/pull-downs are required.<br>• PDD7/SDD7 does not require a 10 kΩ pull-down resistor.<br>• Refer to ATA ATAPI-6 specification.<br>• These signals have integrated series resistors<br>• Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω. | |
| PDDREQ,<br>SDREQ | • No extra series termination resistors.<br>• No pull down resistors needed. | |
| PIORDY,<br>SIORDY | • No extra series termination resistors.<br>• Pull-up to $V_{CC}3\_3$ via a 4.7 kΩ resistor.<br>• These signals have integrated series resistors in the Intel ICH4. | |
| IRQ14, IRQ15 | • Recommend 8.2 kΩ—10 kΩ pull-up resistors to $V_{CC}3\_3$.<br>• No extra series termination resistors.<br>• Open drain outputs from drive. | |
| Cable Detect: | **Host Side/Device Side Detection (*recommended method*):**<br>Connect IDE pin PDIAG#/CBLID to an ICH4 GPIO pin. Connect a 10 kΩ resistor to terminate to GND on the signal line.<br>**Device side detection:**<br>Connect a 0.047 µF capacitor from IDE pin PDIAG#/CBLID to terminate to GND. No ICH4 connection. | |
| **ICH4 / AC'97 Signals** | | |
| AC_SDOUT | • Requires a jumper to 8.2 kΩ Pull Up resistor. Should not be stuffed for default operation.<br>• Series termination resistor 0 Ω to 47 Ω to on board codec and to the CNR | |
| AC_SDIN[1], AC_SDIN[0] | • Internal pull-downs in ICH4; no external pull-downs required.<br>• Series termination resistor 0 Ω to 47 Ω from the AC_SDIN lines to the ICH4 | |
| AC_SDIN[2] | • Requires a 10K pull-down to ground if a CNR card is used on the platform.<br>• Series termination resistor 33Ω to 47Ω from the AC_SDIN lines to the ICH4. | |
| AC_BITCLK | • No extra pull-down resistors required. | |

| Signal | Description | ✓ |
|---|---|---|
| | • Series termination resistor 33 Ω to 47 Ω from the motherboard codec to the ICH4 and also to the CNR<br>• When nothing is connected to the link, BIOS must set a shut off bit for the internal keeper resistors to be enabled. At that point, pull-ups/pull-downs are not needed on any of the link signals. | |
| AC_SYNC | • No extra pull-down resistors required. | |
| **ICH4 / USB Signals** | | |
| USBRBIAS/ USBRBIAS# | • 22.6 Ω ±1% connected to ground | |
| USBP[5:0]P, USBP[5:0]N | • No external resistors are required<br>• Output driver impedance of 45 Ω provided | |
| OC[5:0]# | • If not used, use 10 kΩ ±5% to VCCSus3_3<br>• Inputs must not float | |
| Unconnected USB Data Signals | Can be left as No Connect | |
| **ICH4 Interrupt Interface Items** | | |
| PIRQ[D:A]# | • These signals require a pull-up resistor. Recommend a 2.7 kΩ pull up resistor to VCC5 or 8.2 kΩ ±5% to VCC3_3.<br>• In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering Section. Each PIRQx# line has a separate Route Control Register.<br>• In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[A]# is connected to IRQ16, PIRQ[B]# to IRQ17, PIRQ[C]# to IRQ18, and PIRQ[D]# to IRQ19. This frees the ISA interrupts. | |
| PIRQ[H:E]#/GPIO[5:2] | • These signals require a pull-up resistor. Recommend a 2.7 kΩ pull up resistor to VCC5 or 8.2 kΩ ±5% to VCC3_3.<br>• In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering Section. Each PIRQx# line has a separate Route Control Register.<br>• In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQ[E]# is connected to IRQ20, PIRQ[F]# to IRQ21, PIRQ[G]# to IRQ22, and PIRQ[H]# to IRQ23. This frees the ISA interrupts. | |
| SERIRQ | • External weak (8.2 kΩ) pull up resistor to $V_{CC}$3_3 is recommended. | |

| Signal | Description | ✓ |
|---|---|---|
| APIC | • **If the APIC is used:** 150Ω pull-up resistors on APICD[0:1] Connect APICCLK to clock generator with a 20 Ω – 33 Ω series termination resistor.<br>• **If the APIC is not used on up systems** The APICCLK should be tied directly to GND. Pull APICD[0:1] to GND through a 10 kΩ pull-down resistor. If using XOR chain testing, a pull-down for each APIC signal is required (i.e., two 10K Ω pull-down resistors). | |
| **ICH4 System Bus / SMLink Interface Items** | | |
| SMBDATA, SMBCLK | • Require external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)<br>• Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections.<br>• Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK[0] and SMBDATA should be tied to SMLINK[1]<br>• Value of pull-ups resistors determined by line load. | |
| SMBALERT#/ GPIO[11] | • See GPIO section if SMBALERT# not implemented. | |
| SMLINK[1:0] | • Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)<br>• Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections.<br>• Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK[0] and SMBDATA should be tied to SMLINK[1]<br>• Value of pull-ups resistors determined by line load. Typical value used is 8.2 kΩ. | |
| INTRUDER# | • Pull signal to VCCRTC (VBAT) through a 330k Ω resistor if not needed.<br>• Signal in VCCRTC (VBAT) well. | |

| Signal | Description | ✓ |
|---|---|---|
| **ICH4 / PCI Interface Signals** | | |
| FYI | • All inputs to the ICH4 must not be left floating<br>• Many GPIO signal are fixed inputs that must be pulled up to different sources. See GPIO section for recommendations. | |
| PERR#, SERR#, PLOCK#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, REQ[4:0]#, GPIO[0]/REQ[A]#, GPIO[1]/REQ[B]#/REQ[5] | • These signals require a pull up resistor. Recommend an 8.2 kΩ pull up resistor to VCC3_3 or a 2.7 kΩ pull up resistor to VCC5.<br>• See PCI 2.2 Component Specification pull-up recommendations for VCC3_3 and VCC5. | |
| PCIGNT#[4:0] | • No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented they must be pulled up to $V_{CC}3\_3$.<br>• These signals are actively driven by the ICH4 | |
| GNT[A]# /GPIO[16], GNT[B]/ GNT[5]#/ GPIO[17] | • No extra pull-up needed<br>• These signals have integrated pull-ups of 24 kΩ. GNT[A] has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull down resistor can be added to manually enable the function. | |
| PCIRST# | • The PCIRST# signal should be buffered to form the IDERST# signal 33 Ω series resistor to IDE connectors.<br>• Improves Signal Integrity | |
| PME# | • No extra pull-up needed<br>• This signal has integrated pull-up of 18 kΩ to 42 kΩ. | |
| **ICH4 / RTC Signals** | | |
| VBIAS | • The VBIAS pin of the ICH4 is connected to a 0.047 µF cap.<br>• For noise immunity on VBIAS signal | |

| Signal | Description | ✓ |
|---|---|---|
| RTCX1,<br>RTCX2 | • Connect a 32.768 kHz Crystal Oscillator across these pins with a 10M Ω resistor and use 18 pF decoupling caps at each signal (based on a crystal load of 12.5pF).<br>• The ICH4 implements new internal oscillator circuit as compared with the PIIX4 to reduce power consumption. The external circuitry shown in the DG will be required to maintain the accuracy of the RTC.<br>• The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VCCRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds | |
| RTCRST# | Time constant due to RC filter on this line should be 18-25 ms. Recommended value for Resistor = 180KΩ and Capacitor is 0.1 µF Timing Requirement | |
| **ICH4 / LAN Signals** | | |
| LANCLK | • Connect to LAN_CLK on Platform LAN Connect Device<br>• ICH4 has an integrated 100kΩ nominal pull-down resistor. | |

## 14.6 Miscellaneous MCH Signals

| Signal | Description | ✓ |
|---|---|---|
| 66IN | • Connect to CK_408. | |
| RSTIN# | • Connect to PCIRST# on the ICH4. | |
| TESTIN# | • No Connect. | |

## 14.7 Clock Interface CK_408

| Signal | Description | ✓ |
|---|---|---|
| 66_BUFF0 | • Connect to MCH.<br>• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor. | |
| 66_BUFF1 | • Connect to ICH4.<br>• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor. | |
| 66_BUFF2 | • Connect to AGP.<br>• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor. | |
| 66_INPUT | • No Connect. | |

| Signal | Description | ✓ |
|---|---|---|
| CLK14 | • Connect to ICH4 through a series 33 Ω resistor. | |
| CLK48 | • Connect to ICH4 through a series 33 Ω resistor. | |
| CLK66 | • Connect to ICH4 through a series 33 Ω resistor. | |
| CPU [1:0] | • Connect to processor.<br>• Connect to a series 27Ω ±5% resistor and terminate to GND through a 49.9Ω ±1% resistor. | |
| CPU [1:0]# | • Connect to processor.<br>• Connect to a series 27Ω ±5% resistor and terminate to GND through a 49.9Ω ±1% resistor. | |
| CPU2 | • Connect to MCH.<br>• Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor. | |
| CPU2# | • Connect to MCH.<br>• Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor. | |
| CPU_STOP# | • Terminate to VCC3 through a 1 kΩ ± 1% resistor. | |
| DOT_48 MHz | • No Connect. | |
| DRCG_0 | • Connect to Glue Chip/Discrete Logic.<br>• Connect to a series 33Ω ±5% resistor and terminate to GND through a 10 pF ± 5% capacitor. | |
| DRCG_1/VCH | • No Connect. | |
| IREF | • Terminate to GND through a 475 Ω ± 1% resistor. | |
| MULT0 | • Connected from the VCC3 through a series 10 kΩ ± 5% resistor and terminate to GND through a parallel 1 kΩ ± 1% resistor. | |
| PCI [6:0] | • Connect to a series 33 Ω ±5% resistor and terminate to GND through a 10 pF ± 5% capacitor. | |
| PCIF[2:0] | • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor. | |
| PCI_STOP# | • Terminate to VCC3 through a 1 kΩ ± 5% resistor. | |
| PWRDWN# | • Terminate to VCC3 through a 1 kΩ ± 5% resistor. | |
| REF0 | • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor. | |
| SEL[1:0] | • Terminate to Vcc3_CLK through a 1 kΩ ± 5% resistor. | |
| SEL_2 | • Terminate to GND through a 1 kΩ ± 5% resistor. | |
| SCLK | • Connect to DIMMs. | |
| SDTA | • Connect to DIMMs. | |
| USB_48 MHz | • Connect to ICH4.<br>• Terminate to GND through a 33 Ω ± 5% resistor and a 10 pF ± 5% capacitor. | |
| VDD | • Terminate to VCC3CLK. | |
| VDD_48 MHz | • Terminate to VCC3CLK. | |

| Signal | Description | ✓ |
|---|---|---|
| VDDA | • Terminate to GND through a 0.1 µF ± 5% capacitor. | |
| VSS | • Terminate to GND. | |
| VSS_48 MHz | • Terminate to GND. | |
| VSS_IREF | • Terminate to GND. | |
| VTT_PWRGD# | • Connect to an inverted copy of VCC_CPU . Refer to the respective section of the design guide for more details. | |
| XTAL_IN | • Terminate to GND through a 10 pF ± 5% capacitor. | |
| XTAL_OUT | • Terminate to GND through a 10 pF ± 5% capacitor. | |

## 14.8 Power and Ground

| Signal | Description | ✓ |
|---|---|---|
| VCC3_3 | • Requires six 0.1 µF decoupling capacitors. | |
| VCC1_8 | • Requires two 0.1 µF decoupling capacitors. | |
| 5V_REF | • Connect to VREF[2:1] pins. | |
| VCCSUS3.3 | • Requires one 0.1 µF decoupling capacitor. | |
| VCCSUS1.8 | • Requires one 0.1 µF decoupling capacitor. | |
| 5V_REF SUS | • Requires one 0.1 µF decoupling capacitor.<br>• (V5REFSUS only affects 5 V tolerance for USB OC[3:0] pins and can be connected to VCCSUS3.3 if 5 V tolerance on these signal is not required). | |
| V_CPU_IO[1:0] | • Connected to the proper power plane for the processor's CMOS compatibility signals.<br>• Connect one .1 µF decoupling capacitor. | |
| VSS | • Connect to GND. | |

§

# 15 Intel® 845E Chipset Design Layout Checklist

## 15.1 System Bus

### 15.1.1 System Bus

| Checklist Item | ✓ |
|---|---|
| **Data Signals: D[63:0]#, DBI[3:0]#** | |
| • Point-to-Point Topology. | |
| • Edge to edge spacing versus trace to reference plane height ratio should be 3:1. | |
| • 2.0 in. to 8.0 in. pin to pin data signal lengths. | |
| • Traces should be 7 mils wide with 13 mil spacing. | |
| • Data signals of the same source synchronous group should be routed to the same pad-to-pad length within +100 mils of the associated strobes. | |
| **Data Strobes: DSTBn/p[3:0]** | |
| • Traces should be 7 mils wide with 13 mil spacing. | |
| • Data strobes and their compliments should be routed within ±25 mils of the same pad to pad length. | |
| **Address Strobes: ADSTB[1:0]** | |
| • Point-to-Point Topology. | |
| • Edge to edge spacing versus trace to reference plane height ratio should be 3:1. | |
| • 2.0 in. to 10.0 in. pin to pin address signal lengths. | |
| • Traces should be 7 mils wide with 13 mil spacing. | |
| **Address Signals: A[3:31]#, REQ[4:0]** | |
| • Traces should be 7 mils wide with 13 mil spacing. | |
| • 2.0 in. to 10.0 in. pin to pin address signal lengths. | |
| • Address signals of the same source synchronous group should be routed to the same pad-to-pad length, within ±200 mils of the associated strobes. | |
| **Clocks: BCLK, BCLK#** | |
| • These should be routed as a differential pair with 7 mil traces and 7mil spacing between them. | |
| • 3.0 in. to 10.0 in. pin to pin common clock lengths. | |
| • 25 mil spacing should be maintained around all clocks. | |

| Checklist Item | ✓ |
|---|---|
| **Processor AGTL+: FERR#** | |
| • Traces should be 5 mils wide with 7 mil spacing. | |
| • 1.0 in. to 12.0 in. max from Processor to ICH4. | |
| • 3.0 in. max from ICH4 to VDD. | |
| **Processor AGTL+: PROCHOT#** | |
| • Traces should be 5 mils wide with 7 mil spacing. | |
| • 1.0 in. to 17.0 in. max from Processor to the voltage translator | |
| • 3.0 in. max from voltage translator to Vcc_CPU | |
| • 10.0 in. max from voltage translator to the external logic | |
| **Processor AGTL+: PROCHOT#** | |
| • Traces should be 5 mils wide with 7 mil spacing. | |
| • 1.0 in. to 17.0 in. max from Processor to the series termination | |
| • 2 in max from the series termination to ICH4 | |
| • Series termination should be 60Ohm between 80 Ohms | |
| **ICH4 AGTL+: A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, STPCLK#** | |
| • Traces should be 5 mils wide with 7 mil spacing. | |
| • 1.0 in. to 17.0 in. max from Processor to the series termination | |
| • 2 in max from the series termination to ICH4 | |
| • Series termination should be 60Ohm between 80 Ohms | |
| • Level shifting is required from the INIT# pin to FWH. | |
| **Intel® ICH4 Open Drain AGTL+: PWRGOOD** | |
| • 7 mil spacing. | |
| • 1.0 in. to 12.0 in. max from ICH4 to Processor. | |
| • 1.1 in. max breakout length. | |
| • 3.0 in. max from Processor to VDD. | |
| **Miscellaneous AGTL+: BR0#, RESET#** | |
| • Terminate using discrete components on the system board. | |
| • Minimize the distance between the terminating resistors and the processor. | |
| • Connect the signals between these components. | |
| **Miscellaneous AGTL+: COMP[1:0]** | |
| • Minimize the distance from terminating resistor. | |
| **Miscellaneous AGTL+: THERMDA, THERMDC** | |
| • 10 mils wide by 10 mil spacing. | |

| Checklist Item | ✓ |
|---|---|
| • Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4.0 in. to 8.0 in. away as long as the worst noise sources such as clock generators, data, buses and address buses, etc are avoided. | |
| • Route in parallel and close together with ground guards enclosed. | |

## 15.1.2 Decoupling, VREF, and Filtering

| Checklist Item | ✓ |
|---|---|
| **VCC_CPU Decoupling** | |
| • 9 OSCONs, 560 µF.<br>• 3 Al Electrolytic, 3300 µF.<br>• 38 1206 package, 10 µF.<br>• Refer to Section 0. | |
| **Processor GTLREF** | |
| • The processor must have one dedicated voltage divider. | |
| • Keep the voltage divider within 1.5 in. of the first GTLREF pin. | |
| • Keep signal routing at least 10 mils separated from the GTLREF routes. | |
| • 7 mil min trace length for routing. | |
| • Do not allow signal lines to use the GTLREF routing as part of their return path. | |
| GTLREF Decoupling:<br>• Decouple voltage divider with a 1 µF capacitor.<br>• Decouple pin with a high-frequency capacitor (such as a 220 pF 603).<br>• Place capacitor as close to pin as possible. | |
| **VCCA, VCCIOPLL, and VSSA Filtering for Processor** | |
| • Use shielded type inductors. | |
| • Minimize the distance between VCCA, VSSA pins and capacitors. | |
| • VCCA should be routed parallel and next to VSSA route. | |
| • Filter capacitors and inductors should be routed next to each other. | |
| **MCH HVREF** | |
| • 12 mils wide, 3.0 in. max length | |
| • 10 mil group spacing | |
| • Place 0.1 µF decoupling capacitor at the MCH | |
| • Minimize the distance between the voltage divider, decoupling capacitors and MCH | |

| Checklist Item | ✓ |
|---|---|
| **MCH HVREF** | |
| • 12 mils wide, 3.0 in. max length. | |
| • 10 mil group spacing. | |
| • Place 0.1 μF decoupling capacitor at the MCH. | |
| • Minimize the distance between the voltage divider, decoupling capacitors and MCH. | |
| **MCH HRCOMP[1:0]** | |
| • 10 mils wide, 0.5 in. max length. | |
| • 7 mils group spacing. | |
| • Minimize the distance between HRCOMP and the MCH. | |
| **MCH VTT Decoupling** | |
| • Place five evenly 0.1 μF capacitors within 150 mils of the MCH. | |
| • Place two 10 μF capacitors right behind the 0.1 μF capacitors. | |

## 15.2 System Memory (DDR)

### 15.2.1 2 DIMM DDR-SDRAM

| Data Signals: SDQ[63:0], SCB[7:0], SDQS[8:0] | |
|---|---|
| • Daisy Chain Topology, Routed Entirely on the Top Signal Layer | |
| • Ground Referenced | |
| • 5 mils wide | |
| • 12 mil spacing from MCH to 1st DIMM | |
| • 7 mil minimum spacing within DIMM Pin Field | |
| • 12 mil spacing from DIMM to DIMM | |
| • 7 mil minimum spacing from 2nd DIMM to Rt | |
| • 20 mil minimum Isolation Spacing from Non-DDR Related Signals | |
| • 2.0” to 5.0” trace length from MCH signal ball to series termination resistor pad | |
| • 0.5” max trace length from series termination resistor pad to 1st DIMM pin | |
| • 0.3” to 0.5” trace length from DIMM pin to DIMM pin | |
| • 0.1” to 0.8” trace length from last DIMM pin to parallel termination resistor pad | |

| Data Signals: SDQ[63:0], SCB[7:0], SDQS[8:0] | |
|---|---|
| Breakout guideline:<br>• 5 mils wide by 7 mil spacing for a max of 0.35” | |
| SDQ[63:0], SCB[7:0], SDQS[8:0] Length Matching Guidelines:<br>• See Section 5.3.1.2 for details | |
| **Control Signals: SCKE[3:0], SCS[3:0]#** | |
| • Point to Point Topology | |
| • Ground Referenced | |
| • 5 mils wide | |
| • 12 mil spacing from MCH to 1st DIMM | |
| • 7 mil minimum spacing within DIMM Pin Field | |
| • 12 mil spacing from DIMM to DIMM | |
| • 7 mil minimum spacing from 2nd DIMM to Rtt | |
| • 20 mil minimum Isolation Spacing from Non-DDR Related Signals | |
| • 7 mil minimum Isolation Spacing from the 2.5 V Copper Flood on Layer Four | |
| • 40 mils from MCH signal pin to MCH signal via | |
| • 2.0” to 3.5” from MCH signal via to layer transition via | |
| • 0.5” max from layer transition via to DIMM pins on 1st DIMM (SCS#/SCKE[1:0]) | |
| • 1.0” max from layer transition via to DIMM pins on 2nd DIMM (SCS#/SCKE[3:2]) | |
| • 0.4” to 1.3” from DIMM pins on 1st DIMM to Rt Pad (SCS#/SCKE[1:0]) | |
| • 0.1” to 0.8” from DIMM pins on 2nd DIMM to Rt Pad (SCS#/SCKE[3:2]) | |
| Control Signal to System Memory Clock Routing Requirements:<br>• See section 5.3.2.2 for details | |
| **Command Signals: SMA[12:0], SBS[1:0], SRAS#, SCAS#, SWE#** | |
| • Daisy Chain Topology | |
| • Ground Referenced | |
| • 5 mils wide by 12 mil spacing | |
| • 12 mil spacing from MCH to 1st DIMM | |
| • 7 mil minimum spacing within DIMM Pin Field | |
| • 12 mil spacing from DIMM to DIMM | |
| • 7 mil minimum spacing from 2nd DIMM to Rt | |
| • 20 mil minimum Isolation Spacing from Non-DDR Related Signals | |
| • 7 mil minimum Isolation Spacing from the 2.5 V Copper Flood on Layer Four | |
| • 40 mil max from MCH signal pin to MCH signal via | |
| • 2.0” to 3.5” from MCH signal via to layer transition via | |
| • 0.5” max from layer transition via to 1st DIMM pin | |
| • 0.3” to 0.5” from DIMM pin to DIMM pin | |

| Data Signals: SDQ[63:0], SCB[7:0], SDQS[8:0] | |
|---|---|
| • 0.1” to 0.8” from DIMM pins on 2nd DIMM to Rt pad | |
| Command Signal to System Memory Clock Routing Requirements:<br>• See section 5.3.3.2 for details | |
| **Clock Signals: SCK[5:0], SCK#[5:0]** | |
| • Point to Point Topology, Routed Entirely on the Bottom Signal Layer | |
| • Ground Referenced | |
| • 5 mils wide | |
| • 7 mil Differential Trace Spacing | |
| • 20 mil minimum Isolation Spacing from another DDR Signal Group or from Non-DDR Related Signals | |
| • 10 mil minimum Isolation Spacing from the 2.5 V Copper Flood on Layer Four | |
| • 20 mil minimum of Serpentine Spacing | |
| • 40 mil max from MCH signal pin to MCH signal via | |
| • 2.0” to 6.5” from MCH signal via to associated DIMM pins on First DIMM Connector (SCK/SCK#[2:0]) | |
| • 2.5” to 7.0” from MCH signal via to associated DIMM pins on Second DIMM Connector (SCK/SCK#[5:3]) | |
| System Memory Clock Length Matching:<br>• See section 5.3.4.2 for details | |
| **Feedback Signals: RCVENOUT#, RCVENIN#** | |
| • Point to Point Topology | |
| • Ground Referenced | |
| • 5 mils wide by 12 mil spacing | |
| • 10 mil minimum Isolation Spacing from another DDR Signal Group or from Non-DDR Related Signals | |
| • 7 mil minimum Isolation Spacing from the 2.5 V Copper Flood on Layer Four | |
| • 40 mil max from MCH signal ball to MCH signal via | |
| • MCH RCVEN# output signal via to RCVEN# input signal via must equal 1.0” | |

# 15.3 AGP

## 15.3.1 1X Signals:

| Checklist Item | ✓ |
|---|---|
| **CLK, RBF#, WBF#, ST [2:0], PIPE, REQ#, GNT#, PAR, FRAME#, IRDY#, TRDY, STOP#, DEVSEL#** | |
| • 7.25 in. max trace length. | |
| • 5 mils wide by 5 mil spacing. | |
| • No trace matching requirements. | |

## 15.3.2 2X/4X Signals:

| Checklist Item | ✓ |
|---|---|
| **AD [31:0], C/BE [3:0]#, ADSTB [1:0]#, SBA [7:0], SB_STB, SB_STB#** | |
| • Route AD[15:0], C/BE[1:0], AD_STB0, and AD_STB0# together. | |
| • Route AD[31:16], C/BE[3:2], AD_STB1, and AD_STB1# together. | |
| • Route SBA[7:0], SB_STB, SB_STB# together. | |
| • ±0.1 in. length match strobe pairs. | |
| **Less Than 6 Inches** | |
| • 5 mils wide by 15 mil spacing. | |
| • ±0.25 in. length match from DATA and C/BE# to strobes. | |
| • Signals that require pull-up or pull-down resistors.<br>• 0.5 in. max stub length for 1X signals. | |
| **Greater Than 6 Inches and Less Than 7.25 Inches** | |
| • 5 mils wide by 20 mil spacing. | |
| • ±0.125 in. length match from DATA and C/BE# to strobes. | |
| • Signals that require pull-up or pull-down resistors.<br>• 0.1 in. max stub length for 2X/4X signals. | |
| **AGP Controller Down On Motherboard** | |
| • 5 mils wide by 15 mil spacing. | |
| • 10.0 in. max trace length. | |

## 15.3.3 Decoupling, Compensation, and VREF

| Checklist Item | ✓ |
|---|---|
| **VCC1_5 Decoupling** | |
| • Min of six 0.1 µF capacitors spaced evenly among the AGP signals routed between the MCH and AGP connector to decouple MCH core and MCH AGP I/O. All capacitors must be within 0.25 in. of MCH. | |
| **GRCOMP** | |
| • 10 mils wide, 0.5 in. max length. | |
| • Minimize the distance between GRCOMP resistor and MCH. | |
| **AGPREF** | |
| • Minimum trace width must be 12 mils. | |
| • Minimum trace spacing around the AGPVREF signal must be 25 mils. | |
| • One 0.1 µF bypass capacitor should be placed 0.8 in. maximum from MCH's AGPREF pin. | |

# 15.4 HUB Interface

## 15.4.1 Interface Signals

| Checklist Item | ✓ |
|---|---|
| **General Recommendations** | |
| • It is recommended that all signals be referenced to VSS. | |
| • Board impedance must be 60 Ω ± 10%. | |
| • Traces must be routed 5 mils wide with 15 mils spacing. | |
| • Max trace length is 8 in. | |
| **Data Signals** | |
| • Data signals need to be routed 5 mils wide with 15 mils spacing | |
| • Data signals must be matched within ± 100 mils of the HISTB/ HISTB# differential pair | |
| • For breakout, data signals can be routed to 5 on 5 within 300 mils of the package | |
| **Strobe Signals** | |
| • Strobe signals need to be routed 5 mils wide with 15 mils spacing | |
| • Strobe pair should have a minimum of 15 mils spacing from any adjacent signals. | |
| • 2” to 8” max trace length | |
| • Strobe length mismatch ± 100 mils max | |
| • For breakout, strobe signals can be routed to 5 on 5 within 300 mils of the package | |

## 15.4.2 Decoupling, Compensation, and VREF

| Checklist Item | ✓ |
|---|---|
| **VCCHI1_8 Decoupling** | |
| • Decouple each component, the MCH and the ICH4, with two 0.1µF capacitors within 100 mils from each package.<br>• Capacitors should be adjacent to hub interface rows | |
| **HICOMP** | |
| • Trace impedance must equal 60Ω ± 15%. | |
| **HIREF/HISWING generation circuit** | |
| • Should be placed no more than 4” away from MCH or ICH4.<br>  • If more than 4” is needed, locally generated divider should be used.<br>• Place (2) 0.1 µF caps close to the divider<br>• Place the 0.01 µF bypass caps within 0.25” of the component’s pin (HIREF/VREF/HISWING). | |

## 15.5 Clocks: CK_408

| Checklist Item | ✓ |
|---|---|
| **Host Clock: CPU#, CPU** | |
| • 7 mils wide. | |
| • Differential pair spacing should be based on a distance from BCLK1 to BCLK0. | |
| • Spacing to other traces should 4 times to 5 times greater than distance from BCLK1 to BCKL0. | |
| • Processor routing length—Clock driver to Rs should be 0.5 in. max. | |
| • Processor routing length—Rs to Rs-Rt should be 0 in. to 0.2 in. | |
| • Processor routing length—RS_RT node to Rt should be 0 in. to 0.2 in. | |
| • Processor routing length—RS_RT node to load should be 2 in. to 9 in. | |
| • MCH routing length—Clock driver to Rs should be 0.5 in. max. | |
| • MCH routing length—Rs to Rs-Rt should be 0.5 in. max. | |
| • MCH routing length—RS_RT node to Rt should be 0.0 in. to 0.2 in. max. | |
| • MCH routing length—RS_RT node to load should be 2.0 in. to 9.0 in. max. | |
| • Clock driver to processor and clock driver to chipset length matching should be 600 mils. | |
| • 10 mil length matching between BCLK0 to BCLK1. | |
| • Do not split up the two halves of a differential clock pair between layers. | |
| • Route all agents on the same physical routing layer referenced to ground of the differential clock. | |
| • Make sure that the skew induced by the vias is compensated in the traces to other agents. | |
| • Do not place vias between adjacent complementary clock traces. | |
| • Maintain uniform spacing between the two halves of differential clocks. | |
| • Route clocks on physical layers adjacent to the VSS reference plane only. | |
| **66 MHz Clock Group** | |
| • Point-to-Point Topology. | |
| • 5 mils wide and 20 mil spacing. | |
| • 20 mil group spacing. | |
| • Series termination within 0.5 in. of the driver. | |
| • Trace length from series termination to receiver on the motherboard between 4.0 in. and 8.5 in. | |
| • The total trace lengths must be matched to ± 100 mils of each other. | |
| • Follow these guidelines when routing to an AGP device down on the motherboard. | |
| **AGP Clock (When Routing to an AGP Connector)** | |
| • Point-to-Point Topology. | |
| • 5 mils wide and 20 mil spacing. | |
| • 20 mil group spacing. | |
| • Series termination within 0.5 in. of the driver. | |
| • The total trace length must be 4.0 in. less than the CLK66 total trace lengths ± 100 mils. | |

| Checklist Item | ✓ |
|---|---|
| **33 MHZ Clock Group** | |
| • Point-to-Point Topology. | |
| • 5 mils wide and 15 mil spacing. | |
| • 15 mil group spacing. | |
| • Series termination within 0.5 in. of the driver. | |
| • The total mismatch between any two 33 MHz clocks must be less than 7.5 in. If routing to a PCI connector, 2.6 in. of routing on the PCI card must be included in the 7.5 in. total mismatch. | |
| • The 33 MHz clock to the ICH4 must be matched to ± 100 mils of the 66 MHz clock to the ICH4. | |
| **14 MHz Clock Group** | |
| • Balanced T Topology. | |
| • 5 mils wide and 10 mil spacing. | |
| • 10 mil group spacing. | |
| • Series termination within 0.5 in. of the driver. | |
| • The total trace length from the Clock driver to SIO and Clock driver must be matched to 0.5 in. | |
| • Signal must T within 12 in. of the series termination. | |
| • Max trace length of stubs is 6 in. | |
| • Total trace length matched to ± 0.5 in. of each other. | |
| **USB Clock** | |
| • Point-to-Point Topology. | |
| • 5 mils wide. | |
| • 15 mil group spacing. | |
| • Series termination within 0.5 in. of the driver. | |
| • Trace length from series termination to receiver on the motherboard between 3.0 in. and 12 in. | |

### 15.5.1 Decoupling

| Checklist Item | ✓ |
|---|---|
| **VddA/Vdd Decoupling** | |
| • Place one 10 µF capacitor close to the Vdd generation circuitry. | |
| • Place six 0.1 µF capacitors close to the Vdd pins on the clock driver. | |
| • Place three 0.01 µF capacitors close to the VddA pins on the clock driver. | |
| • Place one 10 µF bulk decoupling capacitor close to the VddA generation circuitry. | |
| • Host clock pairs must be differentially routed on the same physical routing layer. | |
| • Differential clocks must not have more than two via transitions. | |
| • Ground referencing is strongly recommended for all platform clocks. | |
| • Motherboard layer transitions and power plane splits must be kept to a minimum. | |
| • For flooding options, refer to Section 12.5 of the Design Guide. | |

## 15.6 Intel® ICH4

### 15.6.1 IDE

| Recommendations | ✓ |
|---|---|
| • 5 mil width and 7 mil spacing. | |
| • 8.0 in. max trace length from ICH4 to IDE connector. | |
| • Shortest IDE trace length must be 0.5 in. shorter than the longest IDE trace length. No more than 0.5in between the shortest data signal and the longest strobe signal. | |

### 15.6.2 AC ’97

| Recommendations | ✓ |
|---|---|
| • Trace impedance should be 60 Ω ± 15%. | |
| • 5 mil width by 5 mil spacing. | |
| • 14.0 in. max trace length from ICH4 to Codec/CNR connector (Assuming CNR implements its audio solution with a max trace length of 4.0 in.) | |

## 15.6.3 USB 2.0

| Recommendations | ✓ |
|---|---|
| • 5 mils wide, 5 mil spacing | |
| • 20 mil min spacing between USB signal pair and other traces. Helps minimize cross talk. | |
| • 150 mil max trace length mismatch between USB signal pair | |
| • With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first | |
| • Route USB signals ground referenced. | |
| • Route USB signals using a minimum of vias and corners.<br>• This reduces signal reflections and impedance changes. | |
| • When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn.<br>• This reduces reflections on the signal by minimizing impedance discontinuities | |
| • Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks. | |
| • Stubs on USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs on a given data line should not be greater than 200 mils. | |
| • Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.) | |
| • Keep USB signals clear of the core logic set.<br>• High current transients are produced during internal state transitions, which can be very difficult to filter out. | |
| • Keep traces at least 50 mils away from the edge of the plane ($V_{CC}$ or GND depending on which plane to which the trace is routed)<br>• Helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB. | |
| • Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90Ω differential impedance. | |
| • Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines. The minimum recommended spacing to clock signals is 20 mils, though it is recommended to keep clocks and PCI traces at least 50 mils from the USB differential pairs if possible.<br>• Minimize crosstalk | |
| • Use 20 mils minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk. | |
| • USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as DM1 and DP1) should be no greater than 150 mils. | |
| • No termination resistors needed for USB. | |
| • USBRBIAS (ball A23) and USBRBIAS# (ball B23) should be routed with a single trace 500 mis or less to the 22.6Ω 1% resistor to ground. | |

| Recommendations | ✓ |
|---|---|
| • 17” max length from ICH4 to the backpanel.<br>• 10” max length from ICH4 to CNR. | |

## 15.6.4 PCI

| Recommendations | ✓ |
|---|---|
| • For 2 to 4 slot boards (4 to 10 inches to the first slot and then 1 inch to each subsequent slot) | |
| • For 5 slot boards (4 to 8 inches to the first slot and then 1 inch to each subsequent slot) | |

## 15.6.5 RTC

| Recommendations | ✓ |
|---|---|
| • Minimize the capacitance between RTCX1 and RTCX2 in the routing. | |
| • Put a ground plane underneath crystal components. | |
| • 0.25 in. max RTC lead lengths. | |
| • Do not route switching signals under the external components (unless on other side of board). | |

## 15.6.6 LAN

| Recommendations | ✓ |
|---|---|
| • 5 mils wide, 10 mil spacing | |
| • 1.5” to 9.5” max trace length from ICH4 to CNR· (0.75” to 2.75” on card)<br>• To meet timing requirements. | |
| • Stubs due to R-pak CNR/LOM stuffing option should not be present.<br>• To minimize inductance. | |
| • Maximum Trace Lengths: Intel® ICH4 to: Intel® 82562ET:L = 4” to 12”;Intel® 82562EM:L = 4” to 12”<br>• To meet timing requirements. | |
| • Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches (clock must be longest trace)<br>• To meet timing and signal quality requirements. | |
| • Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN PHY.<br>• To meet timing and signal quality requirements. | |
| • Keep the total length of each differential pair under 4 inches.<br>• Issues found with traces longer than 4 inches: IEEE phy conformance failures, excessive EMI and or degraded receive BER. | |

| Recommendations | ✓ |
|---|---|
| • Do not route the transmit differential traces closer than 100 mils to the receive differential traces.<br>• To minimize crosstalk. | |
| • Signal traces and differential traces not route in parallel and closer than 100mil (300 mils recommended)<br>• To minimize crosstalk. | |
| • Route 5 mils on 10 mils for differential pairs (out of LAN phy)<br>• To meet timing and signal quality requirements | |
| • Differential trace impedance should be controlled to be ~100 Ω<br>• To meet timing and signal quality requirements | |
| • For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two 45-degree bends.<br>• To meet timing and signal quality requirements | |
| • Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.<br>• This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards. | |
| • Do not route traces and vias under crystals or oscillators.<br>• This will prevent coupling to or from the clock. | |
| • Trace width to height ratio above the ground plane ratio is between 1:1 and 3:1.<br>• To control trace EMI radiation. | |
| • Traces between decoupling and I/O filter capacitors should be as short and wide as practical.<br>• Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors. | |
| • Vias to decoupling capacitors should be sufficiently large in diameter.<br>• To decrease series inductance. | |
| • Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.<br>• To minimize crosstalk. | |
| • Isolate I/O signals from high speed signals.<br>• To minimize crosstalk. | |
| • Place the Intel® 82562ET/EM part more than 1.5 inches away from any board edge.<br>• This minimizes the potential for EMI radiation problems. | |
| • Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the 82562ET/EM.<br>• Research and development has shown that this is a robust design recommendation. | |
| • Place decoupling caps (0.1 µF) as close to the 82562ET/EM as possible. | |

## 15.7 FWH

| Recommendations | ✓ |
|---|---|
| • 0.1 µF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins. | |
| • 4.7 µF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins. | |

### 15.7.1 ICH4 Decoupling

| Recommendations | ✓ |
|---|---|
| • Place caps within 100 mils from the package | |
| • VCC3_3· (6) 0.1 µF caps – Decoupling Cap (Vss) | |
| • VCCSUS3_3· (2) 0.1 µF caps - Decoupling Cap (Vss) | |
| • V_CPU_IO· (1) 0.1 µF cap - Decoupling Cap (Vcc) | |
| • VCC1_5· (2) 0.1 µF caps - Decoupling Cap (Vss) | |
| • VCCSUS1_5· (2) 0.1 µF caps - Decoupling Cap (Vss) | |
| • V5REF· (1) 0.1 µF cap - Decoupling Cap (Vcc) | |
| • V5_REF_SUS· (1) 0.1 µF cap - Decoupling Cap (Vss) | |
| • VCCRTC· (1) 1.0 µF cap - Decoupling Cap (Vcc) | |
| • VCCHI· (2) 0.1 µF cap - Decoupling Cap (Vss) | |
| • VCCPLL· (1) 0.1 µF and (1) 0.01 µF cap - Decoupling Cap (Vcc) | |

## 15.8 Power

### 15.8.1 Filtering

| Checklist Item | ✓ |
|---|---|
| **MCH PLL Filter Routing Guidelines: PLL0, PLL1** | |
| • 5 mil width by 10 mil spacing. | |
| • 1.5 in. max length from capacitor to MCH. | |

§