Intel® Zone Rendering Technology 3

White Paper

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Revision History

Revision Number	Description	Revision Date
-001	• Initial public release	June 2004
-002	• Updated to include Intel® 915GV Express chipset	August 200f

1 Introduction

With the release of the next-generation Intel® GMCH, the Intel® 915G/915GV/910GL Express chipset, an enhanced graphics engine is introduced, Intel® Graphics Media Accelerator (GMA) 900. One of the updated features of this graphics engine is *Zone Rendering Technology 3*. This paper reviews the updates of the Zone Rendering Technology 3 capabilities of Intel GMA 900, outlines the advantages offered by Zone Rendering Technology 3, and discusses the implications of Zone Rendering Technology 3 to software application developers.

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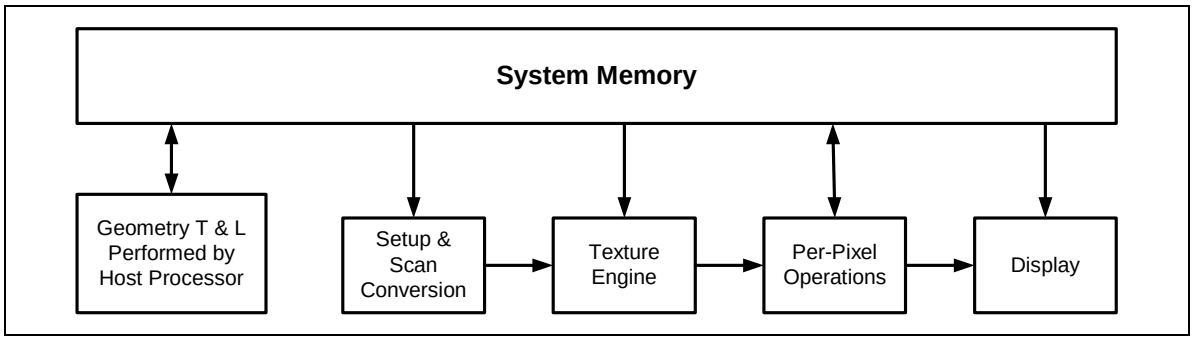
2 Overview

This section provides an overview of the traditional 3D graphics rendering engine as well as a Zone Rendering Technology 3 graphics engine.

2.1 Conventional 3D Rendering

The basic overview of the traditional 3D graphics pipeline is given in the figure below. In this traditional 3D pipeline, each polygon is processed in the order that it is received by the hardware. Hence, the 3D pipeline displayed in the figure below is referred to as “immediate mode” 3D rendering, meaning that as each polygon is sent to the hardware, it is immediately processed through the pipeline and rendered into the frame buffer, as appropriate.

Figure 1. Conventional 3D Graphics Pipeline



2.1.1 Geometry Transform and Lighting Performed by Host Processor

In the initial stage of the pipeline, all of the vertices progress through some number of matrix transformations in order to be converted into 3D world coordinates. The diffuse and specular lighting components are then calculated at each vertex based on its position in the 3D world. These vertices are then finally transformed into 2D screen coordinates. The host processor is used to handle the transform and lighting stage of the pipeline. The vertices may be read from and written to memory multiple times depending on the implementation.

2.1.2 Setup and Scan Conversion

Following the transform and lighting stage the pixel-level specifics of each polygon are calculated. Initially the setup engine receives as input the vertices of each polygon, and then calculates the information needed to convert that polygon into its associated pixels. Also portions of polygon that do not appear on the screen are clipped or culled by the setup engine. The scan converter then receives the information from the setup engine and identifies all the pixels that are being affected by the polygon being rendered.

2.1.3 Texture Engine

Once the associated pixels for each polygon have been calculated, the texture engine is then responsible for retrieving any texture elements, or texels, associated with each pixel. Any required texel operations, such as colorkey matching, color format conversion, or filtering, are then performed by the texture engine. As there are potentially multiple texel fetches for every pixel of every polygon memory access for texels typically account for a large percentage of the graphics memory bandwidth usage.

2.1.4 Per-Pixel Operations

Now that a pixel is fully textured, it's nearly ready to be put into the frame buffer. First, however, the z-buffer is read to determine whether the pixel will even be visible. If it's not, meaning that another pixel would be covering it up in the frame buffer, then the pixel is thrown out and not used. If the pixel is nearer than what is currently in the frame buffer, or needs to be blended with the current frame buffer contents, then both the frame buffer and z-buffer are updated with the new pixels information. For every pixel, then, there is a required z-buffer read and potential z-buffer and frame buffer write in memory. Texel, z-buffer, and frame buffer access in memory will typically account for a large percentage of the memory bandwidth usage.

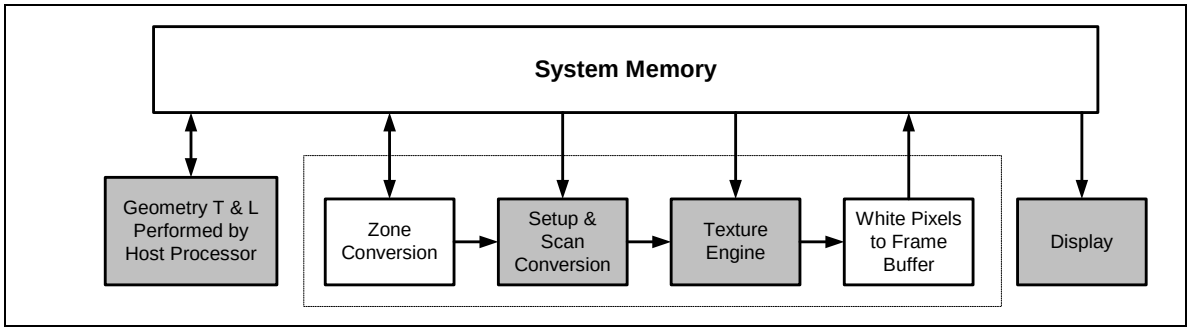
2.2 Zone Rendering Technology 3

2.2.1 Concept of Zone Rendering Technology 3

With immediate mode rendering, discussed in the previous section, any portion of the frame buffer may be drawn to anytime during a single frame. What Zone Rendering Technology 3 does, however, is divide the frame buffer up into a number of rectangular zones, and then renders all of the pixels within a single zone before proceeding on to the next zone. The advantages of this method will be discussed in the next section.

The basic overview of the Zone Rendering Technology 3 3D graphics pipeline featured in the 915G/915GV/910GL Express chipset with Intel GMA 900 graphics is given in the figure below.

Figure 2: Intel® Zone Rendering Technology 3 3D Graphics Pipeline



2.2.2 Zone Conversion

As can be seen in the figure above, the major difference between the Zone Rendering Technology 3 capable 3D graphics pipeline and the conventional 3D graphics pipeline is the inclusion of the zone conversion stage of the pipeline.

In the zone conversion stage, triangles are sorted into memory by zone. Hence all triangles associated with a respective zone are placed into the same zone in memory. Then, these zones are processed one at a time by the remainder of the 3D graphics pipeline, causing only a single zone to be rendered at a time.

2.2.3 Per-Pixel Operations

The second major difference between the Zone Rendering Technology 3 3D graphics pipeline and the conventional pipeline occurs as the pixels are written out to the frame buffer. Because only a single zone is being rendered at a time, all depth calculations can be done on-chip, eliminating the need for a separate depth buffer. Likewise all pixel blend operations are done on-chip. Hence each pixel of a particular zone will only be written once. The need for depth buffer reads and writes, as well as frame buffer reads, has been eliminated.

Additionally, an Intermediate Z test has been added to the ZRT3 rendering path. Intermediate Z allows for pixels that will not appear to be discarded and thus, not rendered. As a result, Intermediate Z allows for a reduction in texture bandwidth since textures do not get applied to pixels that are not rendered.

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3 Advantages of a Zone Rendering Technology 3 3D Graphics Pipeline

The 915G/915GV/910GL Express chipset represents a class of chipset with integrated graphics employing a unified memory architecture (UMA). Integrated graphics chipsets that employ UMA, share system memory resources with the rest of the system, utilizing system memory resources for graphics.

Intel® GMA 900 implements 32 bits per pixel (bpp) graphics allowing for true transparent and translucent surfaces – more realistic shadow effects, smoke effects, clouds, etc. Delivery of these capabilities puts a lot of pressure on the memory subsystem.

Zone Rendering Technology 3 is a unique mechanism that addresses memory bandwidth limitations by reducing the required memory bandwidth for graphics. By processing only a single zone of the frame buffer at a time, the use of the render cache is highly optimized. The high level of spatial coherency in the render cache for any individual zone allows on-chip access to all of the significant color and depth information for a particular frame. As stated previously, this eliminates the need for depth buffer reads and writes, as well as color buffer reads. By eliminating the need for these memory accesses, Zone Rendering Technology 3 reduces the maximum theoretical required graphics memory bandwidth.

The improved memory bandwidth efficiency provides some secondary memory benefits as well. Lower memory bandwidth requirements simplify the memory interface and memory technology used by a Zone Rendering Technology 3 graphics device. This offers potentially large saving in graphics memory cost.

One final benefit of the Zone Rendering Technology 3 architecture is that the fill rate requirements places on the graphics device are reduced. Because no pixels are overdrawn in the frame buffer, the fill rate required to draw any scene is equal to the total number of pixels in the scene (depth complexity = 1). By contrast, traditional 3D graphics architecture may have to redraw each pixel in a scene anywhere that triangles overlap. This means that if the average depth complexity in a scene is 3, meaning each pixel must be drawn 3 times, the fill rate required by a conventional 3D graphics architecture is 3 times the number of pixels in the scene. Thus the fill rate requirements for Zone Rendering Technology 3 will always be the same as the current resolutions, whereas the fill rate requirements for a conventional architecture will increase as a function of the depth complexity.

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4 Software Considerations

Zone Rendering Technology 3 is designed to be completely transparent from an application software point of view. The Intel GMA 900 graphics drivers will feature both a complete Silicon Graphics OpenGL* ICD and full support for Microsoft DirectDraw* and Direct3D* APIs. Furthermore, Zone Rendering Technology 3 will be handled transparently within the driver. Therefore, any application written for OpenGL or the DirectX* graphics APIs will run on the 915G/915GV/910GL Express chipset and make use of Intel GMA 900 graphics hardware capabilities wherever possible.

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5 Summary

5.1 What Is Zone Rendering Technology 3?

Zone Rendering Technology 3 is a process in which the screen is divided into several zones. Each zone is completely cached and rendered on chip before being written to the frame buffer.

5.2 What Are the Benefits of Zone Rendering Technology 3?

Zone Rendering Technology 3 has several benefits:

- Reduction in Depth and Color Bandwidth associated with conventional rendering
- Increased memory efficiency via better localization of data
- Increased on-chip processing speed due to decreased wait time for data
- Reduced power as a result of decreased memory bandwidth
- Increased effective pixel fill rates
- Increased headroom for larger resolution and color depth

5.3 Conclusions

The Zone Rendering Technology 3 architecture featured in the next-generation Intel GMCH, the 915G/915GV/910GL Express chipset with Intel GMA 900 graphics, provides improved performance above conventional 3D architectures through efficient memory bandwidth usage and optimal utilization of the render cache. The Intel GMA 900 graphics drivers provide software support for this new architecture for both Direct3D and OpenGL, allowing both existing and future 3D applications using these APIs to use Zone Rendering Technology 3 without the need for modification.

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