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Issues with Host Processor Card Applications Using the 21554

Application Note

October 1998

Application Note

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1.0   Introduction

This application note describes issues concerning the use of 21554 in add-in cards where the processor on the add-in card is used as a master (or host) processor. It also describes additional concerns where the same card can also be used as a slave (or local) processor card. This dual capability is desired so that two separate card designs do not have to be developed to support master and slave cards. These cards are plugged into a common backplane, as shown in Figure 1. One or two slots are typically designated as master slots while the remaining slots are slave slots. Compact PCI applications are examples of where this type of functionality is desired.

Figure 1. PCI Backplane Application
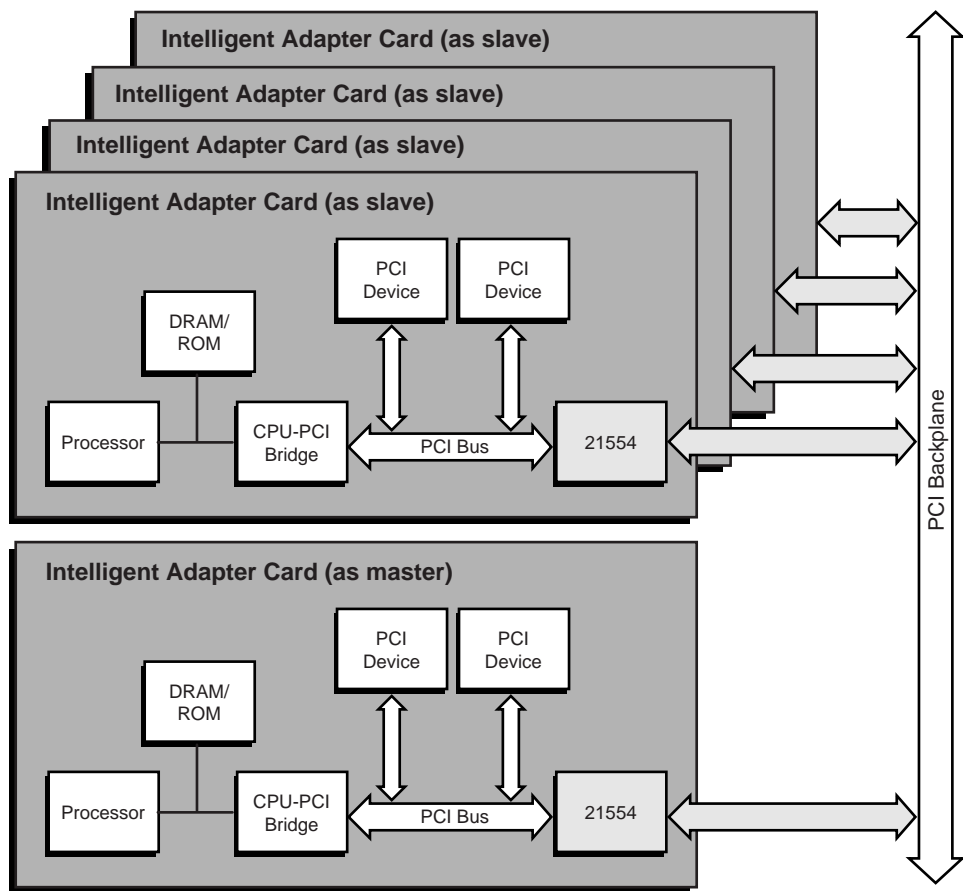
A4841-01

Ideally, an intelligent card plugged into a master slot (acting as host processor) would want the following characteristics:

- Configuration transparency allows host configuration of all slots
    - Allows transparent host access to the primary PCI interface of the slave cards
- Central function support for the backplane PCI bus
    - Clock generation, arbitration, reset generation, REQ64# assertion during reset
    - Secondary interface ideally connects to the backplane to support these functions

However, an intelligent card plugged into a slave slot (acting as local processor) would want these characteristics:

- Configuration and address map isolation of the subsystem
    - Allows local processor control of local subsystem
- Asynchronous clocks
- Secondary interface connects to the local processor, primary interface connects to the backplane (toward the master slot)

Two issues that must be considered when using the same card for both master and slave slots are listed as follows:

1. Transparency versus isolation requirements
2. Symmetry issues

The first issue applies to any card that implements the 21554 when the processor is used as a master processor. Symmetry is an issue when this card plays the dual role of performing either as a master or slave processor card, depending on which slot it is plugged into.

2.0 Transparent and Embedded Bridges

This section provides a conceptual overview of how transparent bridges and embedded bridges differ. A more detailed discussion of differing the features is contained in the *21554 Hardware Reference Manual*.

Transparent bridges are designed for expansion of slots and devices, to overcome electrical loading limits of the PCI bus. Transparent bridges assume that there is a host processor on the upstream (primary) side of the bridge, and do not require intelligence on the downstream (secondary) side. These bridges provide hierarchical configuration support and a flat address map. Transparent bridges adhere to the *PCI-to-PCI Bridge Architecture Specification*.

The 21554 embedded PCI-to-PCI bridge is designed to allow configuration and addressing isolation, so the local processor can effectively control the subsystem. Since the 21554 generates a secondary PCI bus that can support multiple PCI devices on an add-in card, technically it also provides some expansion (although not plug-and-play supported from the primary bus). The 21554 assumes that there is a processor both upstream and downstream of the bridge, although there may be transparent bridges between the processor and the 21554 on either side. It is possible to operate the 21554 without a processor on one side, but there are additional issues that arise that must be handled in a device-specific manner.

3.0 Transparency vs. Isolation Issues

This section describes the often conflicting requirements concerning transparency and isolation, from both a configuration and addressing viewpoint.

3.1 Hierarchy and Configuration

The 21554 is designed to break hierarchy. That is, the 21554 creates a configuration barrier by preventing the host (master) processor from enumerating buses or devices on its secondary side. This configuration barrier provided by the 21554 allows the local (slave) processor to have complete control of subsystem configuration without interference by the host processor. The 21554 does this by using a Type 0 configuration register format. When the standard BIOS or initialization code enumerates buses and devices, the code looks for a Type 1 configuration register format used by standard PCI-to-PCI bridges to indicate the presence of downstream buses and devices. When the initialization code encounters a Type 0 configuration header, it assumes that a PCI device was found and does not attempt to look behind it.

Therefore, an application cannot rely on plug-and-play initialization code for a processor to configure devices on the opposite side of the 21554, either upstream or downstream. The 21554 does not respond to Type 1 configuration transactions, nor does it forward configuration transactions of any kind from one bus to the other.

A mechanism does exist in the 21554 for hierarchical configuration of downstream or upstream devices, but device-specific initialization code is needed. The 21554 implements device specific registers that allow the 21554 to initiate configuration transactions on the opposite interface, upstream or downstream, using any address or data. Refer to the *21554 Hardware Reference Manual* for details on this feature.

Note: A general bus scan using the indirect configuration mechanism is not recommended as the 21554 does not respond to a transaction that it initiates. Therefore, the indirect configuration mechanism cannot be used to access a 21554 configuration register from the opposite interface.

The local processor has direct access to all 21554 configuration registers, while some registers are restricted from host (primary) access. Assuming the secondary interface of the 21554 connects to the processor on the card, which is the typical configuration for slave cards, then all configuration registers are accessible to that processor. Having the local processor perform both primary as well as secondary interface initialization requires device-specific code and is not plug-and-play compatible.

It is also possible to access all configuration registers using a combination of host (primary) access and serial ROM preload without the use of a local processor, as the serial ROM preload can initialize all configuration registers not accessible to the host. Again, the host must use device-specific code to properly initialize the 21554.

3.2   Addressing

Transparent PCI-to-PCI bridges use a flat address map, which is used for all PCI devices on either side of the bridge. Address windows are defined in the transparent PCI-to-PCI bridge for downstream transaction forwarding. Inverse decoding is used to forward upstream those transactions with addresses that fall outside of these windows. No address translation is used. Standard BIOS or initialization code automatically sets up these registers.

The 21554 creates independent address maps for both the primary and secondary bus domains. The 21554 uses base address registers (BARs) to designate both downstream and upstream forwarding windows, with other device-specific registers holding address translation information.   Typically, the serial ROM or local processor will set up the size and type of these BARs. The local processor will also set up the address translation registers and the map the BARs on the secondary interface used for upstream forwarding. The host processor is typically expected to only map the BARs on the primary interface, using plug-and-play BIOS or initialization code after local processor setup. However, in the application described here where the primary interface of the 21554 faces the backplane, device-specific code on the host processor card is needed to initialize the setup registers, address translation registers, and BARs from the secondary interface. Essentially, the host processor on the master card must also perform the local processor duties for the 21554 on its card.

4.0   Symmetry Issues

Typically, the 21554 assumes that a host processor is present on its primary interface and a local processor is present on the secondary interface. Using a card that implements the 21554 as both a slave and master card implies that the secondary interface of the 21554 on the master card connects to the processor, and the primary interface connects to the backplane. Therefore, none of the 21554 devices has a processor on the primary side since all connect to the backplane, and the host processor of this configuration is attempting to control and configure the system from the secondary side of the 21554.

In addition to the configuration issues mentioned previously, this configuration also creates issues around asymmetries between the primary and secondary interfaces in the 21554. There a number of asymmetric features in the 21554 architecture. These features are application dependent, some may have an effect, others may not.

4.1   Reset

The reset signal flows from the primary interface to the secondary interface. The primary reset, **p_rst_l**, is an input signal, the secondary reset, **s_rst_l**, is an output signal. The 21554 assumes a host-driven reset, and when the host system is reset, the subsystem is reset. There are other reset mechanisms, including a secondary reset bit and a chip reset bit, that also assert the secondary reset signal.

The 21554 cannot assert the primary reset signal and does not sample the secondary reset signal.

4.2 Configuration Lockout

The 21554 allows local processor configuration from the secondary interface before a host access is allowed by locking out the primary interface during this time. Primary bus transactions receive a target retry. This primary lockout is avoidable by clearing the primary lockout bit through the serial ROM preload.

4.3 I$_2$O Controller

The 21554's I$_2$O controller is oriented so that the IOP (I/O controller, or local processor) is on the secondary side and the host processor is on the primary side. However, if one assumes that the I$_2$O controllers are only used when the card is used as a slave card, then the 21554 I$_2$O controller on the master card can be disabled.

4.4 Clocks

Clocks are only an issue if the secondary clock output is used; otherwise the clock output can be disabled and the independent primary and secondary clocks can be used. Signal **s_clk_o** is a buffered version of the primary clock **p_clk**. When used, **s_clk_o** is externally buffered and is used for all secondary bus devices, including the 21554's secondary interface.

An external clock source is needed to supply the 21554 primary clock input facing the backplane.

4.5 Arbiter

The 21554 has an internal arbiter for the secondary bus. This arbiter can be disabled, and in its place, an external arbiter can be used if desired. However, external arbiters can be difficult to construct in PALs, and generally require additional loads on the FRAME#, IRDY#, CLK, and RST# signals.

An external arbiter is needed for the primary interface.

4.6 Central Functions

The 21554 drives the secondary signals AD[31:0], C/BE#[3:0], and PAR to 0 during reset. The 21554 also asserts the secondary signal REQ64# during the secondary bus reset. These functions can be disabled and performed externally.

The 21554 does not perform these functions on the primary bus. An external agent must assert the REQ64# signal on the primary bus during primary bus reset to enable the 64-bit interface.

4.7 Expansion ROM BAR

Parallel ROM access through the expansion ROM BAR register is supported only in the primary interface configuration register set. The only way that the parallel ROM can be accessed by the secondary interface is through device specific CSRs. However, if it is assumed that the expansion ROM is only used when the card is a slave card and not used when it is a master card, then this may not be an issue.

4.8 DAC Forwarding

The 21554 uses inverse decoding and does not perform address translation above the 4GB boundary. There is a 64-bit BAR for downstream forwarding, and the 21554 forwards all secondary bus DAC transactions outside of this range upstream. If 64-bit addressing is not used, this is not an issue. Otherwise, set up 64-bit addressing windows carefully!

4.9 Compact PCI Hot Swap

The 21554 assumes that the primary interface connects to the card edge. Upon insertion/removal, the 21554 design assumes that the local reset is ORed on the board with the primary bus reset and input to the **p_rst_l** (primary reset input) pin. The 21554, in turn, asserts **s_rst_l** to reset the subsystem. The enumeration notification interrupt signal, **p_enum_l**, is synchronized to the primary bus clock.

4.10 Power Management

21554 power management PME# support is designed with **s_pme_l** as an input signal on the secondary side and **p_pme_l** as an output signal on the primary side. Also, the 21554 interrupts a secondary bus interrupt (**s_inta_l**) to inform the subsystem that it has been moved from either the D1 or D2 power state to the D0 power state. If power management is not a requirement, this should not be an issue.

4.11 BAR variations

The 21554 primary and secondary base address register vary in the following ways:

- The first BAR at location 10h on the primary side can be configured to also forward downstream memory transactions in addition to mapping 21554 CSRs (primarily to support I$_2$O functionality). The corresponding BAR on the secondary side maps the 21554 CSRs only.

- The primary side implements a BAR that can be configured as a 64-bit BAR, the secondary does not (see Section 4.8).

- The secondary side implements a BAR that uses lookup table base address translation, the primary side does not.

4.12 Class Codes

The primary interface class code configuration register can be preloaded to reflect a vendor specific value. This class code is used to give the subsystem its class identity (for example, storage, network, and so on). The secondary side class code reads as "bridge, other" and cannot be modified.

5.0　Conclusion

With device-specific code and perhaps some special hardware, it can be possible to create a card using the 21554 that is versatile enough to function as both a master and slave card. However, a standard PCI-to-PCI Bridge has the transparency that the master card prefers, both in terms of a plug-and-play hierarchical configuration and a flat addressing model. By using a separate master card, the primary interface can be connected to the host processor and the secondary side to the card edge, which avoids many of the symmetry issues and takes advantage of the clocking, arbitration, and central functions provided on the secondary interface. (A standard PCI-to-PCI Bridge has more stringent requirements for having the host processor on the primary side of the bridge.)

The 21554 is particularly suited for slave cards where subsystem configuration and addressing isolation is desired.

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