21153 PCI-to-PCI Bridge

Brief Datasheet

Product Features

Intel's second-generation PCI-to-PCI bridge and is fully compliant with *PCI Local Bus Specification, Revision 2.1*. The 21153 has a 64-bit primary bus interface and a 32-bit secondary bus interface. The 64-bit interface interoperates transparently with either 64-bit or 32-bit devices. The 21153 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions.

- Complies fully with Revision 2.1 of the *PCI Local Bus Specification*
- Complies fully with Revision 1.1 of the *PCI-to-PCI Bridge Architecture Specification*
- Complies fully with the *PCI Bus Power Management Specification*
- Complies fully with the *Advanced Configuration Power Interface* (*ACPI*) *Specification*
- Provides enhanced address decoding:
  - — A 32-bit I/O address range
  - — A 32-bit memory-mapped I/O address range
  - — A 64-bit prefetchable memory address range
  - — ISA-aware mode for legacy support in the first 64KB of I/O address range
- Supports both 5-V and 3.3-V signaling environments
- Implements delayed transactions for all PCI configuration, I/O, and memory read commands—up to three transactions simultaneously in each direction
- Provides arbitration support for nine secondary bus devices:
  - — A programmable 2-level arbiter
  - — Hardware disable control, permitting use of an external arbiter
- Includes live insertion support
- VGA addressing and VGA palette snooping support
- Provides a 4-pin general purpose I/O interface, accessible through device-specific configuration space
- Supports 64-bit extension signals on the primary interface
- Allows 152 bytes of read data buffering upstream and 72 bytes of read buffering downstream
- Supports PCI transaction forwarding for the following commands:
  - — All I/O and memory commands
  - — Type 1 to Type 1 configuration commands
  - — Type 1 to Type 0 configuration commands (downstream only)
  - — All Type 1 to special cycle configuration commands
- Includes downstream lock support
- Allows 152 bytes of buffering (data and address) for upstream posted memory write commands and 88 bytes of buffering for downstream posted memory write commands
- Provides ten secondary clock outputs:
  - — Low skew, permitting direct drive of option slots
  - — Individual clock disables, capable of automatic configuration during reset
- Provides concurrent primary and secondary bus operation to isolate traffic and also a IEEE standard 1149.1 JTAG interface

Order Number: 278217-001
August 1998

Benefits

- 64-bit primary and 32-bit secondary interfaces enable the high performance, expandable systems, adapter cards, and embedded devices.
- Increases the number of PCI slots that can be supported in a system.
- Enables multicomponent card designs.
- Enhanced PCI bridge performance and efficiency through support for delayed transactions.
- Arbiter clock support for up to nine devices on the secondary bus through onchip logic.

Description

The 21153 has separate posted write, read data, and delayed transaction queues with more significant buffering capability than first-generation bridges. In addition, the 21153 supports buffering of simultaneous, multiple, posted write and delayed transactions in both directions.

Among the new features provided by the 21153 are:

- A programmable 2-level secondary bus arbiter
- An IEEE standard 1149.1 JTAG interface
- Live insertion support
- A 4-pin general-purpose I/O interface
- Individual secondary clock disables
- Enhanced address decoding.

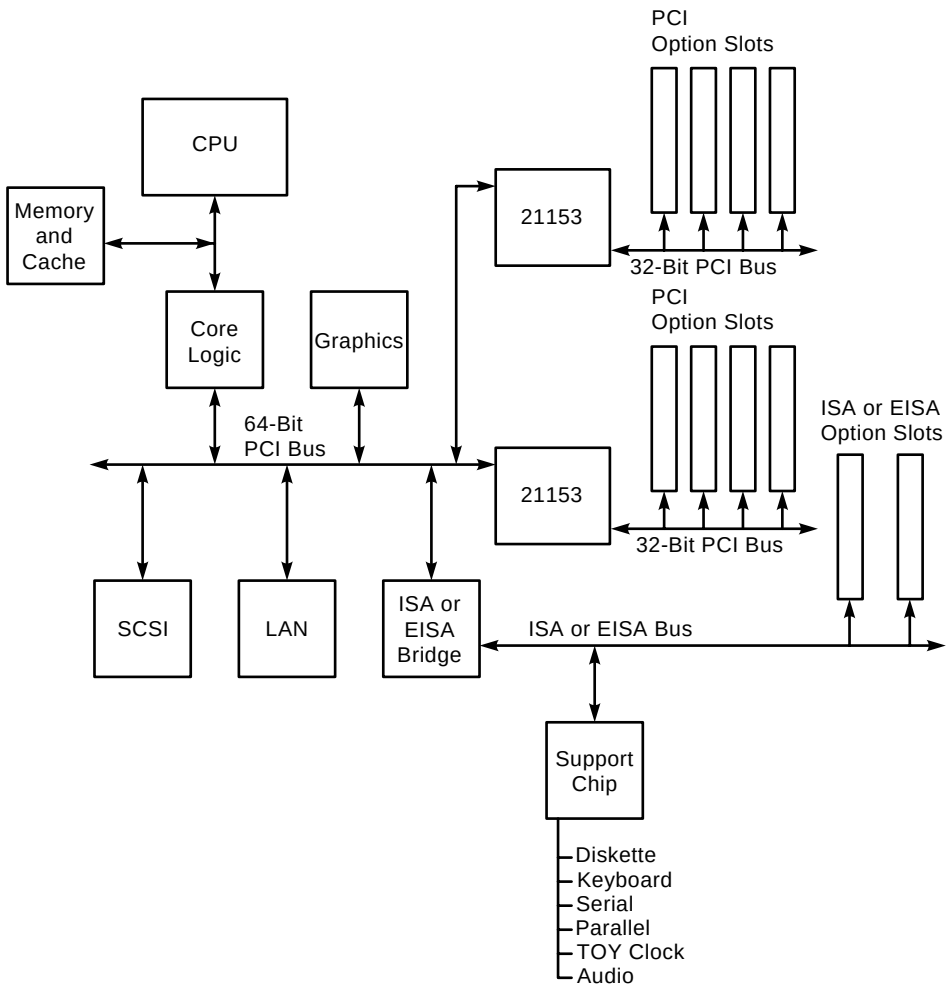
The 21153 has sufficient clock and arbitration pins to support nine PCI bus master devices directly on its secondary interface.

The 21153 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications such as multimedia.

21153 Applications

The 21153 makes it possible to extend a system's load capability limit beyond that of a single PCI bus by allowing motherboard designers to add more PCI devices, or more PCI option card slots, than a single PCI bus can support. Figure 1, the system card block diagram, illustrates the use of two 21153 PCI-to-PCI bridges on a system board. Each 21153 that is added to the board creates a new PCI bus that provides support for the additional PCI slots or devices.

Figure 1. System Card Block Diagram

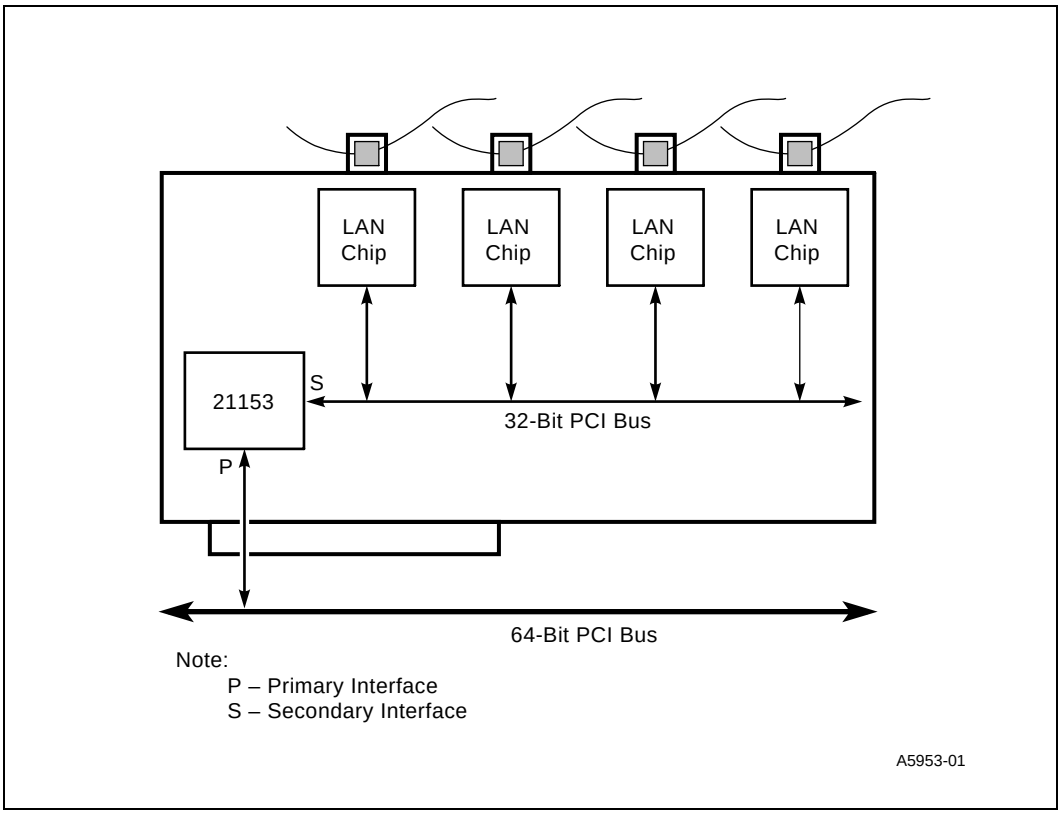


A5948-01

Multidevice PCI Option Cards

Option card designers can use the 21153 to implement multiple-device PCI option cards. Without a PCI-to-PCI bridge, PCI loading rules would limit option cards to one device. The *PCI Local Bus Specification* loading rules limit PCI option cards to a single connection per PCI signal in the option card connector. However, the 21153 overcomes this restriction by providing, on the option card, an independent PCI bus to which up to four devices can be attached. Figure 2, the 21153 option card diagram, shows how the 21153 enables the design of a multi-component option card.

Figure 2. 21153 PCI-to-PCI Bridge with Option Cards



21153 Characteristics	
Characteristic	Specification
Power supply	Vdd 3.3 V Vdd_clamp=5 V or 3.3 V
Operating temperature	Tj maximum=125°C
Storage temperature range	–55°C min. to +125°C max.
Power dissipation (typical)	1.7 W @ Vdd=3.3 V with 33-MHz PCI Clock
Package	256-pin PBGA

Support, Products, and Documentation

If you need technical support, a *Product Catalog*, or help deciding which documentation best meets your needs, visit the Intel World Wide Web Internet site:

http://www.intel.com

Copies of documents that have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling **1-800-332-2717** or by visiting Intel's website for developers at:

http://developer.intel.com

You can also contact the Intel Massachusetts Information Line or the Intel Massachusetts Customer Technology Center. Please use the following information lines for support:

For documentation and general information:	
Intel Massachusetts Information Line	
United States:	1–800–332–2717
Outside United States:	1–303-675-2148
Electronic mail address:	techdoc@intel.com

For technical support:	
Intel Massachusetts Customer Technology Center	
Phone (U.S. and international):	1–978–568–7474
Fax:	1–978–568–6698
Electronic mail address:	techsup@intel.com